Low-Power, Precision Analog Microcontroller, Dual Sigma-Delta ADCs

Silicon Anomaly List – Rev D Silicon

ADuC7060/61

This anomaly list describes the known bugs, anomalies and work-arounds for the ADuC7060/61MicroConverter® Revision A silicon. The anomalies listed apply to all ADuC7060/61 packaged material branded as follows:

First Line	ADuC7060/61 (where: x = 0 to 1)
Third Line	D30 or newer (revision identifier)

Analog Devices, Inc. is committed, through future silicon revisions, to continuously improve silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

ADuC7060/61FUNCTIONALITY ISSUES

Silicon Revision Identifier	Kernel Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Anomalies
		All silicon branded D30	Released	Rev. A	7

RevA

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ANOMALIES

ADuC7060/61 Functionality Issues

1. External IRQ when configured as level sensitive [er002]:

Background:	There are four External Interrupt sources on the ADuC7060/61parts. These can be configured as edge triggered (rising or falling), or level triggered (active high or active low).
Issue:	When any of the External Interrupt Sources are configured as level triggered, either active high or active low, the external pin must remain at the active level until the program vectors to the interrupt vector handler for that external interrupt. If the external pin is activated triggering an interrupt but subsequently goes to an inactive level before the program vectors to the interrupt handler, the IRQSTA bit for the external interrupt may not be set. This will result in the interrupt handler not knowing what interrupt source caused the part to vector to the interrupt vector.
Workaround:	Edge triggered interrupts don't have this problem. A fix is pending for this issue.
Related Issues:	None.

2. DAC output limited to AVdd-250mV [er005]:

Background:	The DAC output range can be configured to four different settings: - 0 V to V_{REF} (1.2 V) range. Internal reference source - VREF– to VREF+. - ADC5/EXT_REF2IN– to ADC4/EXT_REF2IN+. - 0 V to AVDD
Issue:	The DAC output buffer is limited in the maximum output voltage that it can drive to AVdd-250mV. This is less than the datasheet specification.
Workaround:	A fix is pending for this issue.
Related Issues:	None.

SECTION 1. ADUC7060/61 FUNCTIONALITY ISSUES

Reference Number	Description	Status
er001	Power Down Mode Issue	Fixed on Rev C and later Silicon
er002	External IRQ when configured as level sensitive	Open
er003	SPI issue in Slave mode when the SPI Clock Phase bit is set	Fixed on Rev C and later Silicon
er004	Primary ADC Self-Gain Calibration mode	Fixed on Rev C and later Silicon
er005	DAC output limited to AVdd-250mV	Open

SECTION 2. ADUC7060/61 PERFORMANCE RELATED ISSUES

Reference Number	Description	Status
pr001	DAC Relative Accuracy when the output range is greater than 0V- 1.2V	Fixed on Rev C and later Silicon

SECTION 3. ADUC7060/61SILICON FUTURE ENHANCEMENTS

Reference Number	Description	Status
fe001	Primary ADC input buffer Bypass	Fixed on Rev C and later Silicon

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