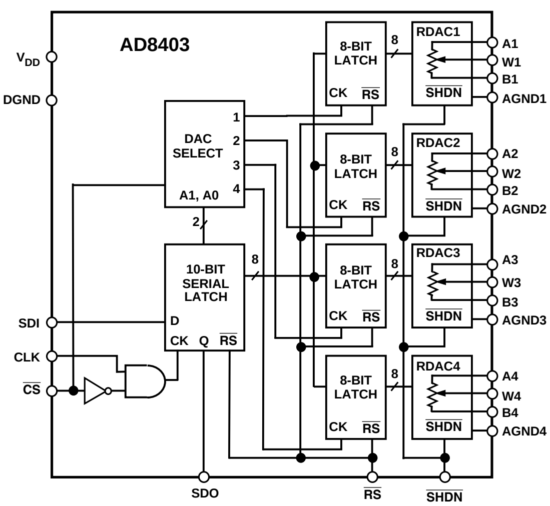
1-/2-/4-Channel Digital Potentiometers

AD8400/AD8402/AD8403

FEATURES
256 Position
Replaces 1, 2 or 4 Potentiometers
1 kΩ, 10 kΩ, 50 kΩ, 100 kΩ
Power Shut Down—Less than 5 μA
3-Wire SPI Compatible Serial Data Input
10 MHz Update Data Loading Rate
+2.7 V to +5.5 V Single-Supply Operation
Midscale Preset

APPLICATIONS
Mechanical Potentiometer Replacement
Programmable Filters, Delays, Time Constants
Volume Control, Panning
Line Impedance Matching
Power Supply Adjustment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD8400/AD8402/AD8403 provide a single, dual or quad channel, 256 position digitally controlled variable resistor (VR) device. These devices perform the same electronic adjustment function as a potentiometer or variable resistor. The AD8400 contains a single variable resistor in the compact SO-8 package. The AD8402 contains two independent variable resistors in space saving SO-14 surface mount package. The AD8403 contains four independent variable resistors in 24-lead PDIP, SOIC and TSSOP packages. Each part contains a fixed resistor with a wiper contact that taps the fixed resistor value at a point determined by a digital code loaded into the controlling serial input register. The resistance between the wiper and either endpoint of the fixed resistor varies linearly with respect to the digital code transferred into the VR latch. Each variable resistor offers a completely programmable value of resistance, between the A terminal and the wiper or the B terminal and the wiper. The fixed A to B terminal resistance of 1 kΩ, 10 kΩ, 50 kΩ or 100 kΩ has a ±1% channel-to-channel matching tolerance with a nominal temperature coefficient of 500 ppm/°C. A unique switching circuit minimizes the high glitch inherent in traditional switched resistor designs avoiding any make-before-break or break-before-make operation.

Each VR has its own VR latch that holds its programmed resistance value. These VR latches are updated from an SPI compatible serial-to-parallel shift register that is loaded from a standard 3-wire serial-input digital interface. Ten data bits make up the data word clocked into the serial input register. The data word is decoded where the first two bits determine the address of the VR latch to be loaded, the last eight bits are data. A serial data output pin at the opposite end of the serial register allows simple daisy-chaining in multiple VR applications without additional external decoding logic.

The reset ($\overline{RS}$) pin forces the wiper to the midscale position by loading 80_H into the VR latch. The $\overline{SHDN}$ pin forces the resistor to an end-to-end open circuit condition on the A terminal and shorts the wiper to the B terminal, achieving a microwatt power shutdown state. When $\overline{SHDN}$ is returned to logic high, the previous latch settings put the wiper in the same resistance setting prior to shutdown. The digital interface is still active in shutdown so that code changes can be made which will produce new wiper positions when the device is taken out of shutdown.

The AD8400 is available in both the SO-8 surface mount and the 8-lead plastic DIP package.

The AD8402 is available in both surface mount (SO-14) and the 14-lead plastic DIP package, while the AD8403 is available in a narrow body 24-lead plastic DIP and the 24-lead surface mount package. The AD8402/AD8403 are also offered in the 1.1 mm thin TSSOP-14/TSSOP-24 package for PCMCIA applications. All parts are guaranteed to operate over the extended industrial temperature range of –40°C to +85°C.

REV. B

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AD8400/AD8402/AD8403–SPECIFICATIONS

10 kΩ VERSION

ELECTRICAL CHARACTERISTICS (V_{DD} = +3 V ± 10% or + 5 V ± 10%, V_A = $+V_{DD}$, V_B = 0 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
DC CHARACTERISTICS RHEOSTAT MODE Specifications Apply to All VRs						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A = NC	–1	±1/4	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A = NC	–2	±1/2	+2	LSB
Nominal Resistance[3]	R	T_A = +25°C, Model: AD840XYY10	8	10	12	kΩ
Resistance Tempco	$\Delta R_{AB}/\Delta T$	$V_{AB} = V_{DD}$, Wiper = No Connect		500		ppm/°C
Wiper Resistance	R_W	I_W = 1 V/R		50	100	Ω
Nominal Resistance Match	$\Delta R/R_O$	CH 1 to 2, 3, or 4, $V_{AB} = V_{DD}$, T_A = +25°C		0.2	1	%
DC CHARACTERISTICS POTENTIOMETER DIVIDER Specifications Apply to All VRs						
Resolution	N		8			Bits
Integral Nonlinearity[4]	INL		–2	±1/2	+2	LSB
Differential Nonlinearity[4]	DNL	V_{DD} = +5 V	–1	±1/4	+1	LSB
	DNL	V_{DD} = +3 V T_A = +25°C	–1	±1/4	+1	LSB
	DNL	V_{DD} = +3 V T_A = –40°C, +85°C	–1.5	±1/2	+1.5	LSB
Voltage Divider Tempco	$\Delta V_W/\Delta T$	Code = 80_H		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = FF_H	–4	–2.8	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 00_H	0	+1.3	+2	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A, B, W}$		0		V_{DD}	V
Capacitance[6] Ax, Bx	$C_{A, B}$	f = 1 MHz, Measured to GND, Code = 80_H		75		pF
Capacitance[6] Wx	C_W	f = 1 MHz, Measured to GND, Code = 80_H		120		pF
Shutdown Current[7]	I_{A_SD}	$V_A = V_{DD}$, V_B = 0 V, $\overline{SHDN}$ = 0		0.01	5	µA
Shutdown Wiper Resistance	R_{W_SD}	$V_A = V_{DD}$, V_B = 0 V, $\overline{SHDN}$ = 0, V_{DD} = +5 V		100	200	Ω
DIGITAL INPUTS & OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = +5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = +5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = +3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = +3 V			0.6	V
Output Logic High	V_{OH}	R_L = 1 kΩ to V_{DD}	V_{DD}–0.1			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{DD} = +5 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or +5 V, V_{DD} = +5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD} Range		2.7		5.5	V
Supply Current (CMOS)	I_{DD}	$V_{IH} = V_{DD}$ or V_{IL} = 0 V		0.01	5	µA
Supply Current (TTL)[8]	I_{DD}	V_{IH} = 2.4 V or 0.8 V, V_{DD} = +5.5 V		0.9	4	mA
Power Dissipation (CMOS)[9]	P_{DISS}	$V_{IH} = V_{DD}$ or V_{IL} = 0 V, V_{DD} = +5.5 V			27.5	µW
Power Supply Sensitivity	PSS	V_{DD} = +5 V ± 10%		0.0002	0.001	%/%
	PSS	V_{DD} = +3 V ± 10%		0.006	0.03	%/%
DYNAMIC CHARACTERISTICS[6, 10]						
Bandwidth –3 dB	BW_10K	R = 10 kΩ		600		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms + 2 V dc, V_B = 2 V dc, f = 1 kHz		0.003		%
V_W Settling Time	t_S	$V_A = V_{DD}$, V_B = 0 V, ±1% Error Band		2		µs
Resistor Noise Voltage	e_{NWB}	R_{WB} = 5 kΩ, f = 1 kHz, $\overline{RS}$ = 0		9		nV/√Hz
Crosstalk[11]	C_T	$V_A = V_{DD}$, V_B = 0 V		–65		dB

NOTES FOR 10 kΩ VERSION

[1] Typicals represent average readings at +25°C and V_{DD} = +5 V.

[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. See Figure 30 test circuit. I_W = 50 µA for V_{DD} = +3 V and I_W = 400 µA for V_{DD} = +5 V for the 10 kΩ versions.

[3] $V_{AB} = V_{DD}$, Wiper (V_W) = No Connect.

[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and V_B = 0 V. DNL Specification limits of ±1 LSB maximum are Guaranteed Monotonic operating conditions. See Figure 29 test circuit.

[5] Resistor terminals A, B, W have no limitations on polarity with respect to each other.

[6] Guaranteed by design and not subject to production test. Resistor-terminal capacitance tests are measured with 2.5 V bias on the measured terminal. The remaining resistor terminals are left open circuit.

[7] Measured at the Ax terminals. All Ax terminals are open circuited in shutdown mode.

[8] Worst case supply current consumed when input logic level at 2.4 V, standard characteristic of CMOS logic. See Figure 21 for a plot of I_{DD} versus logic voltage.

[9] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.

[10] All Dynamic Characteristics use V_{DD} = +5 V.

[11] Measured at a V_W pin where an adjacent V_W pin is making a full-scale voltage change.

Specifications subject to change without notice.

SPECIFICATIONS

50 kΩ & 100 kΩ VERSION ELECTRICAL CHARACTERISTICS

(V_{DD} = +3 V ± 10% or + 5 V ± 10%, V_A = +V_{DD}, V_B = 0 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
DC CHARACTERISTICS RHEOSTAT MODE Specifications Apply to All VRs						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A = NC	–1	±1/4	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A = NC	–2	±1/2	+2	LSB
Nominal Resistance[3]	R	T_A = +25°C, Model: AD840XYY50	35	50	65	kΩ
	R	T_A = +25°C, Model: AD840XYY100	70	100	130	kΩ
Resistance Tempco	$\Delta R_{AB}/\Delta T$	V_{AB} = V_{DD}, Wiper = No Connect		500		ppm/°C
Wiper Resistance	R_W	I_W = 1 V/R		53	100	Ω
Nominal Resistance Match	$\Delta R/R_O$	CH 1 to 2, 3, or 4, V_{AB} = V_{DD}, T_A = +25°C		0.2	1	%
DC CHARACTERISTICS POTENTIOMETER DIVIDER Specifications Apply to All VRs						
Resolution	N		8			Bits
Integral Nonlinearity[4]	INL		–4	±1	+4	LSB
Differential Nonlinearity[4]	DNL	V_{DD} = +5 V	–1	±1/4	+1	LSB
	DNL	V_{DD} = +3 V T_A = +25°C	–1	±1/4	+1	LSB
	DNL	V_{DD} = +3 V T_A = –40°C, +85°C	–1.5	±1/2	+1.5	LSB
Voltage Divider Tempco	$\Delta V_W/\Delta T$	Code = 80_H		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = FF_H	–1	–0.25	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 00_H	0	+0.1	+1	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A, B, W}$		0		V_{DD}	V
Capacitance[6] Ax, Bx	$C_{A, B}$	f = 1 MHz, Measured to GND, Code = 80_H		15		pF
Capacitance[6] Wx	C_W	f = 1 MHz, Measured to GND, Code = 80_H		80		pF
Shutdown Current[7]	I_{A_SD}	V_A = V_{DD}, V_B = 0 V, $\overline{SHDN}$ = 0		0.01	5	µA
Shutdown Wiper Resistance	R_{W_SD}	V_A = V_{DD}, V_B = 0 V, $\overline{SHDN}$ = 0, V_{DD} = +5 V		100	200	Ω
DIGITAL INPUTS & OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = +5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = +5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = +3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = +3 V			0.6	V
Output Logic High	V_{OH}	R_L = 1 kΩ to V_{DD}	V_{DD}–0.1			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{DD} = +5 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or +5 V, V_{DD} = +5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD} Range		2.7		5.5	V
Supply Current (CMOS)	I_{DD}	V_{IH} = V_{DD} or V_{IL} = 0 V		0.01	5	µA
Supply Current (TTL)[8]	I_{DD}	V_{IH} = 2.4 V or 0.8 V, V_{DD} = +5.5 V		0.9	4	mA
Power Dissipation (CMOS)[9]	P_{DISS}	V_{IH} = V_{DD} or V_{IL} = 0 V, V_{DD} = +5.5 V			27.5	µW
Power Supply Sensitivity	PSS	V_{DD} = +5 V ± 10%		0.0002	0.001	%/%
	PSS	V_{DD} = +3 V ± 10%		0.006	0.03	%/%
DYNAMIC CHARACTERISTICS[6, 10]						
Bandwidth –3 dB	BW_50K	R = 50 kΩ		125		kHz
	BW_100K	R = 100 kΩ		71		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms + 2 V dc, V_B = 2 V dc, f = 1 kHz		0.003		%
V_W Settling Time	t_S_50K	V_A = V_{DD}, V_B = 0 V, ±1% Error Band		9		µs
	t_S_100K	V_A = V_{DD}, V_B = 0 V, ±1% Error Band		18		µs
Resistor Noise Voltage	e_{NWB}_50K	R_{WB} = 25 kΩ, f = 1 kHz, $\overline{RS}$ = 0		20		nV/√Hz
	e_{NWB}_100K	R_{WB} = 50 kΩ, f = 1 kHz, $\overline{RS}$ = 0		29		nV/√Hz
Crosstalk[11]	C_T	V_A = V_{DD}, V_B = 0 V		–65		dB

NOTES FOR 50 kΩ and 100 kΩ VERSIONS

1 Typicals represent average readings at +25°C and V_{DD} = +5 V.

2 Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. See Figure 30 test circuit. I_W = V_{DD}/R for V_{DD} = +3 V or +5 V for the 50 kΩ and 100 kΩ versions.

3 V_{AB} = V_{DD}, Wiper (V_W) = No Connect.

4 INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. V_A = V_{DD} and V_B = 0 V. DNL Specification limits of ±1 LSB maximum are Guaranteed Monotonic operating conditions. See Figure 29 test circuit.

5 Resistor terminals A, B, W have no limitations on polarity with respect to each other.

6 Guaranteed by design and not subject to production test. Resistor-terminal capacitance tests are measured with 2.5 V bias on the measured terminal. The remaining resistor terminals are left open circuit.

7 Measured at the Ax terminals. All Ax terminals are open circuited in shutdown mode.

8 Worst case supply current consumed when input logic level at 2.4 V, standard characteristic of CMOS logic. See Figure 21 for a plot of I_{DD} versus logic voltage.

9 P_{DISS} is calculated from (I_{DD} × V_{DD}). CMOS logic level inputs result in minimum power dissipation.

10 All Dynamic Characteristics use V_{DD} = +5 V.

11 Measured at a V_W pin where an adjacent V_W pin is making a full-scale voltage change.

Specifications subject to change without notice.

AD8400/AD8402/AD8403–SPECIFICATIONS

1 kΩ VERSION

ELECTRICAL CHARACTERISTICS (V_{DD} = +3 V ± 10% or + 5 V ± 10%, V_A = +V_{DD}, V_B = 0 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
DC CHARACTERISTICS RHEOSTAT MODE Specifications Apply to All VRs						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A = NC	–5	–1	+3	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A = NC	–4	±1.5	+4	LSB
Nominal Resistance[3]	R	T_A = +25°C, Model: AD840XYY1	0.8	1.2	1.5	kΩ
Resistance Tempco	$\Delta R_{AB}/\Delta T$	V_{AB} = V_{DD}, Wiper = No Connect		700		ppm/°C
Wiper Resistance	R_W	I_W = 1 V/R_{AB}		53	100	Ω
Nominal Resistance Match	$\Delta R/R_O$	CH 1 to 2, V_{AB} = V_{DD}, T_A = +25°C		0.75	2	%
DC CHARACTERISTICS POTENTIOMETER DIVIDER Specifications Apply to All VRs						
Resolution	N		8			Bits
Integral Nonlinearity[4]	INL		–6	±2	+6	LSB
Differential Nonlinearity[4]	DNL	V_{DD} = +5 V	–4	–1.5	+2	LSB
	DNL	V_{DD} = +3 V, T_A = +25°C	–5	–2	+5	LSB
Voltage Divider Temperature Coefficent	$\Delta V_W/\Delta T$	Code = 80_H		25		ppm/°C
Full-Scale Error	V_{WFSE}	Code = FF_H	–20	–12	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 00_H	0	6	10	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A, B, W}$		0		V_{DD}	V
Capacitance[6] Ax, Bx	$C_{A, B}$	f = 1 MHz, Measured to GND, Code = 80_H		75		pF
Capacitance[6] Wx	C_W	f = 1 MHz, Measured to GND, Code = 80_H		120		pF
Shutdown Supply Current[7]	I_{DD_SD}	V_A = V_{DD}, V_B = 0 V, $\overline{SHDN}$ = 0		0.01	5	µA
Shutdown Wiper Resistance	R_{W_SD}	V_A = V_{DD}, V_B = 0 V, $\overline{SHDN}$ = 0, V_{DD} = +5 V		50	100	Ω
DIGITAL INPUTS & OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = +5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = +5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = +3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = +3 V			0.6	V
Output Logic High	V_{OH}	R_L = 1 kΩ to V_{DD}	V_{DD}–0.1			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{DD} = +5 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or +5 V, V_{DD} = +5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD} Range		2.7		5.5	V
Supply Current (CMOS)	I_{DD}	V_{IH} = V_{DD} or V_{IL} = 0 V		0.01	5	µA
Supply Current (TTL)[8]	I_{DD}	V_{IH} = 2.4 V or 0.8 V, V_{DD} = +5.5 V		0.9	4	mA
Power Dissipation (CMOS)[9]	P_{DISS}	V_{IH} = V_{DD} or V_{IL} = 0 V, V_{DD} = +5.5 V			27.5	µW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5 V ± 10%		0.0035	0.008	%/%
	PSS	ΔV_{DD} = +3 V ± 10%		0.05	0.13	%/%
DYNAMIC CHARACTERISTICS[6, 10]						
Bandwidth –3 dB	BW_1K	R = 1 kΩ		5,000		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms + 2 V dc, V_B = 2 V dc, f = 1 kHz		0.015		%
V_W Settling Time	t_S	V_A = V_{DD}, V_B = 0 V, ±1% Error Band		0.5		µs
Resistor Noise Voltage	e_{NWB}	R_{WB} = 500 Ω, f = 1 kHz, $\overline{RS}$ = 0		3		nV/√Hz
Crosstalk[11]	C_T	V_A = V_{DD}, V_B = 0 V		–65		dB

NOTES FOR 1 kΩ VERSION

[1] Typicals represent average readings at +25°C and V_{DD} = +5 V.

[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. See Figure 30 test circuit.
I_W = 500 µA for V_{DD} = +3 V and I_W = 4 mA for V_{DD} = +5 V for 1 kΩ version.

[3] V_{AB} = V_{DD}, Wiper (V_W) = No Connect.

[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. V_A = V_{DD} and V_B = 0 V. DNL Specification limits of ±1 LSB maximum are Guaranteed Monotonic operating conditions. See Figure 29 test circuit.

[5] Resistor terminals A, B, W have no limitations on polarity with respect to each other.

[6] Guaranteed by design and not subject to production test. Resistor-terminal capacitance tests are measured with 2.5 V bias on the measured terminal. The remaining resistor terminals are left open circuit.

[7] Measured at the Ax terminals. All Ax terminals are open circuited in shutdown mode.

[8] Worst case supply current consumed when input logic level at 2.4 V, standard characteristic of CMOS logic. See Figure 21 for a plot of I_{DD} versus logic voltage.

[9] P_{DISS} is calculated from (I_{DD} × V_{DD}). CMOS logic level inputs result in minimum power dissipation.

[10] All Dynamic Characteristics use V_{DD} = +5 V.

[11] Measured at a V_W pin where an adjacent V_W pin is making a full-scale voltage change.

Specifications subject to change without notice.

AD8400/AD8402/AD8403–SPECIFICATIONS

All VERSIONS

ELECTRICAL CHARACTERISTICS (V_{DD} = +3 V ± 10% or + 5 V ± 10%, V_A = +V_{DD}, V_B = 0 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
SWITCHING CHARACTERISTICS[2, 3]						
Input Clock Pulse Width	t_{CH}, t_{CL}	Clock Level High or Low	10			ns
Data Setup Time	t_{DS}		5			ns
Data Hold Time	t_{DH}		5			ns
CLK to SDO Propagation Delay[4]	t_{PD}	R_L = 1 kΩ to +5 V, C_L ≤ 20 pF	1		25	ns
$\overline{CS}$ Setup Time	t_{CSS}		10			ns
$\overline{CS}$ High Pulse Width	t_{CSW}		10			ns
Reset Pulse Width	t_{RS}		50			ns
CLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
$\overline{CS}$ Rise to Clock Rise Setup	t_{CS1}		10			ns

NOTES
[1]Typicals represent average readings at +25°C and V_{DD} = +5 V.
[2]Guaranteed by design and not subject to production test. Resistor-terminal capacitance tests are measured with 2.5 V bias on the measured terminal. The remaining resistor terminals are left open circuit.
[3]See timing diagram for location of measured values. All input control voltages are specified with t_R = t_F = 1 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. Switching characteristics are measured using V_{DD} = +3 V or +5 V. To avoid false clocking a minimum input logic slew rate of 1 V/µs should be maintained.
[4]Propagation Delay depends on value of V_{DD}, R_L and C_L–see applications text.
Specifications subject to change without notice.

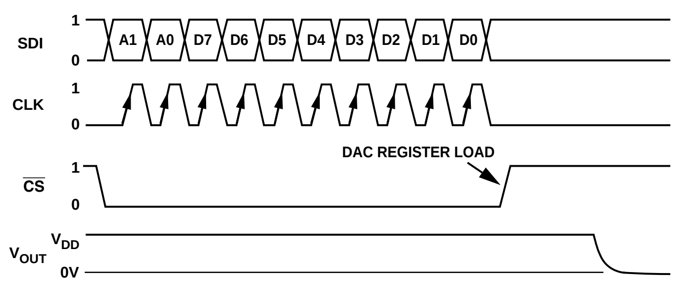


Figure 1a. Timing Diagram

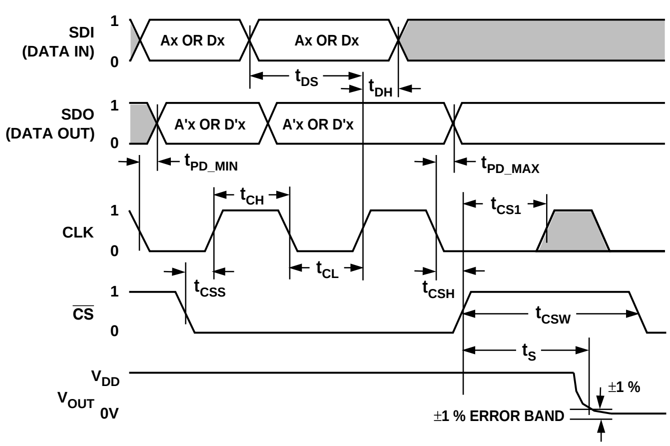


Figure 1b. Detail Timing Diagram

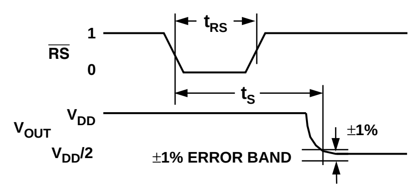


Figure 1c. Reset Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C, unless otherwise noted)

V_{DD} to GND . . . . –0.3 V, +8 V
V_A, V_B, V_W to GND . . . . 0 V, V_{DD}
A_X–B_X, A_X–W_X, B_X–W_X . . . . ±20 mA
Digital Input and Output Voltage to GND . . . . 0 V, +8 V
Operating Temperature Range . . . . –40°C to +85°C
Maximum Junction Temperature (T_J max) . . . . +150°C
Storage Temperature . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . +300°C
Package Power Dissipation . . . . (T_J max–T_A)/θ_{JA}
Thermal Resistance (θ_{JA})
  P-DIP (N-14) . . . . +83°C/W
  P-DIP (N-24) . . . . +63°C/W
  SOIC (SO-14) . . . . +70°C/W
  SOIC (SOL-24) . . . . +120°C/W
  TSSOP-14 (RU-14) . . . . +180°C/W
  TSSOP-24 (RU-24) . . . . +143°C/W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8400/AD8402/AD8403 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

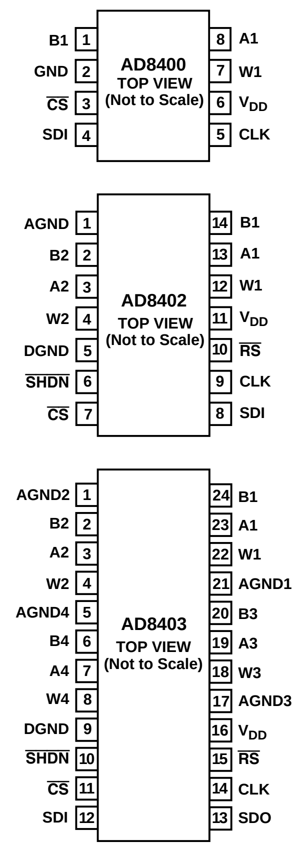
Model	#CHs/ kΩ	Temperature Range	Package Description	Package Option*
AD8400AN10	X1/10	-40°C to +85°C	PDIP-8	N-8
AD8400AR10	X1/10	-40°C to +85°C	SO-8	SO-8
AD8402AN10	X2/10	-40°C to +85°C	PDIP-14	N-14
AD8402AR10	X2/10	-40°C to +85°C	SO-14	SO-14
AD8402ARU10	X2/10	-40°C to +85°C	TSSOP-14	RU-14
AD8403AN10	X4/10	-40°C to +85°C	PDIP-24	N-24
AD8403AR10	X4/10	-40°C to +85°C	SOIC-24	SOL-24
AD8403ARU10	X4/10	-40°C to +85°C	TSSOP-24	RU-24
AD8400AN50	X1/50	-40°C to +85°C	PDIP-8	N-8
AD8400AR50	X1/50	-40°C to +85°C	SO-8	SO-8
AD8402AN50	X2/50	-40°C to +85°C	PDIP-14	N-14
AD8402AR50	X2/50	-40°C to +85°C	SO-14	SO-14
AD8403AN50	X4/50	-40°C to +85°C	PDIP-24	N-24
AD8403AR50	X4/50	-40°C to +85°C	SOIC-24	SOL-24
AD8400AN100	X1/100	-40°C to +85°C	PDIP-8	N-8
AD8400AR100	X1/100	-40°C to +85°C	SO-8	SO-8
AD8402AN100	X2/100	-40°C to +85°C	PDIP-14	N-14
AD8402AR100	X2/100	-40°C to +85°C	SO-14	SO-14
AD8402ARU100	X2/100	-40°C to +85°C	TSSOP-14	RU-14
AD8403AN100	X4/100	-40°C to +85°C	PDIP-24	N-24
AD8403AR100	X4/100	-40°C to +85°C	SOIC-24	SOL-24
AD8403ARU100	X4/100	-40°C to +85°C	TSSOP-24	RU-24
AD8400AN1	X1/1	-40°C to +85°C	PDIP-8	N-8
AD8400AR1	X1/1	-40°C to +85°C	SO-8	SO-8
AD8402AN1	X2/1	-40°C to +85°C	PDIP-14	N-14
AD8402AR1	X2/1	-40°C to +85°C	SO-14	SO-14
AD8403AN1	X4/1	-40°C to +85°C	PDIP-24	N-24
AD8403AR1	X4/1	-40°C to +85°C	SOIC-24	SOL-24
AD8403ARU1	X4/1	-40°C to +85°C	TSSOP-24	RU-24

*N = Plastic DIP; SO = Small Outline; RU = Thin Shrink SO.
The AD8400, AD8402 and the AD8403 contain 720 transistors.

Table I. Serial Data Word Format

ADDR		DATA							
B9	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
MSB	LSB	MSB							LSB
2^9	2^8	2^7							2^0

PIN CONFIGURATIONS



AD8400 PIN DESCRIPTIONS

Pin	Name	Description
1	B1	Terminal B RDAC
2	GND	Ground
3	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high data in the serial input register is loaded into the DAC register.
4	SDI	Serial Data Input
5	CLK	Serial Clock Input, positive edge triggered
6	V_{DD}	Positive power supply, specified for operation at both +3 V and +5 V.
7	W1	Wiper RDAC, addr = 00_2
8	A1	Terminal A RDAC

AD8402 PIN DESCRIPTIONS

Pin	Name	Description
1	AGND	Analog Ground*
2	B2	Terminal B RDAC #2
3	A2	Terminal A RDAC #2
4	W2	Wiper RDAC #2, Addr = 01_2
5	DGND	Digital Ground*
6	$\overline{SHDN}$	Terminal A open circuit. Shutdown controls Variable Resistors #1 and #2
7	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high data in the serial input register is decoded based on the address bits and loaded into the target DAC register.
8	SDI	Serial Data Input
9	CLK	Serial Clock Input, positive edge triggered
10	$\overline{RS}$	Active low reset to midscale; sets RDAC registers to 80_H
11	V_{DD}	Positive power supply, specified for operation at both +3 V and +5 V
12	W1	Wiper RDAC #1, addr = 00_2
13	A1	Terminal A RDAC #1
14	B1	Terminal B RDAC #1

*All AGNDs must be connected to DGND.

AD8403 PIN DESCRIPTIONS

Pin	Name	Description
1	AGND2	Analog Ground #2*
2	B2	Terminal B RDAC #2
3	A2	Terminal A RDAC #2
4	W2	Wiper RDAC #2, addr = 01_2
5	AGND4	Analog Ground #4*
6	B4	Terminal B RDAC #4
7	A4	Terminal A RDAC #4
8	W4	Wiper RDAC #4, addr = 11_2
9	DGND	Digital Ground*
10	$\overline{SHDN}$	Active Low Input. Terminal A open circuit. Shutdown controls variable resistors #1 through #4
11	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high data in the serial input register is decoded based on the address bits and loaded into the target DAC register.
12	SDI	Serial Data Input
13	SDO	Serial Data Output, Open Drain transistor requires pull-up resistor
14	CLK	Serial Clock Input, positive edge triggered
15	$\overline{RS}$	Active low reset to midscale; sets RDAC registers to 80_H
16	V_{DD}	Positive power supply, specified for operation at both +3 V and +5 V
17	AGND3	Analog Ground #3*
18	W3	Wiper RDAC #3, addr = 10_2
19	A3	Terminal A RDAC #3
20	B3	Terminal B RDAC #3
21	AGND1	Analog Ground #1*
22	W1	Wiper RDAC #1, addr = 00_2
23	A1	Terminal A RDAC #1
24	B1	Terminal B RDAC #1

*All AGNDs must be connected to DGND.

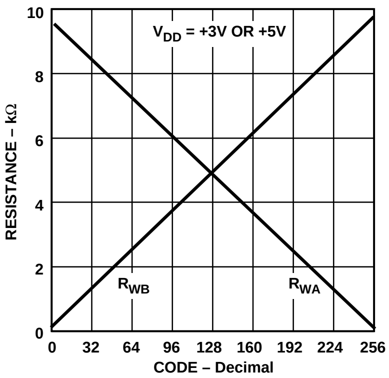


Figure 2. Wiper to End Terminal Resistance vs. Code

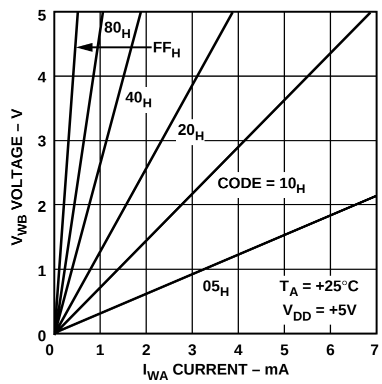


Figure 3. Resistance Linearity vs. Conduction Current

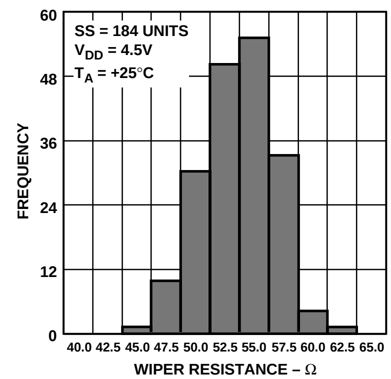


Figure 4. 100 kΩ Wiper-Contact-Resistance Histogram

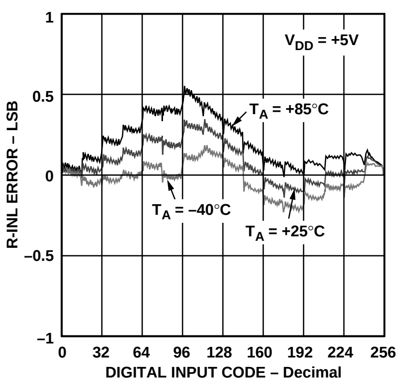


Figure 5. Resistance Step Position Nonlinearity Error vs. Code

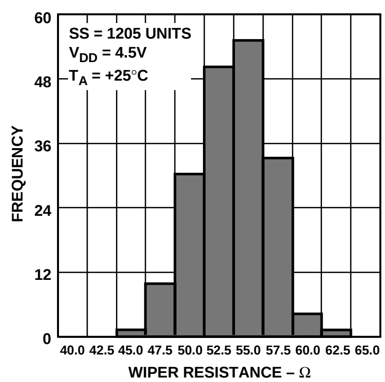


Figure 6. 10 kΩ Wiper-Contact-Resistance Histogram

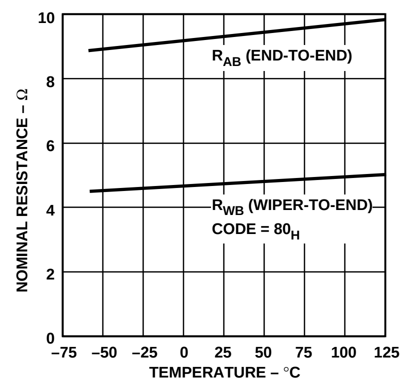


Figure 7. Nominal Resistance vs. Temperature

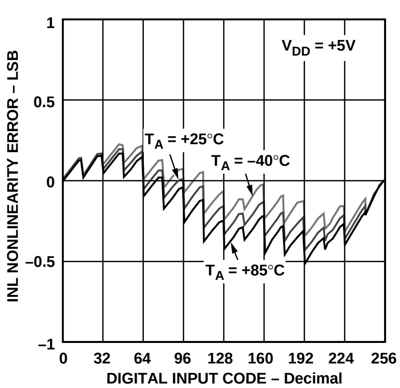


Figure 8. Potentiometer Divider Nonlinearity Error vs. Code

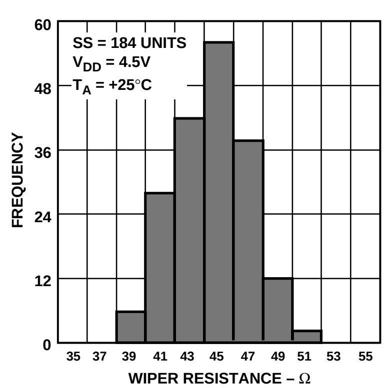


Figure 9. 50 kΩ Wiper-Contact-Resistance Histogram

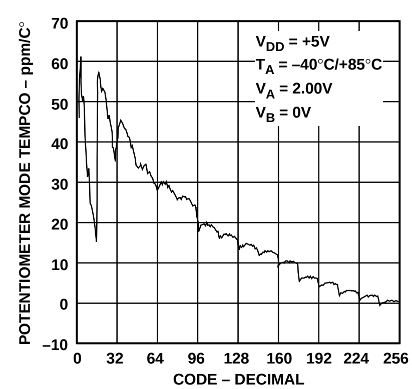


Figure 10. $\Delta V_{WB}/\Delta T$ Potentiometer Mode Tempco

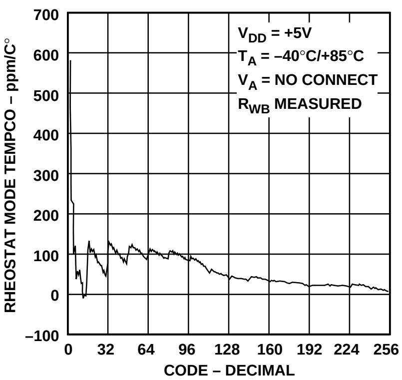


Figure 11. $\Delta R_{WB}/\Delta T$ Rheostat Mode Tempco

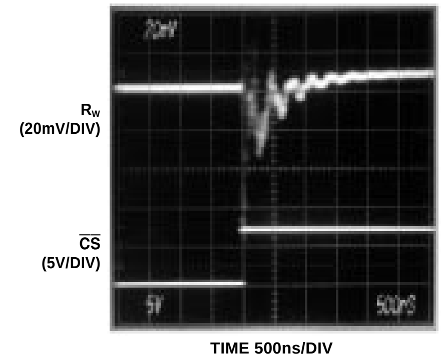


Figure 12. One Position Step Change at Half-Scale (Code $7F_H$ to 80_H)

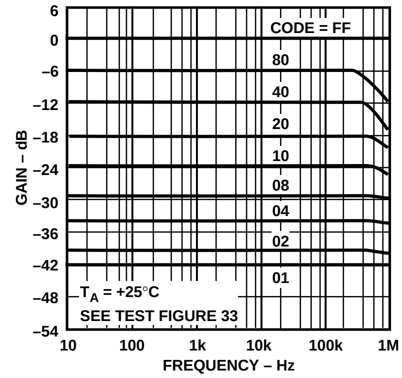


Figure 13. Gain vs. Frequency for R = 10 kΩ

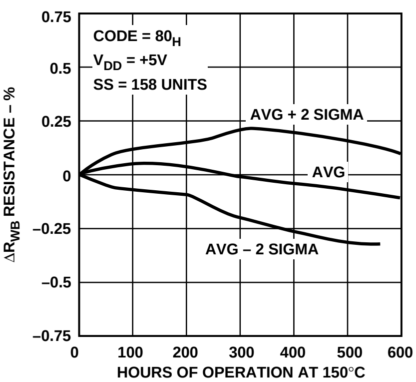


Figure 14. Long-Term Drift Accelerated by Burn-In

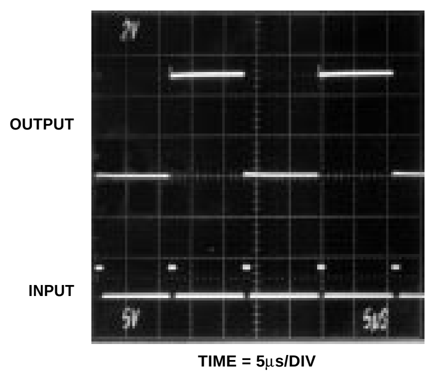


Figure 15. Large Signal Settling Time

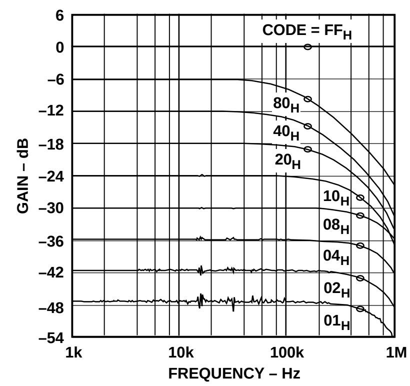


Figure 16. 50 kΩ Gain vs. Frequency vs. Code

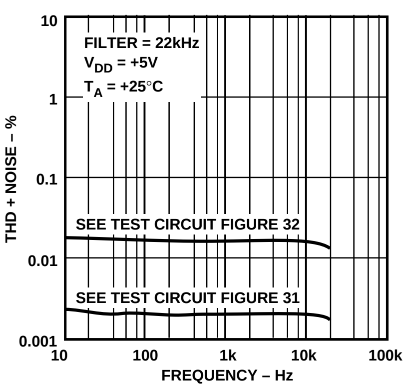


Figure 17. Total Harmonic Distortion Plus Noise vs. Frequency

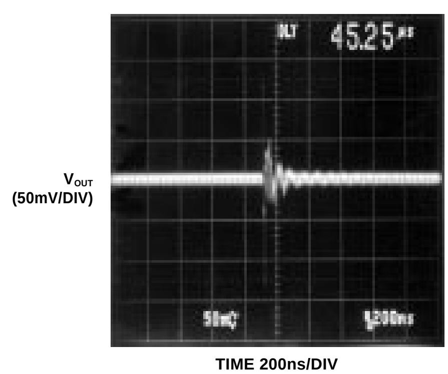


Figure 18. Digital Feedthrough vs. Time

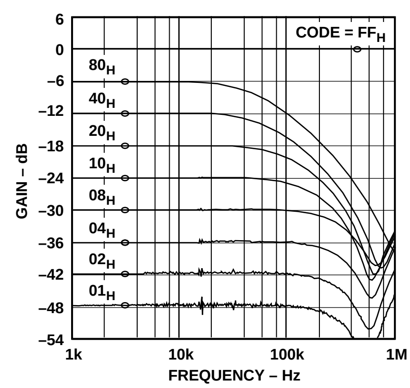


Figure 19. 100 kΩ Gain vs. Frequency vs. Code

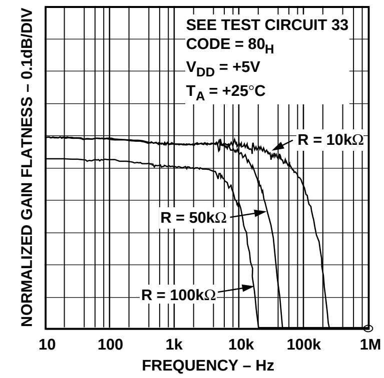


Figure 20. Normalized Gain Flatness vs. Frequency

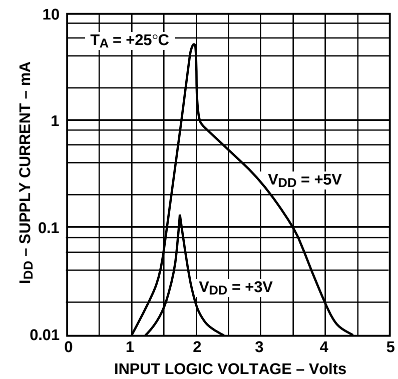


Figure 21. Supply Current vs. Logic Input Voltage

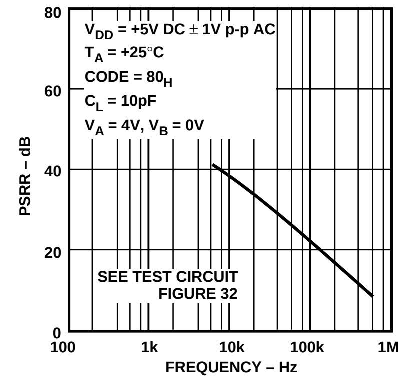


Figure 22. Power Supply Rejection vs. Frequency

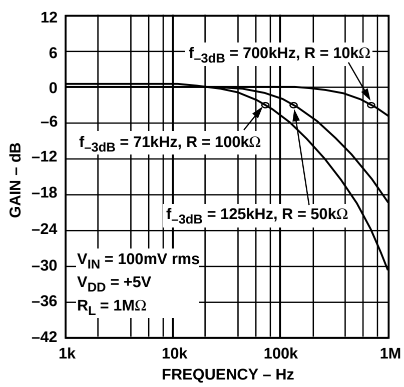


Figure 23. –3 dB Bandwidths

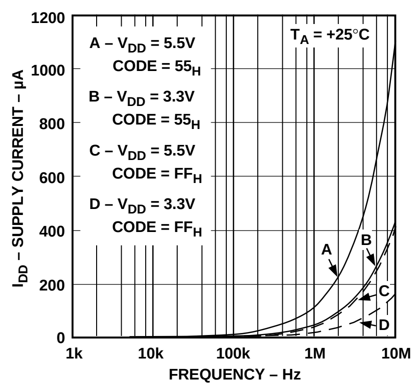


Figure 24. Supply Current vs. Clock Frequency

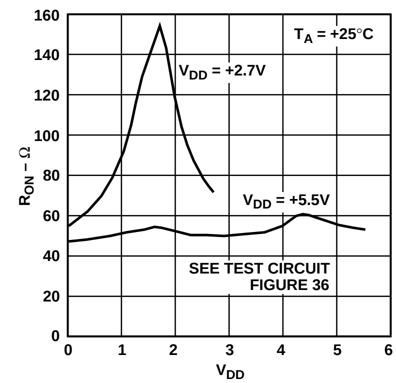


Figure 25. AD8403 Incremental Wiper ON Resistance vs. V_{DD}

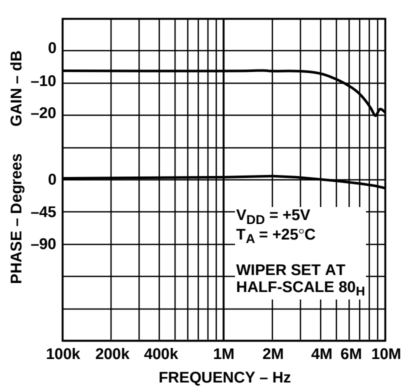


Figure 26. 1 kΩ Gain and Phase vs. Frequency

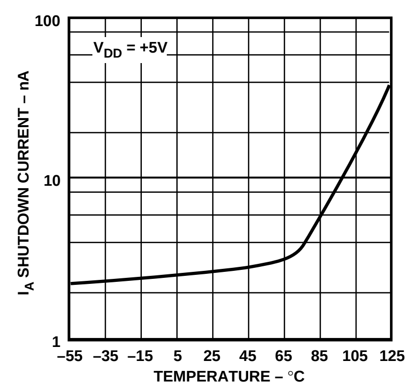


Figure 27. Shutdown Current vs. Temperature

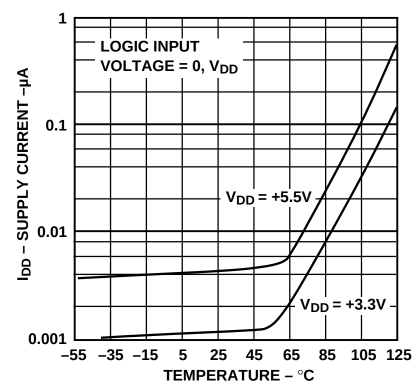


Figure 28. Supply Current vs. Temperature

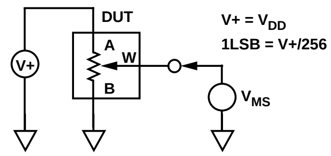


Figure 29. Potentiometer Divider Nonlinearity Error Test Circuit (INL, DNL)

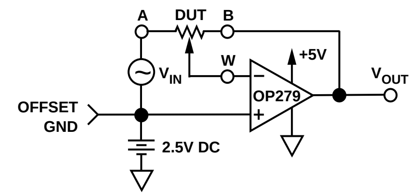


Figure 33. Inverting Programmable Gain Test Circuit

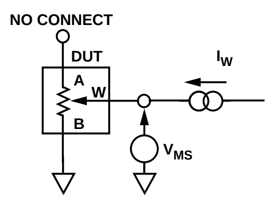


Figure 30. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

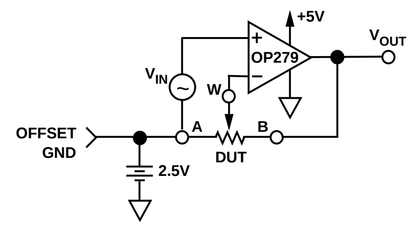


Figure 34. Noninverting Programmable Gain Test Circuit

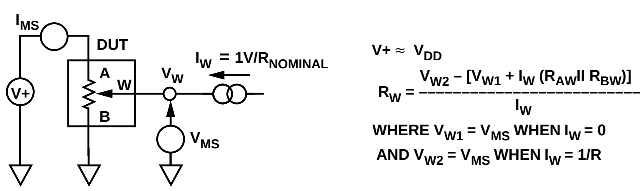


Figure 31. Wiper Resistance Test Circuit

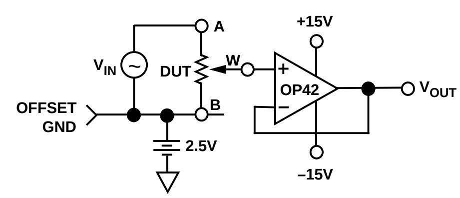


Figure 35. Gain vs. Frequency Test Circuit

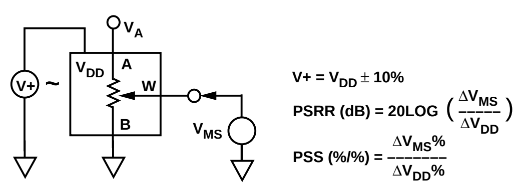


Figure 32. Power Supply Sensitivity Test Circuit (PSS, PSRR)

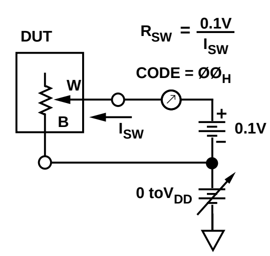


Figure 36. Incremental ON Resistance Test Circuit

OPERATION

The AD8400/AD8402/AD8403 provide a single, dual and quad channel, 256 position digitally controlled variable resistor (VR) device. Changing the programmed VR settings is accomplished by clocking in a 10-bit serial data word into the SDI (Serial Data Input) pin. The format of this data word is two address bits, MSB first, followed by eight data bits, MSB first. Table I provides the serial register data word format. The AD8400/AD8402/AD8403 has the following address assignments for the ADDR decode, which determines the location of VR latch receiving the serial register data in Bits B7 through B0:

$$VR\# = A1 \times 2 + A0 + 1 \qquad \text{Equation 1}$$

The single-channel AD8400 requires A1 = A0 = 0. The dual-channel AD8402 requires A1 = 0. VR settings can be changed one at a time in random sequence. The serial clock running at 10 MHz makes it possible to load all 4 VRs in under 4 µs (10 × 4 × 100 ns) for the AD8403. The exact timing requirements are shown in Figures 1a, 1b and 1c.

The AD8402/AD8403 resets to midscale by asserting the $\overline{RS}$ pin, simplifying initial conditions at power up. Both parts have a power shutdown $\overline{SHDN}$ pin that places the VR in a zero power consumption state where terminals Ax are open circuited and the wiper Wx is connected to Bx resulting in only leakage currents being consumed in the VR structure. In shutdown mode the VR latch settings are maintained so that returning to operational mode from power shutdown, the VR settings return to their previous resistance values. The digital interface is still active in shutdown, except that SDO is deactivated. Code changes in the registers can be made that will produce new wiper positions when the device is taken out of shutdown.

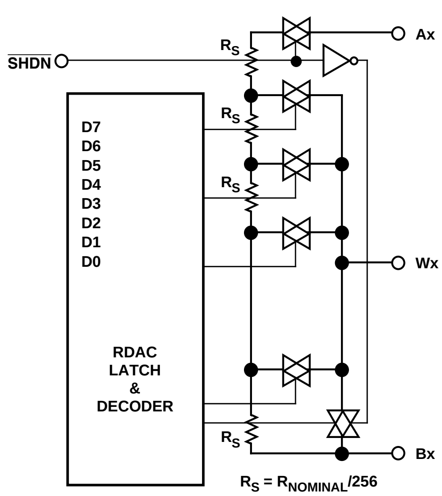


Figure 37. AD8402/AD8403 Equivalent VR (RDAC) Circuit

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the VR (RDAC) between terminals A and B are available with values of 1 kΩ, 10 kΩ, 50 kΩ and 100 kΩ. The final digits of the part number determine the nominal resistance value, e.g., 10 kΩ = 10; 100 kΩ = 100. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The 8-bit data word in the RDAC latch is decoded to select one of the 256 possible settings. The wiper's first connection starts at the B terminal for data 00_H. This B terminal connection has a wiper contact resistance of 50 Ω. The second connection (10 kΩ part) is the first tap point located at 89 Ω [= R_{BA} (nominal resistance)/256 + R_W = 39 Ω + 50 Ω] for data 01_H. The third connection is the next tap point representing 78 + 50 = 128 Ω for data 02_H. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10011 Ω. The wiper does not directly connect to the B terminal. See Figure 37 for a simplified diagram of the equivalent RDAC circuit.

The AD8400 contains one RDAC, the AD8402 contains two independent RDACs and the AD8403 contains four independent RDACs. The general transfer equation that determines the digitally programmed output resistance between Wx and Bx is:

$$R_{WB}(Dx) = (Dx)/256 \times R_{BA} + R_W \qquad \text{Equation 2}$$

where Dx is the data contained in the 8-bit RDAC# latch, and R_{BA} is the nominal end-to-end resistance.

For example, when V_B = 0 V and A terminal is open circuit, the following output resistance values will be set for the following RDAC latch codes (applies to 10 kΩ potentiometers):

D (Dec)	R_{WB} (Ω)	Output State
255	10011	Full Scale
128	5050	Midscale ($\overline{RS}$ = 0 Condition)
1	89	1 LSB
0	50	Zero-Scale (Wiper Contact Resistance)

Note in the zero-scale condition a finite wiper resistance of 50 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum value of 5 mA to avoid degradation or possible destruction of the internal switch contact.

Like the mechanical potentiometer the RDAC replaces, it is totally symmetrical. The resistance between the wiper W and terminal A also produces a digitally controlled resistance R_{WA}. When these terminals are used the B terminal should be tied to the wiper. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the RDAC latch is increased in value. The general transfer equation for this operation is:

$$R_{WA}(Dx) = (256 - Dx)/256 \times R_{BA} + R_W \qquad \text{Equation 3}$$

where Dx is the data contained in the 8-bit RDAC# latch, and R_{BA} is the nominal end-to-end resistance. For example, when V_A = 0 V and B terminal is open circuit, the following output resistance values will be set for the following RDAC latch codes (applies to 10 kΩ potentiometers):

D (Dec)	R_{WA} (Ω)	Output State
255	89	Full Scale
128	5050	Midscale ($\overline{RS}$ = 0 Condition)
1	10011	1 LSB
0	10050	Zero Scale

The typical distribution of R_{BA} from channel-to-channel matches within ±1%. However, device-to-device matching is process lot dependent having a ±20% variation. The change in R_{BA} with temperature has a positive 500 ppm/°C temperature coefficient.

The wiper-to-end-terminal resistance temperature coefficient has the best performance over the 10% to 100% of adjustment range where the internal wiper contact switches do not contribute any significant temperature related errors. The graph in Figure 11 shows the performance of R_{WB} tempco vs. code, using the trimmer with codes below 32 results in the larger temperature coefficients plotted.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates an output voltage proportional to the input voltage applied to a given terminal. For example, connecting A terminal to +5 V and B terminal to ground produces an output voltage at the wiper starting at zero volts up to 1 LSB less than +5 V. Each LSB of voltage is equal to the voltage applied across terminal AB divided by the 256 position resolution of the potentiometer divider. The general equation defining the output voltage with respect to ground for any given input voltage applied to terminals AB is:

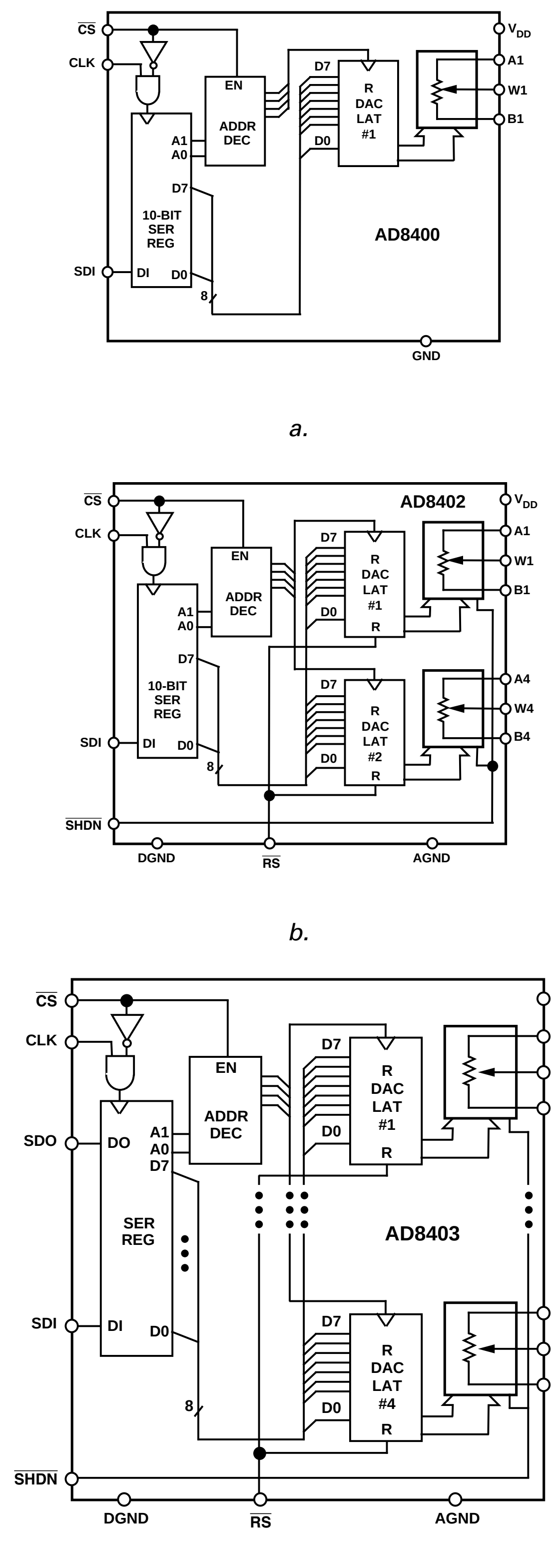
$$V_W(Dx) = Dx/256 \times V_{AB} + V_B \qquad \text{Equation 4}$$

Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. Here the output voltage is dependent on the ratio of the internal resistors, not the absolute value; therefore, the temperature drift improves to 15 ppm/°C.

At the lower wiper position settings, the potentiometer divider temperature coefficient increases due to the contributions of the CMOS switch wiper resistance becoming an appreciable portion of the total resistance from terminal B to the wiper. See Figure 10 for a plot of potentiometer tempco performance versus code setting.

DIGITAL INTERFACING

The AD8400/AD8402/AD8403 contains a standard SPI compatible three-wire serial input control interface. The three inputs are clock (CLK), $\overline{CS}$ and serial data input (SDI). The positive-edge sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. For best results use logic transitions faster than 1 V/µs. Standard logic families work well. If mechanical switches are used for product evaluation, they should be debounced by a flip-flop or other suitable means. The Figure 38 block diagrams show more detail of the internal digital circuitry. When $\overline{CS}$ is taken active low, the clock loads data into the 10-bit serial register on each positive clock edge (see Table II).



c.

Figure 38. Block Diagrams

Table II. Input Logic Control Truth Table

CLK	$\overline{CS}$	$\overline{RS}$	$\overline{SHDN}$	Register Activity
L	L	H	H	No SR effect, enables SDO pin.
P	L	H	H	Shift One bit in from the SDI pin. The tenth previously entered bit is shifted out of the SDO pin.
X	P	H	H	Load SR data into RDAC latch based on A1, A0 decode (Table III).
X	H	H	H	No Operation.
X	X	L	H	Sets all RDAC latches to midscale, wiper centered, and SDO latch cleared.
X	H	P	H	Latches all RDAC latches to 80_H.
X	H	H	L	Open circuits all resistor A–terminals, connects W to B, turns off SDO output transistor.

NOTE: P = positive edge, X = don't care, SR = shift register.

The serial data-output (SDO) pin contains an open drain n-channel FET. This output requires a pull-up resistor in order to transfer data to the next package's SDI pin. The pull-up resistor termination voltage may be larger than the V_{DD} supply (but less than max V_{DD} of +8 V) of the AD8403 SDO output device, e.g., the AD8403 could operate at V_{DD} = 3.3 V and the pull-up for interface to the next device could be set at +5 V. This allows for daisy chaining several RDACs from a single processor serial data line. The clock period needs to be increased when using a pull-up resistor to the SDI pin of the following device in the series. Capacitive loading at the daisy chain node SDO–SDI between devices must be accounted for to successfully transfer data. When daisy chaining is used, the $\overline{CS}$ should be kept low until all the bits of every package are clocked into their respective serial registers insuring that the address bits and data bits are in the proper decoding location. This would require 20 bits of address and data complying to the word format provided in Table I if two AD8403 four-channel RDACs are daisy chained. Note, only the AD8403 has a SDO pin. During shutdown $\overline{SHDN}$ the SDO output pin is forced to the off (logic high state) to disable power dissipation in the pull up resistor. See Figure 40 for equivalent SDO output circuit schematic.

The data setup and data hold times in the specification table determine the data valid time requirements. The last 10 bits of the data word entered into the serial register are held when $\overline{CS}$ returns high. At the same time $\overline{CS}$ goes high it gates the address decoder, which enables one of the two (AD8402) or four (AD8403) positive edge triggered RDAC latches. See Figure 39 detail and Table III Address Decode Table.

Table III. Address Decode Table

A1	A0	Latch Decoded
0	0	RDAC#1
0	1	RDAC#2
1	0	RDAC#3 AD8403 Only
1	1	RDAC#4 AD8403 Only

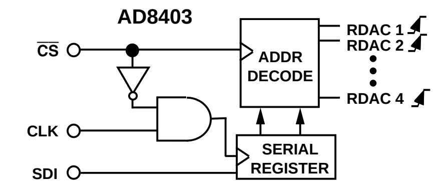


Figure 39. Equivalent Input Control Logic

The target RDAC latch is loaded with the last eight bits of the serial data word completing one DAC update. In the case of the AD8403 four separate 10-bit data words must be clocked in to change all four VR settings.

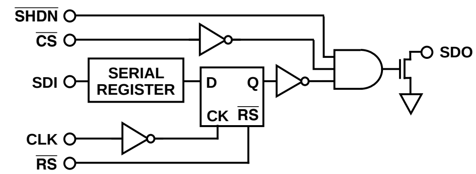


Figure 40. Detail SDO Output Schematic of the AD8403

All digital pins are protected with a series input resistor and parallel Zener ESD structure shown in Figure 41a. This structure applies to digital pins $\overline{CS}$, SDI, SDO, $\overline{RS}$, $\overline{SHDN}$, CLK. The digital input ESD protection allows for mixed power supply applications where +5 V CMOS logic can be used to drive an AD8400/AD8402 or AD8403 operating from a +3 V power supply. The analog pins A, B, W are protected with a 20 Ω series resistor and parallel Zener, see Figure 41b.

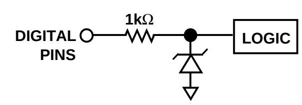


Figure 41a. Equivalent ESD Protection Circuits

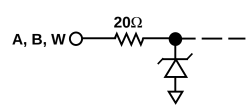


Figure 41b. Equivalent ESD Protection Circuit (Analog Pins)

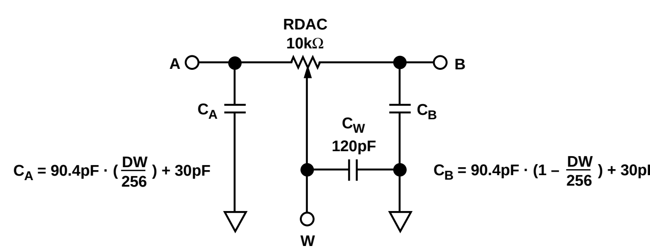


Figure 42. RDAC Circuit Simulation Model for RDAC = 10 kΩ

The ac characteristics of the RDACs are dominated by the internal parasitic capacitances and the external capacitive loads. The –3 dB bandwidth of the AD8403AN10 (10 kΩ resistor) measures 600 kHz at half scale as a potentiometer divider. Figure 23 provides the large signal BODE plot characteristics of the three available resistor versions 10 kΩ, 50 kΩ, and 100 kΩ. The gain flatness versus frequency graph, Figure 26, predicts filter applications performance. A parasitic simulation model has been developed, and is shown in Figure 42. Listing I provides a macro model net list for the 10 kΩ RDAC:

Listing I. Macro Model Net List for RDAC

```
.PARAM DW=255, RDAC=10E3
*
.SUBCKT DPOT (A,W,)
*
CA   A  0  {DW/256*90.4E-12+30E-12}
RAW  A  W  {(1-DW/256)*RDAC+50}
CW   W  0  120E-12
RBW  W  B  {DW/256*RDAC+50}
CB   B  0  {(1-DW/256)*90.4E-12+30E-12}
*
.ENDS DPOT
```

The total harmonic distortion plus noise (THD+N) is measured at 0.003% in an inverting op amp circuit using an offset ground and a rail-to-rail OP279 amplifier, Figure 33. Thermal noise is primarily Johnson noise, typically 9 $nV/\sqrt{Hz}$ for the 10 kΩ version at f = 1 kHz. For the 100 kΩ device, thermal noise becomes 29 $nV/\sqrt{Hz}$. Channel-to-channel crosstalk measures less than –65 dB at f = 100 kHz. To achieve this isolation, the extra ground pins provided on the package to segregate the individual RDACs must be connected to circuit ground. AGND and DGND pins should be at the same voltage potential. Any unused potentiometers in a package should be connected to ground. Power supply rejection is typically –35 dB at 10 kHz (care is needed to minimize power supply ripple in high accuracy applications).

APPLICATIONS

The digital potentiometer (RDAC) allows many of the applications of trimming potentiometers to be replaced by a solid-state solution offering compact size, freedom from vibration, shock and open contact problems encountered in hostile environments. A major advantage of the digital potentiometer is its programmability. Any settings can be saved for later recall in system memory.

The two major configurations of the RDAC include the potentiometer divider (basic 3-terminal application) and the rheostat (2-terminal configuration) connections shown in Figures 29 and 30.

Certain boundary conditions must be satisfied for proper AD8400/AD8402/AD8403 operation. First, all analog signals must remain within the 0 to V_{DD} range used to operate the single-supply AD8400/AD8402/AD8403 products. For standard potentiometer divider applications, the wiper output can be used directly. For low resistance loads, buffer the wiper with a suitable rail-to-rail op amp such as the OP291 or the OP279. Second, for ac signals and bipolar dc adjustment applications, a virtual ground will generally be needed. Whatever method is used to create the virtual ground, the result must provide the necessary sink and source current for all connected loads, including adequate bypass capacitance. Figure 33 shows one channel of the AD8402 connected in an inverting programmable gain amplifier circuit. The virtual ground is set at +2.5 V which allows the circuit output to span a ±2.5 volt range with respect to virtual ground. The rail-to-rail amplifier capability is necessary for the widest output swing. As the wiper is adjusted from its midscale reset position (80_H) toward the A terminal (code FF_H), the voltage gain of the circuit is increased in successfully larger increments. Alternatively, as the wiper is adjusted toward the B terminal (code 00_H), the signal becomes attenuated. The plot in Figure 43 shows the wiper settings for a 100:1 range of voltage gain (V/V). Note the ±10 dB of pseudo-logarithmic gain around 0 dB (1 V/V). This circuit is mainly useful for gain adjustments in the range of 0.14 V/V to 4 V/V; beyond this range the step sizes become very large and the resistance of the driving circuit can become a significant term in the gain equation.

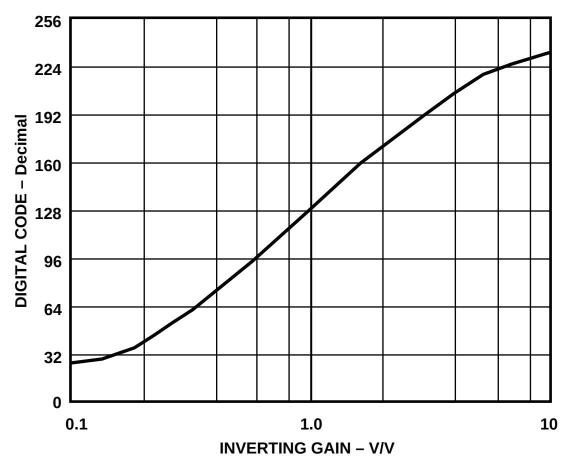


Figure 43. Inverting Programmable Gain Plot

ACTIVE FILTER

One of the standard circuits used to generate a low-pass, high-pass or bandpass filter is the state variable active filter. The digital potentiometer allows full programmability of the frequency, gain and Q of the filter outputs. Figure 44 shows the filter circuit using a +2.5 V virtual ground, which allows a ±2.5 V_P input and output swing. RDAC2 and 3 set the LP, HP and BP cutoff and center frequencies respectively. These variable resistors should be programmed with the same data (as with ganged potentiometers) to maintain the best circuit Q. Figure 45 shows the measured filter response at the bandpass output as a function of the RDAC2 and RDAC3 settings which produce a range of center frequencies from 2 kHz to 20 kHz. The filter gain response at the bandpass output is shown in Figure 46. At a center frequency of 2 kHz, the gain is adjusted over a –20 dB to +20 dB range determined by RDAC1. Circuit Q is adjusted by RDAC4. For more detailed reading on the state variable active filter, see Analog Devices' application note, AN-318.

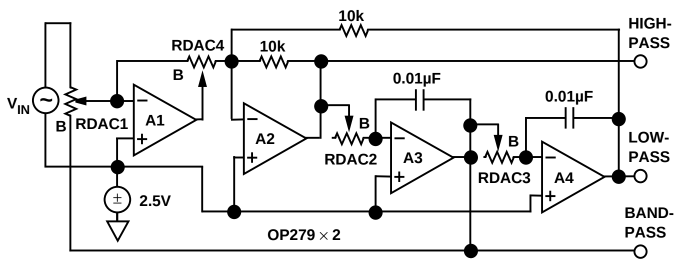


Figure 44. Programmable State Variable Active Filter

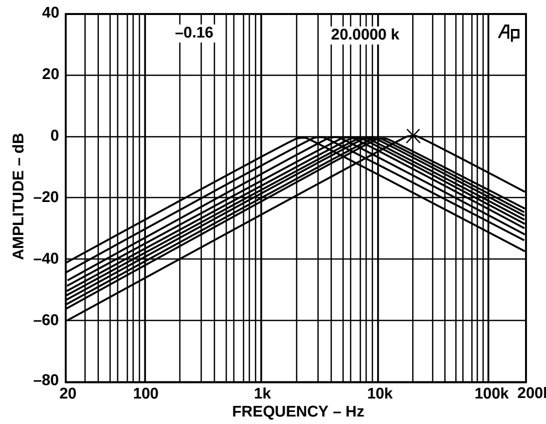


Figure 45. Programmed Center Frequency Bandpass Response

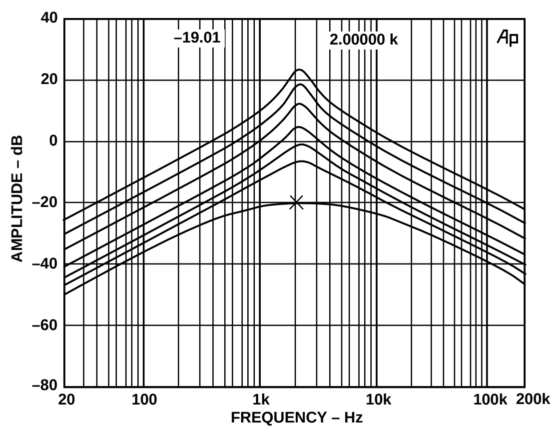
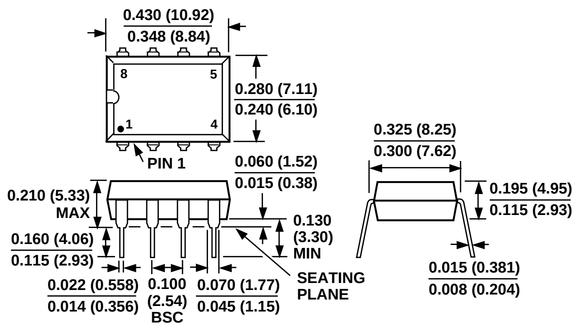


Figure 46. Programmed Amplitude Bandpass Response

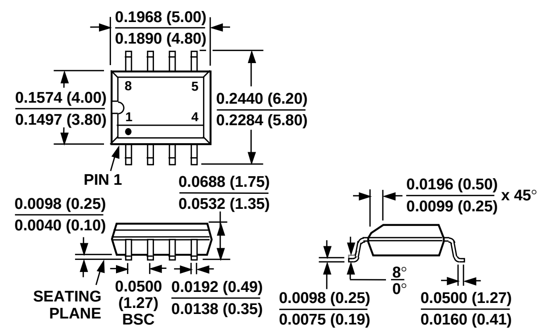
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

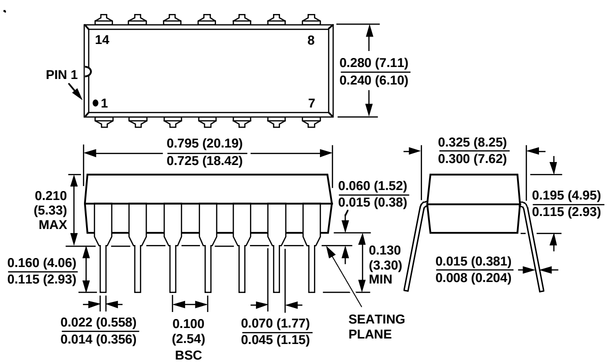
8-Pin Plastic DIP (N-8)



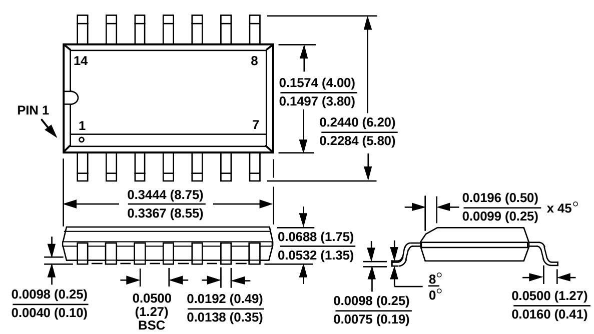
8-Lead SOIC (SO-8)



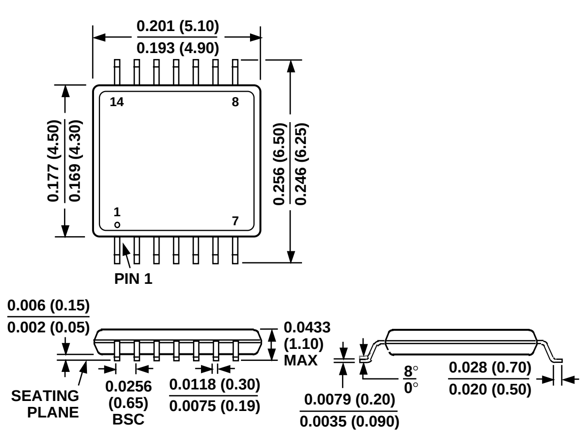
14-Pin Plastic DIP Package (N-14)



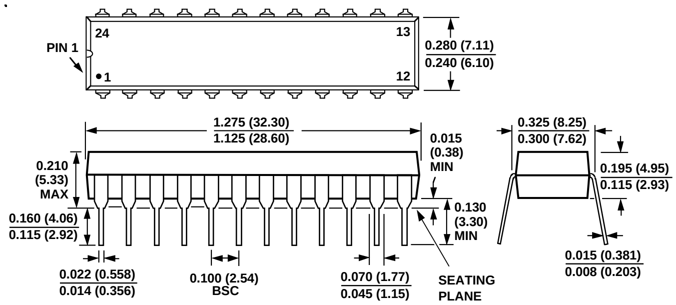
14-Pin Narrow Body SOIC Package (SO-14)



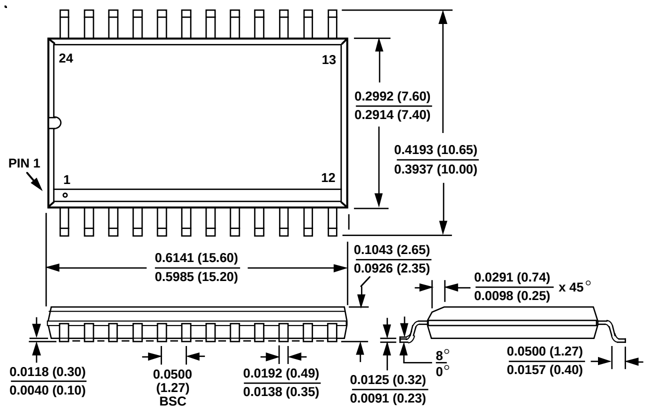
14-Lead TSSOP (RU-14)



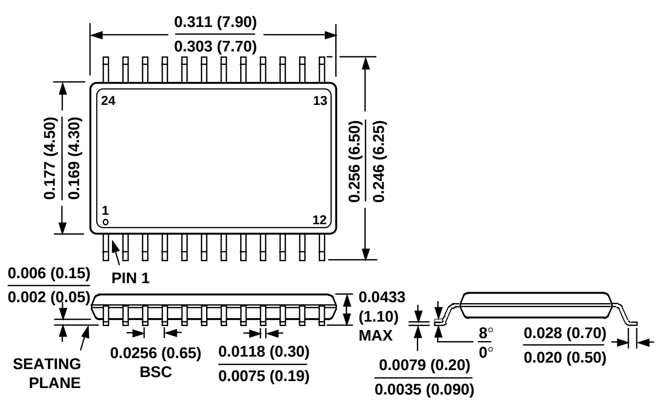
24-Pin Narrow Body Plastic DIP Package (N-24)



24-Pin SOIC Package (SOL-24)



24-Lead Thin Surface Mount TSSOP Package (RU-24)



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