Evaluation Board for Differential Input, 10-/12-Bit ADCs with a Serial Interface

EVAL-AD7440/AD7450A

FEATURES

Full-featured evaluation board for the AD7440/AD7450A
EVAL-CONTROL BRD2 compatible
Standalone capability
On-board analog buffering and reference
On-board single-ended-to-differential conversion
Various linking options
PC software for control and data analysis when used with evaluation board controller

GENERAL DESCRIPTION

This data sheet describes the evaluation board for the AD7440/AD7450A, which are 10-/12-bit, high speed, low power successive approximation ADCs with a fully differential analog input. These parts operate from a single +5 V or +3 V power supply. Full details on the EVAL-AD7440/AD7450A are available in the AD7440/AD7450A data sheet that is available from Analog Devices, Inc., and should be consulted in conjunction with this data sheet when using the evaluation board.

On-board components include an AD780, which is a pin-programmable +2.5 V or +3 V ultrahigh precision band gap reference, one AD713 quad op amp, two AD8022 dual op amps, one AD8138 differential amplifier, and a 7S04 inverter. Various link options are explained in detail in Table 1.

Interfacing to this board is through a 96-way connector. This 96-way connector is compatible with the EVAL-CONTROL BRD2, which is also available from Analog Devices. External sockets are provided for a number of signals including the V_{REF} input; the V_{IN+} and V_{IN-} inputs; the optional, external SCLK and $\overline{CS}$ inputs; and SDATA out.

FUNCTIONAL BLOCK DIAGRAM

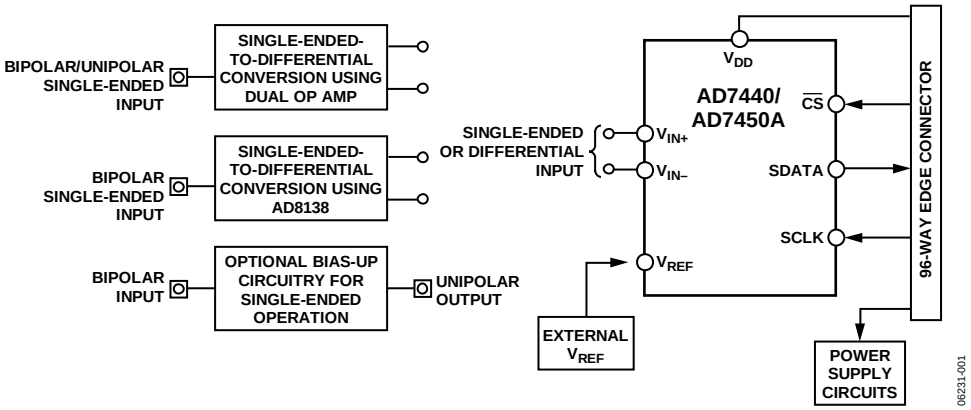

Figure 1.

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REVISION HISTORY

3/07—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES

When using this evaluation board with the EVAL-CONTROL BRD2, all supplies are provided from the EVAL-CONTROL BRD2 through the 96-way connector.

When using the board as a standalone unit, external supplies must be provided. The power supply inputs are AV_{DD} (+5 V), AV_{SS} (−5 V), AGND, +12 V, −12 V, V_{DD} (+5 V/+3 V), and DGND. If the evaluation board is used in standalone mode, +5 V/+3 V must be connected to the V_{DD} input to supply the AD7440/AD7450A V_{DD} pin. ±5 V must be connected to the ±5 V inputs to supply the AD8138 and +12 V and −12 V is needed to supply the AD713 quad op amp, the AD8022 dual op amps, and the AD780 voltage reference. The supplies are decoupled to the relevant ground plane with 10 µF tantalum and 0.1 µF multilayer ceramic capacitors at the point where they enter the board. The supply pins of all the op amps and the reference are also decoupled to AGND with 10 µF tantalum and a 0.1 µF ceramic capacitor. The AD7440/AD7450A V_{DD} supply pin is decoupled to AGND with 10 µF tantalum and 0.1 µF multilayer ceramic capacitors.

Extensive ground planes are used on this board to minimize the effect of high frequency noise interference. There are two ground planes, AGND and DGND. These are connected at one location close to the AD7440/AD7450A.

LINK OPTIONS

There are 27 link options that must be set for the required operating setup before using the evaluation board. The functions of these options are outlined in Table 1.

Table 1. Link Option Functions

Link No.	Function
LK1	This link option selects the source of the AV_{DD} +5 V supply.
	In Position A, the AV_{DD} is supplied from the EVAL-CONTROL BRD2.
	In Position B, the AV_{DD} must be supplied from an external source via the power connector J2.
LK2	This link option selects the source of the AV_{SS} −5 V supply.
	In Position A, the AV_{SS} is supplied from the EVAL-CONTROL BRD2.
	In Position B, the AV_{SS} must be supplied from an external source via the power connector J2.
LK3	This link option selects the source of the V_{DD} supply for the AD7440/AD7450A.
	In Position A, V_{DD} is supplied from the EVAL-CONTROL BRD2, provided LK1 is in Position A.
	In Position B, V_{DD} must be supplied from an external source via J3.
	For 3 V operation, V_{DD} must be supplied from an external source via J3.
LK4	This link option selects the input to U4, the AD8022 dual op amp configuration for performing single-ended-to-differential conversion on the analog input.
	This link should be removed if LK21 is in Position A so that the analog input can be applied to the dual op amp.
	This link should be inserted if LK21 is in Position B to tie the analog input of the dual op amp configuration to ground, as in this case, it is not used.
LK5	This link option selects the reference voltage applied to the V_{REF} pin of the AD7440/AD7450A.
	In Position A, an external signal must be supplied to the V_{REF} pin via P7.
	In Position B, the AD780 provides a 2.5 V reference to the V_{REF} pin. This is intended for 5 V operation of the AD7440/AD7450A.
	In Position C, a 2 V reference, 4/5 the output of the AD780 is applied to V_{REF} pin. This is intended for use in 3 V operation of the AD7440/AD7450A.
LK6	This link option selects the common-mode voltage to be applied to the V_{OCM} pin of the AD8138 differential amplifier.
	In Position A, the common-mode voltage applied to V_{OCM} is V_{REF}.
	In Position B, an external common-mode voltage must be applied to V_{OCM} via P4.
LK7	This link option is used to select the source of the V+ (+12 V) supply which is used to power the op amps and the external reference.
	In Position A, V+ is supplied from the EVAL-CONTROL BRD2 through the 96-way connector.
	In Position B, V+ is supplied from an external source via the power connector, J4.
LK8	This link option is used to select the source of the V− (−12 V) supply that is used to power the op amps.
	When this link is in Position A, the V− is supplied from the EVAL-CONTROL BRD2 through the 96-way connector.
	When this link is in Position B, the V− is supplied from an external source via the power connector, J4.
LK9	This link option controls the program pin of the AD780 reference voltage.
	When this link is inserted, the AD780 output voltage is set to +3.0 V.
	When this link is removed, the AD780 output voltage is set to +2.5 V.

Link No.	Function
LK10	This link option adds a 50 Ω termination to AGND at the VIN S.E. socket of the bias up circuit (P2) for the single-ended input. This link should be inserted if a 50 Ω termination is required on the analog input.
LK11	This link option sets the dc bias voltage that is applied to the optional bias up circuit used in single-ended mode. In Position A, the bias voltage is set to V_{REF} (that is, 2.5 V). In Position B, the bias voltage is set to AGND. In this configuration, the bias-up circuit is not used.
LK12	This link option selects the input to U8, the AD8138 differential amplifier used to perform single ended to differential conversion on the analog input. This link should be inserted if LK21 is in Position A to tie the analog input of the AD8138 to ground, as in this case, it is not used. This link should be removed if LK21 is in Position B so that the analog input can be applied to the AD8138.
LK13	This link option selects the single-ended input source to the AD7440/AD7450A if operating in single-ended mode. In Position A, the single-ended input is generated by the bias up circuit. In Position B, an external unipolar single-ended signal must be applied to the V_{IN+} input via P3. In Position C, the input to U7, the AD8022 op amp used to buffer the single-ended signal is tied to AGND. In this case, single-ended operation is not used.
LK14	This link is used to set up the common-mode voltage applied to U4, the AD8022 dual op amp configuration used to perform single-ended-to-differential conversion on the analog input. In Position A, an external common-mode voltage can be applied to U4 via P11. In Position B, this input is tied to AGND. In this case, the AD8022 dual op amp is not used. In Position C, a portion of V_{REF} is applied to U4 to set up the common-mode voltage.
LK15	This link is used in conjunction with LK27 to set up the AD8022 dual op amp configuration to convert either a unipolar or bipolar, single-ended signal into a differential signal centered on the common-mode voltage. These links should be inserted when the analog input is biased around 0 V (that is, bipolar). These links should be removed when the analog input is biased around 2.5 V (that is, unipolar).
LK16	This link option selects the source of the SCLK input. In Position A, the SCLK input is provided via the external socket, P8. In Position B, the SCLK input is provided by the EVAL-CONTROL BRD2.
LK17	This link is used to control the polarity of the serial clock applied to the SCLK pin. This link must be in Position A when LK16 is in Position B and the SCLK is provided by the EVAL-CONTROL BRD2. This means data is valid on the falling edge of SCLK. This link may be placed in Position B when LK16 is in Position A, to invert an SCLK from P8 if necessary. This would mean data may be read on the rising edge of SCLK but would only be possible with a slower SCLK frequency.
LK18	This link option selects where the serial data out (SDATA) appears. In Position A, the data may be read by the EVAL-CONTROL BRD2. In Position B, the data may be read via the external socket, P9.
LK19	This link option selects the source of the $\overline{CS}$ input. In Position A, the $\overline{CS}$ input is provided by the EVAL-CONTROL BRD2. In Position B, the $\overline{CS}$ input is provided via the external socket, P10.
LK20	This link option selects the source of the +5 V digital supply. In Position A, +5 V is supplied by the EVAL-CONTROL BRD2. In Position B, +5 V must be supplied from an external source via J5.
LK21	This links selects which single-ended-to-differential converter to use. When this link is in Position A, the AD8022 dual op amp configuration is used. In this case, LK4 should be removed and LK12 inserted. When this link is in Position B, the AD8138 differential amplifier is used. In this case, LK4 should be inserted and LK12 removed.
LK22	This link option selects the input to the AD8022, U7-A op amp. This op amp is only used in 3 V operation of the AD7440/AD7450A as it buffers the output of the resistor divider circuit, which divides the output of the AD780 to provide a 2 V reference for 3 V operation. If 3 V operation is being used, then this link should be removed. If 5 V operation is being used, this link should be inserted to tie the input to U7-A to ground as it is not used.
LK23	This link option selects whether the output of the AD780 reference is applied directly to the AD7440/AD7450A or if it is divided down to provide a 2 V reference. This link should be in Position A if a 2.5 V reference is required (usually for 5 V operation). In this case, LK22 should be inserted. This link should be in Position B if a 2 V reference is required (usually for 3 V operation). In this case, LK22 should be removed.

Link No.	Function
LK24	This link option selects the source of the V_{IN+} analog input. In Position A, an external signal must be applied to V_{IN+} via P5. In Position B, V_{IN+} is supplied from the positive output of the AD8022 dual op amp configuration. In Position C, V_{IN+} is supplied from the positive output of the AD8138 differential amplifier. In Position D, a single-ended signal is applied to the V_{IN+} input.
LK25	This link option selects the source of the V_{IN-} analog input. In Position A, an external signal must be applied to V_{IN-} via P6, either for differential or single-ended operation. In Position B, V_{IN-} is supplied from the negative output of the AD8022 dual op amp configuration. In Position C, V_{IN-} is supplied from the negative output of the AD8138 differential amplifier. In Position D, V_{REF} is applied to the V_{IN-} input of the AD7440/AD7450A for single-ended operation.
LK26	This link option adds a 50 Ω termination to AGND at the VIN DIFF socket used for differential operation. This link should be inserted if a 50 Ω termination is required on the analog input. In this case, if the AD8138 differential amplifier is being used, R11 should be increased to 523 Ω. The additional 23 Ω at the input is to balance the parallel impedance of the 50 Ω source and the 50 Ω termination thus making both inputs to the AD8138 have the same gain. If a 50 Ω termination is not required, then all four resistors around the AD8138 (R10, R11, R12, R13) must have the same value.
LK27	This link is used in conjunction with LK15 to set up the AD8022 dual op amp configuration to convert either a unipolar or bipolar, single-ended signal into a differential signal centered on the common mode voltage. These links should be inserted when the analog input is biased around 0 V (that is, bipolar). These links should be removed when the analog input is biased around 2.5 V (that is, unipolar).

SETUP CONDITIONS

Care should be taken before applying power and signals to the evaluation board to ensure that all link positions are as per the required operating mode. There are a few different modes in which to operate the evaluation board. The board offers two ways to perform single-ended-to-differential conversion of the analog input: Using the AD8138 differential amplifier or using a dual op amp configuration (AD8022). The AD8138 can only be used with a bipolar input, while the dual op amp can be used with a unipolar or bipolar input. The AD7440/AD7450A can operate with either a 5 V or a 3 V power supply. The board can also be set up for single-ended mode when the AD7440/AD7450A is operated with a 5 V supply. Table 2 shows the position in which all the links are set when the evaluation board is shipped. This is set up for differential mode using the AD8138 and V_{DD} of 5 V. The link positions for using the dual op amp configuration, for differential 3 V operation, and single-ended operation are discussed following this table. The board is operational with the evaluation board controller as received when shipped to the customer.

Table 2. Initial Link Positions—Differential Mode (Using the AD8138, V_{DD} = 5 V)

Link No.	Position	Function
LK1	A	AV_{DD} is supplied by the EVAL-CONTROL BRD2.
LK2	A	AV_{SS} is supplied by the EVAL-CONTROL BRD2.
LK3	A	V_{DD} for the AD7440/AD7450A is 5 V and is supplied by the EVAL-CONTROL BRD2.
LK4	Inserted	The input to U4-A is tied to ground as the dual op amp configuration is not being used.
LK5	B	V_{REF} is selected to be 2.5 V and is supplied by the AD780.
LK6	A	The common-mode voltage applied to the V_{OCM} pin of the AD8138 is V_{REF}.
LK7	A	V+ is supplied by the EVAL-CONTROL BRD2.
LK8	A	V− is supplied by the EVAL-CONTROL BRD2.
LK9	Removed	The AD780 is set to provide a 2.5 V reference.
LK10	Removed	A 50 Ω termination to AGND is not applied to the input of the bias up circuit as this is only used in single-ended mode.
LK11	B	The bias up circuit is not used so the input to U2-C op amp (reference buffer) is grounded.
LK12	Removed	The AD8138 is used to perform single-ended-to-differential conversion so the AD8138 positive input is connected to the analog input.
LK13	C	The input to U7-B, the op amp buffer for the single-ended input, is tied to ground, as it is not used.
LK14	B	The input to U4-B is tied to ground, as the dual op amp configuration is not used.
LK15	Removed	The dual op amp configuration is not used.
LK16	B	SCLK is supplied by the EVAL-CONTROL BRD2.
LK17	A	SCLK is not inverted.
LK18	A	SDATA is read by the EVAL-CONTROL BRD2.
LK19	A	$\overline{CS}$ is supplied by the EVAL-CONTROL BRD2.
LK20	A	The +5 V source is the EVAL-CONTROL BRD2.
LK21	B	The AD8138 is used to perform single-ended-to-differential conversion on the analog input.
LK22	Inserted	The input to the U7-A op amp is tied to ground, as it is not used.
LK23	A	The output of the AD780 reference is connected directly to LK5 to provide a 2.5 V reference to the AD7440/AD7450A.
LK24	C	V_{IN+} is supplied by the positive output of the AD8138 differential amplifier.
LK25	C	V_{IN-} Is supplied by the negative output of the AD8138 differential amplifier.
LK26	Removed	A 50 Ω termination to AGND is not applied to the analog input. In this case, all four resistors around the AD8138 (R10, R11, R12, R13) have the same value.
LK27	Removed	The dual op amp configuration is not used.

Differential Mode—Using the Dual Op Amp Configuration (AD8022)

The following links should be changed to use the dual op amp configuration (AD8022, U4) to perform single-ended-to-differential conversion on the analog input (the others remain as per Table 2):

Table 3.

Link No.	Position	Function
LK4	Removed	The dual op amp is used to perform single-ended-to-differential conversion so the U4-A input is connected to the analog input.
LK6	Removed	The AD8138 is not used so the V_{OCM} pin is tied to ground through a 0.1 µF capacitor.
LK12	Inserted	The input to AD8138 is tied to ground as it is not being used.
LK14	C	A portion of V_{REF} is applied to U4 to set up the common-mode voltage.
LK15 and LK27		These links should be inserted if the analog input is bipolar and removed if the analog input is unipolar.
LK21	A	The analog input is applied to the dual op amp configuration.
LK24	B	V_{IN+} is supplied by the positive output of the AD8022 dual op amp configuration.
LK25	B	V_{IN-} is supplied by the negative output of the AD8022 dual op amp configuration.

Differential Mode— Using the AD8138, V_{DD} = 3 V

The following links should be changed for 3 V differential operation (the others remain as per Table 2):

Table 4.

Link No.	Position	Function
LK3	B	3 V should be applied externally to V_{DD} of the AD7440/AD7450A via J3.
LK5	C	A 2 V reference is applied to the AD7440/AD7450A V_{REF} pin.
LK22	Removed	AD8022, U7-A, is used to buffer the 1.25 V reference before it is applied to the AD7440/AD7450A.
LK23	B	The output of the AD780 reference is divided to provide a 2 V reference to the AD7440/AD7450A.

Single-Ended Mode, V_{DD} = 5 V

The following links should be changed for 5 V single-ended mode operation (the others remain as per Table 2):

Table 5.

Link No.	Position	Function
LK4	Inserted	The input to the AD8022 dual op amp configuration is connected to AGND, as it is not used.
LK11	A	V_{REF} of 2.5 V is applied to the bias up circuit.
LK12	Inserted	Input to AD8138 is connected to AGND, as it is not used.
LK13	A	The single-ended input to V_{IN+} is supplied by the bias-up circuit
LK14	B	The input to the AD8022 Dual op amp configuration is connected to AGND, as it is not used.
LK24	D	The V_{IN+} input is supplied by the output of U7-B, that is, the buffered single ended input.
LK25	D	V_{IN-} is supplied by V_{REF} to setup the midscale value or common-mode voltage.

INTERFACING TO THE EVALUATION BOARD

Interfacing to the evaluation board is via a 96-way connector, J1. J1 is used to connect the evaluation board to the EVAL-CONTROL BRD2 or other system. The pinout for the J1 connector is shown in Figure 2. Table 6 gives a description of the pins on the 96-way connector used to interface between the EVAL-CONTROL BRD2 and the EVAL-AD7440/AD7450A, and Table 7 gives its pin designations.

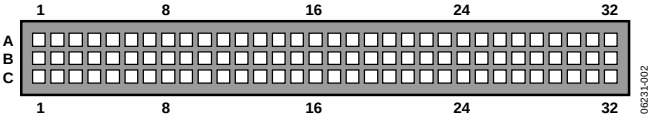

Figure 2. Pin Configuration for the 96-Way Connector, J1

Table 6. 96-Way Connector Pin Description

Signal	Description
DR0	Data Receive Zero. This input is connected to the SDATA pin of the AD7440/AD7450A via LK18. The data stream of the AD7450A consists of four leading zeros followed by the 12-bits of conversion data, provided MSB first. The data stream of the AD7440 consists of four leading zeros, followed by the 10-bits of conversion data, followed by two trailing zeros.
SCLK0	Serial Clock Zero. This continuous clock output is connected to the SCLK pin of the AD7440/AD7450A via LK16.
TFS0	Transmit Frame Sync Zero. This output is connected to the $\overline{CS}$ pin of the AD7440/AD7450A via LK19 to initiate conversions and to frame the serial data transfer.
RFS0	Receive Frame Sync Zero. This input is connected to the TFS0 pin of the ADSP-2189 to frame the serial data read.
DGND	Digital Ground. These lines are connected to the digital ground plane on the evaluation board. This allows the user to provide the digital supply via the connector along with the other digital signals.
AGND	Analog Ground. These lines are connected to the analog ground plane on the evaluation board.
AVDD	Analog +5 V Supply. These lines are connected to the AVDD supply line on the board via LK1 to provide +5 V to the AD8138 differential amplifier. They are also connected to the V_{DD} supply of the AD7440/AD7450A via LK3.
AVSS	Analog −5 V Supply. These lines are connected to the AVSS supply line on the board via LK2 to supply −5 V to the AD8138 differential amplifier.
±12 V	±12 V Supply. These lines are connected to the ±12 V supply lines on the board via LK7 and LK8 to supply ±12 V to the AD713, the AD8022s, and +12 V to the AD780.

Table 7. 96-Way Connector Pin Functions[1]

Pin	Row A	Row B	Row C
1			
2			
3			
4	DGND	DGND	DGND
5			DR0
6	TFS0		RFS0
7	SCLK0		SCLK0
8	+5 V	+5 V	+5 V
9			
10			
11			
12	DGND	DGND	DGND
13			
14			
15			
16	DGND	DGND	DGND
17			
18			
19			
20	DGND	DGND	DGND
21	AGND	AGND	AGND
22	AGND	AGND	AGND
23	AGND	AGND	AGND
24	AGND	AGND	AGND
25	AGND	AGND	AGND
26	AGND	AGND	AGND
27		AGND	
28		AGND	
29	AGND	AGND	AGND
30	−12 V	AGND	+12 V
31	AVSS	AVSS	AVSS
32	AVDD	AVDD	AVDD

[1] The unused pins of the 96-way connector are not shown.

SOCKETS

There are 11 input sockets relevant to the operation of the AD7440/AD7450A on this evaluation board. All of these sockets are used for applying an externally generated signal to the evaluation board. When operating the board with the EVAL-CONTROL BRD2, the only necessary external socket used is P1. All of the other sockets are optional, and if they are not used, their signals are supplied by the EVAL-CONTROL BRD2. Most of these sockets are used when operating the board as a stand-alone unit, as all the signals required are supplied from external sources. The functions of these sockets are outlined in Table 8.

Table 8. Socket Functions

Socket	Function
P1	VIN DIFF. Sub-miniature BNC socket for the bipolar analog input to the AD8138 or the bipolar/unipolar input to the AD8022 dual op amp configuration. These two circuits are used in differential mode.
P2	VIN S.E. Sub-miniature BNC socket for the bipolar analog input to the bias up circuit, which is an option when operating in single-ended mode.
P3	EXT S.E. Sub-miniature BNC socket for the unipolar analog input to V_{IN+}, which is an option when operating in single-ended mode.
P4	EXT COM. Sub-miniature BNC socket for the dc analog input to V_{OCM} pin on the AD8138 differential amplifier.
P5	VIN+ EXT. Sub-miniature BNC socket for a signal to be applied directly to V_{IN+}.
P6	VIN− EXT. Sub-miniature BNC socket for a signal to be supplied directly to V_{IN-}.
P7	EXT VREF. Sub-miniature BNC socket for an external VREF input.
P8	EXT SCLK**.** Sub-miniature BNC socket for an external SCLK input.
P9	EXT SDATA. Sub-miniature BNC socket for the SDATA output.
P10	EXT $\overline{CS}$. Sub-miniature BNC socket for an external $\overline{CS}$ input.
P11	EXT COM2. Sub-miniature BNC socket for setting up the common mode of the AD8022 dual op amp configuration.

CONNECTORS

There are five connectors on the AD7440/AD7450A evaluation board, as outlined in Table 9.

Table 9. Connector Functions

Connector	Function
J1	96-way connector for serial interface and power supply connections.
J2	External AV_{DD}, AV_{SS} and AGND power connector.
J3	External V_{DD} power connector.
J4	External +12 V, −12 V, and AGND power connector.
J5	External +5 V power connector.

OPERATING WITH THE EVAL-CONTROL BRD2

The evaluation board can be operated as a standalone unit or operated in conjunction with the EVAL-CONTROL BRD2. The EVAL-CONTROL BRD2 is available from Analog Devices under the order entry EVAL-CONTROL BRD2.

When interfacing the EVAL-AD7440/AD7450A directly to the EVAL-CONTROL BRD2 all supplies and control signals to operate the AD7440/AD7450A are provided by the EVAL-CONTROL BRD2. However, due to the nature of the DSP interface on the EVAL-CONTROL BRD2, AD7440/AD7450A sampling rates greater than 580 kHz are not supported when interfacing this evaluation board directly to the EVAL-CONTROL BRD2. This is because the clock frequencies on the ADSP-2189 on the EVAL-CONTROL BRD2 are limited by the expression:

$$CLKOUT/(2 \times (SCLKDIV + 1)$$

where:

CLKOUT = 40 MHz
SCLKDIV is the number that the user can choose to determine their required clock frequency.

It can be seen from this expression that the CLKOUT frequency can only be divided by factors of two because the value of SCLKDIV can only be an integer. Therefore, in the case of the AD7440/AD7450A where the maximum clock frequencies at 5 V and 3 V are 18 MHz and 15 MHz, respectively, the nearest clock frequency to these that can be generated by the DSP is 10 MHz (that is, SCLKDIV = 1), which results in a maximum sampling frequency of 580 kHz.

Software to communicate with the EVAL-CONTROL BRD2 and AD7440/AD7450A is provided with the AD7440/AD7450A evaluation board package. This EVAL-CONTROL BRD2 also operates with all Analog Devices evaluation boards that end with the letters CB in their model number.

The 96-way connector on the EVAL-AD7440/AD7450A plugs directly into the 96-way connector on the EVAL-CONTROL BRD2. The EVAL-CONTROL BRD2 provides all the supplies for the evaluation board. It is powered from a 12 V ac transformer. Suitable transformers are available from Analog Devices as an accessory under the following part numbers:

EVAL-110VAC-US:	For use in the U.S. or Japan
EVAL-220VAC-UK:	For use in the U.K.
EVAL-220VAC-EU:	For use in Europe

These transformers are also available from other suppliers, including Digi-Key (U.S.) and Campbell Collins (U.K.).

Connection between the EVAL-CONTROL BRD2 and the serial port of a PC is via a standard Centronics printer port cable, which is provided as part of the EVAL-CONTROL BRD2 package. Please refer to the manual that accompanies the EVAL-CONTROL BRD2 for more details on this package.

EVALUATION BOARD SOFTWARE

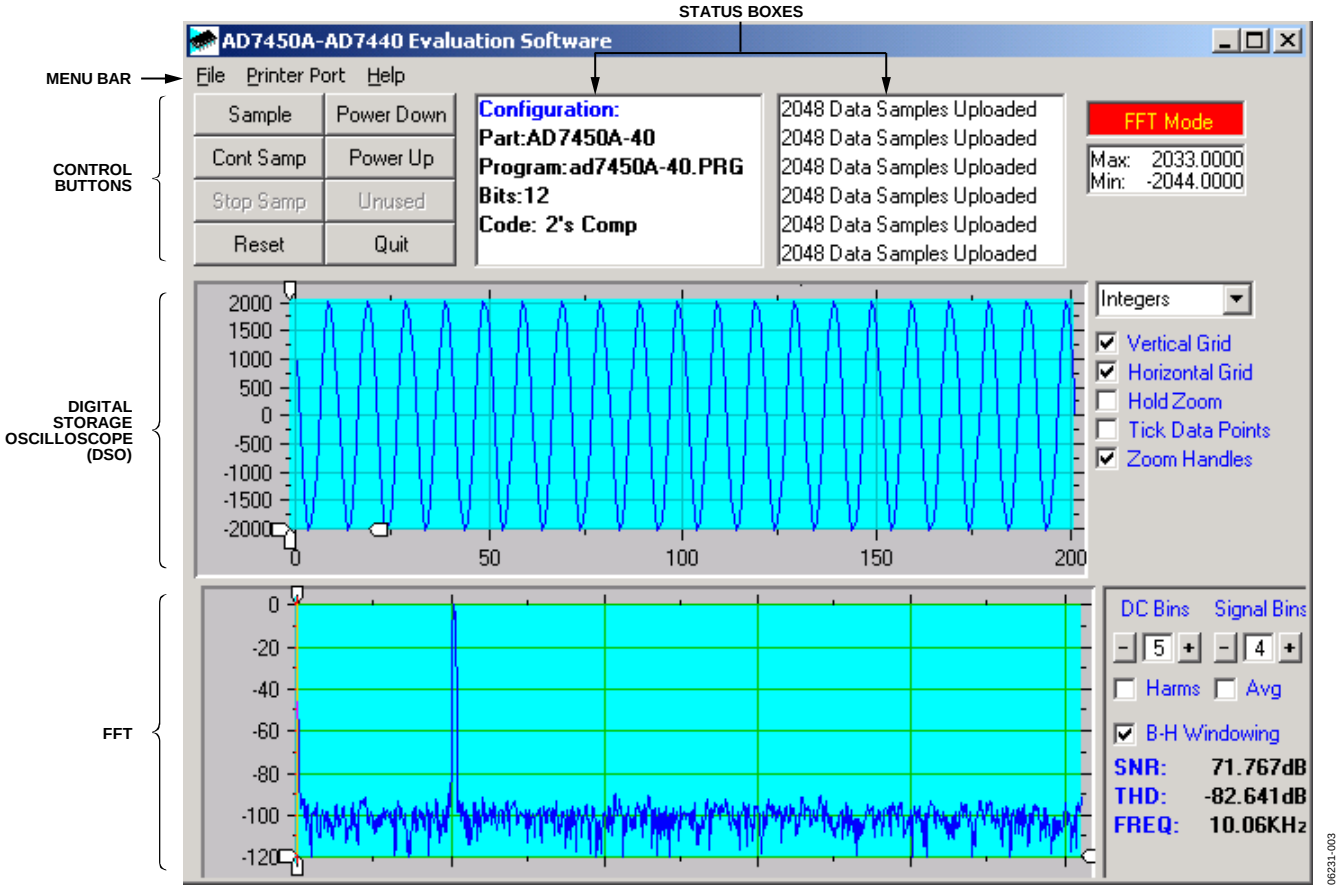

Figure 3. AD7440/AD7450A Main Screen

The software that controls the EVAL-CONTROL BRD2 and hence the evaluation board has three main screens. The screen shown in Figure 3 is the screen that appears when the software is run. The main function of this screen is to allow you to read a predetermined number of samples from the evaluation board and display them in both the time and frequency domain. The screen can be divided into three sections; control buttons, a digital storage oscilloscope (DSO), and a histogram.

Control Buttons

The control buttons allow you to take samples (**Sample**), reset the part (**Reset**), and quit the program (**Quit**). There are also power-down/up options in the control buttons. These buttons allow you to place the part into power-down, and power the part up again.

To enter power-down, click **Power Down**. To exit power-down click **Power Up** (see the AD7440/AD7450A data sheet).

Menu Bar

The menu bar allows you to enter the setup menu; select which printer port is to be used to control the EVAL-CONTROL BRD2 load and save data and get information about the software.

Status Boxes

The status windows indicate the setup of the evaluation board/device, number of samples taken and any information or error messages that are generated.

Digital Storage Oscilloscope (DSO)

When samples are uploaded from the EVAL-CONTROL BRD2, they are displayed in the DSO portion of the main screen. The samples can be displayed either as integer values or as voltages. Once samples have been displayed, clicking at any point on the graph displays the sample number and value of the point directly beneath the cursor. Along the axis of the graph are the zoom handles. These allow you to zoom in and out to get a closer look at a particular sample, if required. When another set of samples is taken, the graph attempts to display all values collected unless the **Hold Zoom** check box is ticked. In this case, the graph keeps the same axis settings as for the previous set of data samples. Additional check boxes are provided to give you control over the vertical and horizontal grids and data points.

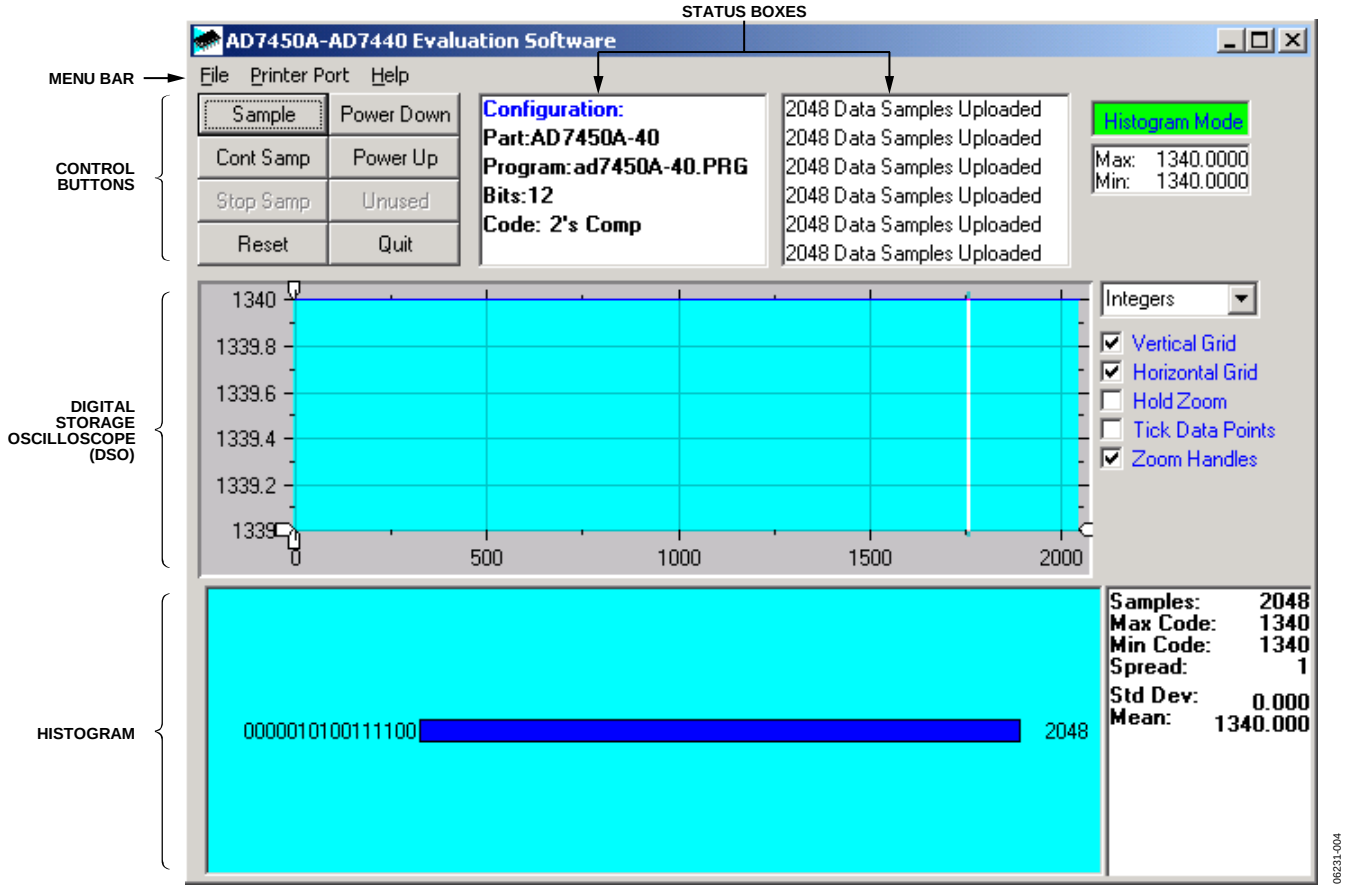

Figure 4. AD7440/AD7450A Main Screen–Histogram Mode

Histogram

The lower section of the screen shows either a fast Fourier transform (FFT) of the data (Figure 3) or a Histogram (Figure 4) which shows the number of occurrences of each particular code read back.

The FFT (the default option) is typically used when you are concerned with examining the ADC's performance in the frequency domain while the Histogram gives an indication of the ADC's performance to DC signals. The option displayed can be toggled by clicking the **FFT Mode/Histogram Mode** button in the top right of the screen. Figure 4 shows the main screen when the Histogram Mode option is selected.

Setup Screen

The setup screen allows you to load the required configuration file for the evaluation board. The configuration file gives the software detailed information about the EVAL-AD7440/AD7450A and the part connected to the EVAL-CONTROL BRD2 such as number of bits, maximum sampling rate, output coding, maximum analog input, power supply requirements, etc. When using the AD7450A, load the **AD7450A.cfg** file and when using the AD7440, load the **AD7440.cfg** file.

As explained in the Operating with the EVAL-CONTROL BRD2 section, the maximum clock frequency that can be used is limited by the ADSP-2189 on the EVAL-CONTROL BRD2. In this case, the maximum clock that can be used is 10 MHz, giving a maximum sampling frequency of 580 kHz.

The configuration file also tells the software the name of the DSP program file, which should download to the evaluation board controller. The setup screen also allows you to choose the sampling frequency and the number of samples to take. Figure 5 shows the setup screen.

SETTING UP THE EVAL-CONTROL BRD2

This section describes how the evaluation board, the EVAL-CONTROL BRD2, and software should be set up to begin using the complete system.

The EVAL-CONTROL BRD2 and evaluation board should be connected together (via the 96-way connector). The power should be applied to the EVAL-CONTROL BRD2 via a 12 V ac transformer. At this stage, the red LED should be flashing, which indicates that the EVAL-CONTROL BRD2 is functional and ready to receive instructions. The software (previously installed) should be loaded before the printer port cable is connected between the EVAL-CONTROL BRD2 and the PC. This ensures that the printer port has been initialized properly. The printer port cable can then be connected between the PC and the EVAL-CONTROL BRD2.

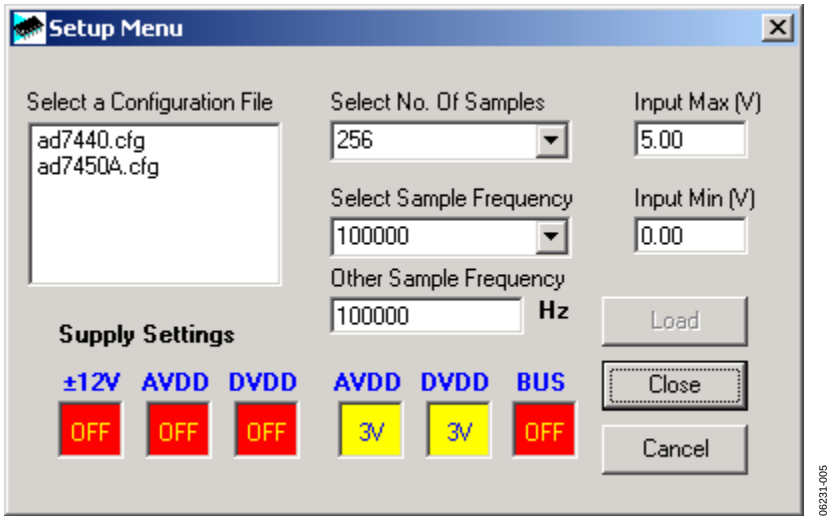

Figure 5. The Setup Screen

Running the Software

With the hardware set up, you are now in a position to use the software to control the EVAL-CONTROL BRD2 and the EVAL-AD7440/AD7450A.

Select the **File** menu and click **Setup**. This displays the setup form (as shown in Figure 5). A window on the left of the setup form lists the available configuration files. The configuration files are text based files that contain information about the particular evaluation board to be tested. The information covers the part name, number of samples to be taken, default and maximum sampling frequency, power supply settings, etc. The configuration file also contains the name of the DSP program file that is to be downloaded to the EVAL-CONTROL BRD2.

Select the relevant configuration file and click **Load**. The EVAL-CONTROL BRD2 resets and the DSP program downloads. When the download has been completed, the power supply settings indicated in the configuration file are set and you may hear some of the relays clicking.

The drop-down list boxes, **Select No. Of Samples** and **Select Sample Frequency** are set to the default values specified by the configuration file. You are free to change these at will. Once all the settings have been decided, click **Close** to return to the main form.

Taking Samples

When you click **Sample**, the software instructs the EVAL-CONTROL BRD2 to take the required number of samples at the required frequency from the evaluation board. The EVAL-AD7440/AD7450A runs up to 580 kSPS so you can choose the sampling frequency up to this rate and can also choose the number of samples to be taken. The maximum sampling frequencies as described in the AD7440/AD7450A data sheet can only be achieved when operating the evaluation board as a standalone unit. This is a clock frequency limitation of the DSP on the EVAL-CONTROL BRD2 (see the Operating with the EVAL-CONTROL BRD2 section).

The samples taken are then uploaded and displayed. An FFT and histogram are also calculated and displayed. If you click **Cont Samp,** the software repeats the process indefinitely until the user clicks **Stop Samp**. While the software is continuously sampling data, the other control buttons are disabled.

Other Buttons

The **Reset** button causes the EVAL-CONTROL BRD2 to perform a reset function. When this happens, the power supplies are turned off and the program in DSP memory is lost. You should repeat the setup instructions to download another program if required.

The **Quit** button exits the software; the program running on the EVAL-CONTROL BRD2 is not terminated.

MENU BAR ITEMS

The main screen of the EVAL-CONTROL BRD2 contains a number of options available as pull-down menu items. Following is a list of these functions.

File Menu

Setup Menu: Selecting this option displays the Setup Screen as shown in Figure 5.

Load Raw Data: Selecting this option allows you to load data that had been saved by the software during a previous session.

Save Raw Data: Selecting this option allows you to save the current set of sample data points. The data can be reloaded to the EVAL-CONTROL BRD2 software later or can be used by other programs for further analysis.

Save Binary Data: Selecting this option allows you to save the current set of sample data points. The data is saved in binary format as a text file. This method can be useful for examining code flicker, looking for stuck bits, etc.

Save FFT Data: Selecting this option allows you to save the current set of FFT data points. FFT data cannot be reloaded into the EVAL-CONTROL BRD2 software but can be loaded into other software packages for further analysis.

Exit: Quits the program.

Printer Port

If the operating system being used is Windows® 95 or Windows® 98, this menu item allows you to select which printer port should be used for communication with the EVAL-CONTROL BRD2.

LPT1: This option selects 0x378 as the printer port address. This is the default option.

LPT2: This option selects 0x278 as the printer port address.

PRN: This option selects 0x3BC as the printer port address.

If Windows® 2000 or Windows NT® is used, the software automatically detects the first printer port.

Help

This menu item gives information about the current revision of software for the particular evaluation board being used.

SOFTWARE CONFIGURATION FILES

Software configuration files give the evaluation board controller software information on how the software and hardware should perform. They contain information such as the name of the DSP program to download, the default and maximum sample frequencies, the number of samples to take, and the power supply settings to use.

Typical Software Configuration File (.cfg)

```
EVAL-CONTROL BRD2
partname:AD7450A
programname:ad7450A-40.PRG

samplefrequency:100000
maxsamplefrequency:580000
samples:2048

+/-15V:on
dvdd:5:on
avdd:5:on
bus:on
;options 2scomp, binary
dataformat:2scomp
numberofbits:12
inputVmax:5
inputVmin:0
[endofconfig]
```

Operating with Difference Voltage Reference Inputs

The functionality of the AD7440/AD7450A allows a variable reference input in the range 100 mV to 3.5 V with the allowable reference input being dependent on the power supply to ensure the maximum ratings of the device are not exceeded. For 5 V operation, the standard reference on the evaluation board is 2.5 V, which corresponds to a differential input of 5 V. This maximum input voltage is setup in the configuration file (see inputVmax: 5 in the Typical Software Configuration File (.cfg) section). For 3 V operation, the standard reference on the evaluation board is 2 V, which corresponds to a differential input of 4 V. Therefore, when operating with 3 V supplies, the configuration file has to be adjusted to show inputVmax: 4. As you change the reference input, you must ensure that you adjust the inputVmax figure in the configuration file to ensure that accurate data is displayed in the software. inputVmax is always be $2 \times V_{REF}$.

EVALUATION BOARD SCHEMATICS AND ARTWORK

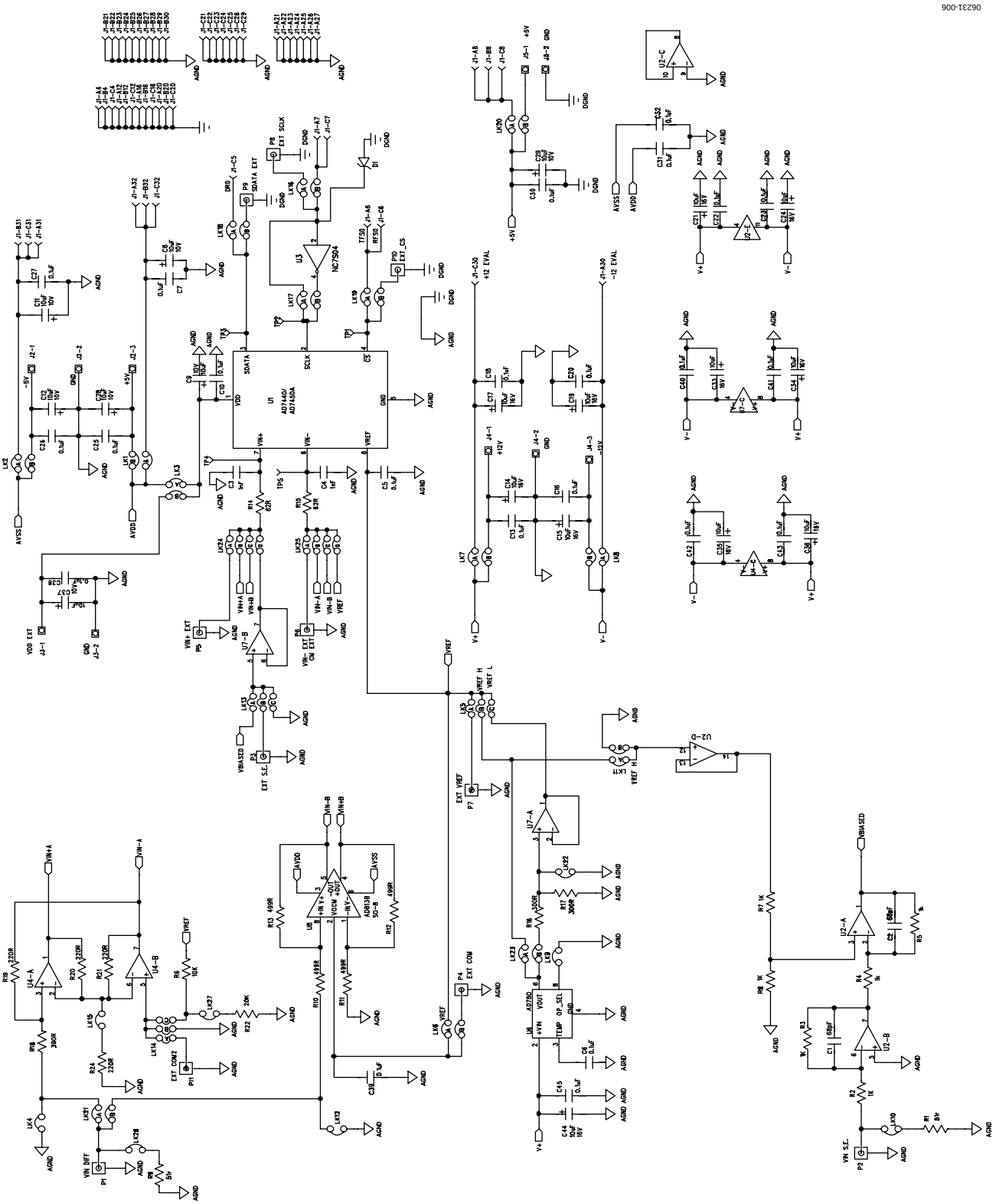

Figure 6. AD7440/AD7450A Evaluation Board Circuit Diagram

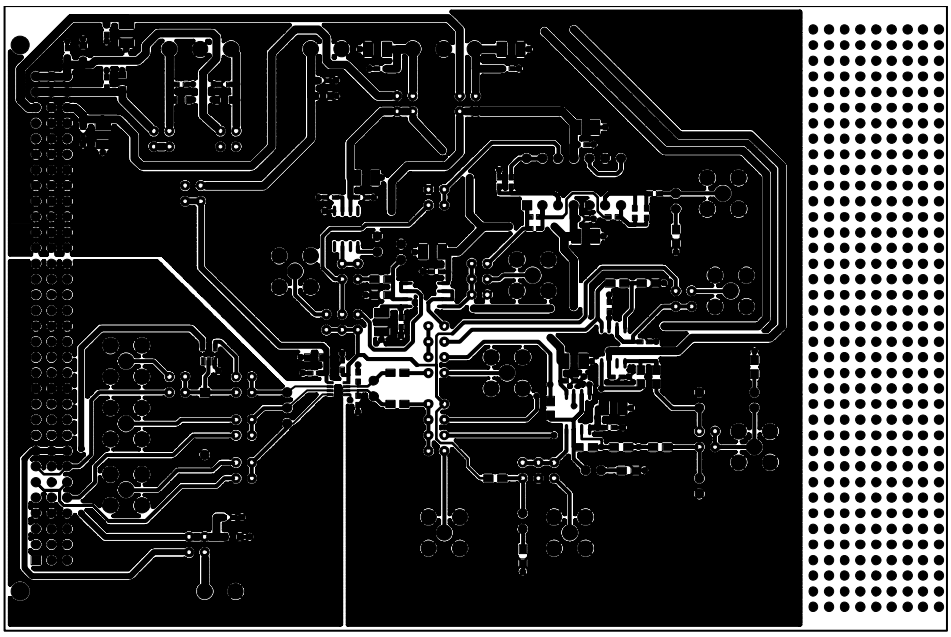

Figure 7. Component Side Artwork

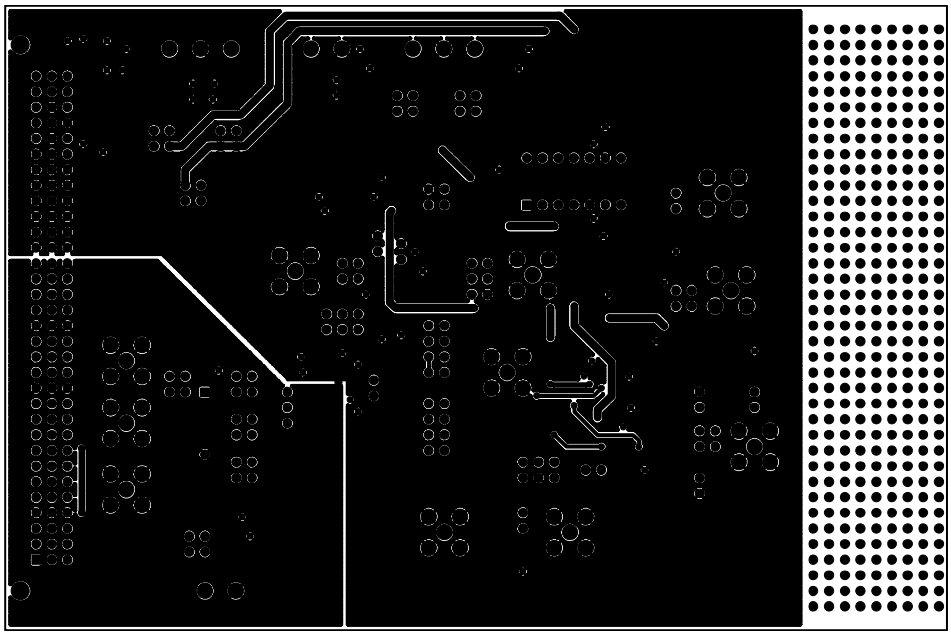

Figure 8. Solder Side Artwork

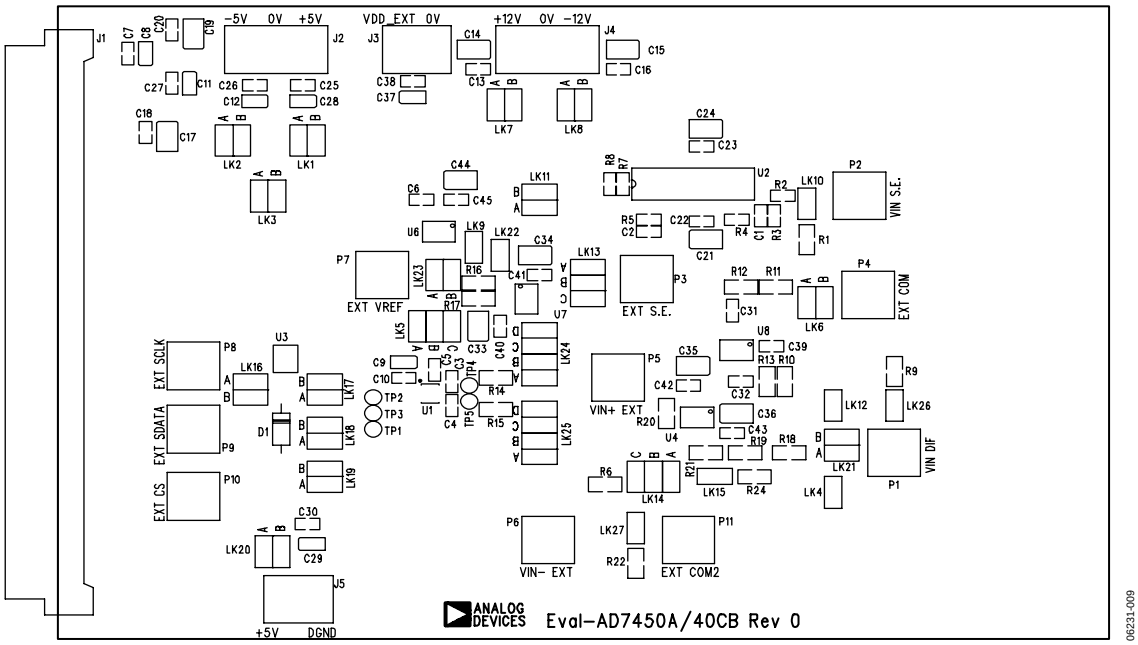

Figure 9. AD7440/AD7450A Evaluation Board Component Placement Drawing

ORDERING INFORMATION

BILL OF MATERIALS/COMPONENTS LISTING

Table 10.

Qty	Part Type	Reference Designator	Order Number[1]
1	AD7440/AD7450A	U1	AD7440BRT/AD7450ABRT
1	AD713	U2	AD713JN
1	NC7S04	U3	FEC 685-914
2	AD8022	U4, U7	AD78022AR
1	AD780	U6	AD780AR
1	AD8138	U8	AD8138AR
2	68 pF ceramic capacitor, SMD 0603	C1, C2	FEC 722-066
2	1 nF ceramic capacitor, SMD 0603	C3, C4	FEC 317-202
23	0.1 µF ceramic capacitor, SMD 0603	C5, C6, C7, C10, C13, C16, C18, C20, C22, C23, C25 to C27, C30 to C32, C38 to C43, C45	FEC 699-675
7	10 µF tantalum capacitor, 10 V	C8, C9, C11, C12, C28, C29, C37	FEC 197-130
11	10 µF tantalum capacitor, 16 V	C14, C15, C17, C19, C21, C24, C33, C34, C35, C36, C44	FEC 498-737
1	SD103C Schottky diode	D1	SD103CDITB-ND
1	51 Ω, 0.1 W, 0.1% resistor, SMD 0805	R1, R9	FEC 321-7905
6	1 kΩ, 0.063 W, 0.1% resistor, SMD 0603	R2, R3, R4, R5, R7, R8	FEC 911-239
1	10 kΩ, 0.1 W, 0.1% resistor, SMD 0805	R6	FEC 321-7905
4	499 Ω, 0.1 W, 0.1% resistor, SMD 0805	R10, R11, R12, R13	FEC 553-712
2	62 Ω, 0.1 W, 0.1% resistor, SMD 0805	R14, R15	FEC 321-7917
2	300 Ω, 0.1 W, 0.1% resistor, SMD 0805	R16, R17	FEC 321-7991
1	390 Ω, 0.1 W, 0.1% resistor, SMD 0805	R18	FEC 911-800
4	220 Ω, 0.1 W, 0.1% resistor, SMD 0805	R19, R20, R21, R24	FEC 911-770
1	20 kΩ, 0.1 W, 0.1% resistor, SMD 0805	R22	FEC 321-8211
1	CON\41612\96 connector	J1	FEC 225-393
2	3-pin terminal block	J2, J4	FEC 151-786
2	2-pin terminal block	J3, J5	FEC 151-785
8	1-way jumper (2 × 1)	LK4, LK9, LK10, LK12, LK15, LK22, LK26, LK27	FEC 511-705
14	2-way jumper (2 × 2)	LK1 to LK3, LK6 to LK8, LK11, LK16 to LK21, LK23	FEC 511-791
3	3-way jumper (2 × 3)	LK5, LK13, LK14	FEC 511-780
2	4-way jumper (2 × 4)	LK24, LK25	FEC 511-791
27	Shorting link	LK1 to LK27	FEC 150-411
11	Gold 50 Ω SMB jack	P1 to P11	FEC 310-682
5	Test point	TP1, TP2, TP3, TP4, TP5	FEC 240-333
4	Stick-on feet	Each corner	FEC 148-922

[1] FEC = Farnell Electronic Components®.

ORDERING GUIDE

Model	Description
EVAL-AD7440CB	AD7440 Evaluation Board
EVAL-AD7450ACB	AD7450A Evaluation Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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