LSK489 Application Note

Introduction

Until now the LSK389 ultra-low noise dual JFET would have been the ideal device to use in a circuit designed to work with high impedance sources from electrometers to microphone pre-amplifiers. With a high input impedance (1TΩ) and low noise (1 nV/√Hz and 2mA drain current); the LSK389 enables power transfer whilst adding almost no noise to the signal. However, the input capacitance of over 20pF causes distortion by increasing the frequency of the input signal if the source impedance is high because the JFET junction capacitances are non-linear.

Introducing the LSK489; though with a slightly higher noise (1.5 nV/√Hz) compared to the LSK389 (1 nV/√Hz) the lower input capacitance of 4pF means it is capable of maintaining its high input impedance as the frequency of the input signal rises. As well as being able to create a circuit that is much less susceptible to intermodulation distortion than one using the LSK389.

This new device designed by Linear Integrated Systems is an N-channel dual low-noise, low capacitance, tightly matched monolithic field effect transistor. Featuring:

- 3ms trans-conductance at 2mA drain current
- 1000 GΩ input impedance
- 60V breakdown voltage
- Gate-drain capacitance of only 1.5pF
- 4pF input capacitance
- 1.5 nV/√Hz noise at 1kHz
- Best low-noise/low-capacitance combination in the industry
- Lowest input capacitance per unit gate length in the industry
- Lowest noise for a given gate length in the industry
- Tight V_{gs} matching at operating bias

Applications such as 48V phantom-powered circuits, like those used in microphone preamplifiers would benefit from these features. For numerous audio and instrumentation applications, the low operating V_{gs}, high *gm*, tight matching, low noise and low capacitance would be very well suited. Not only this but sensor technologies including; piezo, quartz, condenser, electret and MEMs devices would also benefit from the features of the LSK489, in terms of low input capacitance and low noise. Electrometer applications would also benefit greatly.

JFET operation

The equation below describes the DC operation of a JFET. The term β is the trans-conductance coefficient of the JFET.

$$I_d = \beta(V_{gs} - V_T)^2$$

At $V_{gs} = 0$, we have I_{dss}:

$$I_{dss} = \beta(V_T)^2$$

β can be seen from I_{dss} and V_T to be:

$$\beta = I_{dss}/(V_T)^2$$

The operating trans-conductance *gm* is easily seen to be:

$$gm = 2 * \sqrt{\beta * I_d}$$

The value of Beta for LSK489 is about 1.2e-3.

JFET amplifier noise

JFET noise results primarily from *thermal channel noise.* The noise relation for a JFET is remarkably similar to the shot noise source for a BJT.

LSK489 noise advantage

The 4 major sources of noise in JFETS; the first two are largely fundamental to the device, the second two are largely the result of device imperfections:

- Thermal channel noise
- Gate current shot noise
- 1/f noise
- Generation-recombination noise

Thermal channel noise

As discussed above, is akin to the Johnson noise of the resistance of the channel. However, it is important to recognize that the channel is not acting like a resistor in the saturation region where JFETs are usually operated. The channel is operating as a doped semiconductor whose conduction region is pinched off by surrounding depletion regions to the point where the current is self-limiting. Conduction is by majority carriers. The constant 0.67 in the equation where $r_n = 0.67/gm$ is largely empirical, can vary with the individual device geometry and is often a bit smaller than 0.67. However, it is unusual for the constant to be less than 0.5.

Gate shot noise current

JFET input current noise results from the shot noise associated with the gate input junction leakage current. This noise is normally very small, on the order of fA per √Hz. It can usually be neglected. However, in extremely high-impedance circuits and/or at very high temperatures, this noise must be taken into account. Shot noise increases as the square root of DC current. A useful relationship is that $I_{shot} = 0.57pA/\sqrt{Hz}/\sqrt{\mu A}$. Alternately, $I_{shot} = 0.57fA/\sqrt{Hz}/\sqrt{pA}$.

I/F noise

At very low frequencies the input noise power of a JFET rises as the inverse of frequency. That is why this noise is referred to as 1/f noise. When expressed as noise voltage, this means that the noise rises at a rate of 3dB/octave as frequency decreases. In a good JFET, the 1/f spot noise at 10Hz may be twice the spot noise at 1kHz (up 6dB) when expressed as nV/√Hz. The noise might typically be up by 3dB at 40Hz. 1/f noise is associated with imperfections in the fabrication process, such as imperfections in the crystal lattice.2 The improved processing of the
LSK489 contributes to reduced 1/f noise.

Generation-recombination noise

A less-known source of voltage noise results from carrier generation-recombination in the channel of the JFET. This is referred to as G-R noise. This excess noise is governed by fluctuation in the number of carriers in the channel and the lifetime of the carriers. G-R noise manifests itself as drain current noise. When referred back to the input by the trans-conductance of the JFET, it is expressed as a voltage noise.

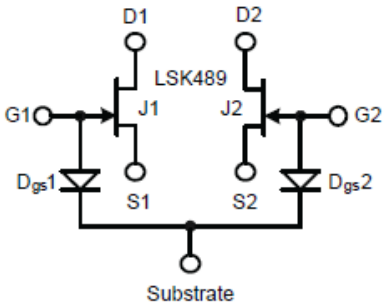
LSK489 noise improvement

The LSK489 noise advantage derives from the process improvements that reduce device imperfections, which create G-R noise and 1/f noise, these include crystal lattice damage and charge trap sites. This meaning that all JFETS are not as quiet as they can be. Where the LSK489 is involved the improvements made are the reduction of both 1/f noise and G-R noise.
The geometry and electrical performance of the LSK489 are essentially the same as the LS844; the only main difference is the more advanced processing that reduces device imperfections as well as the superior noise performance of the LSK489.

The common substrate

The LSK489 is a monolithic dual JFET which means the substrate is shared between the two integrated JFET devices. The two gates are isolated from the common substrate; the anodes are connected to the gates, whilst the cathodes are connected to the common substrate.

The isolated gates are shown in the figure below;

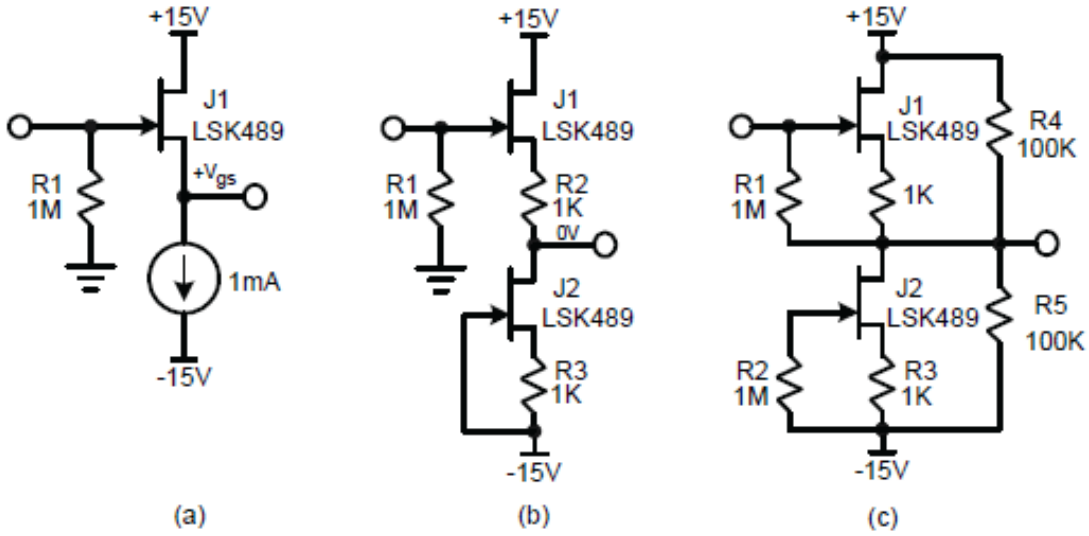


LSK489 Common Substrate

The substrate is not normally accessible and it harmlessly floats, in some applications this needs to be taken into consideration. The 6-pin versions of the LSK489 simply floats the substrate, the 8-pin SOIC package brings out the substrate for connection.

JFET buffers

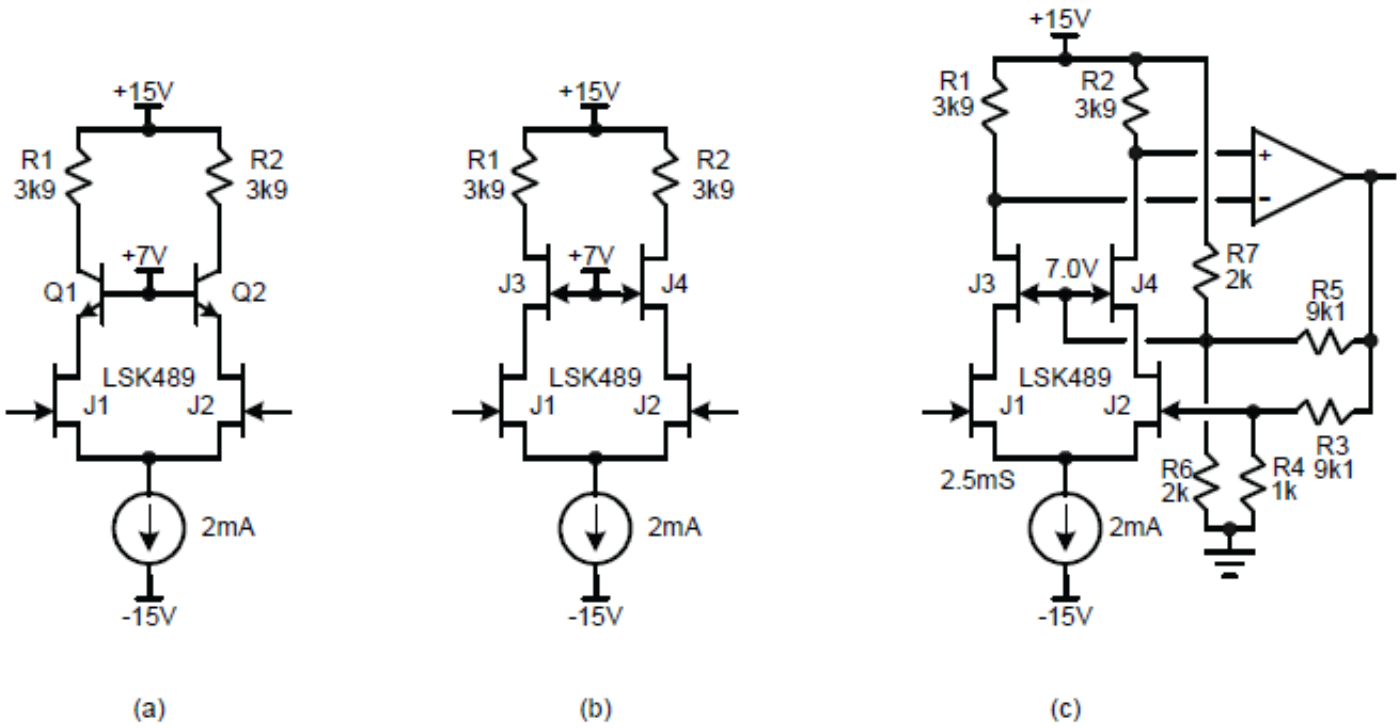
The figure below shows the LSK489 connected as a simple unity-gain source follower buffer. In (a) an output voltage offset equal to Vgs will result. If a dual JFET like the LSK489 is used, the circuit in (b) can be used. J2 acts as the pull-down current source. Because of the tight matching between J1 and J2, the same Vgs will appear across R2 and R3, resulting in an output voltage with nearly zero offset. A circuit like this built with a randomly selected LSK489 exhibited offset of only 5mV. R3 can be conveniently trimmed to adjust for zero offset. In (c) the gate bias resistor R1 has been bootstrapped to provide higher input resistance. R4 and R5 help stabilize the output voltage to near 0V. Here resistor R2 creates the same voltage offset in the gate of J2 as exists in the gate circuit of J1.



LSK489 Source Followers

The figures below show differential CFP FET Buffer; (a) illustrates a differential buffer with low output impedance and low distortion. The key to this design is that each JFET is connected in a complementary feedback pair (CFP) configuration with a PNP transistor, greatly augmenting its effective trans-conductance and providing distortion-reducing local negative feedback. Notice that the PNP transistors are actually connected as a differential pair, providing additional common-mode rejection. For a given choice of R3 and R4, the value of the current sources can be chosen to make the common-mode DC offset at the output fairly small. If the current sources are controlled by common-mode feedback from the outputs, common mode offset can be made very small.

The figure (b) shows how the differential JFET buffer can be used to build an audio power amplifier with very high impedance differential inputs by buffering the relatively low input impedance presented by the power amplifier connected as a differential amplifier.



Differential CFP FET Buffer

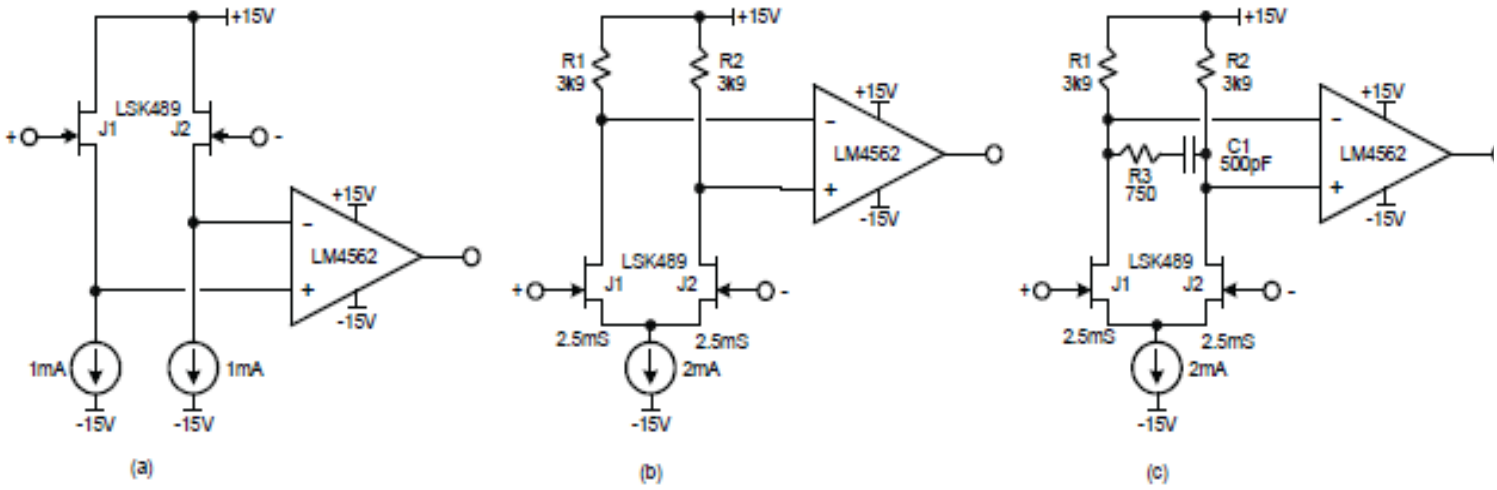
JFET hybrid op amps

The idea of combining the low noise and simplicity of a BJT op amp with the high input impedance of a JFET input would be ideal, as the IC JFET op amps offer many advantages over BJT op amps, including the absence of input bias current and input noise current. However, they have a greater input voltage noise of no better than 8 nV/√Hz. Low-noise BJT op amps easily achieve input voltage noise levels of 1.5 nV/√Hz. The figure below shows several ways in which a high-impedance JFET input can be added to a BJT op amp so as to reap the advantages of both technologies.

In (a) a pair of source followers is simply put in front of the op amp, eliminating the BJT input bias current and input noise current. This arrangement has the disadvantage that the input noise of the op amp adds to that of the JFETs.

In (b) a JFET differential pair with a gain of 10X is placed in front of the op amp. The gain of the JFET stage swamps out the noise contribution of the op amp and increases total open‐loop gain by 20dB. If a unity-gain compensated op amp is used, the arrangement must be used with closed loop gain greater than 10 for stability. In this case, a 20dB gain stage can be made that has the same high open-loop gain as the op amp were it used by itself in a unity-gain configuration. In some cases the extra pole created at the input of the op amp may require more conservative frequency compensation.

In (c), a compensation arrangement is shown that allows the circuit of (b) to be configured for closed loop gain as low as unity. This is accomplished by R3 and C1, which add a pole-zero pair that decreases open-loop gain by 20dB at high frequencies well before the unity loop gain frequency is reached. The overall effect is like that of so-called two-pole compensation (TPC) sometimes used in feedback amplifiers to achieve higher loop gain at lower frequencies.



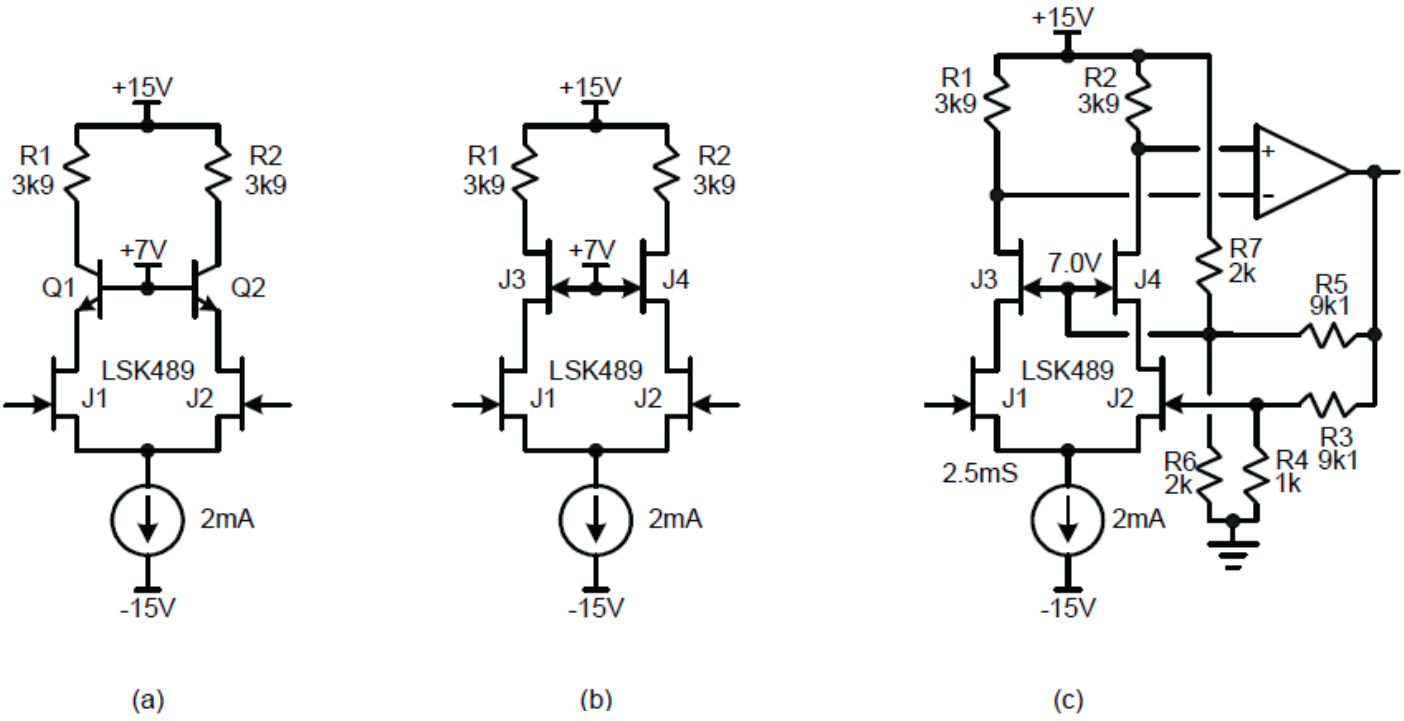
JFET Op Amps

However, with this arrangement, when used at low closed-loop gain, the circuit would be susceptible to latch-up. If the gate of J2 gets driven out to the point where it runs out of drain voltage headroom, the circuit may latch to the positive rail.

Cascoded JFETs

Single-ended and differential JFET amplifier stages are often cascaded in order to add voltage headroom. The cascade device can be either a BJT or another JFET, if the cascade device is a JFET, all of the signal current from the amplifying JFET passes through the cascade devices and no noise is added to the signal. If the cascade device is a BJT, some noise will be added as a result of base current noise flowing from the base to the cascade reference voltage, which adds noise to the signal. This noise must then be put into perspective in comparison with the noise of the amplifying JFET, which can be evaluated by simulation. It is important that the BJT cascade transistor be a low-noise device with high beta.

The figure below shows some simple circuits where the amplifying JFET is cascoded. Sometimes it is necessary to cascode a JFET in order to achieve higher bandwidth by eliminating the Miller effect multiplication of the gate-drain capacitance, even in cases where C_{rss} is already low as with the LSK489. Cascoding may also be necessary when higher-voltage rails are used or when it is desirable to keep the drain-source voltage of the amplifying JFETs small to minimize dissipation or noise.



JFET Cascodes

The figure (a) shows a conventional arrangement where bipolar transistors are used for the cascade function. Some shot noise from the base current is added to the signal. In (b), JFETs are used for the cascodes, largely eliminating any noise penalty from the use of a cascode.

The circuit in (c) bootstraps the drains of J1 and J2 so as to nearly eliminate the effective input capacitance from C_{rss}. This is done by driving the gates of cascodes J3 and J4 with a replica of the feedback signal that is fed to the gate of J2. This is referred to as a *driven cascode*. Although the cascode circuits illustrated here are all differential cascodes, all of the principles and techniques apply to single-ended cascode circuits as well.

Phono preamp

When using high-performance moving magnet (MM) phono preamplifiers, the LSK489 would be an ideal option. While achieving low noise it can also present very high input impedance to the MM cartridge. BJT designs suffer from input noise current; however the JFET design does not have this problem due to the absence of the input bias current. This helps in making the JFET even more attractive, as well as the resistance to EMI and a soft overload characteristic contributing also.

Dynamic microphone preamp

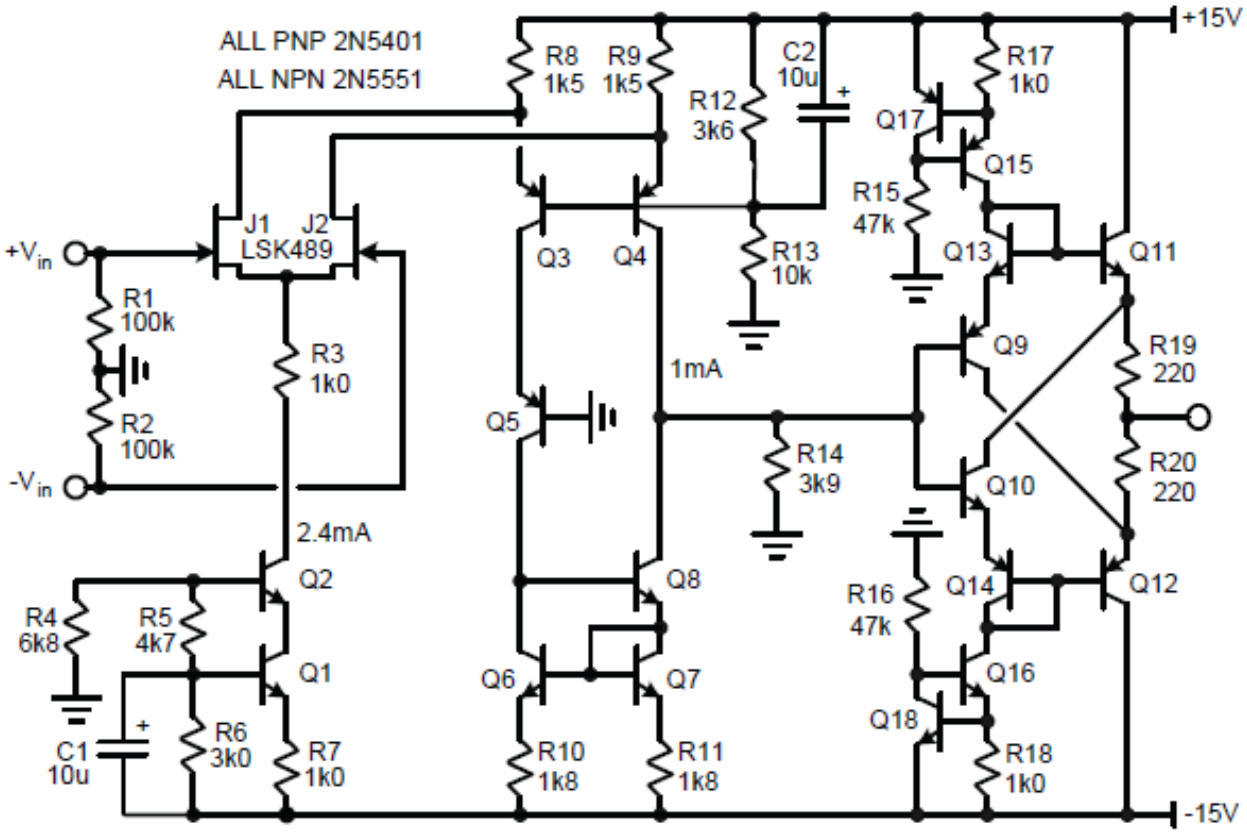
The requirements for a dynamic microphone preamp are similar to that of the phono preamp, in the sense of the voltage levels and source impedance, low input voltage and current noise is also important. The microphone preamp does not require equalization, however a balanced input must be accepted and also have a large controllable gain range. The LSK489's features of low noise and low input capacitance make it an ideal device for this application, also due to its strong resistance to EMI effects and soft overload characteristics, which further enhance sound quality.

Condenser microphone preamp

Just like the dynamic microphone preamp and the phono preamp, the LSK489's combination of low noise and low input capacitance make the ideal device for such applications, this is the same for the input stage of condenser and electret microphones. A condenser microphone typically consists of a condenser microphone capsule and a built-in amplifier. The LSK489 is an advantage here due to the need for low input capacitance.

Discrete JFET amplifier

The figure below shoes a discrete JFET amplifier that employs a folded cascode and a diamond buffer output stage. As shown the amplifier is operated open-loop at a gain of about 10, as determined by shunt resistor R14. The amplifier in this configuration offers a true balanced high-impedance input, exceptional resistance to EMI and a very soft overload characteristic. The amplifier can also be used as an operational amplifier with fairly high open-loop gain if R14 is removed and suitable feedback compensation is added. In any configuration, the use of the folded cascode architecture offers wide bandwidth.

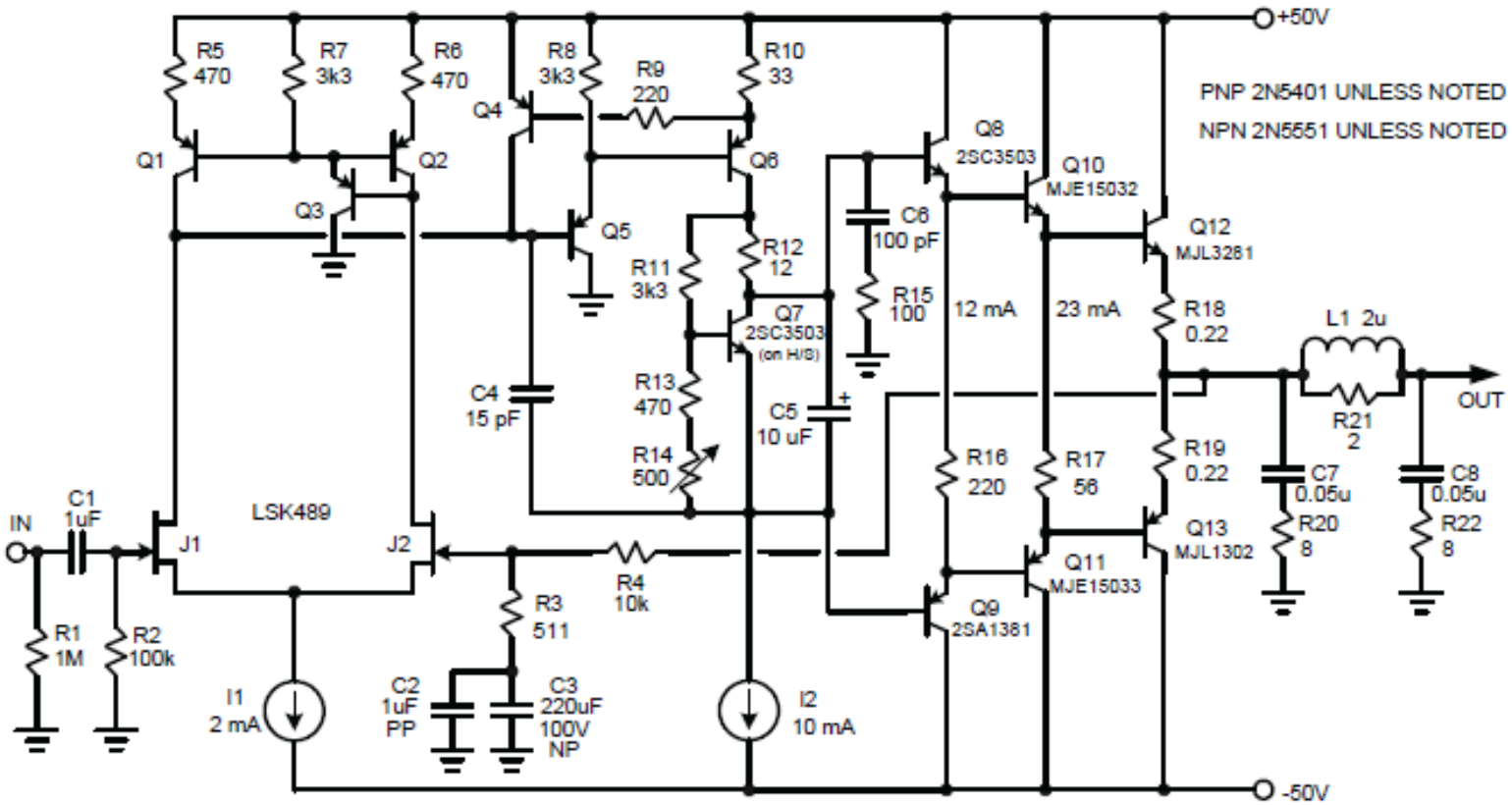


JFET Discrete Amplifier

Power amplifier with JFET input

Dual JFETs like the LSK489 provide a better alternative in the input stage for an audio power amplifier; many believe the sound is better as well as its softer overloading characteristic. Its superior resistance to EMI is also seen as being very important. The absence of input bias current for the JFET often has advantages in DC offset control and selection of input stage operating impedances. It is still important to achieve low noise because there is no volume control in the power amplifier to reduce noise from the input stage.

The figure below shows a simple100 watt audio power amplifier with a JFET input stage incorporating an LSK489 differential pair. Input noise is only 6 nV/√Hz. The 60V breakdown of the LSK489 allows the use of a JFET input without a cascode for amplifiers with nominal rail voltages of up to 50V, assuming that the rail voltages do not exceed 60V under worst case light-loading and high mains voltage conditions.



Power Amplifier

Conclusion

Due to the low noise, low input capacitance and tight matching features of the LSK489, it is an ideal candidate for many high-frequency circuits as well as numerous audio and instrumentation applications.

References

[1]. Designing Audio Power Amplifiers, Bob Cordell, McGraw-Hill, 2010.

[2]. Alicja Konczakowska and Bogdan M. Wilamowski, *Noise in Semiconductor Devices,* Chapter 11 in *Industrial Electronics Handbook,* vol. 1, *Fundamentals of Industrial Electronics*, 2nd edition, CRC Press 2011.

[3]. Bob Cordell, *VinylTrak – a full-featured MM/MC phono preamp,* Linear Audio, vol. 4, September 2012, www.linearaudio.net

[4]. Website: www.cordellaudio.com