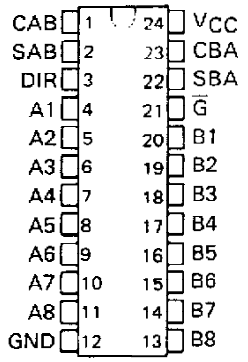
SN54LS646 THRU SN54LS649
SN74LS646 THRU SN74LS649
OCTAL BUS TRANSCEIVERS AND REGISTERS

D2661, DECEMBER 1982 – REVISED MARCH 1988

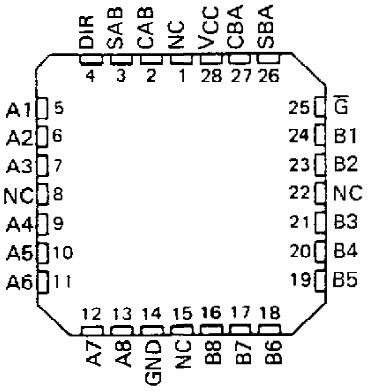
- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True or Inverting Data Paths**
- **Choice of 3-State or Open-Collector Outputs**
- **Included Among the Package Options Are Compact 24-pin 300-mil-Wide Plastic and Ceramic DIPs, Ceramic Chip Carriers, and Plastic "Small Outline" Packages**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	OUTPUT	LOGIC
'LS646	3-State	True
'LS647	Open-Collector	True
'LS648	3-State	Inverting
'LS649	Open-Collector	Inverting

SN54LS' . . . JT PACKAGE
SN74LS' . . . DW OR NT PACKAGE
(TOP VIEW)

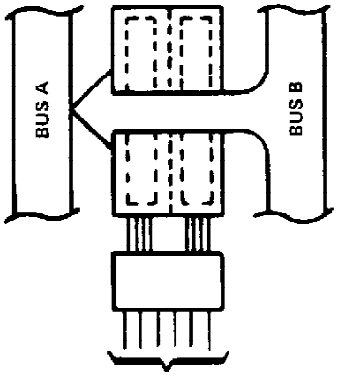


SN54LS' . . . FK PACKAGE
(TOP VIEW)



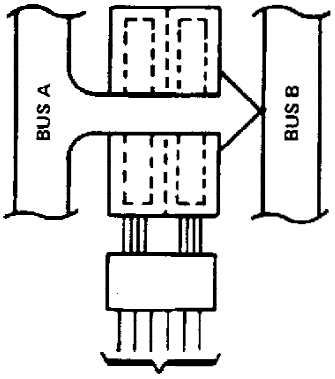
description

These devices consist of bus transceiver circuits with 3-state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.



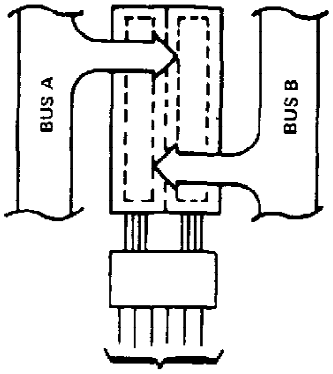
(21)	(3)	(1)	(23)	(2)	(22)
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	L	X	H or L	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



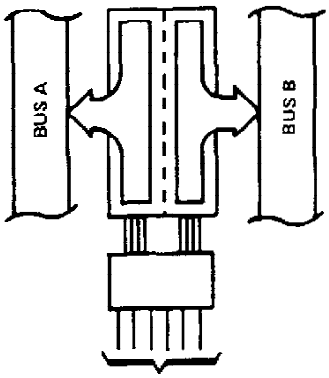
(21)	(3)	(1)	(23)	(2)	(22)
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	H	H or L	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



(21)	(3)	(1)	(23)	(2)	(22)
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



(21)	(3)	(1)	(23)	(2)	(22)
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	L	X	X	X	H
L	H	X	X	H	X

TRANSFER
STORED DATA
TO A OR B

Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode (control $\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0° to 70°C.

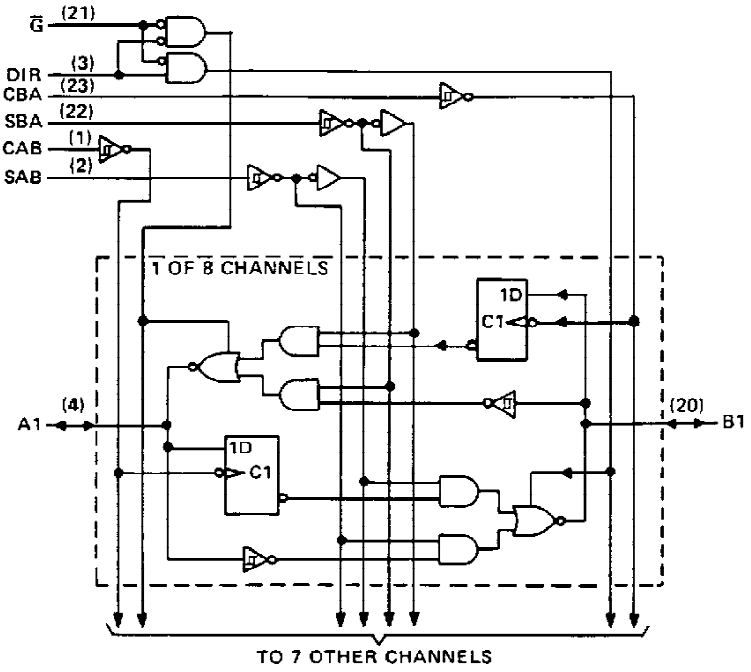
FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	LS646, LS647	LS648, LS649
X	X	↑	X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X	↑	X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	H or L	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	H or L	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	X	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

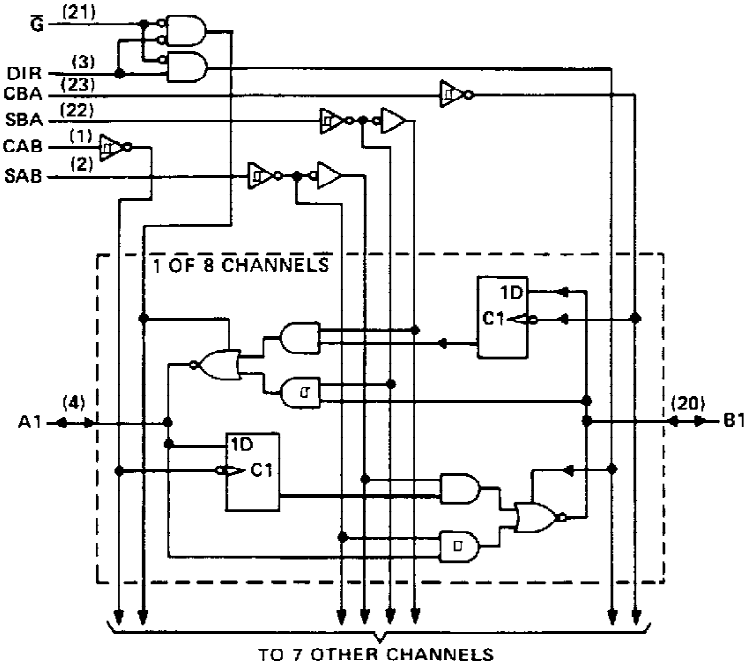
† The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic diagrams (positive logic)

'LS646, 'LS647



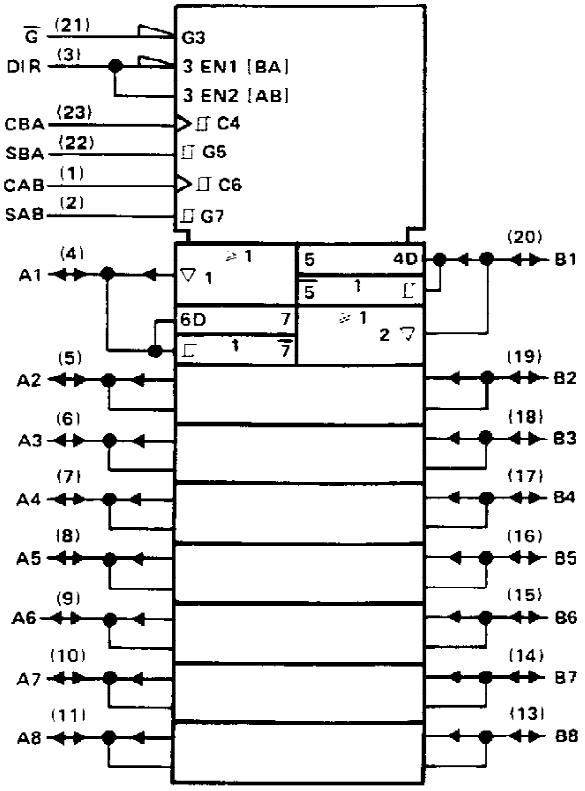
'LS648, 'LS649



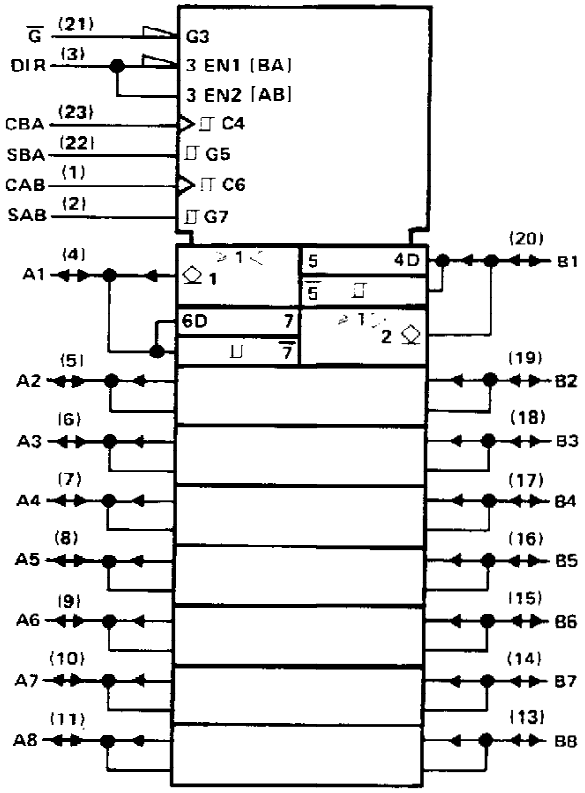
Pin numbers shown are for DW, JT, and NT packages.

logic symbols†

'LS646



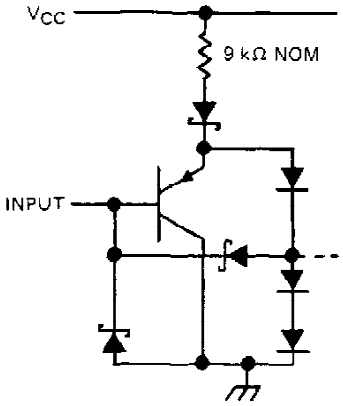
'LS647



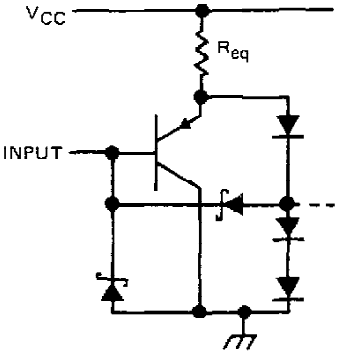
†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

schematics of inputs and outputs

EQUIVALENT OF DIRECTION INPUTS

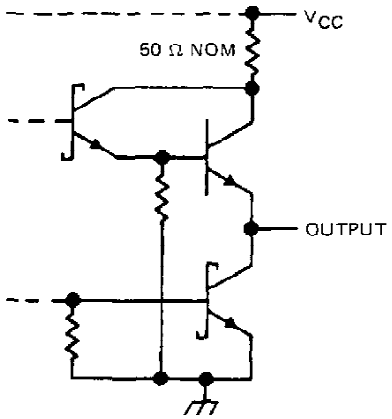


EQUIVALENT OF ALL OTHER INPUTS

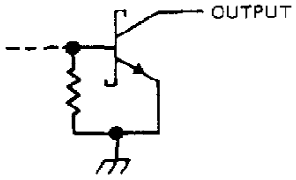


A and B: R_{eq} = 15 kΩ NOM
$\overline{G}$, CAB and CBA: R_{eq} = 10 kΩ NOM
SAB and SBA: R_{eq} = 6 kΩ NOM

TYPICAL OF ALL 'LS646, 'LS648 OUTPUTS



TYPICAL OF ALL 'LS647, 'LS649 OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54LS646, SN54LS648 . . . . . −55°C to 125°C
SN74LS646, SN74LS648 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54LS646/648			SN74LS646/648			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.5			0.6	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration	CBA or CAB high	15			15			ns
		CBA or CAB low	30			30			
		Data high or low	30			30			
t_{su}	Setup time before CAB↑ or CBA↑	A or B	15			15			ns
t_h	Hold time after CAB↑ or CBA↑	A or B	0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS646/648			SN74LS646/648			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
Hysteresis ($V_{T+}-V_{T-}$)	A or B input	V_{CC} = MIN		0.1	0.4		0.2	0.4		V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
			I_{OH} = −12 mA	2						
			I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
	A or B ports	V_{CC} = MAX, V_I = 5.5 V				0.1			0.1	
I_{IH}	Control inputs	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
	A or B ports¶					20			20	
I_{IL}	Control inputs	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
	A or B ports¶					−0.4			−0.4	
I_{OS}§		V_{CC} = MAX, V_O = 0 V		−40		−225	−40		−225	mA
I_{CC}	LS646	V_{CC} = MAX	Outputs high		91	145		91	145	mA
			Outputs low		103	165		103	165	
			Outputs disabled		103	165		103	165	
	LS648		Outputs high		91	145		91	145	
			Outputs low		103	165		103	165	
			Outputs disabled		120	180		120	180	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
¶ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS646			'LS648			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CAB or CBA	A or B	R_L = 667 Ω, C_L = 45 pF, See Note 2		15	25		15	25	ns
t_{PHL}					23	35		24	40	ns
t_{PLH}	A or B	B or A			12	18		12	18	ns
t_{PHL}					13	20		15	25	ns
t_{PLH}	SAB or SBA† with Bus input high	A or B			26	40		37	55	ns
t_{PHL}					21	35		24	40	ns
t_{PLH}	SAB or SBA† with Bus input low				33	50		26	40	ns
t_{PHL}					14	25		23	40	ns
t_{PZH}	$\overline{G}$	A or B			33	55		30	50	ns
t_{PZL}					42	65		37	55	ns
t_{PZH}	DIR				28	45		23	40	ns
t_{PZL}					39	60		30	45	ns
t_{PHZ}	$\overline{G}$	A or B	R_L = 667 Ω, C_L = 5 pF, See Note 2		23	35		28	45	ns
t_{PLZ}					22	35		22	35	ns
t_{PHZ}	DIR				20	30		24	35	ns
t_{PLZ}					19	30		19	30	ns

† These parameters are measured with the internal output state of the storage register opposite to that of the input.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.