Title	***Engineering Prototype Report for ADAK-91B 16.8W Converter Using TNY279PN (TnySwitch®-III)***
Specification	85–265 VAC Input, 12 V, 1.4A, 16.8W Output
Application	Evaluation Board for TNY279PN
Author	David Gale
Document Number	ADAK-91B
Date	13th November 2006
Revision	0.3

Summary and Features

- *EcoSmart®* – Meets all existing and proposed harmonized energy efficiency
- standards including: CECP (China), CEC, EPA, AGO, European Commission No-load consumption 150 mW at 265 VAC (no bias winding required)
- 79% active-mode efficiency (exceeds standards requirement of 74%)
- BP/M capacitor value selects MOSFET current limit for greater design flexibility
- Tightly toleranced I^2f parameter (–10%, +12%) reduces system cost:
  - Increases MOSFET and magnetics power delivery
  - Reduces overload power, which lowers output diode and capacitor costs
- Integrated *TinySwitch-III* Safety/Reliability features:
  - Accurate (± 5%), auto-recovering, hysteretic thermal shutdown function maintains safe PCB temperatures under all conditions
  - Auto-restart protects against output short circuit and open loop fault conditions
  - 3.2 mm creepage on package enables reliable operation in high humidity and high pollution environments
- Meets EN550022 and CISPR-22 Class B conducted EMI with >10 dBµV margin

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This report describes a universal input, 12V, 1400mA flyback power supply using a TNY279PN device from the *TinySwitch-III* family of ICs. It contains the complete specification of the power supply, a detailed circuit diagram, the entire bill of materials required to build the supply, extensive documentation of the power transformer, along with test data and oscillographs of the most important electrical waveforms. The board provides a number of user configurable options, which are designed to demonstrate the features and flexibility of the *TinySwitch-III* family. This includes easy adjustment of the device current limit for increased output power.

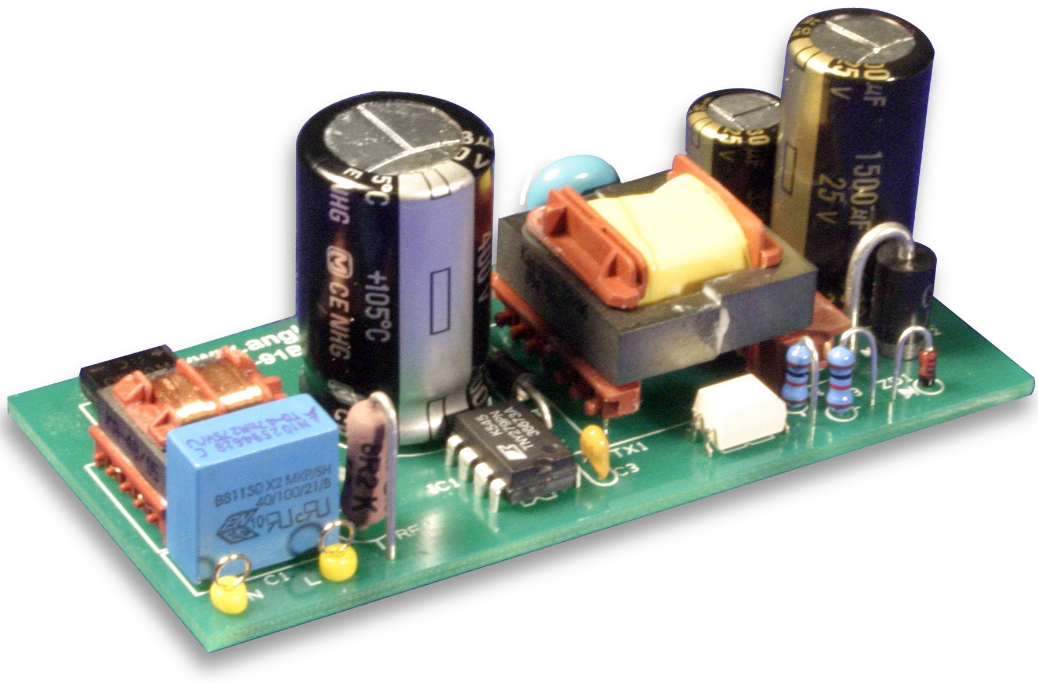

Figure 1 – ADAK-91B Populated Circuit Board Photograph

2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				0.3	W	
Output						
Output Voltage 1	V_{OUT1}	10.8	12	13.2	V	± 5%
Output Ripple Voltage 1	$V_{RIPPLE1}$		100		mV	20 MHz bandwidth
Output Current 1	I_{OUT1}		1400		mA	
Total Output Power						
Continuous Output Power	P_{OUT}			16.8	W	
Efficiency						
Full Load	η		80		%	Measured at P_{OUT} 25 °C
Average Efficiency			79			
Required average efficiency at 25%, 50% 75% and full load	η_{cec}	74.4				As per CEC As per CEC, Californian Energy Commission, and Energy Star
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				>10dB Margin
Surge		1.5			kV	1.2/50 µs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω
Ambient Temperature	T_{AMB}	0		40	°C	Free convection, sea level

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3 Schematic

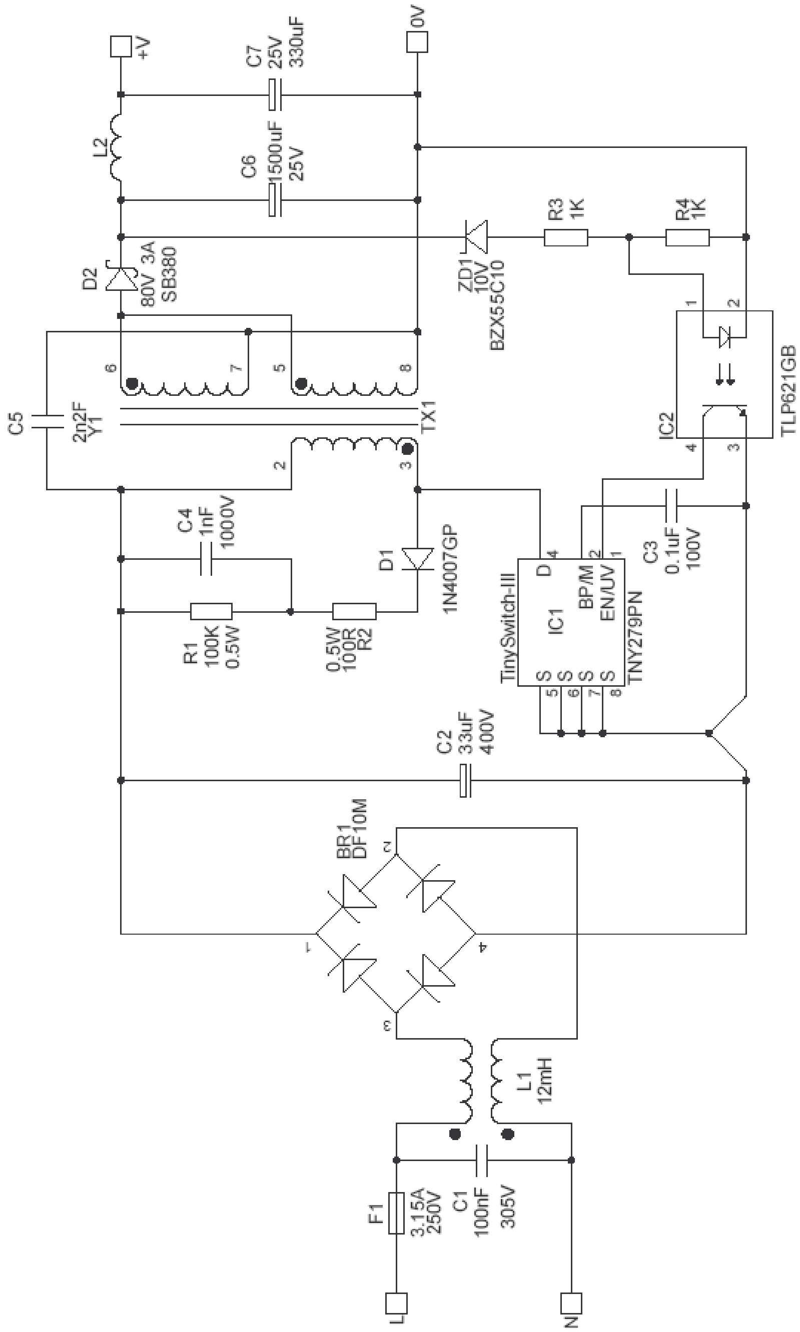

Figure 2 – ADAK-91B Schematic.

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4 Circuit Description

This flyback power supply was designed around the TNY279P (IC1 in Figure 2). The output voltage is sensed and fed back to IC1 through optocoupler IC2. That feedback is used by IC1 to maintain constant voltage (CV) regulation of the output.

4.1 Input Rectification and Filtering

Bridge rectifier BR1 rectifies the AC input. Capacitor C2 filters the rectified DC. Common mode choke, L1, and X1 Rated capacitor, C1 form an effective filter differential and common mode conducted EMI.

4.2 TNY279P Operation

The TNY279P device (IC1) integrates an oscillator, a switch controller, startup and protection circuitry, and a power MOSFET, all on one monolithic IC.

One side of the power transformer (TX1) primary winding is connected to the positive leg of C2, and the other side is connected to the DRAIN pin of IC1. At the start of a switching cycle, the controller turns the MOSFET on, and current ramps up in the primary winding, which stores energy in the core of the transformer. When that current reaches the limit threshold, the controller turns the MOSFET off. Due to the phasing of the transformer windings and the orientation of the output diode, the stored energy then induces a voltage across the secondary winding, which forward biases the output diode, and the stored energy is delivered to the output capacitor. When the MOSFET turns off, the leakage inductance of the transformer induces a voltage spike on the drain node. The amplitude of that spike is limited by an RCD clamp network that consists of D1, C4 and R1. Resistor R2 also limits the reverse current that flows through D1 when the MOSFET turns on. This allows a slow, low-cost, glass passivated diode (with a recovery time of 2µs.) to be used for D1, which improves conducted EMI and efficiency.

Using ON/OFF control, IC1 skips switching cycles to regulate the output voltage, based on feedback to its EN/UV pin. The EN/UV pin current is sampled, just prior to each switching cycle, to determine if that switching cycle should be enabled or disabled. If the EN/UV pin current is <115 µA, the next switching cycle begins, and is terminated when the current through the MOSFET reaches the internal current limit threshold. To evenly spread switching cycles, preventing group pulsing, the EN pin threshold current is modulated between 115 µA and 60 µA based on the state during the previous cycle. A state-machine within the controller adjusts the MOSFET current limit threshold to one of four levels, depending on the load being demanded from the supply. As the load on the supply drops, the current limit threshold is reduced. This ensures that the effective switching frequency stays above the audible range until the transformer flux density is low. When the standard production technique of dip varnishing is used for the transformer, audible noise is practically eliminated.

4.3 Output Rectification and Filtering

Diode D2 rectifies the output of TX1. Output voltage ripple was minimized by using a low ESR capacitor for C6 (see Section 6 for component part numbers and values). A post filter (ferrite bead L2 and C7) attenuates the high frequency switching noise.

4.4 Feedback and Output Voltage Regulation

The supply's output voltage regulation set point is set by the voltage that develops across Zener diode ZD1, R3 and the LED in opto-coupler IC2. The value of R4 was calculated to bias ZD1 to about 0.5 mA when it starts to conduct. This ensures that it is operating close to its rated knee current. Resistor R3 limits the maximum current during load transients. The values of R4 and R3 can both be varied slightly to fine-tune the output regulation set point. When the output voltage rises above the set point, the LED in IC2 becomes forward biased. On the primary side, the photo-transistor of IC2 turns on and draws current out of the EN/UV pin of IC1. Just before the start of each switching cycle, the controller checks the EN/UV pin current. If the current flowing out of the EN/UV pin is greater than 115 µA, that switching cycle will be disabled. As switching cycles are enabled and disabled, the output voltage is kept very close to the regulation set point. For tighter regulation accuracy, a shunt reference IC such as a TL431 can be used in place of ZD1.

4.5 EMI Design Aspects

A common mode input filter (C1, and L1) attenuates conducted and differential mode EMI noise. As this design uses a standard transformer, a Y1 rated safety capacitor is also required to attenuate common mode noise generated by parasitic currents within the transformer. If Shielding techniques (*E-Shield*™) were used in the construction of TX1 to reduce common mode EMI displacement currents, it is likely that the EMC filtering could be changed to a simple PI filter, and the value of the Y capacitor could most likely be reduced. These techniques produce excellent conducted EMI performance (see Section 12 of this report).

4.6 Peak Primary Current Limit Selection

The value of the capacitor installed on the BP/M pin allows the current limit of IC1 to be selected. The power supply designer can change the current limit of the MOSFET by simply changing the capacitance value connected to the BP/M pin (see the *TinySwitch-III* data sheet for more details).

- Installing a 0.1 uF capacitor on the BP/M pin selects the standard current limit of the IC, and is the normal choice for enclosed adapter applications.
- Installing a 1 uF capacitor on the BP/M pin reduces the MOSFET current limit, which lowers conduction losses and improves efficiency (at the expense of reducing the maximum power capability of the IC).
- A 10 uF capacitor on the BP/M pin will raise the MOSFET current limit and extend the power capability of the IC (for higher power applications that do not have the thermal constraints of an enclosed adapter, or to supply short-duration, peak load demands).

The demonstration board comes with a 0.1 µF capacitor installed as C3, which causes IC1 to select the standard current limit specified in the *C* sheet. If C3 were replaced by a 1uF capacitor, the current limit of IC1 will be the same as the standard current limit for a

TNY278 device. If a 10uF capacitor is installed, the current limit of IC1 will be the same as the standard current limit for a TNY280 device. The flexibility of this option enables the designer to do three things. First, it allows the designer to measure the effect of switching to an adjacent device without actually removing and replacing the IC. Second, it allows a larger device to be used with a lower current limit, for higher efficiency. Third, it allows a smaller device to be used with a higher current limit in a design when higher power is not required on a continual basis, which effectively lowers the cost of the supply.

4.8 UV Lockout

This board does not implement UV lockout, but if required, a single resistor to sample the DC rectified mains voltage can implement this feature. For more details see the *TinySwitch-III* data sheet.

4.7 Further design optimisation.

This reference design is intended to demonstrate the capabilities of the *TinySwitch-III* using readily available and standard components. It provides a low risk solution that can be employed with minimal effort. Further optimization is still possible, where higher volumes require lower costs, or where smaller physical size is required. In particular, the following changes should be considered at an early stage.

The use of *E-Shield*TM techniques in the transformer may allow the common mode choke and X capcitor to be removed, and replaced with a simple, lower cost PI filter. The Y capacitor value could be reduced, or possibly removed depending on the effectiveness of the shielding. However, the use of a small value (100pF) Y1 capacitor provides improved EMI consistency if transformer construction variation is a concern.

Additional functions are also available to make use of the enhanced features of the *TinySwitch-III*, and in particular:

- Under-voltage lockout
- Lower No-Load power consumption by using a bias winding
- Over-voltage protection using the bias winding and zener feedback

More information on the above techniques can be found in the PI engineering report for the *TinySwitch-III*, EPR91, which is available as a download from the PI website.

The transformer used in this design is a generic 6-12V transformer, 094.941, and if required, the output can be adjusted via changes to the feedback network. For 3-6V outputs, the transformer can be changed to 094.940.

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5 PCB Layout

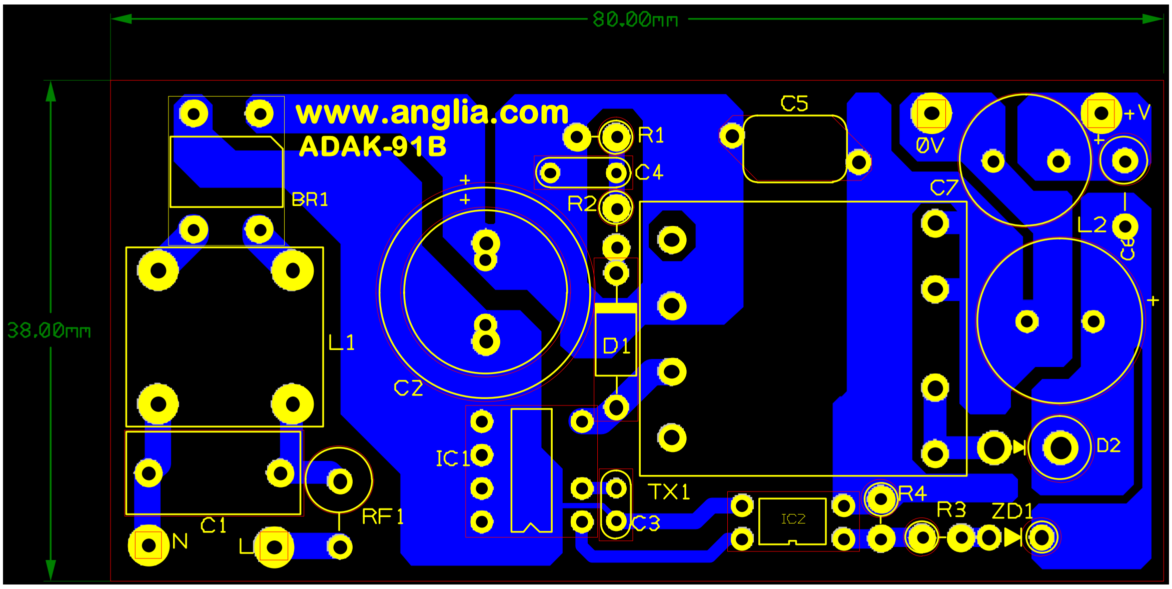

Figure 3 – ADAK-91B Printed Circuit Layout.

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6 Bill Of Materials

REF	Description	Part No.	MFR	QTY
+V	PCB TEST TERMINAL - RED	492051	M-PRO	1
0V	PCB TEST TERMINAL - BLACK	492050	M-PRO	1
L,N	PCB TEST TERMINAL - GREEN	492052	M-PRO	2
BR1	BRIDGE RECTIFIER DF10M 1000V 1A	DF10M	DIODES INC	1
C1	CAPACITOR 100nF 305V AC POLY 10mm	PCX233730104	PILKOR	1
C2	CAPACITOR 33uF 400V NHG SERIES 16x25	ECA2GHG330	PANASONIC	1
C3	CAPACITOR CERAMIC 100nF 100V 10% 2.5mm X7R	096525	CTC	1
C4	CAPACITOR 1nF 1KV CERAMIC	DEBB33A102KA2B	MURATA	1
C5	CAPACITOR 2n2F Y1 250V 20%	DE1E3KX222MA5BA01	MURATA	1
C6	CAPACITOR 1500uF 25V ELECTROLYTIC 12.5X25	EEUFM1E152	PANASONIC	1
C7	CAPACITOR 330uF 25V ELECTROLYTIC 10X12.5	EEUFM1E331	PANASONIC	1
D1	DIODE 1N4007GP DO-41	1N4007GP	INVAC	1
D2	SCHOTTKY DIODE SB380 3A 80V DO27	SB380	INVAC	1
IC1	IC SMPS CONTROLLER TNY277PN DIP-8	TNY279PN	PI	1
IC2	IC TLP621GB OPTO ISOLATOR DIP 4	TLP621GB	TOSHIBA	1
L1	COMMON MODE CHOKE 12mH 540mA	071.921	KASCHKE	1
L2	INDUCTOR RADIAL FERRITE BEAD	BL02RN1R2M2B	MURATA	1
R1	RESISTOR 100K 5% 0.5W C/F	001104A	EUROHM	1
R2	RESISTOR 100R 5% 0.5W C/F	001101A	EUROHM	1
R3, R4	RESISTOR 1K 1% 0.25W M/F	006102DK	EUROHM	2
F1	FUSE 3.15A RADIAL ETF 5MM PITCH	690319	BUSSMAN	1
TX1	TRANSFORMER EF20 SMARTPOWER	094.941	KASCHKE	1
ZD1	ZENER DIODE BZX55C10	BZX55C10	INVAC	1

Note: Depending on the PCB revision, F1 may be marked RF1 on the silkscreen.

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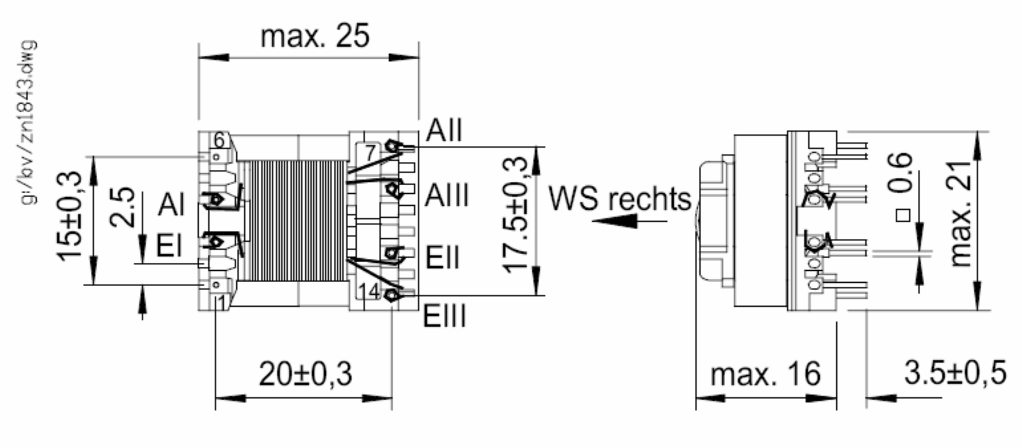
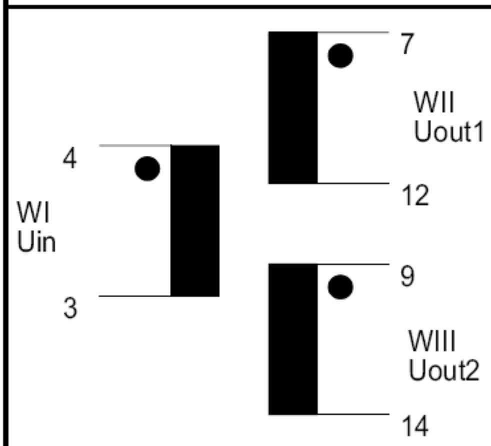
7 Transformer Design

KASCHKE	***Technical Data Sheet***		
	Customer: Kaschke Göttingen	Part designation: SP-E 20/6	Customer part no.: SKNY268-9-14





Core / material / air gap / AL	**E20/6 K2006 or equiv**	
Nominal inductance	**LI = 1,16 mH ± 10%**	
maximum transmissible power	**14W (TNY268 univ.)**	
Working frequency	**132 kHz**	
Transformation ratio	**88:8:8**	
dielctric strength (50Hz/2s)	**WI-WII/WIII=4kVeff/50Hz**	
Nominal Current		
Design in comp. with standard	**S08 EN60950**	
Working / storage temperature	**-25°C- 115°C**	**-25°C- 85°C**
Miscellaneous	**F (DIN 40040)**	

Remarks : **a.) marking**

Measuring device of L: **W&K 3245** | Measuring conditions of L: **50 mV/10 KHz**

Measured quantity	Unit	No. 1	No. 2	No. 3	No. 4	No. 5

Responsible person:	Date:	Design regulation no:	Index:
Uwe Dickhut	. .	**094.941**	**01**

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8 Design Spreadsheet

ACDC_TinySwitch-III_031006; Rev.1.11; Copyright Power Integrations 2006	INPUT	INFO	OUTPUT	UNIT	ACDC_TinySwitch-III_031006_Rev1-11.xls; TinySwitch-III Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					**Customer**
VACMIN	85			Volts	
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	12.00			Volts	Output Voltage (at continuous power)
IO	1.40			Amps	Power Supply Output Current (corresponding to peak power)
Power			16.8	Watts	Continuous Output Power
n	0.70				Efficiency Estimate at output terminals. Under 0.7 if no better data available
Z	0.50				Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC	3.00			mS	Bridge Rectifier Conduction Time Estimate
CIN	33.00		33	uFarads	Input Capacitance
ENTER TinySwitch-III VARIABLES					
TinySwitch-III	**TNY279**		**TNY279**		User defined TinySwitch-III
Chosen Device		*TNY279*			
Chose Configuration	**STD**		Standard Current Limit		Enter "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications)
ILIMITMIN			0.605	Amps	Minimum Current Limit
ILIMITTYP			0.650	Amps	
ILIMITMAX			0.695	Amps	Maximum Current Limit
fSmin			124000	Hertz	Minimum Device Switching Frequency
I^2fmin			50.193	A^2kHz	I^2f (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR	140.00		140	Volts	Reflected Output Voltage (VOR < 135 V Recommended)
VDS			10	Volts	TinySwitch-III on-state Drain to Source Voltage
VD			0.7	Volts	Output Winding Diode Forward Voltage Drop
KP			0.57		Ripple to Peak Current Ratio (KP < 6)
KP_TRANSIENT			0.42		Transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25
ENTER BIAS WINDING VARIABLES					
VB			22.00	Volts	Bias Winding Voltage
VDB			0.70	Volts	
NB			17.32		Bias Winding Number of Turns
VZOV			28.00	Volts	Over Voltage Protection zener diode voltage.
UVLO VARIABLES					
V_UV_TARGET			93.99	Volts	Target DC under-voltage threshold, above which the power supply with start
V_UV_ACTUAL			92.20	Volts	Typical DC start-up voltage based on standard value of RUV_ACTUAL
RUV_IDEAL			3.67	Mohms	Calculated value for UV Lockout resistor

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RUV_ACTUAL			3.60	Mohms	Closest standard value of resistor to RUV_IDEAL
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	EF20		EF20		Enter Transformer Core
Core		*EF20*		*P/N:*	PC40EF20-Z
Bobbin		*EF20_BOBBIN*		*P/N:*	EF20_BOBBIN
AE			0.335	cm^2	Core Effective Cross Sectional Area
LE			4.49	cm	Core Effective Path Length
AL			1570	nH/T^2	Ungapped Core Effective Inductance
BW			12.2	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	3.00		3		Number of Primary Layers
NS	10		10		Number of Secondary Turns

DC INPUT VOLTAGE PARAMETERS					
VMIN			85	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage

CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.65		Duty Ratio at full load, minimum primary inductance and minimum input voltage
IAVG			0.32	Amps	Average Primary Current
IP			0.61	Amps	Minimum Peak Primary Current
IR			0.35	Amps	Primary Ripple Current
IRMS			0.41	Amps	Primary RMS Current

TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			1116	uHenries	Typical Primary Inductance. +/- 12% to ensure a minimum primary inductance of 996 uH
LP_TOLERANCE			12	%	Primary inductance tolerance
NP			110		Primary Winding Number of Turns
ALG			92	nH/T^2	Gapped Core Effective Inductance
BM			2100	Gauss	Maximum Operating Flux Density, BM<3000 is recommended
BAC			600	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1675		Relative Permeability of Ungapped Core
LG			0.43	mm	Gap Length (Lg > 0.1 mm)
BWE			36.6	mm	Effective Bobbin Width
OD			0.33	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.28	mm	Bare conductor diameter
AWG			30	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			102	Cmils	Bare conductor effective area in circular mils
CMA			247	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)

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TRANSFORMER SECONDARY DESIGN PARAMETERS					
ISP			6.67	Amps	Peak Secondary Current
ISRMS			3.32	Amps	Secondary RMS Current
IRIPPLE			3.02	Amps	Output Capacitor RMS Ripple Current
CMS			665	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			21	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)

VOLTAGE STRESS PARAMETERS					
VDRAIN		***Warning***	689	Volts	!!! REDUCE DRAIN VOLTAGE Vdrain<680 Volts. Reduce VOR or Reduce VACMAX – **SEE NOTE BELOW**
PIVS			46	Volts	Output Rectifier Maximum Peak Inverse Voltage

TRANSFORMER SECONDARY DESIGN PARAMETERS					
VO1			12	Volts	Main Output Voltage (if unused, defaults to single output design)
IO1			1.400	Amps	Output DC Current
PO1			16.80	Watts	Output Power
VD1			0.7	Volts	Output Diode Forward Voltage Drop
NS1			10.00		Output Winding Number of Turns
ISRMS1			3.324	Amps	Output Winding RMS Current
IRIPPLE1			3.02	Amps	Output Capacitor RMS Ripple Current
PIVS1			46	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diodes			**SB360, MBR360**		Recommended Diodes for this output
CMS1			665	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			21	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.73	mm	Minimum Bare Conductor Diameter
ODS1			1.22	mm	Maximum Outside Diameter for Triple Insulated Wire

Total power			16.8	Watts	Total Output Power

Note: This design uses a standard transformer intended to provide 6-12V. At 12V output, the reflected voltage (VOR) is relatively high at 140V, and leads to a high calculated drain voltage of 689V. For this design, the snubber circuit is very active, and in practice this voltage is never reached. Ideally the transformer would be optimized to have a lower VOR. This would allow a less aggressive snubber circuit to be used, which would improve efficiency, while still maintaining a good drain voltage margin.

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9 Performance Data

All measurements performed at room temperature, 50 Hz input frequency.

9.1 Efficiency

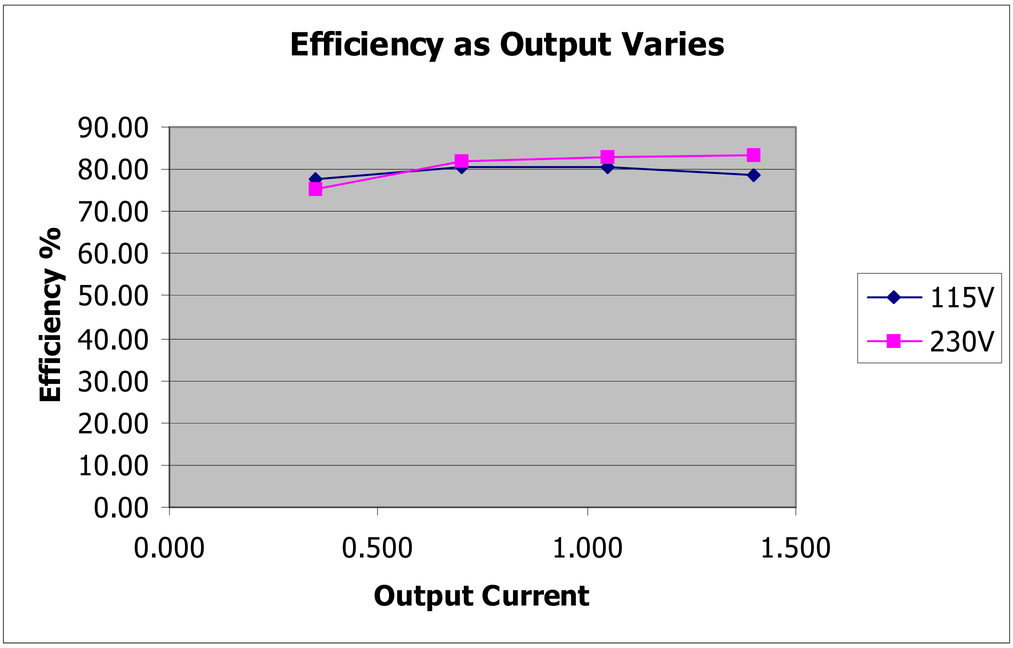

Figure 4- Efficiency vs. Input Voltage, Room Temperature, 50 Hz.

9.1.1 Active Mode CEC Measurement Data

All single output adapters, including those provided with products, for sale in California after January 1st, 2007 must meet the California Energy Commission (CEC) requirement for minimum active mode efficiency and no load input power. Minimum active mode efficiency is defined as the average efficiency at 25, 50, 75 and 100% of rated output power with the limit based on the nameplate output power:

Nameplate Output (P_O)	**Minimum Efficiency in Active Mode of Operation**
< 1 W	$0.49 \times P_O$
≥ 1 W to ≤ 49 W	$0.09 \times \ln(P_O) + 0.49$ [ln = natural log]
> 49 W	0.84 W

For adapters that are single input voltage only then the measurement is made at the rated single nominal input voltage (115 VAC or 230 VAC), for universal input adapters the measurement is made at both nominal input voltages (115 VAC and 230 VAC).

To meet the standard the measured average efficiency (or efficiencies for universal input supplies) must be greater than or equal to the efficiency specified by the CEC/Energy Star standard.

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Name Plate Output Power	16.8	[W]
Required Average Efficiency	74.39	%
	115V	230V
Percent Of Full Load	[V]	[V]
25 %	77.66	75.52
50 %	80.42	82.07
75 %	80.61	82.94
100 %	78.59	83.16
Average Efficiency	79.32	80.93
Result/Verdict	PASS	PASS

Figure 5- CEC Efficiency Chart 50 Hz.

More states within the USA and other countries are adopting this standard, for the latest up to date information please visit the PI Green Room:
http://www.powerint.com/greenroom/regulations.htm

9.2 No-load Input Power

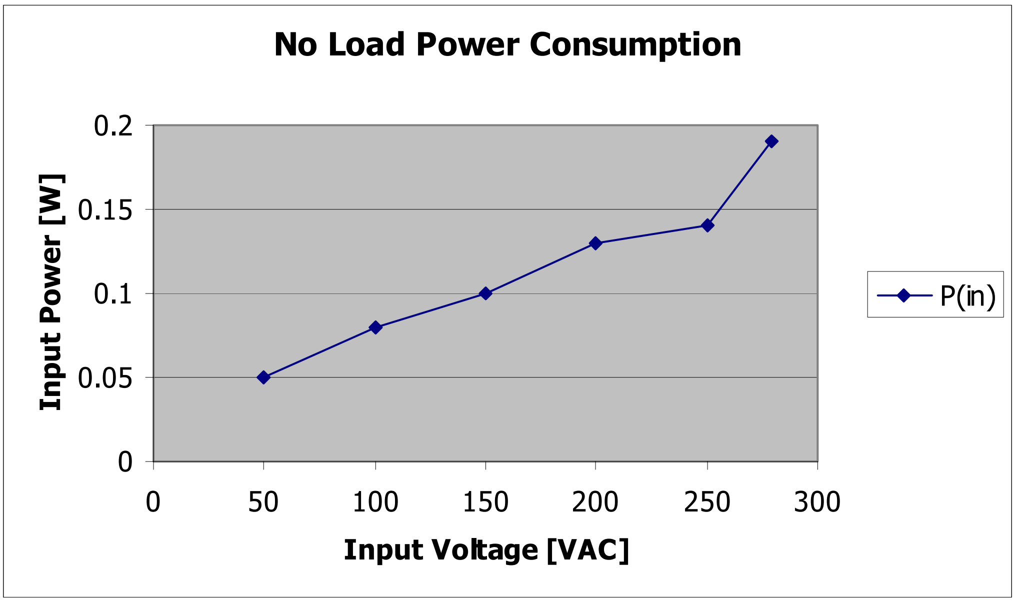

Figure 6- Zero Load Input Power vs. Input Line Voltage, Room Temperature, 50 Hz.

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9.3 Regulation

9.3.1 Load

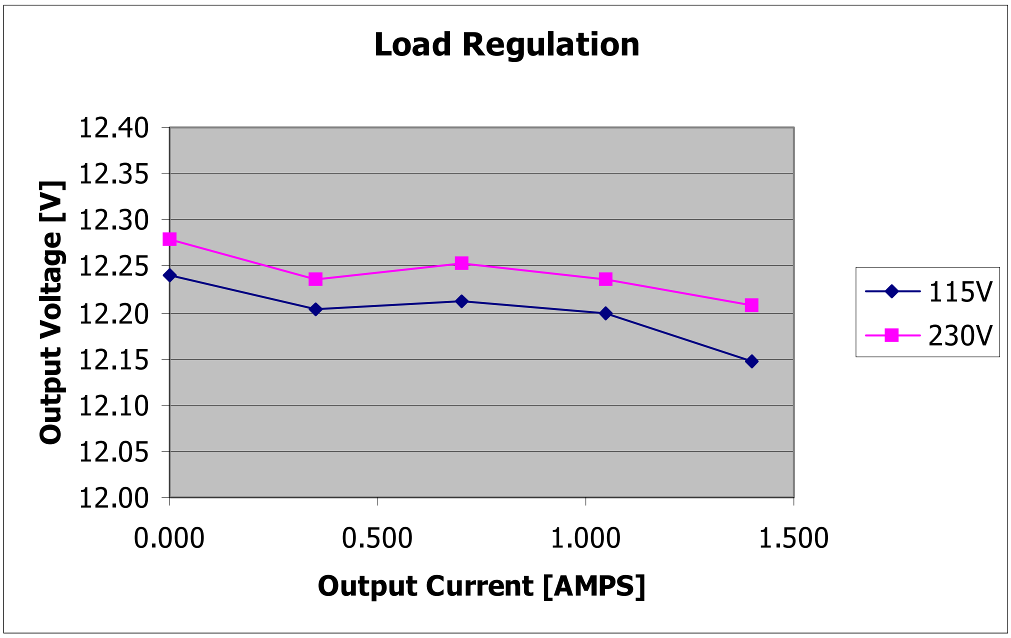

Figure 7 –Load Regulation, Room Temperature.

9.3.2 Line

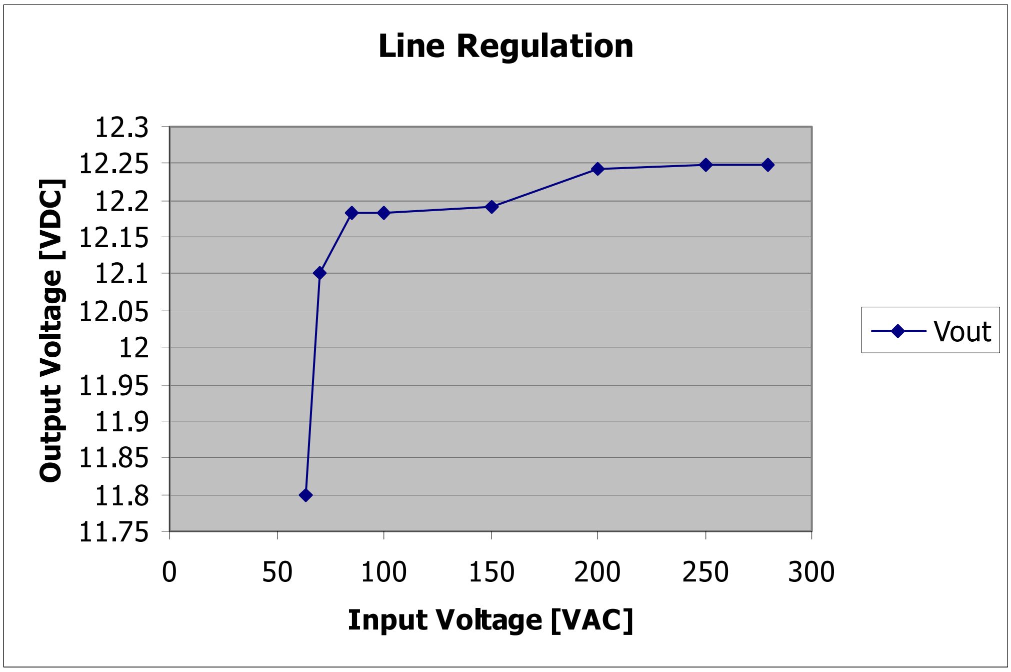

Figure 8 – Line Regulation, Room Temperature, Full Load.

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10 Thermal Performance

Item	Temperature (°C)		
	115VAC	230 VAC	
Ambient	24	24	
CM Choke L1	54	40	
Bridge BR1	68	47	
C2	55	47	
R1	61	57	
R2	88	75	
TNY279PN	87	65	
D1	82	69	
TX1	68	69	
D2	75	71	
C6	51	49	

Figure 9 – Temperature of major components when operated at full load

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11 Waveforms

11.1 Drain Voltage and Current, Normal Operation

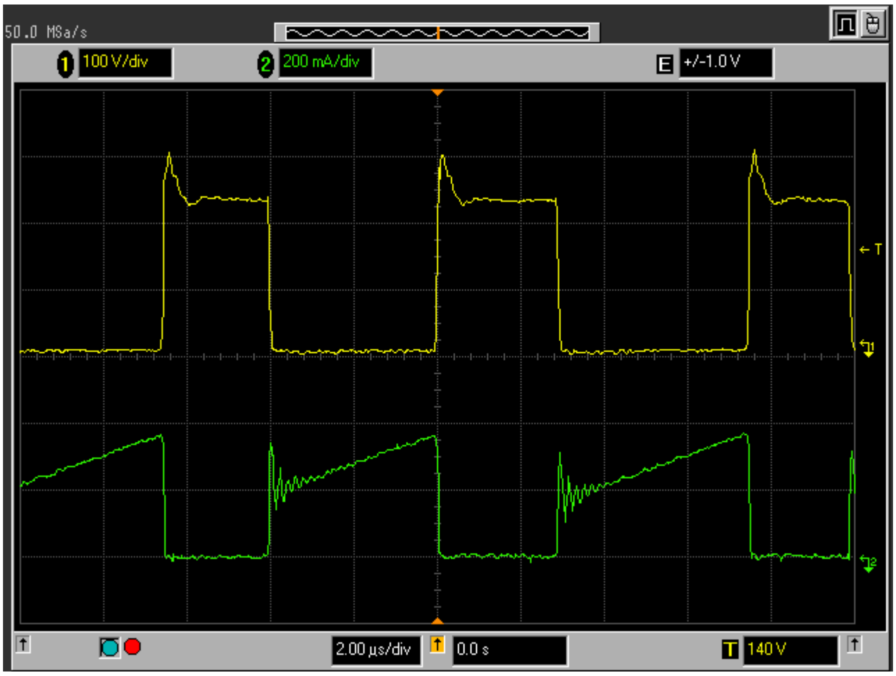

Figure 10 - 85 VAC, Full Load

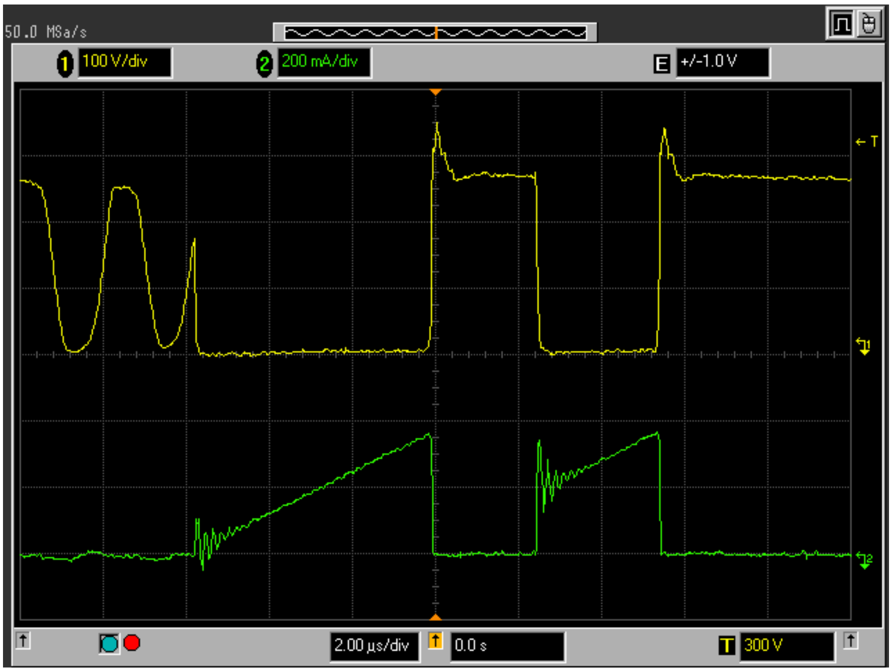

Figure 11 - 115 VAC, Full Load

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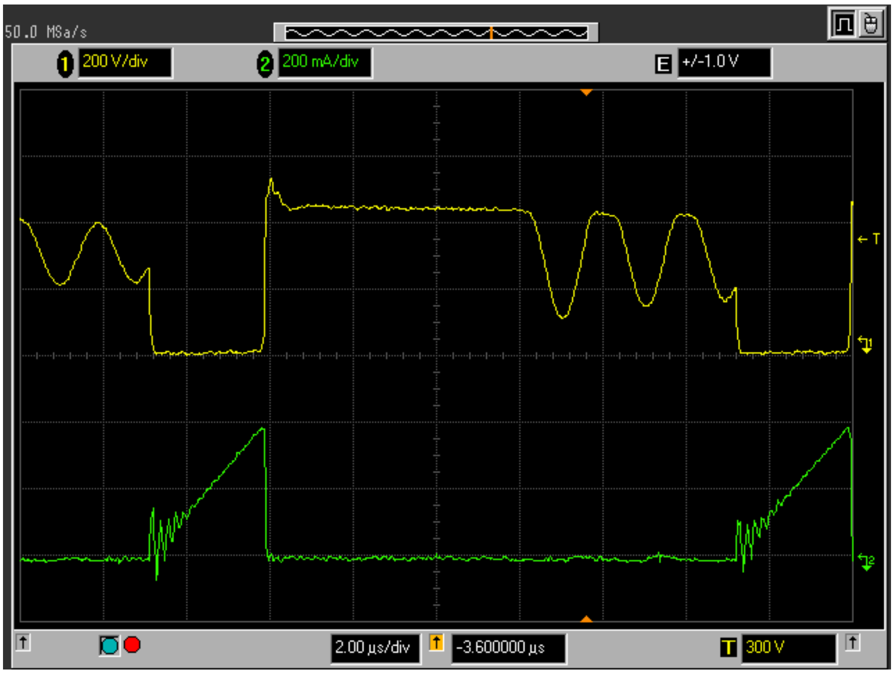

Figure 12 - 230 VAC, Full Load

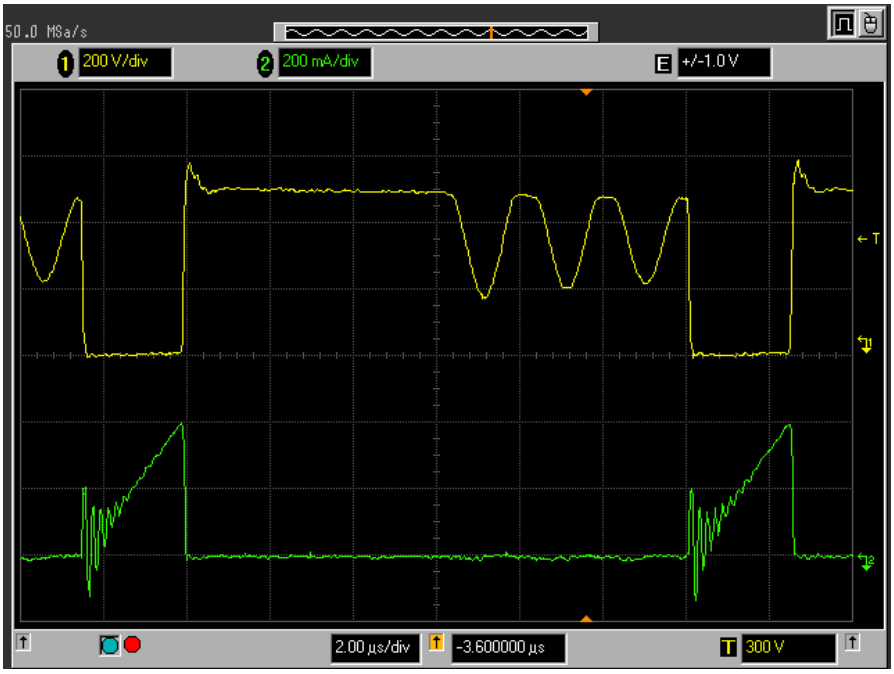

Figure 13 - 265 VAC, Full Load

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11.2 Output Voltage Start-up Profile

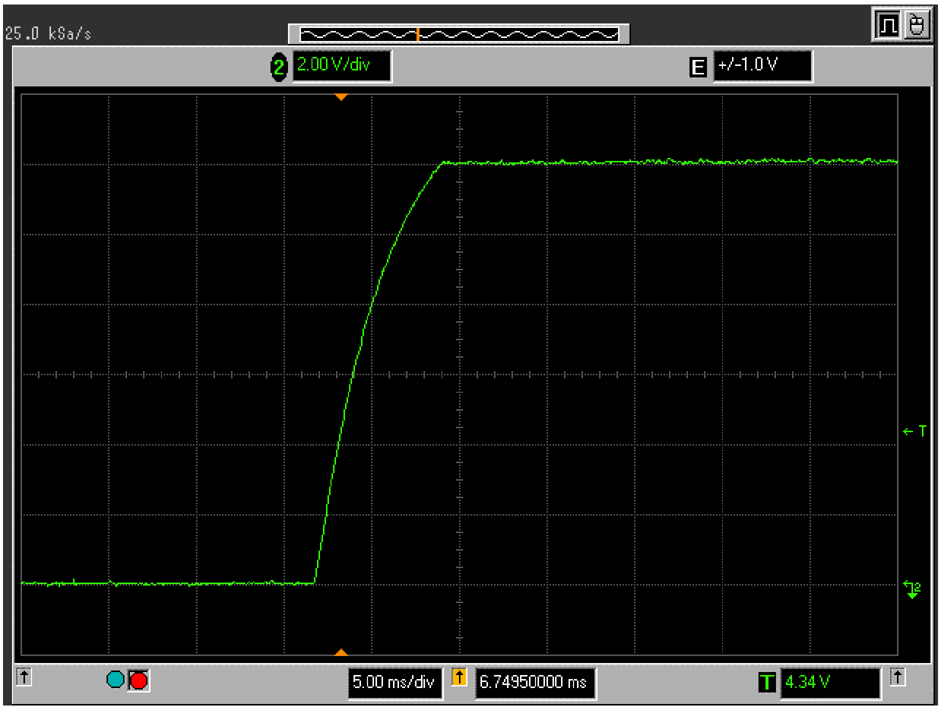

Figure 14 - Start-up Profile, 230 VAC 2 V/DIV, 5 ms / div.

11.3 Drain Voltage, Start-up Profile

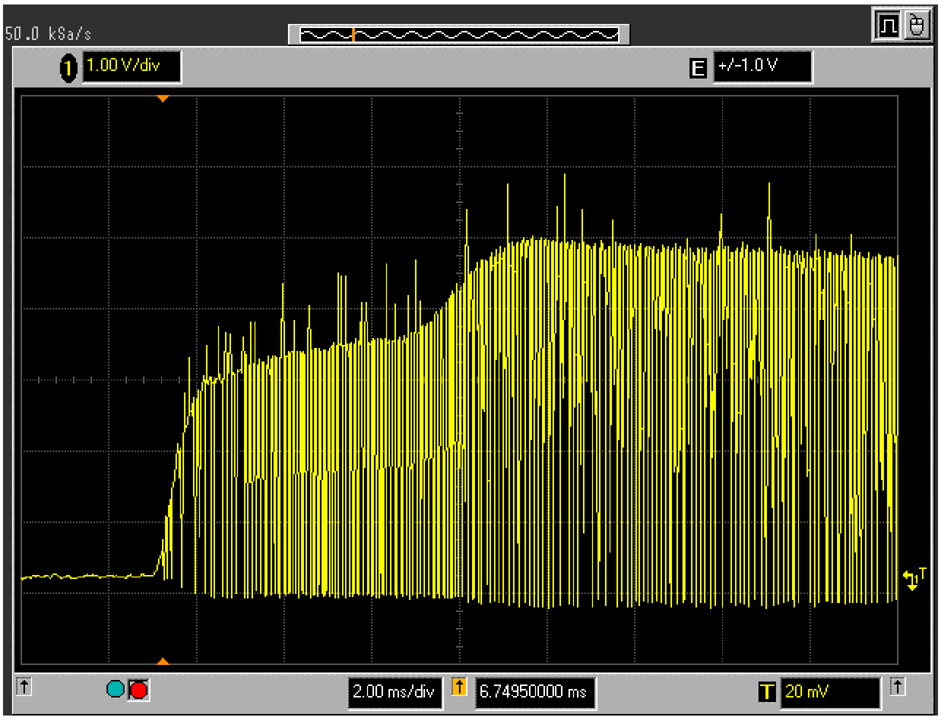

Figure 15 - 230 VAC Input and Maximum Load. 100 V , 2 ms / div.

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11.4 Output Ripple Measurements

11.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in Figure 16 and Figure 17.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 µF/50 V ceramic type and one (1) 1.0 µF/50 V aluminum electrolytic. ***The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).***

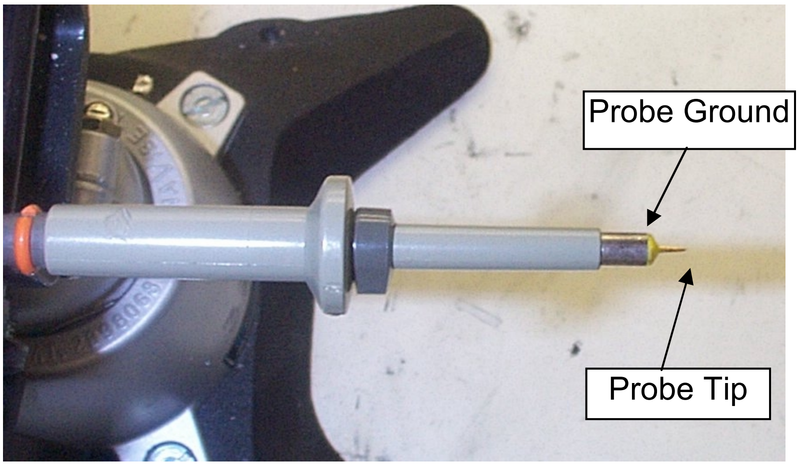

Figure 16 - Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

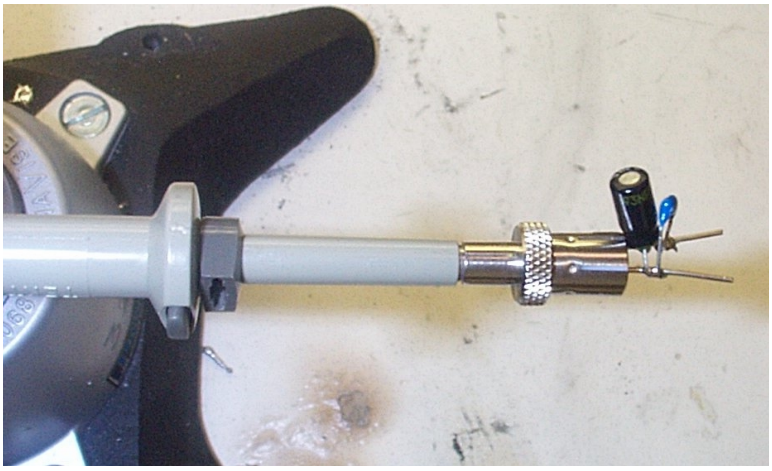

Figure 17 - Oscilloscope Probe with Probe Master 5125BA BNC Adapter. (Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added)

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11.4.2 Measurement Results

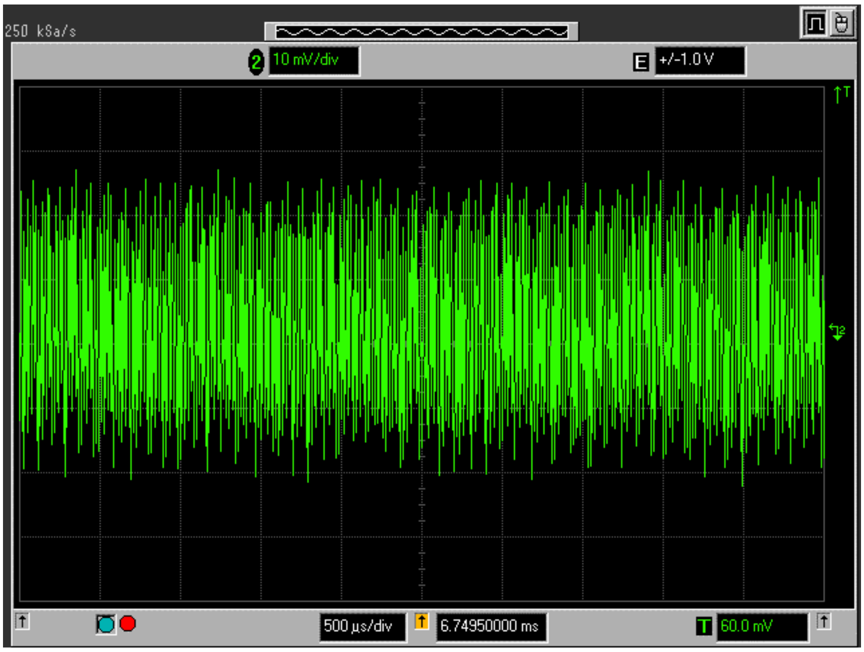

Figure 18 – Output Ripple, 230 VAC, Full Load. 500uS, 10 mV /div

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12 Conducted EMI

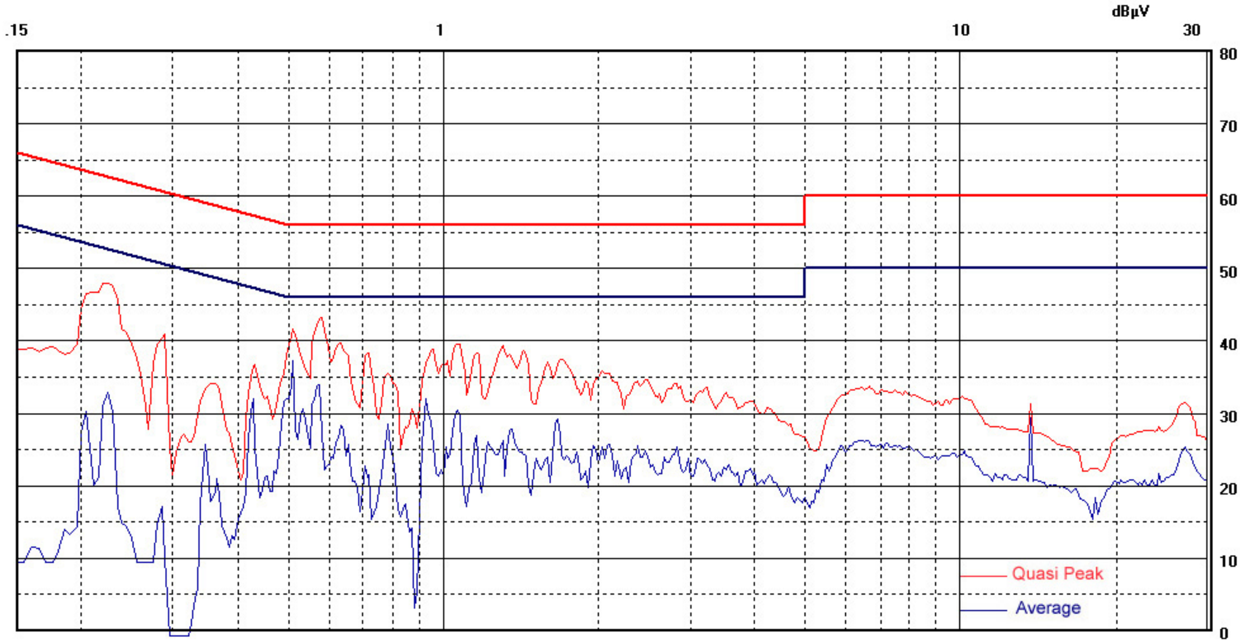

Figure 19 - Conducted EMI, Maximum Load, Live 230 VAC, 50 Hz, and EN55022 B Limits

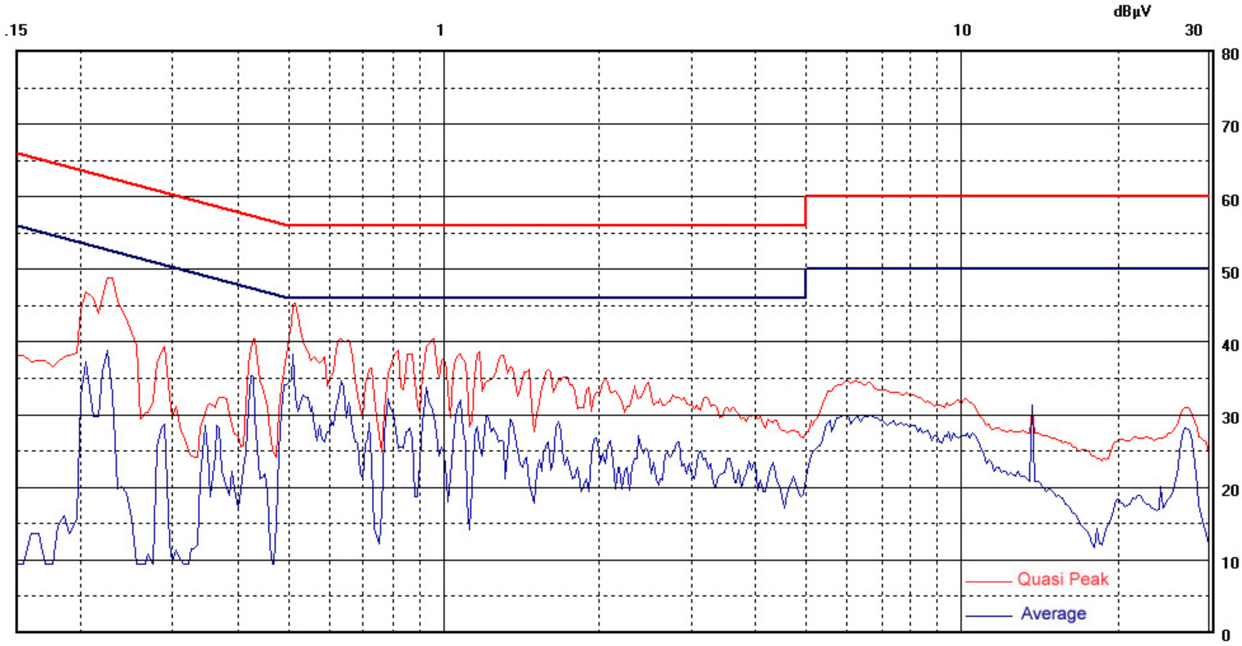

Figure 20 - Conducted EMI, Maximum Load, Neutral 230 VAC, 50 Hz, and EN55022 B Limits

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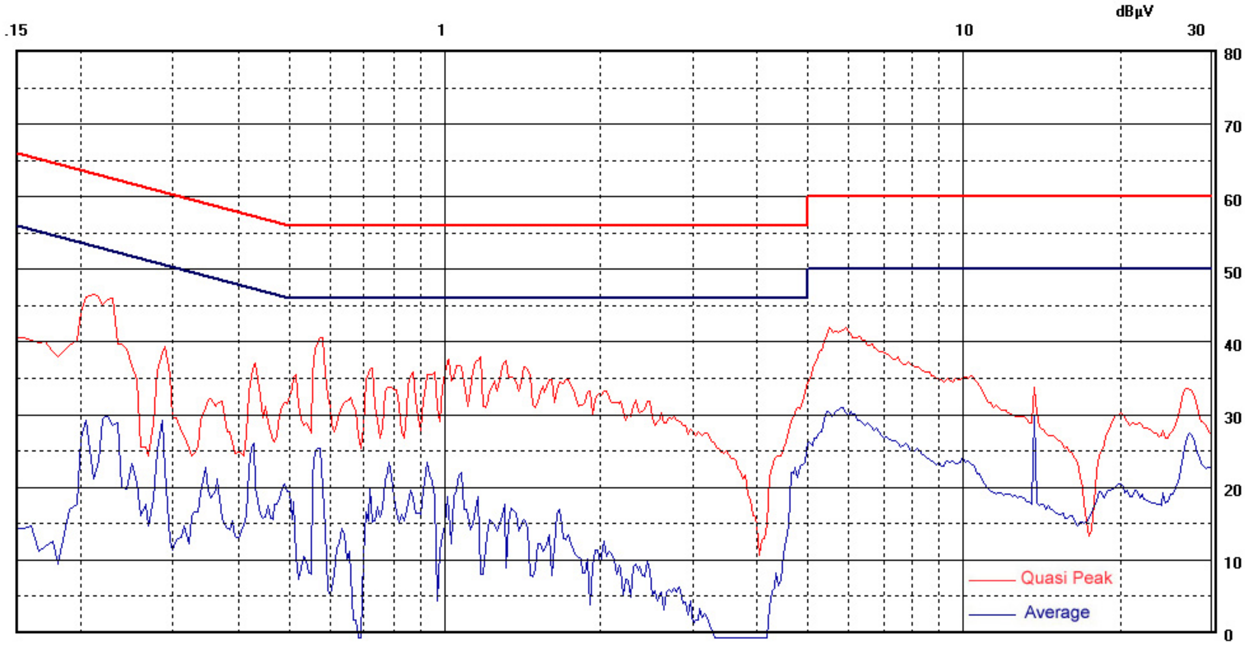

Figure 21 - Conducted EMI, Maximum Load, Live, Hand 230 VAC, 50 Hz, and EN55022 B Limits

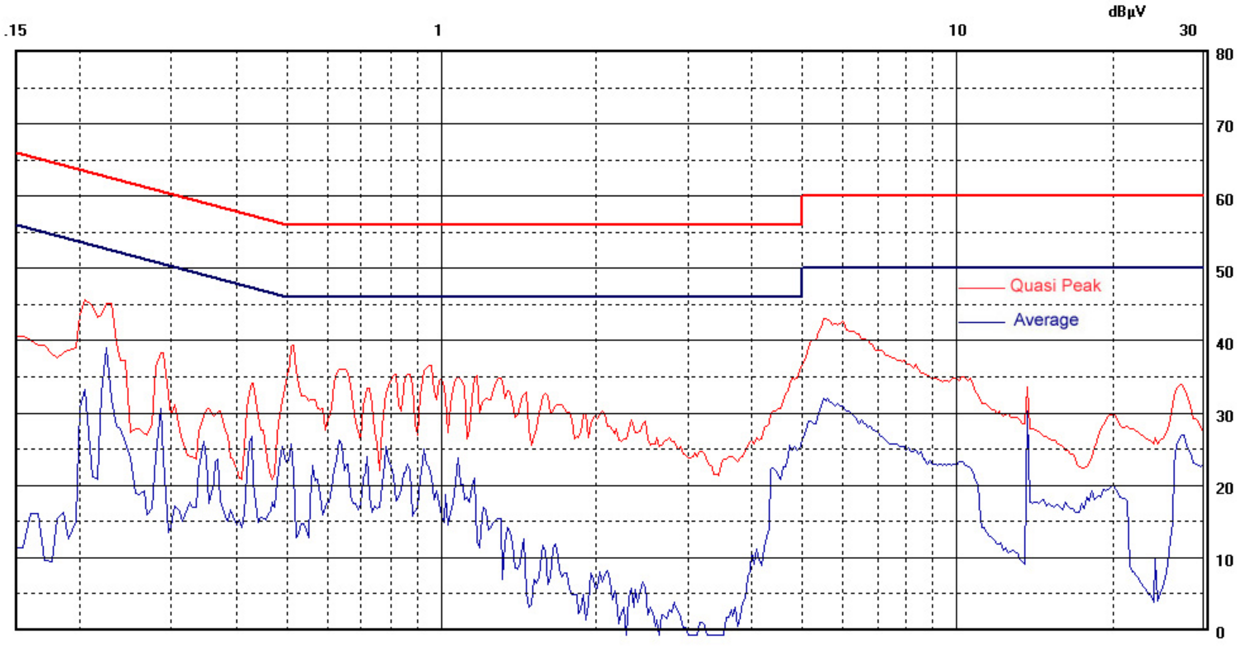

Figure 22 - Conducted EMI, Maximum Load, Neutral, Hand 230 VAC, 50 Hz, and EN55022 B Limits

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13 Revision History

Date	Author	Revision	Description & changes	Reviewed
12th Sept 06	DG	0.1	First Draft	PW
29th Sept 06	DG	0.2	First revision	FJ
13th Nov 06	DG	0.3	Second Revision	FJ

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