LinkSwitch®-XT Design Guide

Application Note AN-40

Introduction

The *LinkSwitch-XT* family is designed for low power adapters and chargers (cell/cordless phones, PDAs, digital cameras, portable audio etc), as well as auxiliary supplies employed in applications such as white goods. The ICs combine a high voltage power MOSFET switch with an ON/OFF controller in one device. It is completely self-powered from the DRAIN pin, has a jittered switching frequency for low EMI and is fully fault protected. Auto-restart limits device and circuit dissipation during overload, output short circuit and open loop conditions while hysteretic over-temperature protection disables the internal MOSFET during thermal faults. *EcoSmart®* technology enables designs to easily attain <150 mW no-load consumption. *LinkSwitch-XT* is ideal for linear charger replacement circuits because of its low cost and also because it can meet the efficiency standards set forth by the California Energy Commission (CEC). *LinkSwitch-XT* is designed to operate without the need for a primary-side clamp circuit (*Clampless*™) for output powers below 2 W (and up to 2.5 W with a bias winding) and thus dramatically reduces component count and total system cost. Figure 1 shows a *LinkSwitch-XT* based 2 W power supply without a primary-side clamp.

Scope

This application note is for engineers designing an isolated AC-DC flyback power supply using the *LinkSwitch-XT* family of devices. It provides guidelines to enable an engineer to quickly select key components and complete a transformer design for an application requiring either a constant voltage (CV) or constant voltage and constant current (CV/CC) output. To simplify the task of transformer design, this application note refers directly to the *PI Xls* design spreadsheet that is part of the *PI Expert* design software suite.

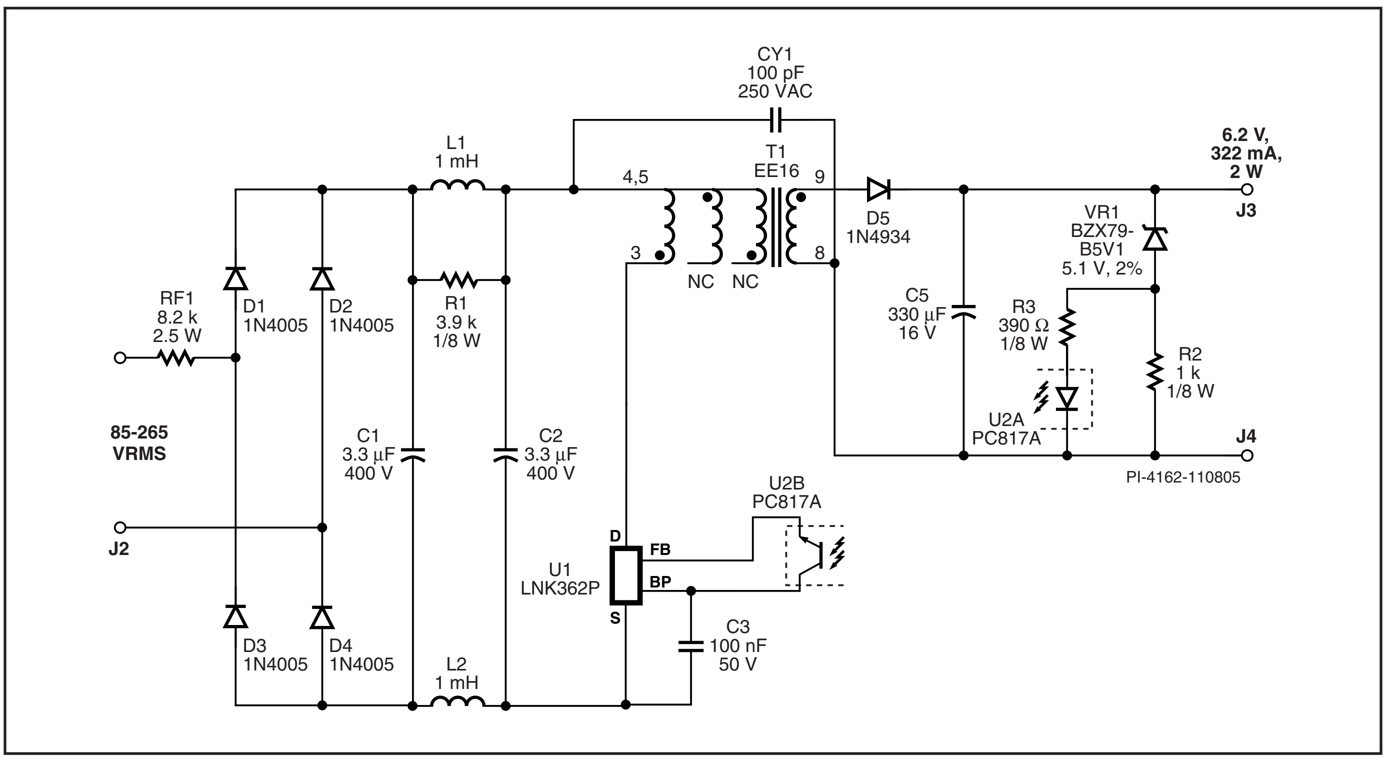


Figure 1. Basic Configuration Using LinkSwitch-XT in a Clampless Design.

Step-by-Step Design procedure

Step 1 – Enter Application Variables: VAC_{MIN}, VAC_{MAX}, f_L, V_O, I_O, CC Threshold Voltage, PO, Clamp and Feedback type, η, Z, t_C and C_{IN}.

Determine the input voltage range (VAC_{MIN} and VAC_{MAX}) from Table 1 below

Nominal Input Voltage	VAC_{MIN}	VAC_{MAX}
100/115	85	132
230	195	265
Universal	85	265

Table 1. Standard Worldwide Input Line Voltage Ranges.

Line frequency, f_L (Hz)
Enter the worst-case line frequency under which the supply should operate normally.

Output Voltage, V_O (V)
Enter the output voltage. For CV/CC designs this should be the typical output voltage at the nominal peak power point in the output characteristic. For CV only outputs, this should be the specified output voltage. For designs with an output cable, enter the voltages at the load. For multiple output designs, enter the voltage for the main output from which feedback is taken.

Output Current, I_O (A)
For CV/CC designs this should be the maximum output current at the maximum peak power point in the output characteristic (see Figure 2). For CV only outputs, this should be the maximum output current. In multiple output designs, the output current of the main output (typically the output from which feedback is taken) should be increased such that P_O matches the sum of the output power from all the outputs in the design. The individual output voltages and currents should then be entered at the bottom of the spreadsheet.

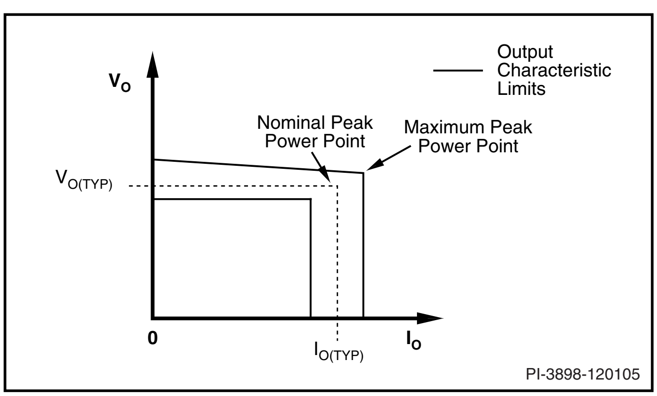


Figure 2. Diagram Showing Correct Values of I_O and V_O to Enter for CV/CC Designs.

CC Threshold Voltage (V)
For CV only designs, this is not applicable; enter 0. For CV/CC designs, this is the expected voltage developed across the current sense resistor at the nominal CC point. Typically, this value is in the range of 0.3 V to 1.3 V, depending on the specific circuit used. For designs using the V_{BE} of a bipolar transistor (~ 0.65 V) as the CC reference voltage, to maintain CC control, the optocoupler LED has to stay forward biased. This may require an additional resistor to be added in series with the CC sense resistor to increase the overall voltage drop (> ~1.1 V). It is this overall voltage drop that should be entered as the CC threshold. For the exact forward drop of the optocoupler LED, consult the manufacturer's data sheet.

Output Cable Resistance (Ω)
Enter the output cable resistance. If there is no output cable enter 0. This parameter is used as part of the total output power calculation.

Power Supply Efficiency (η)
This is the complete power supply efficiency measured at the point of load, therefore including any CC sense and cable losses. For a CV/CC design with a nominal peak power point at a voltage of 5.5 V and current of 0.5 A, use a value of 0.57. Use a value of 0.64 for a 5.5 V CV only design if no better data is available, or until measurements can be made on a prototype.

Power Supply Loss Allocation Factor, Z
This factor represents the proportion of losses between the primary and the secondary of the power supply.

$$Z = \frac{Secondary\ Side\ Losses}{Total\ Losses}$$

If no better data is available then the following values are recommended:

- Bias winding feedback designs (CV): 0.5 (0.35)
- Optocoupler CV feedback: 0.5 (0.35)
- Optocoupler CV and CC feedback: 0.75 (0.6)

For designs using *Filterfuse*™ use the values in parenthesis, these take into account the additional primary side losses due to a typical value of ~ 50 Ω for the resistance of the *Filterfuse* inductor

Bridge Diode conduction Time, t_C (ms)
Enter the bridge diode conduction time. Use 3 ms if no other data is available or until a measurement can be made on a prototype.

Total Input Capacitance, C_{IN} (μF)
Enter total input capacitance using Table 2 for guidance.

	Total Input Capacitance per Watt of Output Power (μF/W)	
AC Input Voltage (VAC)	**Half-Wave Rectification**	**Full-Wave Rectification**
100/115	5-8	3-4
230	1-2	1
85-265	5-8	3-4

Table 2. Suggested Total Input Capacitance for Different Input Voltage Ranges.

The capacitance should be selected to keep the minimum DC input voltage, V_{MIN} > 50 V and ideally > 70 V. Insufficient input capacitance may cause excessive line output ripple and reduce efficiency.

Note: For designs that have a DC rather than an AC input, the value of the minimum and maximum DC input voltages, V_{MIN} and V_{MAX}, may be entered directly into the gray override cells on the design spreadsheet (see Figure 3).

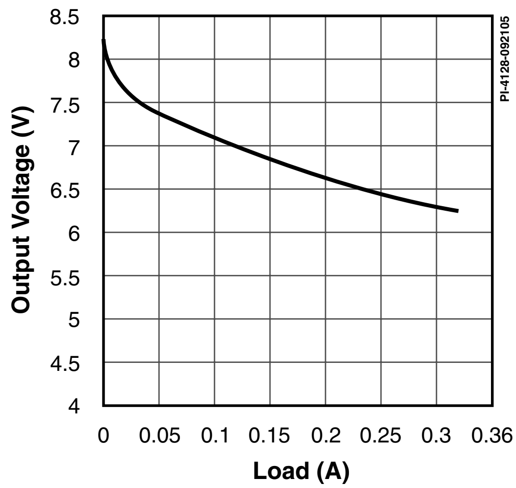
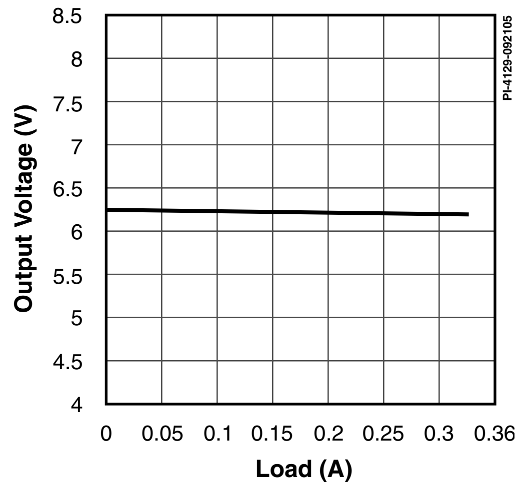
	Bias Winding Feedback	Optocoupler Feedback
Typical Output Characteristics		
Cost	Lower cost	Higher cost
Component count	Lower component count	Higher component count
CV/CC characteristic possible	No	Yes

Table 3. Summary of Comparison Between Bias Winding Feedback and Optocoupler Feedback.

ENTER APPLICATION VARIABLES					AN40 Example
VACMIN	85			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	6.00			Volts	Output Voltage (main) (For CC designs enter upper CV tolerance limit)
IO	0.33			Amps	Power Supply Output Current (For CC designs enter upper CC tolerance limit)
CC Threshold Voltage	0.00			Volts	Voltage drop across sense resistor.
Output Cable Voltage Resistance			0.17	Ohms	Enter the resistance of the output cable (if used)
PO			2.00	Watts	Output Power (VO x IO + CC dissipation)
Feedback Type	Opto		Opto		Enter 'BIAS' for Bias winding feedback and 'OPTO' for Optocoupler feedback
Add Bias Winding	No		No		Enter 'YES' to add a Bias winding. Enter 'NO' to continue design without a Bias winding. Addition of Bias winding can lower no load consumption
Clampless design (LNK 362 only)	Yes		Clampless		Clampless design selected. Verify peak Drain Voltage and EMI performance
n			0.64		Efficiency Estimate at output terminals.
Z	0.50		0.5		Loss Allocation Factor (suggest 0.5 for CC=0 V, 0.75 for CC=1 V)
tC	2.90			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	9.40			uFarads	Input Capacitance
Input Rectification Type	F		F		Choose H for Half Wave Rectifier and F for Full Wave Rectification

DC INPUT VOLTAGE PARAMETERS					
VMIN			99	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage

Figure 3. Application Variable Section of LinkSwitch-XT Design Spreadsheet.

Enter Feedback, Bias type and Clamp information
Select between either bias winding feedback (primary-side feedback), Figure 9, or optocoupler feedback (secondary-side feedback), Figure 10. Bias winding makes use of a primary-side auxiliary winding to set the output voltage. Optocoupler feedback directly senses the output voltage and can provide any level of accuracy depending on the voltage reference selected. Secondary-side feedback also allows for a CV/CC output characteristic. See Table 3 for a summary of feedback types.

Figure 1 shows a CV only optocoupler design, Table 9 provides guidance for component selection for both CV and CV/CC configurations. Figure 9 shows a CV only bias winding configuration.

If optocoupler feedback is selected, the user still has the option to use a bias winding. It may be used to externally power the *LinkSwitch-XT* device for lower no-load consumption. In addition, the bias winding can be configured as a shield for reduced EMI.

Designs below 2.5 W output power may be able to eliminate the primary-side clamp circuit. *Clampless* circuits offer the benefit of low cost and component count, but these circuits rely on specific transformer construction techniques. See the section on transformer construction for details.

For designs greater than 2.5 W, a *Clampless* solution is not recommended. See the section on clamp design for details.

All the variables described above can be entered in the “Enter Application variables” section of the *LinkSwitch-XT* design spreadsheet in *PI Xls* design software (see Figure 3).

Step 2 –Enter ***LinkSwitch-XT***, V_{OR}, V_{DS}, V_D

To select the correct *LinkSwitch-XT* device, refer to the *LinkSwitch-XT* data sheet power table and select based on the input voltage, enclosure type and output power of the design.

Reflected Output Voltage, V_{OR} (V)
This parameter is the secondary winding voltage reflected back to the primary through the turns ratio of the transformer (during the conduction time of the output diode). The default value is 80 V, however this can be increased up to 120 V to achieve the maximum power capability from the selected *LinkSwitch-XT* device. In general, start with the default value of 80 V, increasing the value when necessary to maintain K_P above its lower limit of 0.6. For *Clampless* designs, there is less flexibility in selecting the value of V_{OR}. Increasing V_{OR} directly increases the peak Drain voltage. Therefore, for *Clampless* designs, a value of 80 V should be used and only increased once the peak Drain voltage has been measured and adequate margin to BV_{DSS} determined.

***LinkSwitch-XT* On-State DRAIN to SOURCE Voltage, V_{DS} (V)**
This parameter is the average on-state voltage developed across the DRAIN and SOURCE pins of *LinkSwitch-XT*. By default, if the gray override cell is left empty, a value of 10 V is assumed. Use the default value if no better data is available.

Output Diode Forward Voltage Drop, V_D (V)
Enter the average forward voltage drop of the (main) output diode. Use 0.5 V for a Schottky diode or 1 V for a PN diode if no better data is available. By default, a value of 0.5 V is assumed.

Calculated Ripple to Peak Current Ratio, K_P
Below a value of 1, indicating continuous conduction mode, K_P is the ratio of ripple to peak primary current (K_{RP}). Above a value of 1, indicating discontinuous conduction mode, K_P is the ratio of primary MOSFET off-time to the secondary diode conduction time (K_{DP}). The value of K_P should be in the range of $0.6 < K_P < 6$ and guidance is given in the comments cell if the value is outside this range. A value above 1 will typically result in lower noise, discontinuous conduction mode at 115 VAC, where EMI measurements are made.

Variables referenced in Step 2 are found in the “Enter *LinkSwitch-XT* Variables” section of the spreadsheet (see Figure 4).

Step 3 – Choose Core and Bobbin Based on Output Power and Enter A_e, L_e, A_L, BW, M, L, N_S

Core Effective Cross-Sectional Area, A_e (cm^2)
Core Effective Path Length, L_e (cm), Core Ungapped Effective Inductance, A_L (nH/turn^2), Bobbin Width, BW (mm)

ENTER LinkSwitch-XT VARIABLES					
LinkSwitch-XT	LNK362		LNK362		User selection for LinkSwitch-XT
Chosen Device		*LNK362*			
ILIMITMIN			*0.130*	Amps	Minimum Current Limit
ILIMITMAX			*0.150*	Amps	Maximum Current Limit
fSmin			*124000*	Hertz	Minimum Device Switching Frequency
I^2fmin			2199	A^2Hz	I^2f (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR			80	Volts	VOR > 90V not recommended for Clampless designs with no Bias windings. Reduce VOR below 90V
VDS			10	Volts	LinkSwitch-XT on-state Drain to Source Voltage
VD			0.5	Volts	Output Winding Diode Forward Voltage Drop
KP			1.03		Ripple to Peak Current Ratio (0.6 < KP < 6.0)

Figure 4. LinkSwitch-XT Variables Section of LinkSwitch-XT Design Spreadsheet.

By default, if the Core Type cell is left empty, the spreadsheet will select the EE16 core. The user can change this selection and choose an alternate core from a list of commonly available cores suitable for the output power (shown in Table 4). The values shown are based on an assumed output voltage of 6 V, 4 primary winding layers and the default input parameters as described in Step 1. Changes to these values will change the power capability of a given core size, therefore Table 4 should be used for guidance only.

Core Size	Commonly Used	Suggested Power Range	
		100/115 or 85-265 VAC	230 VAC Only
EE8	No	< 1 W	< 1 W
EP10	No	< 1.75 W	< 1.75 W
EE10	No	< 2 W	< 2 W
EF12.6	Yes	< 3.3 W	< 3.3 W
EE13	Yes	< 4 W	< 4 W
EE16	Yes	< 5 W	< 6 W
EE1616	Yes	< 5.5 W	< 7 W
EE19	Yes	< 5.6 W	< 7.1 W
EF20	Yes	< 6 W	< 8 W
EF25	Yes	< 6 W	< 9 W

Table 4. Maximum Power Capability of Cores Used in Flyback Topology

be entered into the spreadsheet. For vertical bobbins, the margin may not be symmetrical however, the total margin divided by 2 should still be entered.

As the margin reduces the available area for the windings, margin construction may not be suitable for small core sizes. If after entering the margin, more than 4 primary layers (L) are required, it is suggested that either a larger core be selected or switch to a zero margin design using triple insulated wire for the secondary winding.

Primary Layers, L

By default, if the override cell is empty, a value of 2 is assumed. Primary layers should be in the range of $1 < L < 4$, and in general it should be the lowest number that meets the primary current density limit (CMA) of 150 Cmils/Amp. Values above 4 layers are possible, but the increased leakage inductance and physical fit of the windings should be considered.

For *Clampless* designs without a bias winding, 2 primary layers must be used. This is to ensure sufficient primary capacitance to limit the peak Drain voltage below the BV_{DSS} rating of the internal MOSFET.

Secondary Turns, N_S

By default, if the grey override cell is left blank, the minimum number of secondary turns is calculated such that the maximum operating flux density, B_M, is kept below the recommended maximum. In general, it is not necessary to enter a number in

ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type			EE16		Suggested smallest commonly available core
Core		*EE16*		*P/N:*	PC40EE16-Z
Bobbin		*EE16_BOBBIN*		*P/N:*	EE16_BOBBIN
AE			0.192	cm^2	Core Effective Cross Sectional Area
LE			3.5	cm	Core Effective Path Length
AL			1140	nH/T^2	Ungapped Core Effective Inductance
BW			8.6	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			2		L > 2 or L < 1 not recommended for Clampless designs with no Bias windings. Enter L = 2
NS			11		Number of Secondary Turns
NB			N/A		Bias winding not used
VB			N/A	Volts	Bias winding not used
PIVB			N/A	Volts	N/A - Bias Winding not in use

Figure 5. Transformer Core and Construction Variables Section of Spreadsheet.

The gray override cells can be used to enter the core and bobbin parameters directly. This is useful if a core is selected that is not on the list or the specific core or bobbin information differs from that recalled by the spreadsheet.

Safety Margin, M (mm)

For designs that require isolation but are not using triple insulated wire for the secondary winding, the width of the safety margin to be used on each side of the bobbin should be entered here. Typically, for universal input designs, a total margin of 6.2 mm would be required; therefore a value of 3.1 mm would

the override cell except in designs where a higher operating flux density is acceptable (see Minimizing Audible Nose section for an explanation of B_M limits).

Calculated Bias Winding Turns and Voltage N_B, V_B

Where a bias winding is used, the number of turns and voltage developed are displayed. The relatively large default number of turns allows the bias to be used as a shield winding for reduced EMI. If desired, the number of turns can be adjusted by entering a value into the gray override cell.

The variables described in step 3 are found in the "Enter Transformer Core/Construction Variables" section of the spreadsheet (see Figure 5).

Step 4 – Iterate Transformer Design and Generate Transformer Design Output

Iterate the design making sure that no warnings are displayed. Any parameters outside the recommended range of values can be corrected by following the guidance given in the right hand column.

Once all warnings have been cleared, the output transformer design parameters can be used to either wind a prototype transformer or send to a vendor for samples.

The key transformer electrical parameters are:

Primary Inductance, L_P (μH)
This is the target nominal primary inductance of the transformer.

Primary Inductance Tolerance, $L_{P\_TOLERANCE}$ (%)
This is the assumed primary inductance tolerance. A value of ±10% is used by default, however if specific information is known from the transformer vendor, then this may be overridden by entering a new value in the gray override cell.

Maximum operating flux density, B_M (Gauss)
The cycle skipping mode of operation used in *LinkSwitch-XT* can generate audio frequency components in the transformer. To limit this audible noise generation the transformer should be designed such that the peak core flux density is below 1500 Gauss (150 mT). Following this guideline, and using the standard transformer production technique of dip varnishing, practically eliminates audible noise. Vacuum impregnation of the transformer should not be used due to the high primary capacitance and increased losses that result. Higher flux densities are possible, however careful evaluation of the audible noise performance should be made using production transformer samples before approving the design. Audible noise may also be created by ceramic capacitors that use dielectrics such as Z5U, when used in clamp circuits may also generate audio noise. If this is the case, try replacing them with a capacitor having a different dielectric, for example a film type. Flux densities above 3000 Gauss (300 mT) are not recommended.

Other transformer parameters calculated in the spreadsheet are:

N_P - Primary Winding Number of Turns
A_{LG} (nH/T^2) - Gapped Core Effective Inductance
B_{AC} (Gauss) - AC Flux Density for Core Loss Curves (0.5 x Peak to Peak)
ur - Relative Permeability of Ungapped Core
L_G (mm) - Gap Length (L_G > 0.1 mm).
B_{WE} (mm) - Effective Bobbin Width (Accounts for Margin tape if used)
O_D (mm) - Maximum Primary Wire Diameter including insulation
INS (mm) - Estimated Total Insulation Thickness (= 2 * film thickness)
DIA (mm) - Bare conductor diameter
AWG - Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM (Cmils) - Bare conductor effective area in circular mils
CMA (Cmils/Amp) - Primary Winding Current Capacity (150 < CMA < 500)

Variables described in step 4 can be found under the "Transformer Primary Design Parameters" section of the spreadsheet (see Figure 6).

Step 5 – Selection of Input Stage

The input stage comprises a fusible element(s), input rectification and line filter network. The fusible element can be either a fusible resistor, fuse or make use of Power Integration's *Filterfuse* technique. Here, the input inductor may also used as a fuse, typically requiring the addition of a heatshrink shroud to prevent incandescent material being ejected during a fault. By using *Filterfuse*, the input stage can be simplified in saving the cost of a fusible resistor, but requiring a larger single input capacitor. However, please verify with a safety engineer or

TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			2563	uHenries	Typical Primary Inductance. +/- 10%
LP_TOLERANCE			10	%	Primary inductance tolerance
NP			135		Primary Winding Number of Turns
ALG			140	nH/T^2	Gapped Core Effective Inductance
BM			1479	Gauss	Maximum Operating Flux Density, BM<1500 is recommended
BAC			624	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1654		Relative Permeability of Ungapped Core
LG			0.15	mm	Gap Length (Lg > 0.1 mm)
BWE			17.2	mm	Effective Bobbin Width
OD			0.13	mm	Maximum Primary Wire Diameter including insulation
INS			0.03	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.10	mm	Bare conductor diameter
AWG			39	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			13	Cmils	Bare conductor effective area in circular mils
CMA			242	Cmils/Amp	Primary Winding Current Capacity (150 < CMA < 500)

Figure 6. Transformer Primary Design Parameters Section of Design Spreadsheet.

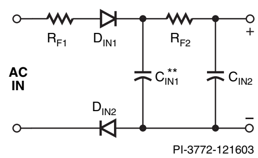
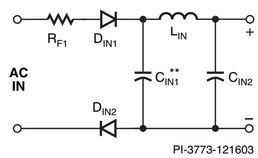
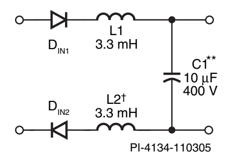
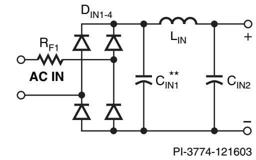
P_{OUT}	≤ 1 W	≤ 3 W		
Suggested 85-265 VAC Input Stage				
Component Selection Guide	R_{F1}: 8.2 Ω, 1 W Fusible R_{F2}: 100 Ω, 0.5 W, Flameproof C_{IN1}, C_{IN2}: ≥ 3.3 µF, 400 V each D_{IN1}, D_{IN2}: 1N4007, 1 A, 1000 V	R_{F1}: 8.2 W, 1 W Fusible L_{IN}: 470 µH-2.2 mH, (0.05 A-0.3 A) C_{IN1}, C_{IN2}: ≥4 µF/ W_{OUT}, 400 V each D_{IN1}, D_{IN2}: 1N4007, 1 A, 1000 V	L1, L2*: 3.3 µH, 0.06 A Filterfuse® C1: ≥ 5 µF/ W_{OUT}, 400 V D_{IN1}: 1N4937, 600 V D_{IN2}: 1N4007, 1000 V	R_{F1}: 8.2 W, 1 W Fusible L_{IN}: 470 µH-2.2 mH, (0.05 A-0.3 A) C_{IN1}, C_{IN2}: ≥ 2 µF/ W_{OUT}, 400 V each D_{IN1}-D_{IN4}: 1N4007, 1 A, 1000 V
Comments	**Increase value to meet required differ-ential line	**Increase value to meet required differ-ential line	*Check for safety agencies approval **Increase value to meet required differ-ential line surge performance †Second inductor may be required in *Clampless* designs	**Increase value to meet required differ-ential line surge

Table 5. Input Filter Recommendation Based on Total Output Power.

agency if *Filterfuse* is acceptable. *Clampless* designs ≥ 2 W without a bias winding may require an additional inductor for acceptable conducted EMI.

If a fusible resistor is selected, it should be a flameproof type and, depending on the differential line input surge requirements, a wire-wound type may be required. Care should be taken in using metal or carbon film types as these can fail simply due to the inrush current when AC is connected to the supply.

Designs using a Y-capacitor require the EMI filter impedance to be placed on the appropriate side of the input. Therefore when Y capacitor is returned to the DC rail, the fusible resistor(s)/ *Filterfuse* should be placed in the opposite side of the input.

For designs < 1 W, it is generally lower cost to use half-wave rectification; and ≥ 1 W, full-wave rectification. However if *Filterfuse* is used, even above 1 W, half wave rectification may lower cost and should be selected accordingly.

	Clampless		**External Clamp**
	≤2 W	2 W < P_O ≤ 2.5 W	
Bias winding required	N	Y	N
Device	LNK362 only		Any
Primary layers	= 2 (no bias winding) ≤4 (with bias winding)	≤4	≤4
V_{OR} (V)	≤90	≤130	≤130
Recommended Transformer Parameters	Leakage inductance <90 µH Primary capacitance ≥50 pF	No restriction	
Leakage ring effect on EMI	High	Medium	Low

Table 6. Factors to be Considered While Deciding Between a Clampless or External Clamp Design.

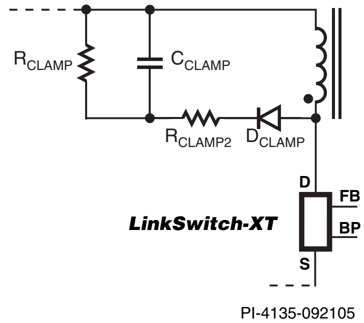
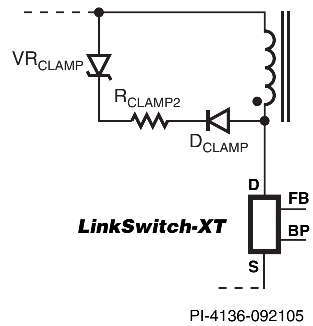
Type	RCD	Zener
Suggested Primary Clamp		
Advantages	• Lower cost • Lower EMI	• Lower parts count • Lower no-load consumption
Component Selection Guide	• D_{CLAMP} (1 A, 600 V) - UF4005, 1N3947 or 1N4007GP - 1N4007 improves EMI and efficiency but must be glass passivate type (1N4007GP) • R_{CLAMP2} - Not necessary when using ultra-fast (UF4005) or fast diode (1N4937) - A value in the range of 50 Ω to 330 Ω, 1/4 W should be used with a slow diode (1N4007GP) to limit reverse pull out current	
	• R_{CLAMP} - 47 kΩ to 200 kΩ, 1/4 W or 1/2 W • C_{CLAMP} - 390 pF to 2.2 nF, ≥ 400 V ceramic or film (Note ceramic capacitors may create audible noise)	• VR_{CLAMP} - Select voltage to be 1.5 • V_{OR} with a power rating of 0.5 W to 1 W (P6KExxx and BZY97Cxxx series are good examples of suitable Zener diodes)

Table 7. Primary Clamp Recommendation (for Output Power > 2.5 W).

The EMI performance of half-wave rectified designs is improved by adding a second diode in the lower return rail. This provides EMI gating (EMI currents only flow when the diode is conducting) and also doubles the differential surge-withstand as the surge voltage is shared across two diodes. In designs using a single input capacitor at least one of the input diodes should be a fast type (t_{rr} ≤ 200 ns). This reduces ringing and associated increase in EMI. Table 5 shows the recommended input stage based on output power for a universal input design while Table 2 shows how to adjust the input capacitance for other input voltage ranges.

Step 6 – Selection of *LinkSwitch-XT* External Components

LinkSwitch-XT requires a 0.1 μF / 50 V capacitor across the BYPASS and SOURCE pins.

Step 7 – Selection of Primary Clamp Circuit

For output powers of 2.5 W or below and using the LNK362, it is possible to eliminate external clamp components by careful design of the transformer and bias winding. For *Clampless* designs, a 2-layer primary should be used. The resultant increase in the intra-winding capacitance limits the peak drain voltage at turn off. For output powers greater than 2 W, the winding capacitance is not sufficient to limit peak drain voltage. Therefore a bias winding should be added to the transformer and rectified with a standard recovery (rectifier) diode. Suitable diodes for the bias winding include 1N4003–1N4007. The addition of a bias winding acts as a clamp and also reduces leakage inductance ringing and improves EMI. Table 6 summarizes the requirements between *Clampless* designs and designs using an external clamp.

Clampless designs should only be attempted with the LNK362 device. The higher current limit of the larger family members make it impractical to limit the peak drain voltage without an external clamp.

For output powers > 2.5 W, either an RCD or Zener clamp is suggested. Select the initial clamp components using Table

Series Number	Type	VR Range	I_F	Package	Manufacturer
		V	A		
1N5817 to 1N5819	Schottky	20-40	1	Leaded	Vishay
SB120 to SB1100	Schottky	20-100	1	Leaded	Vishay
11DQ50 to 11DQ60	Schottky	50-60	1	Leaded	IR
1N5820 to 1N5822	Schottky	20-40	3	Leaded	Vishay
MBR320 to MBR360	Schottky	20-60	3	Leaded	IR/On Semi
SS12 to SS16	Schottky	20-60	1	SMD	Vishay
SS32 to SS36	Schottky	20-60	3	SMD	Vishay
UF4002 to UF4006	Ultrafast	100-600	1	Leaded	Vishay
MUR110 to MUR160	Ultrafast	100-600	1	Leaded	On Semi
UF5401 to UF5408	Ultrafast	100-800	3	Leaded	Vishay
ES1A to ES1D	Ultrafast	50-200	1	SMD	Vishay
ES2A to ES2D	Ultrafast	50-200	2	SMD	Vishay

Table 8. List of Recommended Diodes That May Be Used With LinkSwitch-XT Designs.

TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			6.00	Volts	Main Output Voltage (if unused, defaults to single output design)
IO1			0.33	Amps	Output DC Current
PO1			2.00	Watts	Output Power
VD1			0.50	Volts	Output Diode Forward Voltage Drop
NS1			11.00		Output Winding Number of Turns
ISRMS1			0.68	Amps	Output Winding RMS Current
IRIPPLE1			0.60	Amps	Output Capacitor RMS Ripple Current
PIVS1			36.45	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diodes			UF4001, SB150		Recommended Diodes for this output
Pre-Load Resistor			2	k-Ohms	Recommended value of pre-load resistor
CMS1			136.99	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			28.00	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.32	mm	Minimum Bare Conductor Diameter
ODS1			0.78	mm	Maximum Outside Diameter for Triple Insulated Wire

Figure 7. Secondary Design Parameters. Includes a Recommended Diode Part.

as guide. If an RCD clamp is selected, then some empirical adjustment of the values is normally required to take account of the actual V_{OR} and transformer leakage inductance of the design. As a general rule, minimize the value of the capacitor and maximize the value of the resistor. For both RCD and Zener clamps, verify that the peak drain voltage does not exceed 650 V at the highest input voltage and peak (overload) output power.

Step 8 – Selection of Output Diode and Pre-Load Resistor

$V_R \geq 1.25 \bullet \text{PIVS}$, where PIVS is taken from the Voltage Stress Parameters section of the spreadsheet and Transformer Secondary Design Parameters.

$I_D \geq 2 \bullet I_O$, where I_D the diode rated DC current and I_O is the output current.

Additionally, Table 8 lists some of the suitable Schottky and ultra-fast diodes that may be use with *LinkSwitch-XT* circuits. The *LinkSwitch-XT* spreadsheet also recommends a diode based on the above guidelines (see Figure 7).

Select the pre-load resistor such that it will sink 3 mA at the specified voltage. Note that a pre-load resistor also increases the no-load losses, so verify acceptable no-load consumption.

Step 9 – Selection of Output Capacitors

Ripple Current Rating

Select the output capacitor(s) such that the ripple rating is greater than the calculated value, I_{RIPPLE} from the spreadsheet.

Many capacitor manufacturers provide factors that increased the allowable ripple current as the capacitor temperature is reduced or the frequency of the ripple is increased from the

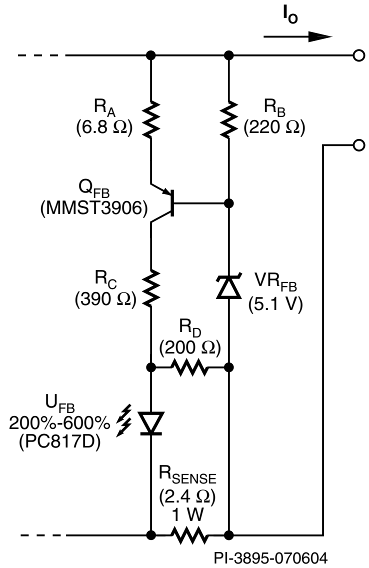
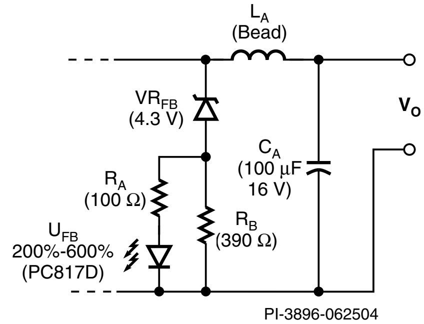
<table>
<tr><th>Output Type</th><th>CV/CC</th><th>CV Only</th></tr>
<tr><td>Suggested Feedback</td><td>
</td><td>
</td></tr>
<tr><td>Notes</td><td>R_{SENSE}: $V_{F(UFB)}/I_O$
VR_{FB}: V_O-$V_{BE(QFB)}$ (Use a Zener with a low I_{ZT} such as the BZX79 series)
R_B: $V_{BE(QFB)}/I_{ZT(VRFB)}$
R_A: Limits base-emitter current of Q_{FB}
R_C and R_D: Limits U_{FB} current
U_{FB}: Use high CTR device (200% - 600%)
Q_{FB}: Any small signal PNP transistor (Values shown for a 5.5 V, 500 mA output)</td><td>VR_{FB}: V_O-$V_{F(UFB)}$ (Use a Zener with a low I_{ZT} such as the BZX79 series)
R_B: $V_{F(UFB)}/I_{ZT(VRFB)}$
R_A: Limits U_{FB} current during transients and allows small output voltage adjustments.
U_{FB}: Use high CTR device (200% - 600%)
L_A: Optional for lower output switching noise (Use ferrite bead or low value (1-3 µH) inductor rated for I_O)
C_A: Optional for lower output switching noise (Use low ESR, 100 µF with voltage rating >1.25 • V_O)
(Values shown are for a 5 V output)</td></tr>
</table>

Table 9. Examples of Feedback Configurations.

data sheet specified values. This should be considered to ensure the capacitor is not oversized, increasing the cost. Two or more capacitors may be used in parallel to given a combined ripple current rating equal to the sum of the individual capacitor ratings.

ESR specification

Select a low ESR type, which gives acceptable output switching ripple. The switching ripple voltage is equal to the peak secondary current multiplied by the ESR of the output capacitor. Generally the selection the capacitor for ripple current rating will also result in an acceptable ESR

Voltage Rating

Select a voltage rating such that $V_{RATED} \geq 1.25 \bullet V_O$.

Step 10 – Choose Feedback Scheme and Select Feedback Components

Two separate feedback schemes are recommended with the *LinkSwitch-XT*. The first is primary-side regulated feedback (also called bias winding feedback), shown in Figure 9. This scheme relies on the bias winding to regulate the output voltage. The bias winding voltage is divided down by a resistor divider such that the feedback pin is 1.65 V at the specified output voltage. The output voltage is then regulated through the turns ratio of the secondary and bias windings.

In bias winding feedback, the bias winding may be placed closer to the secondary winding for tighter coupling and thus better regulation or it may be placed away from the secondary winding for loose regulation of output voltage. Bias winding

FEEDBACK COMPONENTS					
Recommended Bias Diode			1N4003 - 1N4007		Recommended diode is 1N4003. Place diode on return leg of bias winding for optimal EMI. See LinkSwitch-XT Design Guide
R1			500 - 1000	ohms	CV bias resistor for CV/CC circuit. See LinkSwitch-XT Design Guide
R2			200 - 820	ohms	Resistor to set CC linearity for CV/CC circuit. See LinkSwitch-XT Design Guide

Figure 8. Feedback Components Section.

feedback (for a CV only output characteristic) is shown in Figure 9 and involves selection of two resistors R1 and R2, which form a divider network to regulate the bias winding. Resistors R1 and R2 are also calculated in the design spreadsheet (see Figure 8). As these resistors also draw current from the bias winding, a combined value of 8 kΩ results in a good compromise between no-load consumption and prevention of peak charging due to leakage inductance to improve load regulation.

The alternate choice is secondary side optocoupler feedback. Here the output signal is directly sensed and fed back to the *LinkSwitch-XT* FEEDBACK pin via an optocoupler (see Figure 10). Secondary-side feedback eliminates the need for a bias winding and is more accurate then primary-side (bias winding) feedback. However, it requires additional components and is higher cost compared to bias winding feedback. Both of these schemes are also summarized in Table 3.

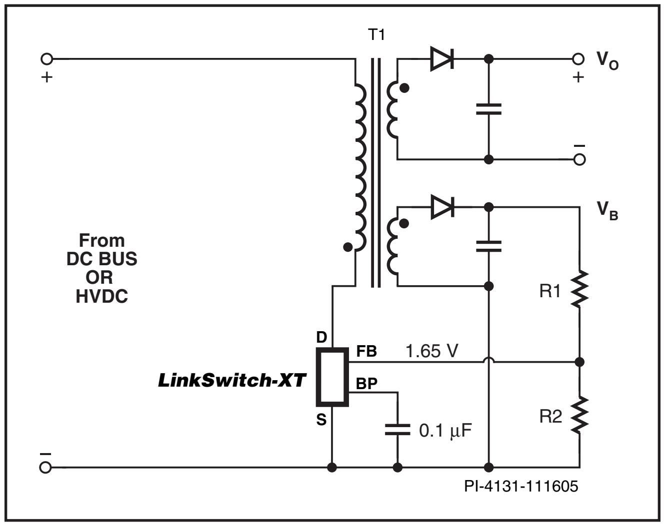


Figure 9. Primary-Side Feedback (Bias Winding Feedback) Scheme Used in a CV Only Output Characteristic Design.

Tips for *Clampless* designs

The mechanical construction of the transformer plays a crucial role in *Clampless* designs. Care should be taken to reduce the leakage inductance and increase the intra-winding capacitance of the primary winding. Intra-winding capacitance is defined as the capacitance measured from one end of a winding to the other end while all other windings are open. This is best achieved by using a 2-layer primary winding as noted in Figure 12. It is common to use a layer of tape between 2 primary layers. This should be avoided for *Clampless* designs, as this tends to reduce intra-winding capacitance. Even with the increased winding capacitance, no-load power of < 300 mW is easily possible with *LinkSwitch-XT*. For typical *Clampless* designs, the leakage inductance is below 90 µH and the intra-winding capacitance is greater than 40 pF.

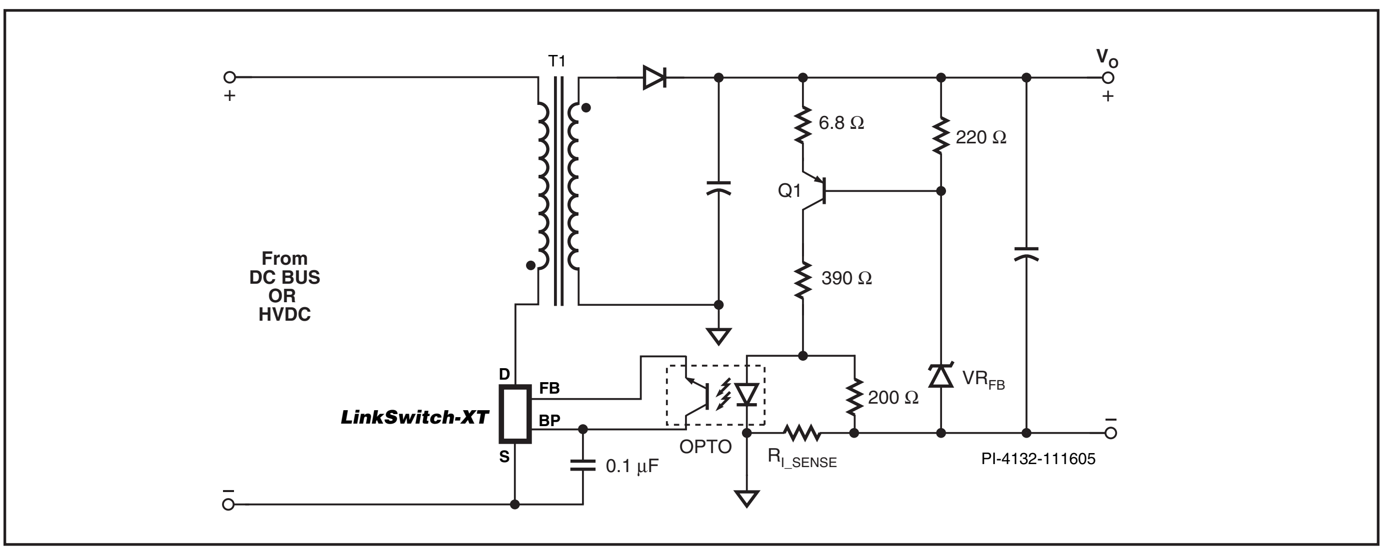


Figure 10. Secondary-Side Feedback Scheme Used for a CV/CC Output Characteristic Design.

Figure 11 shows the factors to be considered while deciding the mechanical structure of the transformer.

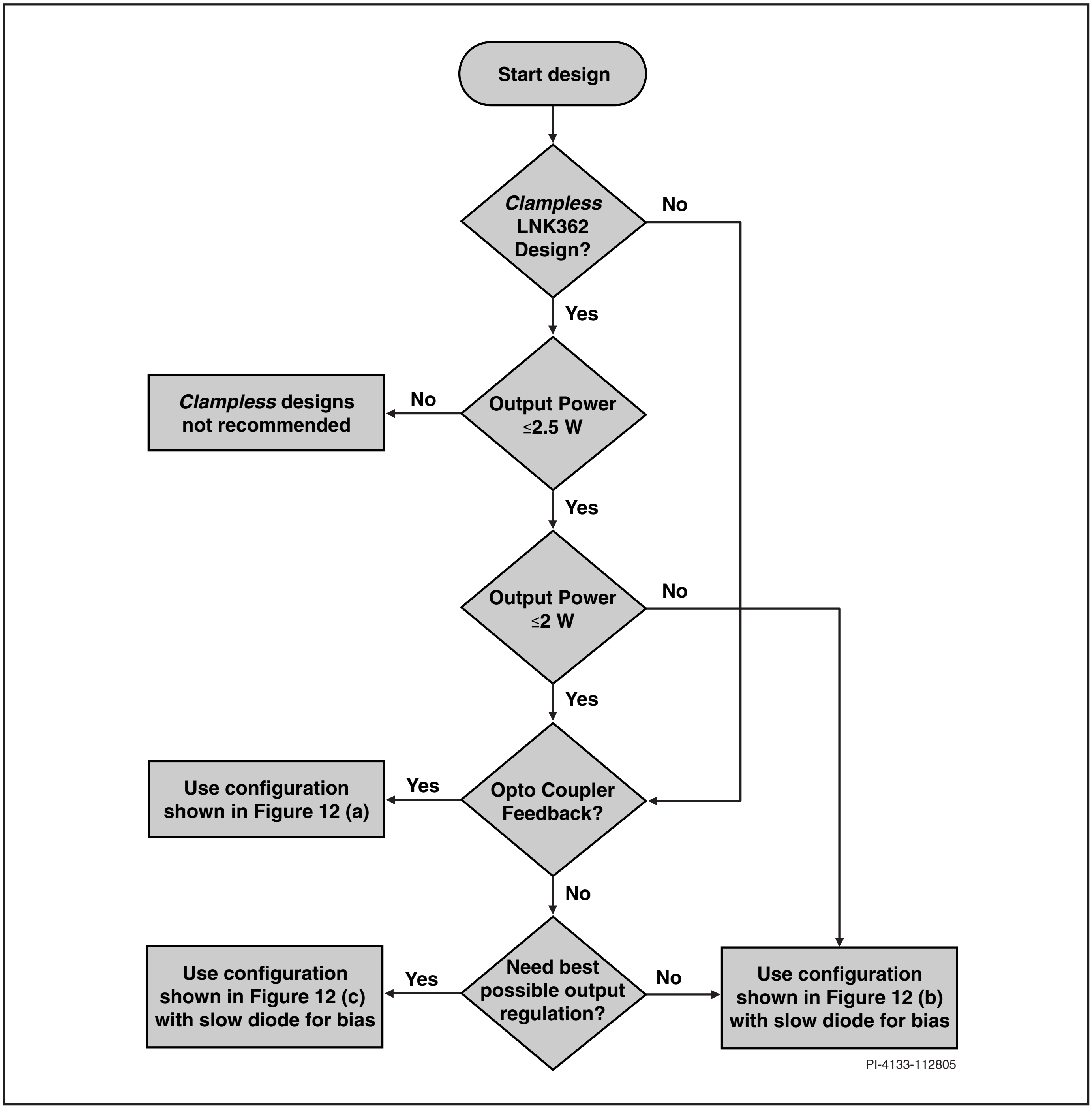
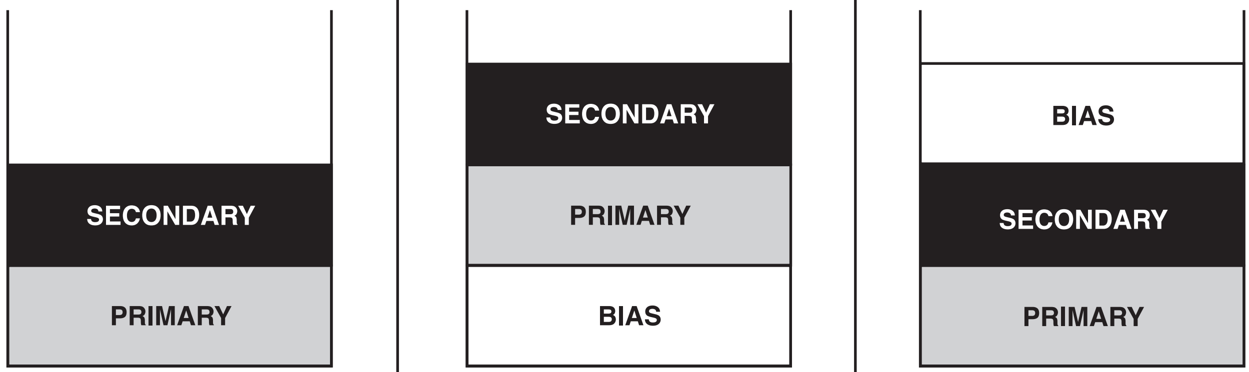


Figure 11. Flowchart For Deciding Mechanical Structure of Transformer.



(a)	(b)	(c)
• No bias winding • For *Clampless* designs use 2 primary layers, LNK362 and ≤ 2 W only	• For *Clampless* LNK362 designs and ≤ 2.5 W only • Bias winding feedback ideal for designs that require loosely regulated output voltage • Improved EMI performance over (a) & (c) due to reduction in leakage inductance ringing	• For *Clampless* LNK362 designs, 2 primary layers and ≤ 2 W only • Provides best output voltage regulation with bias winding feedback

Figure 12. Mechanical Structure of the Transformer in LinkSwitch-XT Designs.

Notes

Notes

Revision	Notes	Date
A	-	11/05
B	Formatting	11/05

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