Semiconductor insights inc.

3000 Solandt Road
Kanata, Ontario,
K2K 2X2 Canada
Tel: (613) 599-6500
Fax: (613) 599-6501
e-mail: info@semiconductor .com
web site: http://www.semiconductor.com

June 2002

Key Feature Analysis of the
(Manufacturer) (Part #) (Part Description)

THIS COPY SUPPLIED EXCLUSIVELY
FOR THE USE OF:

Marketing

Important notice regarding the use of this report:

Report ID#: 0403-00000-S-5KF-11

04/29/03

Key Feature Analysis of the (Manufacturer) (Part #) (Part Description)

By

Analyst's Name

June 2002

Semiconductor Insights Inc. 3000 Solandt Road, Kanata, Ontario, Canada, K2K 2X2 Tel: (613) 599-6500, Fax: (613) 599-6501

Table of Contents

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

List of Photographs and Figures

Section 2 - Architectural Overview

Section 3 – Data Path

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

Section 4 – Address Path

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

Section 5 – RX Prescaler

Section 6 – Phase Frequency Detector

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

Section 7 – ADC Converter

Section 8 – SI Standard Cells

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

Device Summary Table

Package Type:	100-pin TQFP
Package Markings (Top):	SI Example IC Kanata, Canada 0230
Package Markings (Bottom):	None
Manufacturer:	Semiconductor Insights
Die Markings:	SI © Ⓜ 2002 Example
Speed	166 Mhz
Die Size:	4.86 mm x 5.82 mm = 120 mm2
Process:	Double Metal, multipoly* CMOS Triple Well Technology
Organization:	Memory composed of 4 Banks Each Bank has 16 X 4 X 2 = 128 memory Blocks. Each memory block has 128C x 512R. Memory space of a Bank is thus given as 128 x 512 x 128 = 8M and Total space = 32M Horizontal Wordlines Vertical Bitlines.
Redundancy:	Each memory Block has four Redundant Wordline Drivers. And one Redundant Column Access Decoder.
Minimum Observed Line Width/Pitch by optical Microscopy (+ 0.15 μm)	
Poly Gate Length:	0.35 μm**
Metal 1:	0.6/1.2 μm
Metal 2:	0.8/1.6 μm

* Indicates cross-section is required to identify the number of poly layers.
** Indicates cross-section is required to confirm these statements.

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

1.0 Introduction

The following report is an example report produced by Semiconductor Insights to illustrate the reports that the company produces. Examples of text, photographs and schematics have been taken from a variety of devices including a DRAM device, a Flash device, an A/D converter and a Frequency Synthesizer. The following introduction was taken from the analysis on the DRAM device.

The following report is a design analysis of the Semicondcutor Insights example report, which is a 16M Synchronous DRAM (SDRAM) organized in a 512K × 16 Bit × 2 Banks arrangement. The device comes packaged in a 50-pin Thin Small Outline Package (TSOP II) measuring 21.12 mm x 10.11 mm = 213.50 mm^2. The operating voltage is 3.3 V and the clock frequency range includes 83 MHz, 100 MHz, 111 MHz, 125 MHz and 143 MHz.

An interesting layout feature of the Semiconductor Insights example device is that the SN and SP generation circuits are located among the bitline sense amplifiers, thus requiring less layout space and increasing the die efficiency.

The Semiconductor Insights example device is fabricated using a double metal, double poly CMOS process on a 3.22 mm × 5.73 mm die.

This report includes the following sections:

- Architectural Overview (Section 2.0);
- Data Path - DRAM (Section 3.0);
- Address Path – Flash (Section 4.0);
- RX Prescaler – Frequency Synthesizer (Section 5.0);
- Phase Frequency Detector (Section 6.0);
- A/D Converter – A/D Converter (Section 7.0);
- SI Standard Cells (Section 8.0);
- Signal List.

Unless stated otherwise, the default transistor length is 0.35 µm.

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

©Semiconductor Insights Inc.
3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

2.0 Architectural Overview

The Architecture Overview is intended to provide an overview of the package and the die. The following section contains information about the device package, die structure and also information about transistor and device structure.

2.1 Package Overview

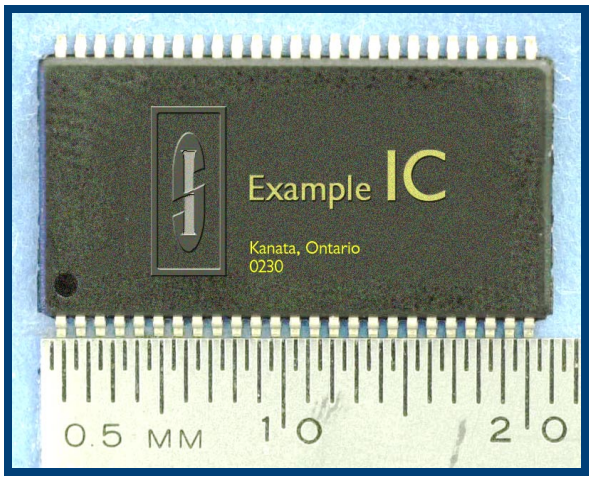
The SI Example IC is packaged inside a 50-pin TSOP II (Thin Small Outline Package) with dimensions of 21.12 mm × 10.11 mm = 213.50 mm^2.

The package contains the following top markings:

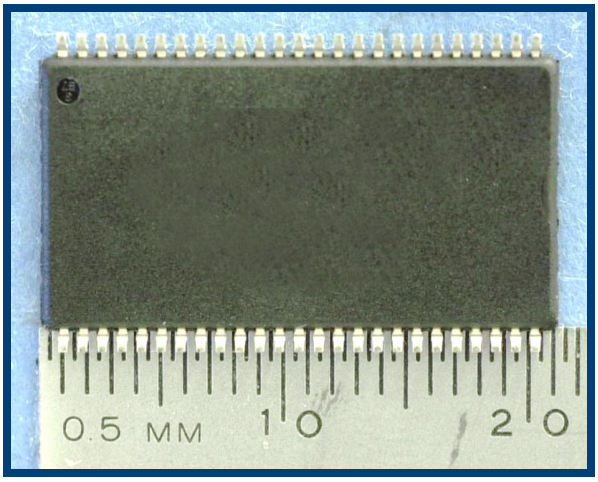
SI Example IC
Kanata, Ontario
0230

and there are no bottom markings:

The packages are presented as Photographs 2.1.1 and 2.1.2.



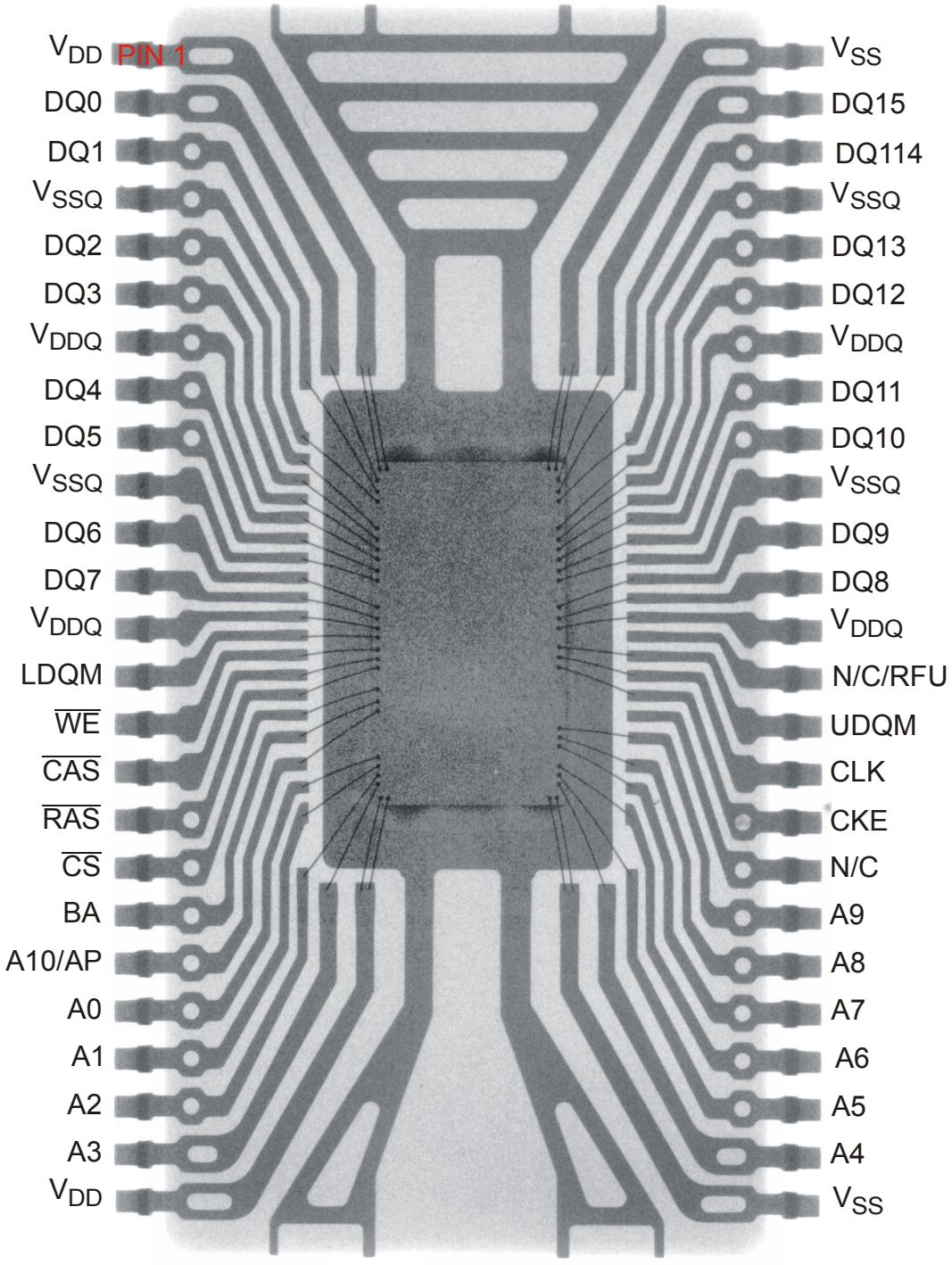
Photograph 2.1.1: Package (top).



Photograph 2.1.2: Package (bottom).

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

The pinout for the package and the package X-ray is presented as Photograph 2.1.3. For pad layout, refer to Photograph 2.2.1.



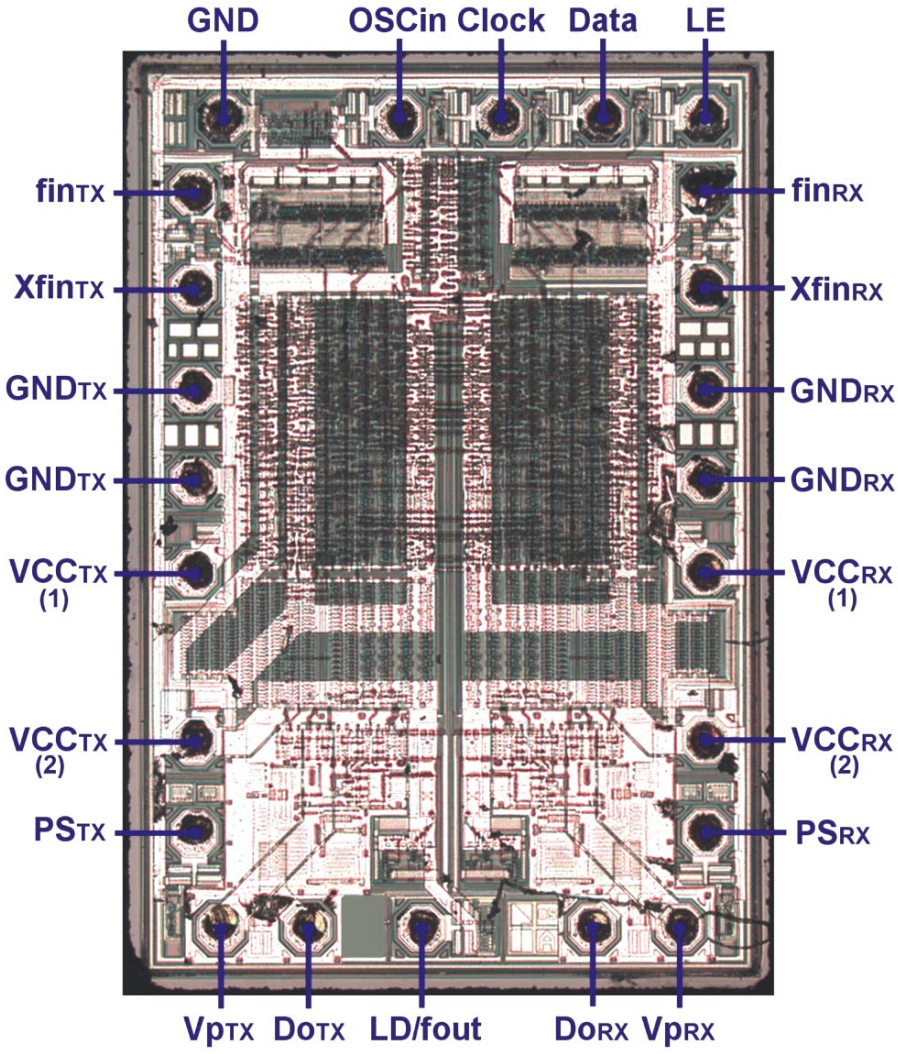
Photograph 2.1.3: Package X-ray.

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

2.2 Physical Die Overview

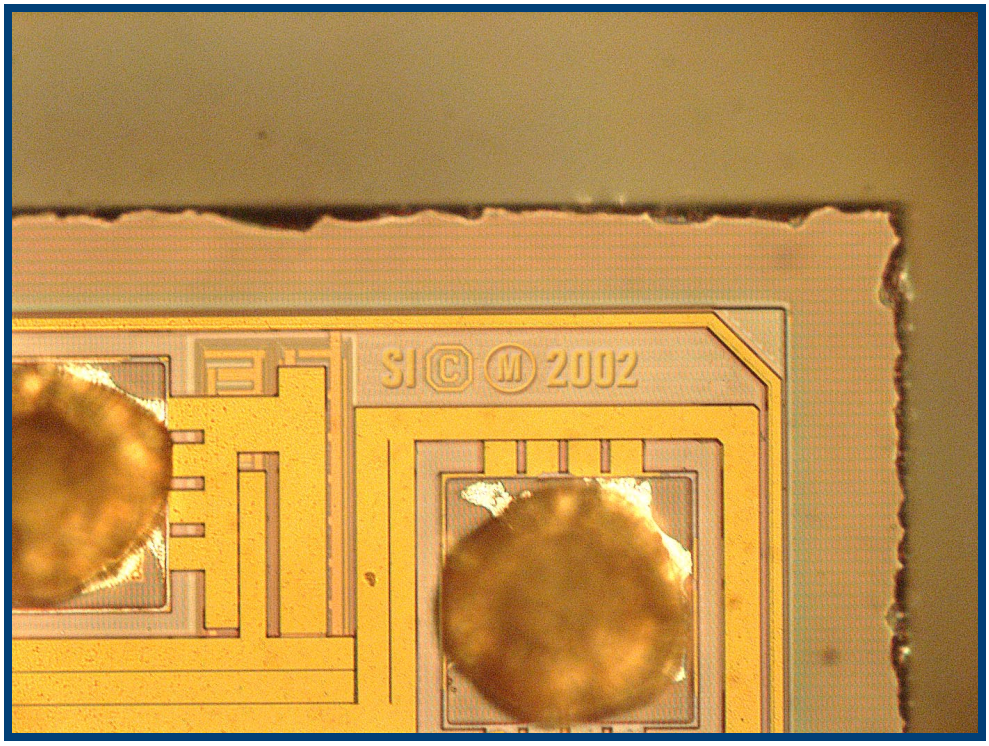
The physical die overview contains photographs of the die and any markings found on the die. In this example the pins have been annotated on the die.

The SI Example IC is manufactured using a 0.35 µm triple-metal double poly U-ESBIC4 BiCMOS process. However, the minimum feature size observed on the die was 0.5 µm. Trace pitches are 1.0 µm for polysilicon and 1.75 µm for metals 1 and 2. The die is presented in Photograph 2.2.1 and Photograph 2.2.2 shows the die markings.



Photograph 2.2.1: Die with annotated bond pad names.

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com



Photograph 2.2.2: Die Markings.

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

2.3 Functional Die Overview

2.3.1 Overview

The following section contains information about the layout of the circuitry found on the device. The section contains a die map, power bussing and for memory devices a die structure and address bit maps. The following write up was taken from a memory report.

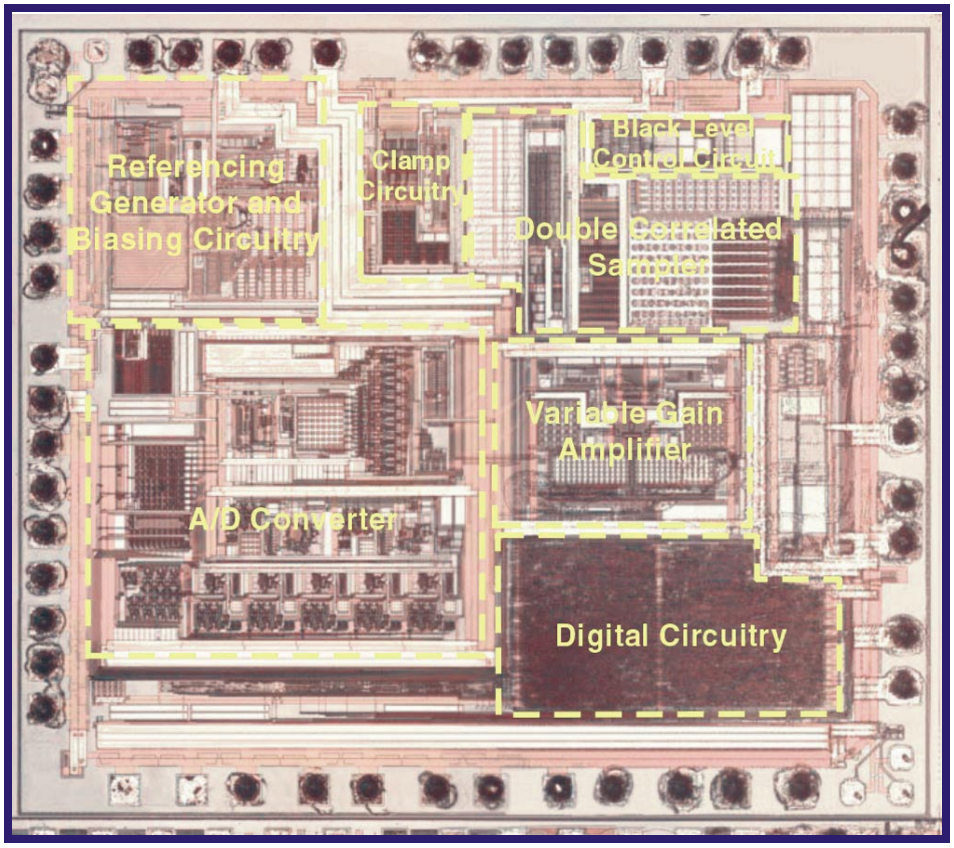
The die is functionally divided into two BANKS, then further into eight BLOCKS. Every Block contains eight 128 kb SUB-BLOCKS and two REDUNDANT 2 kb SUB-BLOCKS for redundant column accesses. There are 2 redundant wordlines for an additional 2 kb of redundant row access. For further explanation of the die structure refer to Figure 2.3.1.2.

A more specific breakdown of the die dimensions is found in Figure 2.2.1, from which we can estimate a die efficiency of 56%. The estimated die efficiency is within the expected range for SDRAM memories, but slightly higher due to the improved layout scheme of the SN and SP generator circuitry.

This section includes the following functional information about the die:

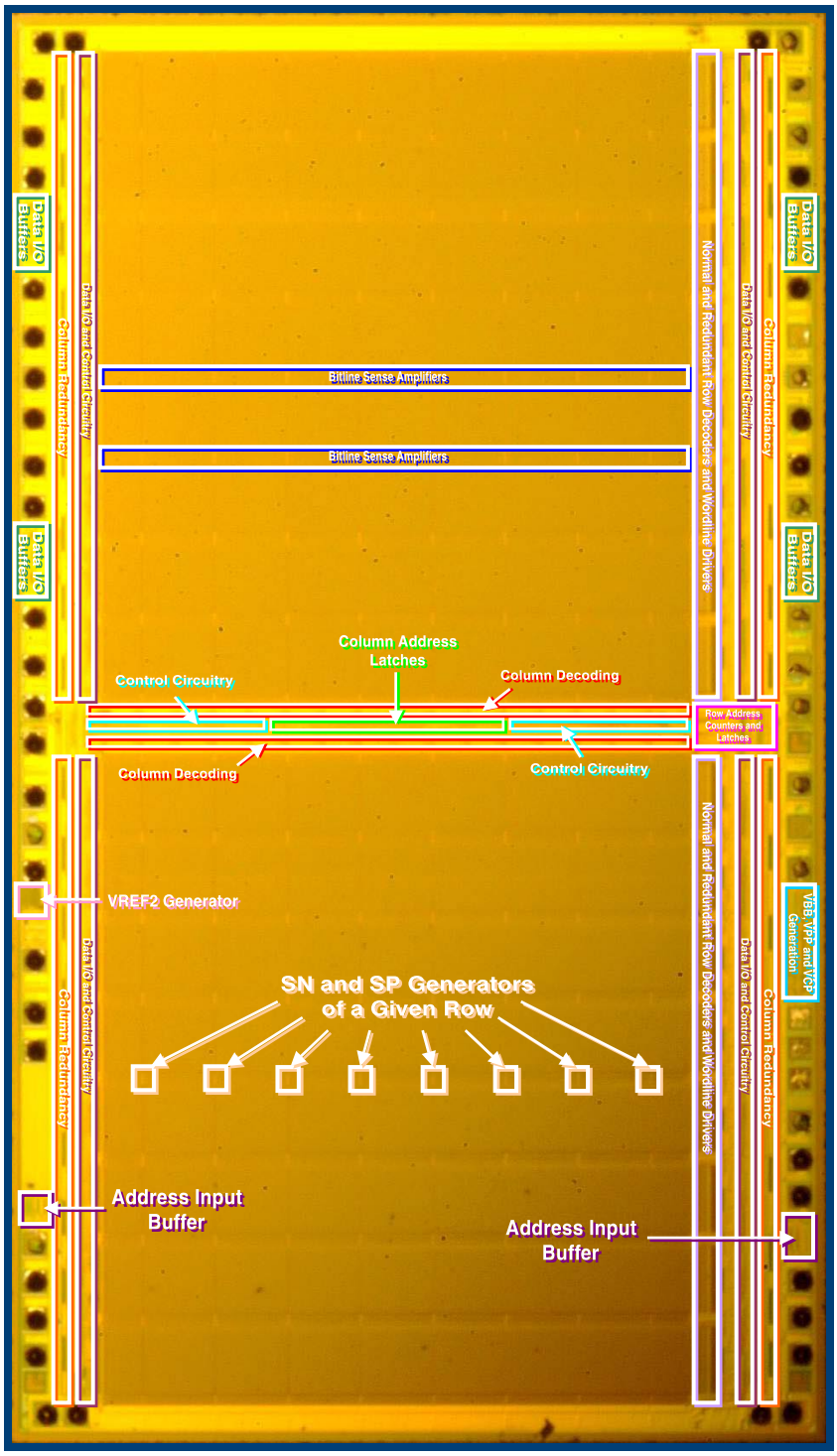
- Die Map (Photograph 2.3.1.1 and 2.3.1.2);
- Die Dimensions (Figure 2.3.1.1)
- Die Structure (Figure 2.3.1.2);
- Bitmap - Column Select (Figure 2.3.2.1);
- Address Bitmap - Row Select (Figure 2.3.2);
- Power Bussing (Photograph 2.3.3.1 and Figure 2.3.3.1);

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com



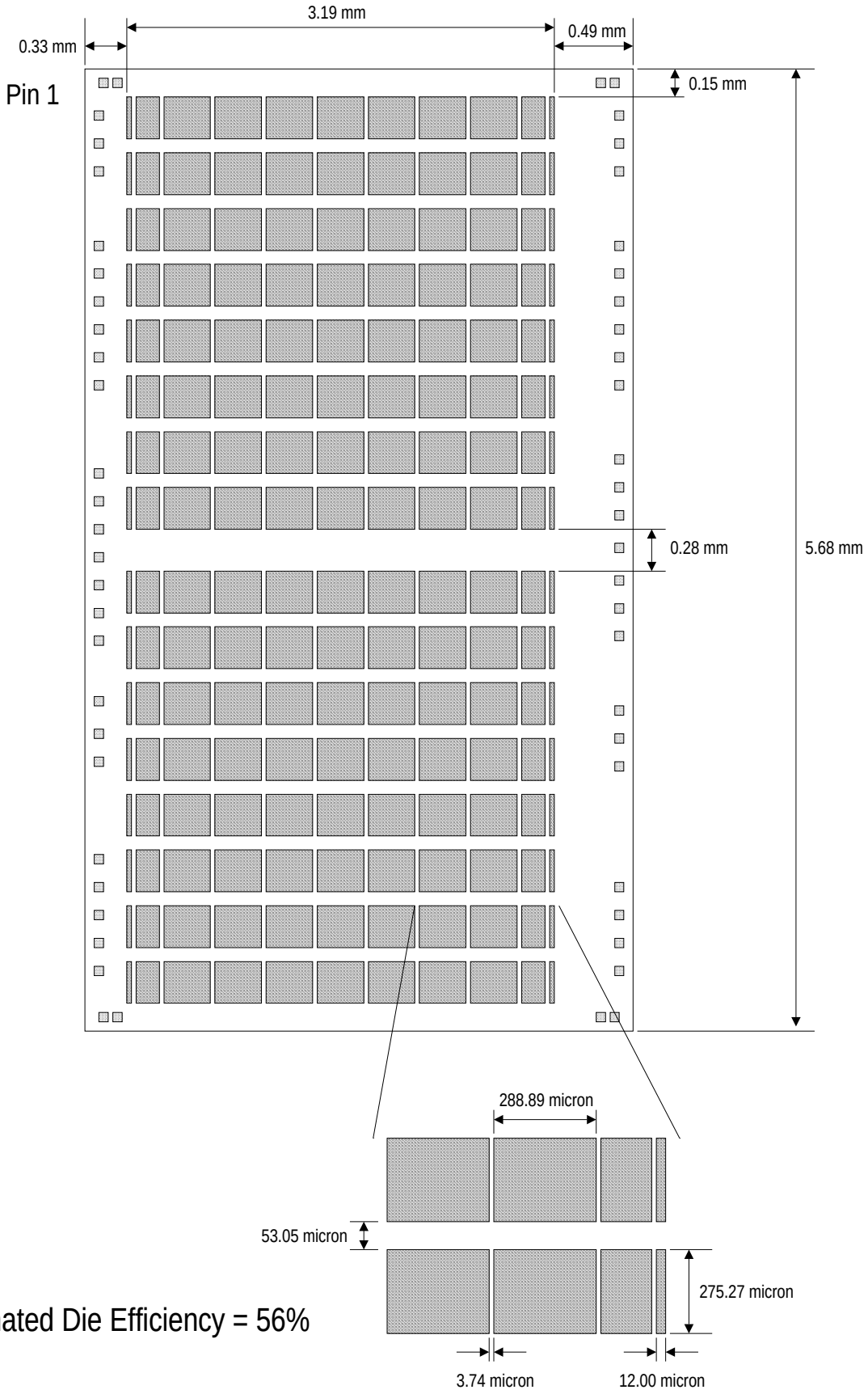
Photograph 2.3.1.1 Die Map 1.

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com



Photograph 2.3.1.2: Die map. 2

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com



Estimated Die Efficiency = 56%

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	DIEDIMEN	SI NUMBER:	SI01
DATE_TIME:	6-17-2002_13:38		
LOCATION:	XXX	INITIALS:	DM

Figure 2.3.1.1 DIE DIMENSIONS

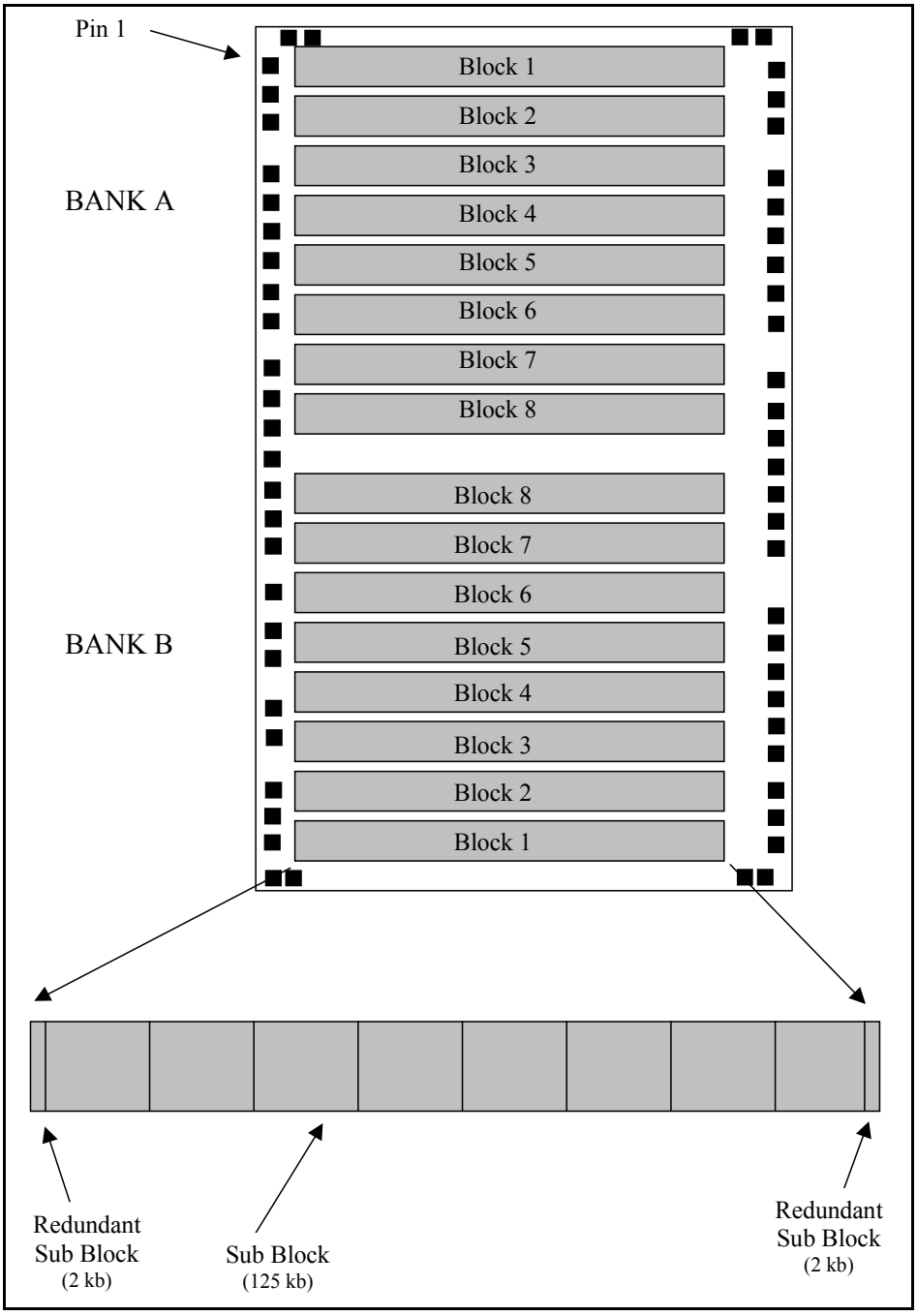


Figure 2.3.1.2: Die Structure.

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

2.3.2 Address Bitmap

For memory devices SI can include address bit maps which show the phisical storage locations corresponding to logical address designations.

Bank Decoding

A dedicated pin [BA] is used for Bank decoding. The [BA] pin is buffered in Figure 4.1 and the buffered signal ~BA1 is then bussed to the control Section where it derives several signals.

In the Bank Address Control Block the ~BA1 signal is used to produce the complementary signals BARAA and BARAB for row control and the complementary signals AYCK2A and AYCK2B for column control. The BARAA and BARAB signals are used in two instances of the Row Address Latches, one for each bank. Depending on the value of the complementary signals, it will choose Row circuitry for one bank, and deactivate the other one. The complementary signals AYCK2A and AYCK2B are used for two instances, one for each bank. The signal will select column circuitry for one bank, and deactivate the other bank.

In the Bank Selection Block, the complementary signals ~BSB2 and ~BSA2 are derived from ~BA1. These signals are used to reset the line in the Row Address Latches for the bank that is deselected.

Wordline Decoding

Within each Bank, there are four levels of row decoding to select a wordline.

First in the Row Address Path schematic for 1 Bank, [A10] and [A9] are decoded to select two BLOCKS out of 8. Each Block contains 16 groups of 32 Wordlines. In the Row Predecoders 3, addresses [A8], [A7], [A6], and [A5] are decoded to select one of these groups.

The Row Predecoders 2 schematic decodes addresses [A4], [A3], and [A2] to choose, within one group of 32 Wordlines, a sub-group of 4 Wordlines.

The Row Predecoders 1 schematic decodes addresses [A1] and [A0] to choose one of these four wordlines.

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

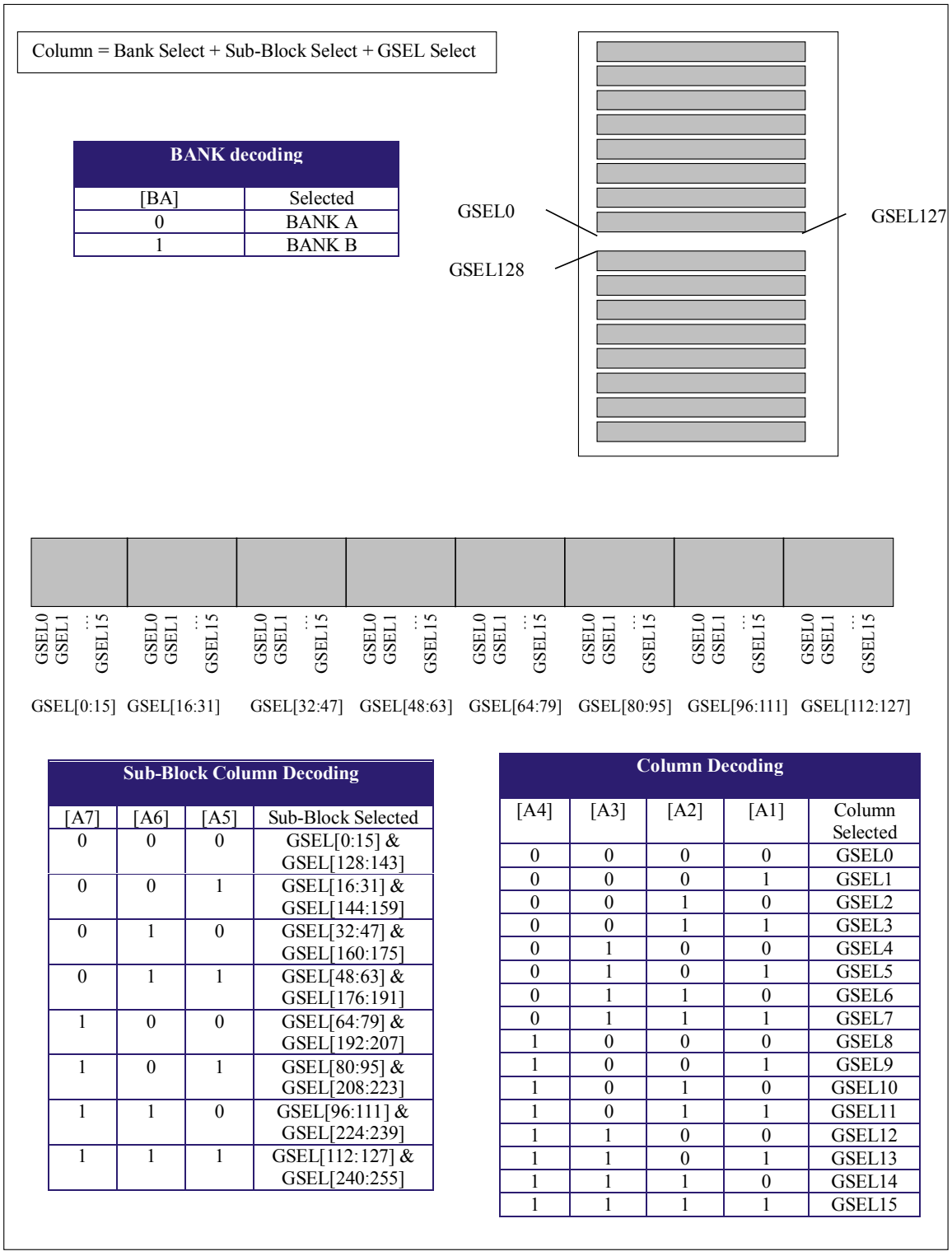
Bitline Control

There are two levels of Column decoding besides the Bank decoding in order to activate a bitline.

First a sub-block needs to be selected. Each block contains 8 of these sub-blocks. The Column Address Decoders schematic selects two sub-blocks that shall remain active.

Afterwards addresses [A4], [A3], [A2], and [A1] will select a GSEL signal that will be activated in the two sub-blocks in the Column Address Decoder.

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com



BANK decoding	
[BA]	Selected
0	BANK A
1	BANK B

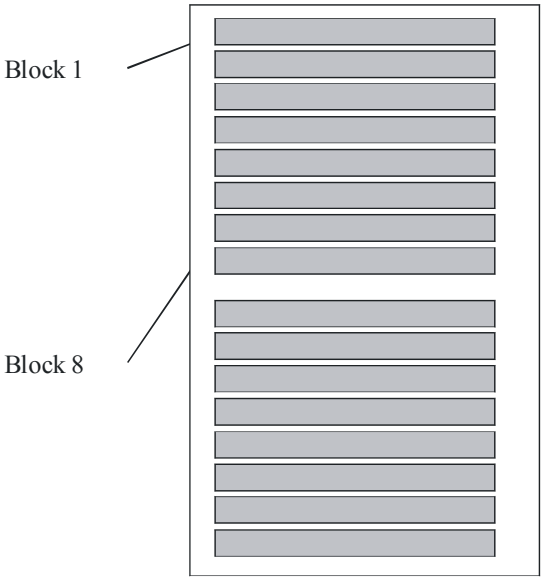
Sub-Block Column Decoding			
[A7]	[A6]	[A5]	Sub-Block Selected
0	0	0	GSEL[0:15] & GSEL[128:143]
0	0	1	GSEL[16:31] & GSEL[144:159]
0	1	0	GSEL[32:47] & GSEL[160:175]
0	1	1	GSEL[48:63] & GSEL[176:191]
1	0	0	GSEL[64:79] & GSEL[192:207]
1	0	1	GSEL[80:95] & GSEL[208:223]
1	1	0	GSEL[96:111] & GSEL[224:239]
1	1	1	GSEL[112:127] & GSEL[240:255]

Column Decoding				
[A4]	[A3]	[A2]	[A1]	Column Selected
0	0	0	0	GSEL0
0	0	0	1	GSEL1
0	0	1	0	GSEL2
0	0	1	1	GSEL3
0	1	0	0	GSEL4
0	1	0	1	GSEL5
0	1	1	0	GSEL6
0	1	1	1	GSEL7
1	0	0	0	GSEL8
1	0	0	1	GSEL9
1	0	1	0	GSEL10
1	0	1	1	GSEL11
1	1	0	0	GSEL12
1	1	0	1	GSEL13
1	1	1	0	GSEL14
1	1	1	1	GSEL15

Figure 2.3.2.1: Address Bitmap - Column Select.

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

Wordline Select = Bank Select + Block Select
+ Group of 32 Wordlines Select
+ Group of 4 Wordlines Select
+ Wordline Select



BANK Decoding	
[BA]	Selected
0	BANK A
1	BANK B

Block Decoding		
[A10]	[A9]	Blocks Selected
0	0	BLOCK 1 & BLOCK 5
0	1	BLOCK 2 & BLOCK 6
1	0	BLOCK 3 & BLOCK 7
1	1	BLOCK 4 & BLOCK 8

Group of 32 Wordlines Decoding				
[A8]	[A7]	[A6]	[A5]	Selected
0	0	0	0	WL0 - WL31
0	0	0	1	WL32 - WL63
0	0	1	0	WL64 - WL95
0	0	1	1	WL96 -WL127
0	1	0	0	WL128 - WL159
0	1	0	1	WL160 - WL191
0	1	1	0	WL192 - WL223
0	1	1	1	WL224 - WL255
1	0	0	0	WL256 - WL287
1	0	0	1	WL288 - WL319
1	0	1	0	WL320 - WL351
1	0	1	1	WL352 - WL383
1	1	0	0	WL384 - WL415
1	1	0	1	WL416 - WL447
1	1	1	0	WL448 - WL479
1	1	1	1	WL480 - WL511

Group of 4 Wordlines Decoding			
[A4]	[A3]	[A2]	Selected
0	0	0	WL0 - WL3
0	0	1	WL4 - WL7
0	1	0	WL8 - WL11
0	1	1	WL12 - WL15
1	0	0	WL16 - WL19
1	0	1	WL20 - WL23
1	1	0	WL24 - WL27
1	1	1	WL28 - WL31

Wordline Decoding		
[A1]	[A0]	Selected
0	0	WL0
0	1	WL1
1	0	WL2
1	1	WL3

Figure 2.3.2.2: Address Bitmap - Row Select.

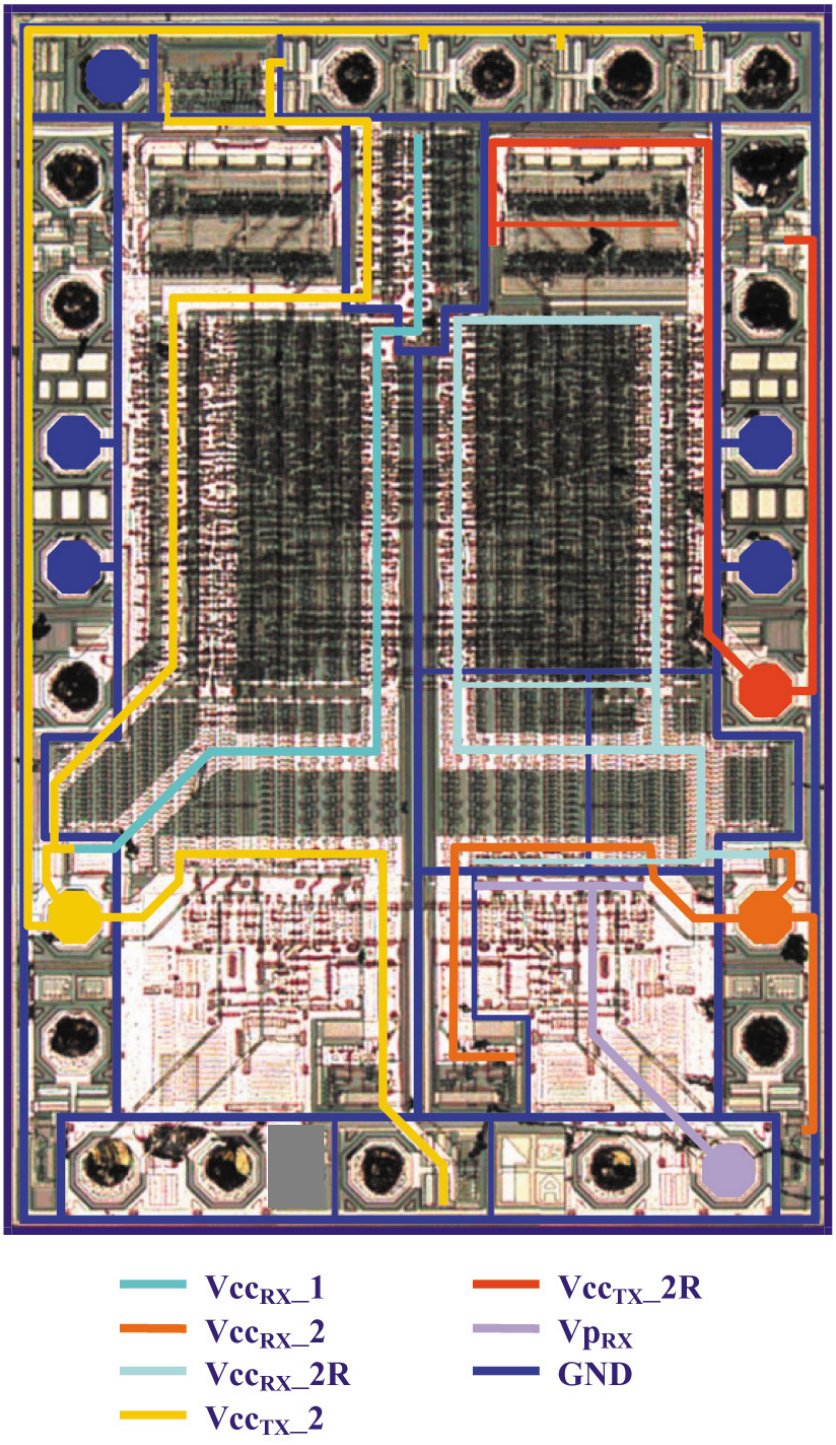
3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

2.3.3 Power Bussing Map

SI provides simplified diagrams showing the routing of power lines, namely power ground although other voltages are shown when appropriate. Examples of power bussing diagrams have been taken from both a mixed signal device and a memory device.

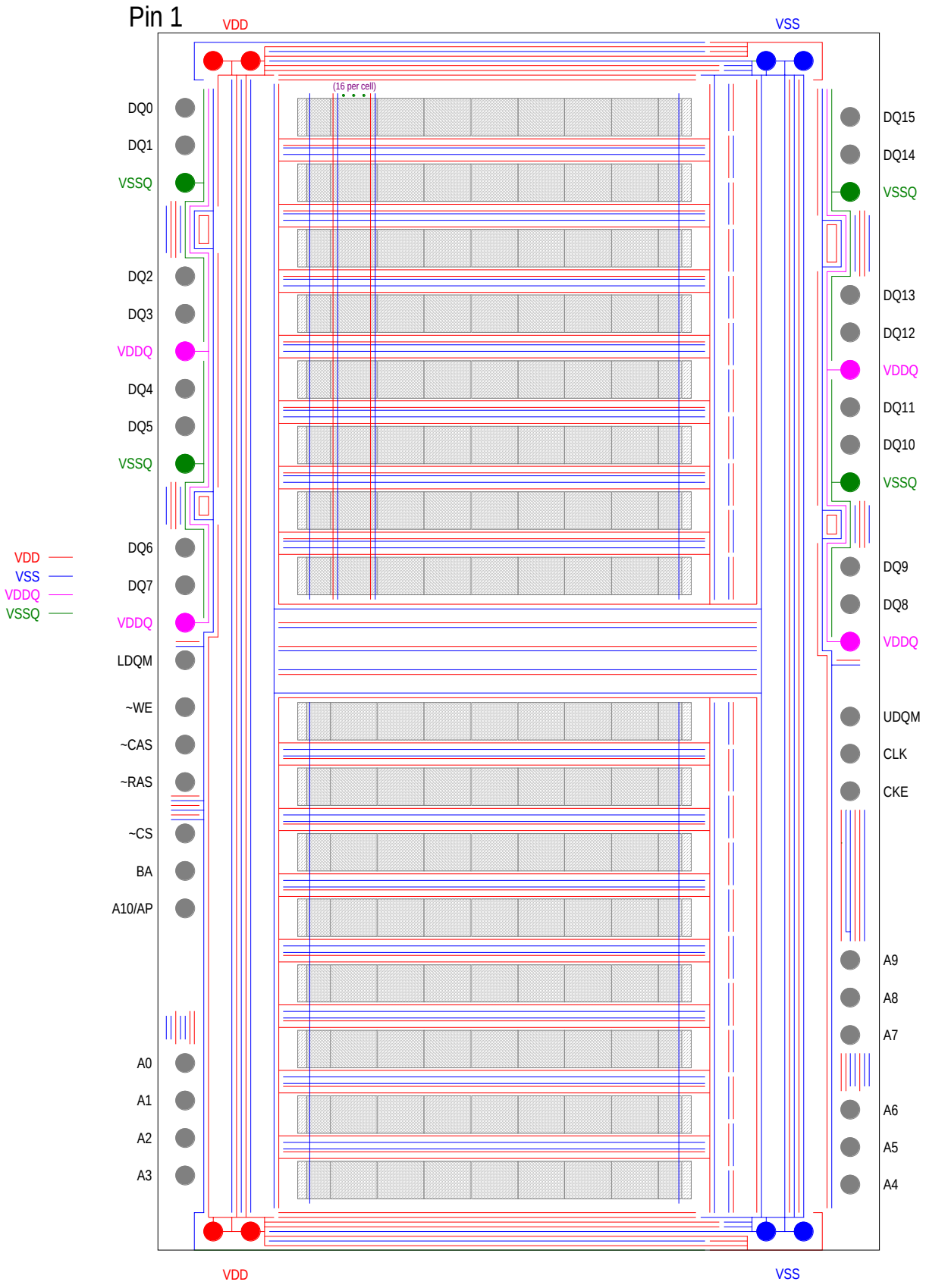
The SI Example IC die contains two pairs of GND_{TX}, GND_{RX}, Vcc_{TX} and Vcc_{RX} supply pads. Each pad pair has been bonded to a single package pin (i.e., a total of 4 package pins, each bonded to a pad pair as noted above). Internally, the GND_{RX} and GND_{TX} pads are shorted. The Vcc_{RX} pads are not shorted internally and the upper pad $Vcc_{RX}(2)$ supplies only the BiPolar Prescaler, while the bottom pad supplies the remaining RX synthesizer logic. The RX Charge Pump is supplied from a separate Vp_{RX} pad. There is a separate ground (GND) pad for the OSCin buffer and the Serial Interface logic. However GND, GND_{RX} and GND_{TX} pads are shorted internally. The OSCin buffer and Serial Interface is supplied from the Vcc_{TX} bottom pad. Photograph 2.3.2.1 shows the Power Supply distribution throughout the die.

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com



Photograph 2.3.3.1: Power Bussing

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

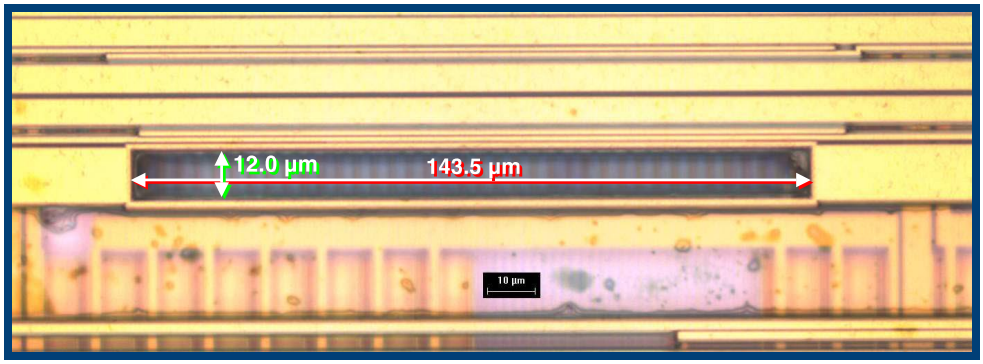


Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	POWERBUSSING	SI NUMBER:	SI01
DATE_TIME:	6-24-2002_10:40		
LOCATION:	XXX	INITIALS:	DM

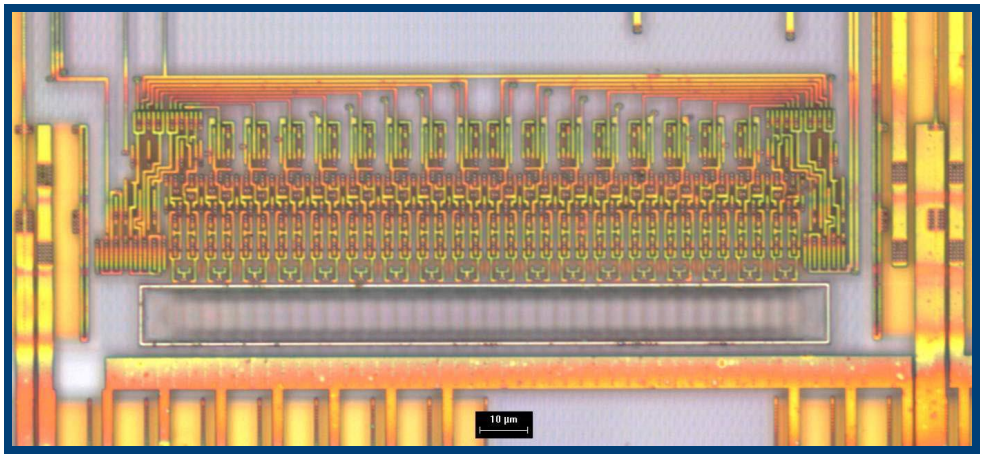
Figure 2.3.3.1 POWER BUSSING DIAGRAM (NOT TO SCALE)

2.3.4 Device Structures

The following section contains select images from a variety of IC's intended to illustrate various structures found on analyzed IC's.

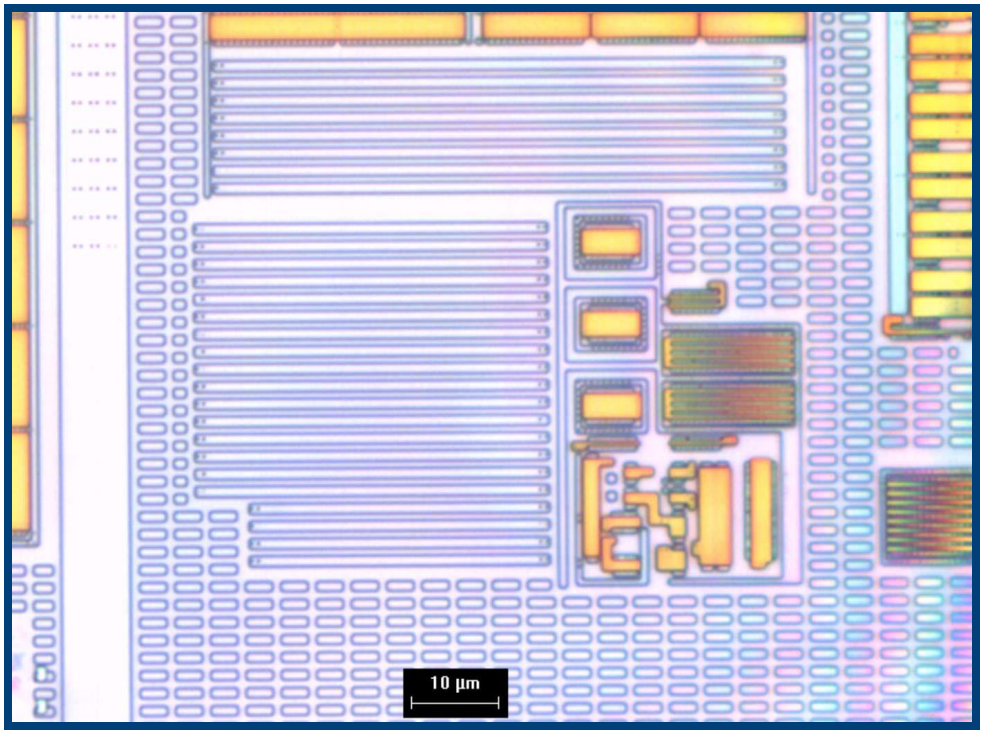


Photograph 2.3.4.1: Column fuses (metal 2).

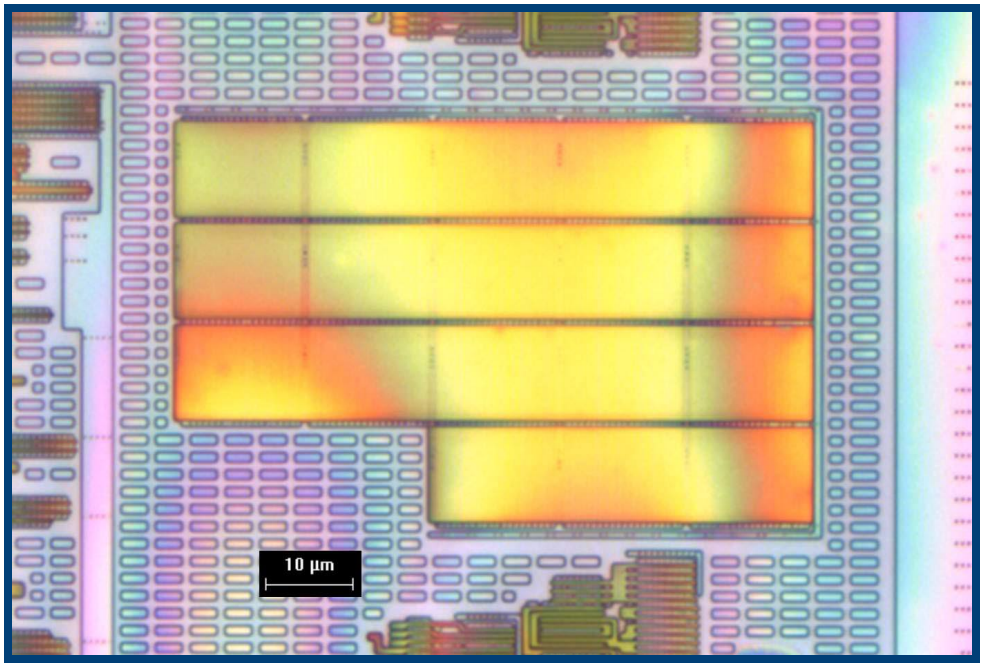


Photograph 2.3.4.2 Column fuses (metal 1).

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

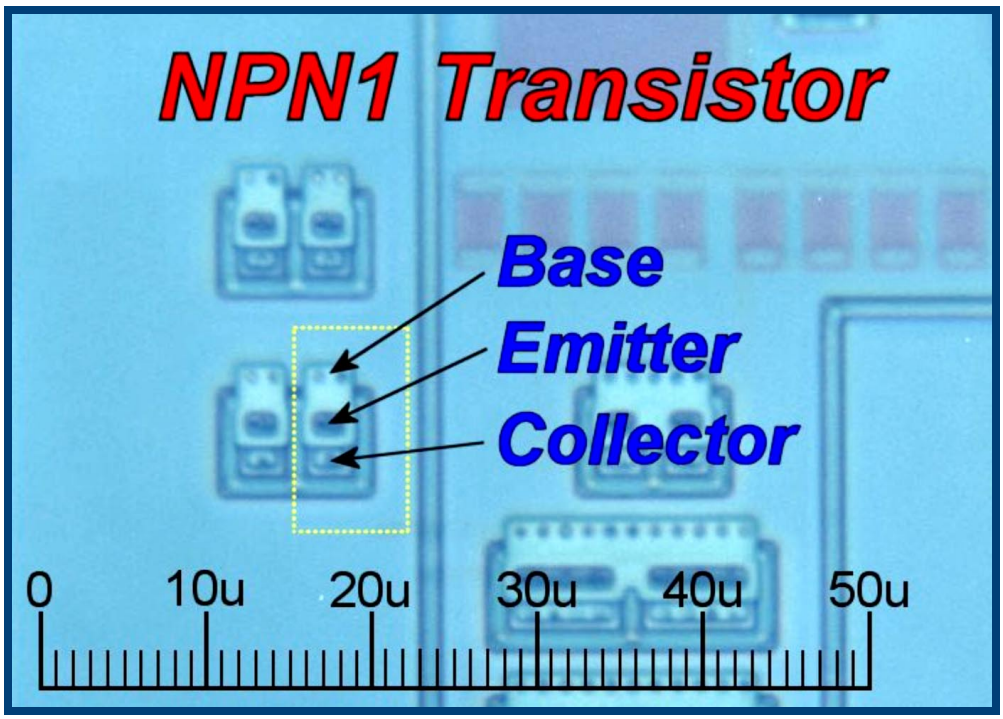


Photograph 2.3.4.3: Diffusion resistor.



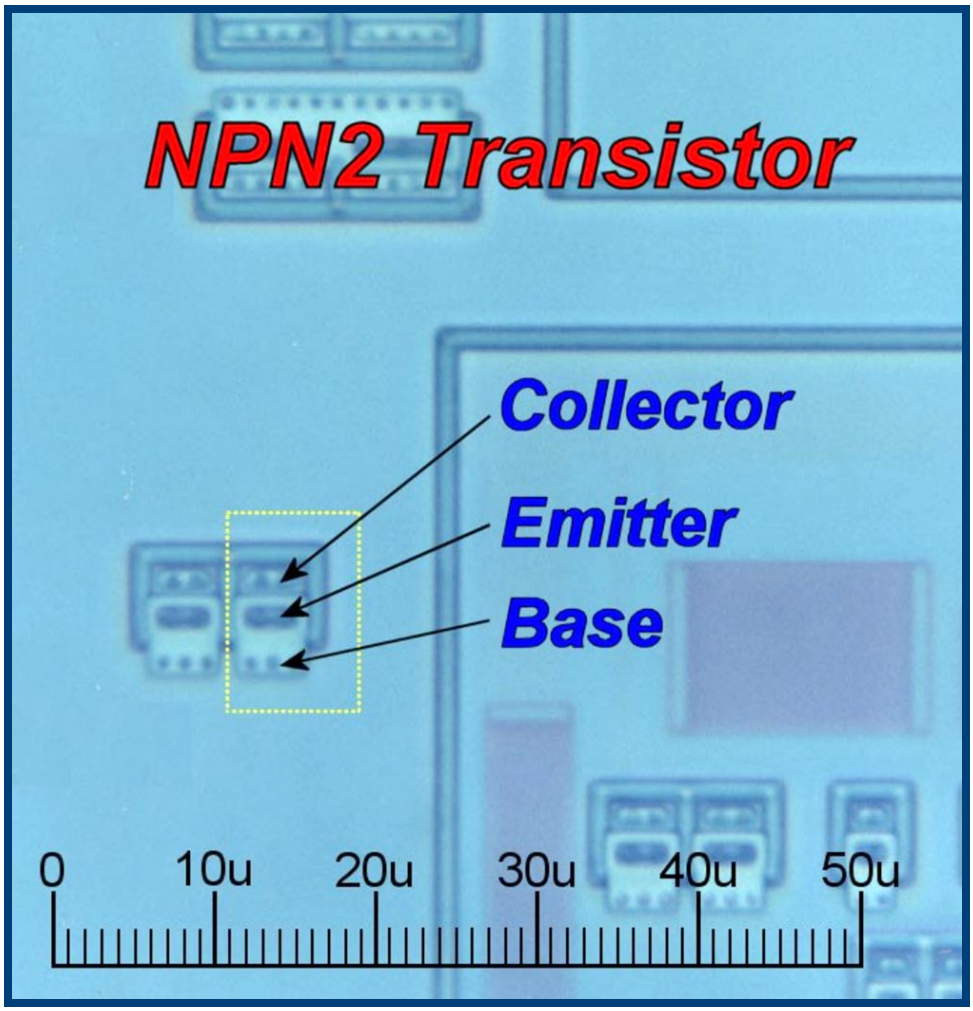
Photograph 2.3.4.4: Poly-diffusion capacitor.

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com



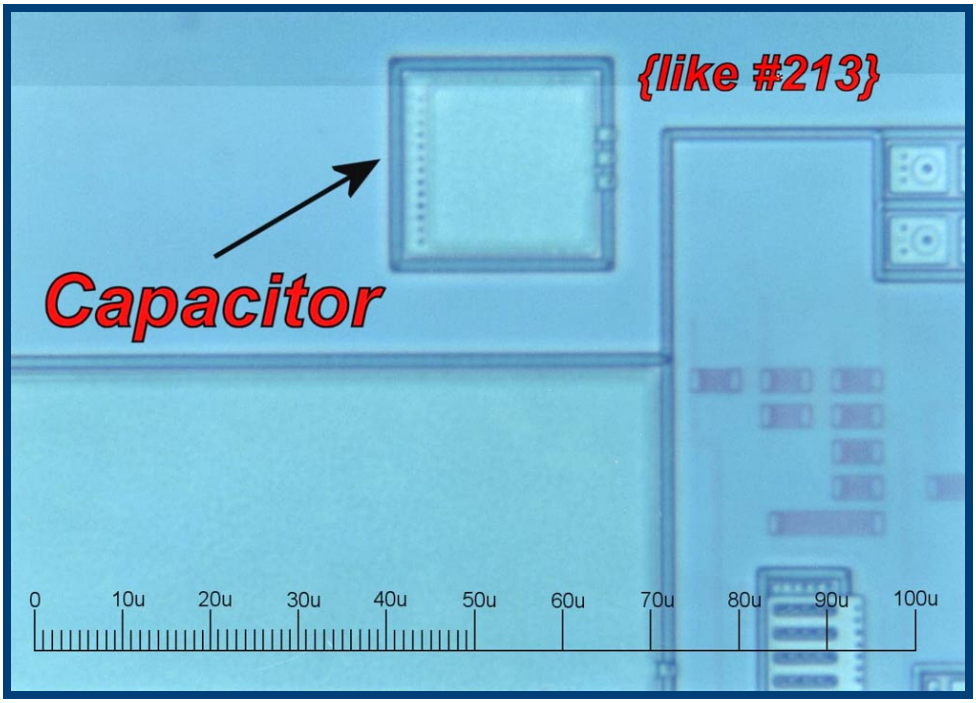
Photograph 2.3.4.5 NPN HBT (NPN1).

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com



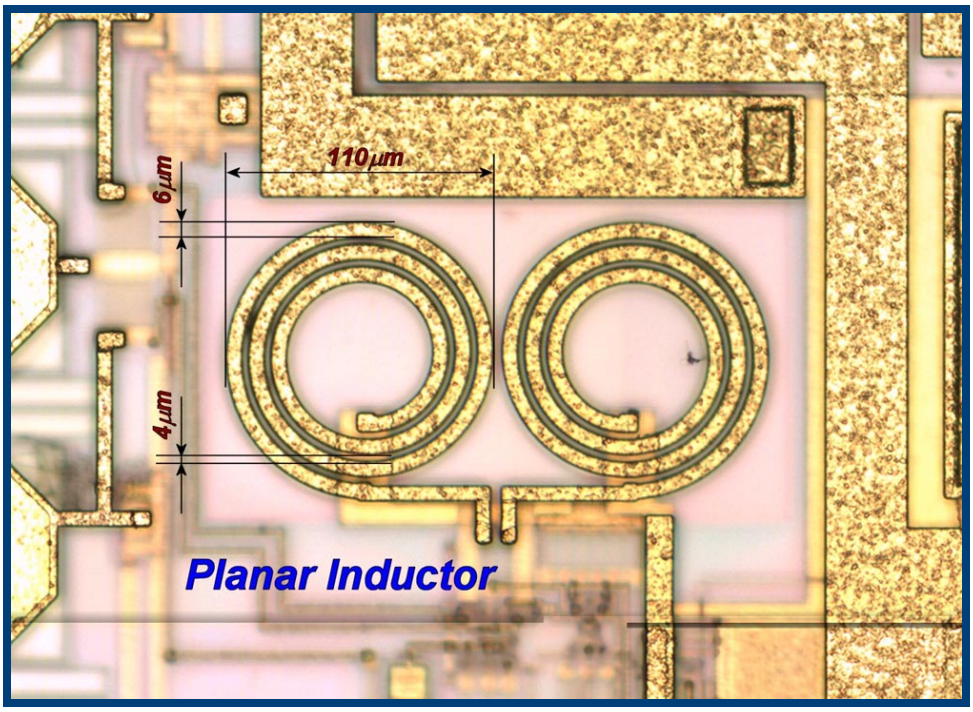
Photograph 2.3.4.6 NPN HBT (NPN2).

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com



Photograph 2.3.4.7 Capacitor (device #213).

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com



Photograph 2.3.4.8 Planar Inductor.

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

2.4 Design Overview

The following section gives an overview of the structure of the device from a circuit standpoint and contains information about the overall structure of the device. The text was taken from a report on a frequency synthesizer. A top level diagram is included in Figure 2.4.1.

Note: The figure numbers found in this section refer to the original report, that the content was taken from.

The SI Example IC is a double PLL integer frequency synthesizer. It contains two very similar synthesizers, the RX synthesizer (2.6 GHz) the TX synthesizer (1.2 GHz). This Key Feature Report covers only the RX synthesizer circuitry.

The RX synthesizer contains:

- dual modulus Prescaler (32/33 or 64/65)
- 7-bit programmable swallow counter with divide ratio from 0 to 127
- 11-bit programmable N divider with divide ratio from 3 to 2047
- 14-bit programmable reference divider with divide ratio from 3 to 16,383
- Phase Frequency Detector
- Charge Pump with Current Switch and Fast Lock circuitry
- Power saving mode control

Both the RX and TX synthesizers are programmed through a simple 3-wire Serial Interface. The Reference Frequency (OSCin) input buffer is common for both synthesizers. The LD/fout Output pad allows monitoring of the Lock condition for both synthesizers as well as the Reference and N Counter output frequencies.

The Synthesizer design is rather conventional and not altogether sophisticated. The main benefit from the innovative BiCMOS technology is high operation frequency and low power consumption. However, the Charge Pump circuitry implements some solutions that minimize power consumption.

It has been found that the Standard Cell block, where the Synthesizer Programmable Counters are implemented, does not contain any flip-flop Standard Cells. Flip-flops are built from transmission gate based multiplexers and NAND gates. Connections between flip-flop elements are made through routing channels. A lot of Standard Cell simple gates (inverters, NANDS, NORS) have been found in the design with equally dimensioned PMOS and NMOS transistors.

The extracted SI Example IC RX Synthesizer circuitry is presented through schematics organized in a fully hierarchical manner with a top level shown in Figure 2. The top-level schematics contain, apart from the RX synthesizer circuitry, the Serial Interface, the OSCin Buffer and the Lock Detect/Frequency Monitoring circuitry. Connections to and from the TX synthesizer are left unconnected in Figure 2.

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

The main functional blocks of the SI Example IC covered by this Key Feature Report are described below:

1. RX ECL Prescaler: This circuit receives the RX frequency from the fin_{RX} pad and divides it by 32/33 or 64/65 depending on the RXSW bit setting and SWEN (Swallow Enable) input state.
2. RX Programmable Counters: There are 3 programmable counters: the Reference Counter with divide ratio R = 3 to 16,383, the N-Counter with ratio N = 3 to 2,047 and the Swallow Counter which is programmable between 0 and 127. Each Counter has an associated latch, containing the actual divide ratio.
3. RX Intermittent Mode Control: This circuit controls the RX Synthesizer Power Down mode and recovery from Power Down to Operating Mode. It also controls the RX Charge Pump operation to lower the supply current in a Lock condition.
4. RX Phase Frequency Detector (PFD): This is a rather conventional solution of a PFD. The RX_FC bit controls PFD operation depending on the VCO polarity type.
5. RX Charge Pump: The pump contains a current switch allowing the selection of a full scale output current between 1.5 mA and 6 mA. The RX Charge Pump also contains some interesting features like Fast Lock and Power Saving in Lock condition.
6. LD/fout Selector: This circuit drives the LD/fout PAD. Depending on signal LDS, T1 and T2 bit settings, it outputs Lock Detect information or one of TX/RX Reference or N-Counter output frequencies.
7. Serial Interface: This is a very simple 3-wire interface, based on a 23-bit serial register. The Serial Interface is used to program both TX and RX synthesizers.
8. OSCin Buffer: This circuit generates the internal Reference clocks for the TX and RX Reference Counters and Intermittent Control Circuits.

Input and Output Pad schematics and symbols can be found in Figures 11 through 11.5. Figures 12 through 12.12 contain symbols and schematics of Standard Cells and flip-flop macro-cells used in the CMOS logic portion of the design.

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

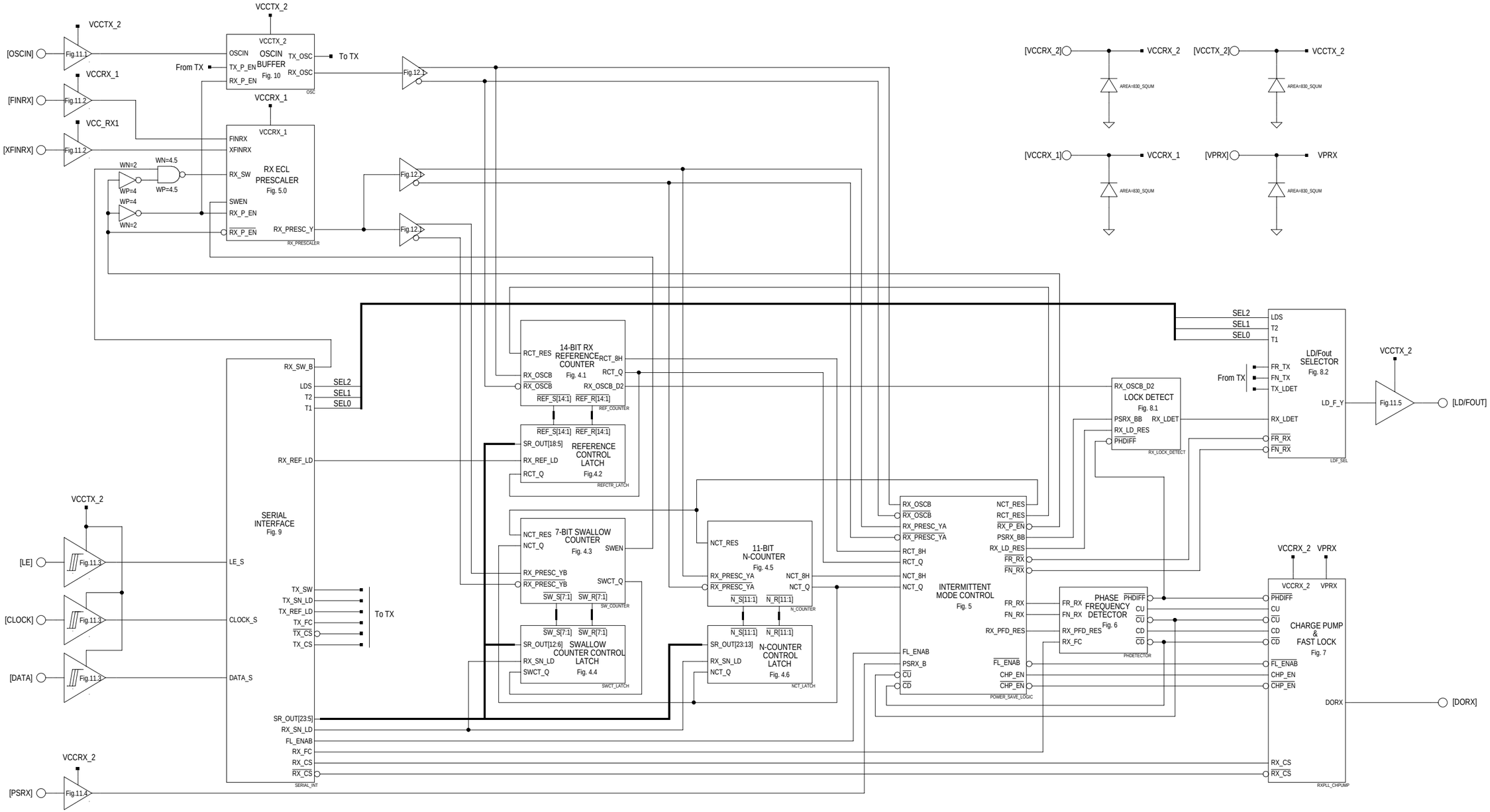


Figure 2.4.1 RX SYNTHESIZER BLOCK DIAGRAM

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT
DATE CODE:	0230
SCH_NAME:	RX_BLOCK
SI NUMBER:	SI01
DATE_TIME:	6-26-2002_10:51
LOCATION:	A1
INITIALS:	GM

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

3.0 Data Path

The data path section was taken from a memory report. The section is complex so a simplified top-level diagram was included as Figure 3.0. The data path then was divided into three main parts, 3.1, 3.2 and 3.3. Each subsection is fully hierarchical and contains a page-by-page signal list. These page by page signal list, which are inserted to help navigate through the report.

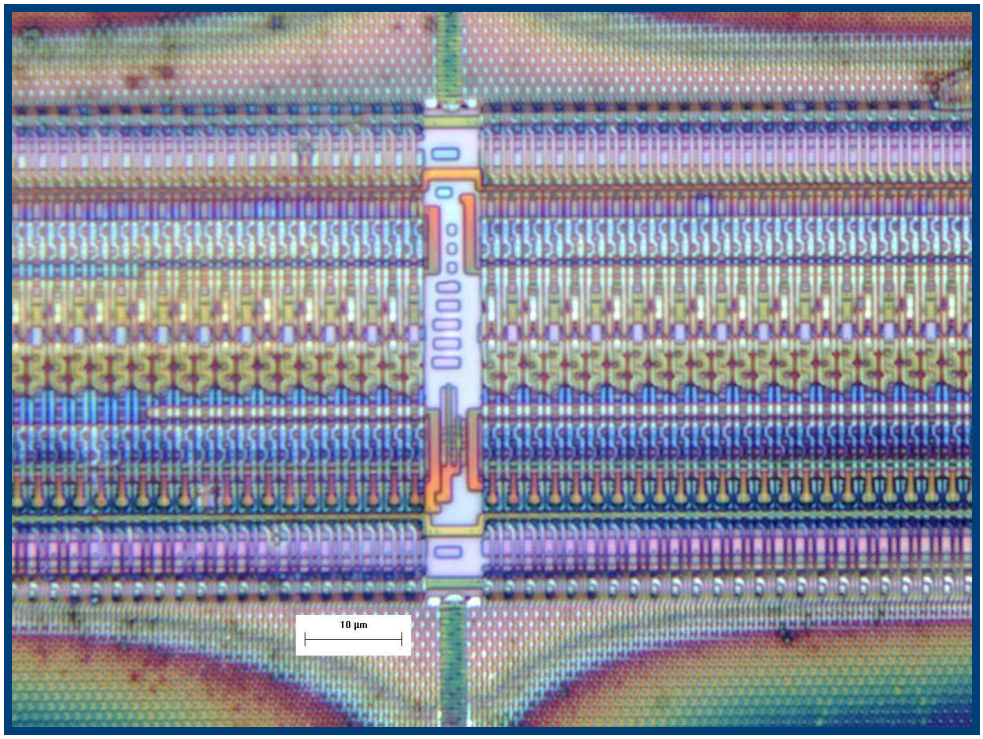
Note: The page-by-page lists were taken directly from the original report and therefore the figure numbers are not valid for this document.

3.1 Read and Write Paths

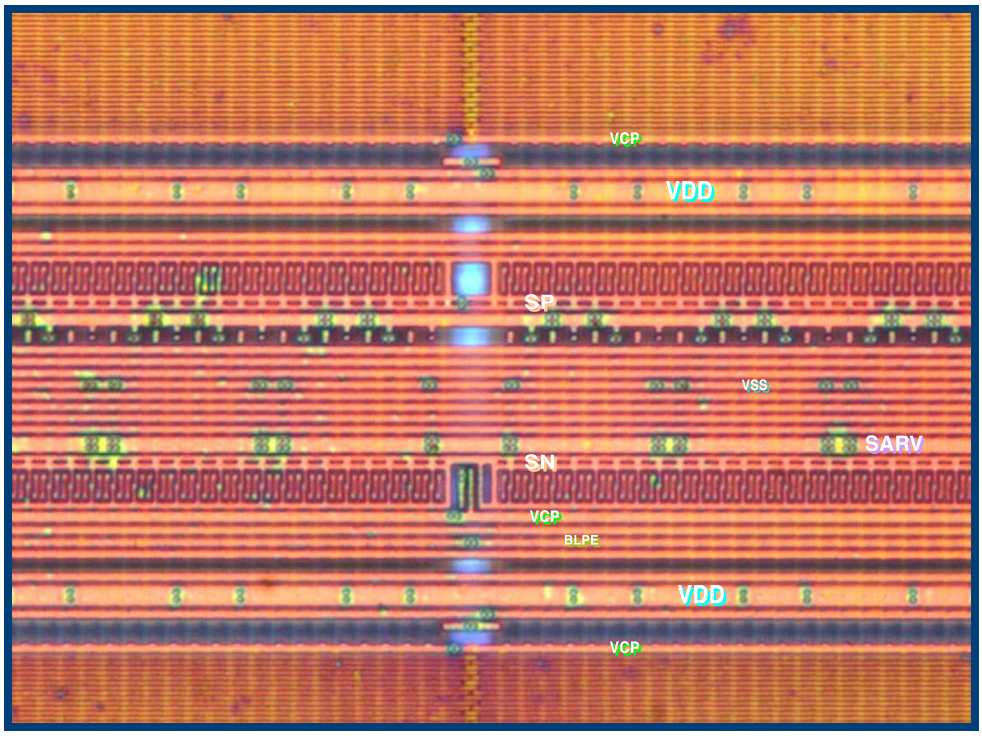
A functional block diagram of the data path is shown in Figure 3.0. The lower byte of the data is stored/read by accessing the left quadrant of each bank and DQ_[0:7] on the left side of the chip. The upper byte is stored/read by accessing the right quadrant of each bank and DQ_[8:15] on the right side of the chip.

Data is transferred to the bi-directional Global Data Buses through the Data Input Buffer of Figure 3.1.1.1 and routed to the Local Data Buses through the Data Bus Sense Amplifiers of Figures 3.2.3.1, 3.2.4.1 and 3.2.5.1. These schematics also show the global data bus/local data line structure. Read data is placed on the normal data lines or the redundant data lines by the bitline sense amplifiers (shown in Figures 3.2.6.1 and 3.2.7.1). The redundant data lines are used to transfer read data between the data bus sense amplifiers and the normal data lines or the global data bus. Write data is transferred via pass gates to the normal data lines and/or the redundant data lines. Redundant memory access is controlled by normal column enable or redundant column enable signal. SN and SP generation circuitry is located between the bitline sense amplifier blocks of each memory array sub-block thus taking up virtually no real estate on the die.

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com



Photograph 3.1.1: SN-SP generator circuit (poly).



Photograph 3.1.2: SN-SP generator circuit (metal 1).

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

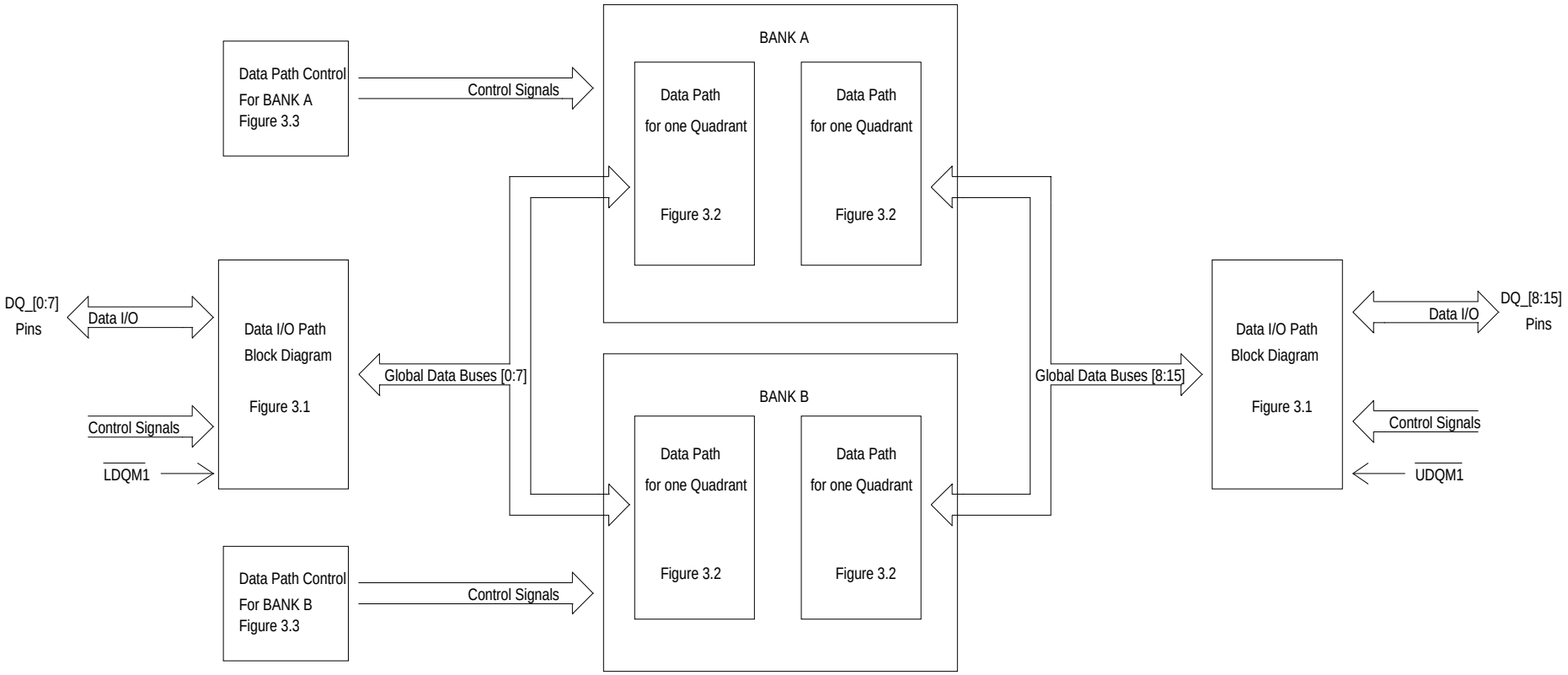


Figure 3.0 FUNCTIONAL BLOCK DIAGRAM DATA PATH

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	FBDDATA	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:33		
LOCATION:	A1	INITIALS:	AZ, LW

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Figure 3.1 – Data I/O Path for Left Side of Die

Signal ID	Source	Destination
CASLAT2		3.1
CASLAT3		3.1
CKE2	5.0	4.1, 3.1
CKPLSIL	5.0	3.2, 3.1
CLK2	5.0	4.1, 3.1
CLK2~	5.0	4.1, 3.1
DBPEL~	5.0	3.1
DQ0		3.1
DQ1		3.1
DQ2		3.1
DQ3		3.1
DQ4		3.1
DQ5		3.1
DQ6		3.1
DQ7		3.1
GDBO		3.1(BI)
GDBO~`		3.1(BI)
GDB1		3.1(BI)
GDB1~`		3.1(BI)
GDB2		3.1(BI)
GDB2~`		3.1(BI)
GDB3		3.1(BI)
GDB3~`		3.1(BI)
GDB4		3.1(BI)
GDB4~`		3.1(BI)
GDB5		3.1(BI)
GDB5~`		3.1(BI)
GDB6		3.1(BI)
GDB6~`		3.1(BI)
GDB7		3.1(BI)
GDB7~`		3.1(BI)
IO0CTRL[0:11]	3.1(BUS)	
IO1CTRL[0:11]	3.1(BUS)	
IO2CTRL[0:11]	3.1(BUS)	
IO3CTRL[0:11]	3.1(BUS)	
LDQM1~	5.0	3.2, 3.1
VREF2	7.4	5.0, 4.1, 3.1
WCACK	5.0	3.2, 3.1

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

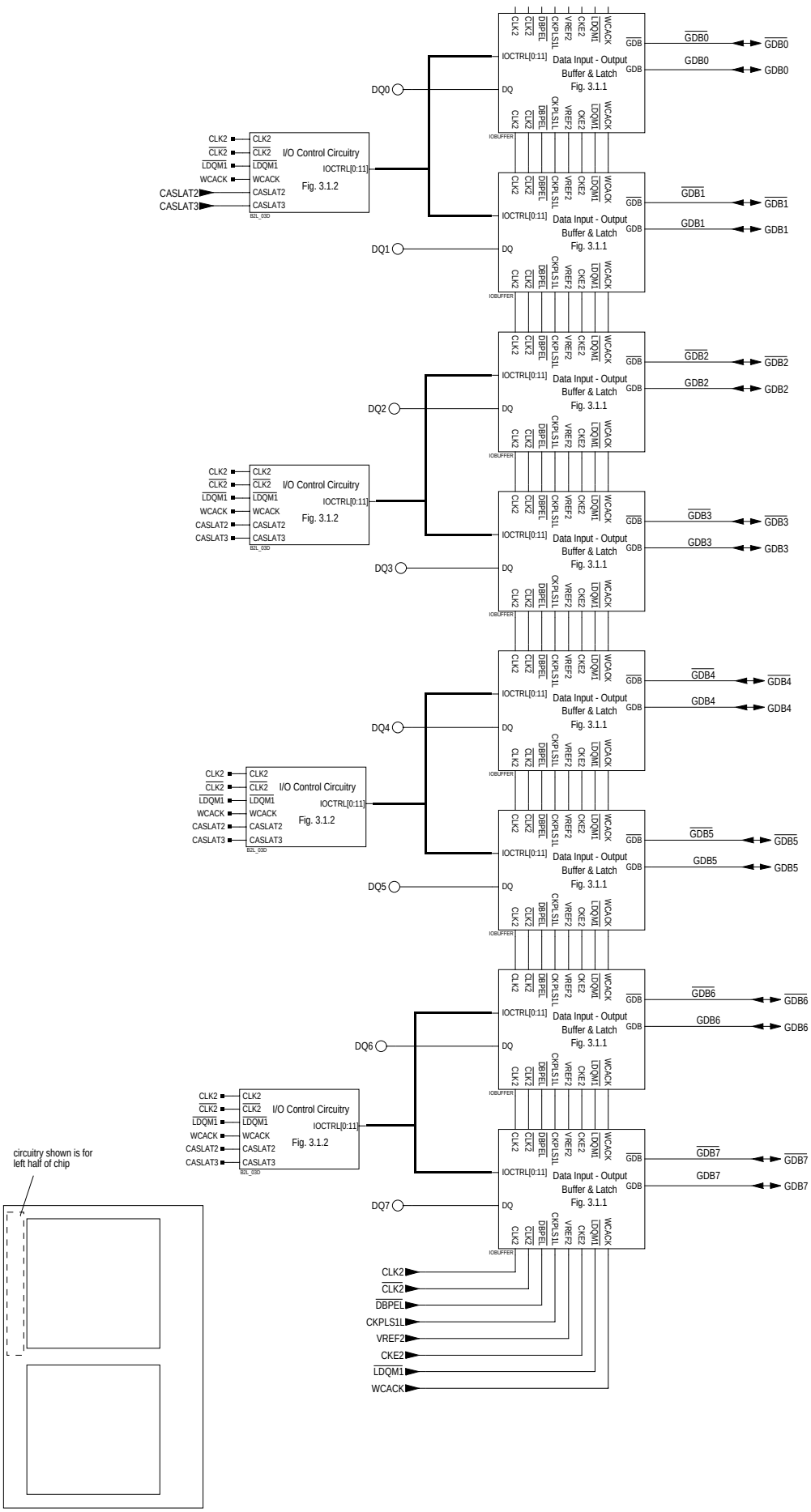


Figure 3.1 DATA I/O PATH FOR LEFT SIDE OF DIE

Part #:	SI EXAMPLE REPORT
DATE CODE:	FILE NAME OR DATE CODE
SCH_NAME:	SI NUMBER: SI01
DATE_TIME:	
LOCATION: AREA B2	INITIALS: AZ, LW

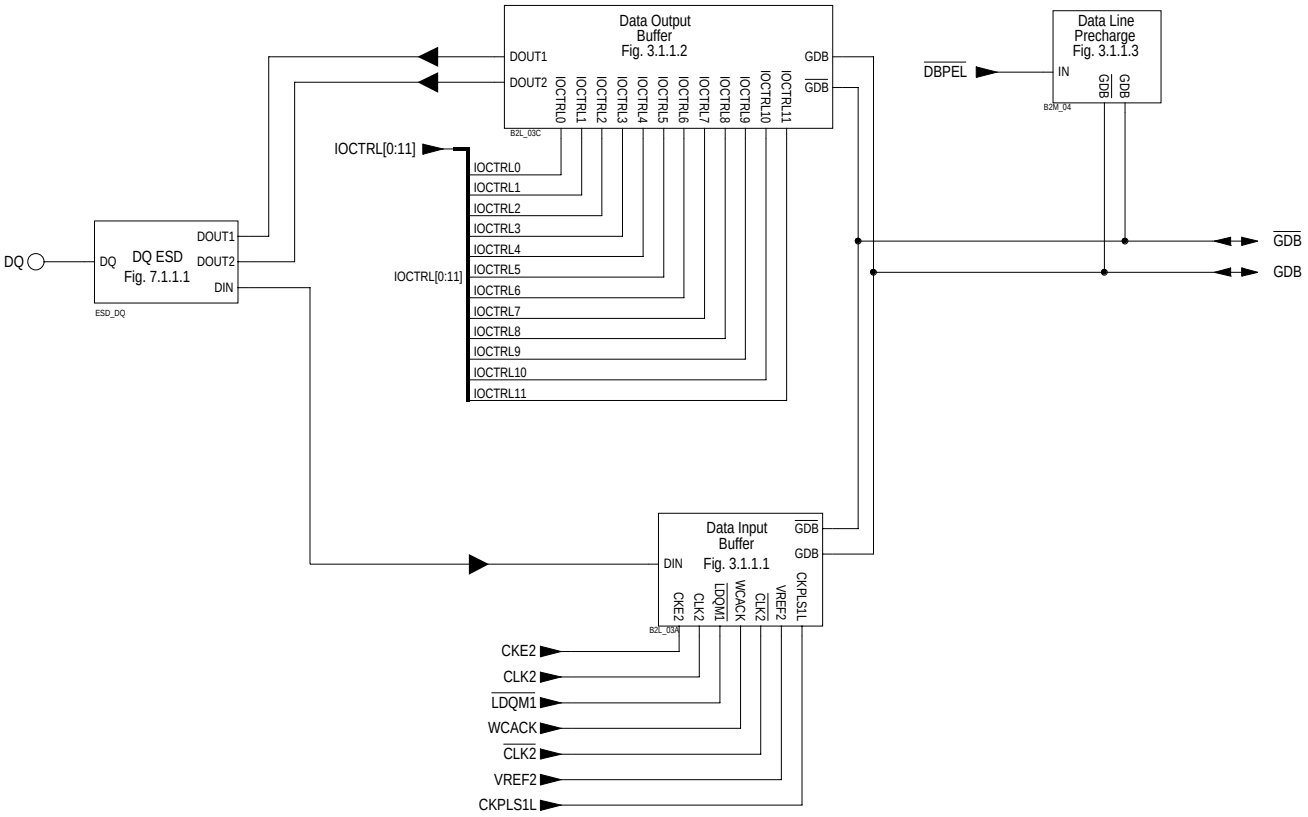


Figure 3.1.1 DATA INPUT/OUTPUT BUFFER AND LATCH

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	IOBUFFER	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:53		
LOCATION:	XXX	INITIALS:	AZ, LW

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

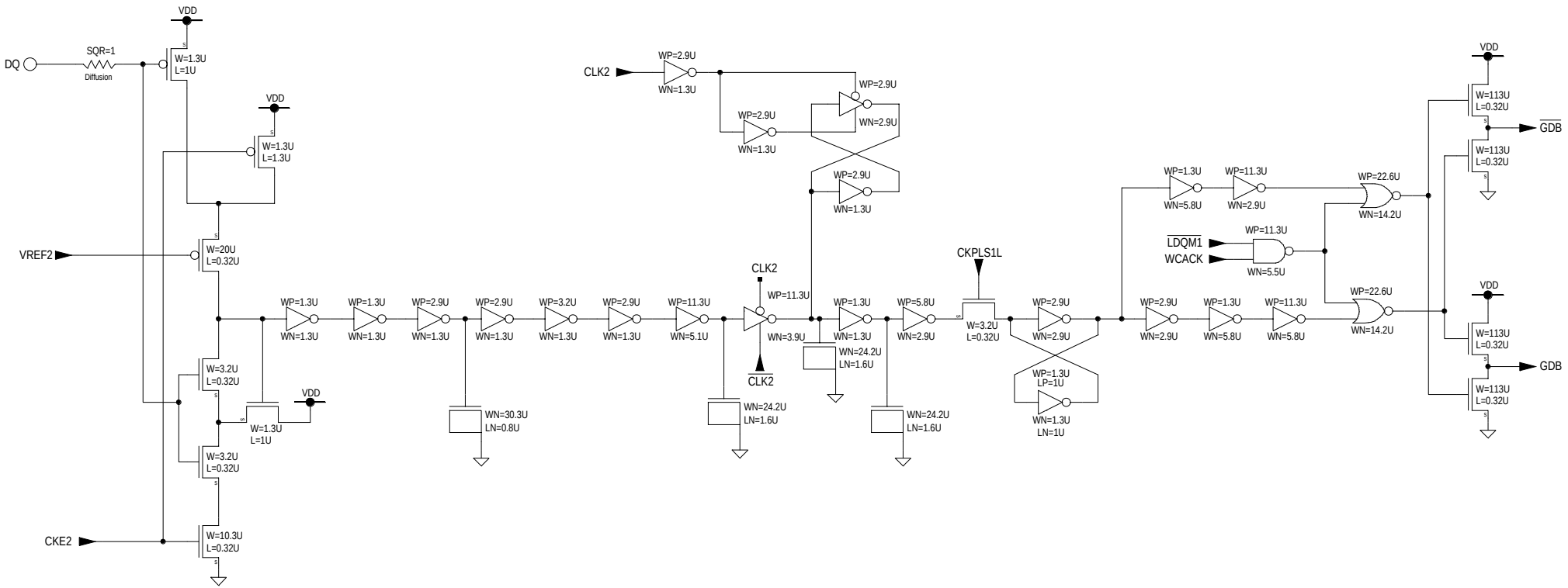
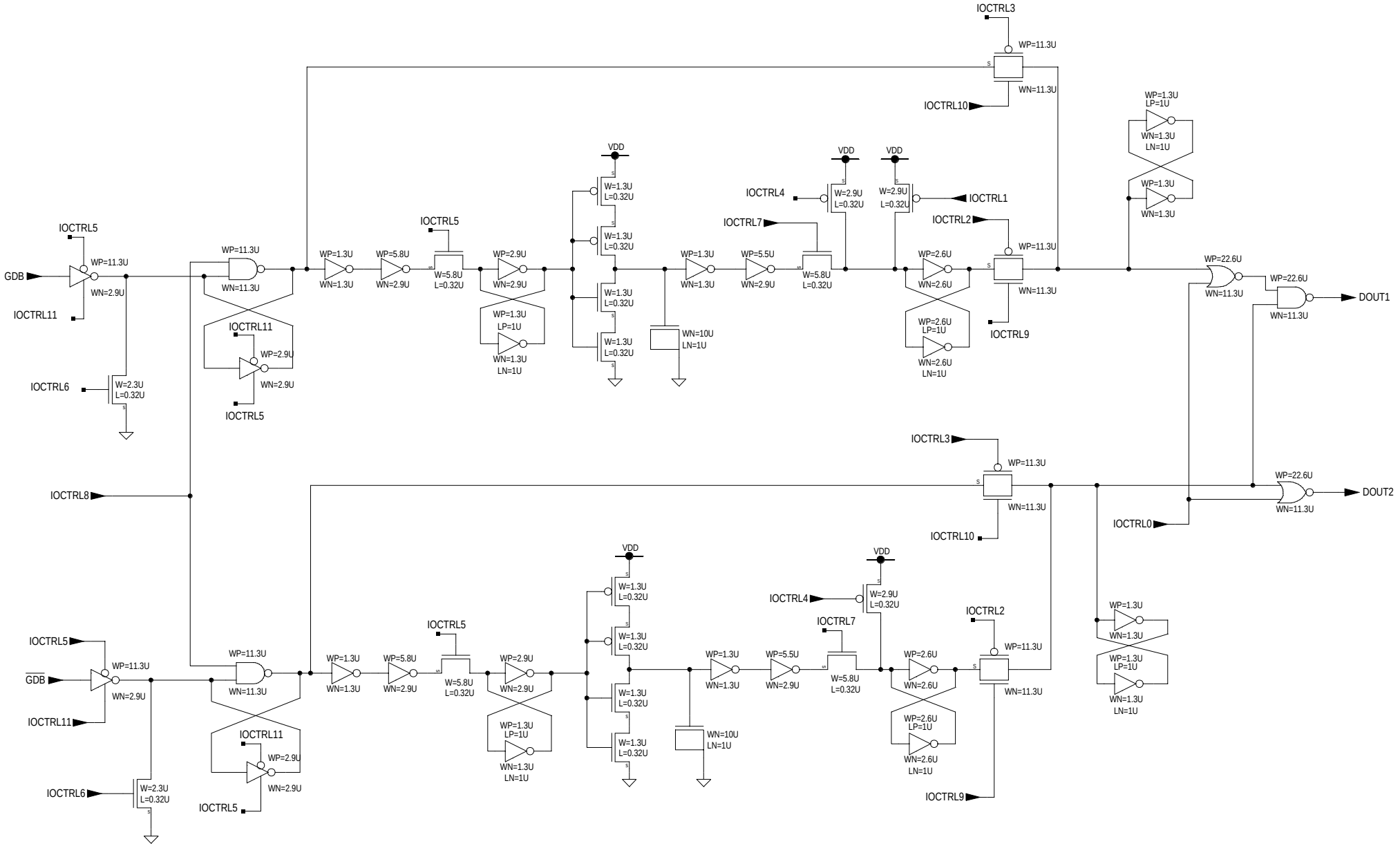


Figure 3.1.1.1 DATA INPUT BUFFER

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2L_03A	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:53		
LOCATION:	AREA C	INITIALS:	MW

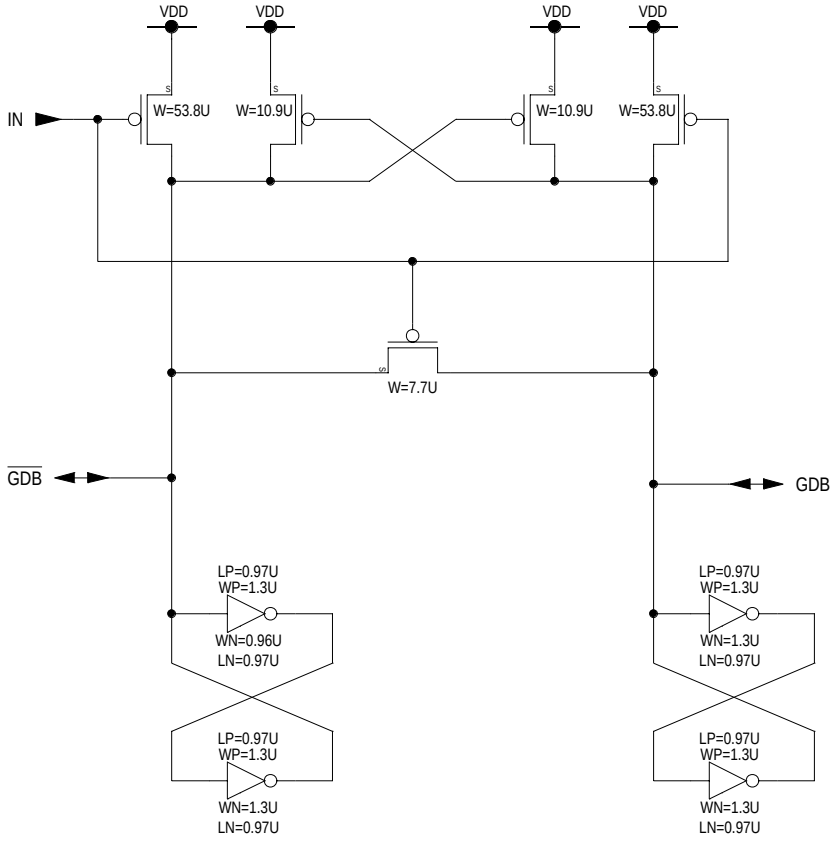
SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



PAGE 36

Figure 3.1.1.2 DATA OUTPUT BUFFER

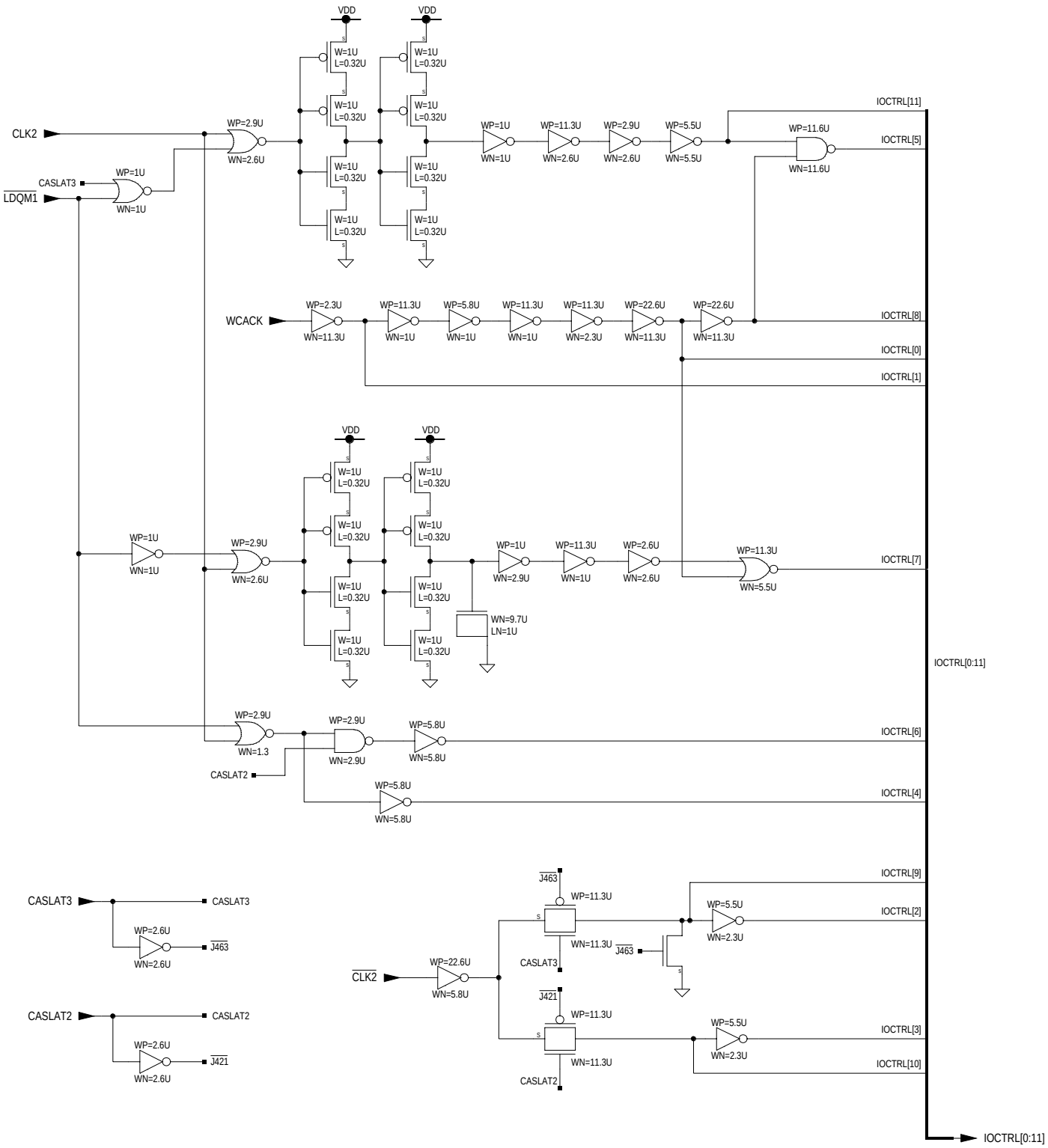
Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2L_03C	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:53		
LOCATION:	XXX	INITIALS:	AZ, LW



*LP is assumed to be 0.32 µm unless otherwise stated

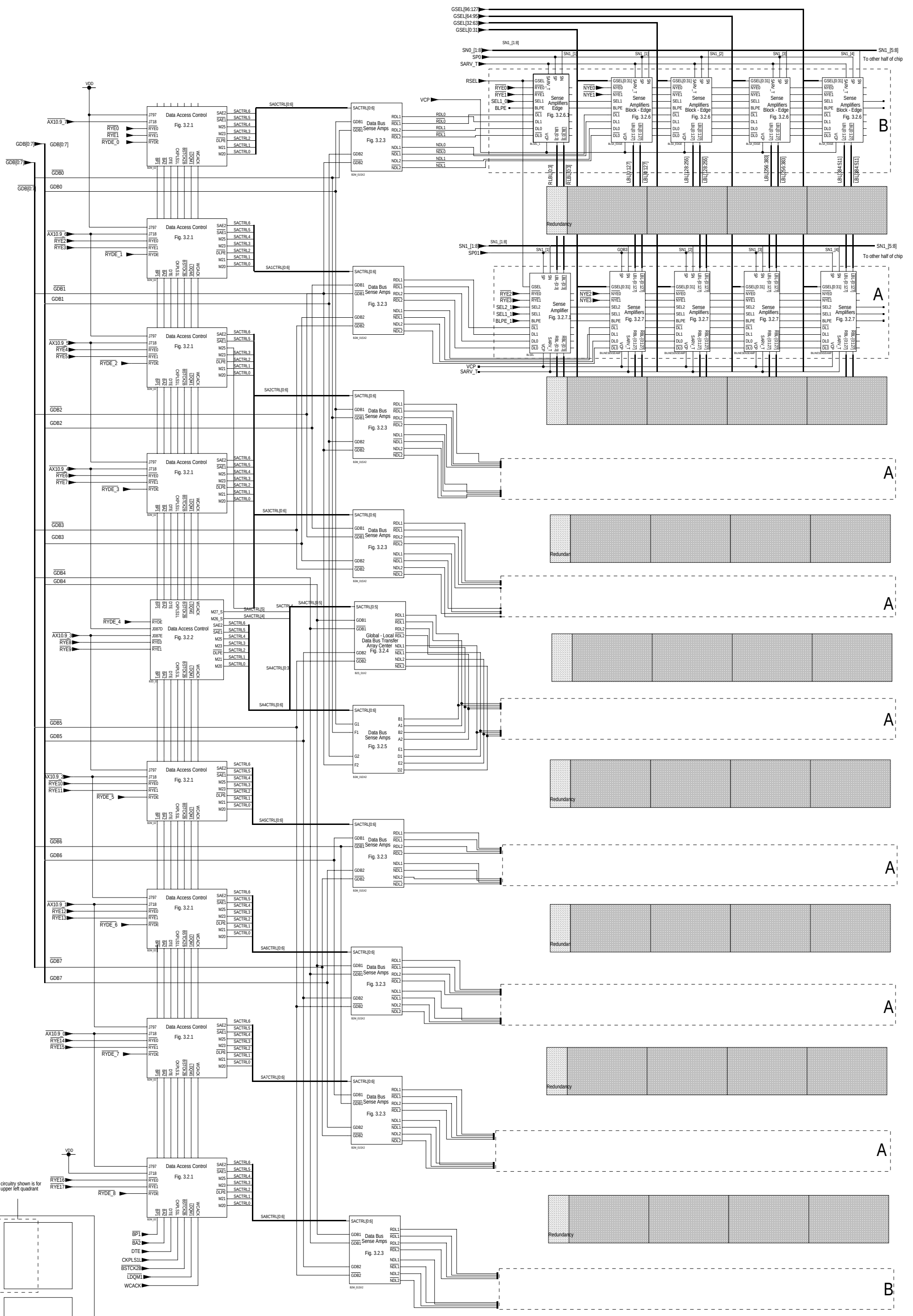
Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2M_04	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:53		
LOCATION:	AREA B2	INITIALS:	MW

Figure 3.1.1.3 DATA LINE PRECHARGE CIRCUITRY



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2L_03D	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:53		
LOCATION:	XXX	INITIALS:	AZ, LW

Figure 3.1.2 I/O CONTROL CIRCUITRY



PAGE 39

Figure 3.2 DATA PATH FOR ONE QUADRANT

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	DATAPATHQUAD	SI NUMBER:	SI01
DATE_TIME:	6-26-2002_10:40		
LOCATION:	AREA B2	INITIALS:	AZ, LW

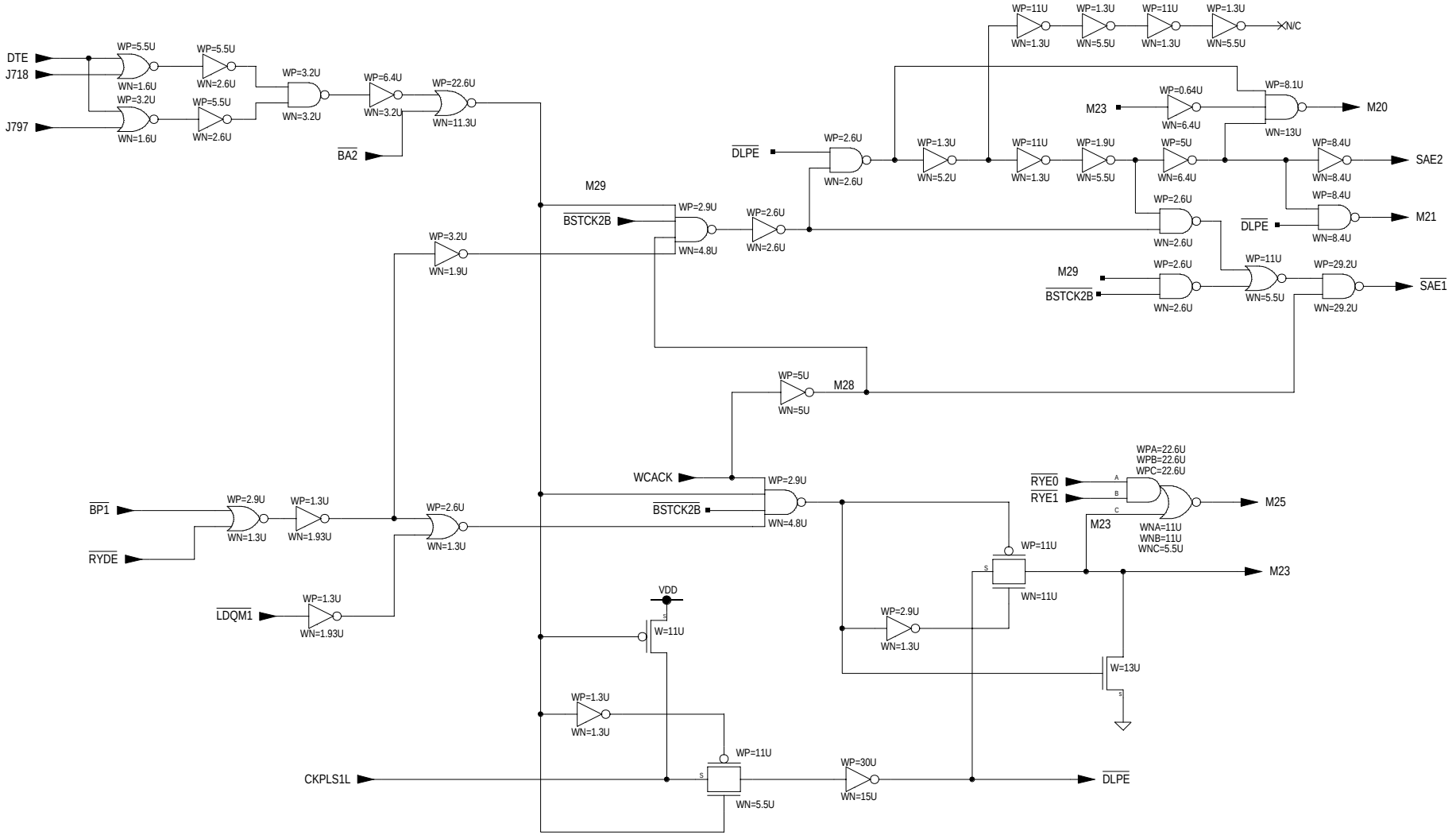


Figure 3.2.1 DATA ACCESS CONTROL

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2M_02	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:54		
LOCATION:	XXX	INITIALS:	AZ, LW

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

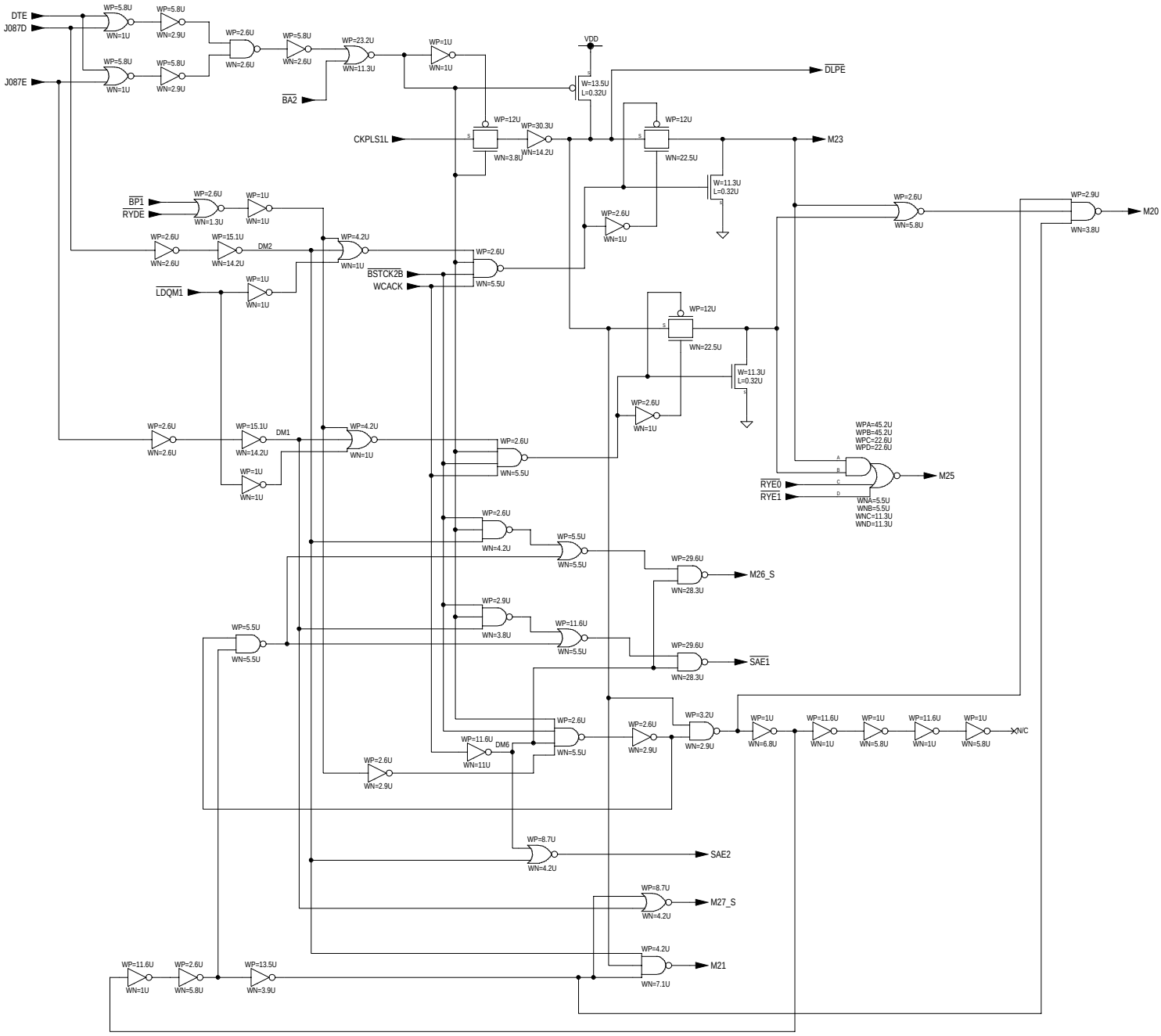


Figure 3.2.2 DATA ACCESS CONTROL

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2D_01	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:54		
LOCATION:	XXX	INITIALS:	DM

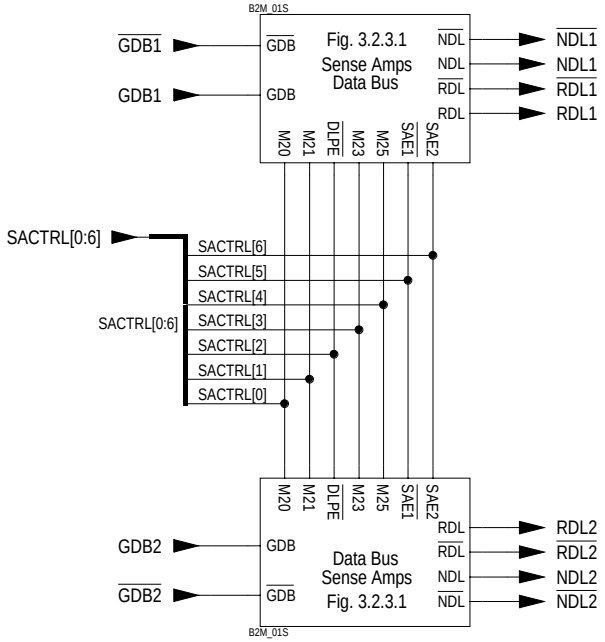
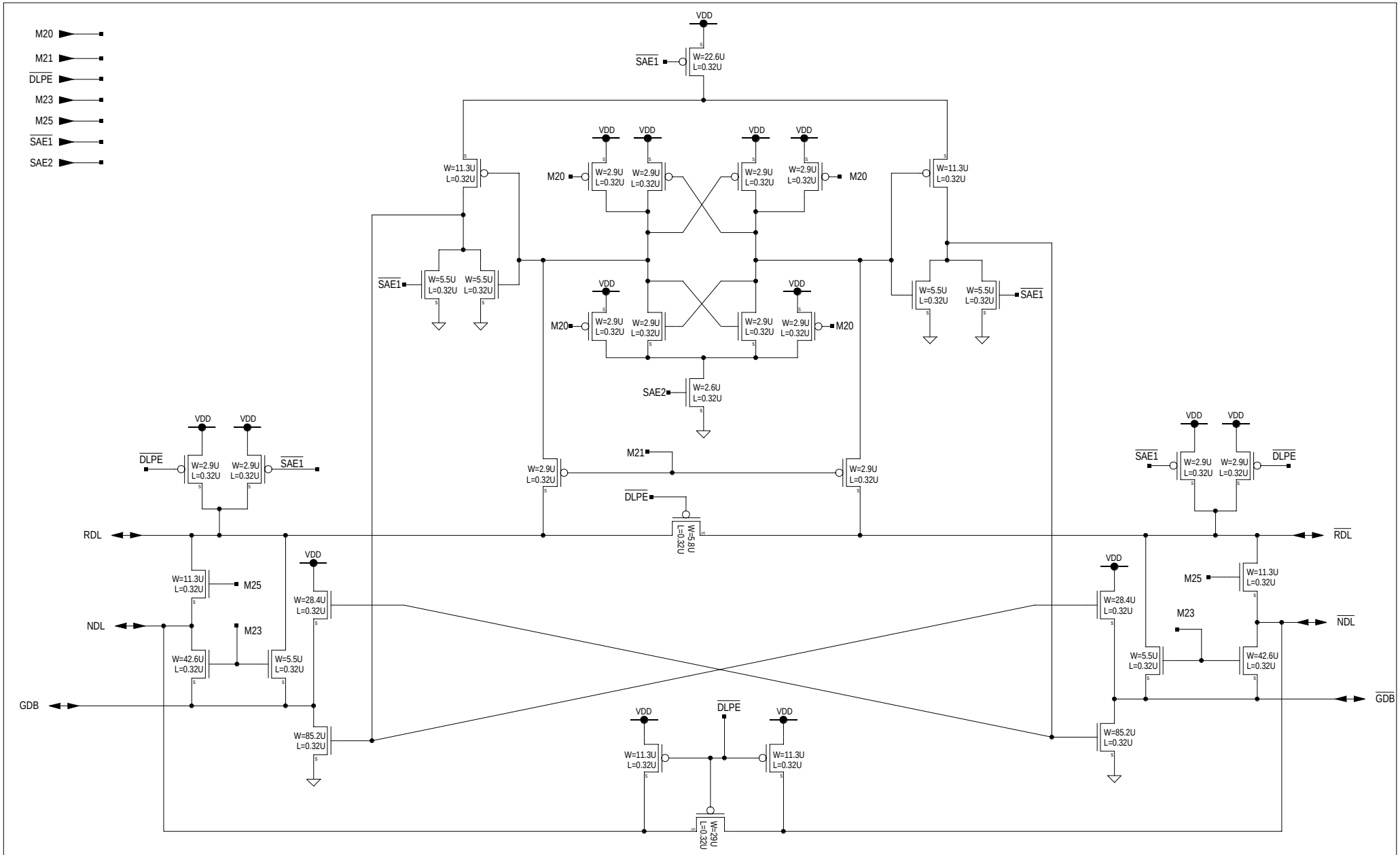


Figure 3.2.3 DATA BUS SENSE AMPLIFIERS TYPE 1

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2M_01SX2	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:55		
LOCATION:	AREA B2	INITIALS:	MW

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



PAGE 43

Figure 3.2.3.1 DATA BUS SENSE AMPLIFIERS

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2M_01S	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:55		
LOCATION:	AREA B2	INITIALS:	MW

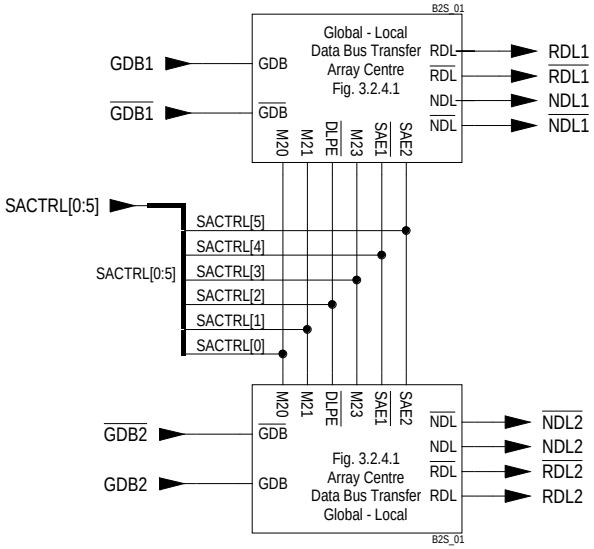


Figure 3.2.4 DATA BUS SENSE AMPLIFIERS TYPE 2

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2S_01X2	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:55		
LOCATION:	AREA B2	INITIALS:	MW

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

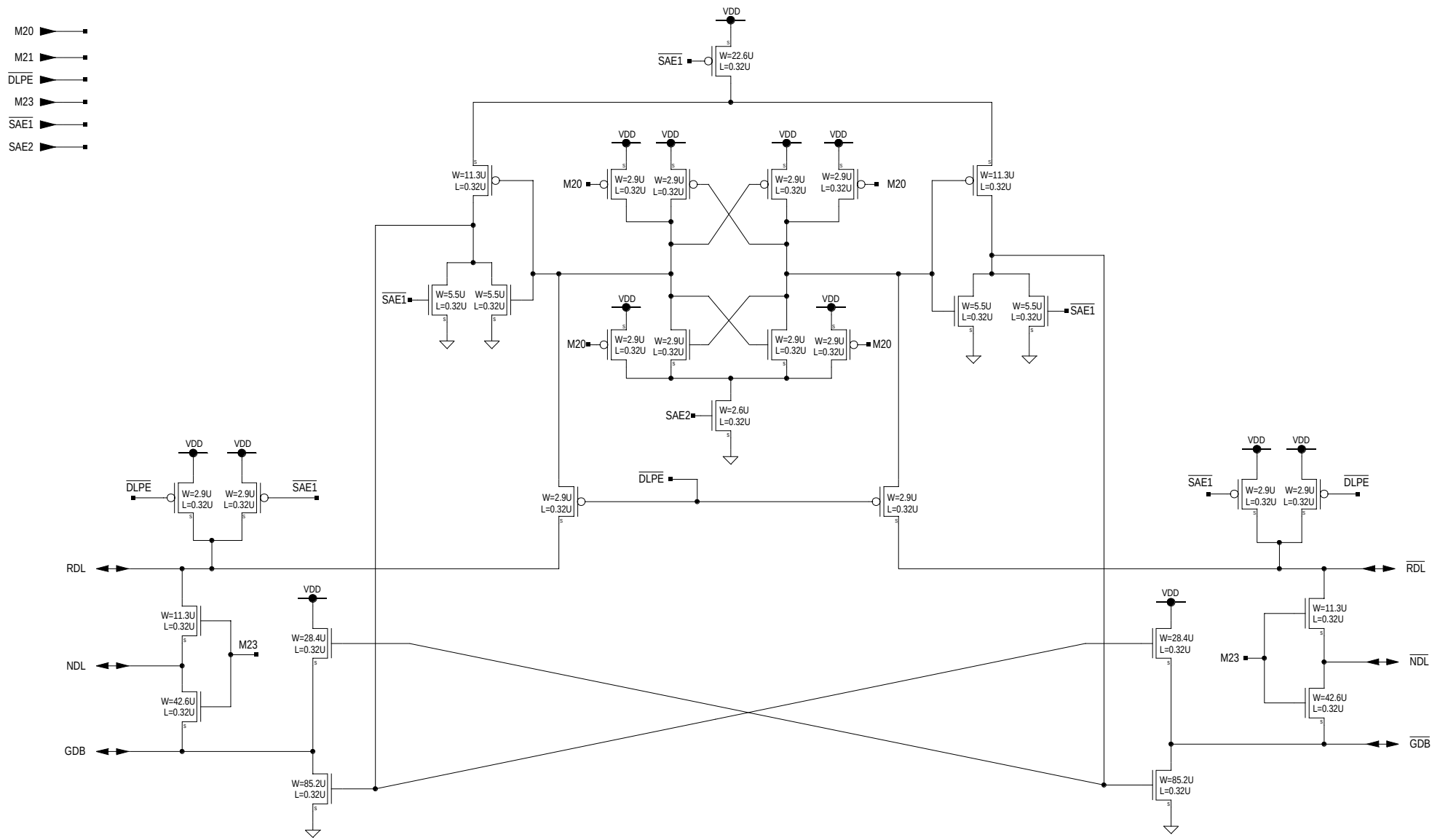


Figure 3.2.4.1 DATA BUS SENSE AMPLIFIERS

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2S_01	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:55		
LOCATION:	AREA B2	INITIALS:	MW

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

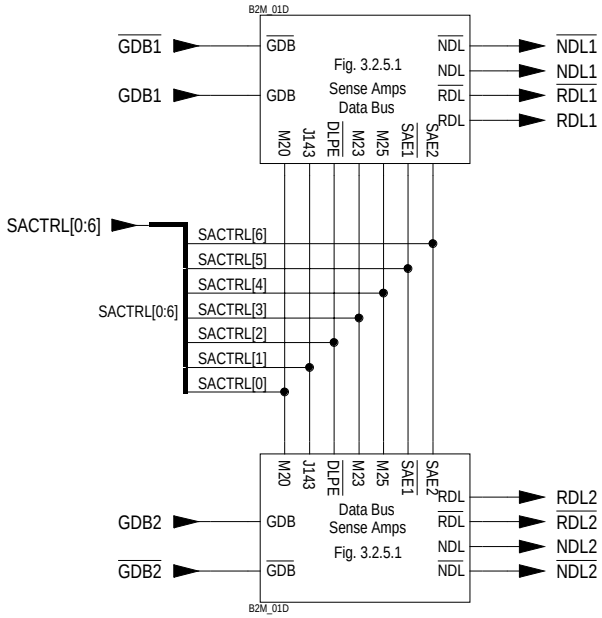
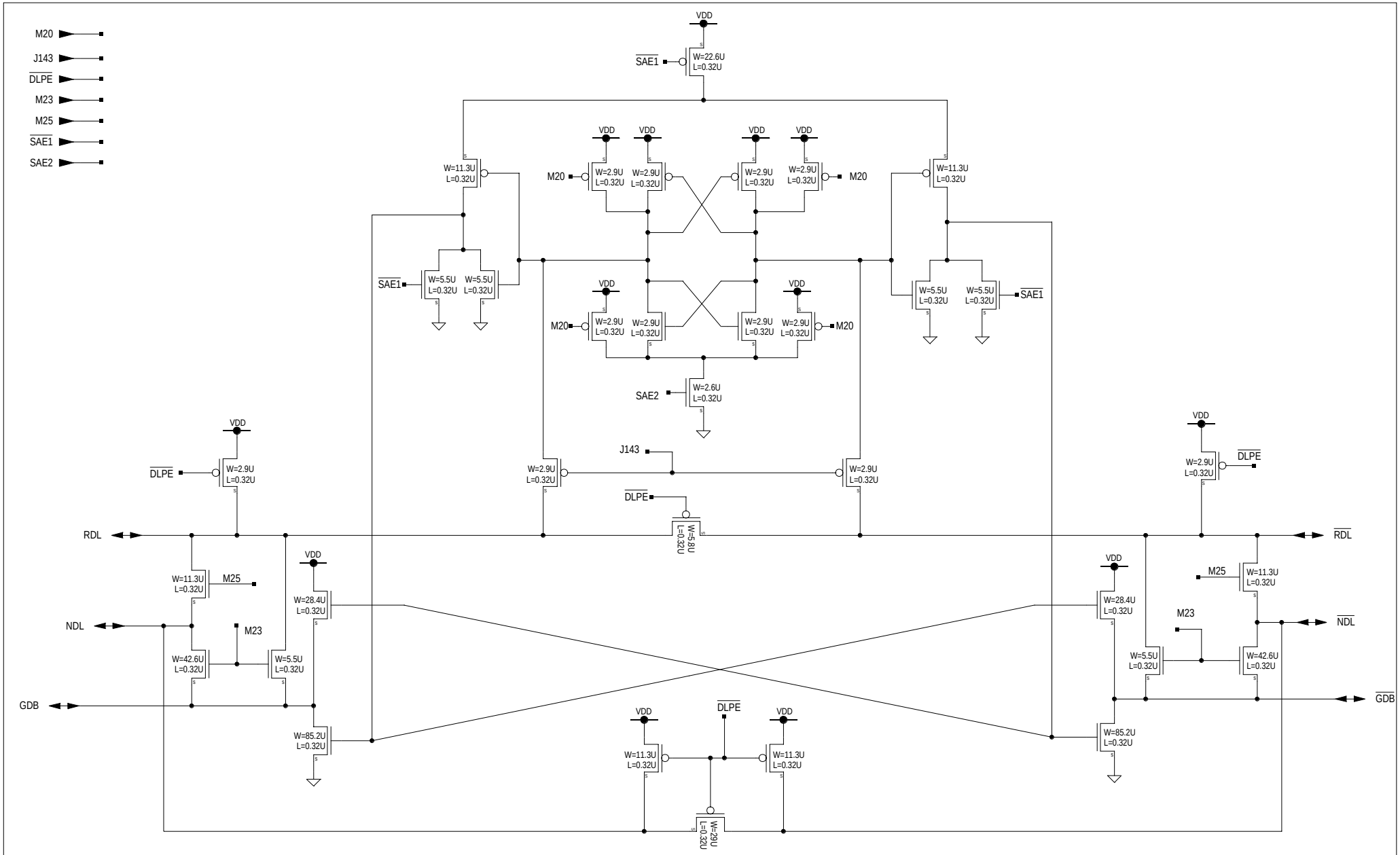


Figure 3.2.5 DATA BUS SENSE AMPLIFIERS TYPE 3

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2M_01DX2	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:55		
LOCATION:	AREA B2	INITIALS:	MW



PAGE 47

Figure 3.2.5.1 DATA BUS SENSE AMPLIFIERS

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2M_01D	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:55		
LOCATION:	AREA B2	INITIALS:	MW

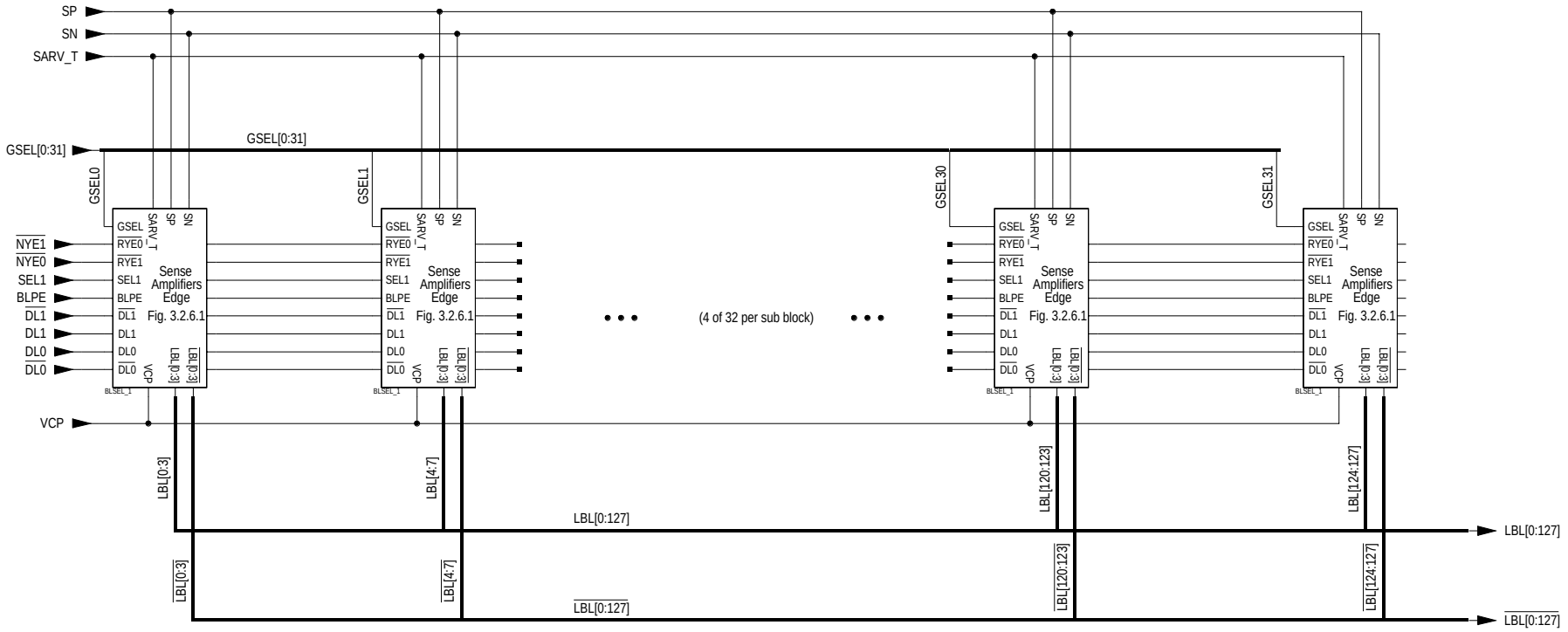


Figure 3.2.6 SENSE AMPLIFIER

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	BLSA_EDGE	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:55		
LOCATION:	XXX	INITIALS:	AZ, LW

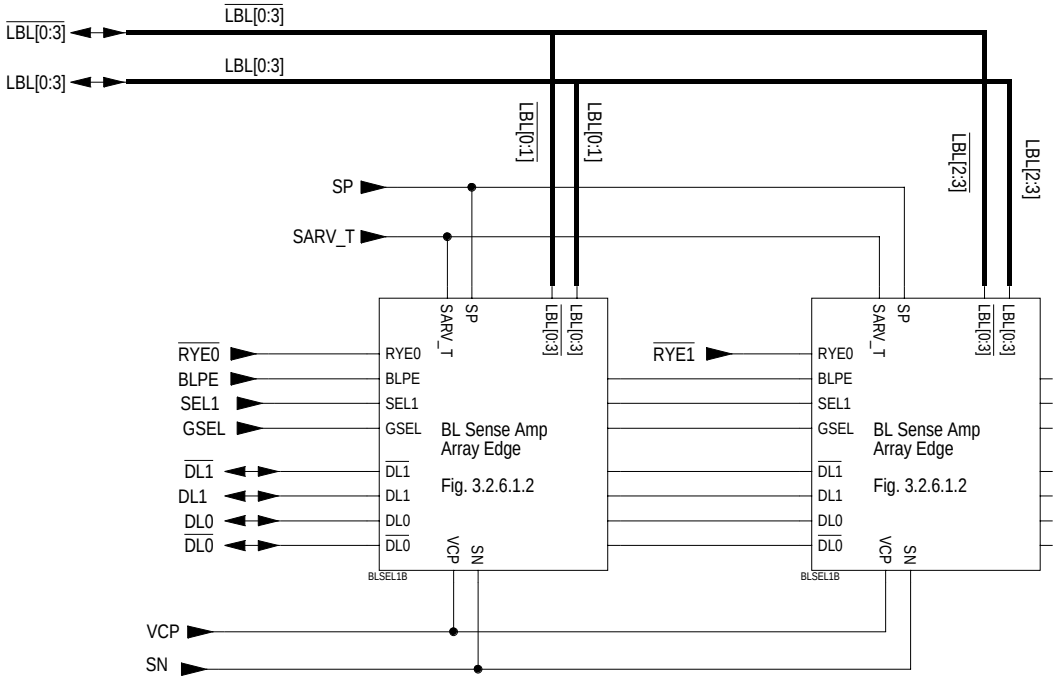
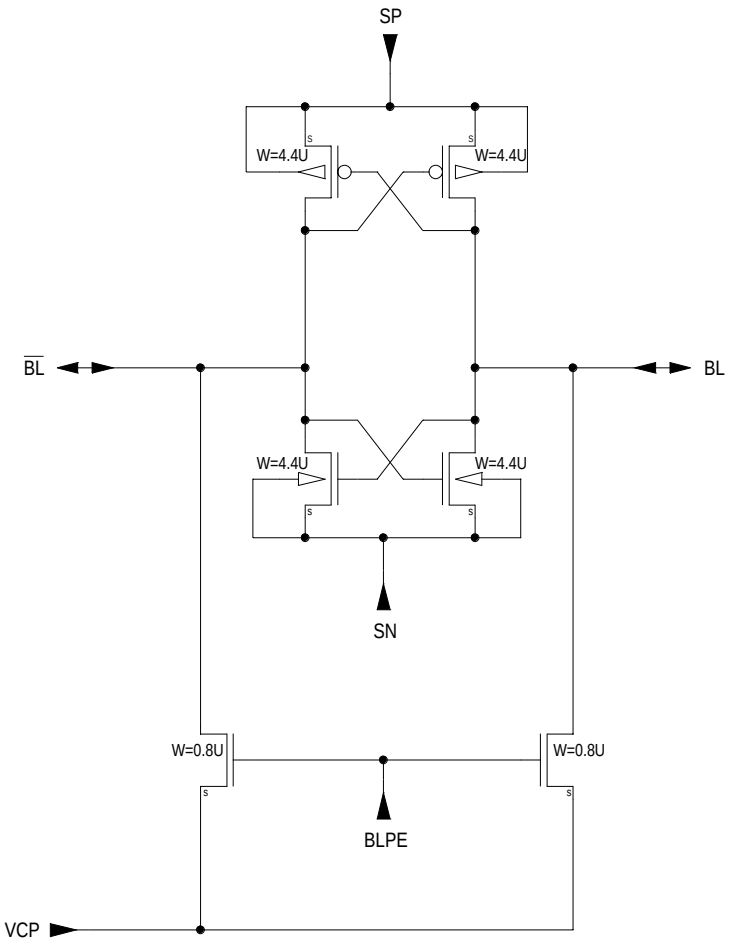


Figure 3.2.6.1 SENSE AMPLIFIERS/ BITLINE SELECTION EDGE OF MEMORY ARRAY

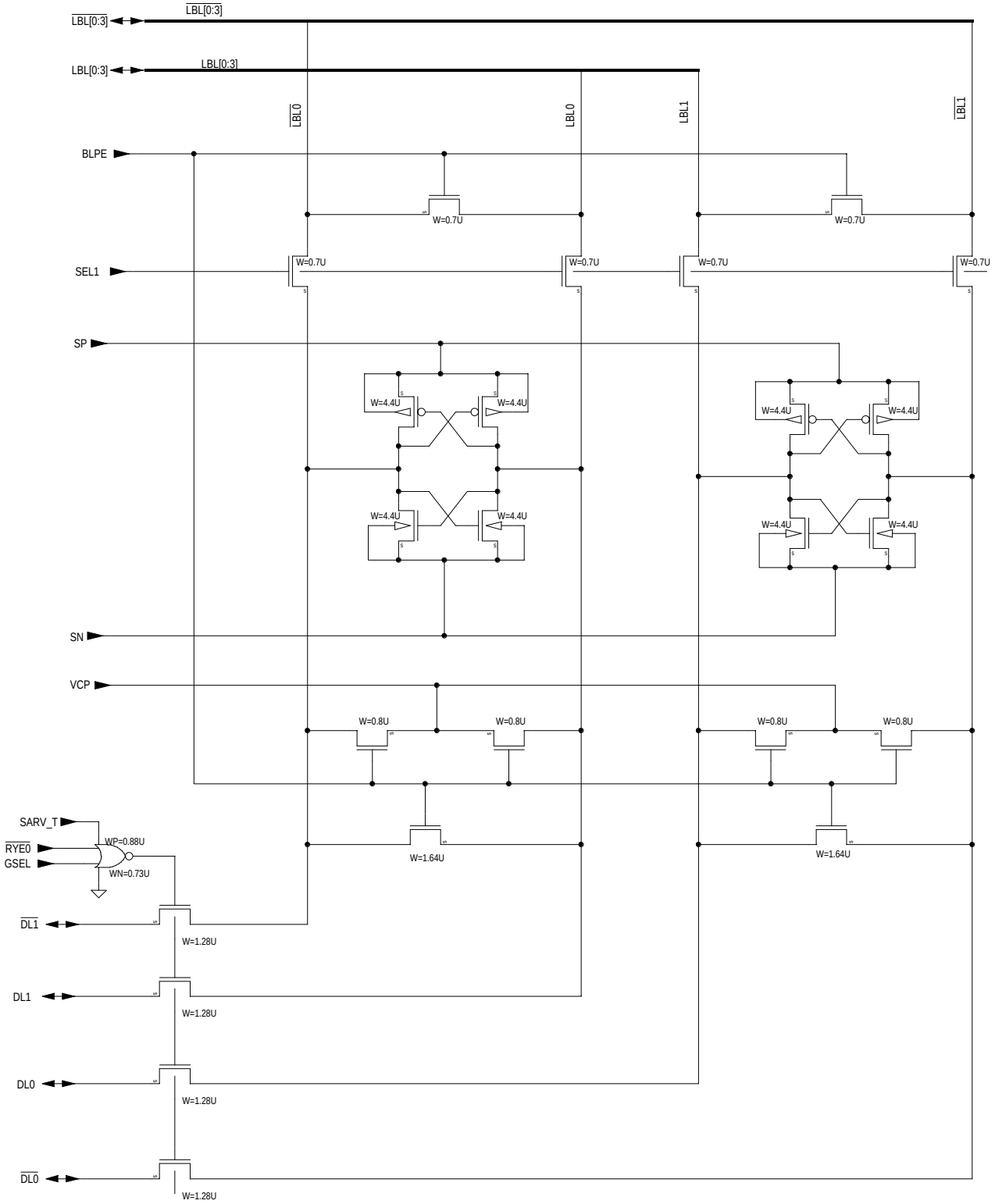
SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	BLSEL_1	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:55		
LOCATION:	XXX	INITIALS:	XX



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	BLSENSEAMPS	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:56		
LOCATION:	XXX	INITIALS:	AZ, LW

Figure 3.2.6.1.1 SENSE AMPLIFIER



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	BLSEL1B	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:56		
LOCATION:	XXX	INITIALS:	XX

Figure 3.2.6.1.2 BIT LINE SENSE AMP ARRAY EDGE

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

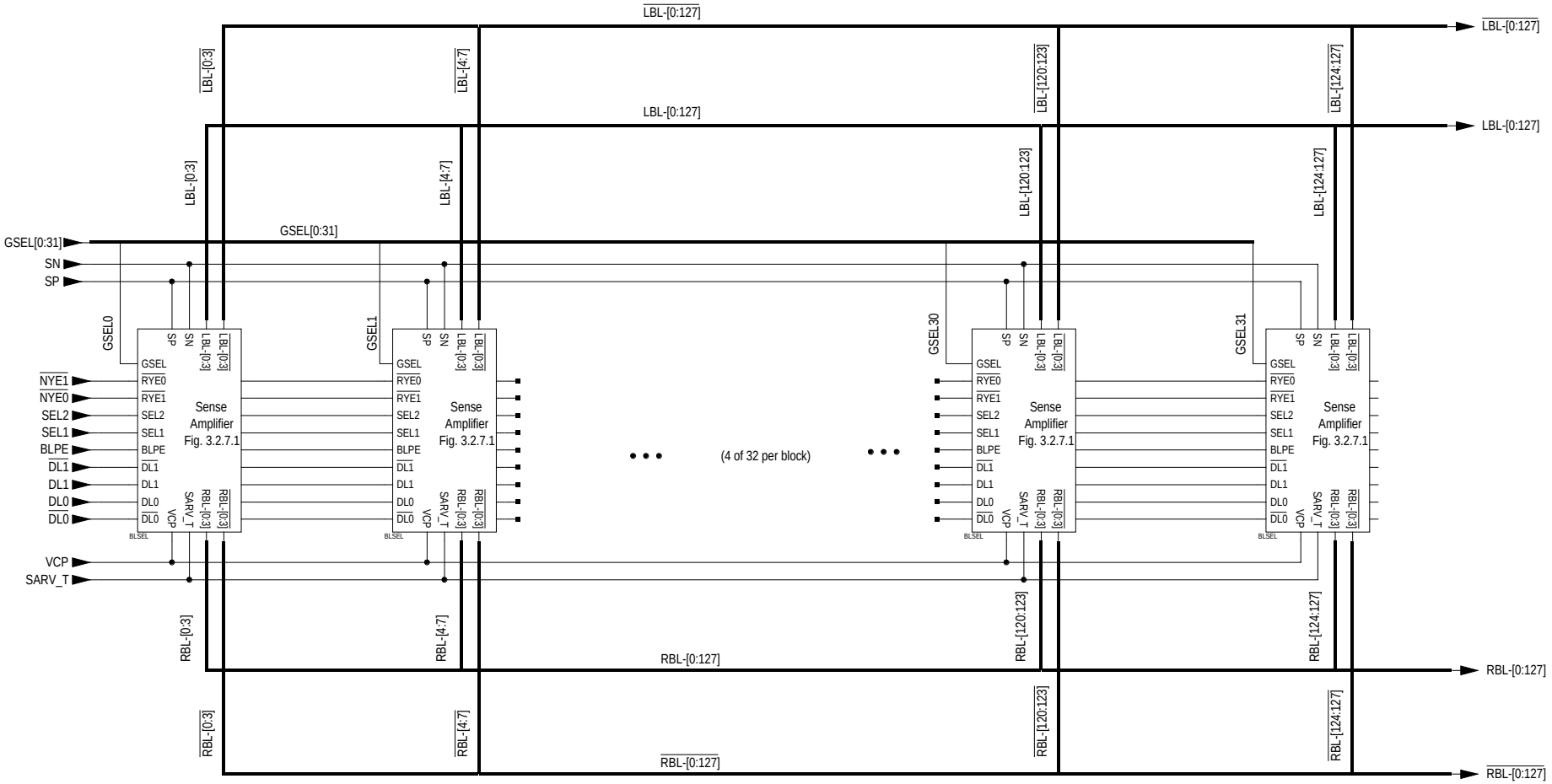


Figure 3.2.7 SENSE AMPLIFIER

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	BILINESENSEAMP	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:56		
LOCATION:	XXX	INITIALS:	AZ, LW

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

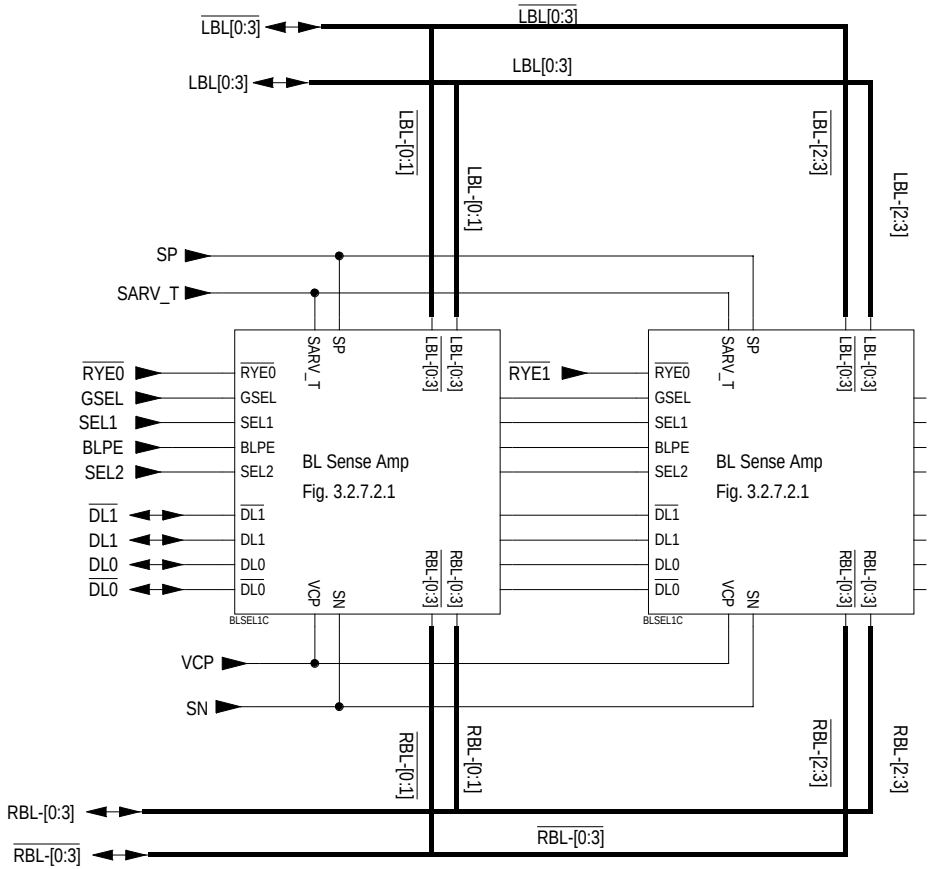


Figure 3.2.7.1 SENSE AMPLIFIERS/ BITLINE SELECTION

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	BLSEL	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:56		
LOCATION:	XXX	INITIALS:	AZ, LW

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

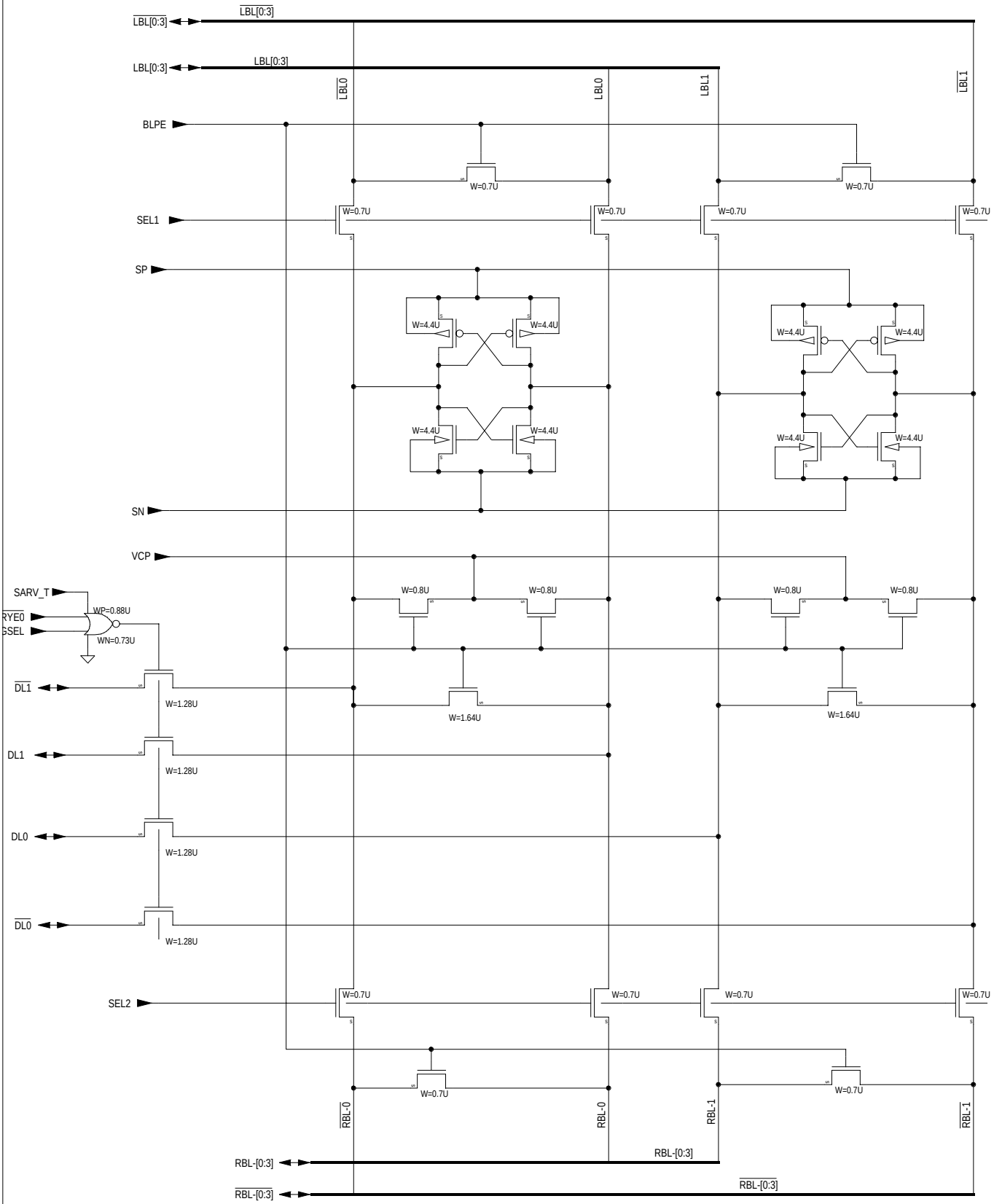
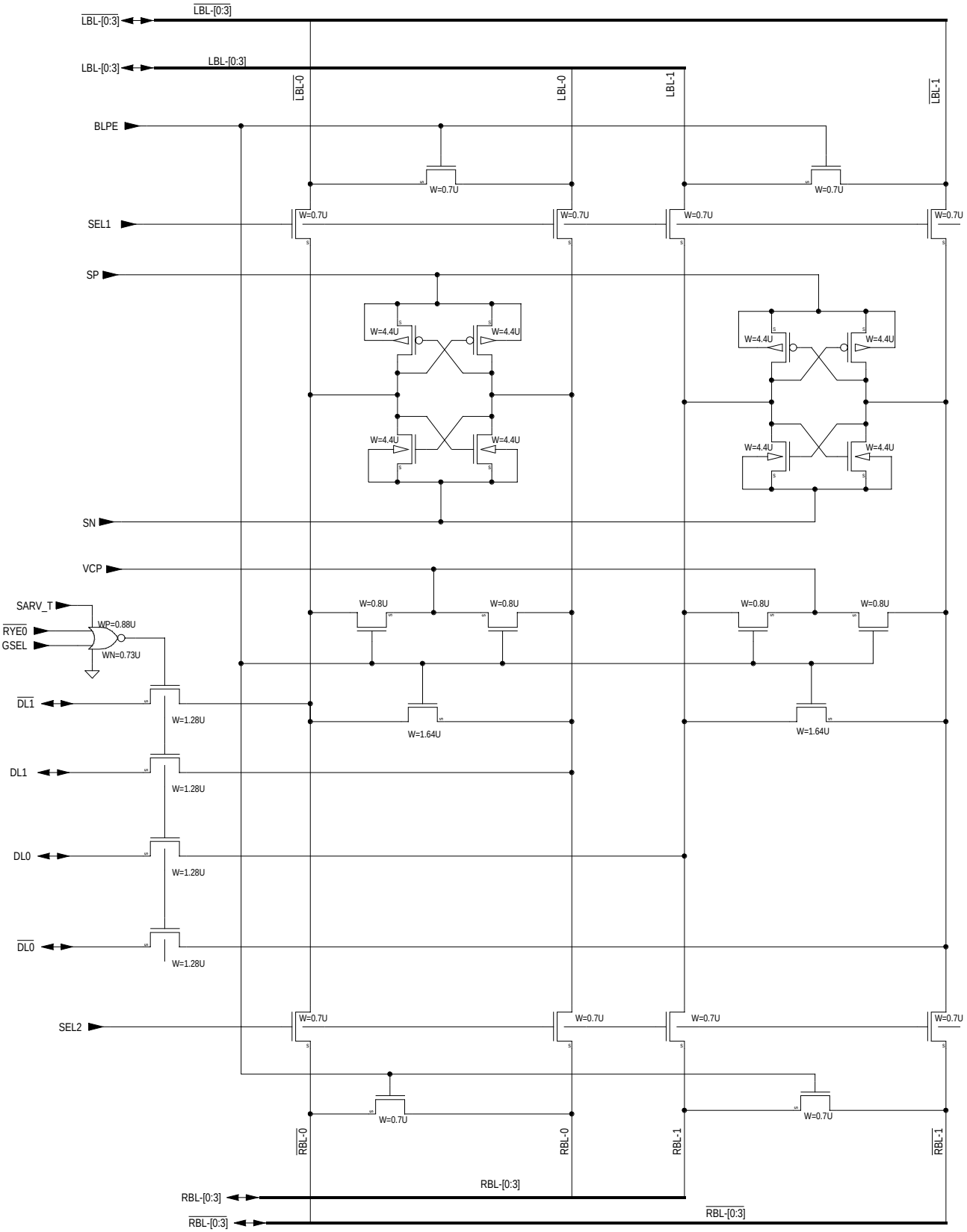


Figure 3.2.7.2 SENSE AMPLIFIERS/ BITLINE SELECTION

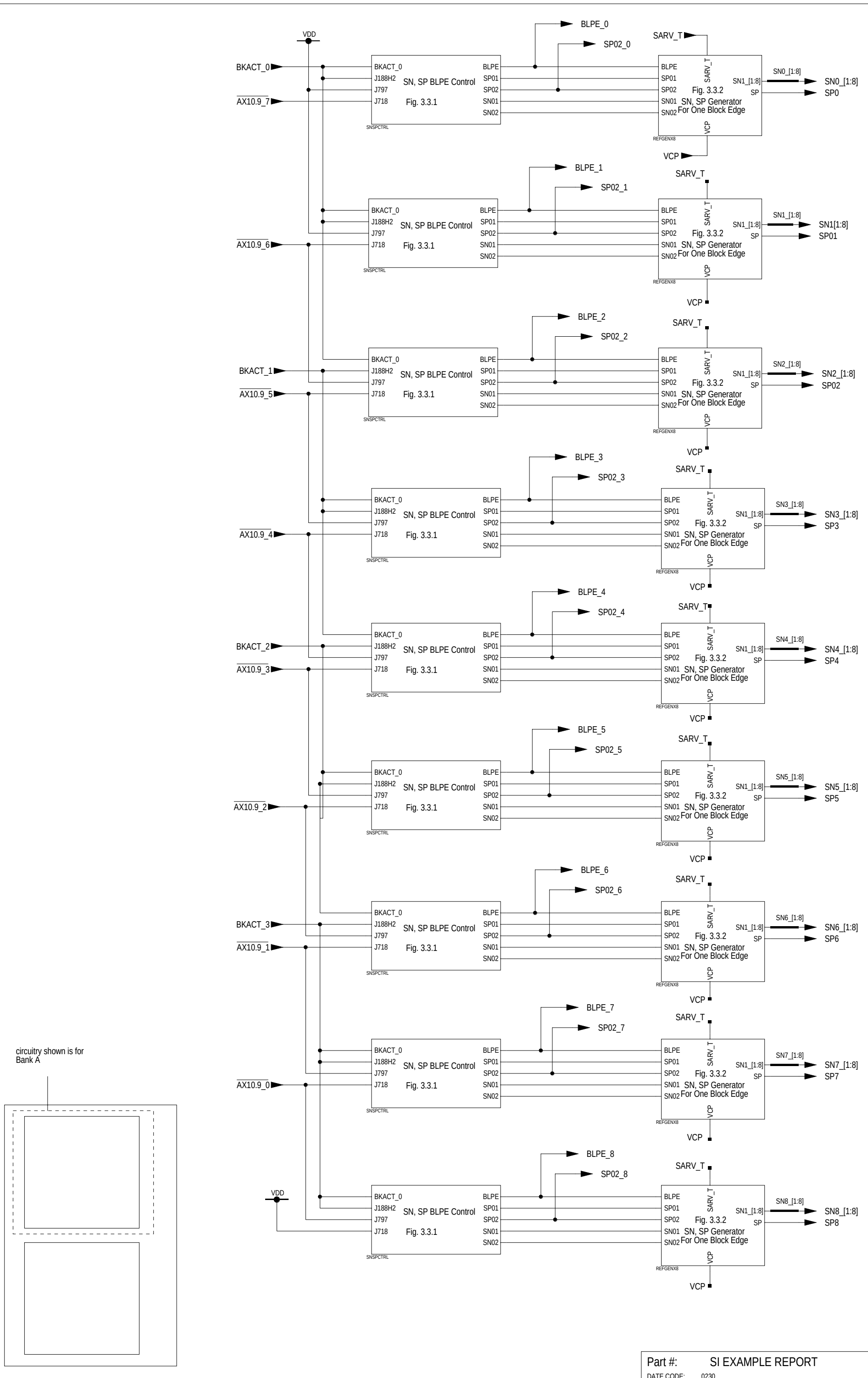
Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	BILINESENSEAMP1	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:57		
LOCATION:	XXX	INITIALS:	AZ, LW

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	BLSEL1C	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:57		
LOCATION:	XXX	INITIALS:	AZ, LW

Figure 3.2.7.2.1 BIT LINE SENSE AMP



circuitry shown is for
Bank A

Figure 3.3 DATA PATH CONTROL FOR BANK A

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	DATAPATHCTRL	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_12:21		
LOCATION:	AREA B2	INITIALS:	AZ, LW

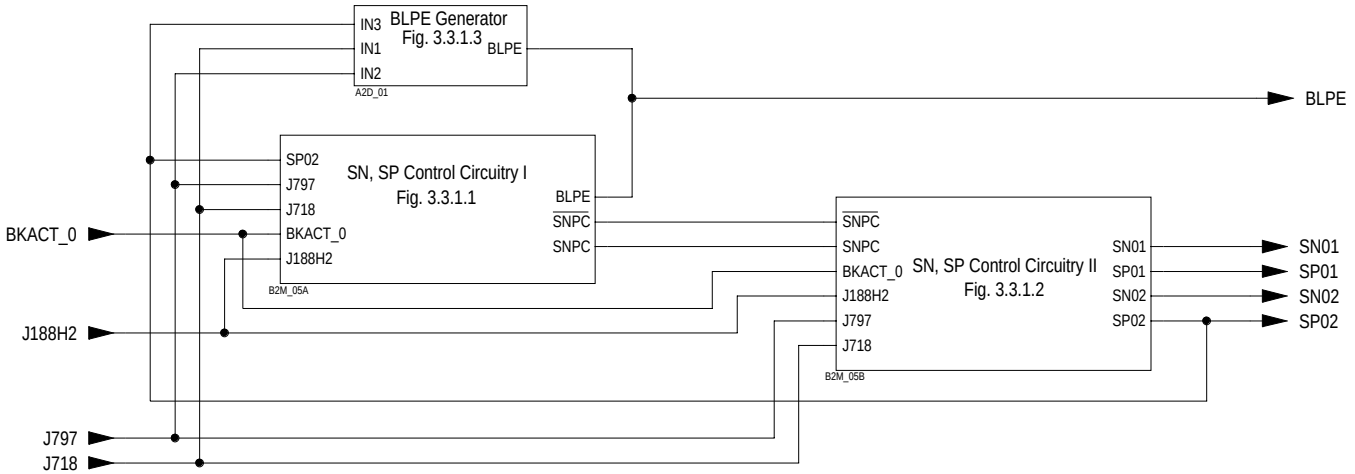
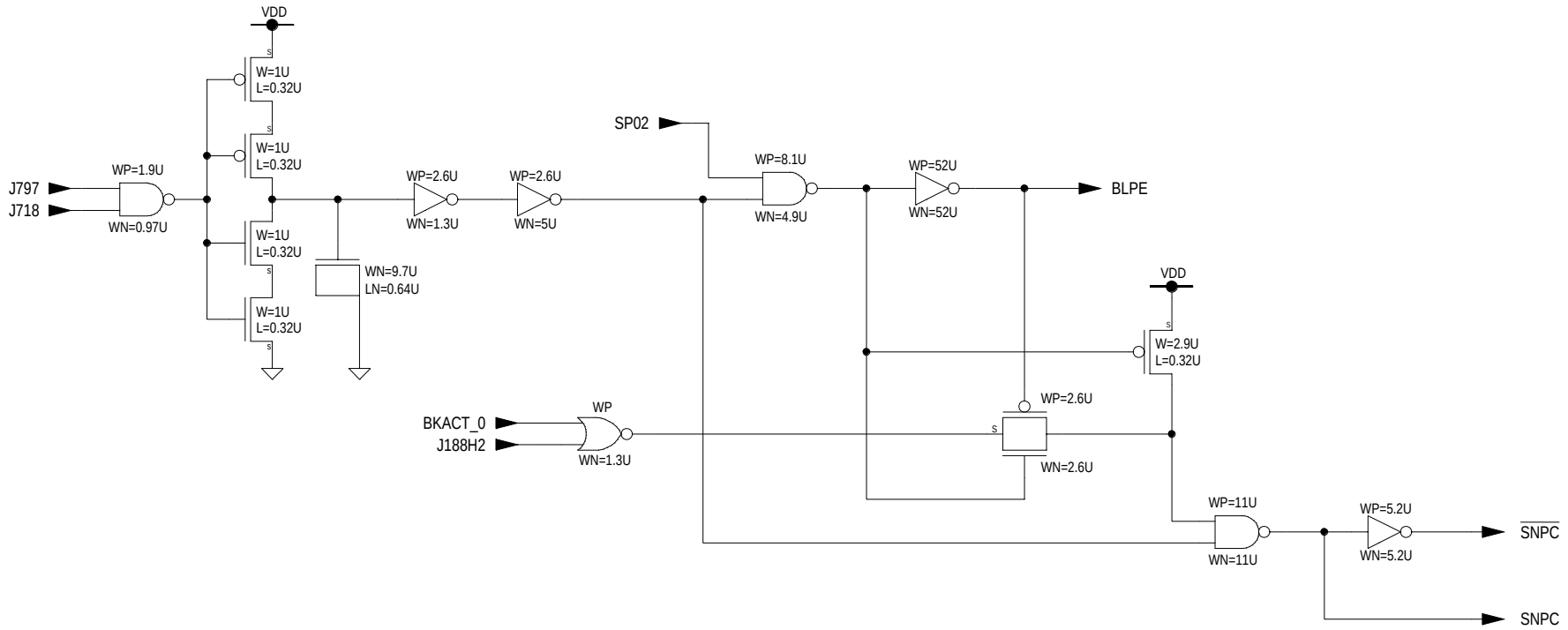


Figure 3.3.1 SN, SP CONTROL BLOCK

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

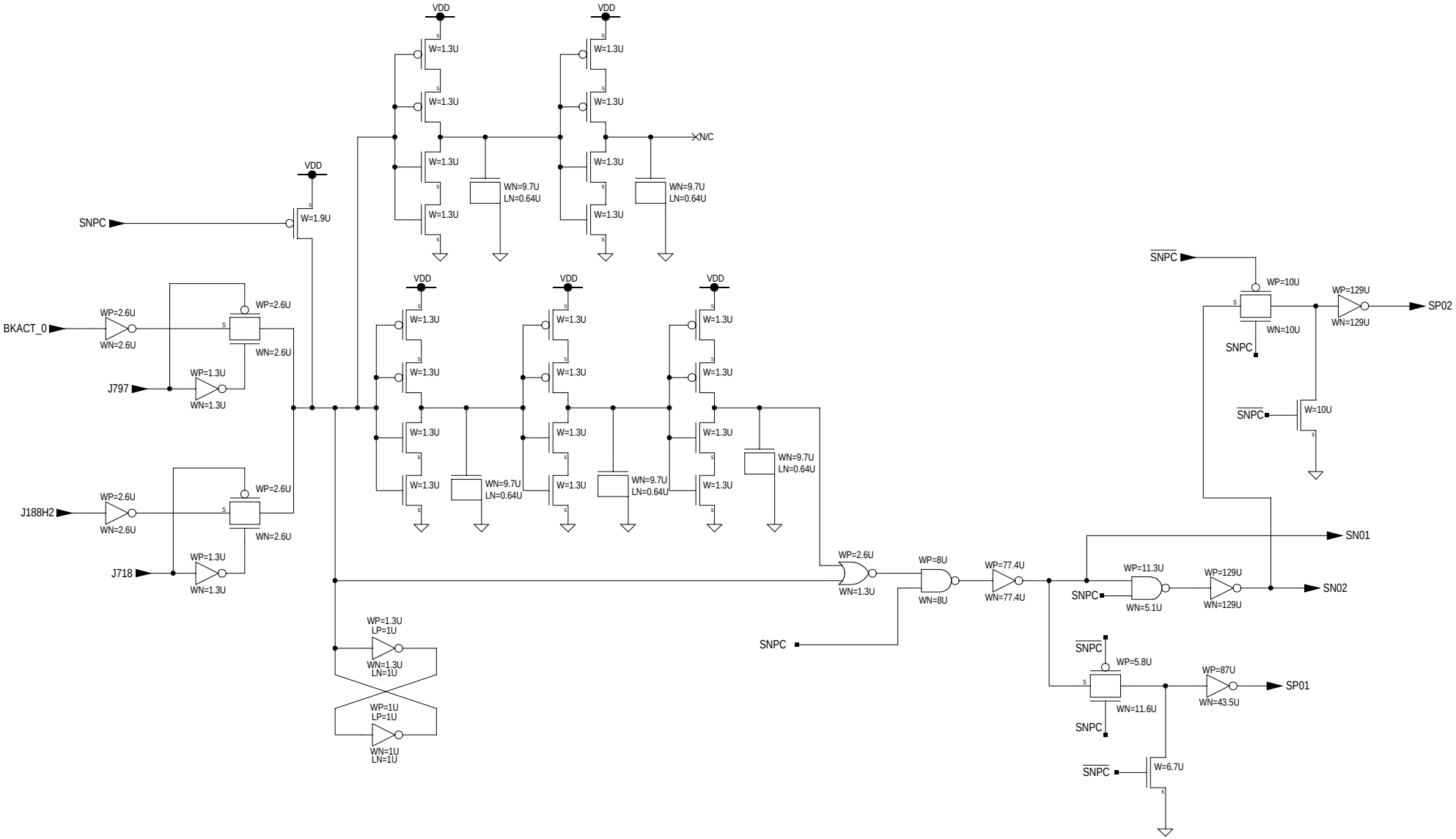
Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	SNSPCTRL	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:57		
LOCATION:	XXX	INITIALS:	AZ, LW



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2M_05A	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:58		
LOCATION:	XXX	INITIALS:	AZ, LW

Figure 3.3.1.1 SN, SP CONTROL CIRCUITRY I

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2M_05B	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:58		
LOCATION:	XXX	INITIALS:	AZ, LW

Figure 3.3.1.2 SN, SP CONTROL CIRCUITRY II

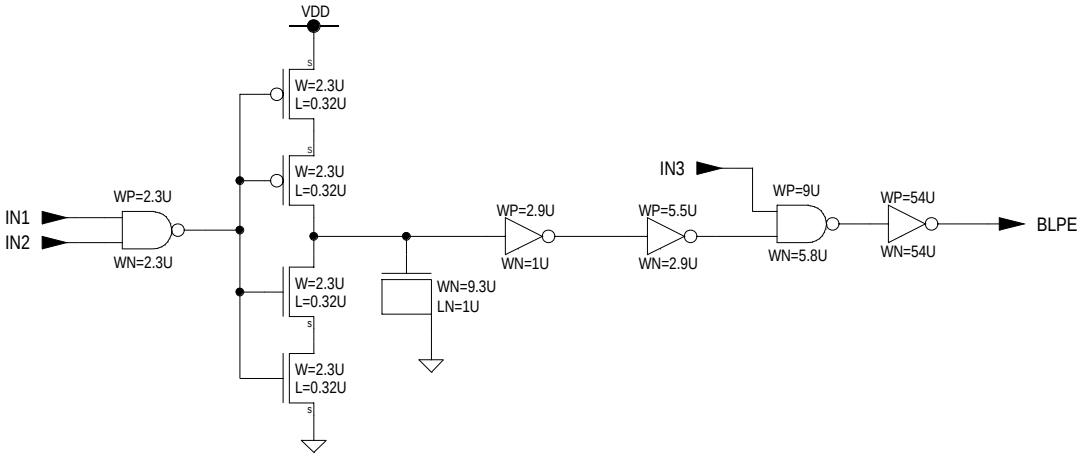
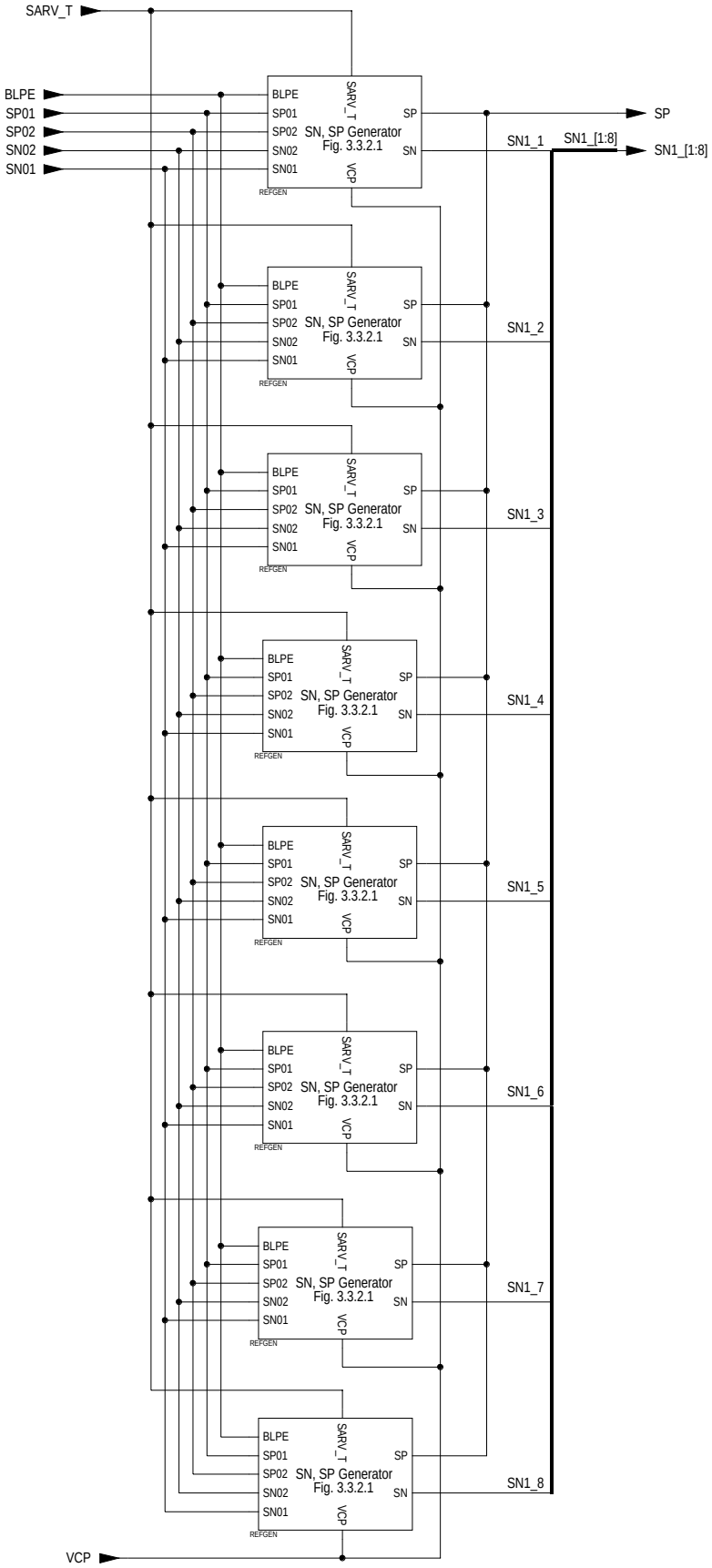


Figure 3.3.1.3 BLPE GENERATOR

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	A2D_01	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:58		
LOCATION:	XXX	INITIALS:	DM



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	REFGENX8	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:58		
LOCATION:	XXX	INITIALS:	AZ, LW

Figure 3.3.2 SN, SP GENERATION FOR ONE BLOCK EDGE

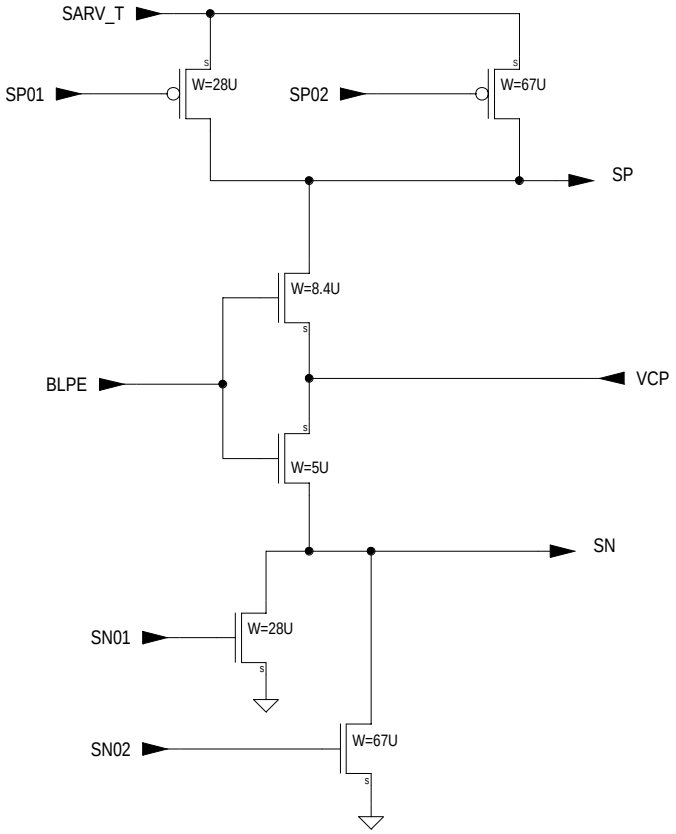


Figure 3.3.2.1 SN AND SP GENERATOR

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	REFGEN	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_8:58		
LOCATION:	XXX	INITIALS:	AZ, LW

4.0 Address Path

The following section was taken from a report on a Flash device. This section is headed by a top-level diagram (Figure 4.0). The layout of this schematic has been constructed to illustrate the rough layout of the circuitry extracted. There is also a page-by-page signal list present in this section.

Note: The page-by-page signal list was taken directly from the original report and therefore the figure numbers are not valid for this document.

4.1 Basic Operation

The two Flash banks found on the device are very similar and the address circuitry for one Flash bank is shown in Figure 4. The circuitry for this schematic is located on the left hand side of a bank of Flash cells. The address circuitry has a unique feature that may help in decreasing the access time for the memory. The feature involves the use of two wordline drivers and will be discussed in more detail below.

The address circuitry is controlled by two buses, a column address bus (AY[0:4]) and a row address bus (AX[0:10]). There may be other address signals but these were the only signals that could be identified with certainty based on the partial nature of the analysis. Both of these sets of address signals are buffered and driven into decoding circuitry. The decoding circuitry contains latches that are controlled by one of two address clocks. The latched decoded addresses are used to select one of thirty-two global bitlines or select one of 2 K wordlines in a normal read or program operation.

4.2 Two-Way Wordline Drivers

The unique feature of the address path is the presence of two wordline drivers. One wordline driver is used for normal read operations while the other is used for program/erase operations (Figure 4.13.7). The normal read address path uses the same addresses as the program path but the wordline driver is constructed of low voltage, high performance transistors. The low voltage wordline driver can be isolated from the wordline via a high voltage pass transistor. The isolation device is necessary because of the high voltages used during program and erase operations. Each wordline driver arrangement has some of its own address decoding circuitry. The address path for programming operations consists of a set of level shifters (Figure 4.11) and a tri-stateable wordline driver. The majority of transistors used in the programming path are high voltage low performance transistors. These transistors must be used in this path because of the high voltages used during program and erase. The two sets of wordline drivers improve the performance of the memory because the normal read operation uses high performance

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

transistors. Therefore the normal transistor wordline driver is faster than the high voltage wordline driver. However the high voltage wordline driver is necessary because the cell must still be programmed and erased using voltages that the normal transistor would not be able to stand.

The erase operation is accomplished with the aid of the erase block select (EBS[0:11]) signals. These signals select one of the blocks of Flash arrays described in Section 2 and in conjunction with some source line circuitry (not presented in this report) erase a block of cells. It appears that the wordline driver arrangement can also support a single wordline erase but more analysis is necessary to support this statement.

Figure 4.0 – ADDRESS PATH

Signal ID	Source	Destination
512EN		3
ADCK1		3; 6.1
ADCK2		3
ADLR1	3	6.1
ADLR2	3	
AX[0:10]	BUS	3; 3
AX[0:10]	BUS	3; 3
AY[0:4]	BUS	3; 3
AY[0:4]	BUS	3; 3
BAX[0:4]	BUS	3
BAX[0:4]~	BUS	3
BAX[6:10]	BUS	3
BAX[6:10]~	BUS	3
BAY[0:3]	BUS	3
BAY[0:3]~	BUS	3
BBES		3
BBLBLIO L	3	
BBLBLIOJJ	3	
BBLBLI1_L	3	
BBLBLI1 U	3	
BBWL[0:15]	3	
BBWL[16:31]	3	
DAXO-4 [0:31]	BUS	3
DAXO-4 J0:31]~	BUS	3
DAX5	3	
DAX6-10 [0:31]	BUS	3
DAY[0:15]	BUS	3
EBS[0:11]	BUS	3; 3
EBS[0:11]	BUS	3; 3
ENVNPRO		3
OADRS1		3
OADRS2		3
ONRI		3
LAYO-	3	
LAYS	3	
LAYS-	3	
LAY4-	3	
LBLIO L	3	
LBLIO U	3	
MS		3
NF/BB		3
NSACS1		3
NSACS2		3

Signal ID	Source	Destination
NSAS1		3
NSAS2		3
NSEBS1		3
NSEBS2		3
NSLBLI1	3	4.6
NSLBLI2	3	4.6
NSWL1	3	4.6
NSWL2	3	4.6
NWLS[0:31]_A~	BUS	3
NWLS[0:31]_B~	BUS	3
NWLS[0:31] C~	BUS	3
NWLS[0:31]_D~	BUS	3
P/EADS		3
P/EAEN1		3
P/EAEN2		3
P/ECSO		3
P/ECS1		3
P/ECS2		3
P/ECS3		3
P/ECS4		3
P/ECS5		3
P/EDIS	6.1	3
P/EWLSN[0:31]	BUS	3
P/EWLSP[0:31]	BUS	3
VNISO		3
VNPRO	3	
VPERS		3; 6.1
VPISO		3
VPNR		3; 4
VPNRI		3
VPPRO		3
VP VNPRO		3
WL[0:31]	3	
YADCK1		3
YADCK2		3
YADEN1		3
YADEN2		3
YADRS		3
Y[0:15]	BUS	3; 4; 4
Y[0:15]	BUS	3; 4; 4

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

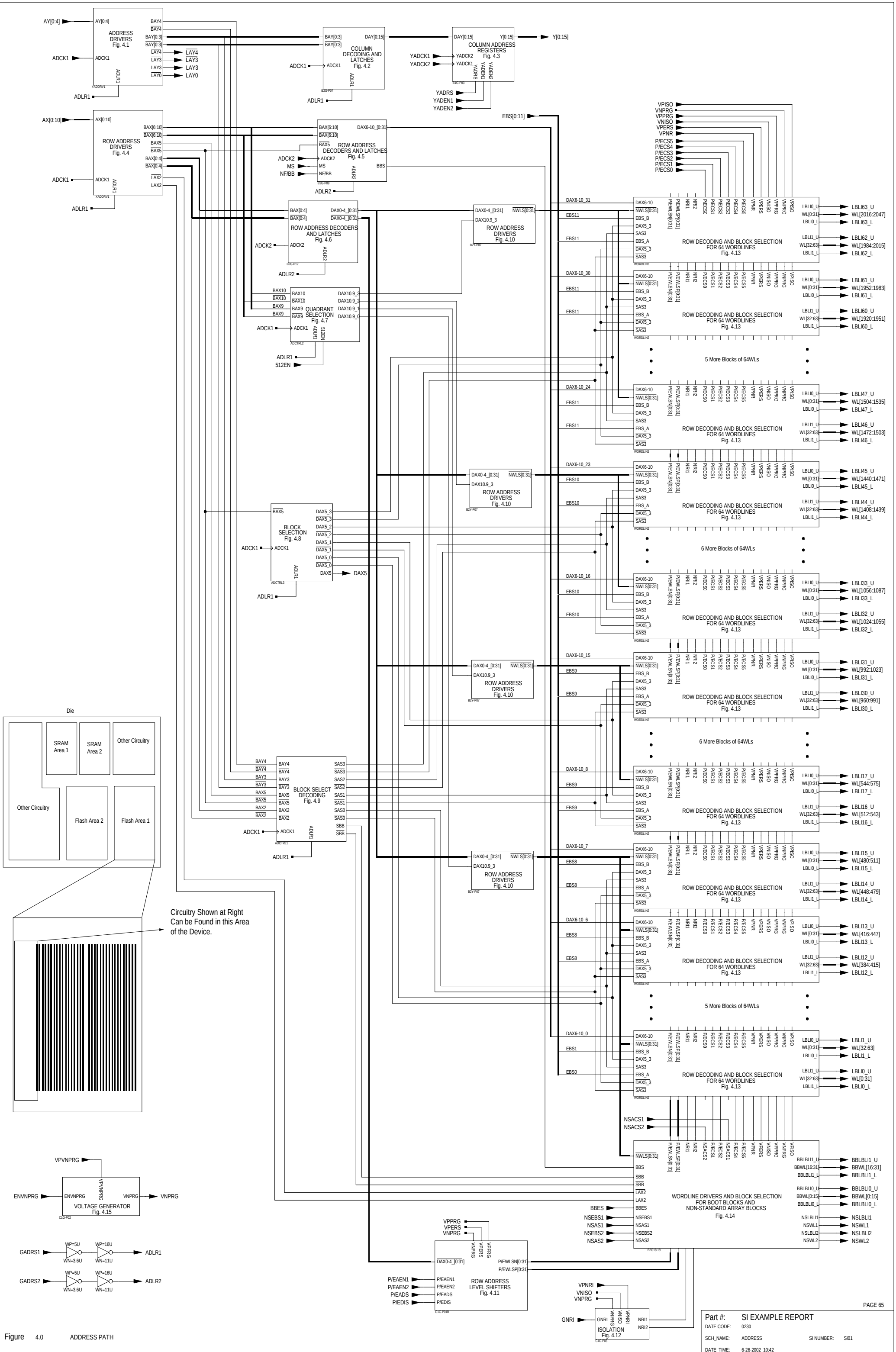


Figure 4.0 ADDRESS PATH

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	ADDRESS	SI NUMBER:	SI01
DATE_TIME:	6-26-2002_10:42		
LOCATION:	BLOCK_NAME	INITIALS:	GM

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

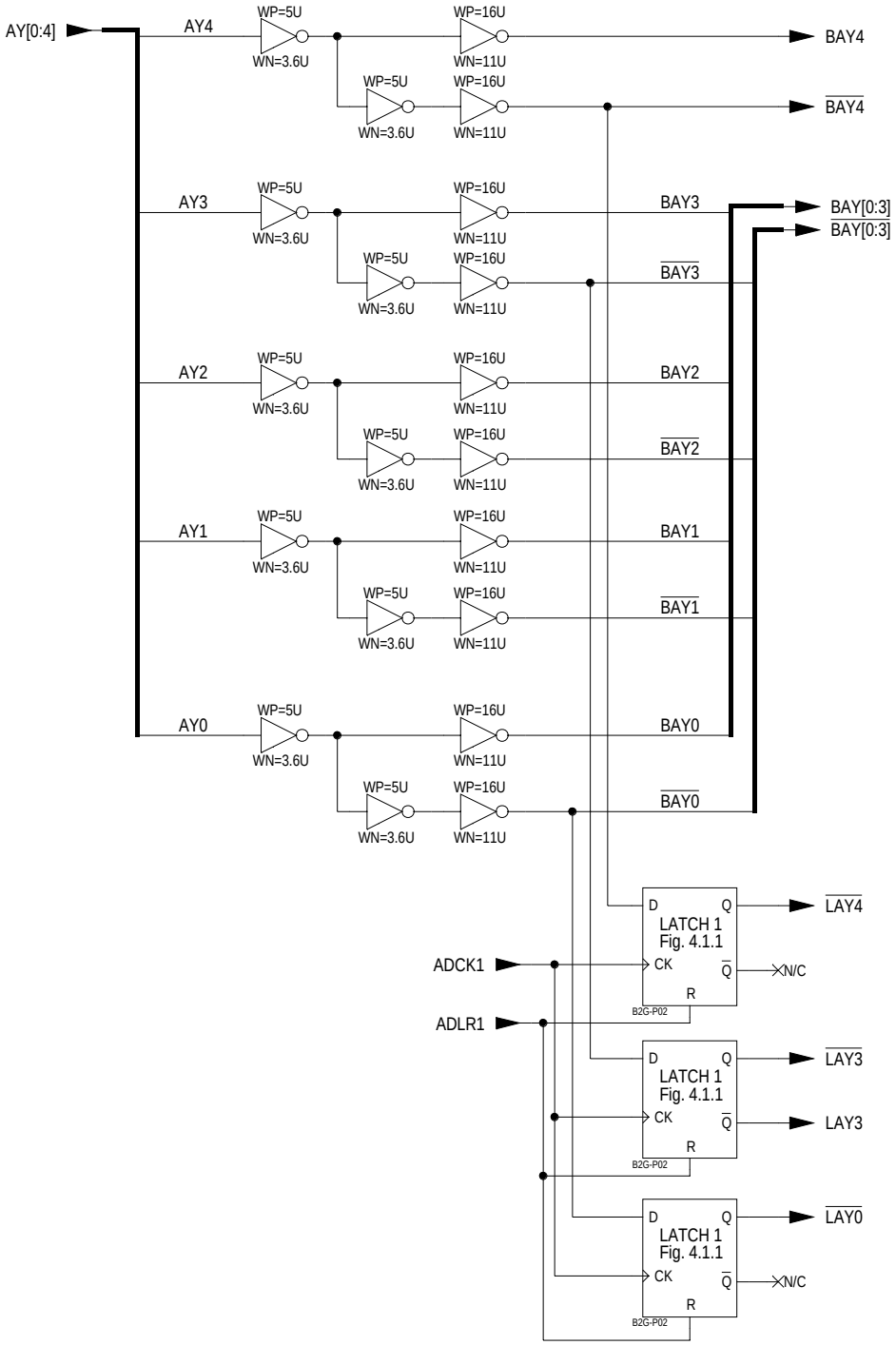


Figure 4.1 COLUMN ADDRESS DRIVERS

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	YADDRV1	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_12:51		
LOCATION:	BLOCK_NAME	INITIALS:	GM

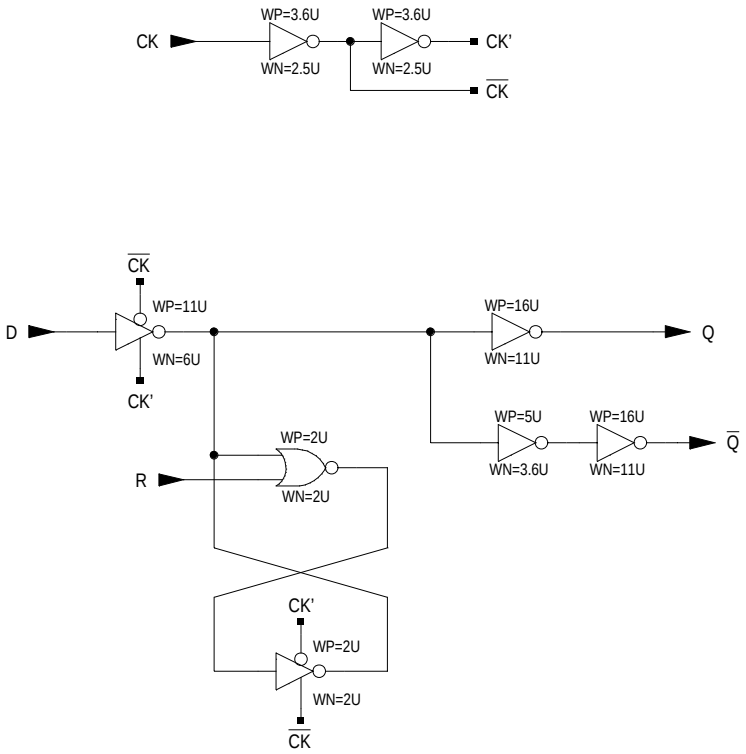
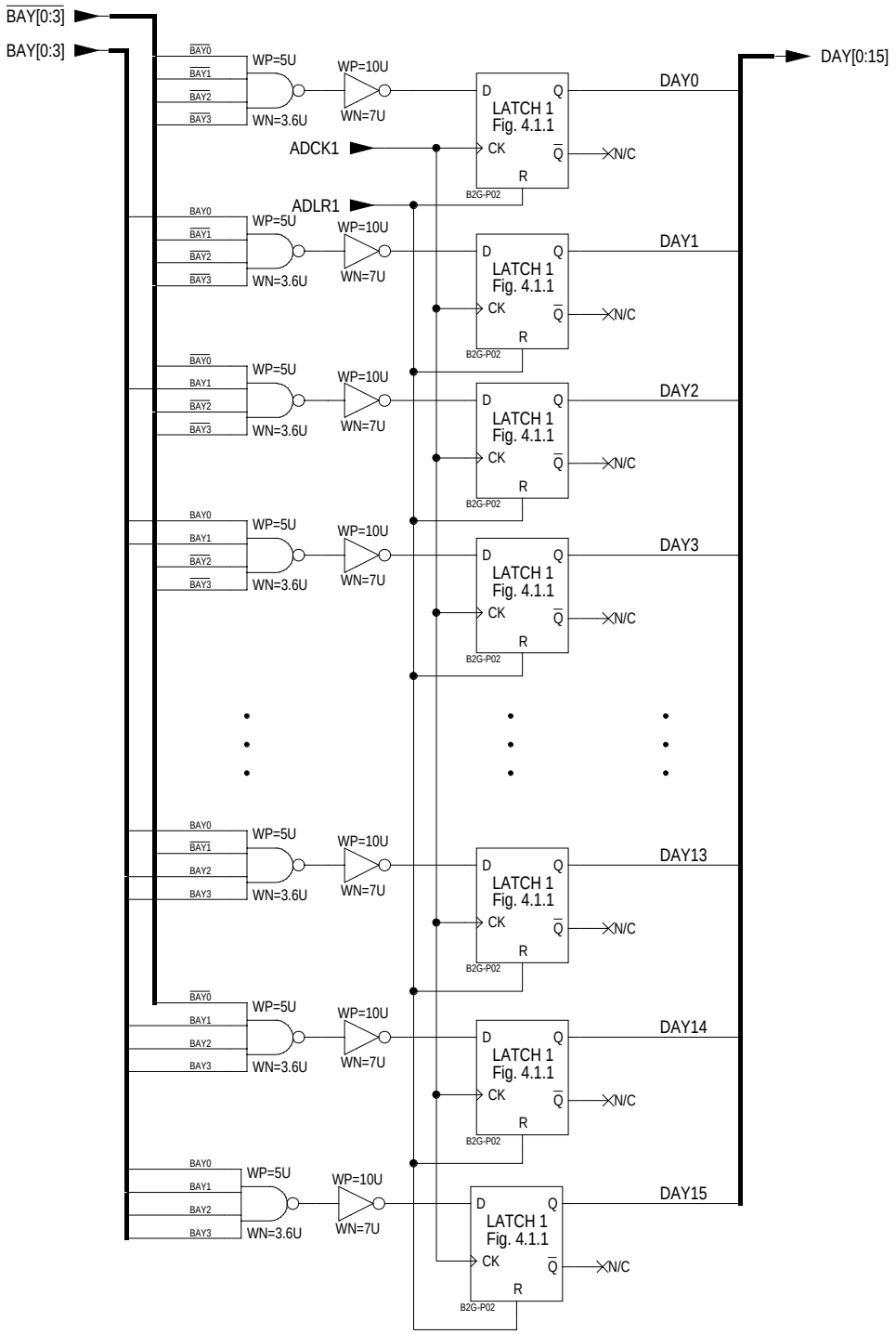


Figure 4.1.1 LATCH TYPE 1

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT		
DATE CODE:	EMBEDDED FLASH		
SCH_NAME:	B2G-P03	SI NUMBER:	3945
DATE_TIME:	6-20-2002_12:52		
LOCATION:	BLOCK_NAME	INITIALS:	GM



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2G-P07	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_12:52		
LOCATION:	BLOCK_NAME	INITIALS:	GM

Figure 4.2 COLUMN DECODING AND LATCHES

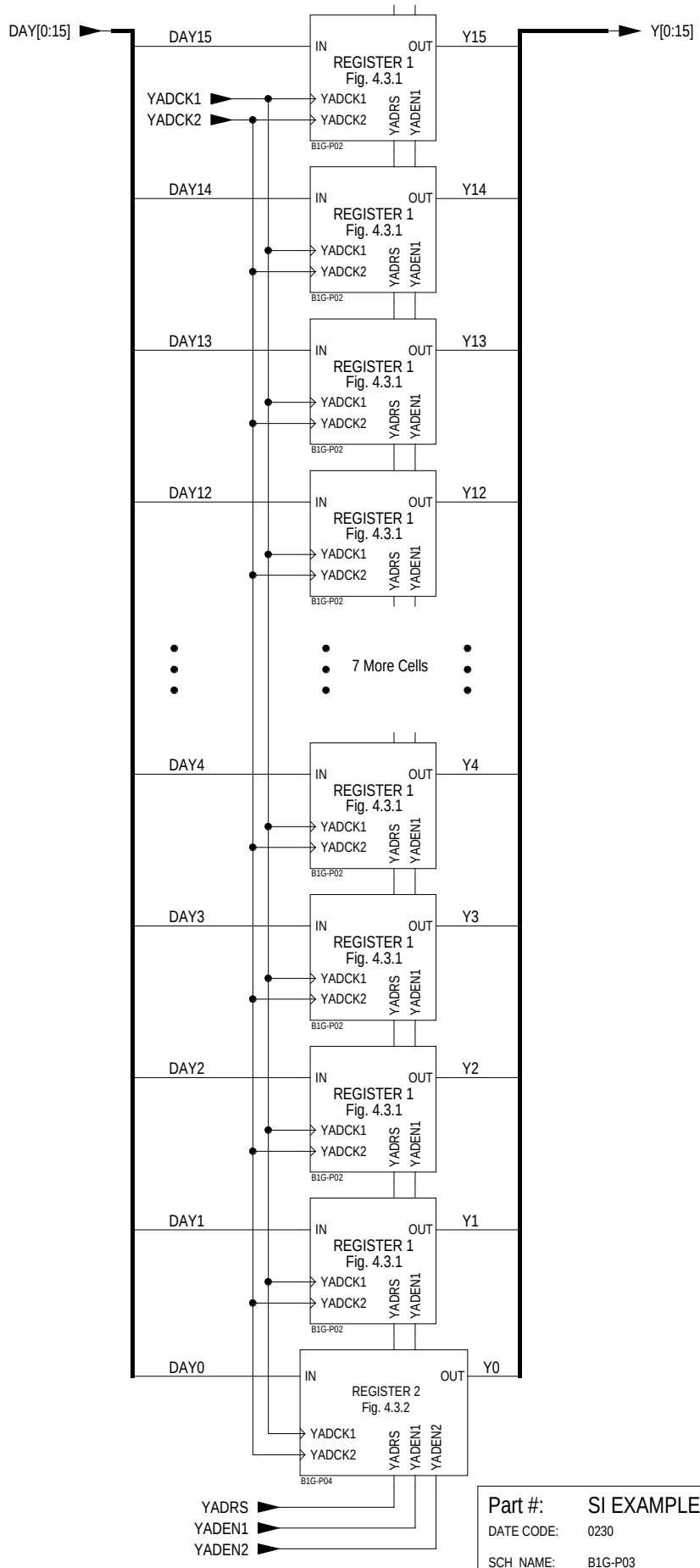


Figure 4.3 COLUMN ADDRESS REGISTERS

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B1G-P03	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_12:52		
LOCATION:	BLOCK_NAME	INITIALS:	GM

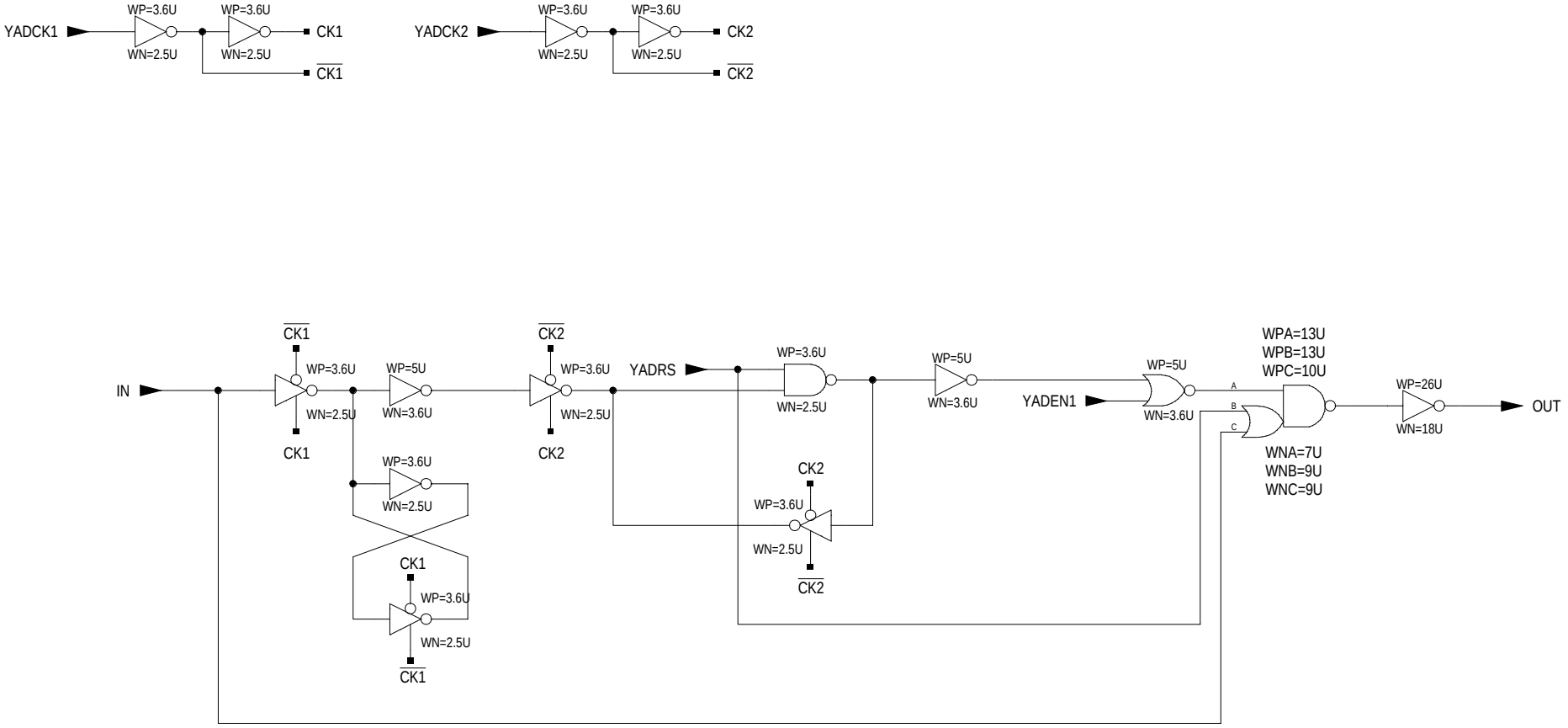


Figure 4.3.1 REGISTER 1 FOR DECODED COLUMN ADDRESSES

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B1G-P02	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_12:58		
LOCATION:	BLOCK_NAME	INITIALS:	GM

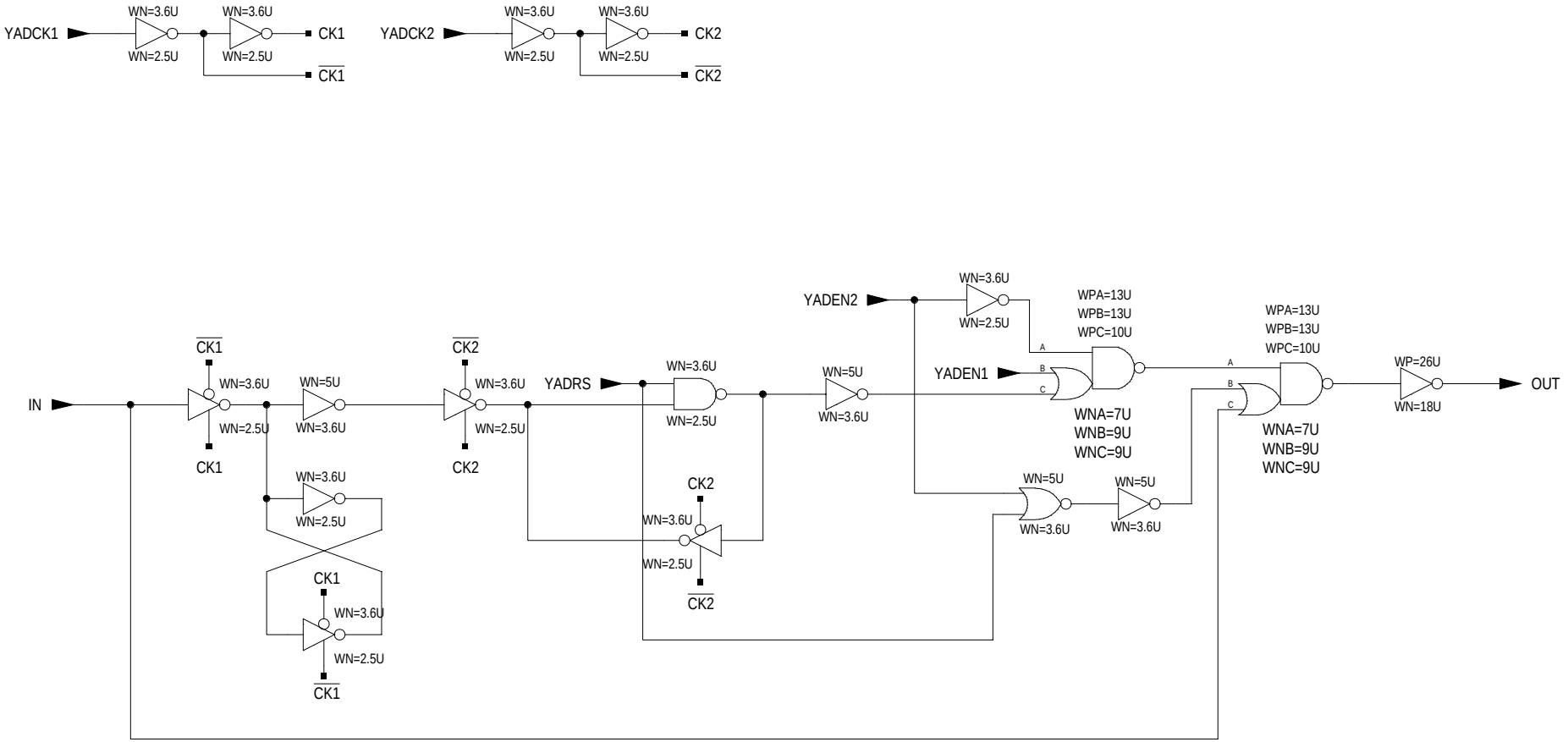


Figure 4.3.2 REGISTER 2 FOR DECODED COLUMN ADDRESSES

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B1G-P04	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_12:58		
LOCATION:	BLOCK_NAME	INITIALS:	GM

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

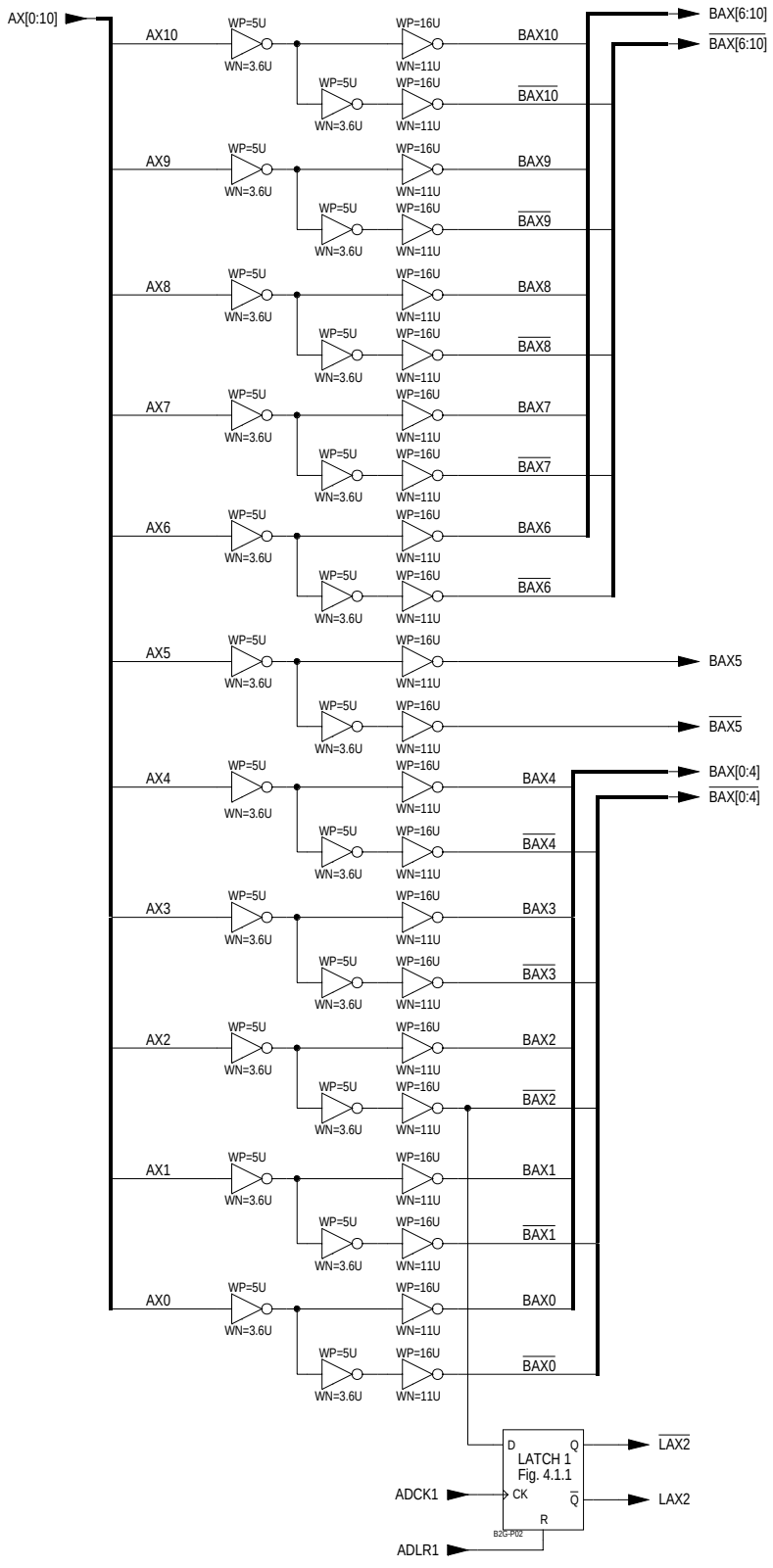


Figure 4.4 ROW ADDRESS DRIVERS

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	XADDRV1	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_12:58		
LOCATION:	BLOCK_NAME	INITIALS:	GM

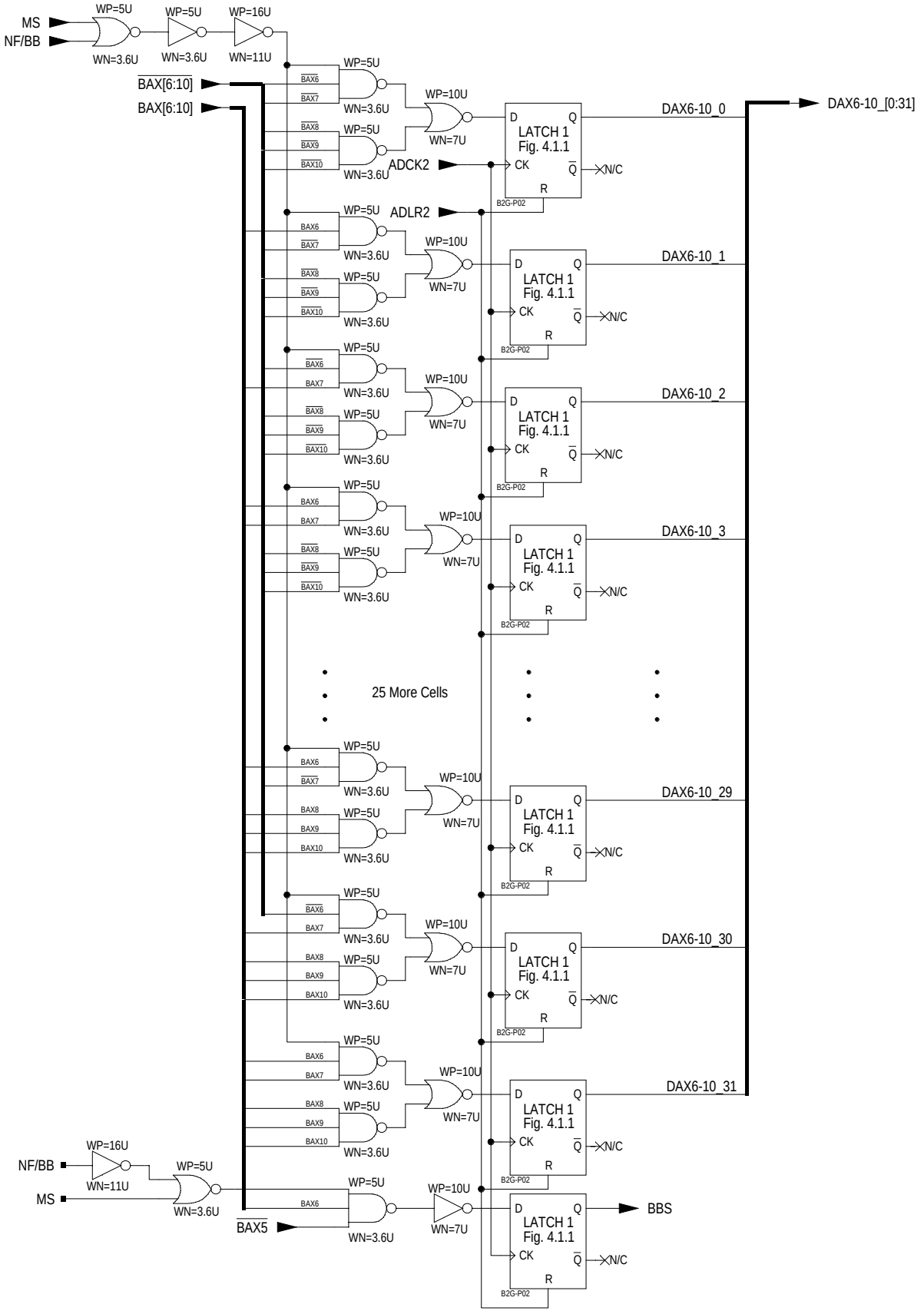


Figure 4.5 ROW ADDRESS DECODING AND LATCHES (UPPER BITS)

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2G-P09	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_12:58		
LOCATION:	BLOCK_NAME	INITIALS:	GM

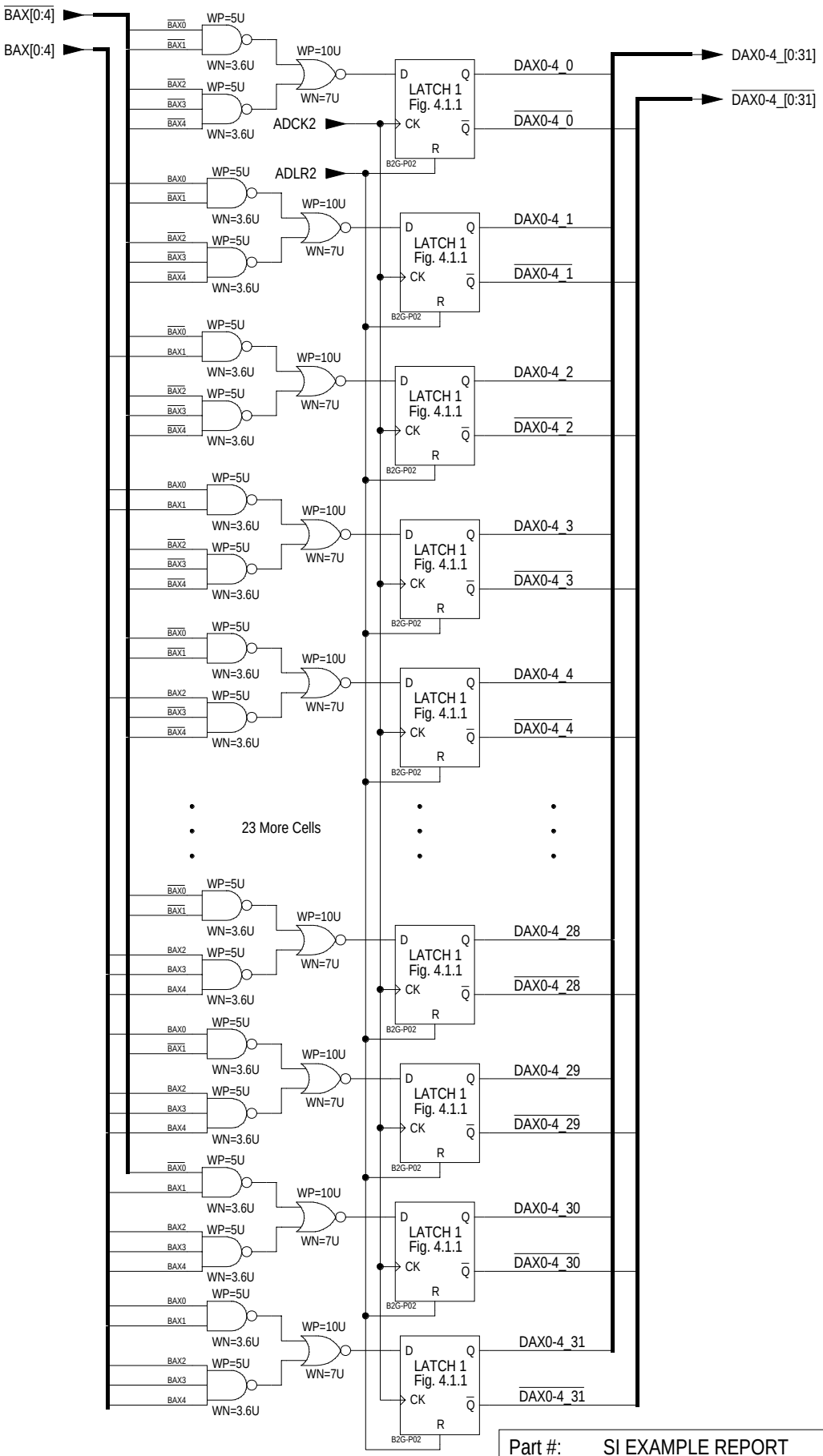


Figure 4.6 ROW ADDRESS DECODING AND LATCHES (LOWER BITS)

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2G-P12	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_12:58		
LOCATION:	BLOCK_NAME	INITIALS:	GM

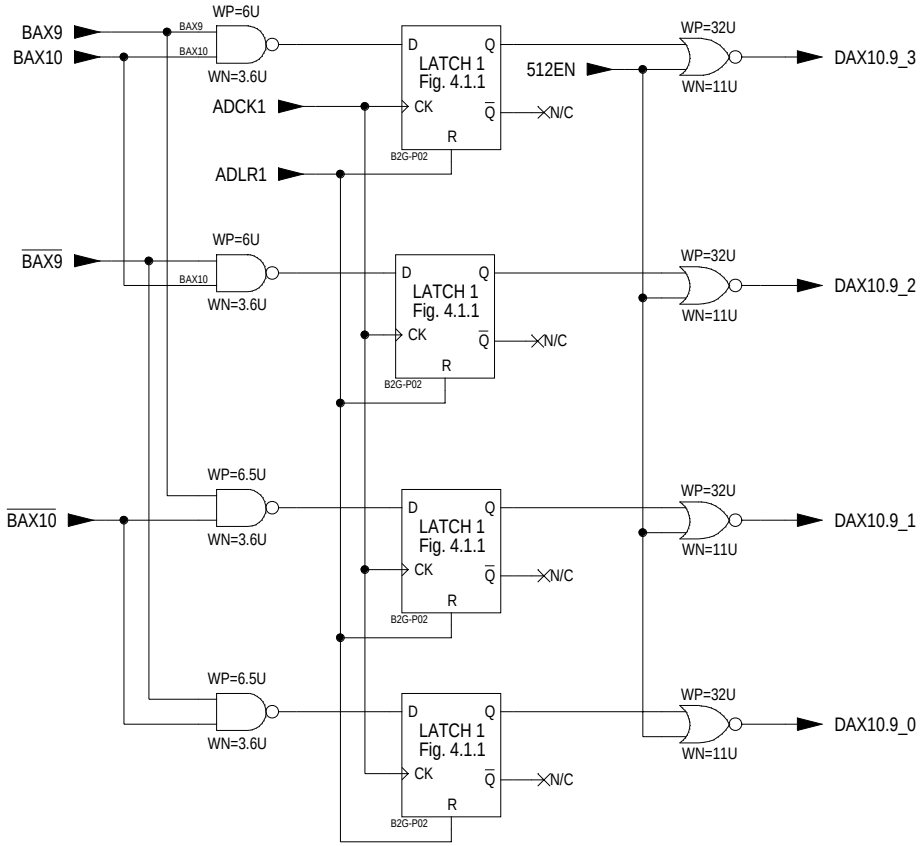


Figure 4.7 ROW ADDRESS DECODING QUADRANT SELECTION

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	ADCTRL2	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_12:59		
LOCATION:	BLOCK_NAME	INITIALS:	GM

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

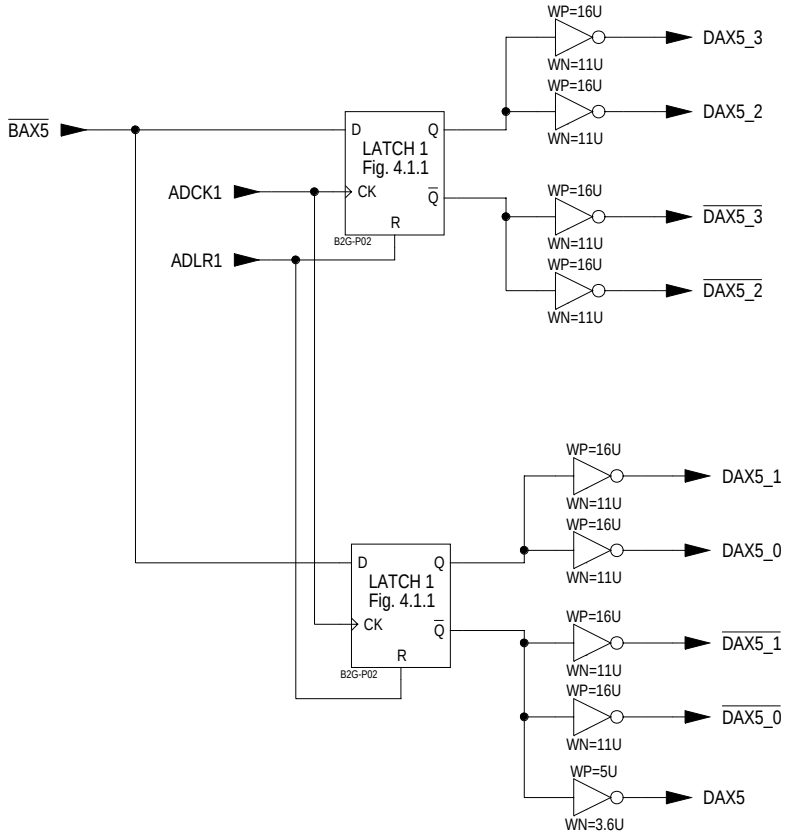


Figure 4.8 ROW ADDRESS LATCH AND DRIVERS

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	ADCTRL3	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_12:59		
LOCATION:	BLOCK_NAME	INITIALS:	GM

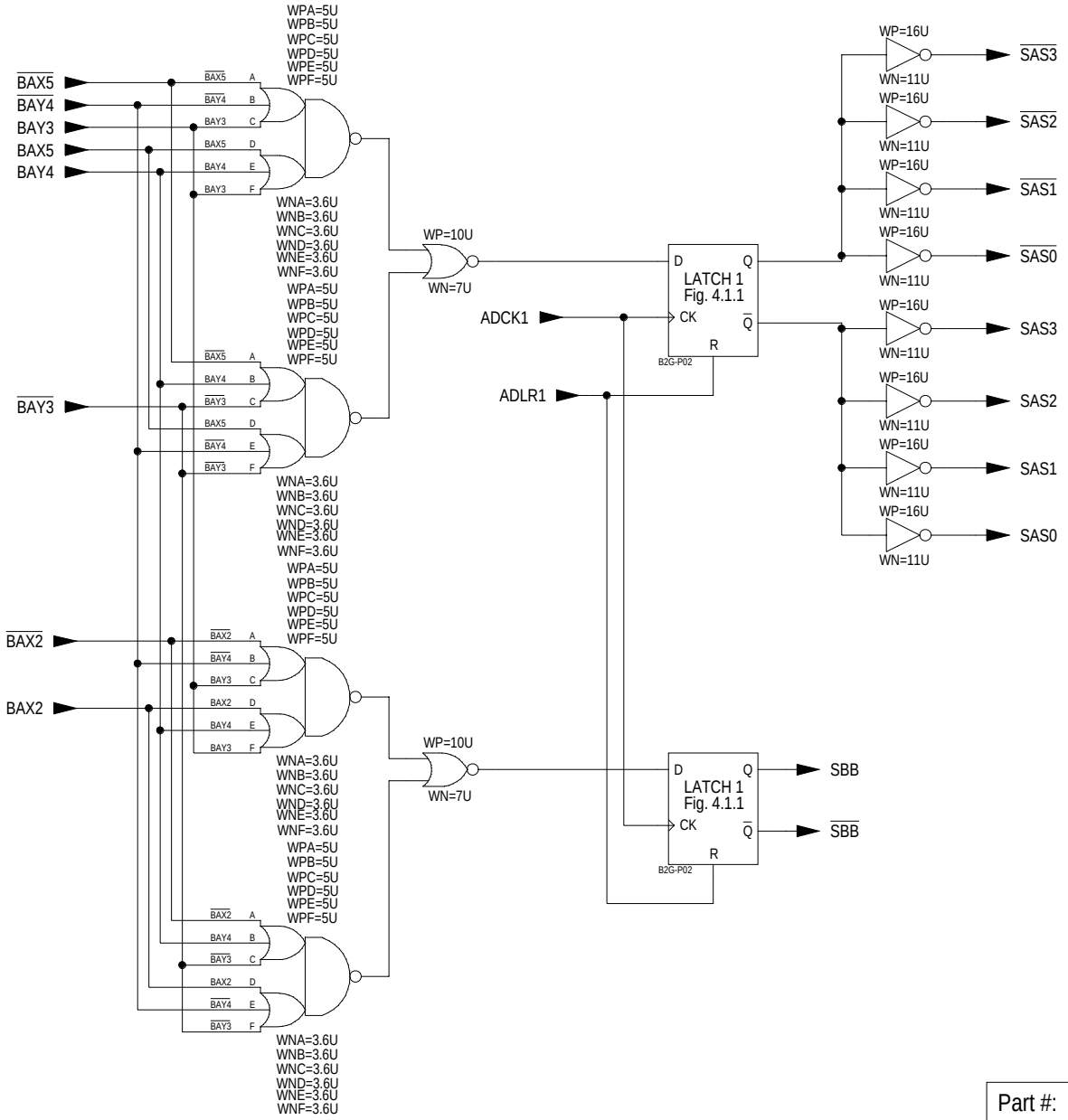
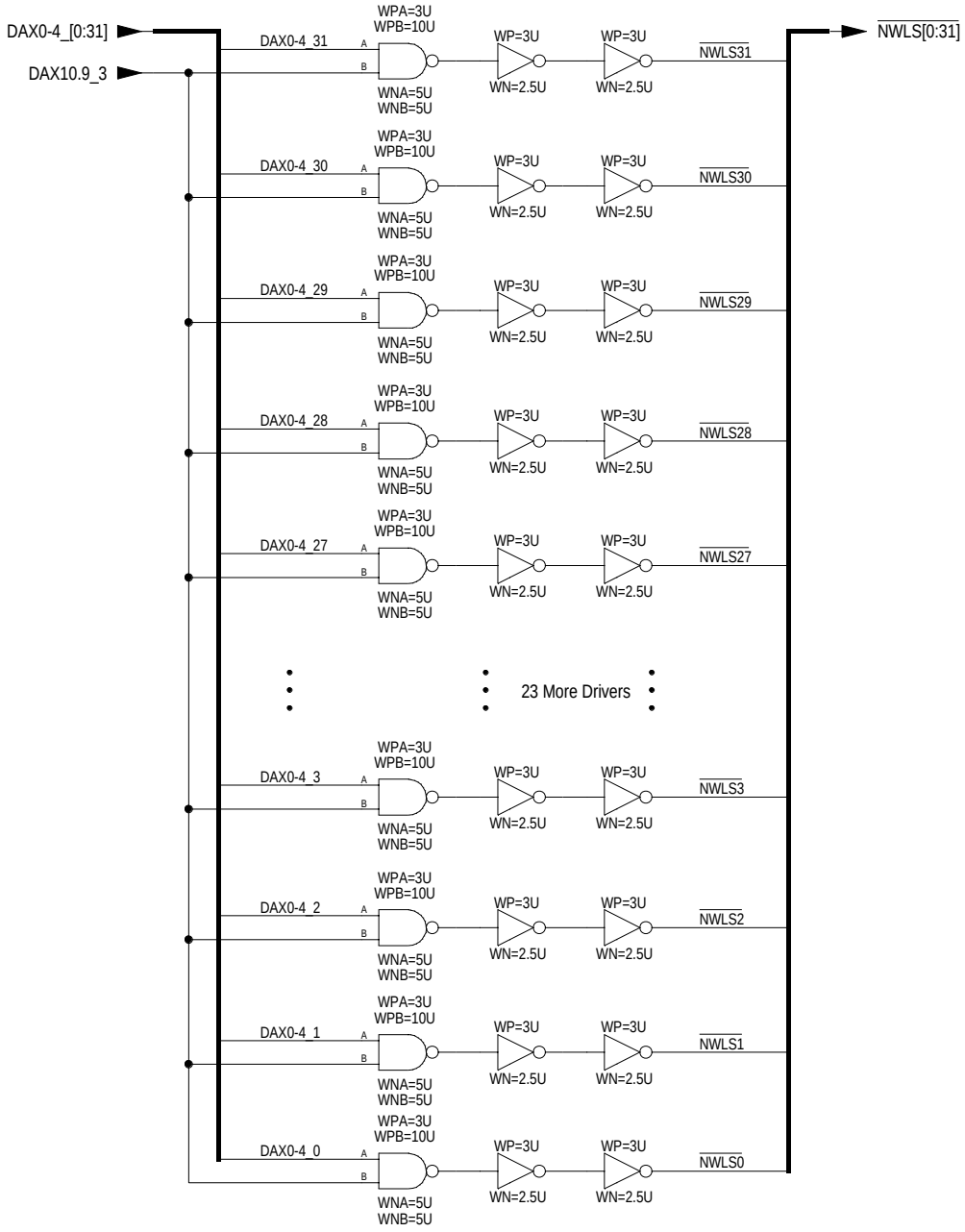


Figure 4.9 BLOCK SELECTION DECODING

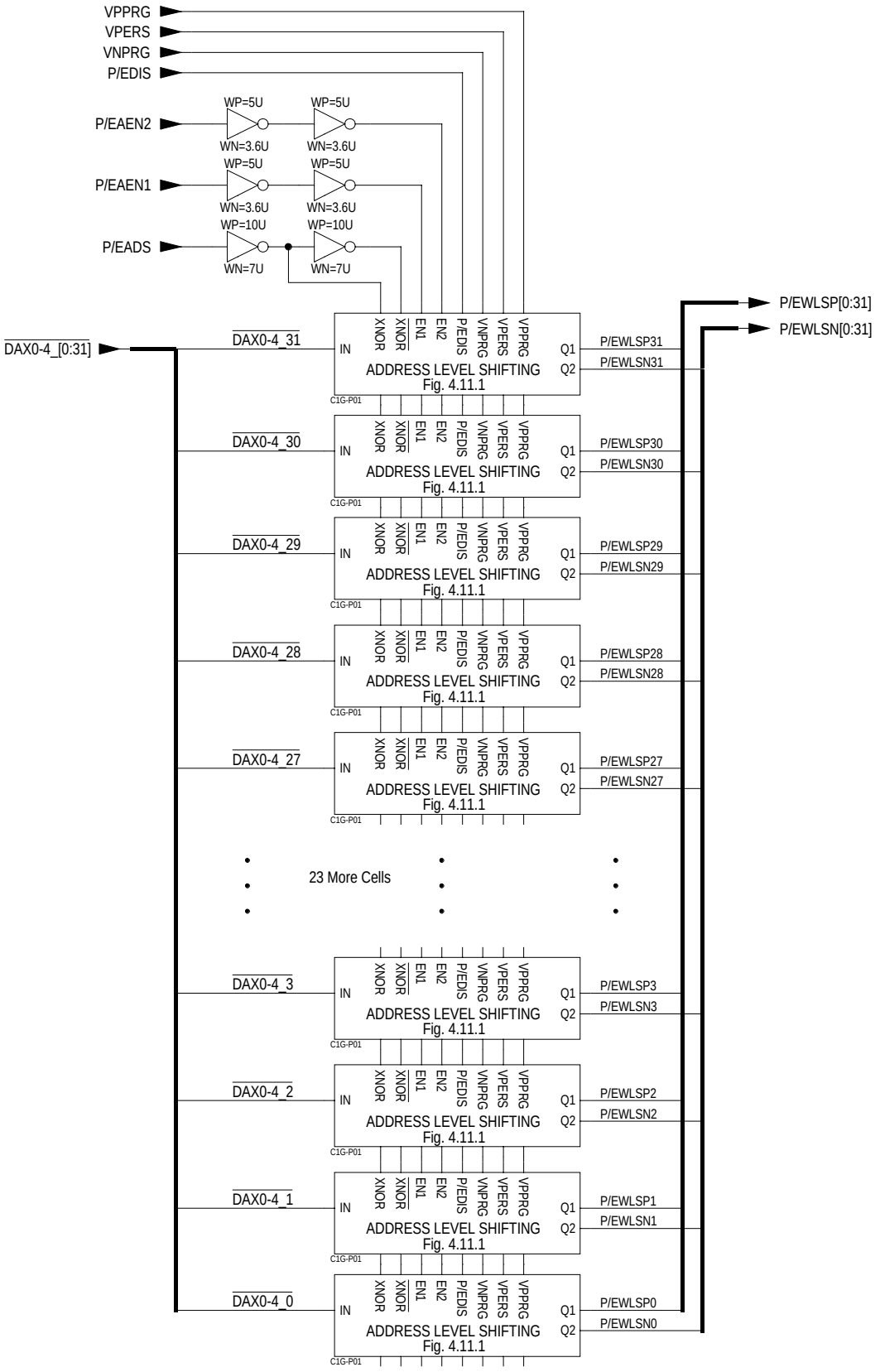
Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	ADCTRL1	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_12:59		
LOCATION:	BLOCK_NAME	INITIALS:	GM

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2Y-P07	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_12:59		
LOCATION:	BLOCK_NAME	INITIALS:	GM

Figure 4.10 DECODED ROW ADDRESS DRIVERS



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	C1G-P01B	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_12:59		
LOCATION:	BLOCK_NAME	INITIALS:	GM

Figure 4.11 DECODED ROW ADDRESS LEVEL SHIFTERS FOR PROGRAM/ERASE

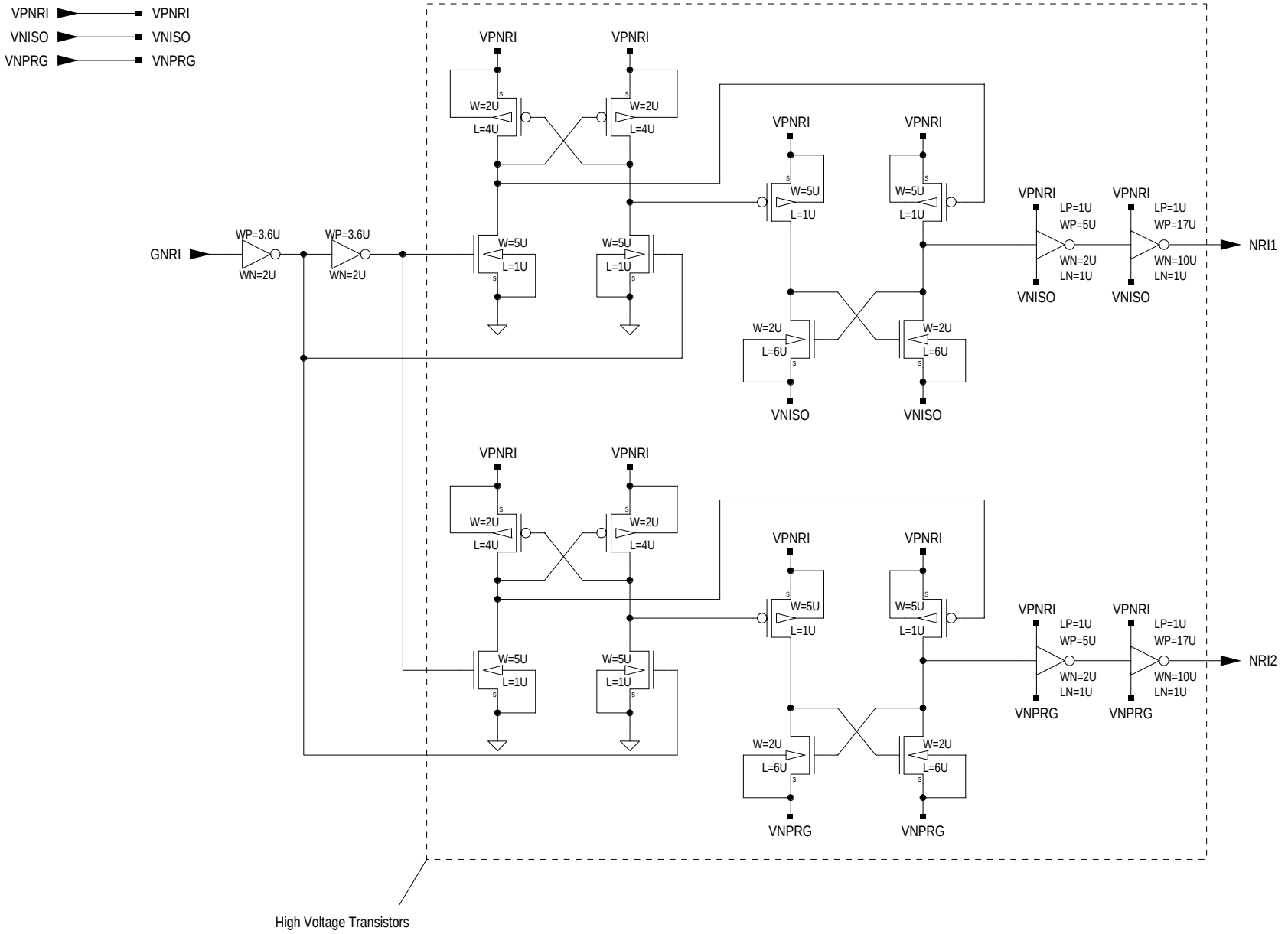


Figure 4.12 ROW ADDRESS ENABLE SIGNAL DRIVERS

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	C1G-P03	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:00		
LOCATION:	BLOCK_NAME	INITIALS:	GM

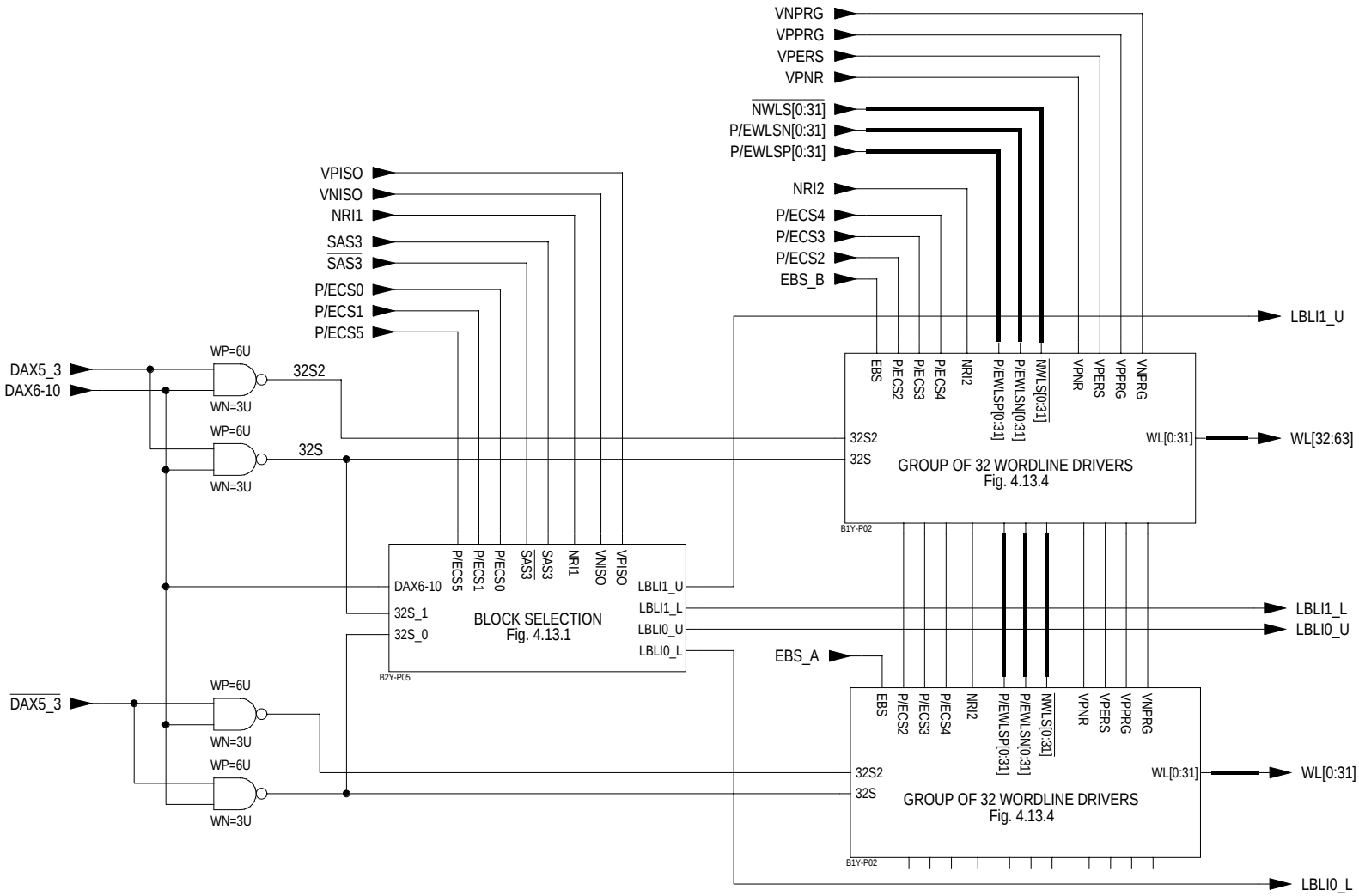
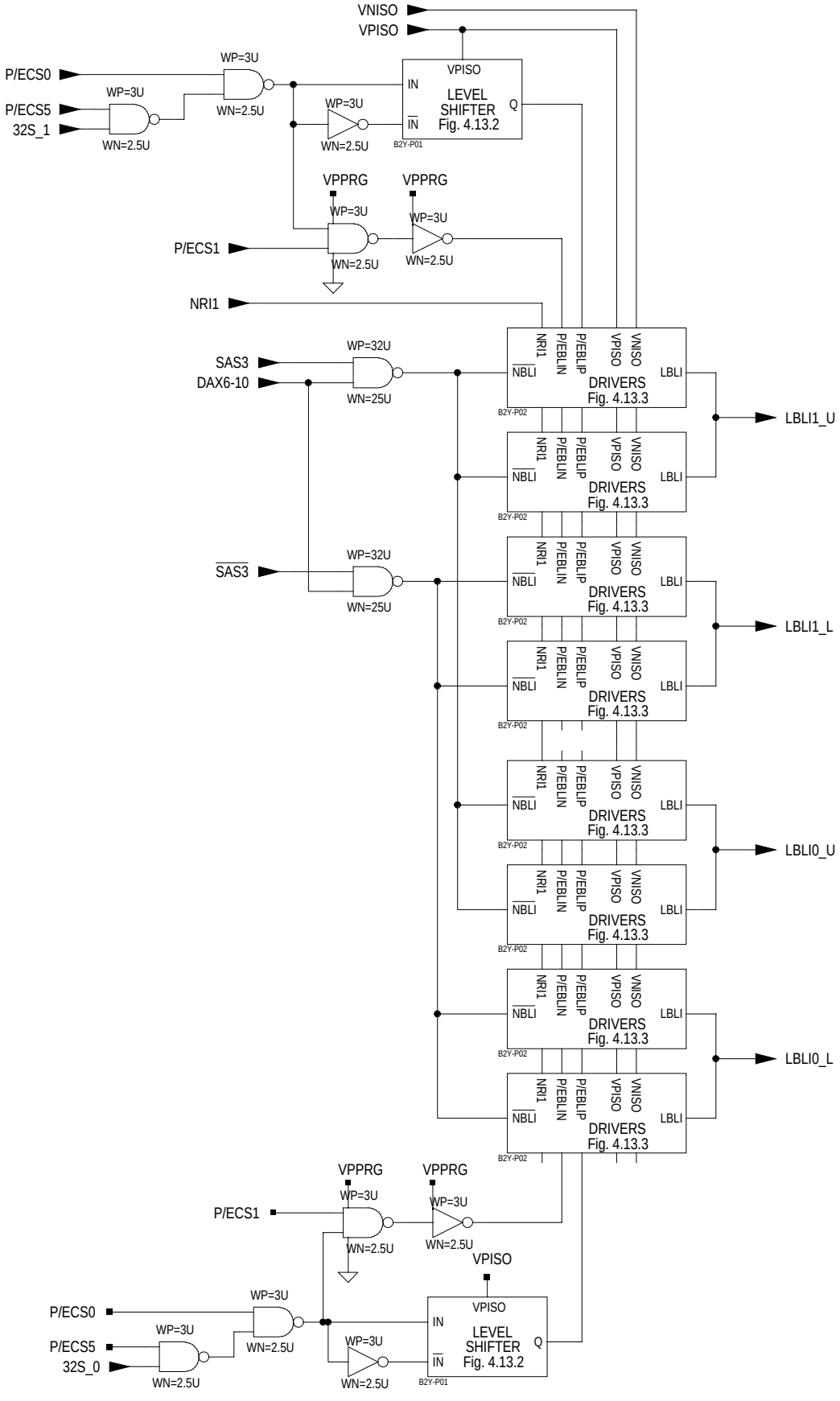


Figure 4.13 GROUP OF 32 WORDLINE DRIVERS

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	WORDLIN2	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:00		
LOCATION:	BLOCK_NAME	INITIALS:	GM

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



PAGE 82

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2Y-P05	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:01		
LOCATION:	BLOCK_NAME	INITIALS:	GM

Figure 4.13.1 BLOCK SELECT SIGNAL GENERATORS FOR 64 WORDLINES

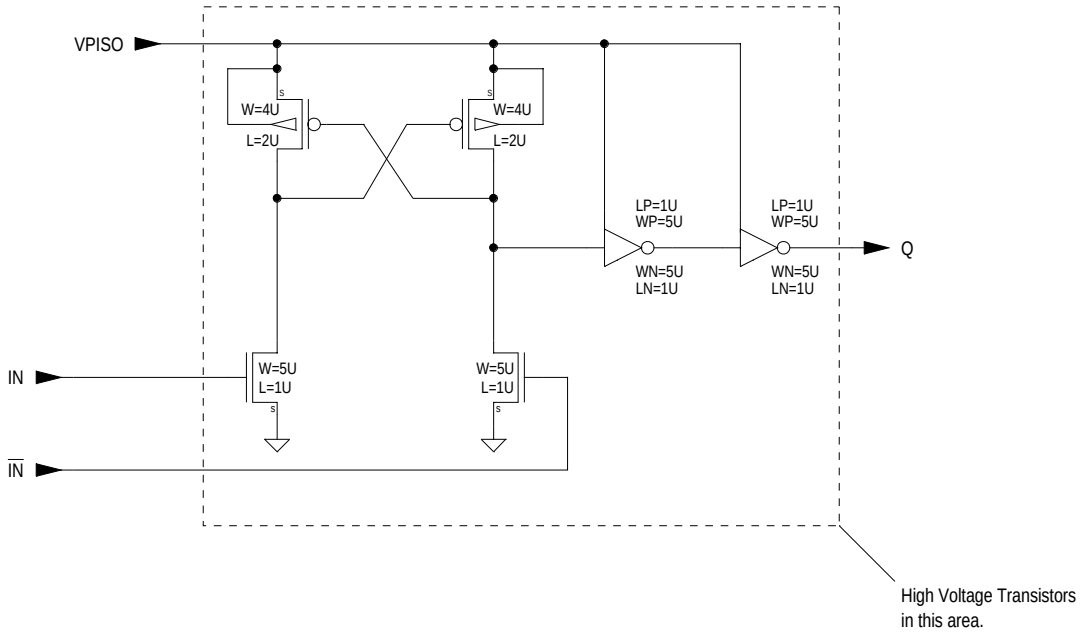


Figure 4.13.2 LEVEL SHIFTER

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2Y-P01	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:01		
LOCATION:	BLOCK_NAME	INITIALS:	GM

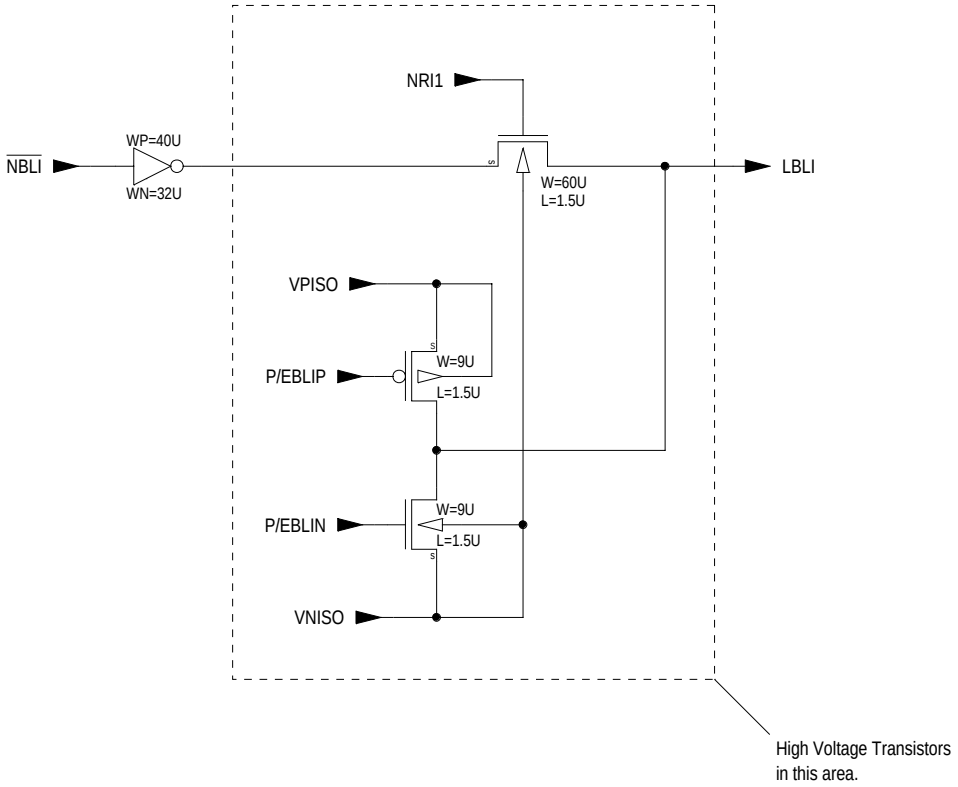


Figure 4.13.3 DRIVER ARRANGEMENTS FOR NORMAL READ, PROGRAM AND ERASE

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2Y-P02	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:01		
LOCATION:	BLOCK_NAME	INITIALS:	GM

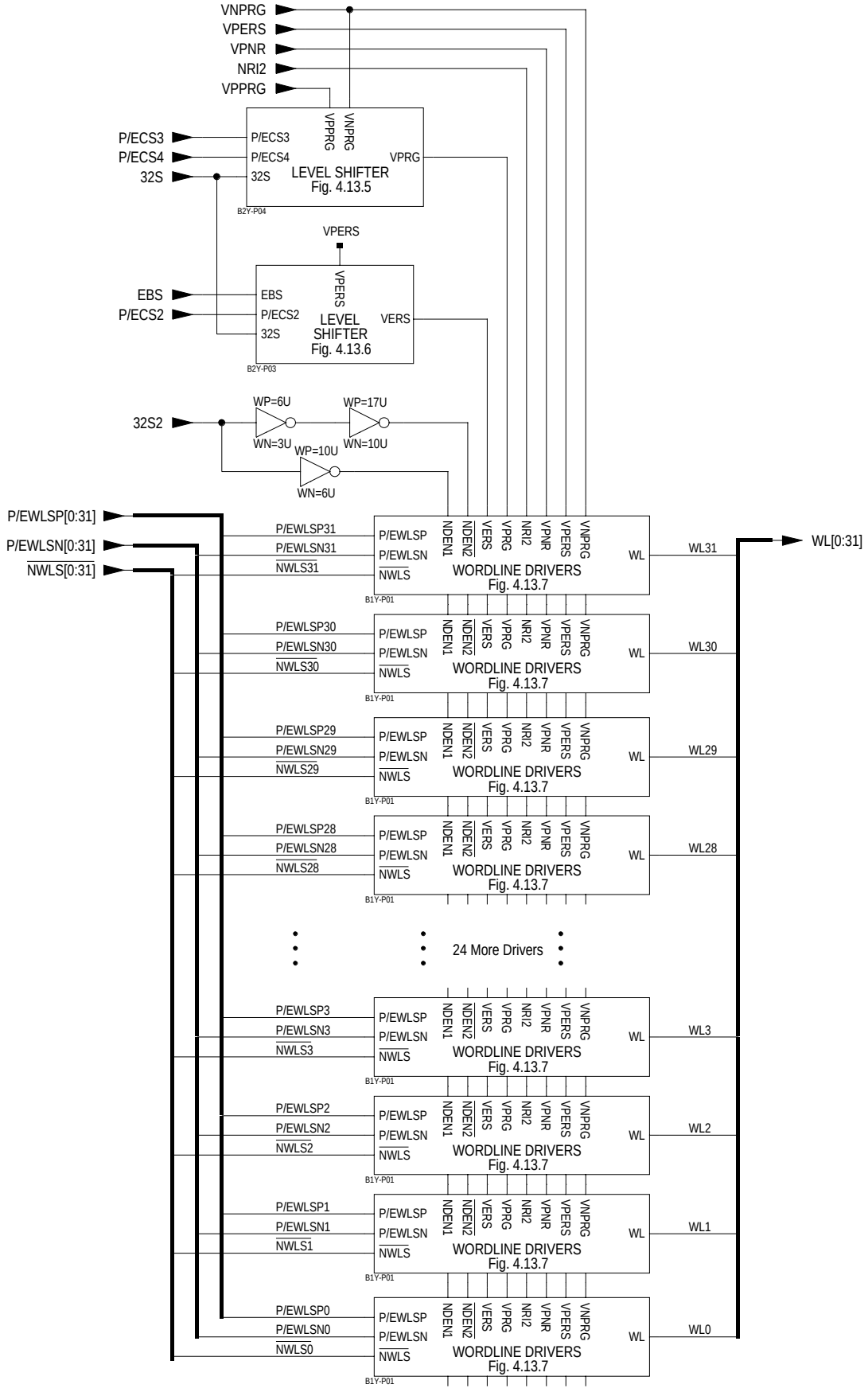


Figure 4.13.4 GROUP OF 32 WORDLINE DRIVERS

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B1Y-P02	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:02		
LOCATION:	BLOCK_NAME	INITIALS:	GM

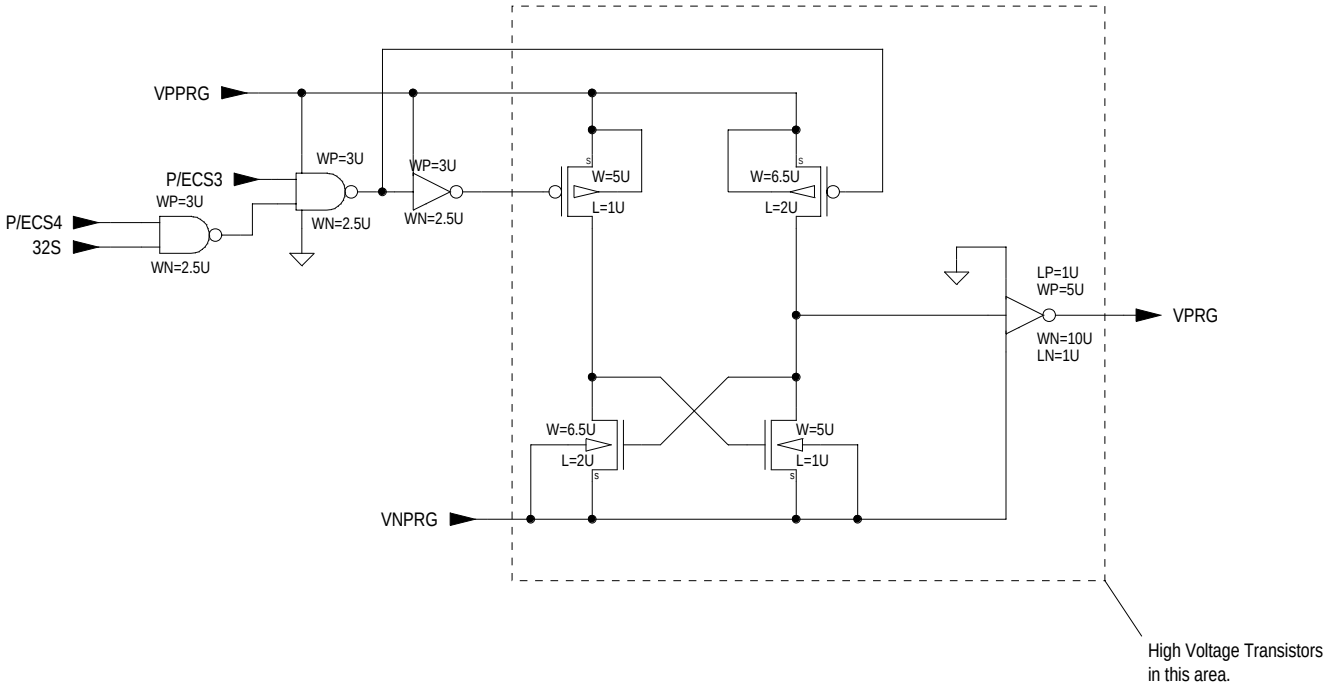


Figure 4.13.5 LEVEL SHIFTER FOR PROGRAMMING PURPOSES

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2Y-P04	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:02		
LOCATION:	BLOCK_NAME	INITIALS:	GM

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

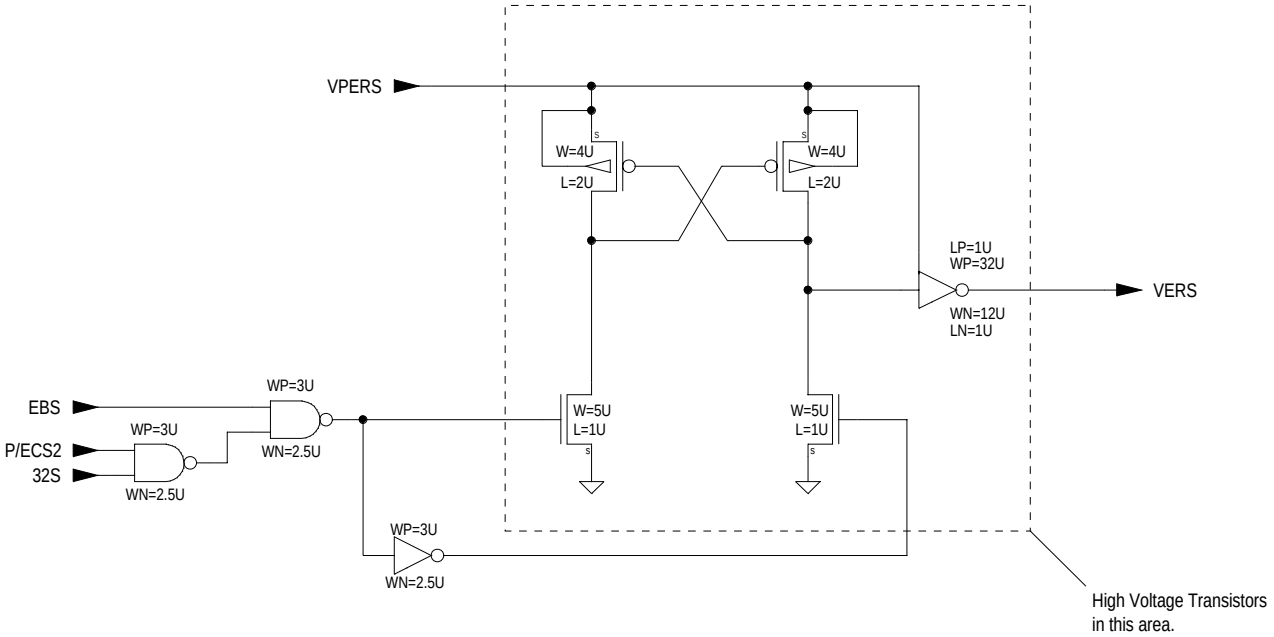


Figure 4.13.6 LEVEL SHIFTER FOR ERASE PURPOSES

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2Y-P03	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:02		
LOCATION:	BLOCK_NAME	INITIALS:	GM

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

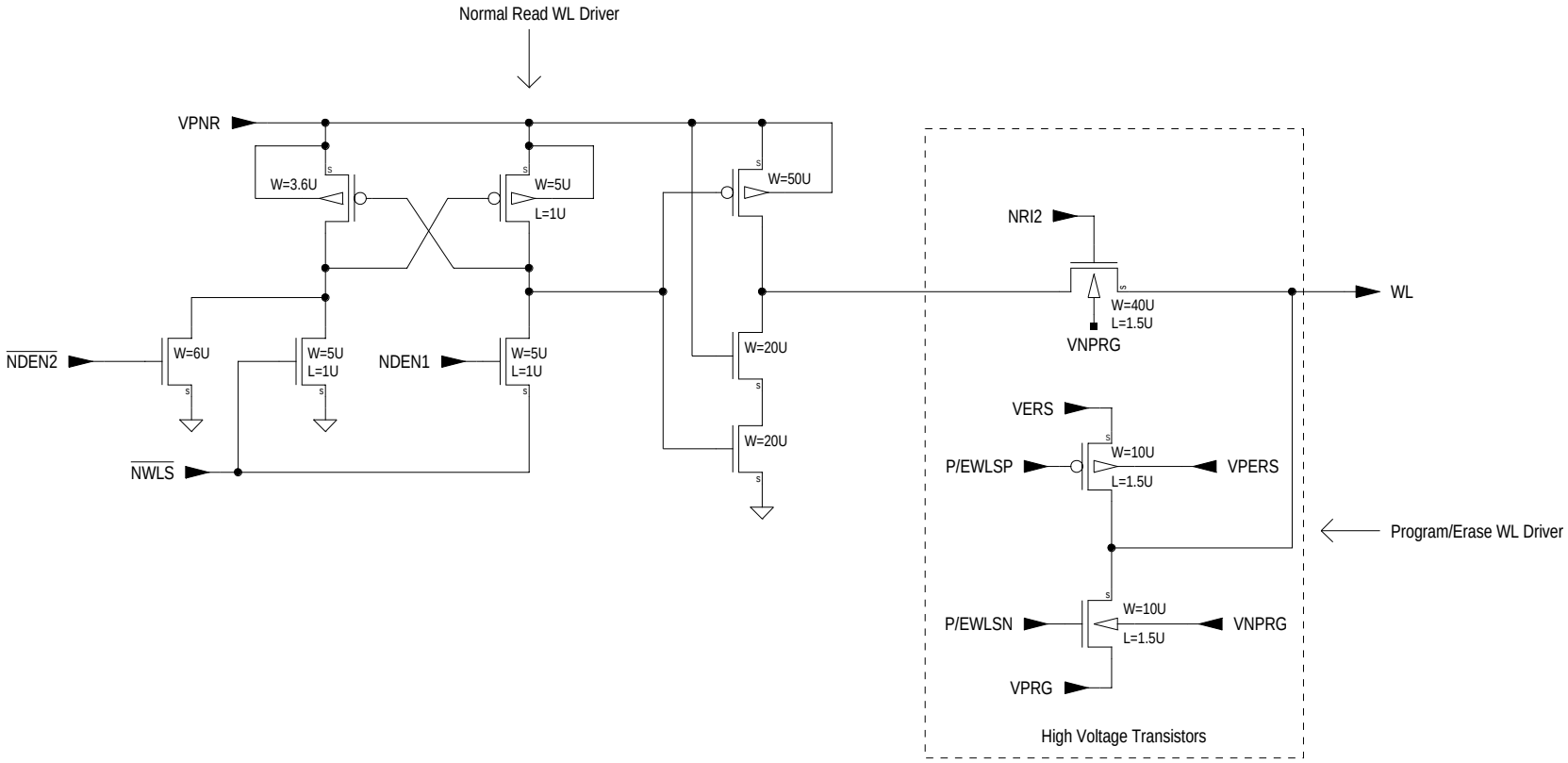
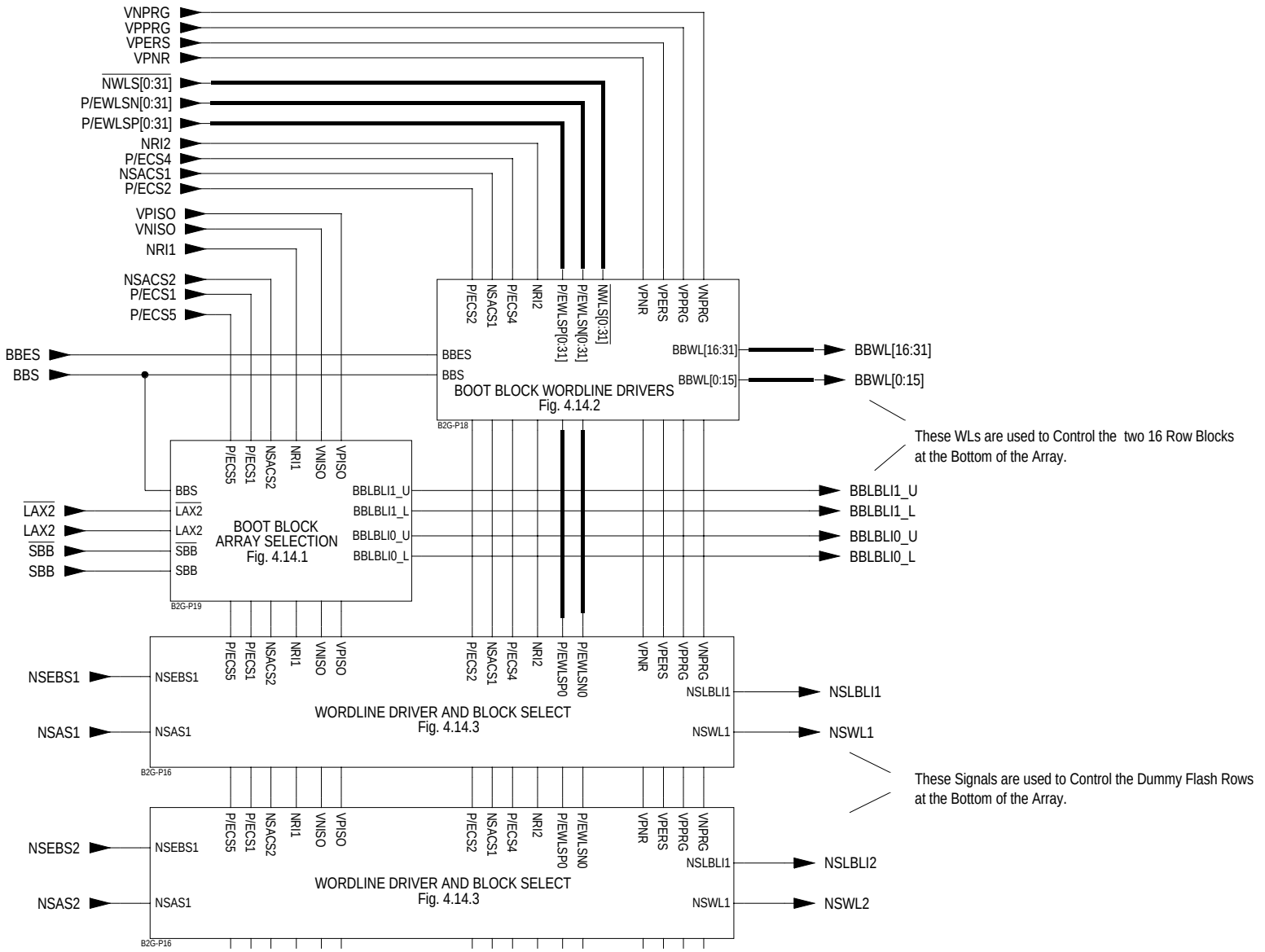


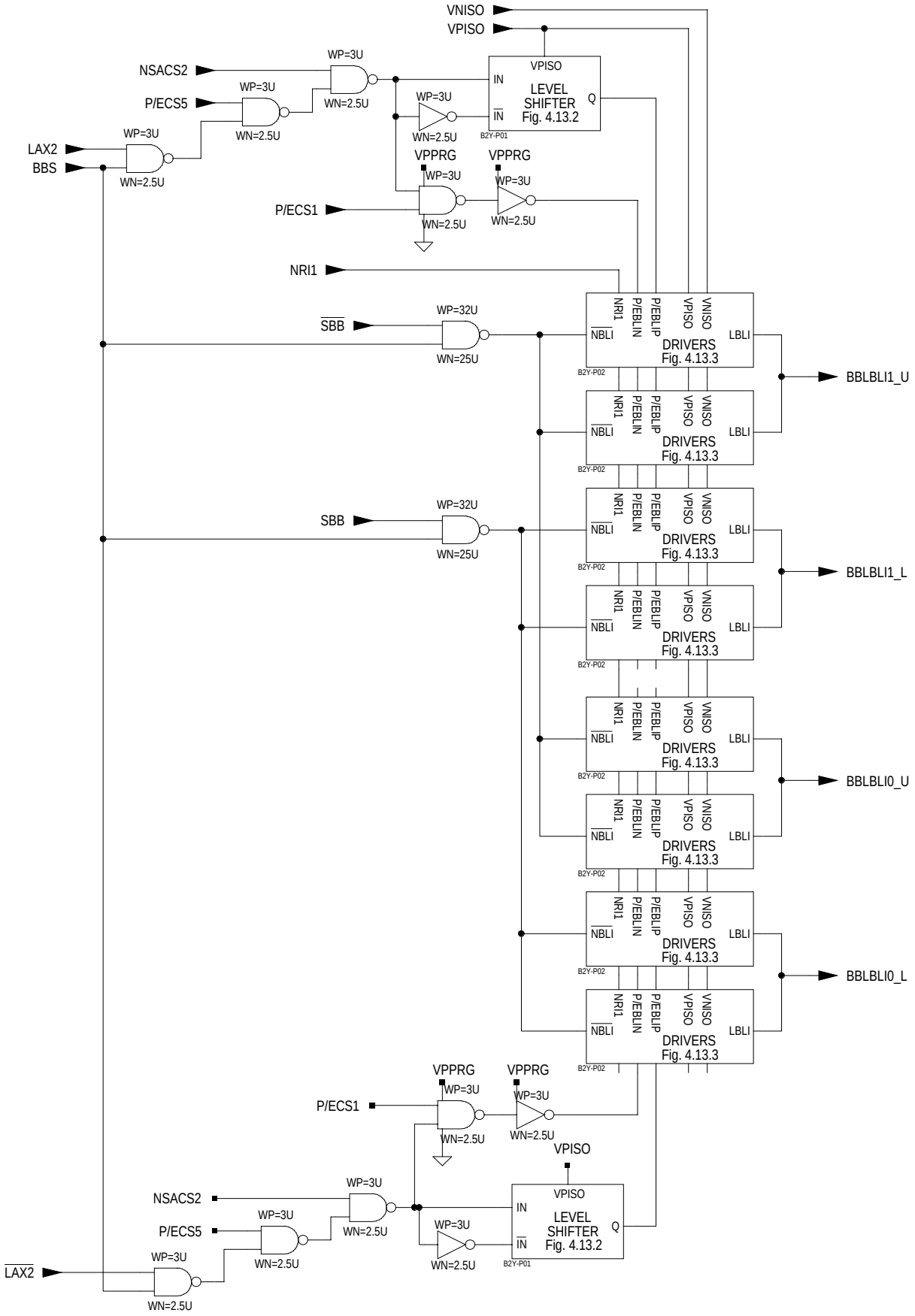
Figure 4.13.7 WORDLINE DRIVERS

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B1Y-P01	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:02		
LOCATION:	BLOCK_NAME	INITIALS:	GM



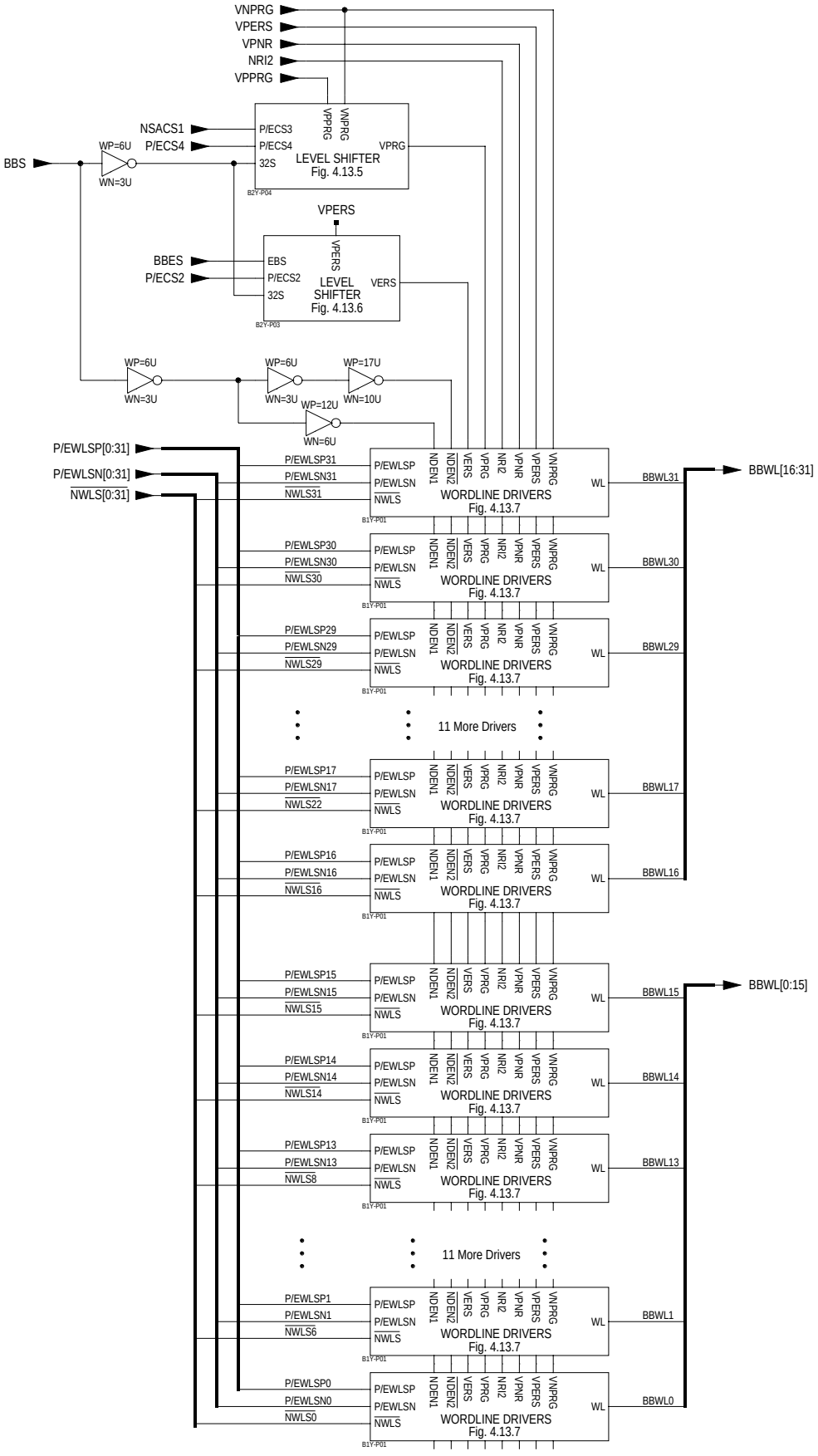
Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2G18-19	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:12		
LOCATION:	BLOCK_NAME	INITIALS:	GM

Figure 4.14 ROW ADDRESS CIRCUITRY FOR BOOT BLOCK AND NON STANDARD ARRAYS



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2G-P19	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:03		
LOCATION:	BLOCK_NAME	INITIALS:	GM

Figure 4.14.1 BLOCK SELECT SIGNAL GENERATORS FOR BOTTOM GROUP OF 32 WLS



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2G-P18	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:03		
LOCATION:	BLOCK_NAME	INITIALS:	GM

Figure 4.14.2 GROUP OF 32 WORDLINE DRIVERS FOR THE BOOT BLOCK

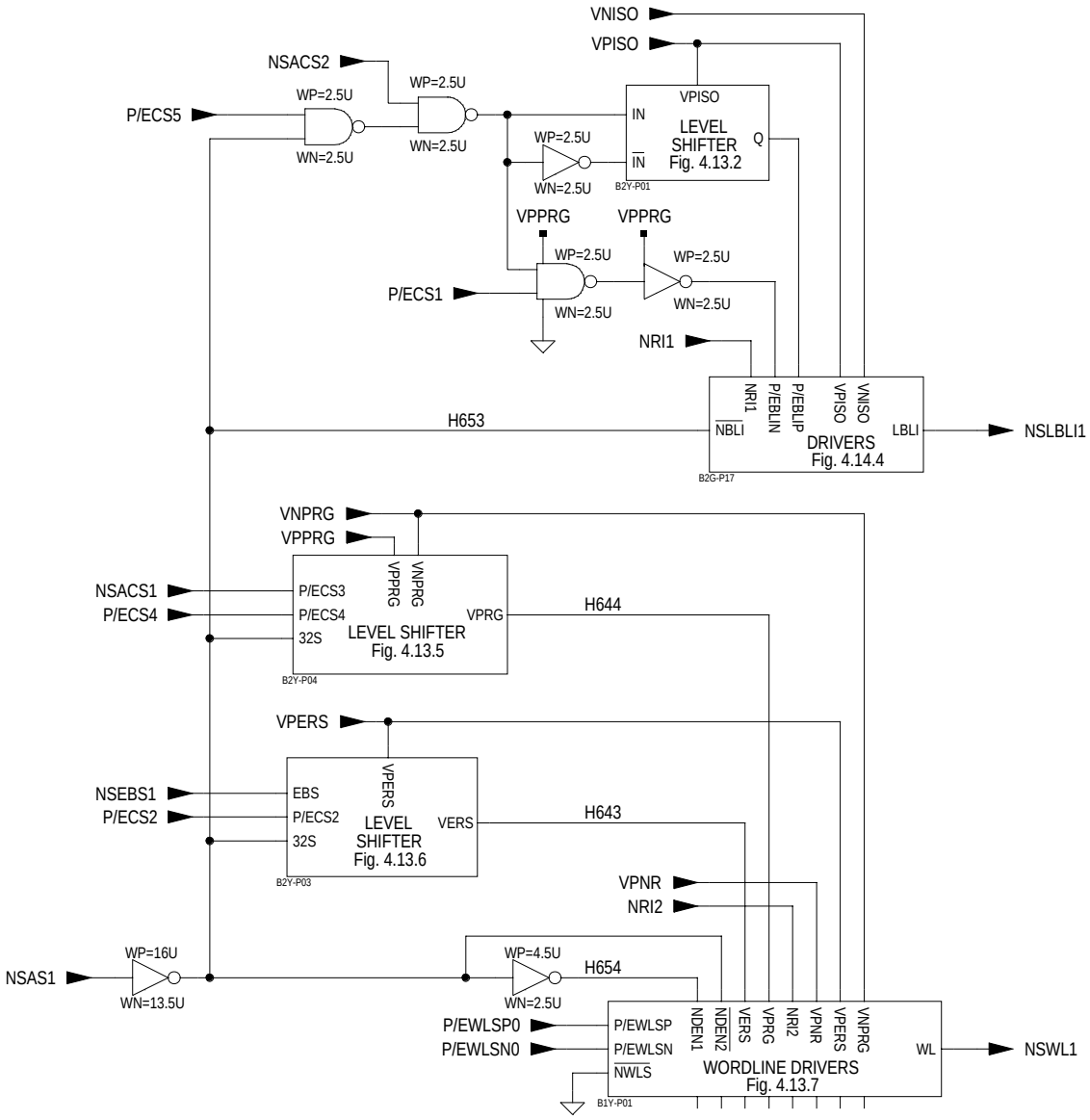
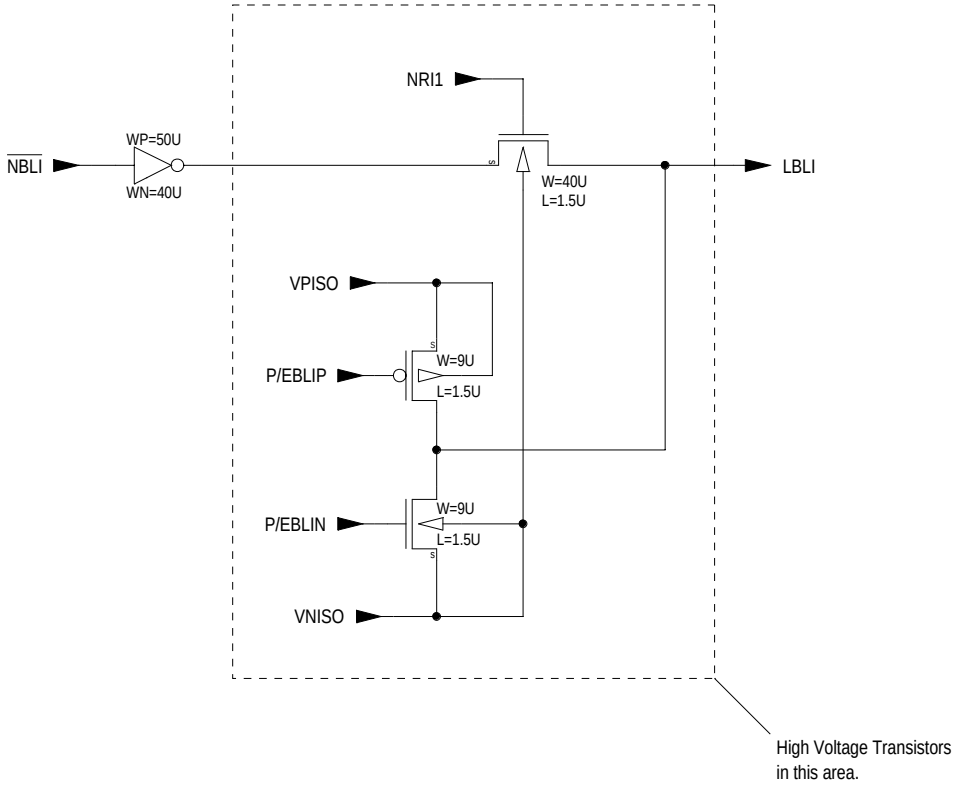


Figure 4.14.3 WORDLINE DRIVER AND BLOCK SELECT FOR BOTTOM SINGLE FLASH ARRAYS

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2G-P16	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:04		
LOCATION:	BLOCK_NAME	INITIALS:	GM



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	B2G-P17	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:05		
LOCATION:	BLOCK_NAME	INITIALS:	GM

Figure 4.14.4 SWITCH AND PRECHARGE

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

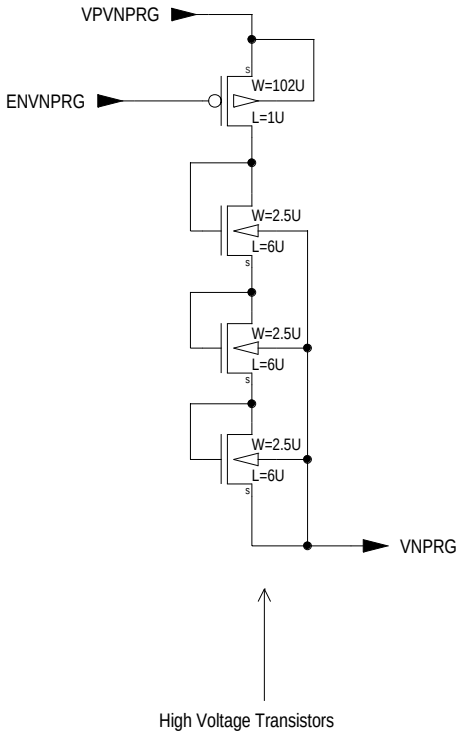


Figure 4.15 VOLTAGE GENERATOR

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	C1G-P02	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:13		
LOCATION:	BLOCK_NAME	INITIALS:	GM

5.0 RX Prescaler

The following section was taken from a frequency synthesizer report This particular device was manufactured with a BiCMOS process and the schematics therefore contain bipolar transistors.

The RX Synthesizer Prescaler is a separate layout block that implements Emitter Coupled Logic (ECL) logic. ECL gates and flip-flops utilize only BiPolar NPN transistors. ECL Divider flip-flops are individually tuned, accordingly to operating frequency, to minimize power consumption. Individual tuning is achieved by selecting the appropriate length of polysilicon emitter and collector resistors. The Prescaler schematic is shown in Figure 5.

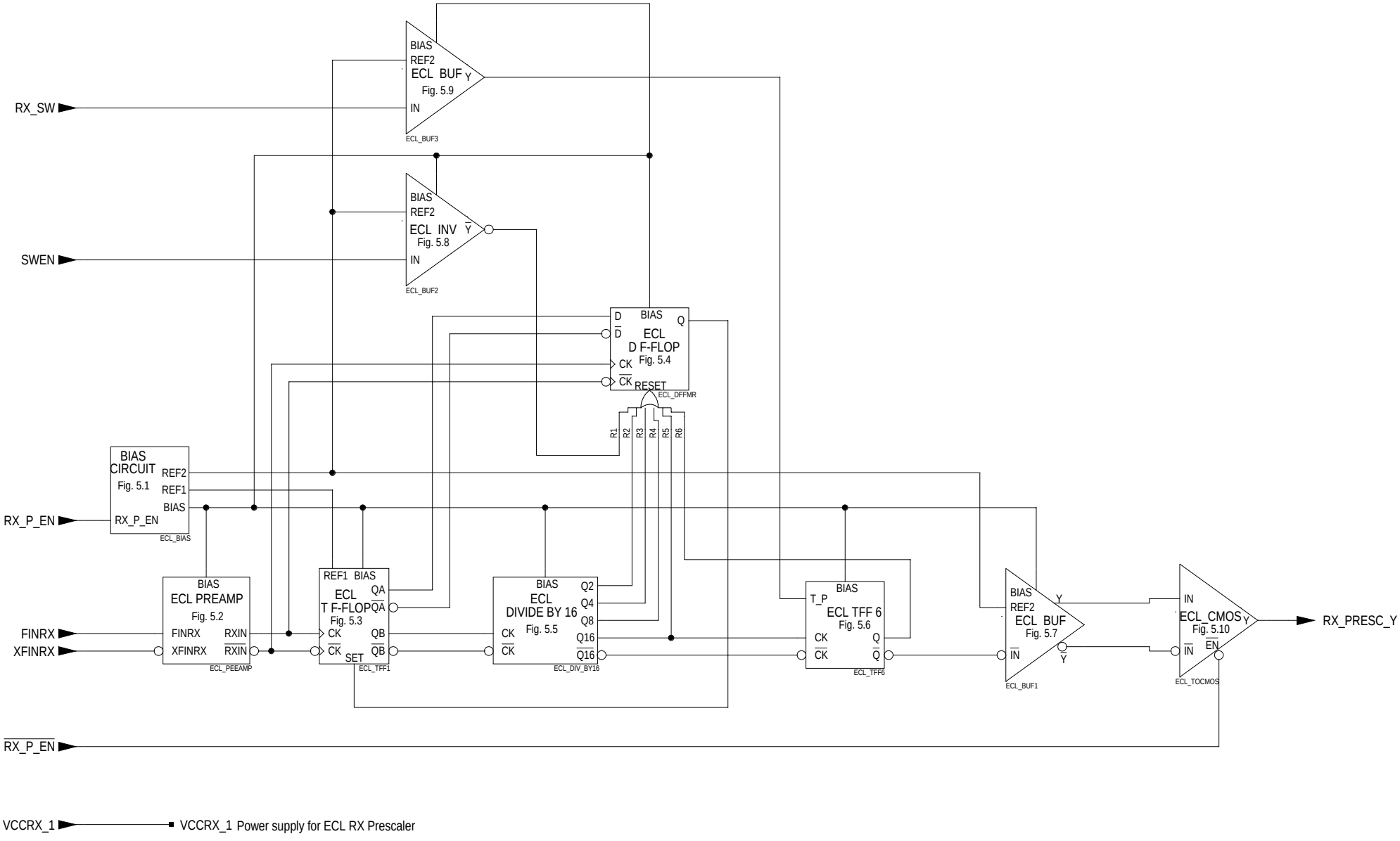
The input frequency FINRX goes through a differential pre-amplifier to form RXIN and ~RXIN complementary clocks. The divide ratio of the Prescaler (32/64) is set with the RX_SW input. The RX_SW signal controls the Toggle_Pass (T_P) input of the flip flop in Figure 3.6. The clock swallow is controlled with the SWEN input. When SWEN = 0, the divide ratio of the Prescaler is 32 or 64. When SWEN = 1, the Prescaler swallows one clock pulse, after an "all zeros" state, and the resulting divide ratio becomes 33 or 65.

The ECL to CMOS converter layout (Figure 5.10) is not located in the Prescaler block but in the RX Counters Standard Cells block. All Prescaler circuits are supplied from the upper $Vcc_{RX}(1)$ pad, except for the ECL_CMOS converter and the entire RX Standard Cell block which are supplied from the bottom $Vcc_{RX}(2)$ pad. Both Vcc_{RX} pads are bonded to a common package pin.

As seen on the Prescaler schematics the BiPolar NPN transistors have an attached AREA attribute. Only two types of BiPolar NPN transistors are used in the design. The smaller one (Type 1) has an AREA = 1 or is left without an AREA attribute on the schematics. The larger transistors (Type 2) have an AREA = 2. If an NPN transistor on a schematic has an attribute of AREA = 4 it is a parallel connection of two Type 2 transistors.

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

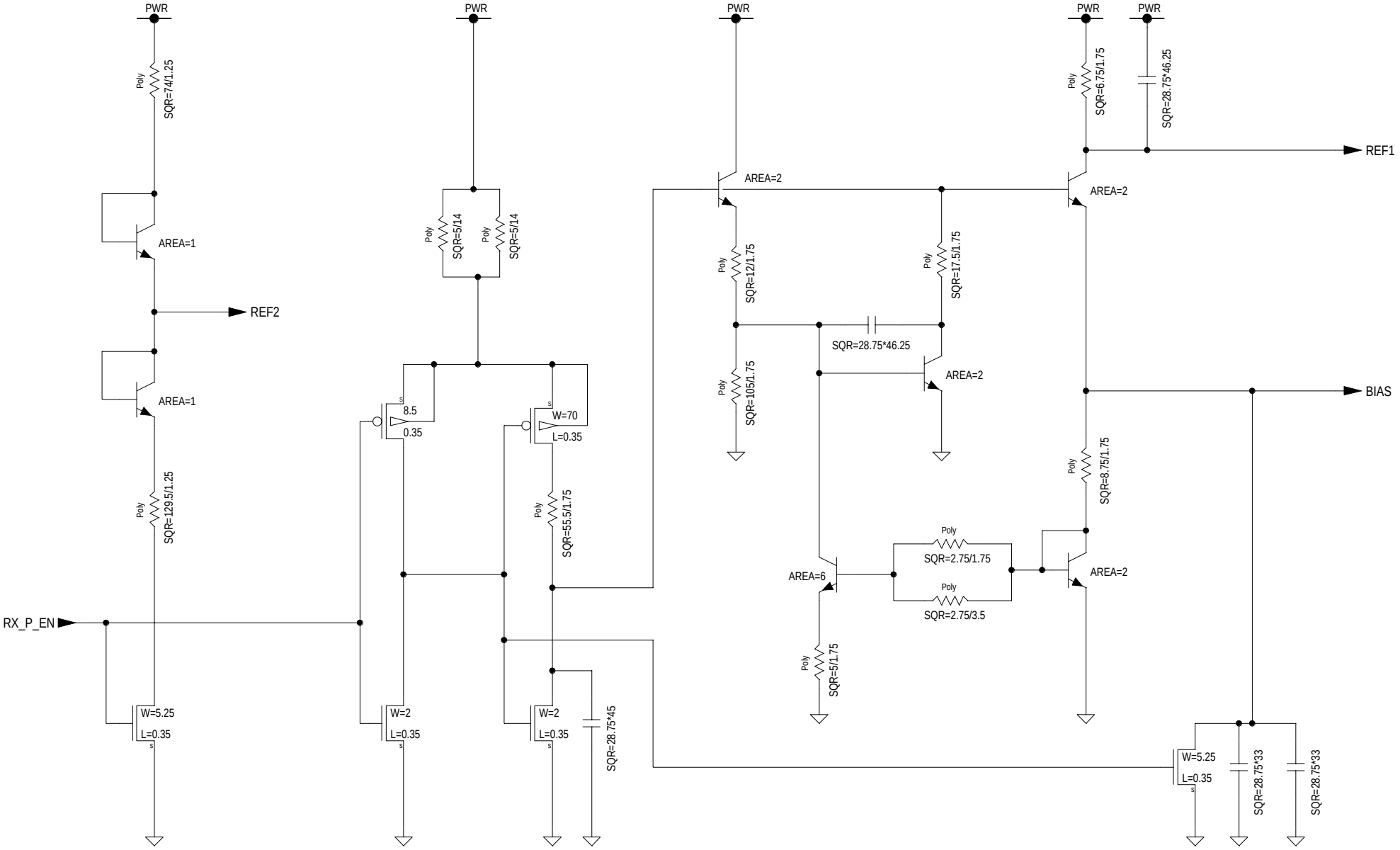
3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	RX_PRESCALER	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:13		
LOCATION:	XX	INITIALS:	GY

Figure 5.0 RX ECL DIVIDE BY 32/33 OR 62/63 PRESCALER

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	ECL_BIAS	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:13		
LOCATION:	XX	INITIALS:	GY

Figure 5.1 BIAS AND REFERENCE VOLTAGES FOR ECL PRESCALER

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

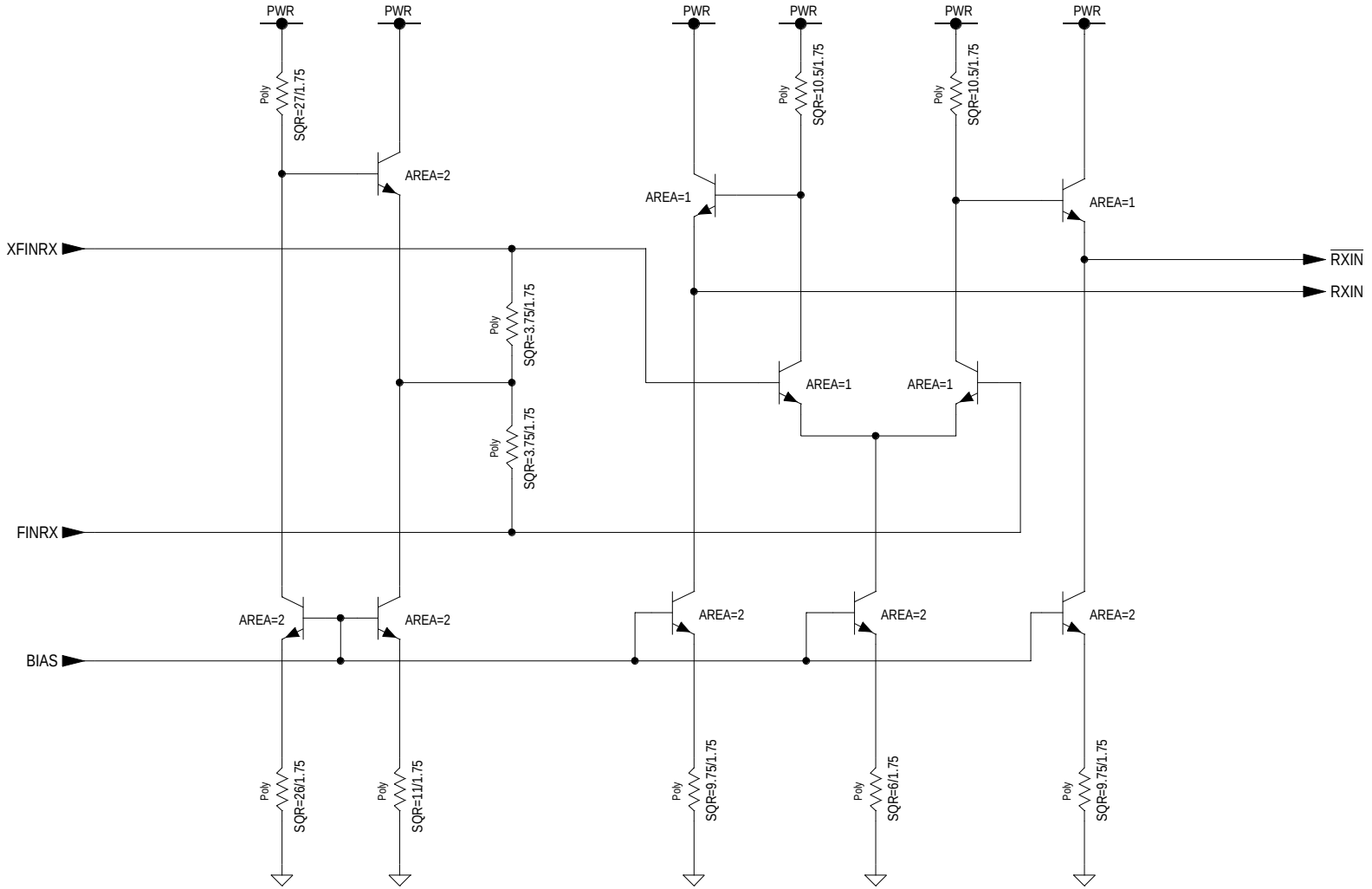
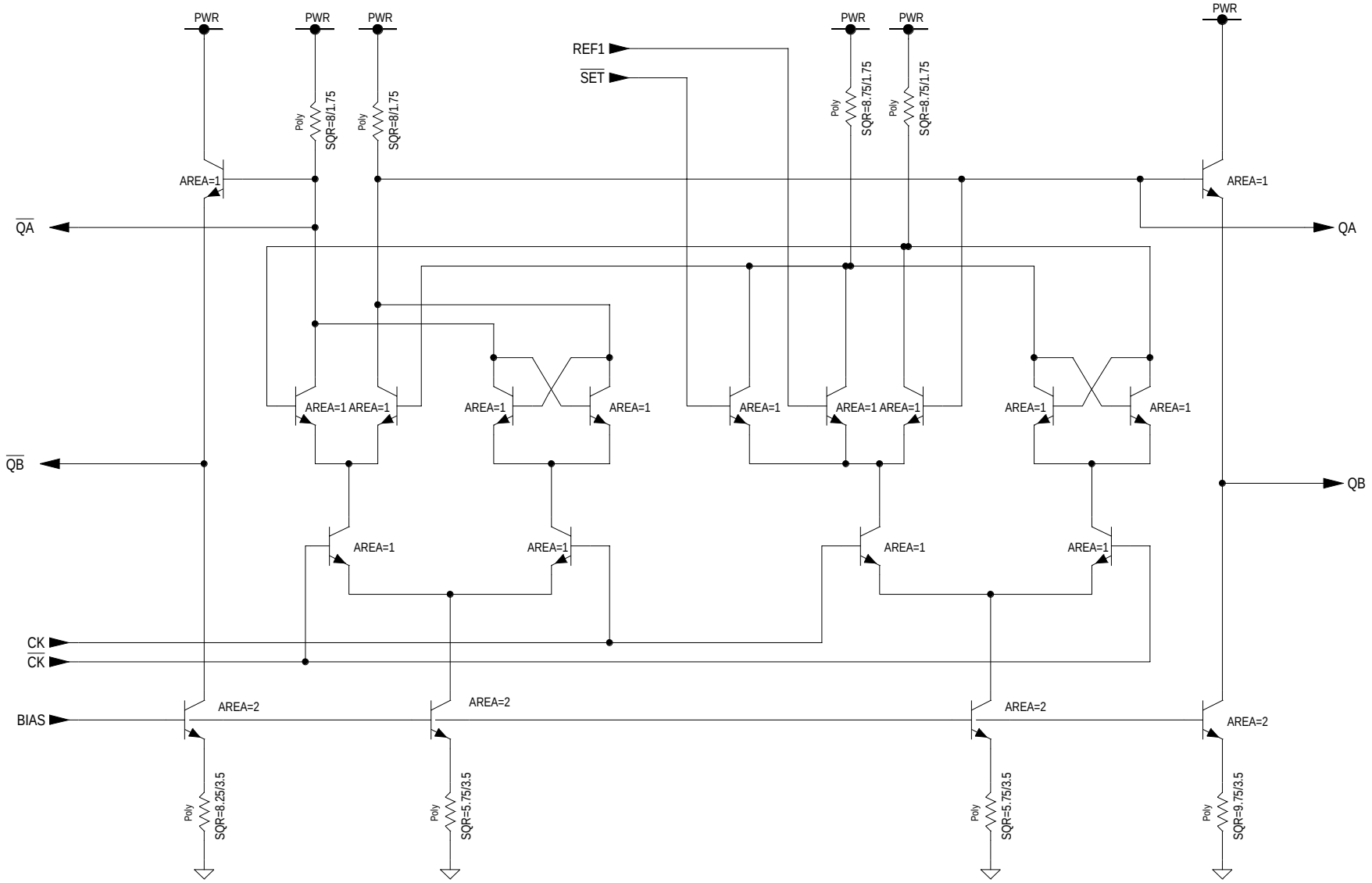


Figure 5.2 RX INPUT PRE-AMPLIFIER

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

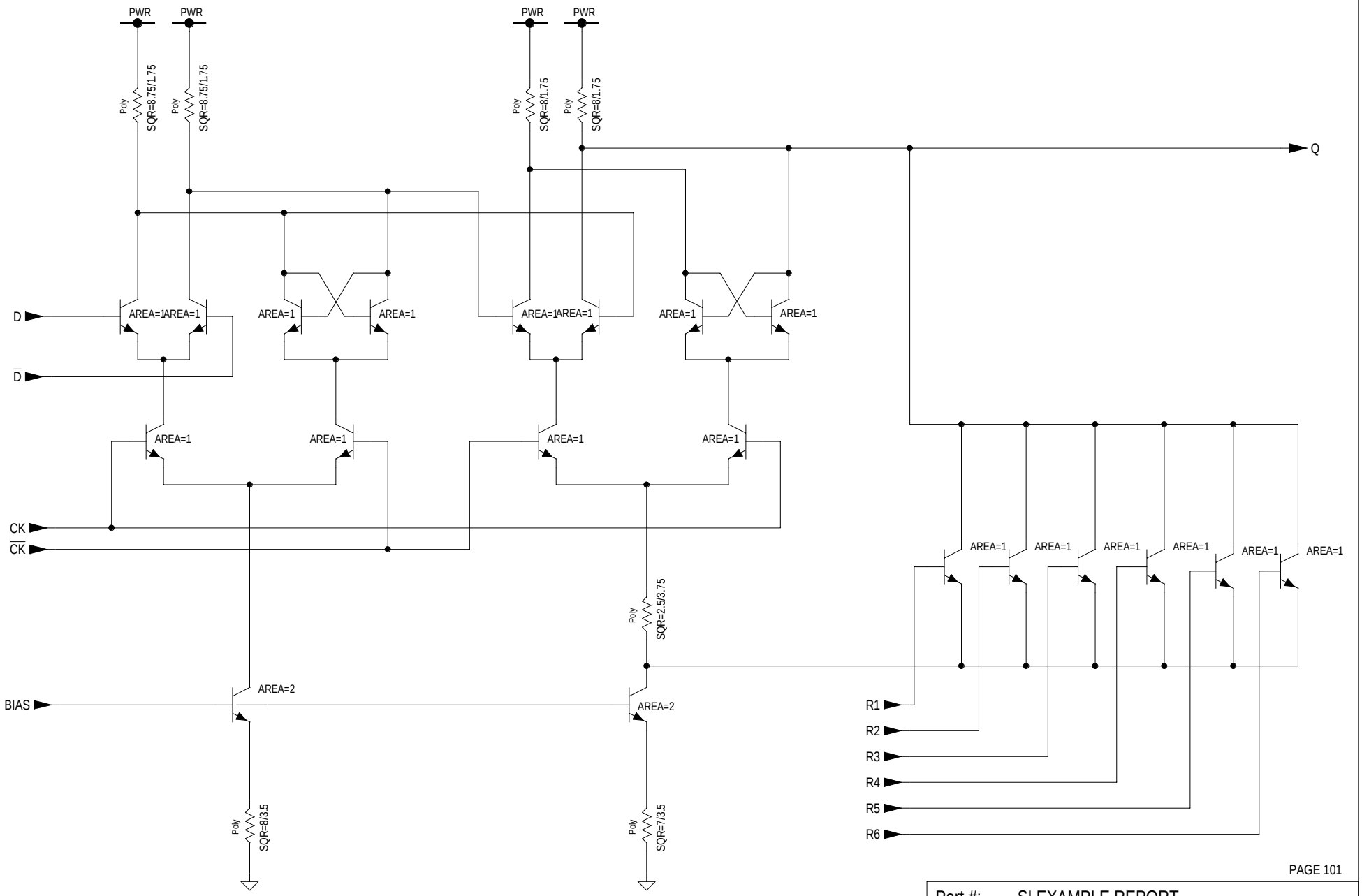
Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	ECL_PREAMP	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:14		
LOCATION:	XX	INITIALS:	GY



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	ECL_TFF1	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:05		
LOCATION:	XX	INITIALS:	GY

Figure 5.3 ECL - T FLIP-FLOP WITH RESET

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



PAGE 101

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	ECL_DFFMR	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:14		
LOCATION:	XX	INITIALS:	GY

Figure 5.4 ECL - D FLIP-FLOP WITH MULTI-INPUT RESET

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

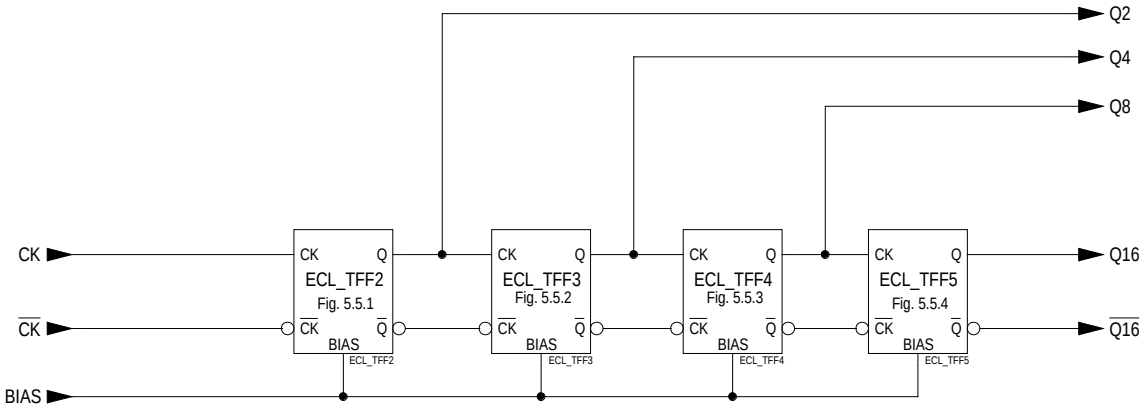
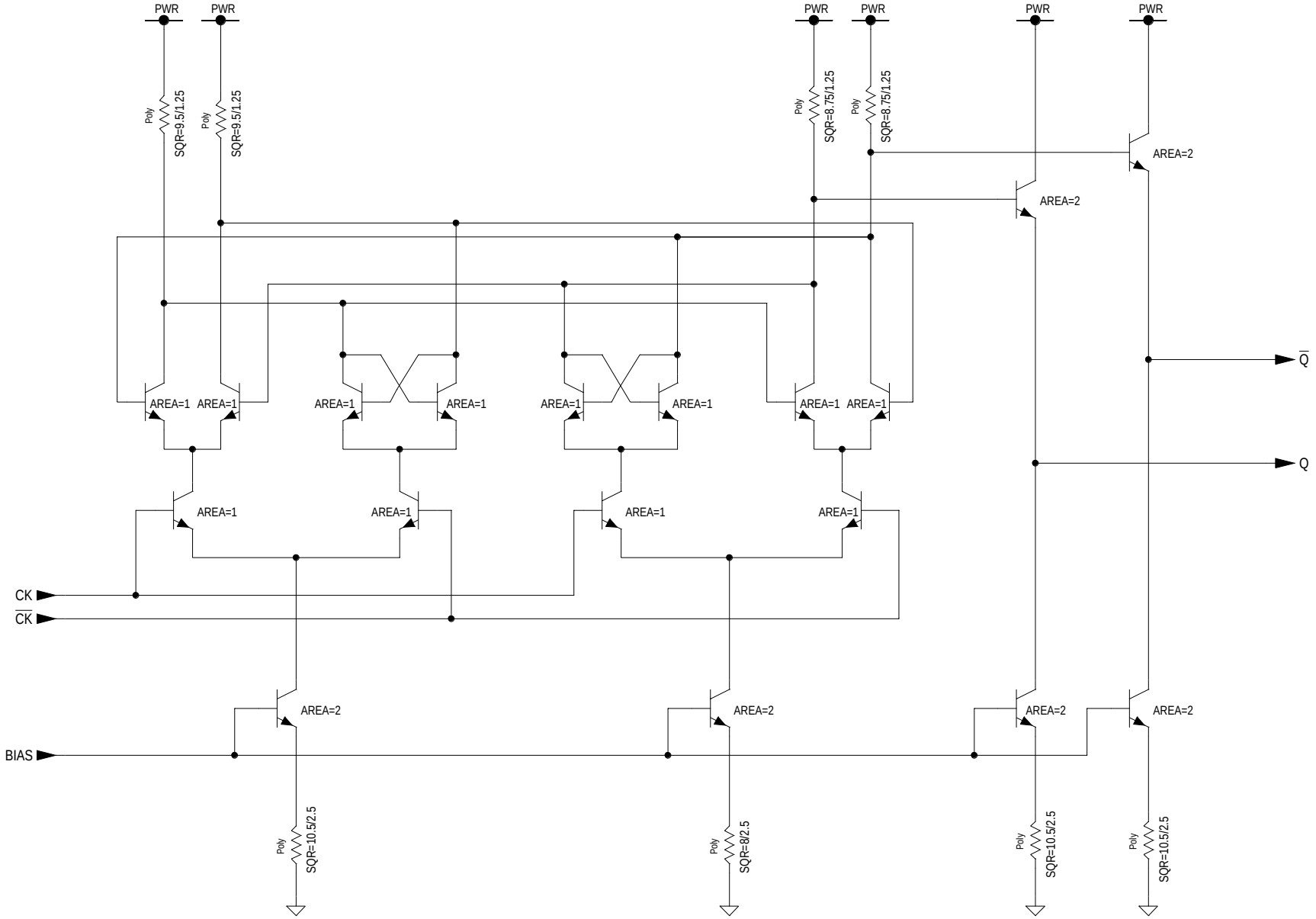


Figure 5.5 ECL PRESCALER DIVIDE BY 16 SECTION

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

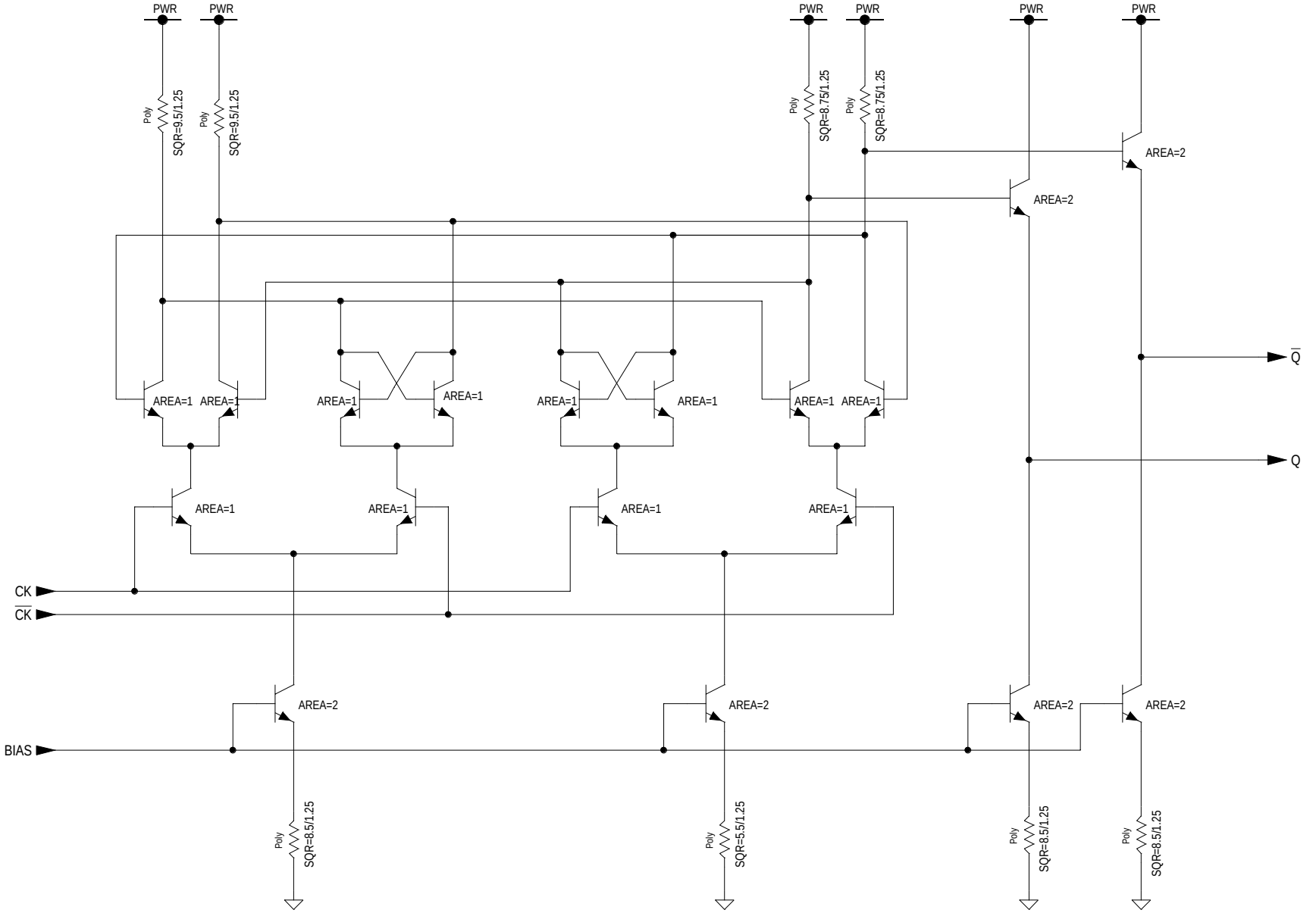
Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	ECL_DIV_BY16	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:14		
LOCATION:	XX	INITIALS:	GY



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	ECL_TFF2	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:14		
LOCATION:	XX	INITIALS:	GY

Figure 5.5.1 ECL - T FLIP-FLOP TYPE 2

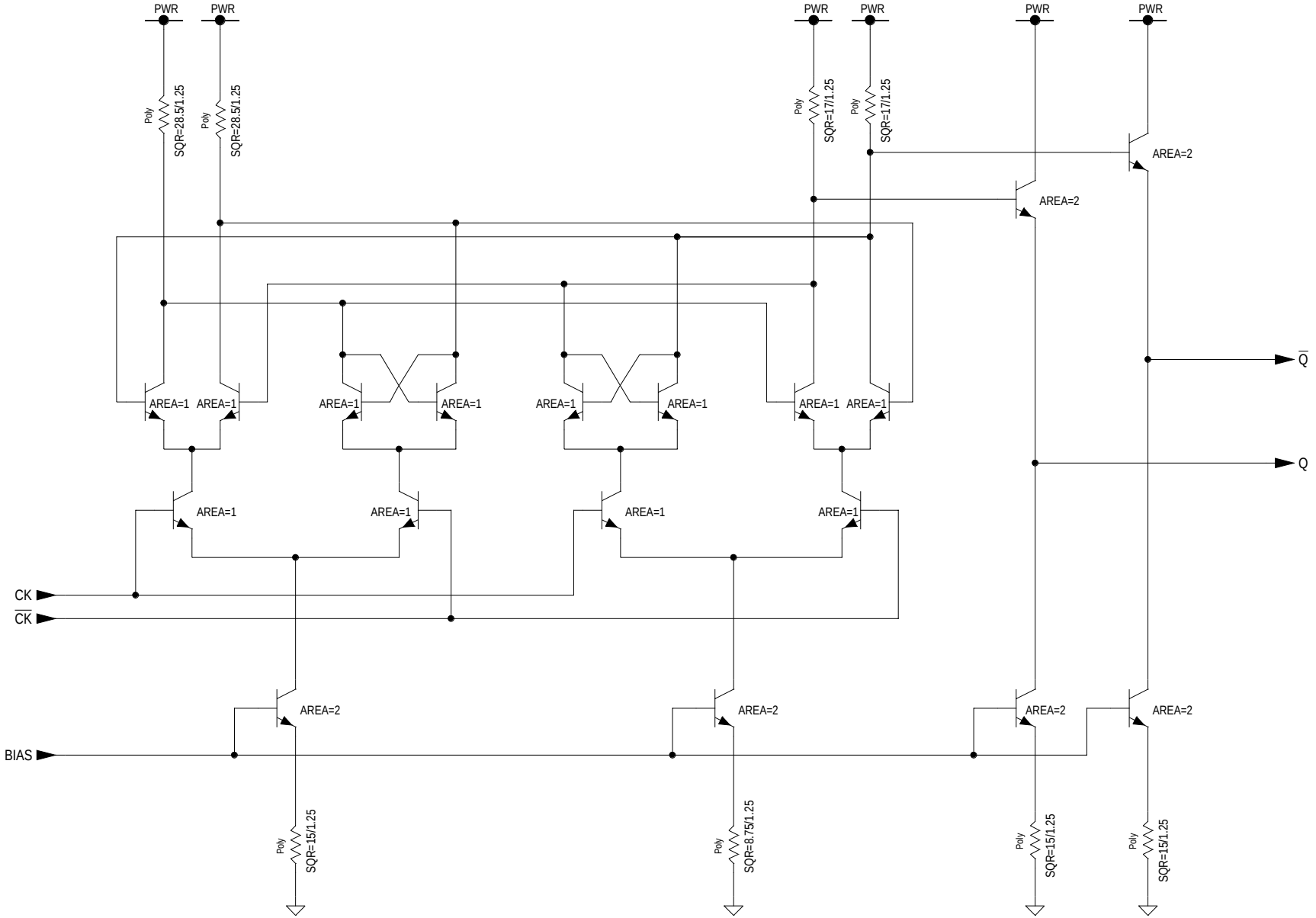
SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	ECL_TFF3	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:14		
LOCATION:	XX	INITIALS:	GY

Figure 5.5.2 ECL - T FLIP-FLOP TYPE 3

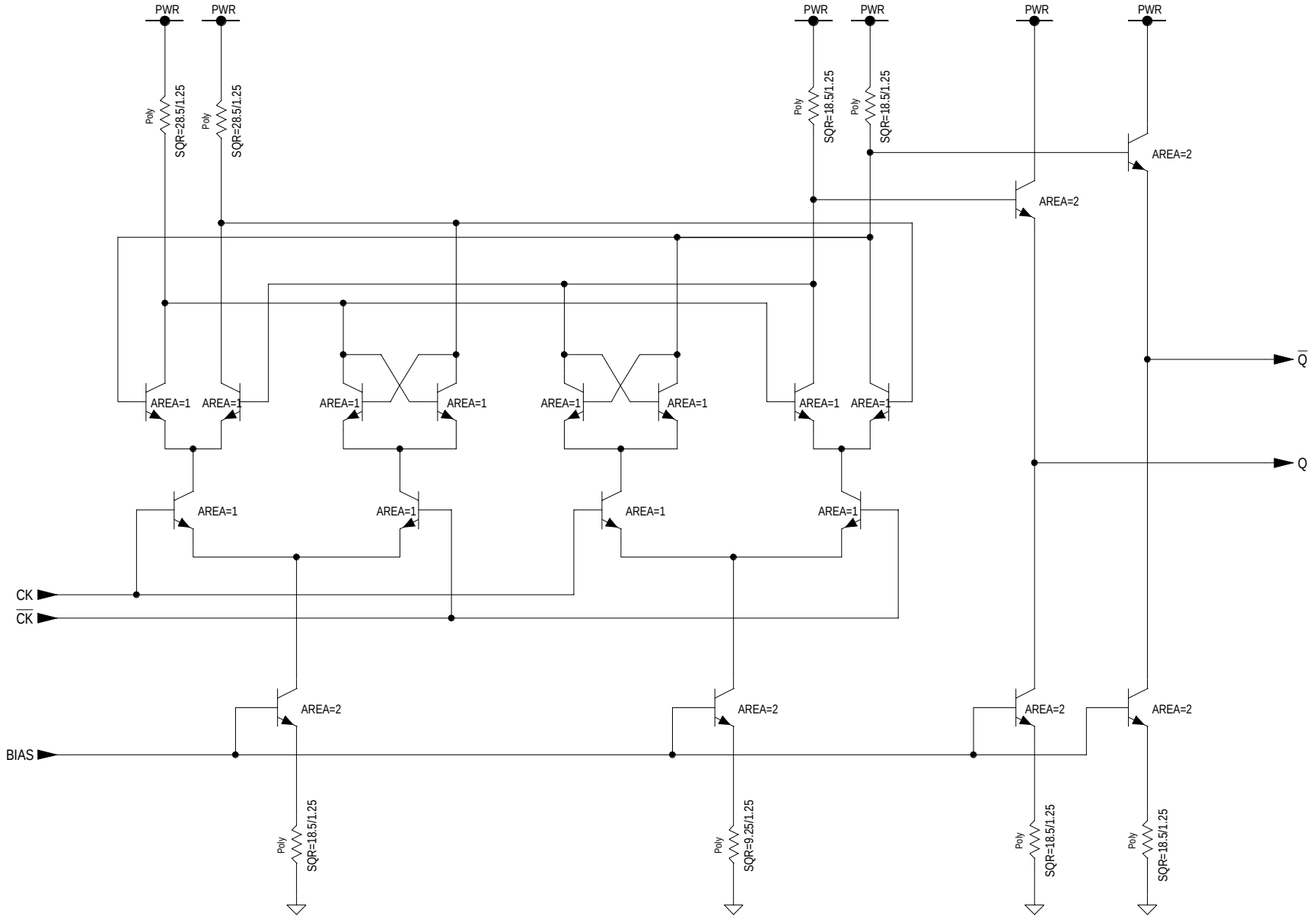
SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	ECL_TFF4	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:14		
LOCATION:	XX	INITIALS:	GY

Figure 5.5.3 ECL T FLIP-FLOP TYPE 4

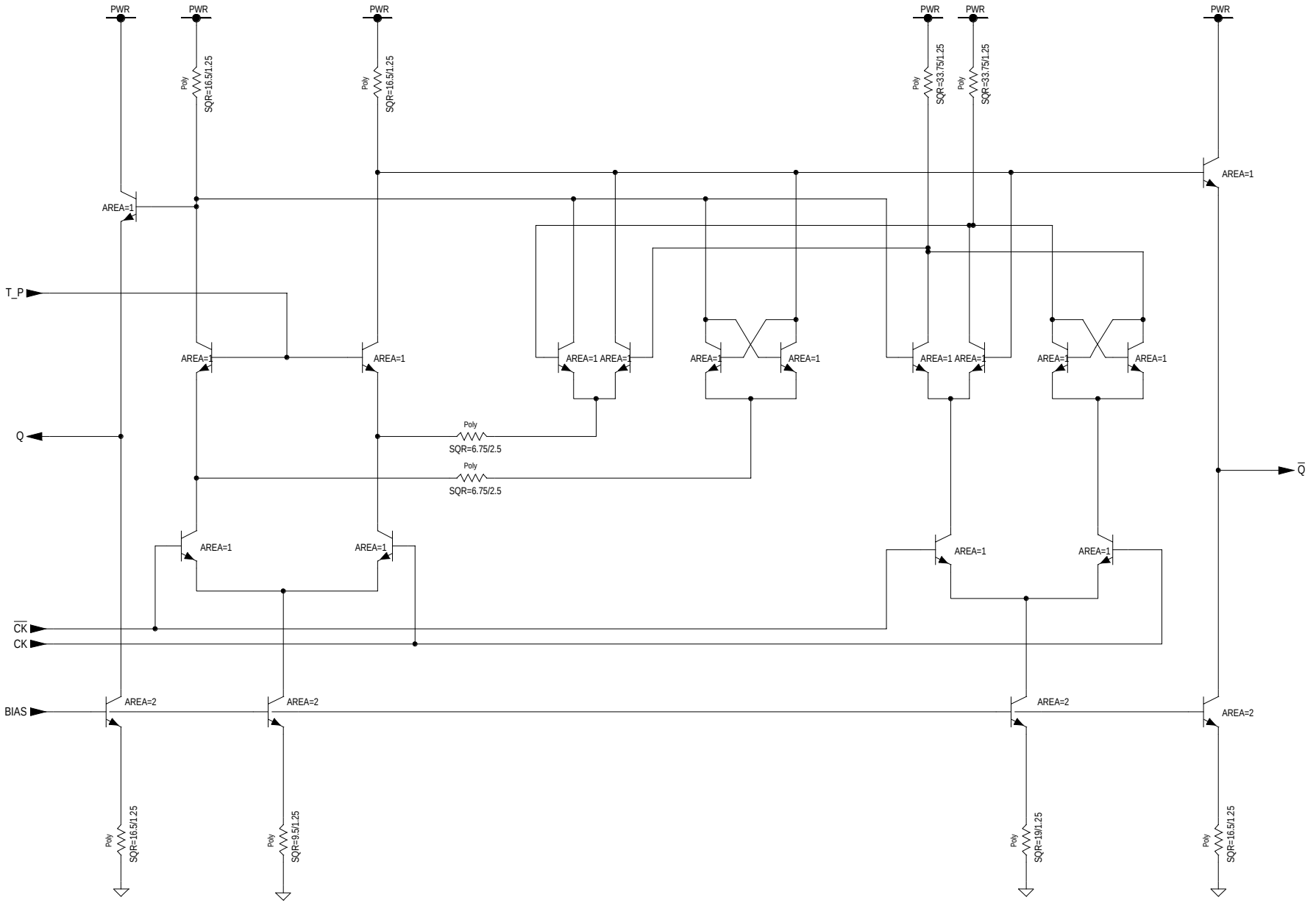
SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	ECL_TFF5	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:14		
LOCATION:	XX	INITIALS:	GY

Figure 5.5.4 ECL - T FLIP-FLOP TYPE 5

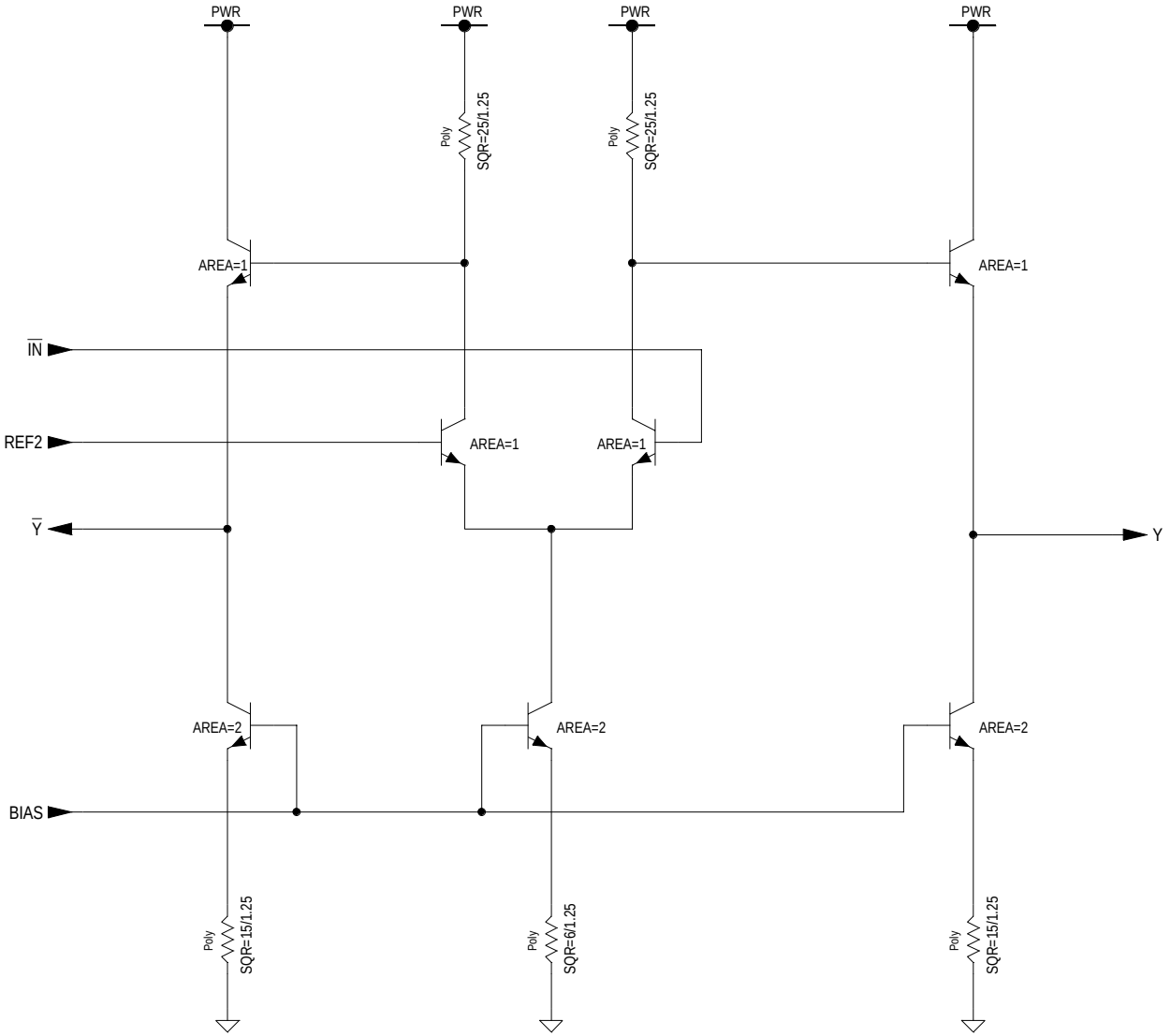
SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	ECL_TFF6	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:14		
LOCATION:	XX	INITIALS:	GY

Figure 5.6 ECL T FLIP-FLOP TYPE 6

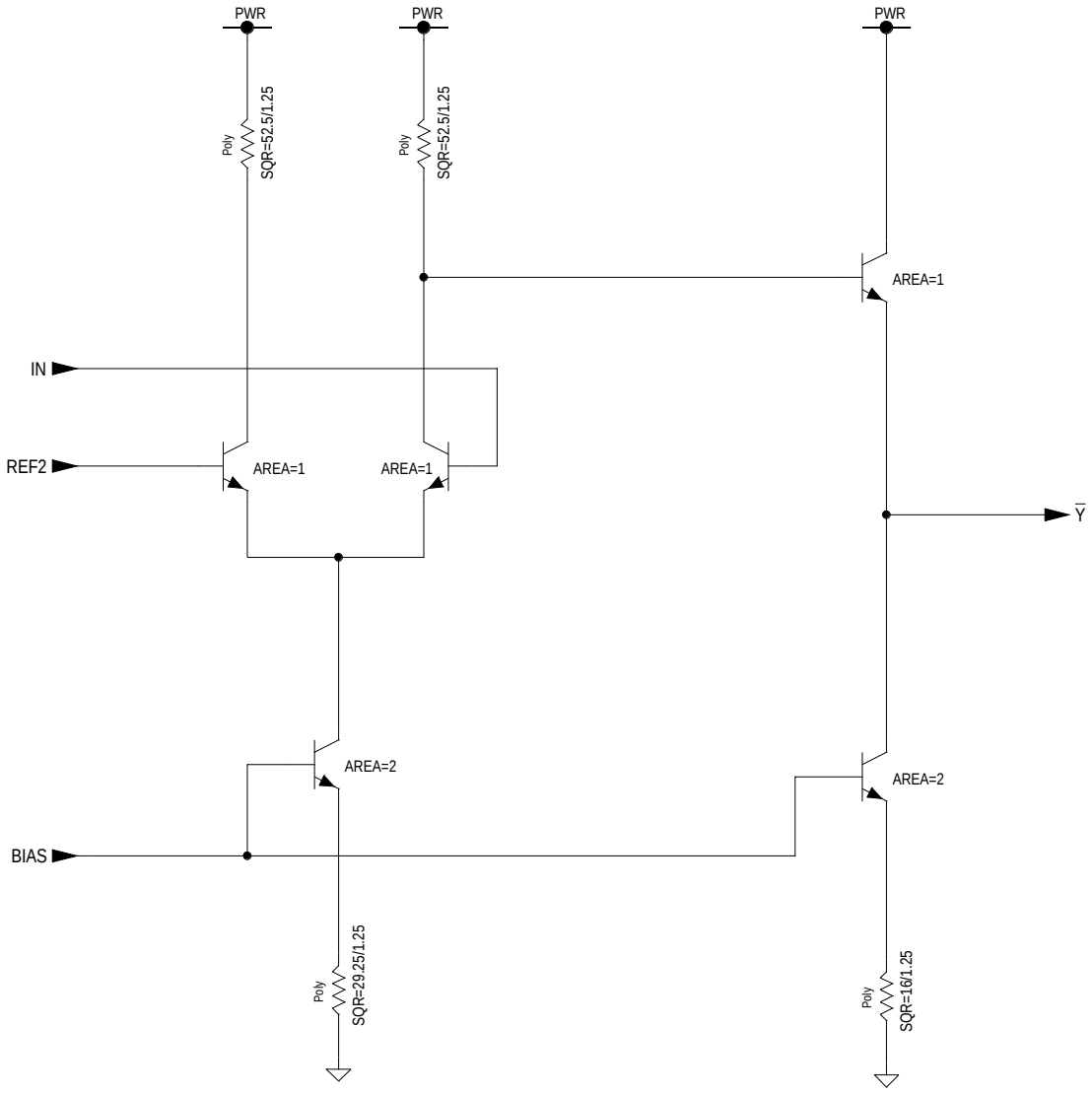
SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	ECL_BUF1	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:14		
LOCATION:	XX	INITIALS:	GY

Figure 5.7 ECL BUFFER TYPE 1

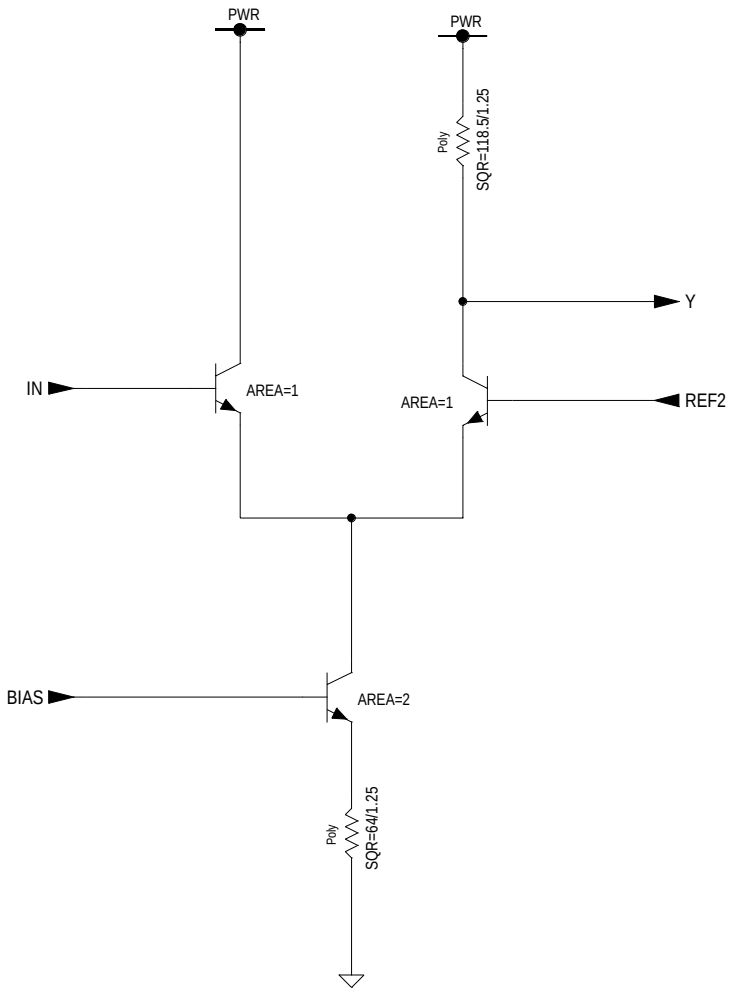
SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	ECL_BUF2B	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:05		
LOCATION:	XX	INITIALS:	GY

Figure 5.8 ECL INVERTER

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	ECL_BUF3	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:05		
LOCATION:	XX	INITIALS:	GY

Figure 5.9 ECL BUFFER TYPE 3

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

6.0 Phase Frequency Detector

The following section was taken from a frequency synthesizer report The analysis for this section included simulation results.

The Phase Frequency Detector (PFD) shown in Figure 6 is of conventional design methodology. Except for the Charge_Up (CU) and Charge_Down (CD) outputs, it generates the Phase Difference (~PHDIFF) signal, which is used to drive the Lock detector and Charge Pump & Fast Lock logic. The RX_FC input is used to control PFD operation, depending on external Voltage Controlled Oscillator (VCO) polarity. There are two types of VCOs. Type 1 increases output frequency with increasing control voltage and type 2 decreases output frequency with increasing control voltage. PFD timing is shown in Diagram 6.1.

The PFD logic includes a small delay in the CU and CD flip-flop Reset path. This delay ensures the generation of short compensating pulses that prevent the Phase Lock Loop (PLL) from entering the "dead zone" and eliminates crossover distortion. Diagram 6.2 shows the compensating pulses. For this simulation all gate delays were set to 0.3 ns.

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

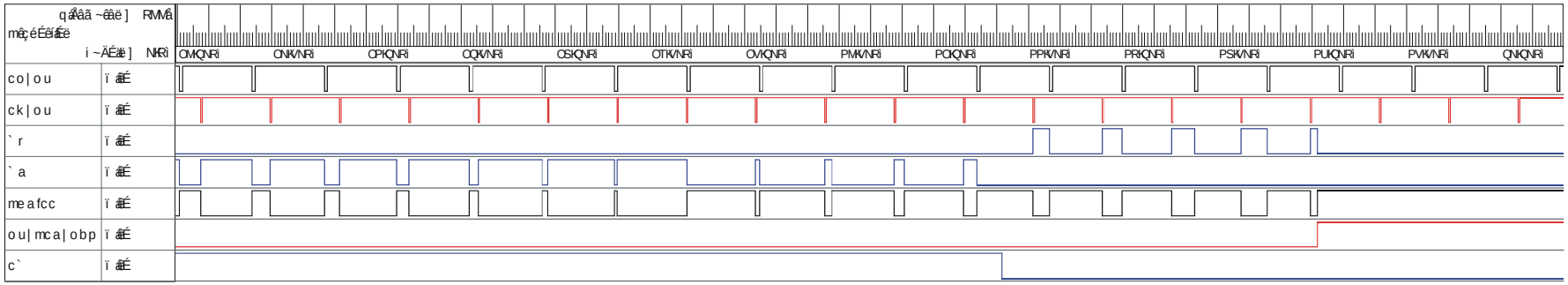


Diagram 6.1: Phase Frequency Detector timing.

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

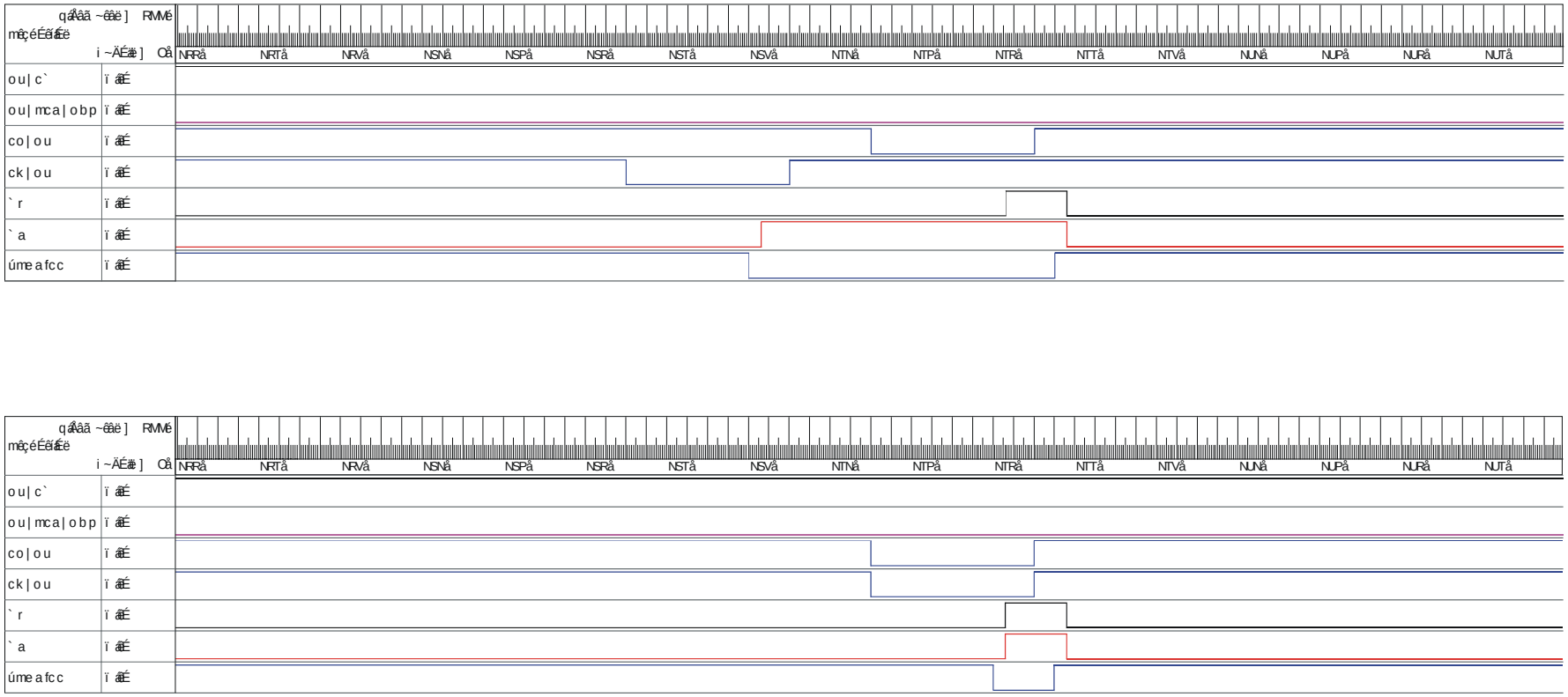
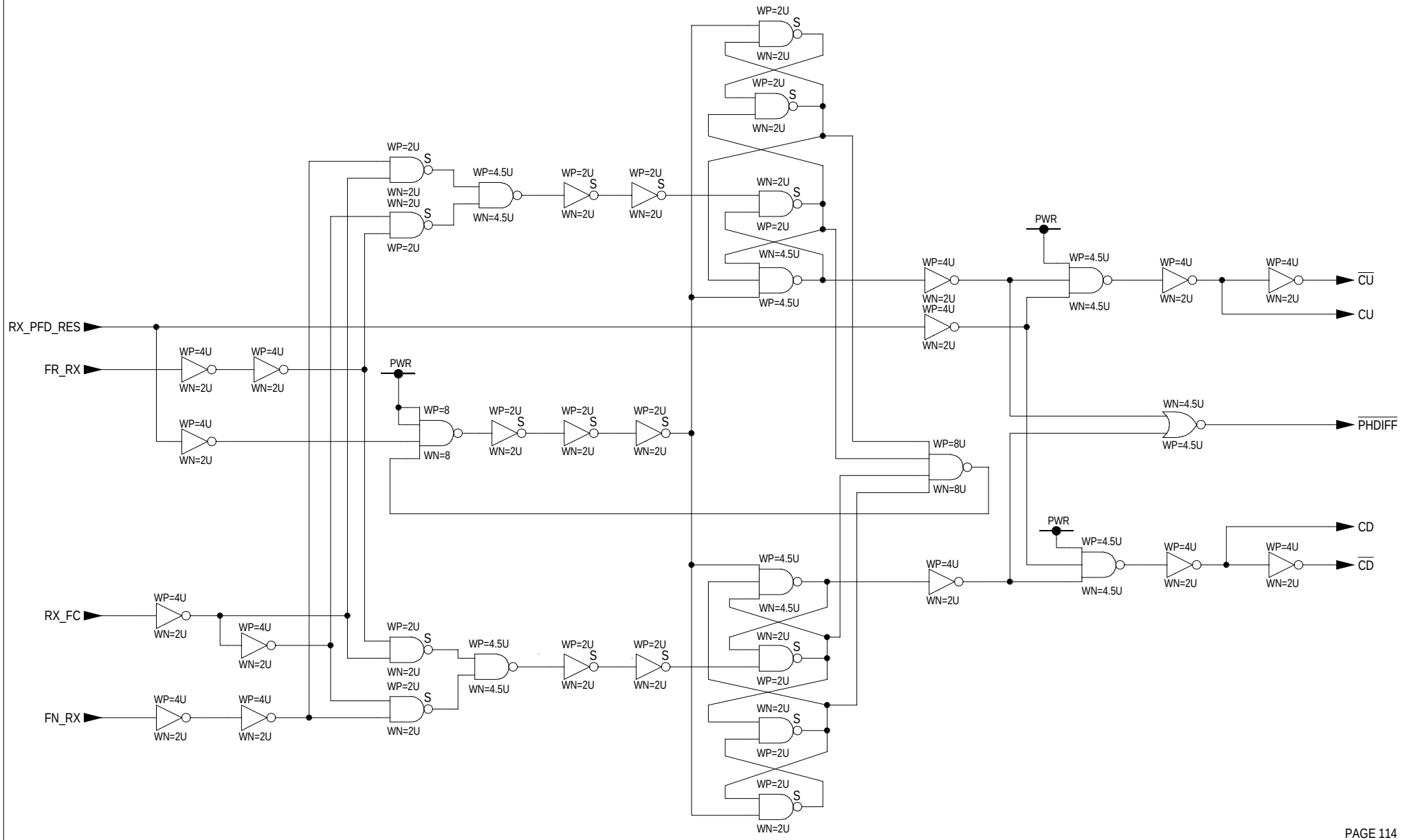


Diagram 6.2: PFD detailed timing.

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	PHDETECTOR	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:05		
LOCATION:	XX	INITIALS:	GY

Figure 6.0 PHASE / FREQUENCY DETECTOR

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

7.0 ADC Converter

The following section was taken from an mixed signal device and consists of a portion of the analog to digital converter.

The SI Example IC ADC schematic is found in Figure 7.0 contained in Section 7. The ADC has a pipelined nine-stage architecture. The first stage comprises a 2½ bit flash converter and a residue amplifier. The end stage is also a two and half bit flash converter. The ADC can be configured as a 12bit converter, although it is specified as a 10 bit in the data sheet.

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

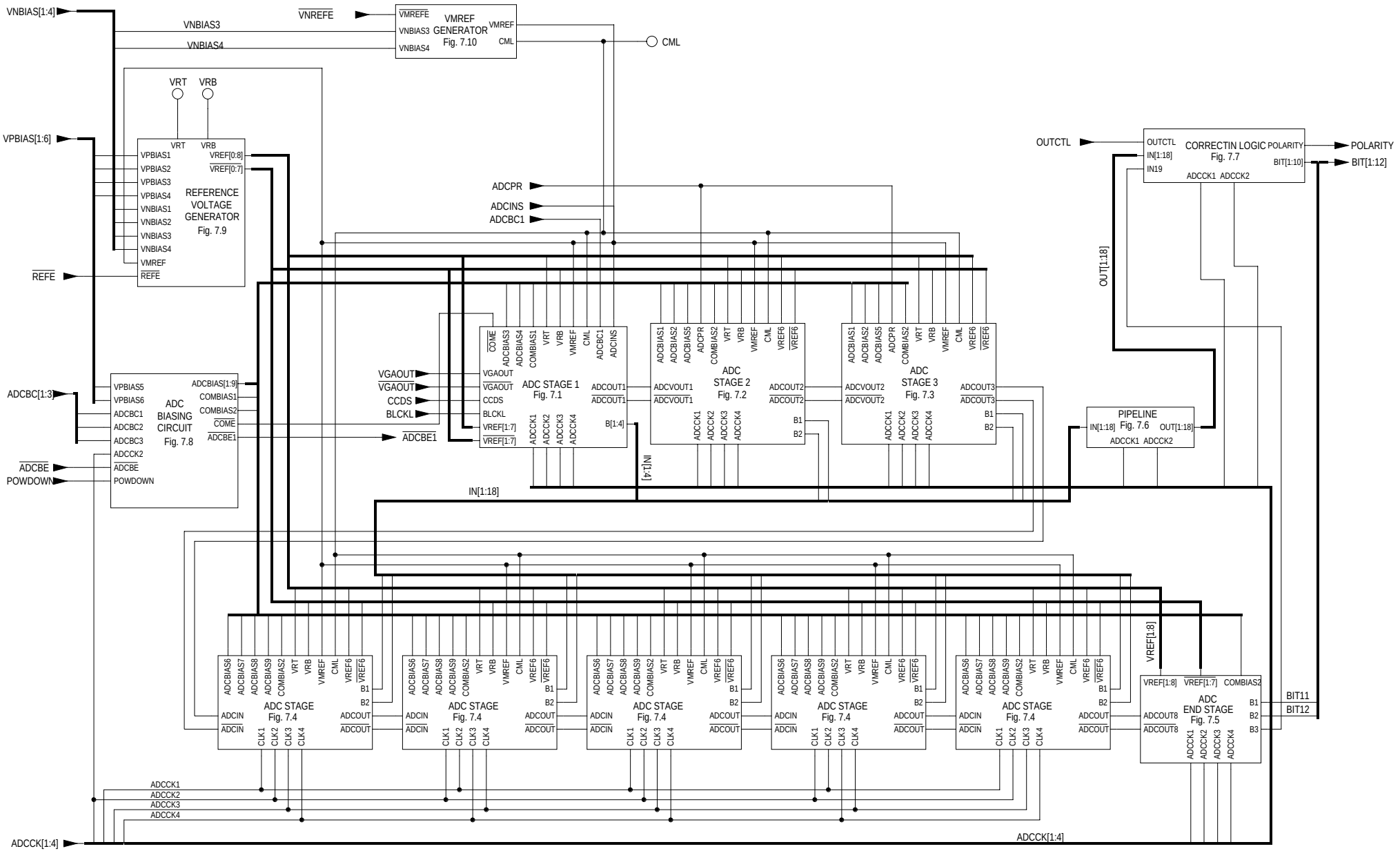
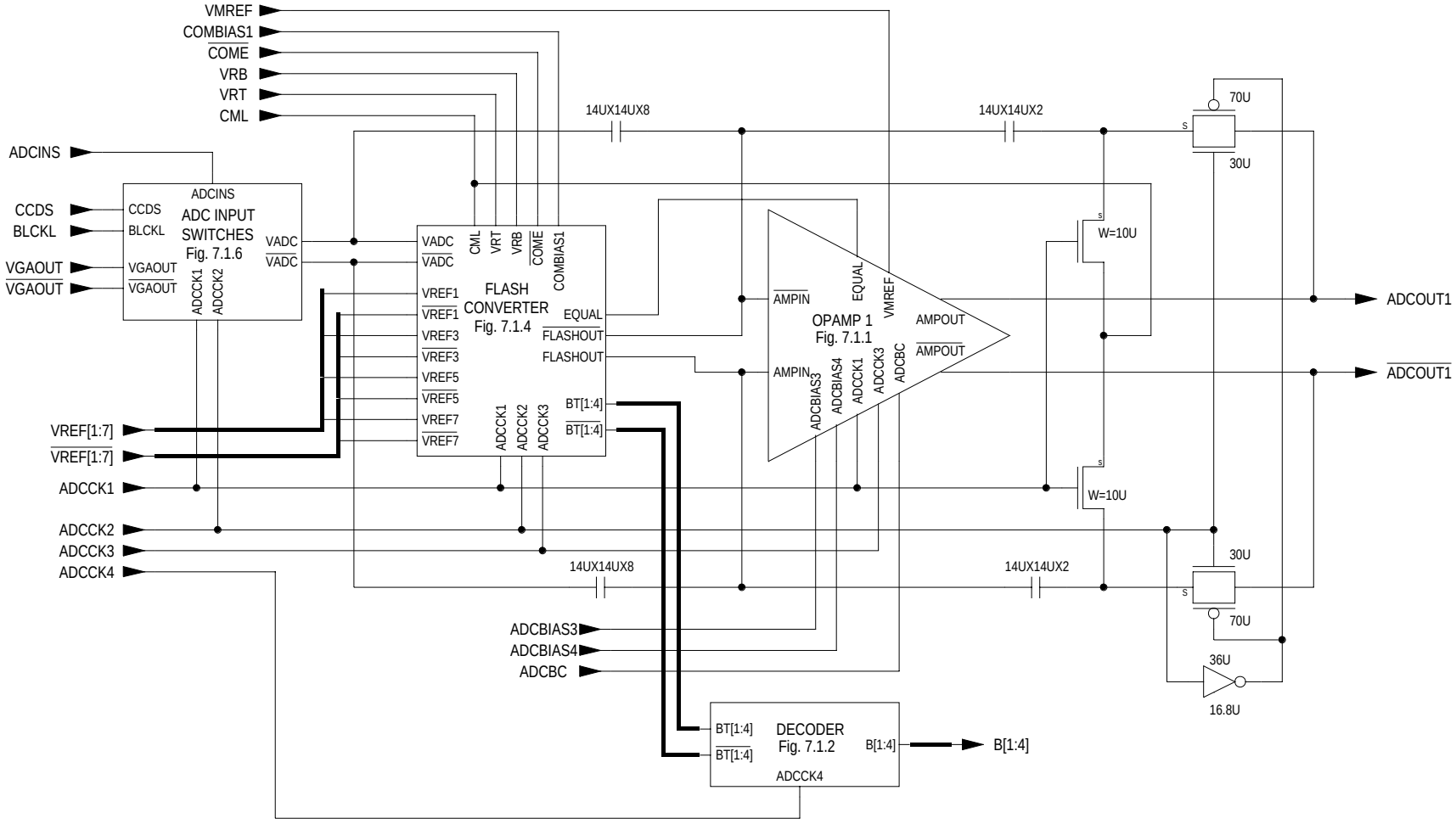


Figure 7.0 ADC

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	61	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:15		
LOCATION:	XX	INITIALS:	GY



PAGE 117

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	53	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:15		
LOCATION:	XX	INITIALS:	MH

Figure 7.1 ADV STAGE 1

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

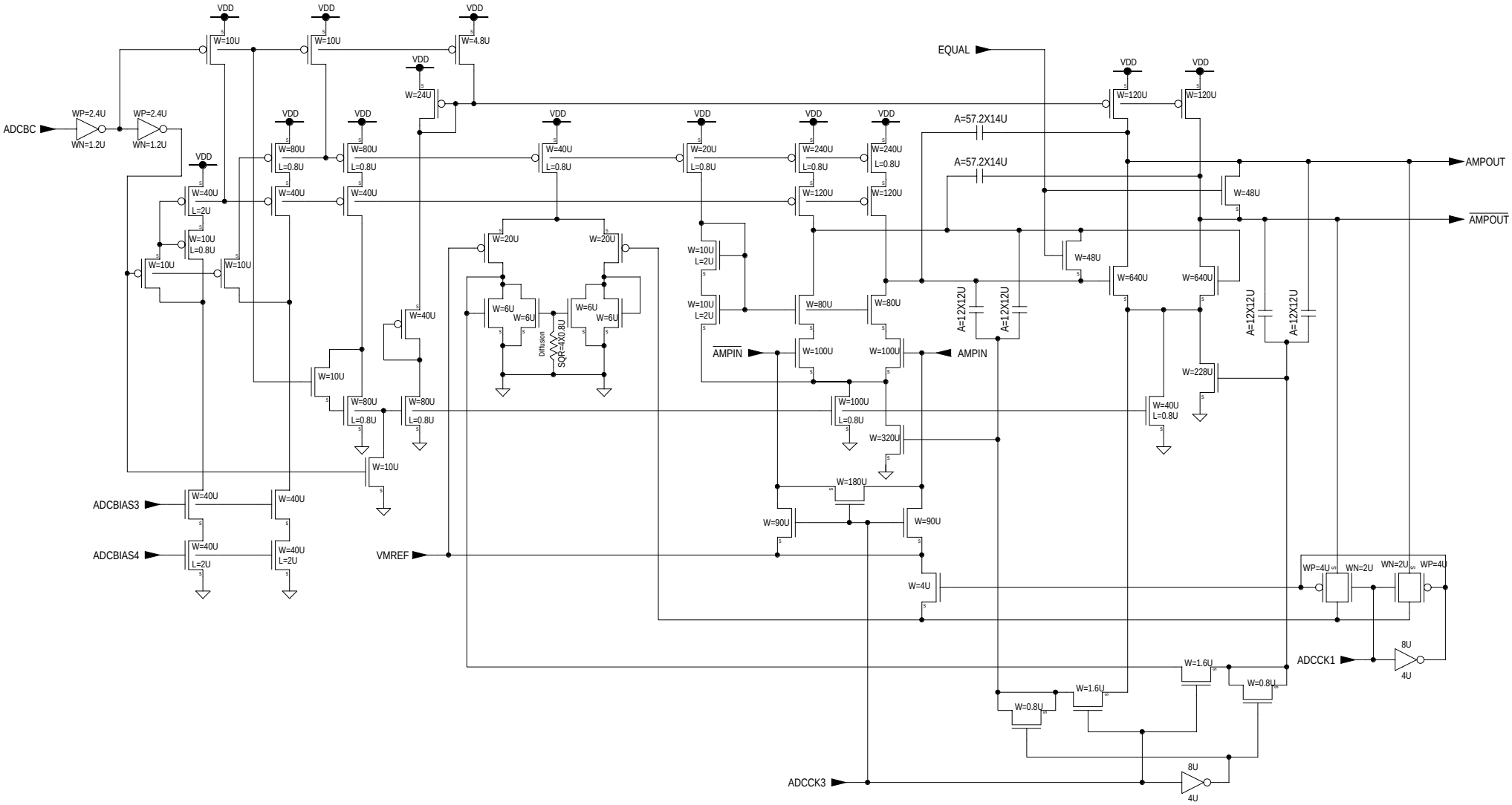


Figure 7.1.1 OPAMP1

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	52	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:15		
LOCATION:	XX	INITIALS:	MH

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

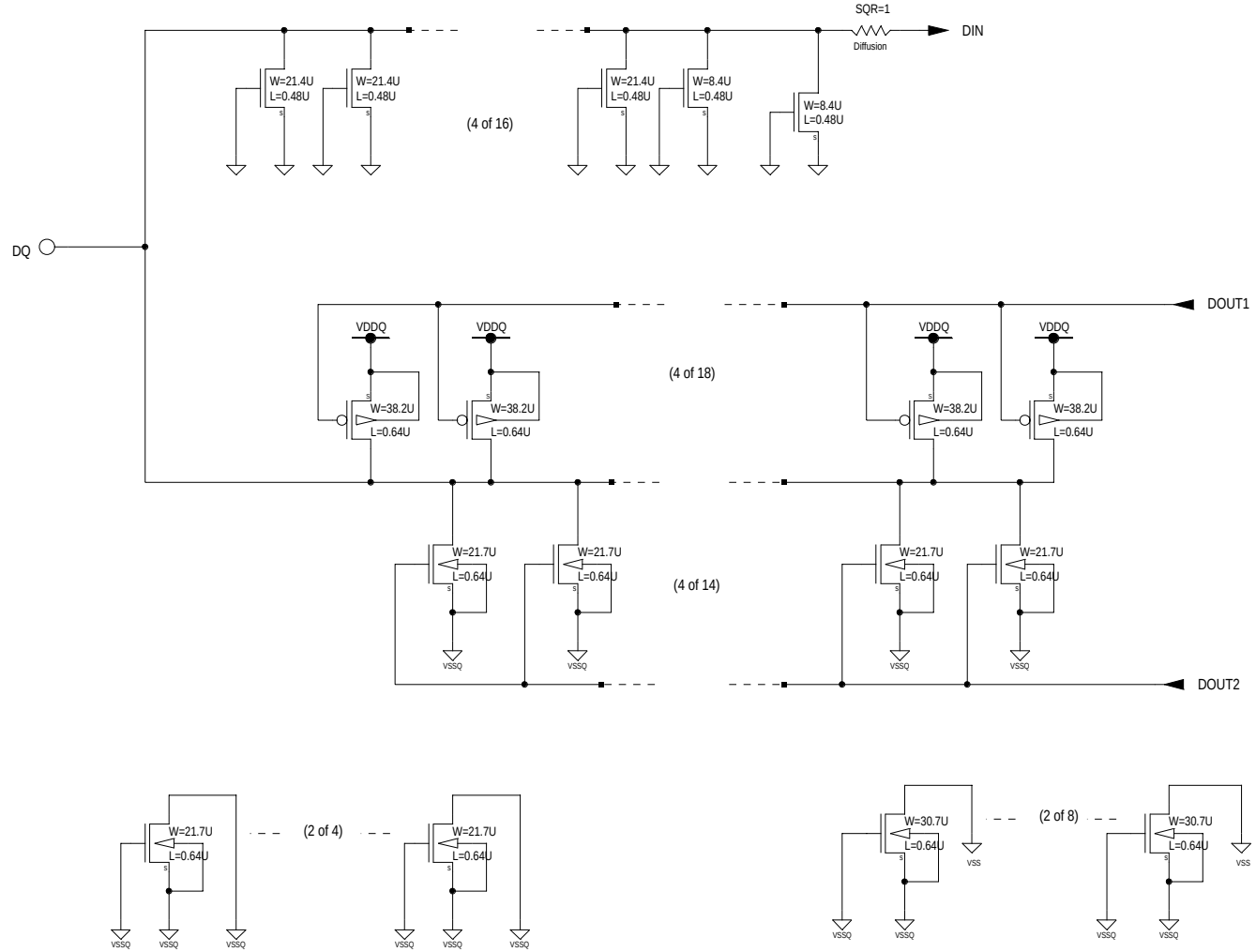


Figure 7.1.1.1 ESD PROTECTION - DQ PIN

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0031		
SCH_NAME:	ESD_DQ	SI NUMBER:	4967
DATE_TIME:	6-18-2002_9:15		
LOCATION:	XXX	INITIALS:	AZ, LW

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

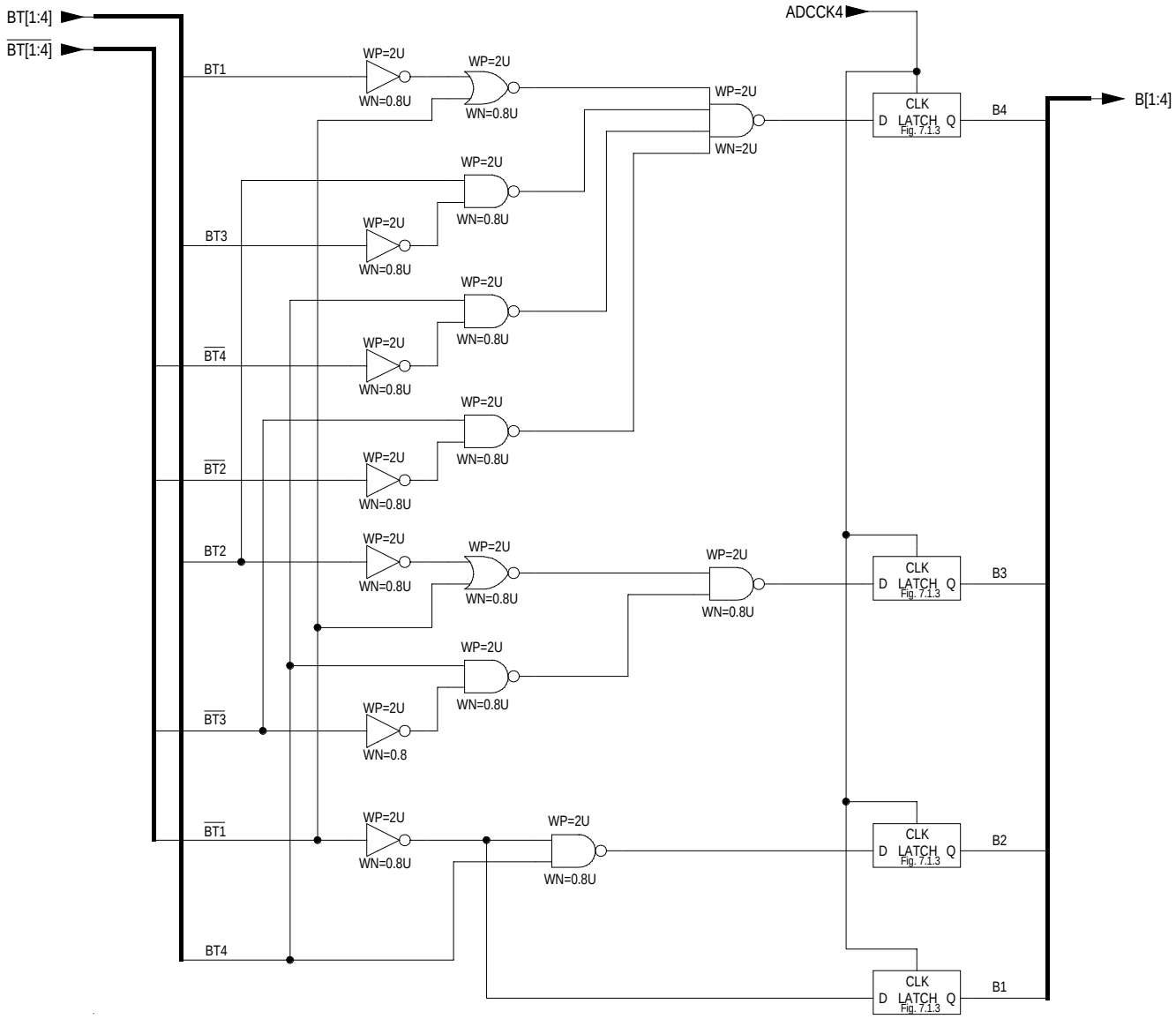


Figure 7.1.2 FLASH CONVERTER DECODER

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	51	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:05		
LOCATION:	XX	INITIALS:	MH

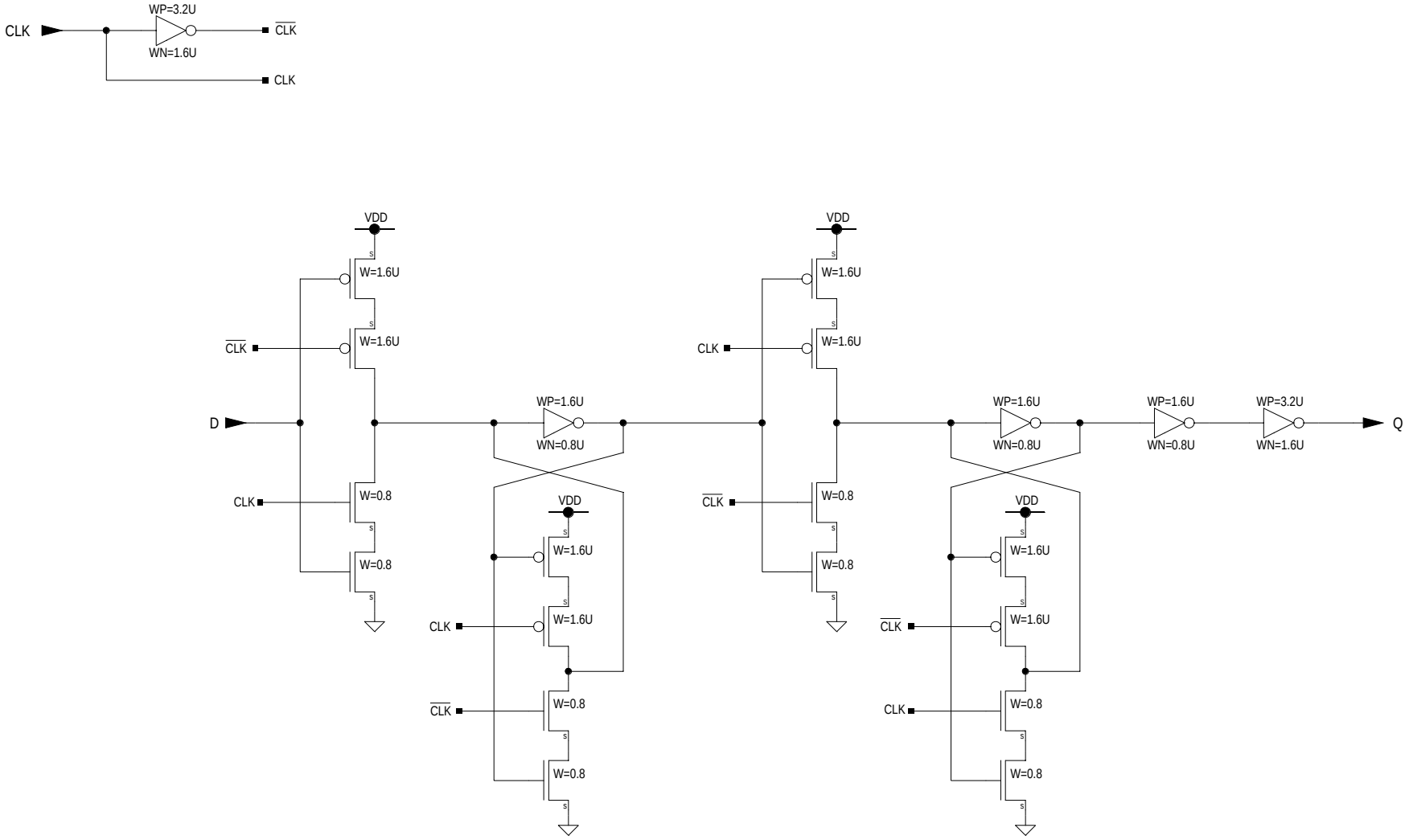


Figure 7.1.3 LATCH 1

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	50	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:05		
LOCATION:	XX	INITIALS:	MH

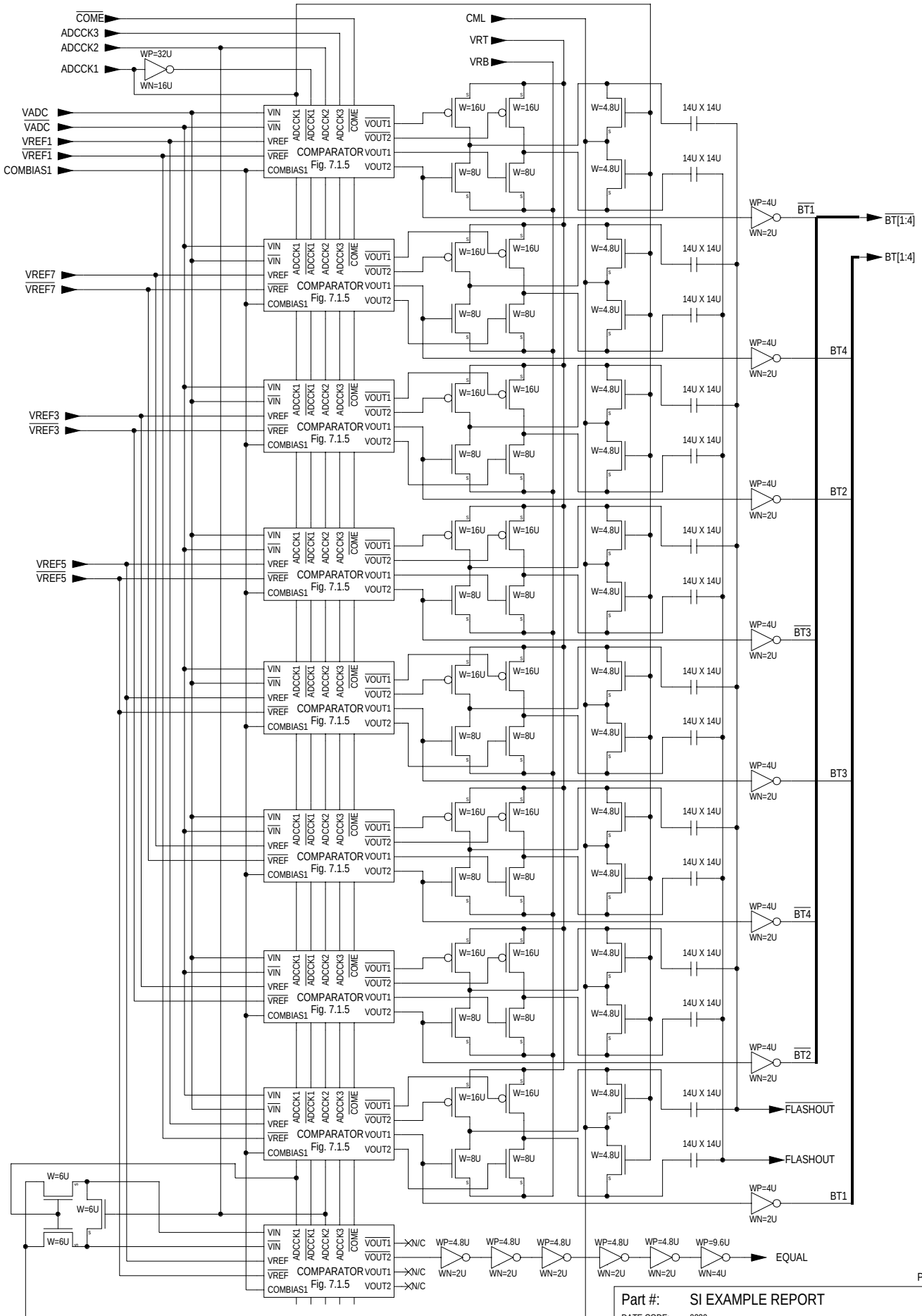


Figure 7.1.4 FLASH CONVERTER

PAGE 122

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	49	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:05		
LOCATION:	XX	INITIALS:	MH

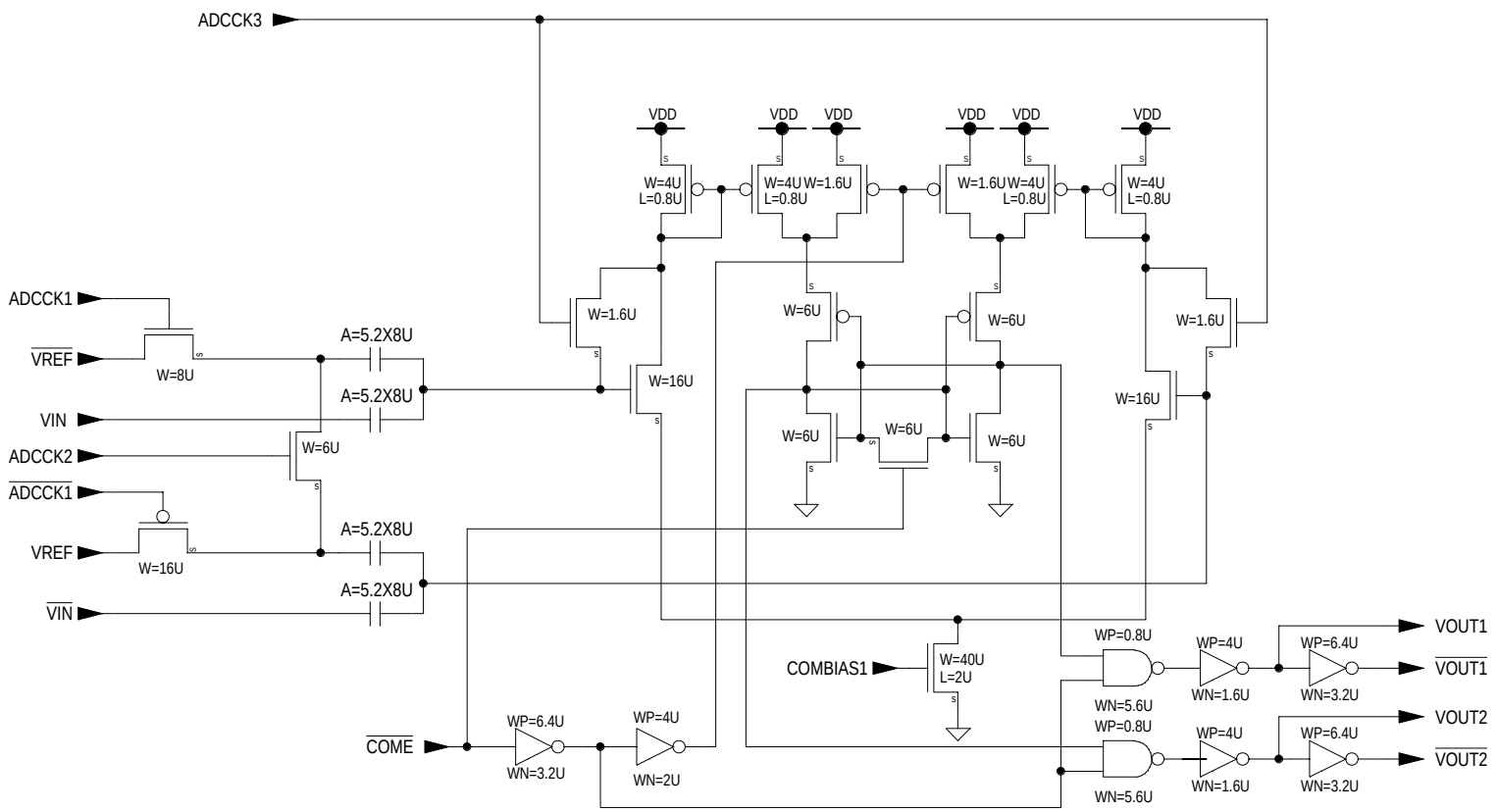


Figure 7.1.5 COMPARATOR 1

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	48	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:22		
LOCATION:	XX	INITIALS:	MH

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

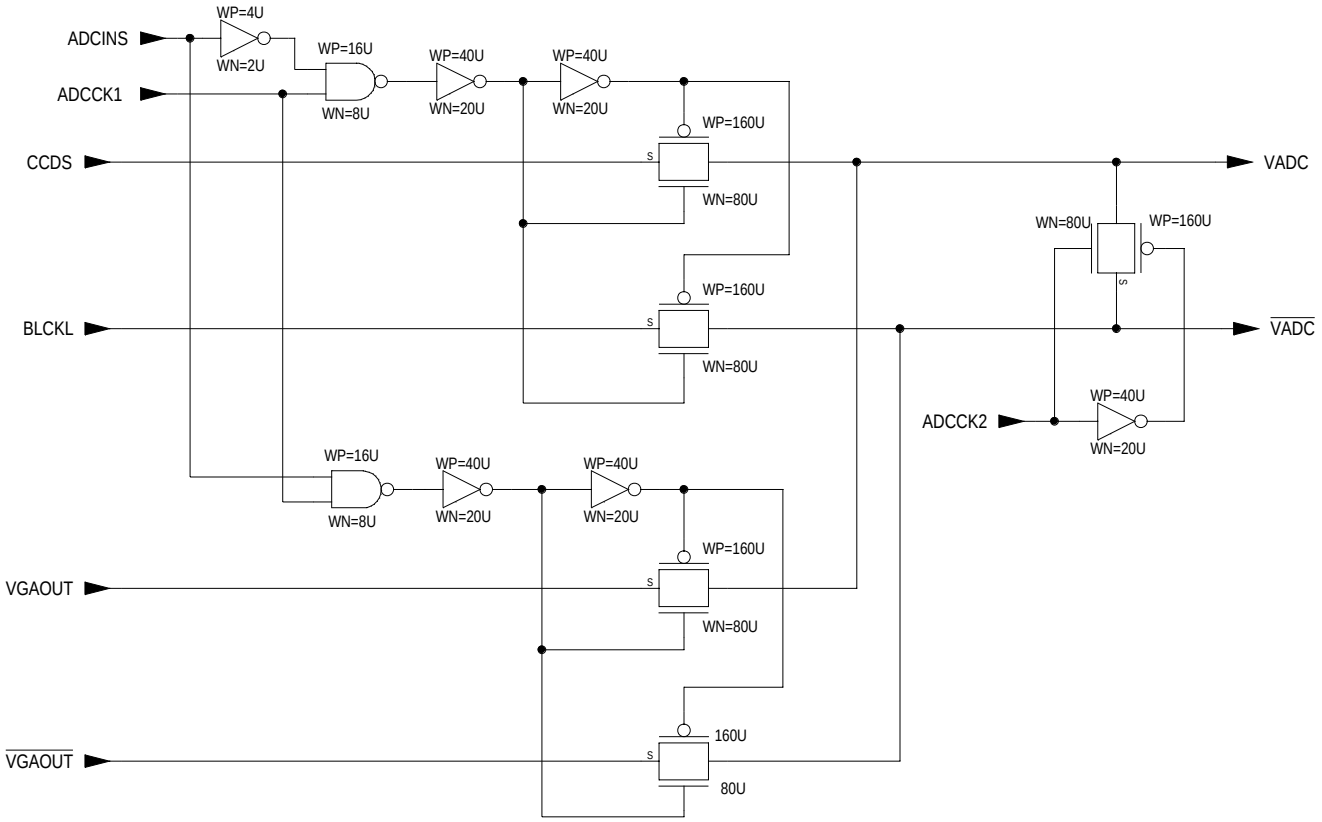


Figure 7.1.6 INPUT SWITCHES

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	47	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:07		
LOCATION:	XX	INITIALS:	MH

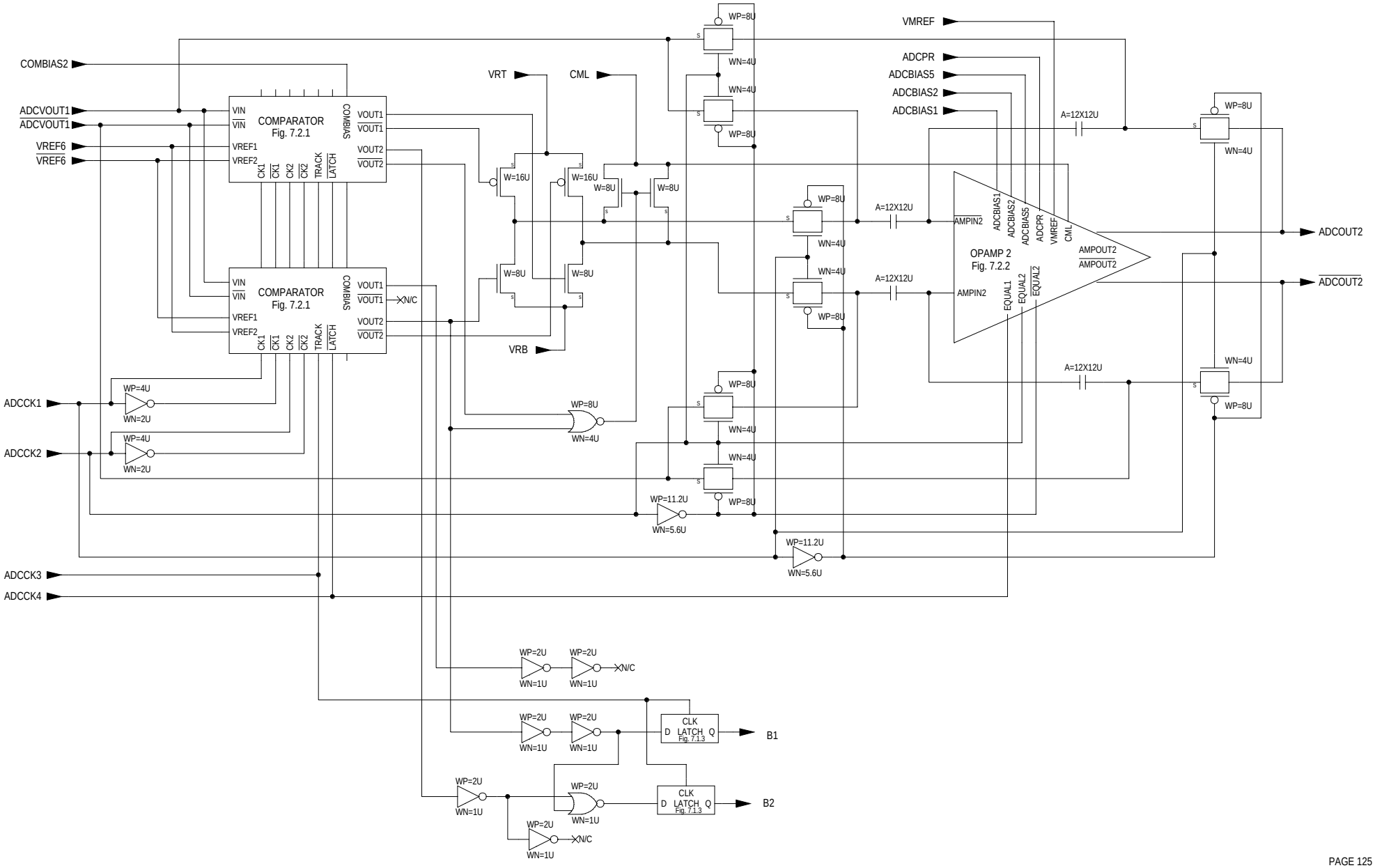


Figure 7.2 ADC STAGE 2

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	56	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:22		
LOCATION:	XX	INITIALS:	MH

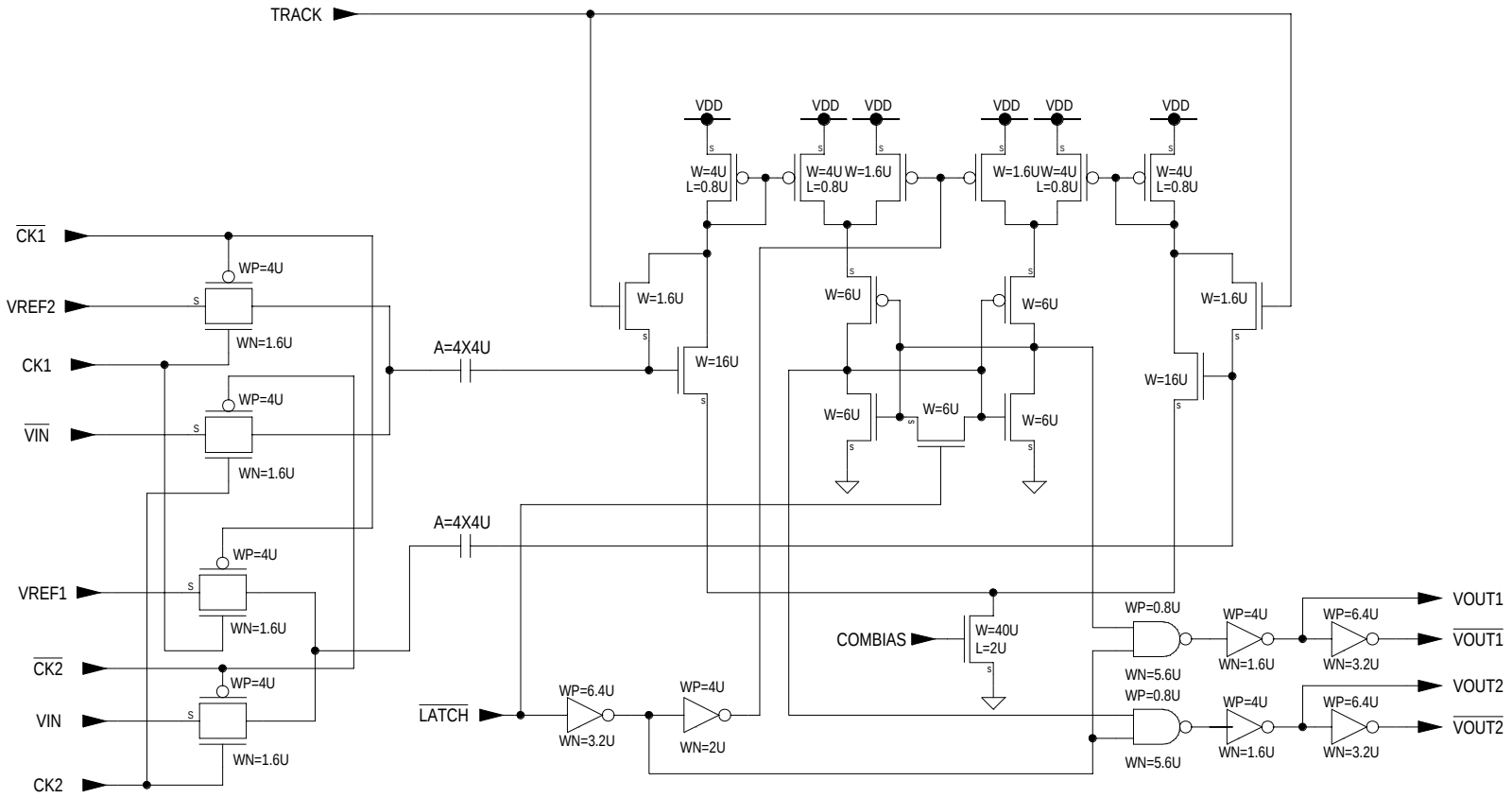
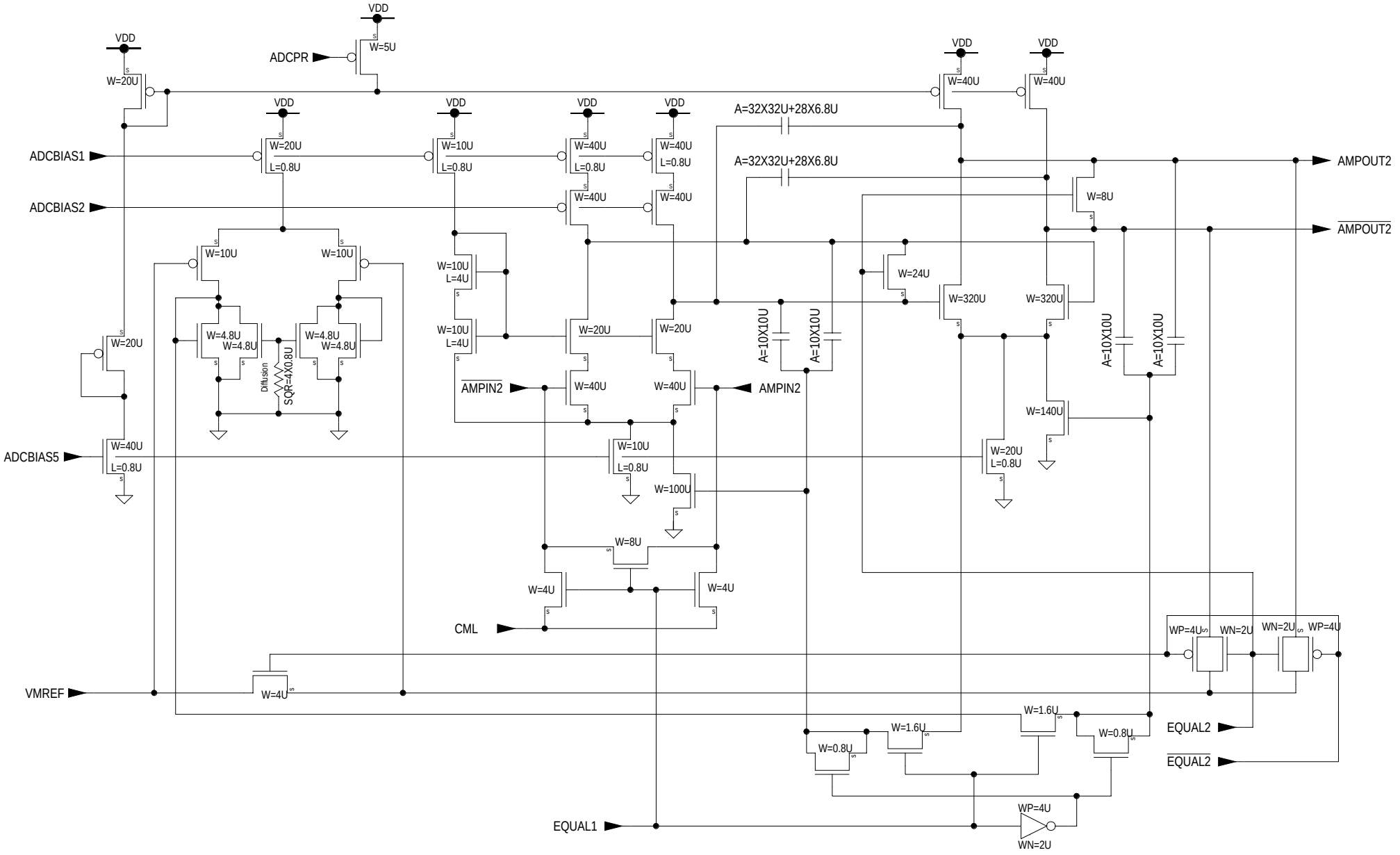


Figure 7.2.1 COMPARATOR 2

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	54	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:22		
LOCATION:	XX	INITIALS:	MH



PAGE 127

Figure 7.2.2 OPAMP 2

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	55	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:07		
LOCATION:	XX	INITIALS:	GY

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

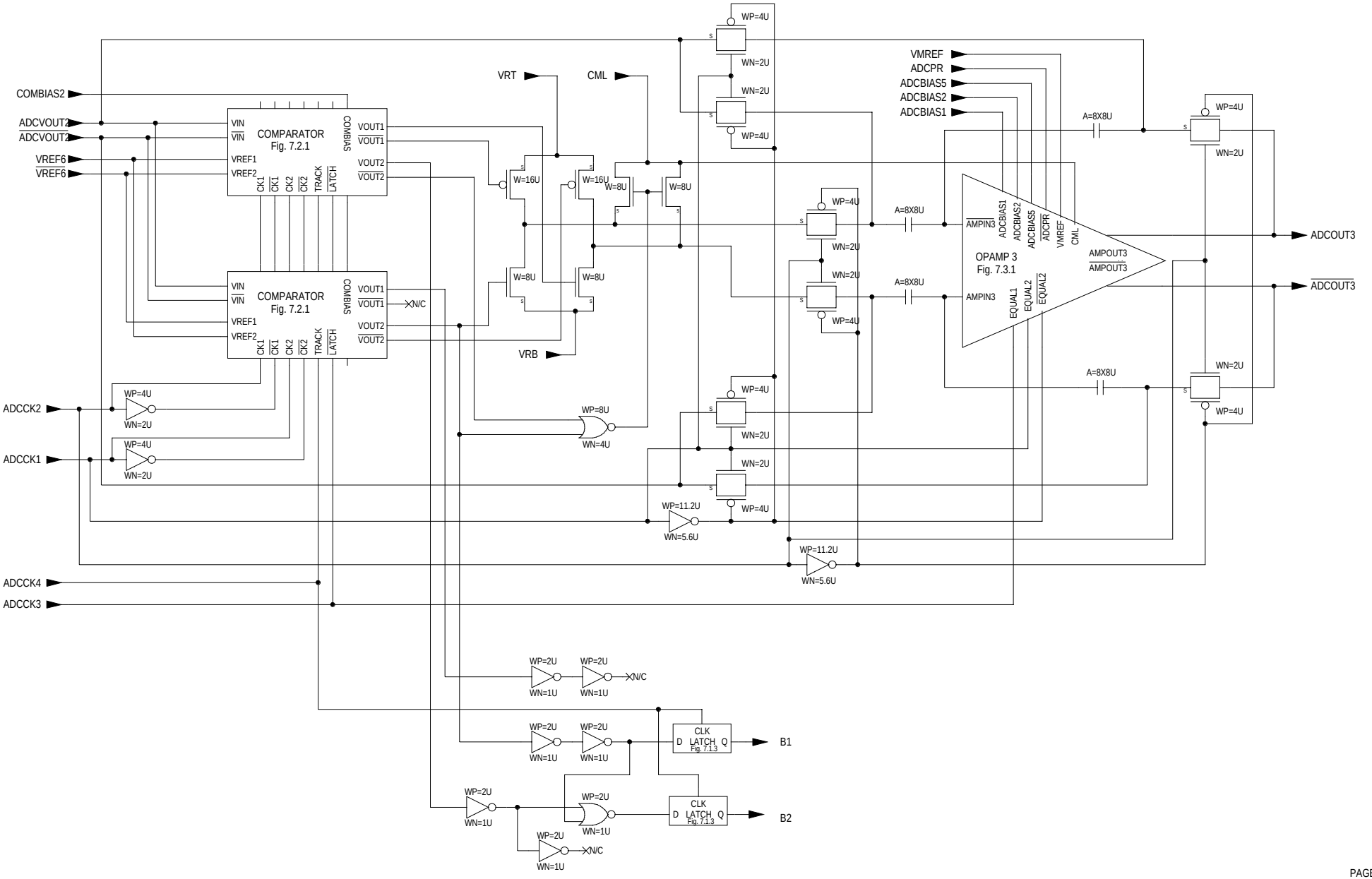
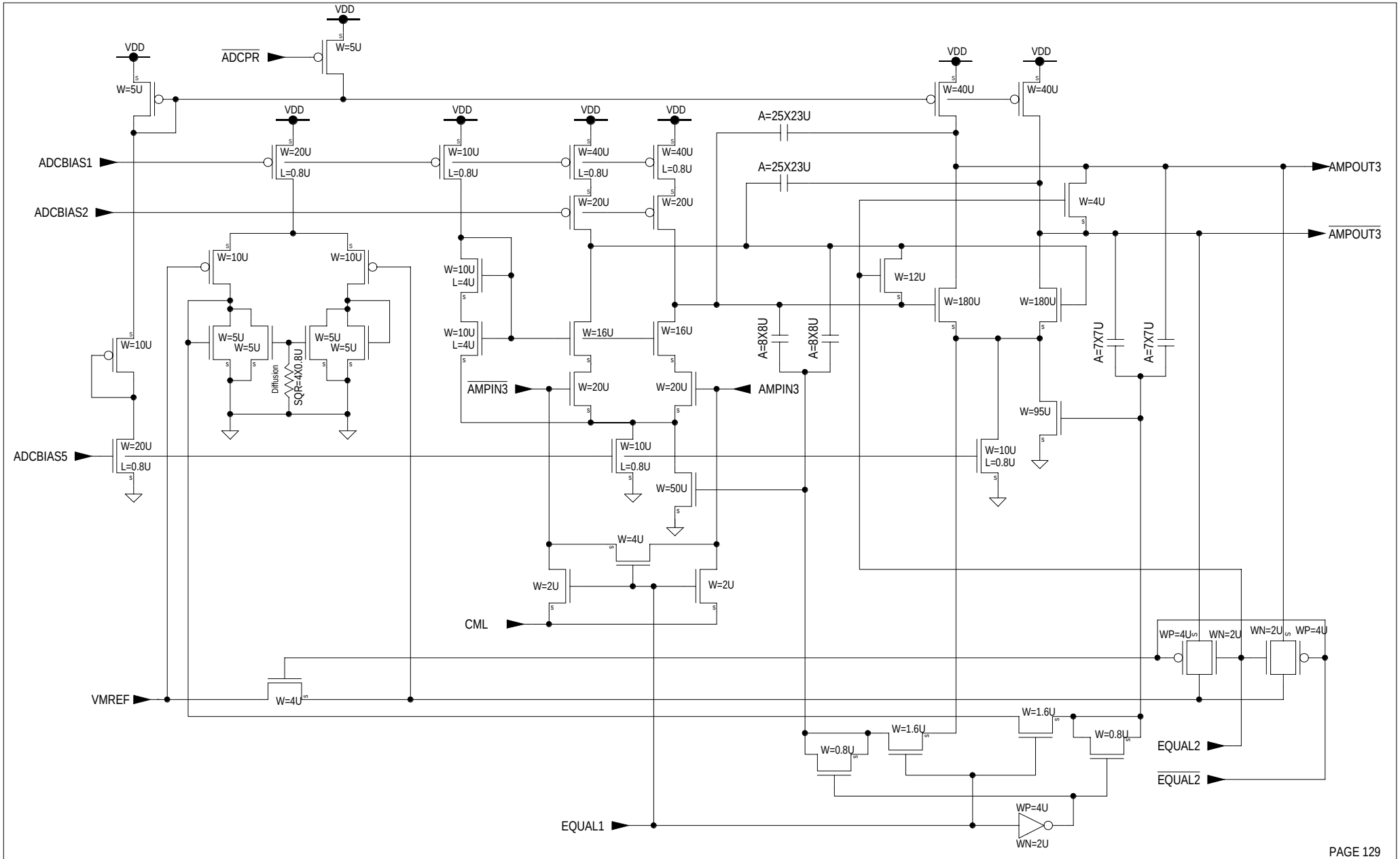


Figure 7.3 ADC STAGE 3

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	58	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:22		
LOCATION:	XX	INITIALS:	MH



PAGE 129

Figure 7.3.1 OPAMP 3

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	57	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:07		
LOCATION:	XX	INITIALS:	MH

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

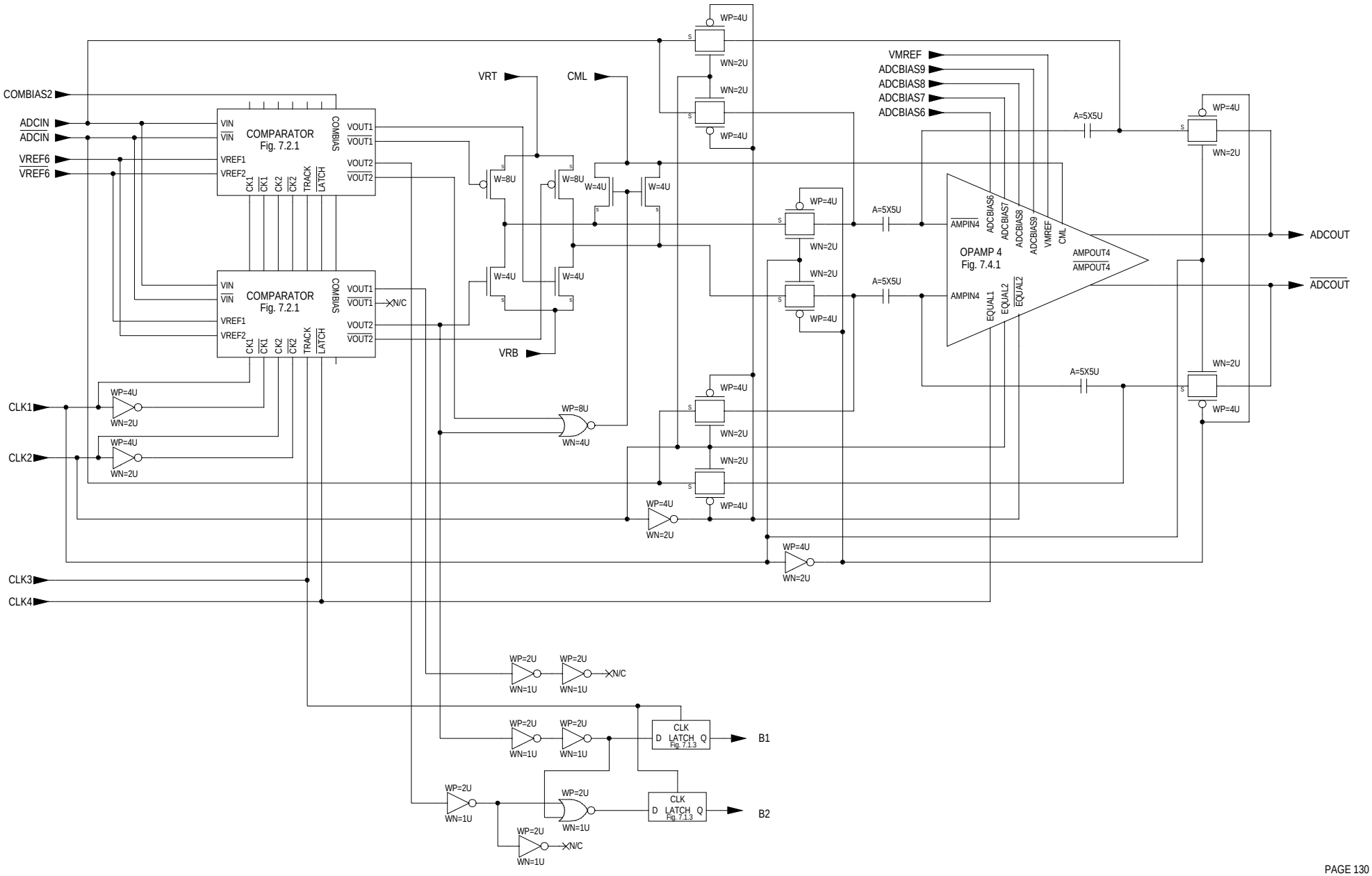


Figure 7.4 ADC STAGE 4

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	60	SI NUMBER:	SI01
DATE_TIME:	6-26-2002_10:47		
LOCATION:	XX	INITIALS:	MH

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

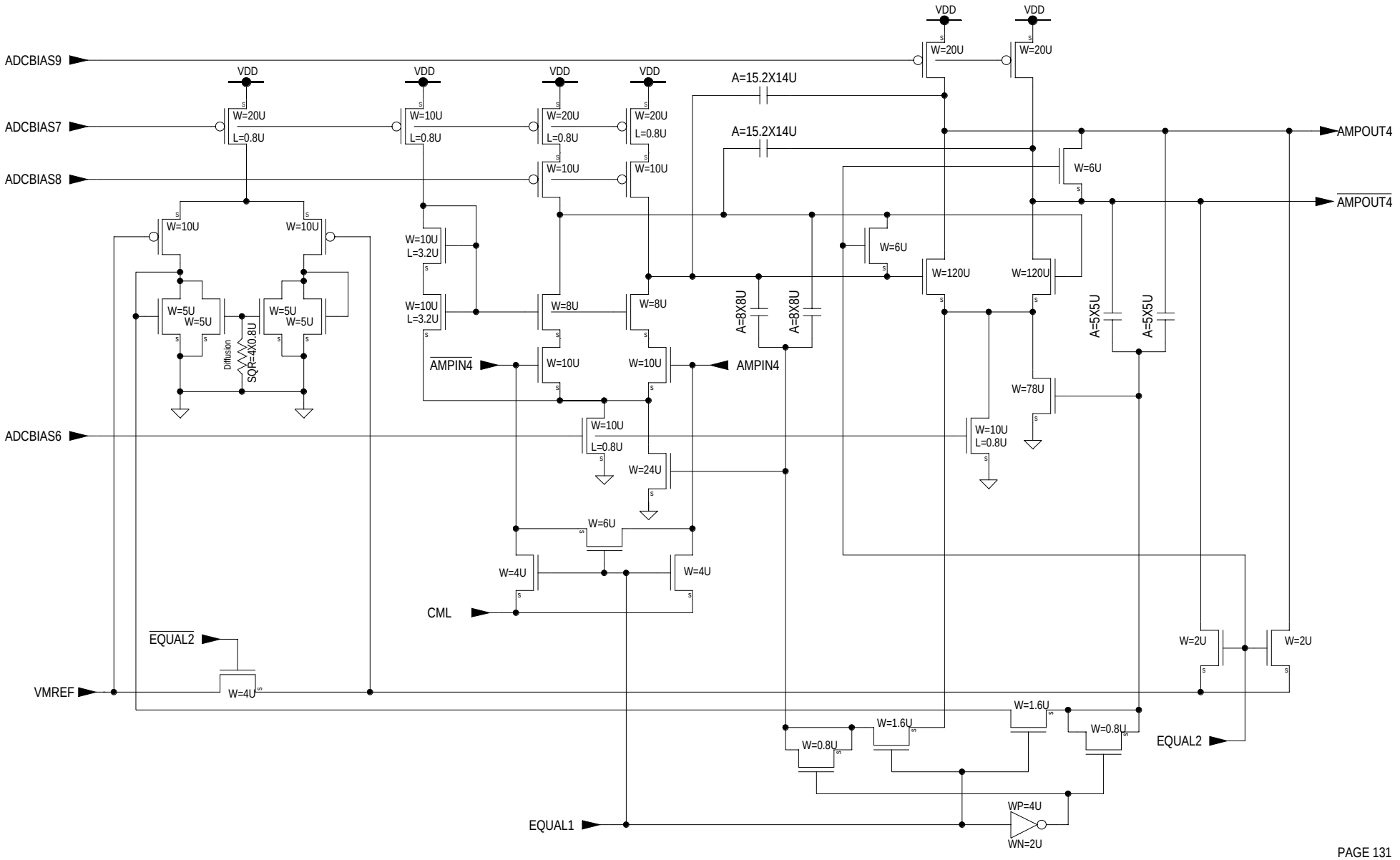


Figure 7.4.1 OPAMP 4

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	59	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:07		
LOCATION:	XX	INITIALS:	MH

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

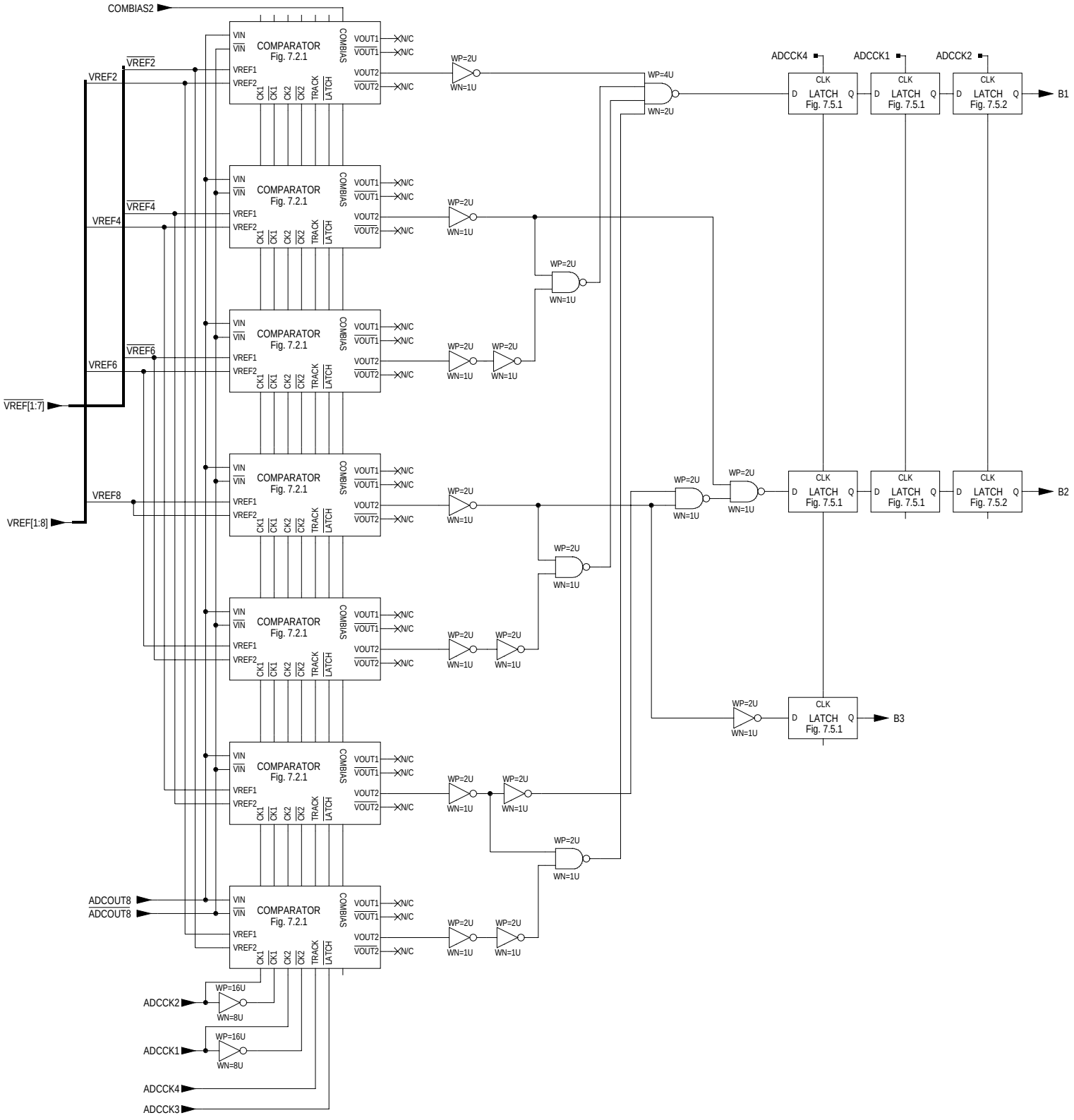


Figure 7.5 ADC END STAGE

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	68	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:23		
LOCATION:	XX	INITIALS:	GY

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

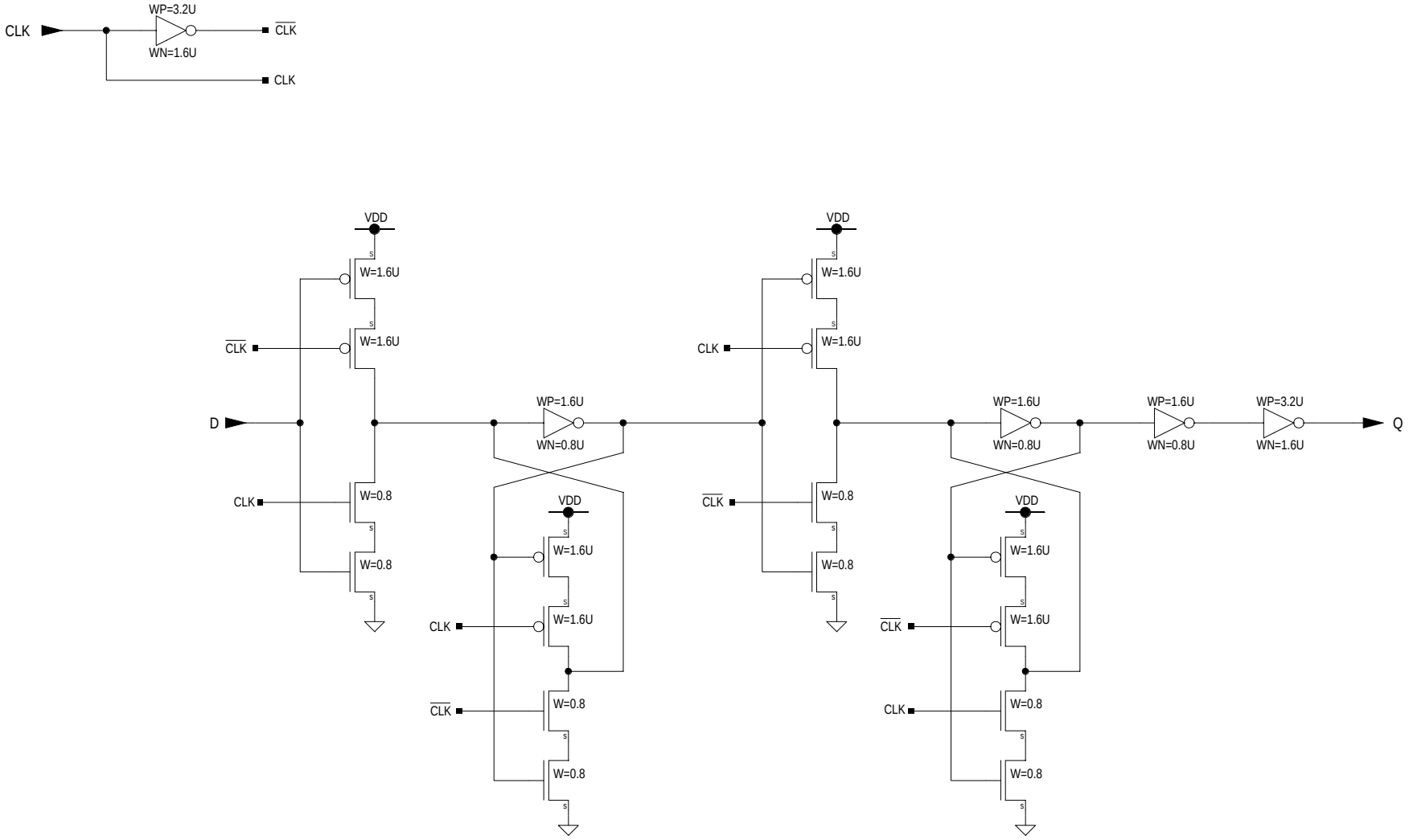


Figure 7.5.1 LATCH 2

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	62	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:08		
LOCATION:	XX	INITIALS:	MH

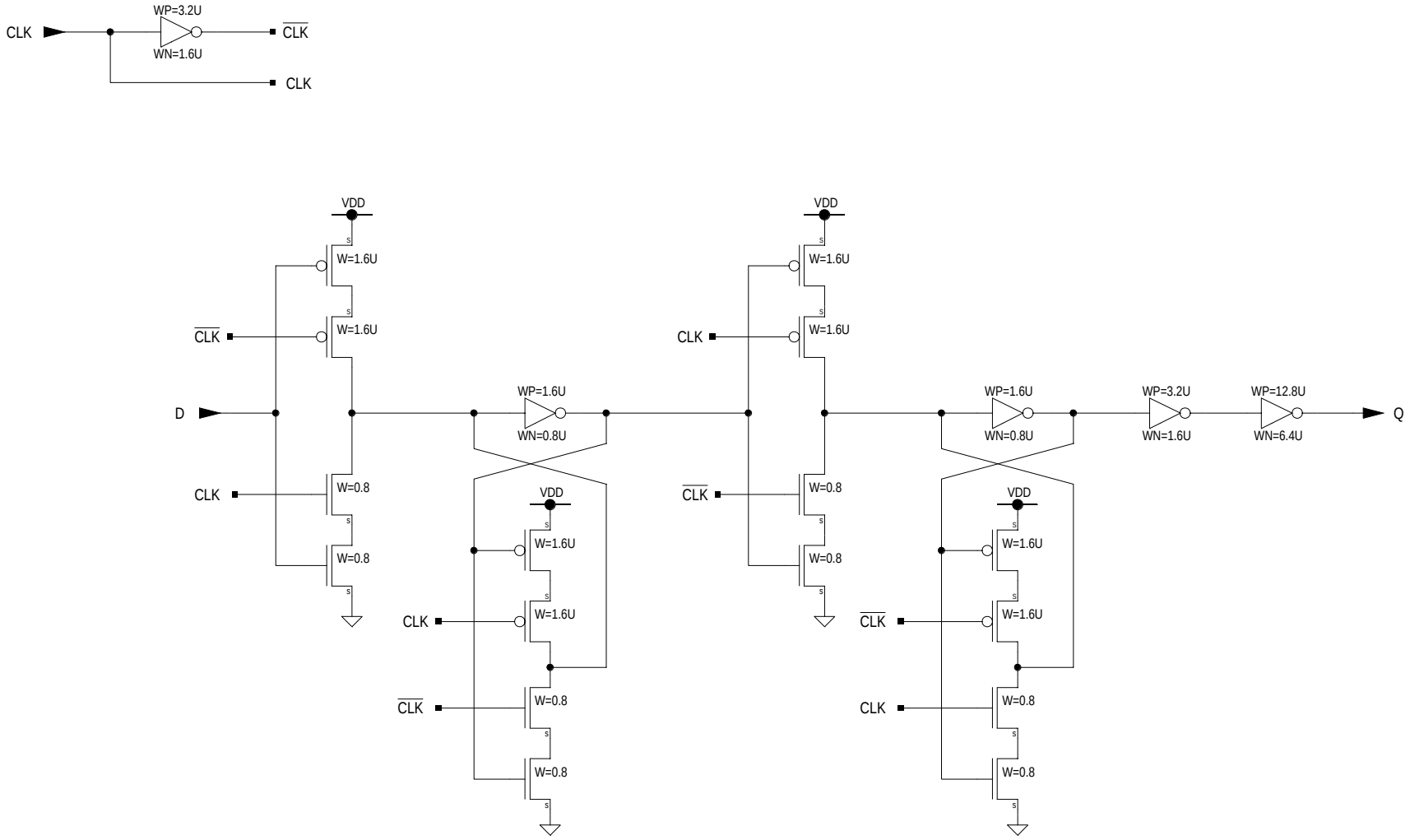


Figure 7.5.2 LATCH 3

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	66	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:08		
LOCATION:	XX	INITIALS:	MH

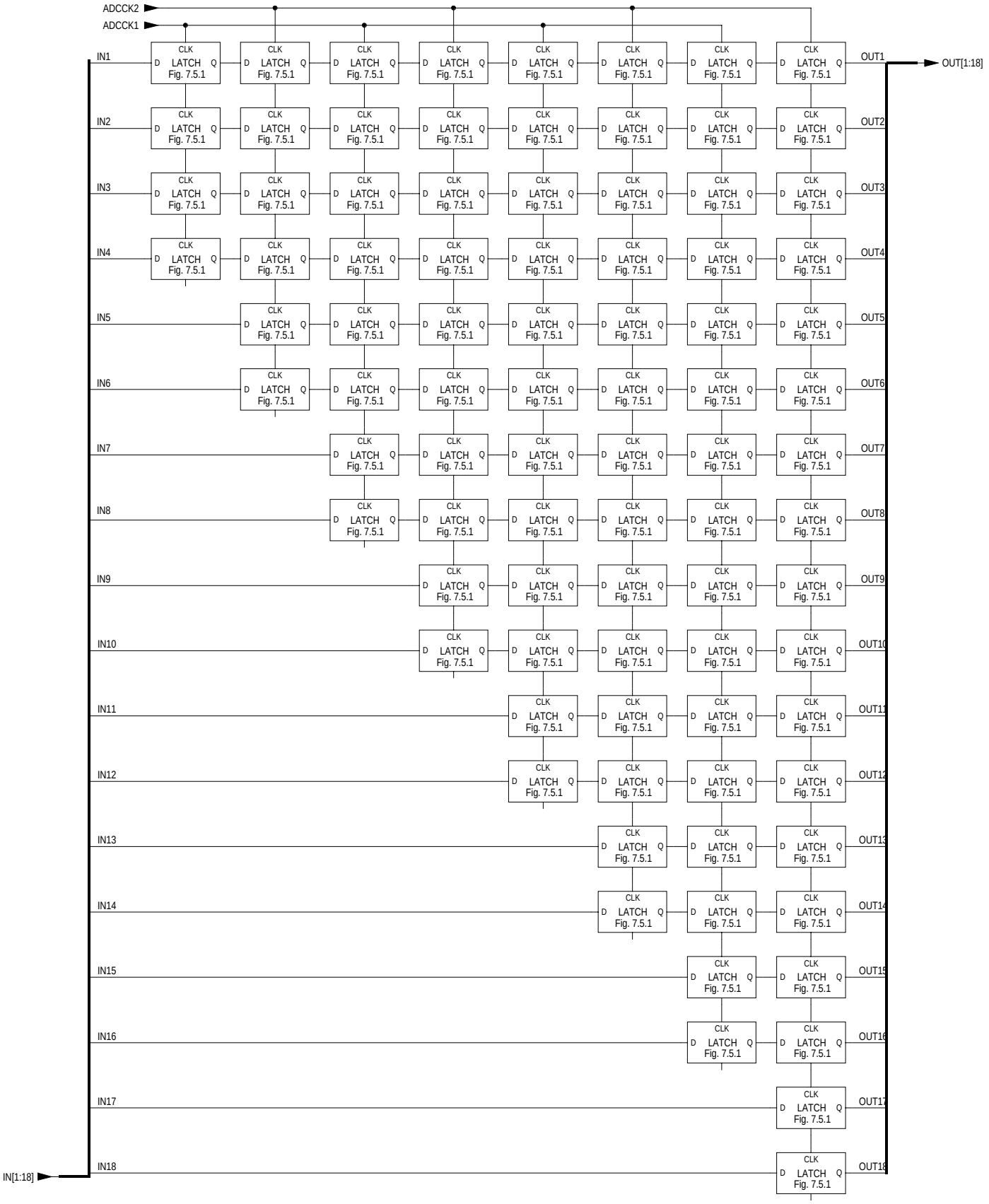
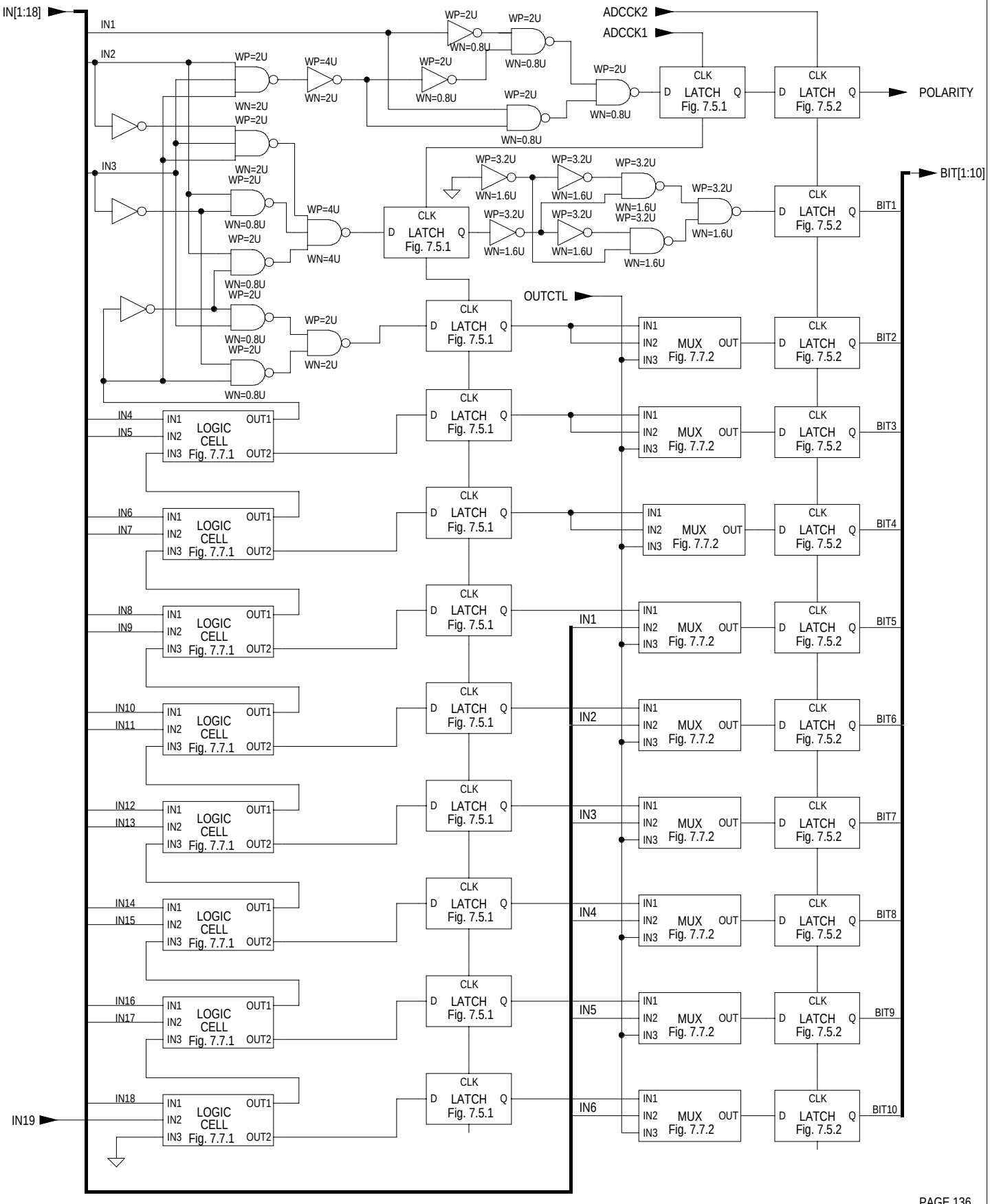


Figure 7.6 PIPELINE

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	63	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:23		
LOCATION:	XX	INITIALS:	MH

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



PAGE 136

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	67	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:23		
LOCATION:	XX	INITIALS:	MH

Figure 7.7 CORRECTION LOGIC

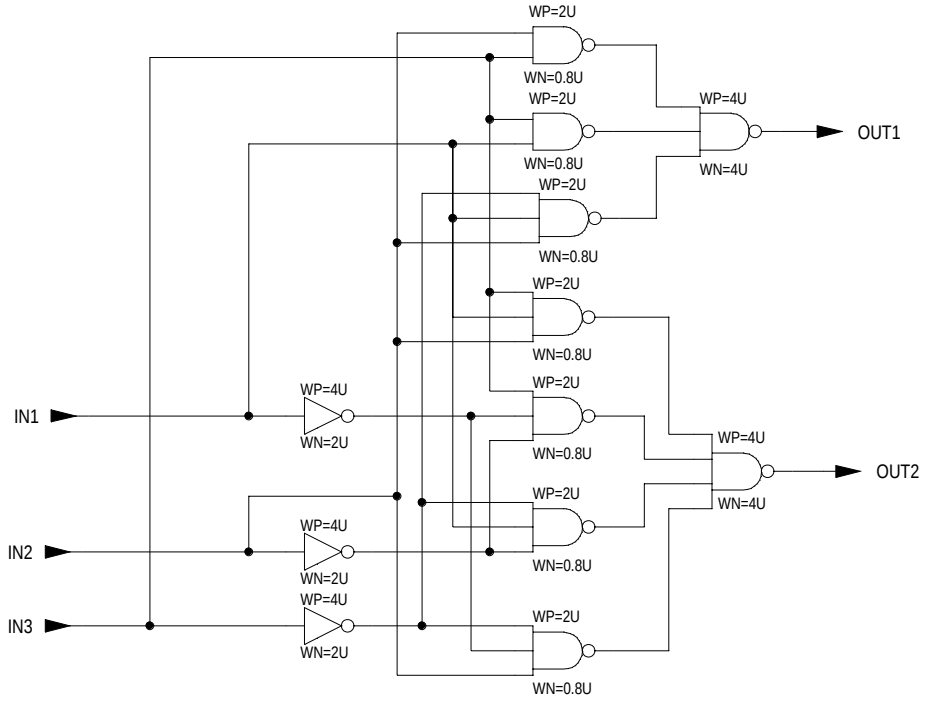


Figure 7.7.1 CORRECTION LOGIC CELL

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	64	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:24		
LOCATION:	XX	INITIALS:	MH

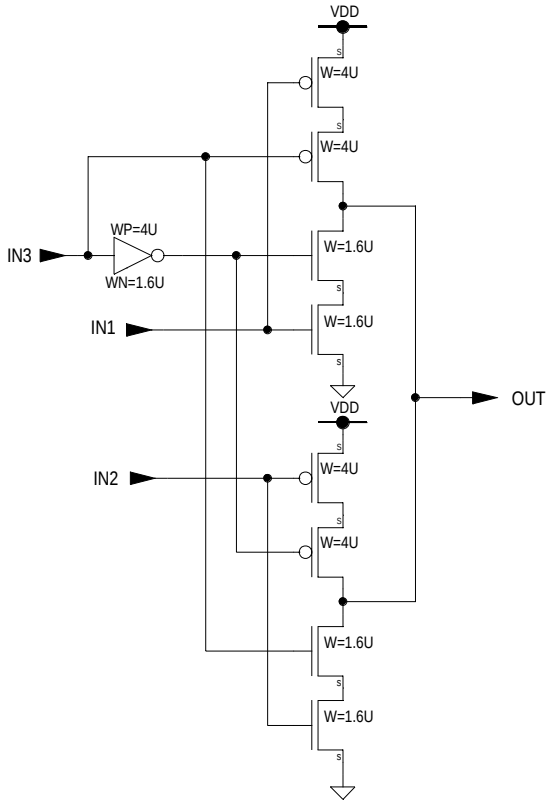


Figure 7.7.2 MULTIPLEXER

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	65	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:24		
LOCATION:	XX	INITIALS:	MH

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

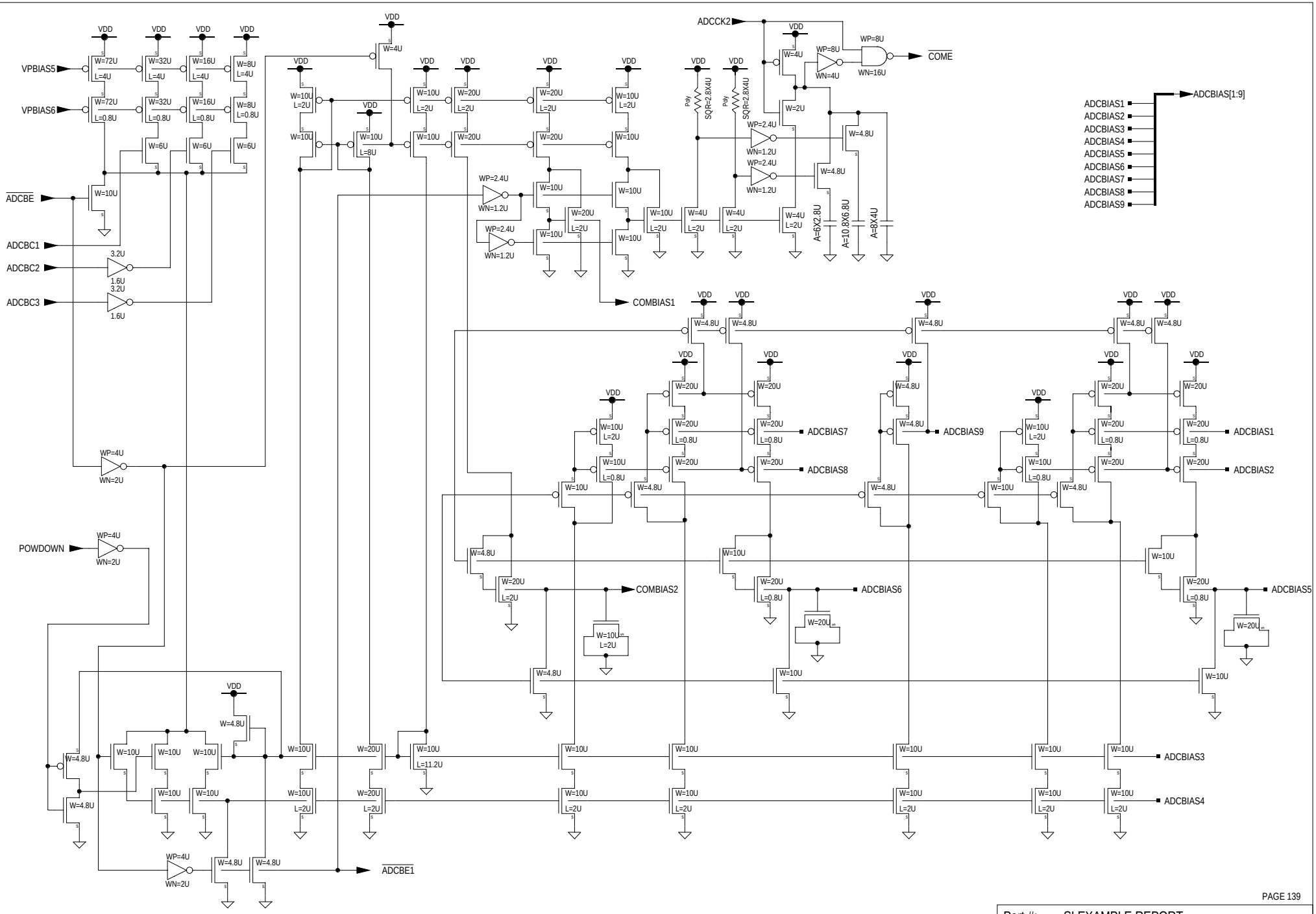
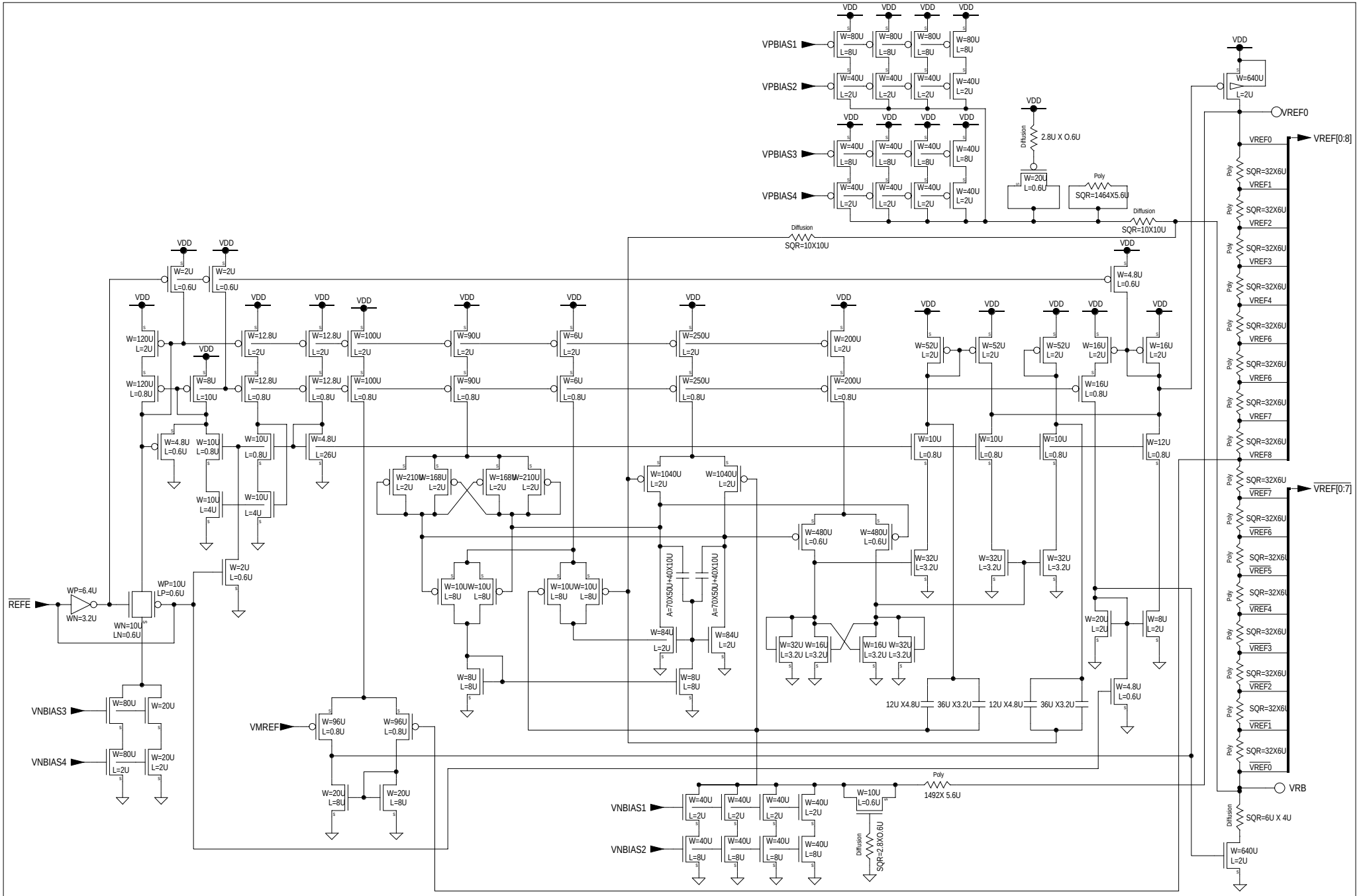


Figure 7.8 ADC BIASING VOLTAGE GENERATOR

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	36	SI NUMBER:	SI01
DATE_TIME:	6-18-2002_9:24		
LOCATION:	XX	INITIALS:	GY

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



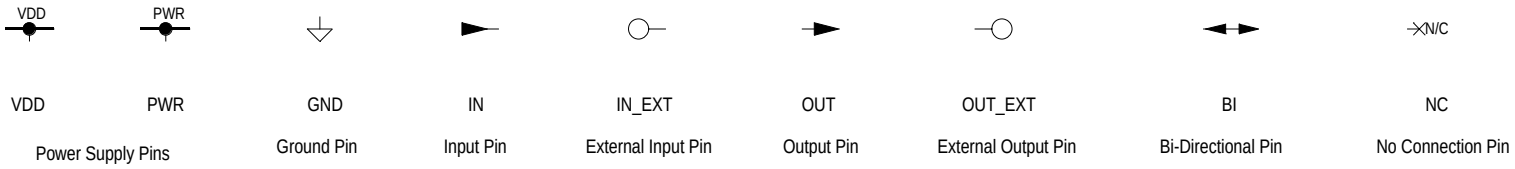
Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	15	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:08		
LOCATION:	XX	INITIALS:	MH

Figure 7.9 REFERENCE VOLTAGE GENERATOR

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

8.0 SI Standard Cells

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com



VDD — Power Supply Pins

PWR — Power Supply Pins

GND — Ground Pin

IN — Input Pin

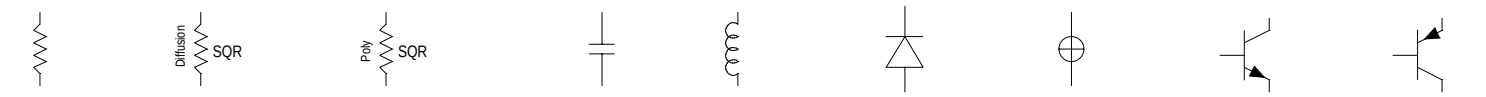
IN_EXT — External Input Pin

OUT — Output Pin

OUT_EXT — External Output Pin

BI — Bi-Directional Pin

NC — No Connection Pin



RES — Resistor (Ohms)

RES_DIFF — Diffusion Resistor (Squares - L/W)

RES_POLY — Polysilicon Resistor (Squares- L/W)

CAP — Capacitor (Farads)

INDUCT — Inductor (Henris)

DIODE — DIODE

FUSE — FUSE

BJTNPN — Bi-Polar NPN

BJTPNP — Bi-Polar PNP

NMOS — NMOS Transistor

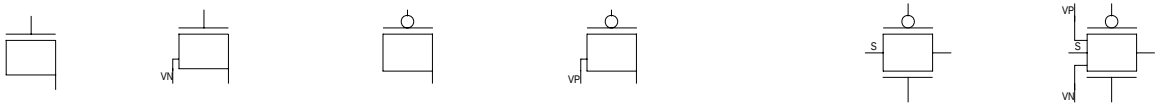
NMOSSUB — NMOS Transistor with Substrate Connection

NMOSPAS — NMOS Transistor with Pass-through Pin

PMOS — PMOS Transistor

PMOSSUB — PMOS Transistor with Substrate Connection

PMOSPAS — PMOS Transistor with Pass-through Pin



NCAP — NMOS Polysilicon-Diffusion Capacitor

NCAP_SW — NMOS Polysilicon-Diffusion Capacitor With Substrate Connection

PCAP — PMOS Polysilicon-Diffusion Capacitor

PCAP_SW — PMOS Polysilicon-Diffusion Capacitor With Substrate Connection

TRAN1 — CMOS Transfer Gate

TRAN1_SW — CMOS Transfer Gate With Substrate Connection

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	STCELL1	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:30		
LOCATION:	XX	INITIALS:	GY

Figure 8.0 SI_LIB SYMBOL DEFINITION PAGE 1

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

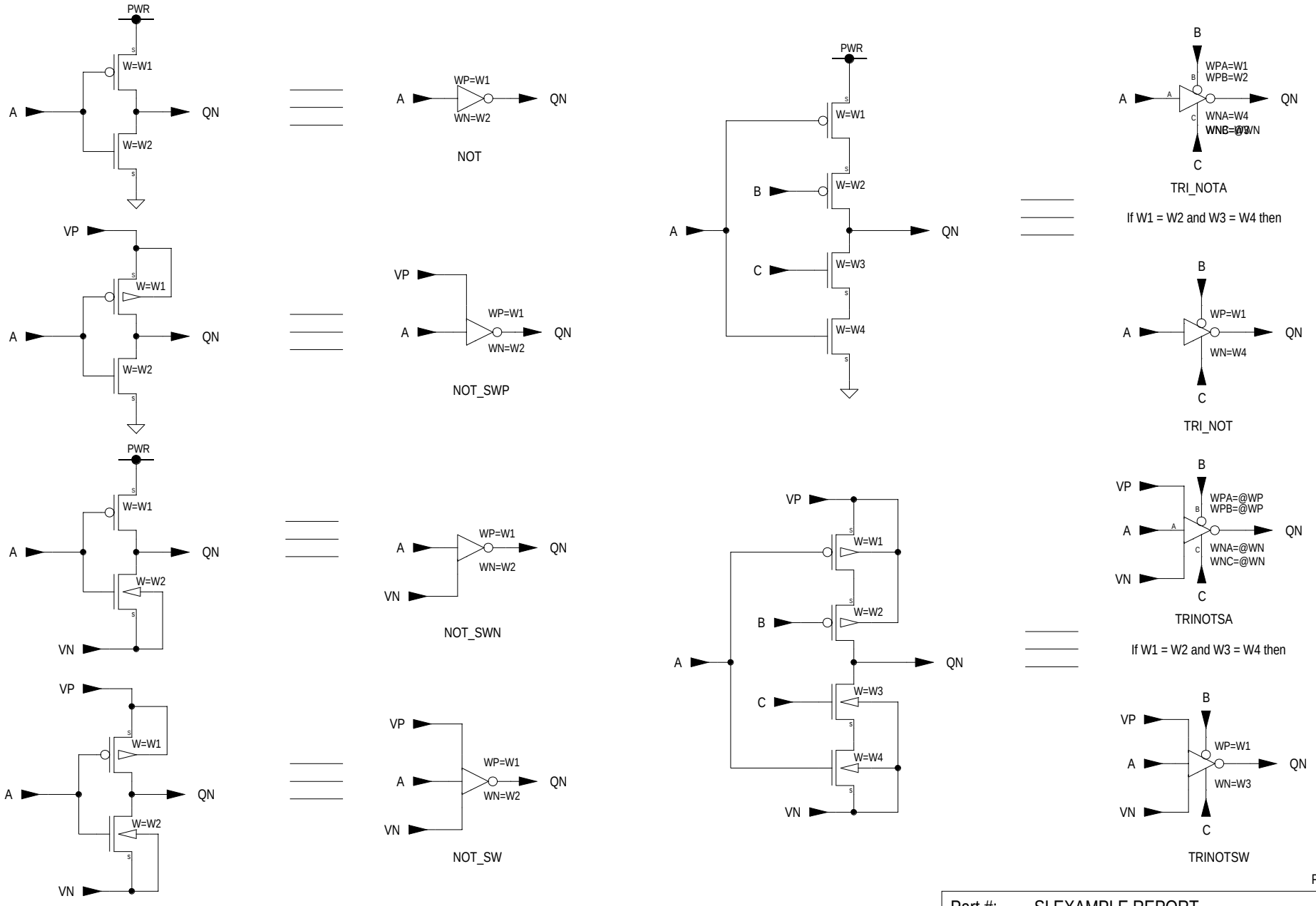
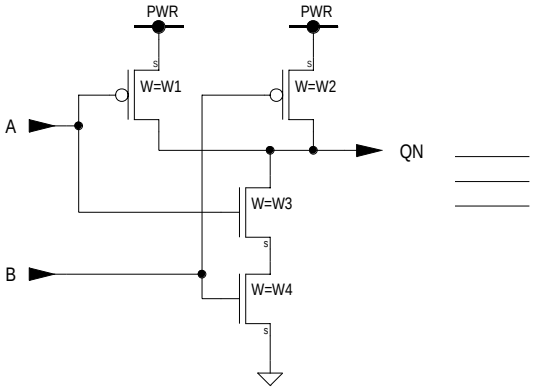
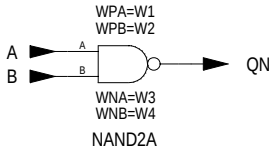


Figure 8.1 SI_LIB SYMBOL DEFINITION PAGE 2 - INVERTERS

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	STCELL2	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:31		
LOCATION:	XX	INITIALS:	GY

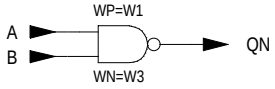
SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



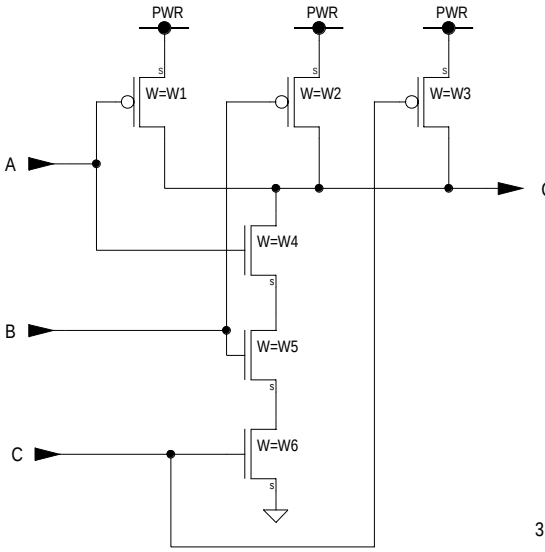


NAND2A

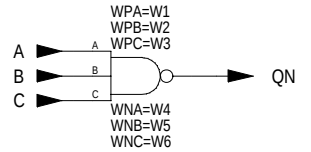
If W1 = W2 and W3 = W4 then



NAND2

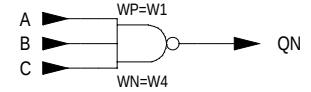


3 Input NAND

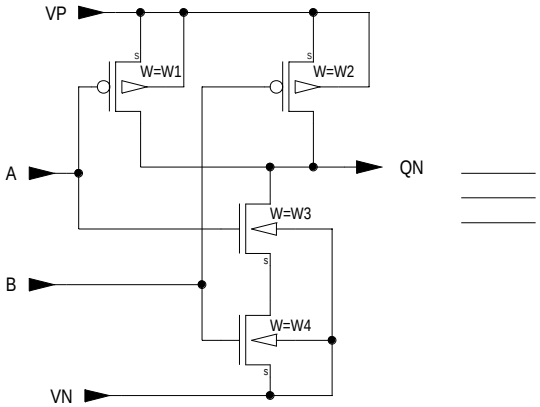


NAND3A

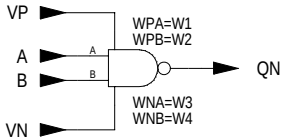
If W1 = W2 = W3 and W4 = W5 = W6 then



NAND3

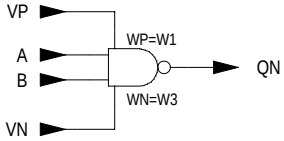


2 Input NANDS

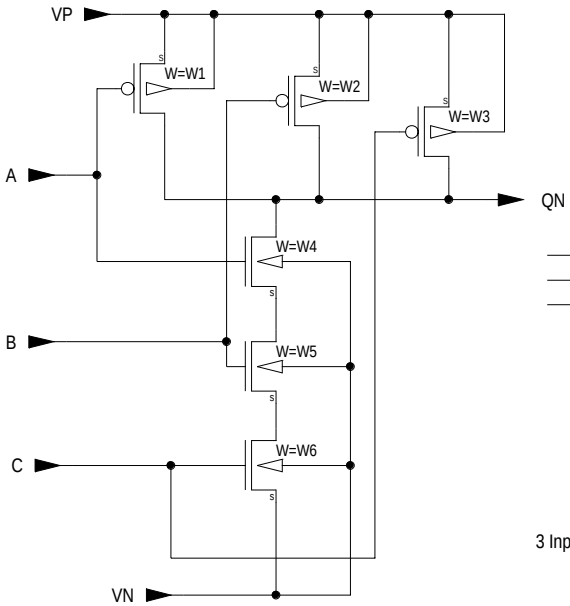


NAND2SWA

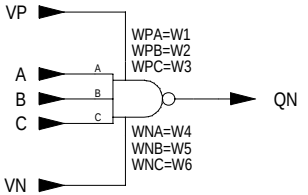
If W1 = W2 and W3 = W4 then



NAND2_SW

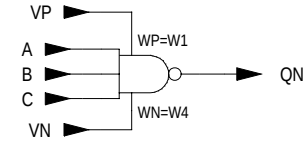


3 Input NAND



NAND3A

If W1 = W2 = W3 and W4 = W5 = W6 then

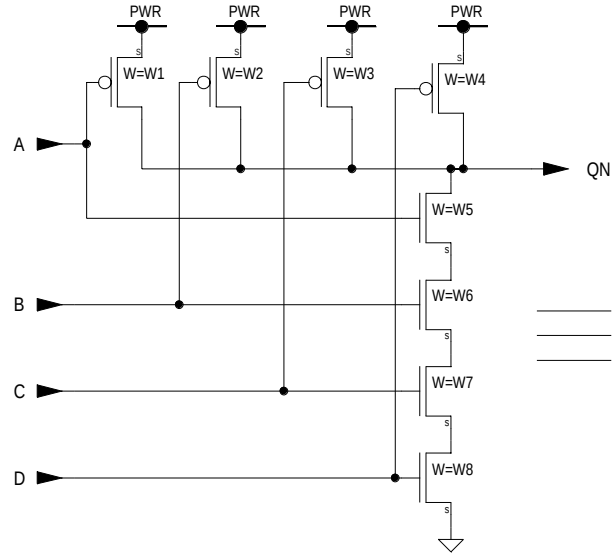


NAND3

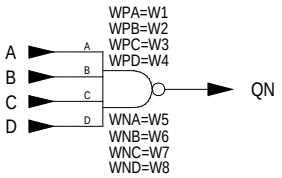
Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	STCELL3	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:31		
LOCATION:	XX	INITIALS:	GY

Figure 8.2 SI_LIB SYMBOL DEFINITION PAGE 3 - NANDS

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



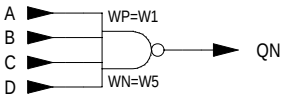
4 Input NAND



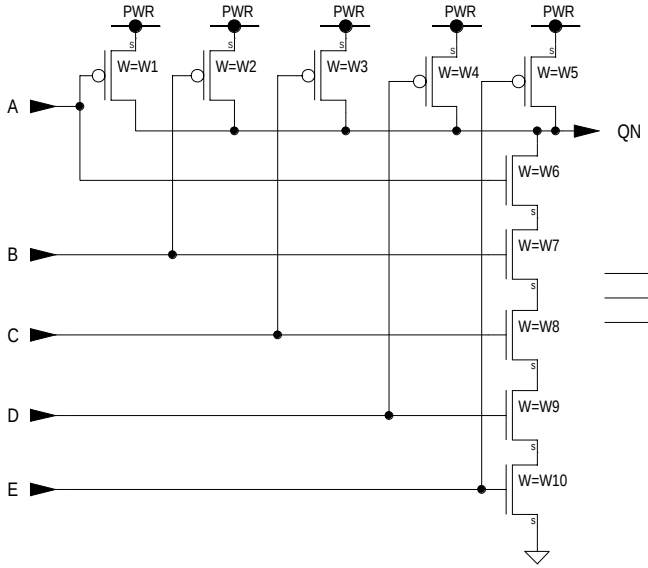
NAND4A

If W1 = W2 = W3 = W4 and

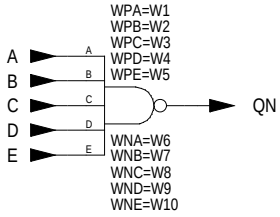
W5 = W6 = W7 = W8 then



NAND4



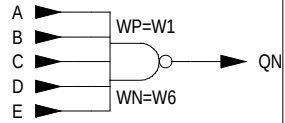
5 Input NAND



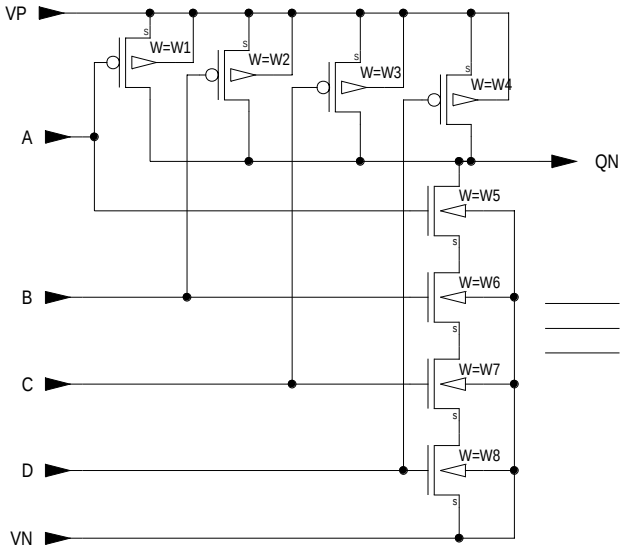
NAND5A

If W1 = W2 = W3 = W4 = W5 and

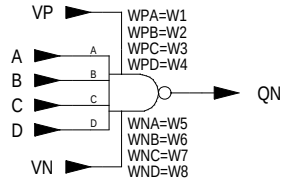
W6 = W7 = W8 = W9 = W10 then



NAND5



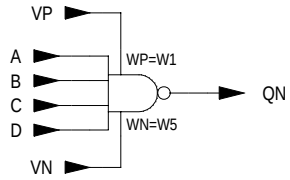
4 Input NAND with alternate power supplies



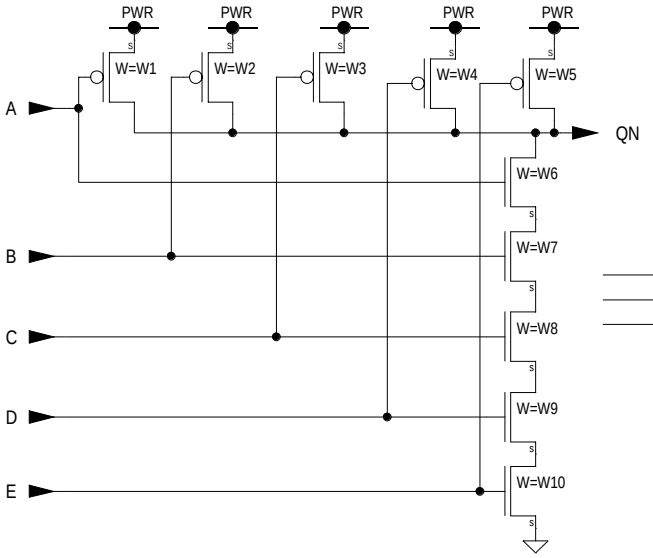
NAND4A

If W1 = W2 = W3 = W4 and

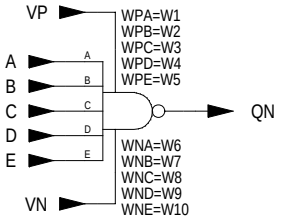
W5 = W6 = W7 = W8 then



NAND4



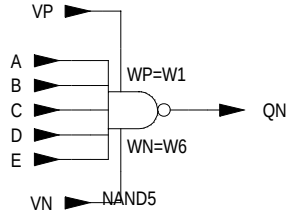
5 Input NAND with alternate power supplies



NAND5A

If W1 = W2 = W3 = W4 = W5 and

W6 = W7 = W8 = W9 = W10 then



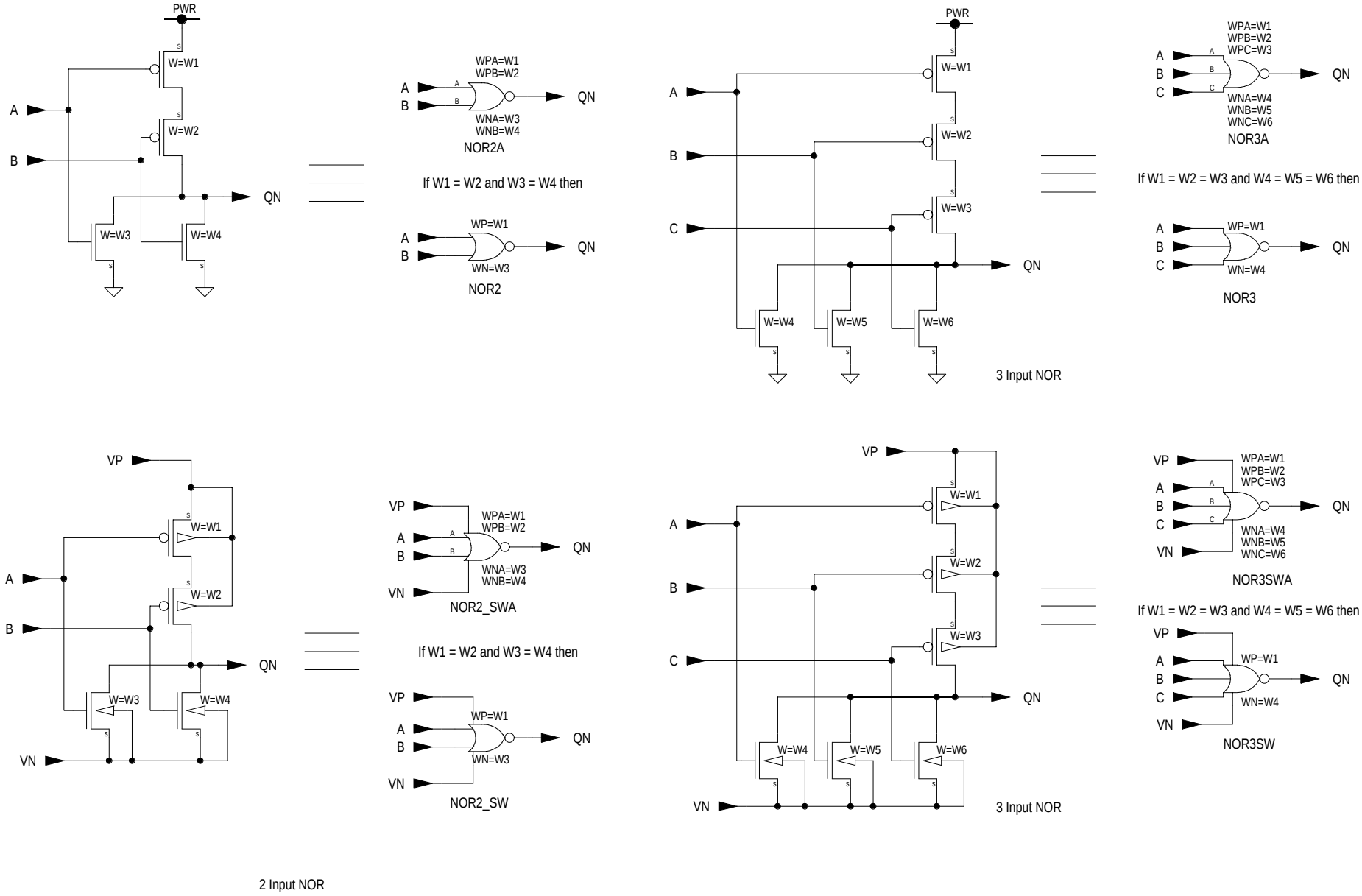
NAND5

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	STCELL4	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:31		
LOCATION:	XX	INITIALS:	GY

Figure 8.3 SI_LIB SYMBOL DEFINITION PAGE 4 - NANDS

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501

http://www.semiconductor.com

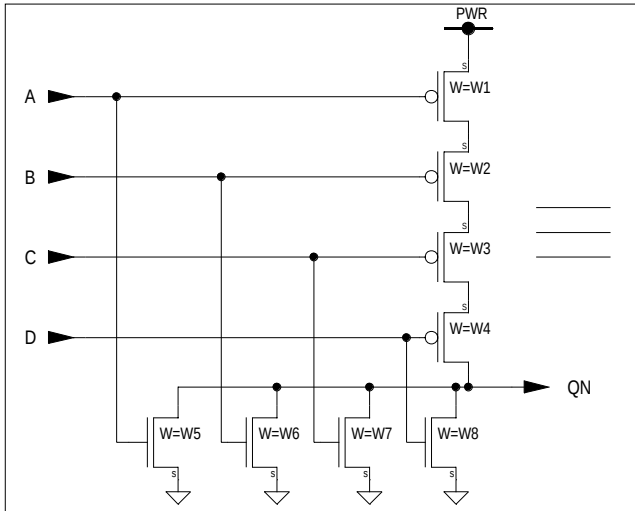


PAGE 146

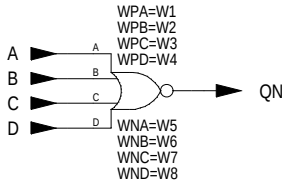
Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	STCELL5	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:31		
LOCATION:	XX	INITIALS:	GY

Figure 8.4 SI_LIB SYMBOL DEFINITION PAGE 5 - NORS

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



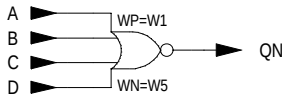
4 Input NOR



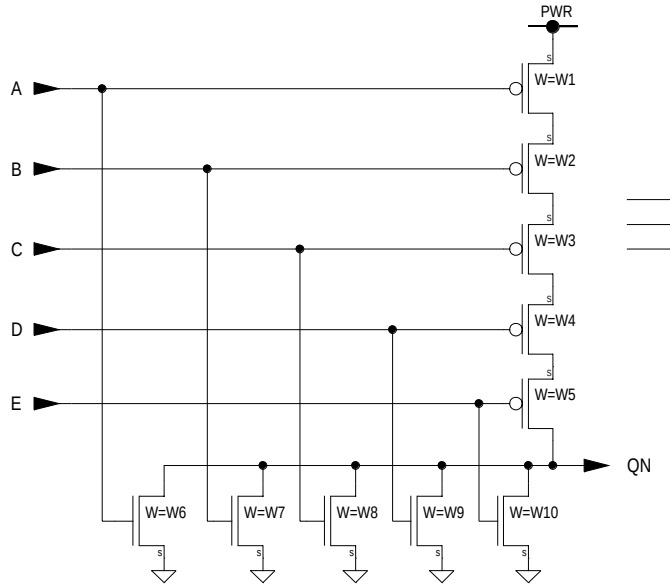
NOR4A

If W1 = W2 = W3 = W4 and

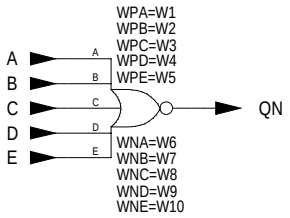
W5 = W6 = W7 = W8 then



NOR4



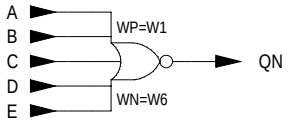
5 Input NOR



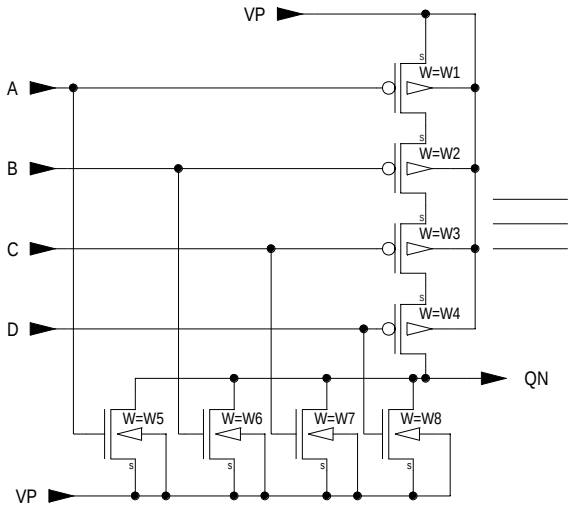
NOR5A

If W1 = W2 = W3 = W4 = W5 and

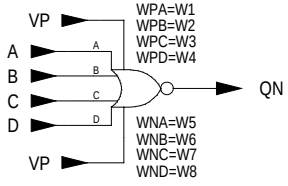
W6 = W7 = W8 = W9 = W10 then



NOR5



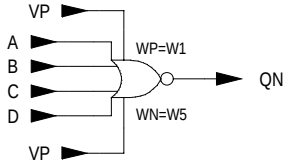
4 Input NOR



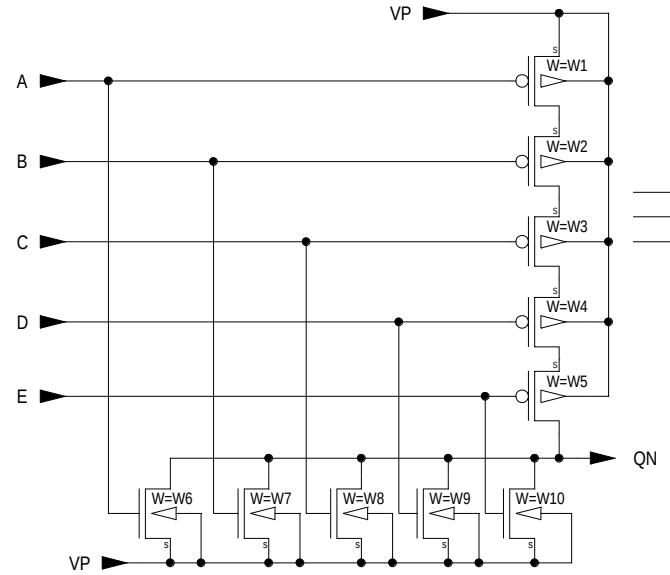
NOR4SWA

If W1 = W2 = W3 = W4 and

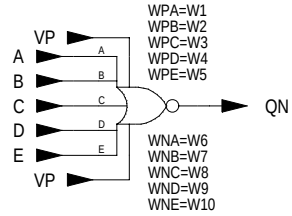
W5 = W6 = W7 = W8 then



NOR4_SW



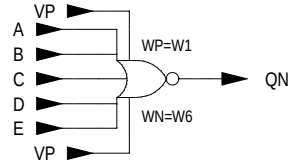
5 Input NOR



NOR5SWA

If W1 = W2 = W3 = W4 = W5 and

W6 = W7 = W8 = W9 = W10 then

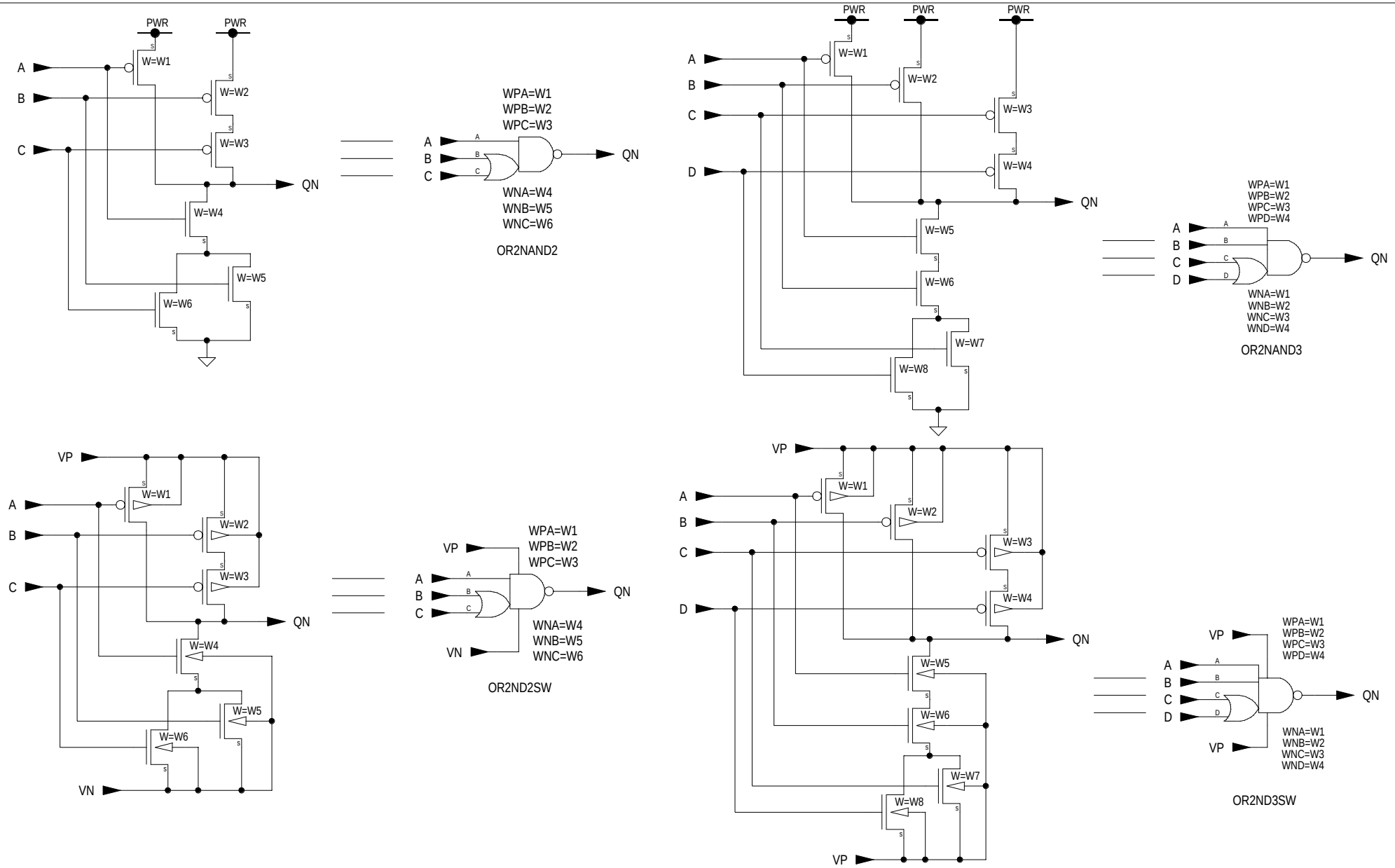


NOR5_SW

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	STCELL6	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:35		
LOCATION:	XX	INITIALS:	GY

Figure 8.5 SI_LIB SYMBOL DEFINITION PAGE 6 - NORS

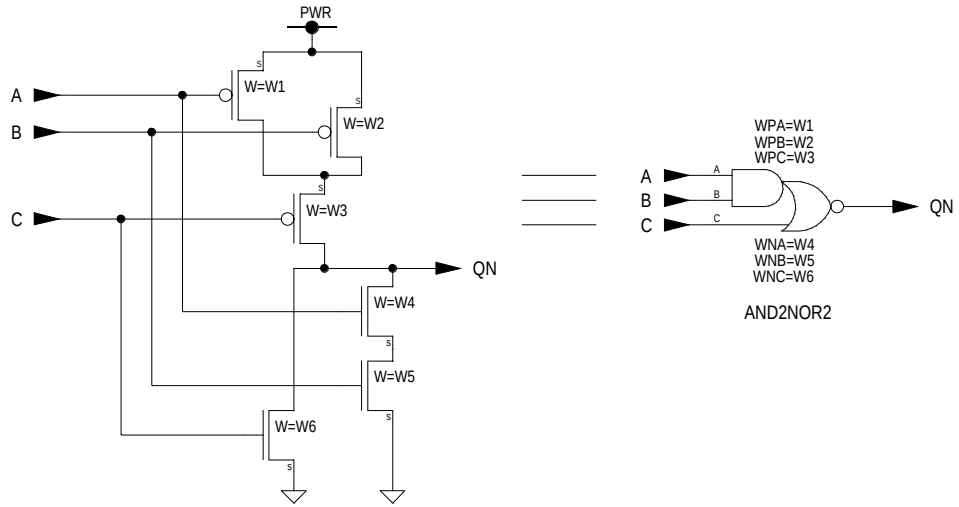
SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

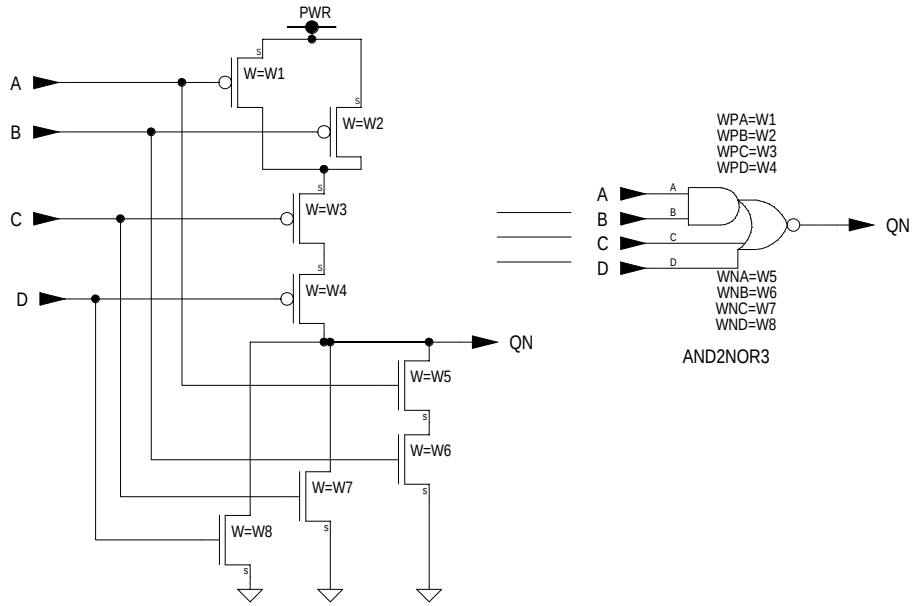


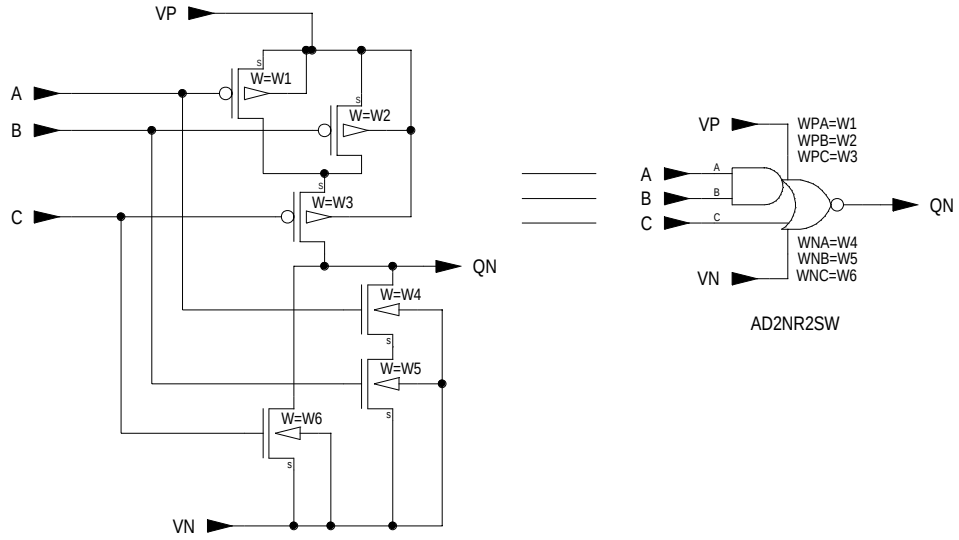
PAGE 148

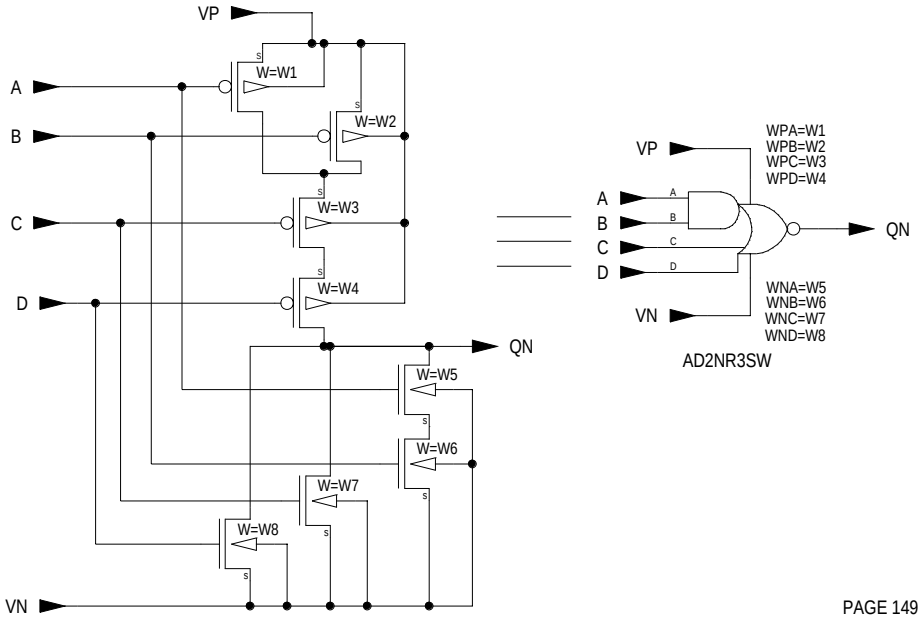
Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	STCELL7	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:31		
LOCATION:	XX	INITIALS:	GY

Figure 8.6 SI_LIB SYMBOL DEFINITION PAGE 7





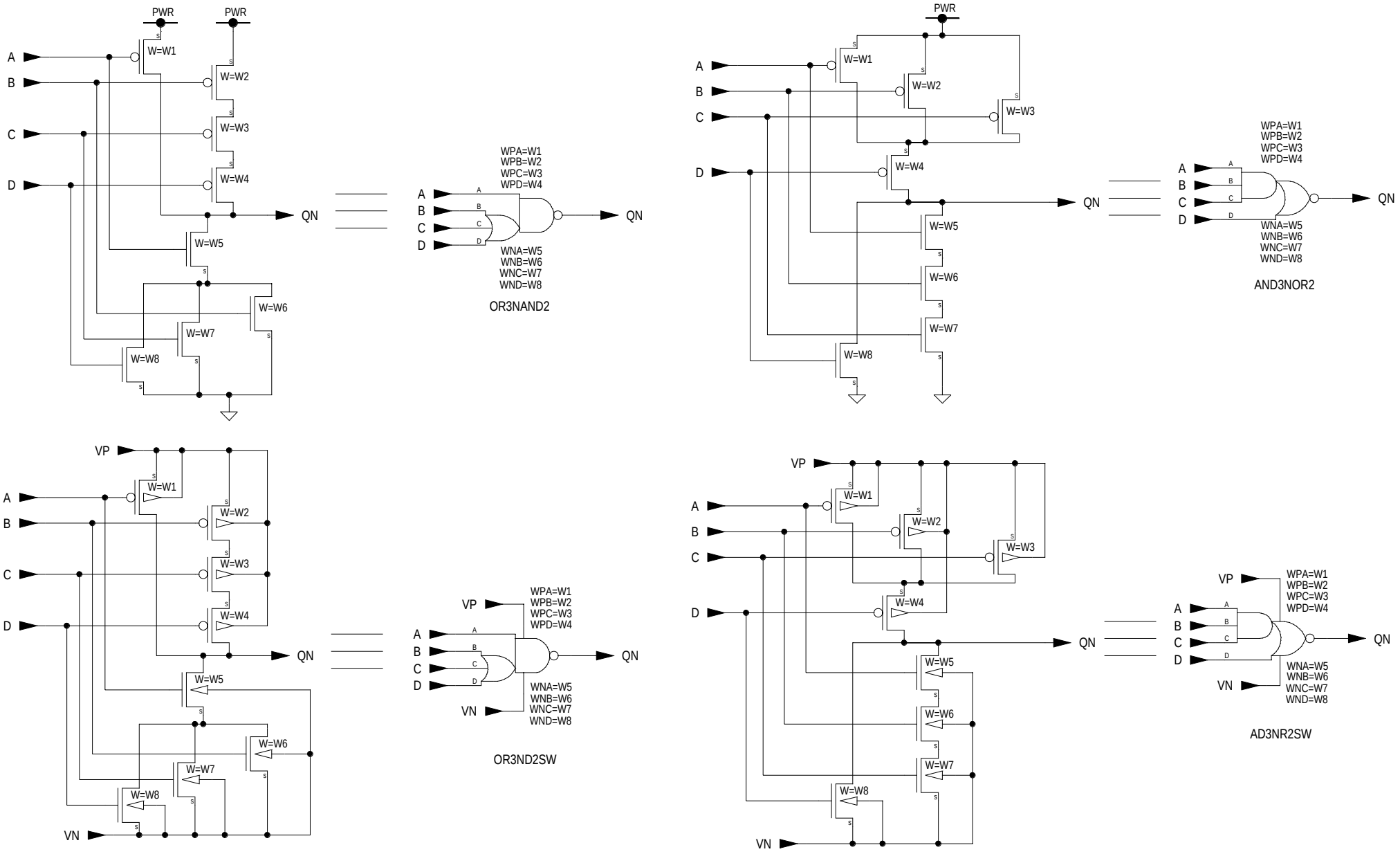




Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	STCELL8	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:31		
LOCATION:	XX	INITIALS:	GY

Figure 8.7 SI_LIB SYMBOL DEFINITION PAGE 8

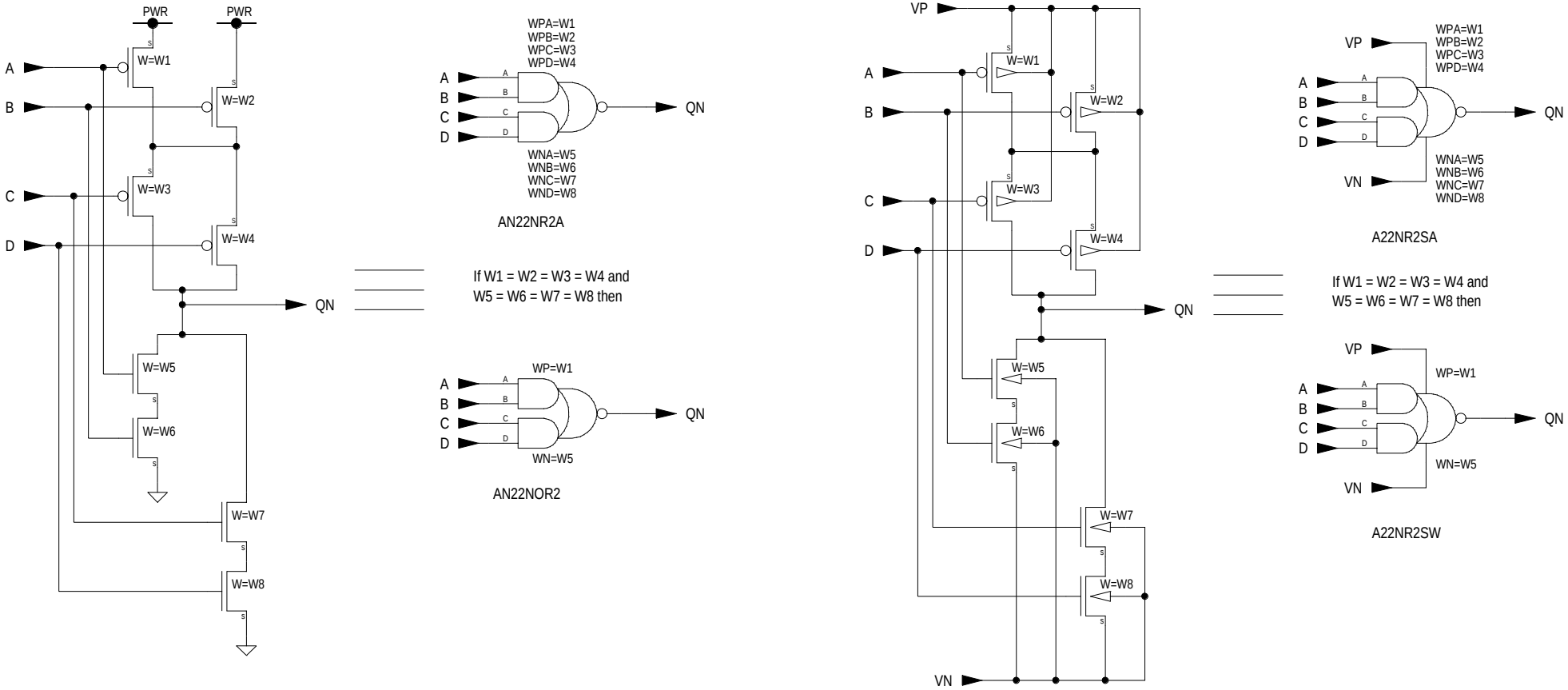
SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



PAGE 150

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	STCELL9	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:31		
LOCATION:	XX	INITIALS:	GY

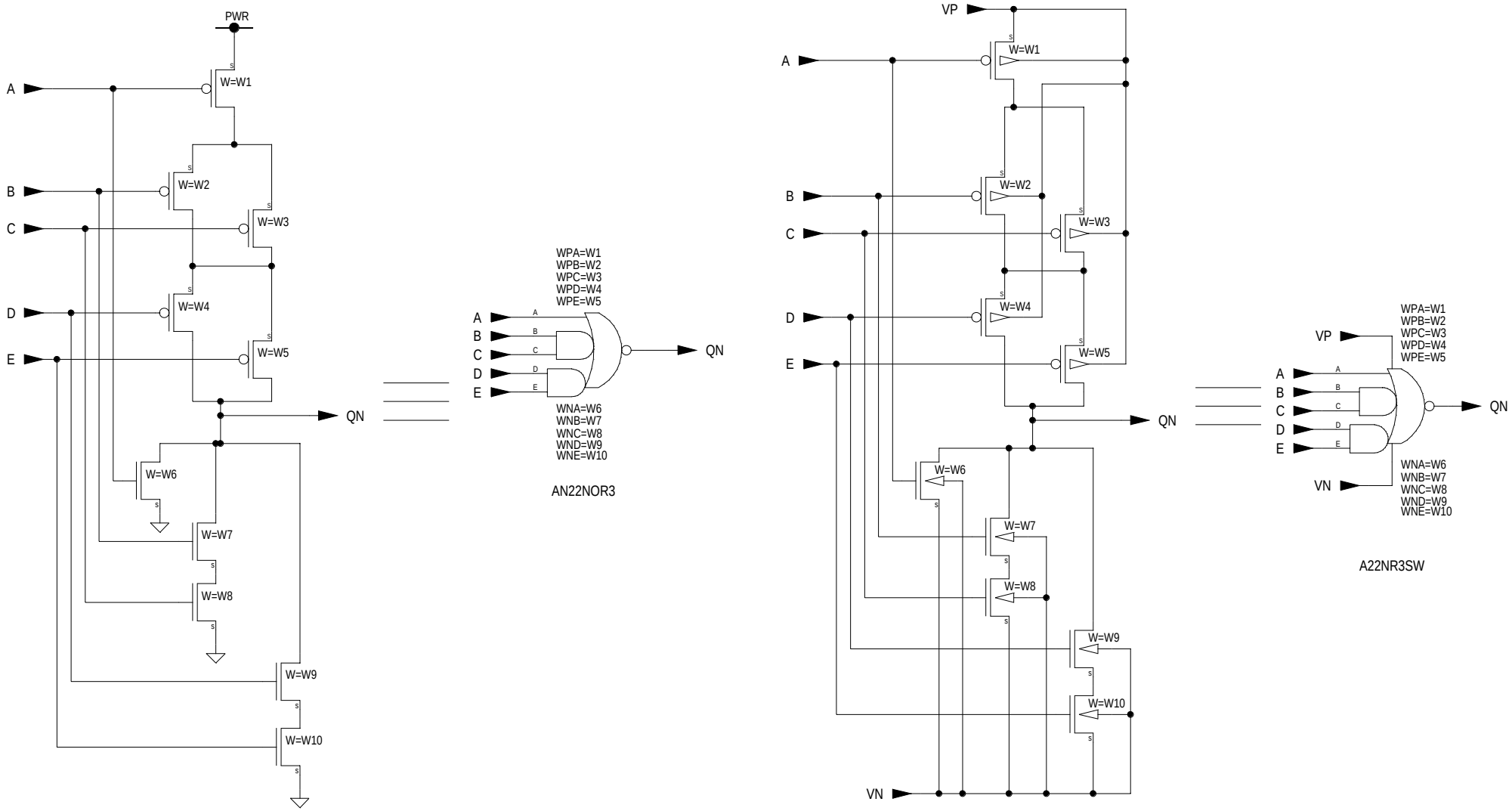
Figure 8.8 SI_LIB SYMBOL DEFINITION PAGE 9



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	STCELL10	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:30		
LOCATION:	XX	INITIALS:	GY

Figure 8.9 SI_LIB SYMBOL DEFINITION PAGE 10

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com



Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	STCELL11	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:30		
LOCATION:	XX	INITIALS:	GY

Figure 8.10 SI_LIB SYMBOL DEFINITION PAGE 11

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

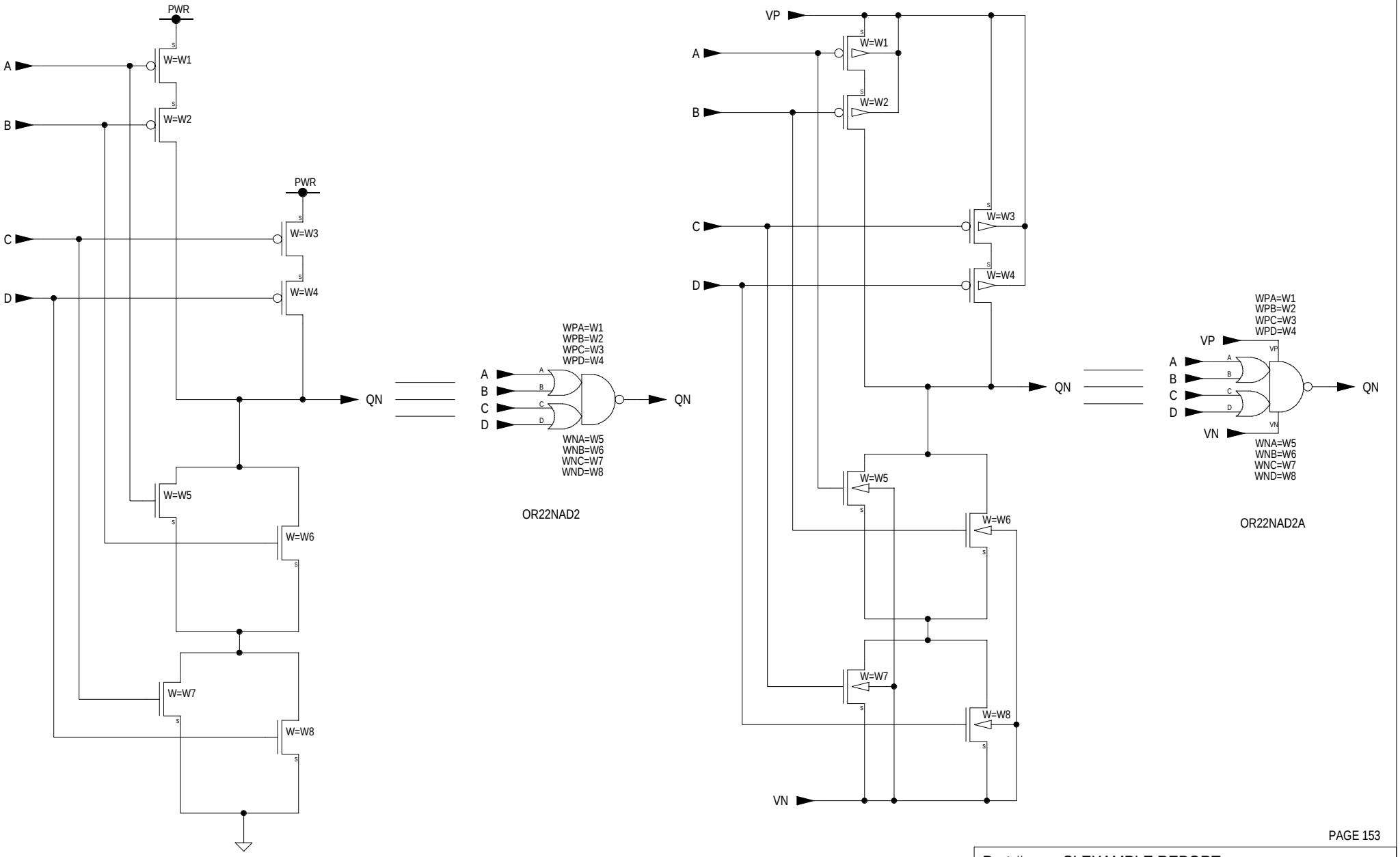


Figure 8.11 SI_LIB SYMBOL DEFINITION PAGE 12 - SIGNAL GENERATORS

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	STCELL12	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:30		
LOCATION:	XX	INITIALS:	GY

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

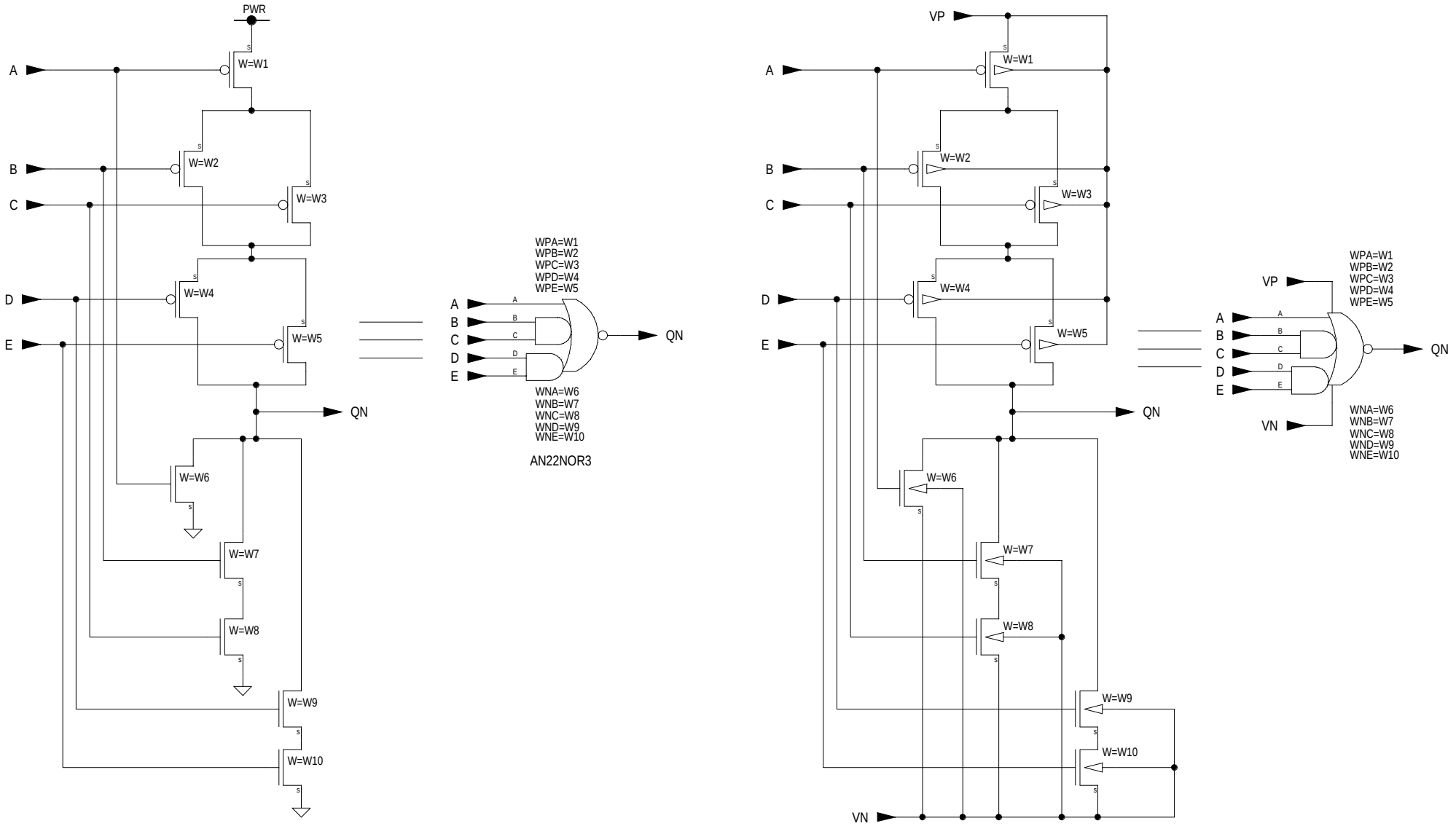


Figure 8.12 SI_LIB SYMBOL DEFINITION PAGE 13

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	STCELL13	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:30		
LOCATION:	XX	INITIALS:	GY

SEMICONDUCTOR INSIGHTS INC., 3000 SOLANDT RD., KANATA ONT., CANADA K2K 2X2 TEL: (613) 599-6500 FAX: (613) 599-6501 http://www.semiconductor.com

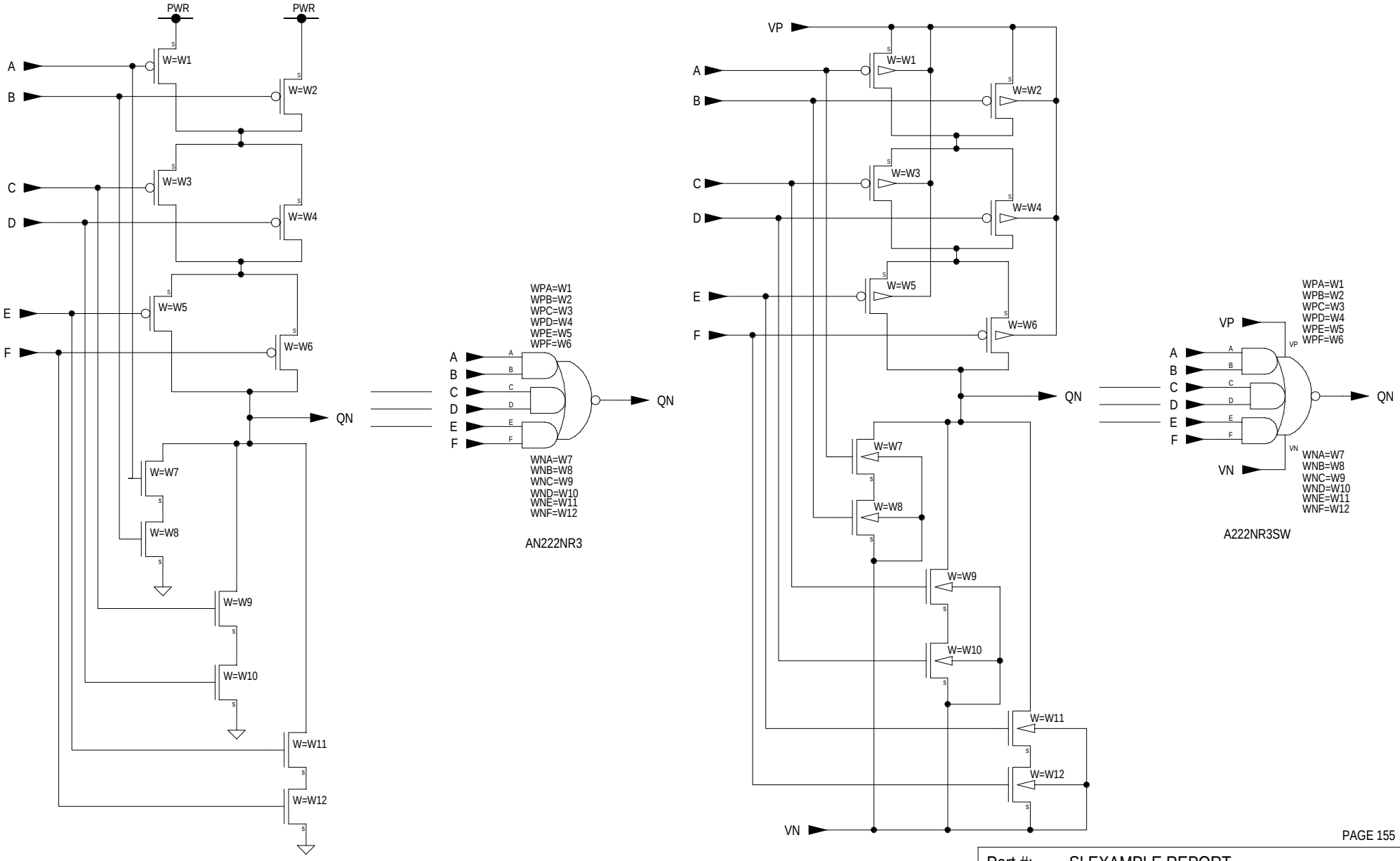


Figure 8.13 SI_LIB SYMBOL DEFINITION PAGE 14

Part #:	SI EXAMPLE REPORT		
DATE CODE:	0230		
SCH_NAME:	STCELL14	SI NUMBER:	SI01
DATE_TIME:	6-20-2002_13:30		
LOCATION:	XX	INITIALS:	GY

Appendix A – List of Signals

The following section contains a list of signals and there descriptions. The signal list is intended to aid navigation in this report by providing source and destination schematics for all signals.

Note: This signal list is an example and the figure numbers do not necessarily match with the schematics found in this report.

Signal Name	I/O	Fig. #	Signal Description
BIAS	IN	3.5	ECL Dividers Bias Voltage
BIAS	IN	3.4	ECL Dividers Bias Voltage
BIAS	IN	3.8	ECL Dividers Bias Voltage
BIAS	IN	3.2	ECL Dividers Bias Voltage
BIAS	IN	3.5.3	ECL Dividers Bias Voltage
BIAS	IN	3.6	ECL Dividers Bias Voltage
BIAS	OUT	3.1	ECL Dividers Bias Voltage
BIAS	IN	3.3	ECL Dividers Bias Voltage
BIAS	IN	3.5.4	ECL Dividers Bias Voltage
BIAS	IN	3.5.1	ECL Dividers Bias Voltage
BIAS	IN	3.7	ECL Dividers Bias Voltage
BIAS	IN	3.9	ECL Dividers Bias Voltage
BIAS	IN	3.5.2	ECL Dividers Bias Voltage
CD	OUT	6	PFD Charge Down
CD	IN	7.1	PFD Charge Down
CD	IN	7	PFD Charge Down
CD~	IN	5	Inverted CD
CD~	IN	7	Inverted CD
CD~	OUT	6	Inverted CD
CD~	IN	7.1	Inverted CD
CHP_EN	IN	7.2	Charge Pump Enable
CHP_EN	OUT	5	Charge Pump Enable
CHP_EN	IN	7	Charge Pump Enable
CHP_EN	IN	7.1	Charge Pump Enable
CHP_EN~	OUT	5	Charge Pump Enable Inverted
CHP_EN~	IN	7.1	Charge Pump Enable Inverted
CHP_EN~	IN	7.2	Charge Pump Enable Inverted
CHP_EN~	IN	7	Charge Pump Enable Inverted
CHP_VREF	IN	7.1	Charge Pump Reference Voltage
CHP_VREF	OUT	7.2	Charge Pump Reference Voltage

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

Signal Name	I/O	Fig. #	Signal Description
CLOCK_S	IN	9	Serial Interface Clock, Buffered
CU	OUT	6	PFD Charge Up
CU	IN	7	PFD Charge Up
CU	IN	7.1	PFD Charge Up
CU~	OUT	6	Inverted CU
CU~	IN	5	Inverted CU
CU~	IN	7.1	Inverted CU
CU~	IN	7	Inverted CU
DATA_S	IN	9	Serial Register Data Input, Buffered
DATA_S	IN	9.1	Serial Register Data Input, Buffered
DORX	OUT	7.1	RX Charge Pump Output
DORX	OUT	7	RX Charge Pump Output
FINRX	IN	3	RX Prescaler Input
FINRX	IN	3.2	RX Prescaler Input
FLC1	IN	7.1	Fast Lock Control 1
FLC1	OUT	7.3	Fast Lock Control 1
FLC1~	OUT	7.3	FLC1 Inverted
FLC1~	IN	7.1	FLC1 Inverted
FLC2	OUT	7.3	Fast Lock Control 2
FLC2	IN	7.1	Fast Lock Control 2
FLC2~	OUT	7.3	FLC2 Inverted
FLC2~	IN	7.1	FLC2 Inverted
FL_ENAB	OUT	9	Fast Lock Enable
FL_ENAB	IN	5	Fast Lock Enable
FL_ENAB~	IN	7.3	Fast Lock Enable, LOW Active
FL_ENAB~	IN	7	Fast Lock Enable, LOW Active
FL_ENAB~	OUT	5	Fast Lock Enable, LOW Active
FN_RX	IN	6	RX N Counter Frequency
FN_RX	OUT	5	RX N Counter Frequency
FN_RX~	IN	8.2	Inverted RX N Counter Frequency
FN_RX~	OUT	5	Inverted RX N Counter Frequency
FN_TX	IN	8.2	TX N Counter frequency
FR_RX	IN	6	RX Reference counter Frequency
FR_RX	OUT	5	RX Reference counter Frequency
FR_RX~	IN	8.2	Inverted RX Reference Counter Frequency
FR_RX~	OUT	5	Inverted RX Reference Counter Frequency
FR_TX	IN	8.2	TX Reference Counter Frequency
LDS	IN	8.2	LDS BIT (Common for RX and TX)
LDS	OUT	9	LDS BIT (Common for RX and TX)
LDS_LD	OUT	9.2	LDS BIT LOAD

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

Signal Name	I/O	Fig. #	Signal Description
LD_F_Y	IN	11.5	LD/Fout Selector Output
LD_F_Y	OUT	8.2	LD/Fout Selector Output
LE_S	IN	9	Serial Interface Latch Enable, Buffered
LE_SB	IN	9.2	Serial Interface Latch Enable, Buffered
NCT_8H	OUT	4.5	RX N Counter value less than 08/h
NCT_8H	IN	5	RX N Counter value less than 08/h
NCT_Q	IN	4.6	RX N Counter Output
NCT_Q	OUT	4.5	RX N Counter Output
NCT_Q	IN	5	RX N Counter Output
NCT_Q	IN	4.3	RX N Counter Output
NCT_RES	OUT	5	RX N Counter output FF Reset
NCT_RES	IN	4.5	RX N Counter output FF Reset
NCT_RES	IN	4.3	RX N Counter output FF Reset
N_R[11:1]~	BUS	2	N Counter Reset BUS
N_R[11:1]~	BUS	4.6	N Counter Reset BUS
N_R[11:1]~	OUT	4.6	N Counter Reset BUS
N_R[11:1]~	BUS	4.5	N Counter Reset BUS
N_R[11:1]~	IN	4.5	N Counter Reset BUS
N_S[11:1]~	BUS	4.6	N Counter SET BUS
N_S[11:1]~	BUS	2	N Counter SET BUS
N_S[11:1]~	OUT	4.6	N Counter SET BUS
N_S[11:1]~	IN	4.5	N Counter SET BUS
N_S[11:1]~	BUS	4.5	N Counter SET BUS
OSCIN	IN	10	Reference Frequency from OSCin Pad
PHDIFF~	OUT	6	Phase Difference, Active Low
PHDIFF~	IN	7	Phase Difference, Active Low
PHDIFF~	IN	7.3	Phase Difference, Active Low
PHDIFF~	IN	8.1	Phase Difference, Active Low
PSRX_B	OUT	11.4	PSRX from Input Buffer
PSRX_B	IN	5	PSRX from Input Buffer
PSRX_BB	IN	8.1	Logic Equivalent of PSRX_B
PSRX_BB	OUT	5	Logic Equivalent of PSRX_B
RCT_8H	IN	5	RX Reference Counter value less than 08/h
RCT_8H	OUT	4.1	RX Reference Counter value less than 08/h
RCT_Q	IN	5	RX Reference Counter Underflow (=0001/h)
RCT_Q	IN	4.2	RX Reference Counter Underflow (=0001/h)
RCT_Q	OUT	4.1	RX Reference Counter Underflow (=0001/h)
RCT_RES	IN	4.1	RX Reference Counter output FF Reset
RCT_RES	OUT	5	RX Reference Counter output FF Reset
REF1	OUT	3.1	ECL FFLOP Reference Voltage

Signal Name	I/O	Fig. #	Signal Description
REF1	IN	3.3	ECL FFLOP Reference Voltage
REF2	IN	3.7	ECL Buffers Reference Voltage
REF2	IN	3.8	ECL Buffers Reference Voltage
REF2	OUT	3.1	ECL Buffers Reference Voltage
REF2	IN	3.9	ECL Buffers Reference Voltage
REF_R[14:1]~	IN	4.1	REF Counter RESET BUS
REF_R[14:1]~	BUS	2	REF Counter RESET BUS
REF_R[14:1]~	BUS	4.2	REF Counter RESET BUS
REF_R[14:1]~	BUS	4.1	REF Counter RESET BUS
REF_R[14:1]~	OUT	4.2	REF Counter RESET BUS
REF_S[14:1]~	OUT	4.2	REF Counter SET BUS
REF_S[14:1]~	BUS	4.2	REF Counter SET BUS
REF_S[14:1]~	BUS	2	REF Counter SET BUS
REF_S[14:1]~	BUS	4.1	REF Counter SET BUS
REF_S[14:1]~	IN	4.1	REF Counter SET BUS
RXIN	OUT	3.2	RX Preamplifier Output
RXIN~	OUT	3.2	Complementary RX Preamplifier Output
RX_CS	IN	7	RX Charge Pump Current Setting
RX_CS	IN	7.1	RX Charge Pump Current Setting
RX_CS	OUT	9	RX Charge Pump Current Setting
RX_CS~	IN	7	RX_CS Inverted
RX_CS~	OUT	9	RX_CS Inverted
RX_CS~	IN	7.1	RX_CS Inverted
RX_FC	OUT	9	RX FC BIT
RX_FC	IN	6	RX FC BIT
RX_LDET	IN	8.2	RX Lock Detect Bit
RX_LDET	OUT	8.1	RX Lock Detect Bit
RX_LD_RES	IN	8.1	RX Lock Detector Reset
RX_LD_RES	OUT	5	RX Lock Detector Reset
RX_OSC	OUT	10	OSCIn Input for RX Synthesizer
RX_OSCB	IN	4.1	Buffered RX_OSC
RX_OSCB	IN	5	Buffered RX_OSC
RX_OSCB_D2	OUT	4.1	RX_OSCB Clock divided by 2
RX_OSCB_D2	IN	8.1	RX_OSCB Clock divided by 2
RX_OSCB~	IN	5	Inverted RX_OSC
RX_OSCB~	IN	4.1	Inverted RX_OSC
RX_PFD_RES	IN	6	RX Phase Frequency Detector Reset
RX_PFD_RES	OUT	5	RX Phase Frequency Detector Reset
RX_PRESC_Y	OUT	3	RX Prescaler Output
RX_PRESC_YA	IN	4.5	RX_PRESC_Y Buffered

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

Signal Name	I/O	Fig. #	Signal Description
RX_PRESC_YA	IN	5	RX_PRESC_Y Buffered
RX_PRESC_YA~	IN	4.5	RX_PRESC_Y Inverted
RX_PRESC_YA~	IN	5	RX_PRESC_Y Inverted
RX_PRESC_YB	IN	4.3	RX_PRESC_Y Buffered
RX_PRESC_YB~	IN	4.3	RX_PRESC_Y Inverted
RX_P_EN	IN	3	RX Prescaler Enable
RX_P_EN	IN	10	RX Prescaler Enable
RX_P_EN	IN	3.1	RX Prescaler Enable
RX_P_EN~	OUT	5	RX Prescaler Enable. LOW Active
RX_P_EN~	IN	3	RX Prescaler Enable. LOW Active
RX_REF_LD	OUT	9	RX Reference Counter Ratio Load
RX_REF_LD	IN	4.2	RX Reference Counter Ratio Load
RX_REF_LD	OUT	9.2	RX Reference Counter Ratio Load
RX_SN_LD	IN	4.6	RX Swallow/N-Counter Ratios Load
RX_SN_LD	IN	4.4	RX Swallow/N-Counter Ratios Load
RX_SN_LD	OUT	9.2	RX Swallow/N-Counter Ratios Load
RX_SN_LD	OUT	9	RX Swallow/N-Counter Ratios Load
RX_SW	IN	3	RX Prescaler Divide Ratio setting
RX_SW_B	OUT	9	RX SW Bit (RX Prescaler Ratio Setting)
SR_CK	IN	9.1	Serial Register Clock
SR_OUT1	IN	9.2	CN1 Bit
SR_OUT1~	IN	9.2	CN1 Bit, Inverted
SR_OUT1~	OUT	9.1	CN1 Bit, Inverted
SR_OUT2	IN	9.2	CN2 Bit
SR_OUT2~	IN	9.2	CN2 Bit, Inverted
SR_OUT2~	OUT	9.1	CN2 Bit, Inverted
SR_OUT[12:6]	BUS	4.4	Serial Register Output BUS
SR_OUT[12:6]	IN	4.4	Serial Register Output BUS
SR_OUT[12:6]	BUS	2	Serial Register Output BUS
SR_OUT[18:5]	IN	4.2	Serial Register Output BUS
SR_OUT[18:5]	BUS	2	Serial Register Output BUS
SR_OUT[18:5]	BUS	4.2	Serial Register Output BUS
SR_OUT[23:13]	BUS	2	Serial Register Output BUS
SR_OUT[23:13]	BUS	4.6	Serial Register Output BUS
SR_OUT[23:13]	IN	4.6	Serial Register Output BUS
SR_OUT[23:1]	OUT	9.1	Serial Interface Register Output BUS
SR_OUT[23:1]	BUS	9.1	Serial Interface Register Output BUS
SR_OUT[23:1]	BUS	9	Serial Interface Register Output BUS
SR_OUT[23:5]	OUT	9	Serial Register Output BUS
SR_OUT[23:5]	BUS	2	Serial Register Output BUS

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

Signal Name	I/O	Fig. #	Signal Description
SR_OUT[23:5]	BUS	9	Serial Register Output BUS
SWCT_Q	IN	4.4	Swallow Counter Output
SWCT_Q	OUT	4.3	Swallow Counter Output
SWEN	OUT	4.3	Swallow Enable (RX Prescaler)
SWEN	IN	3	Swallow Enable (RX Prescaler)
SW_R[7:1]~	OUT	4.4	Swallow Counter Reset BUS
SW_R[7:1]~	BUS	4.3	Swallow Counter Reset BUS
SW_R[7:1]~	BUS	2	Swallow Counter Reset BUS
SW_R[7:1]~	IN	4.3	Swallow Counter Reset BUS
SW_R[7:1]~	BUS	4.4	Swallow Counter Reset BUS
SW_S[7:1]~	IN	4.3	Swallow Counter SET BUS
SW_S[7:1]~	OUT	4.4	Swallow Counter SET BUS
SW_S[7:1]~	BUS	2	Swallow Counter SET BUS
SW_S[7:1]~	BUS	4.3	Swallow Counter SET BUS
SW_S[7:1]~	BUS	4.4	Swallow Counter SET BUS
T1	OUT	9	T1 BIT (Common for RX and TX)
T1	IN	8.2	T1 BIT (Common for RX and TX)
T1_T2_LD	OUT	9.2	T1 and T2 Bits Load
T2	OUT	9	T2 BIT (Common for RX and TX)
T2	IN	8.2	T2 BIT (Common for RX and TX)
TX_CS	OUT	9	TX CS BIT
TX_CS~	OUT	9	Inverted TX_CS
TX_FC	OUT	9	TX FC Bit
TX_LDET	IN	8.2	TX Lock Detect Bit
TX_OSC	OUT	10	OSCin Input to TX Synthesizer
TX_P_EN	IN	10	From TX Synthesizer Logic
TX_REF_LD	OUT	9	TX Reference Counter Ratio Load
TX_REF_LD	OUT	9.2	TX Reference Counter Ratio Load
TX_SN_LD	OUT	9.2	TX Swallow/N-Counter Ratios Load
TX_SN_LD	OUT	9	TX Swallow/N-Counter Ratios Load
TX_SW	OUT	9	TX SW Bit
VCCRX_1	IN	3	RX Section Power Supply
VCCRX_2	IN	7	RX Section Power Supply
VCCRX_2	IN	11.4	RX Section Power Supply
VCCRX_2R	IN	7.3	RX Charge Pump logic Power Supply
VCCRX_2R	IN	7.1	RX Charge Pump logic Power Supply
VCCTX_2	IN	10	TX Section and Serial Interface Power Supply
VCCTX_2	IN	11.5	TX Section and Serial Interface Power Supply
VPRX	IN	7.1	RX Charge Pump Power Supply
VPRX	IN	7	RX Charge Pump Power Supply

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

Signal Name	I/O	Fig. #	Signal Description
XFINRX	IN	3	Complementary RX Prescaler Input
XFINRX	IN	3.2	Complementary RX Prescaler Input
[CLOCK]	IN	2	Serial Interface Clock Input PAD
[DATA]	IN	2	Serial Interface Data Input PAD
[DORX]	OUT	2	RX Charge Pump Output PAD
[FINRX]	IN	2	RX Prescaler Input PAD
[LD/FOUT]	OUT	2	RX/TX Lock Detect Output PAD
[LE]	IN	2	Load Enable, Serial Interface Input PAD
[OSCIN]	IN	2	Reference Frequency Input PAD
[PSRX]	IN	2	RX Power Saving Mode Control Input PAD
[VCCRX_1]	IN	2	RX Section Power Supply PAD 1
[VCCRX_2]	IN	2	RX Section Power Supply PAD 2
[VCCTX_2]	IN	2	TX Section and Serial Interface Power Supply PAD 2
[VPRX]	IN	2	RX Charge Pump Power Supply PAD
[XFINRX]	IN	2	Complementary RX Prescaler Input PAD

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com

3000 Solandt Road, Kanata, ON, Canada K2K 2X2
Tel: (613) 599-6500 Fax: (613) 599-6501
Web Site: http://www.semiconductor.com