SDRAM Timing Diagram

* Samsung Electronics reserves the right to change products or specification without notice.

Single Bit Read - Write - Read Cycle(Same Page) @CAS Latency=3, Burst Length=1
Power Up Sequence
Read & Write Cycle at Same Bank @Burst Length=4, tRDL=1CLK
Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK
Page Read & Write Cycle at Same Bank @Burst Length=4, tRDL=1CLK
Page Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK
Page Read Cycle at Different Bank @Burst Length=4
Page Write Cycle at Different Bank @Burst Length=4, tRDL=1CLK
Page Write Cycle at Different Bank @Burst Length=4, tRDL=2CLK
Read & Write Cycle at Different Bank @Burst Length=4
Read & Write Cycle With Auto Precharge I @Burst Length=4
Read & Write Cycle With Auto Precharge II @Burst Length=4
Clock Suspension & DQM Operation Cycle @CAS Letency=2, Burst Length=4
Read Interrupted by Precharge Command & Read Burst Stop Cycle @ Full Page Burst
Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, tRDL=1CLK
Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, tRDL=2CLK
Burst Read Single bit Write Cycle @Burst Length =2
Active/precharge Power Dower Down Mode @CAS Latency=2 Burst Length=4
Self Refresh Entry & Exit Cycle & Exit Cycle
Mode Register Set Cycle
Auto Refresh Cycle

Single Bit Read-Write-Read Cycle(Same Page) @CAS Latency=3, Burst Length=1

CLOCK 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
tCH tCL tCC
CKE HIGH
tRAS tRC
*Note 1
CS tSH tSS tRCD tRP
RAS tSH tSS tCCD
CAS tSH tSS
ADDR tSH tSS Ra Ca Cb Cc Rb
*Note 2 *Note 2,3 *Note 2,3 *Note 2,3 *Note 4 *Note 2
BA0 ~ BA1 BS BS BS BS BS BS
*Note 3 *Note 3 *Note 3 *Note 4
A10/AP Ra Rb
tRAC tSAC tSH
DQ Qa Db Qc
tSLZ tOH tSS
tSH
WE tSS
tSS tSH
DQM

Row Active Read Write Read Precharge Row Active

: Don't care

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***Note :** 1. All input except CKE & DQM can be don't care when $\overline{CS}$ is high at the CLK high going edge.
2. Bank active & read/write are controlled by BA0~BA1.

64Mb/128Mb		256Mb		Active & Read/Write
BA0	BA1	BA0	BA1	
0	0	0	0	Bank A
0	1	1	0	Bank B
1	0	0	1	Bank C
1	1	1	1	Bank D

For 16Mb only

BA	Active & Read/Write
0	Bank A
1	Bank B

3. Enable and disable auto precharge function are controlled by A10/AP in read/write command

A10/AP	64Mb/128Mb		256Mb		Operation
	BA0	BA1	BA0	BA1	
0	0	0	0	0	Disable auto precharge, leave bank A active at end of burst.
	0	1	1	0	Disable auto precharge, leave bank B active at end of burst.
	1	0	0	1	Disable auto precharge, leave bank C active at end of burst.
	1	1	1	1	Disable auto precharge, leave bank D active at end of burst.
1	0	0	0	0	Enable auto precharge, precharge bank A at end of burst.
	0	1	1	0	Enable auto precharge, precharge bank B at end of burst.
	1	0	0	1	Enable auto precharge, precharge bank C at end of burst.
	1	1	1	1	Enable auto precharge, precharge bank D at end of burst.

For 16Mb only

A10/AP	BA	Operation
0	0	Disable auto precharge, leave bank A active at end of burst.
	1	Disable auto precharge, leave bank B active at end of burst.
1	0	Enable auto precharge, precharge bank A at end of burst.
	1	Enable auto precharge, precharge bank B at end of burst.

4. A10/AP and BA0~BA1 control bank precharge when precharge command is asserted.

A10/AP	64Mb/128Mb		256Mb		Precharge
	BA0	BA1	BA0	BA1	
0	0	0	0	0	Bank A
0	0	1	1	0	Bank B
0	1	0	0	1	Bank C
0	1	1	1	1	Bank D
1	x	x	x	x	All Banks

For 16Mb only

A10/AP	BA	Precharge
0	0	Bank A
0	1	Bank B
1	X	Both Banks

Power Up Sequence

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

CLOCK

CKE *High level is necessary*

CS

tRP tRC tRC

RAS

CAS

ADDR Key RAa

BA_0

BA_1

A_{10}/AP RAa

DQ High-Z

WE

DQM *High level is necessary*

Precharge (All Banks)

Auto Refresh

Auto Refresh

Mode Register Set

Row Active (A-Bank)

: Don't care

ELECTRONICS

Read & Write Cycle at Same Bank @Burst Length=4, tRDL=1CLK

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

CLOCK

CKE — HIGH

tRC *Note 1

CS

tRCD

RAS

*Note 2

CAS

ADDR: RAa, CAa, RAb, CAb

BA_0

BA_1

A_{10}/AP: Ra, RAb

DQ

CL=2: QAa0 QAa1 QAa2 QAa3, DAb0 DAb1 DAb2 DAb3; tOH; tRAC *Note 3; tSAC; tSHZ *Note 4; tRDL

CL=3: QAa0 QAa1 QAa2 QAa3, DAb0 DAb1 DAb2 DAb3; tOH; tRAC *Note 3; tSAC; tSHZ *Note 4; tRDL

WE

DQM

Row Active (A-Bank) | Read (A-Bank) | Precharge (A-Bank) | Row Active (A-Bank) | Write (A-Bank) | Precharge (A-Bank)

: Don't care

***Note :**
1. Minimum row cycle times is required to complete internal DRAM operation.
2. Row precharge can interrupt burst on any cycle. [CAS Latency - 1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(t_{SHZ}) after the clcok.
3. Access time from Row active command. t_{CC} *(t_{RCD} + CAS latency - 1) + t_{SAC}
4. Ouput will be Hi-Z after the end of burst. (1, 2, 4, 8 & Full page bit burst)

Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK

***Note :**
1. Minimum row cycle times is required to complete internal DRAM operation.
2. Row precharge can interrupt burst on any cycle. [CAS Latency - 1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(t_{SHZ}) after the clcok.
3. Access time from Row active command. t_{CC} *(t_{RCD} + CAS latency - 1) + t_{SAC}
4. Ouput will be Hi-Z after the end of burst. (1, 2, 4, 8 & Full page bit burst)

Page Read & Write Cycle at Same Bank @Burst Length=4, tRDL=1CLK

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

CLOCK

CKE HIGH

$\overline{CS}$ tRCD

$\overline{RAS}$ *Note 2

$\overline{CAS}$

ADDR RAa CAa CAb CAc CAd RAb

BA0

BA1

A10/AP RAa RAb

tRDL

DQ CL=2 QAa0 QAa1 QAb0 QAb1 QAb2 DAc0 DAc1 DAd0 DAd1

tDAL *Note 4

CL=3 QAa0 QAa1 QAb0 QAb1 DAc0 DAc1 DAd0 DAd1

tCDL

$\overline{WE}$

DQM *Note 1 *Note 3

Row Active (A-Bank) | Read (A-Bank) | Read (A-Bank) | Write (A-Bank) | Write (A-Bank) | Precharge (A-Bank) | Row Active (A-Bank)

: Don't care

***Note :** 1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.
2. Row precharge will interrupt writing. Last data input, tRDL before Row precharge, will be written.
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
4. tDAL, last data in to active delay, is 1CLK + 20ns

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Page Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK

Row Active (A-Bank) | Read (A-Bank) | Read (A-Bank) | Write (A-Bank) | Write (A-Bank) | Precharge (A-Bank) | Row Active (A-Bank)

: Don't care

***Note :**

1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.
2. Row precharge will interrupt writing. Last data input, tRDL before Row precharge, will be written.
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
4. tDAL ,last data in to active delay, is 2CLK + 20ns.

Page Read Cycle at Different Bank @Burst Length=4

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

CLOCK

CKE HIGH

*Note 1

$\overline{CS}$

$\overline{RAS}$ *Note 2

$\overline{CAS}$

ADDR RAa RBb CAa RCc CBb RDd CCc CDd

BA_0

BA_1

A_{10}/AP RAa RBb RCc RDd

DQ

CL=2 QAa0 QAa1 QAa2 QBb0 QBb1 QBb2 QCc0 QCc1 QCc2 QDd0 QDd1 QDd2

CL=3 QAa0 QAa1 QAa2 QBb0 QBb1 QBb2 QCc0 QCc1 QCc2 QDd0 QDd1 QDd2

$\overline{WE}$

DQM

Row Active (A-Bank)
Row Active (B-Bank)
Read (A-Bank)
Row Acive (C-Bank)
Read (B-Bank)
Precharge (A-Bank)
Row Active (D-Bank)
Read (C-Bank)
Precharge (B-Bank)
Read (D-Bank)
Precharge (C-Bank)
Precharge (D-Bank)

: Don't care

***Note :** 1. $\overline{CS}$ can be don't cared when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high at the clock high going dege.

2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

Page Write Cycle at Different Bank @Burst Length=4, tRDL=1CLK

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

CLOCK

CKE HIGH

$\overline{CS}$

$\overline{RAS}$ *Note 2

$\overline{CAS}$

ADDR RAa RBb CAa CBb RCc RDd CCc CDd

BA_0

BA_1

A_{10}/AP RAa RBb RCc RDd

DQ DAa0 DAa1 DAa2 DAa3 DBb0 DBb1 DBb2 DBb3 DCc0 DCc1 DDd0 DDd1 DDd2

tCDL tRDL

$\overline{WE}$ *Note 1

DQM

Row Active (A-Bank)
Row Active (B-Bank)
Write (A-Bank)
Write (B-Bank)
Row Active (C-Bank)
Row Active (D-Bank)
Write (C-Bank)
Write (D-Bank)
Precharge (All Banks)

: Don't care

***Note :** 1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt burst write by Row precharge, both the write and the precharge banks must be the same.

ELECTRONICS

Page Write Cycle at Different Bank @Burst Length=4, tRDL=2CLK

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

CLOCK

CKE HIGH

CS

RAS *Note 2

CAS

ADDR RAa RBb CAa CBb RCc RDd CCc CDd

BA0

BA1

A10/AP RAa RBb RCc RDd

DQ DAa0 DAa1 DAa2 DAa3 DBb0 DBb1 DBb2 DBb3 DCc0 DCc1 DDd0 DDd1 DDd2

tCDL tRDL

WE

DQM *Note 1

Row Active (A-Bank)

Row Active (B-Bank)

Write (A-Bank)

Write (B-Bank)

Row Active (C-Bank)

Row Active (D-Bank)

Write (C-Bank)

Write (D-Bank)

Precharge (All Banks)

: Don't care

***Note :** 1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt burst write by Row precharge, both the write and the precharge banks must be the same.

Read & Write Cycle at Different Bank @Burst Length=4

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

CLOCK

CKE HIGH

$\overline{CS}$

$\overline{RAS}$

$\overline{CAS}$

ADDR RAa CAa RDb CDb RBc CBc

BA_0

BA_1

A_{10}/AP RAa RDb RBc

tCDL *Note 1

DQ

CL=2 QAa0 QAa1 QAa2 QAa3 DDb0 DDb1 DDb2 DDb3 QBc0 QBc1 QBc2

CL=3 QAa0 QAa1 QAa2 QAa3 DDb0 DDb1 DDb2 DDb3 QBc0 QBc1

$\overline{WE}$

DQM

Row Active (A-Bank) Read (A-Bank) Precharge (A-Bank) Write (D-Bank) Read (B-Bank)

Row Active (D-Bank) Row Active (B-Bank)

: Don't care

***Note :** 1. t_{CDL} should be met to complete write.

Read & Write Cycle with Auto Precharge I @Burst Length=4

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

CLOCK

CKE HIGH

$\overline{CS}$

$\overline{RAS}$

$\overline{CAS}$

ADDR RAa RBb CAa CBb RAc CAc

BA_0

BA_1

A_{10}/AP RAa RBb RAc

DQ CL=2 QAa0 QAa1 QBb0 QBb1 QBb2 QBb3 DAc0 DAc1

CL=3 QAa0 QAa1 QBb0 QBb1 QBb2 QBb3 DAc0 DAc1

$\overline{WE}$

DQM

Row Active (A-Bank)

Row Active (B-Bank)

Read with Auto Pre charge (A-Bank)

Read without Auto precharge(B-Bank) Auto Precharge Start Point (A-Bank)*Note1

Precharge (B-Bank)

Row Active (A-Bank)

Write with Auto Precharge (A-Bank)

: Don't care

***Note1:** When Read(Write) command with auto precharge is issued at A-Bank after A and B Bank activation.

- if Read(Write) command without auto precharge is issued at B-Bank before A-Bank auto precharge starts, A-Bank auto precharge will start at B-Bank read command input point .
- any command can not be issued at A-Bank during tRP after A-Bank auto precharge starts.

Read & Write Cycle with Auto Precharge II @Burst Length=4

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

CLOCK

CKE HIGH

$\overline{CS}$

$\overline{RAS}$

$\overline{CAS}$

ADDR Ra Ca Rb Cb

BA0

BA1

A10/AP Ra Rb

DQ CL=2 Qa0 Qa1 Qa2 Qa3 Qb0 Qb1 Qb2 Qb3

CL=3 Qa0 Qa1 Qa2 Qa3 Qb0 Qb1 Qb2 Qb3

$\overline{WE}$

DQM

*Note1

Row Active (A-Bank)

Read with Auto Precharge (A-Bank)

Auto Precharge Start Point (A-Bank) Row Active (B-Bank)

Read with Auto Precharge (B-Bank)

Auto Precharge Start Point (B-Bank)

: Don't care

***Note 1:** Any command to A-bank is not allowed in this period.
tRP is determined from at auto precharge start point

ELECTRONICS

Clock Suspension & DQM Operation Cycle @CAS Latency=2, Burst Length=4

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

CLOCK

CKE

$\overline{CS}$

$\overline{RAS}$

$\overline{CAS}$

ADDR: Ra, Ca, Cb, Cc

BA_0

BA_1

A_{10}/AP: Ra

DQ: Qa0, Qa1, Qa2, Qa3, tSHZ, Qb0, Qb1, tSHZ, Dc0, Dc2

$\overline{WE}$

DQM: *Note 1

Row Active

Read

Clock Suspension

Read

Read DQM

Write

Write DQM

Clock Suspension

Write DQM

: Don't care

***Note1 :** DQM is needed to prevent bus contention.

Read Interrupted by Precharge Command & Read Burst Stop Cycle @ Full Page Burst

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

CLOCK

CKE HIGH

$\overline{CS}$

$\overline{RAS}$

$\overline{CAS}$

ADDR RAa CAa CAb

BA_0

BA_1

A_{10}/AP RAa

DQ

CL=2 QAa0 QAa1 QAa2 QAa3 QAa4 [1] QAb0 QAb1 QAb2 QAb3 QAb4 QAb5 [1]

CL=3 QAa0 QAa1 QAa2 QAa3 QAa4 [2] QAb0 QAb1 QAb2 QAb3 QAb4 QAb5 [2]

$\overline{WE}$

DQM

Row Active (A-Bank)

Read (A-Bank)

Burst Stop

Read (A-Bank)

Precharge (A-Bank)

: Don't care

***Note :**
1. At full page mode, burst is finished by burst stop or precharge.
2. About the valid DQs after burst stop, it is same as the case of $\overline{RAS}$ interrupt.
   Both cases are illustrated above timing diagram. See the label 1, 2 on them.
   But at burst write, Burst stop and $\overline{RAS}$ interrupt should be compared carefully.
   Refer the timing diagram of "Full page write burst stop cycle".
3. Burst stop is valid at every burst length.

Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, tRDL=1CLK

***Note :**

1. At full page mode, burst is finished by burst stop or precharge.
2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of tRDL.
   DQM at write interrupted by precharge command is needed to prevent invalid write.
   DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
3. Burst stop is valid at every burst length.

Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, tRDL=2CLK

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

CLOCK

CKE — HIGH

$\overline{CS}$

$\overline{RAS}$

$\overline{CAS}$

ADDR — RAa, CAa, CAb

BA_0

BA_1

A_{10}/AP — RAa

tBDL *Note 1

tRDL *Note 1,2

DQ — DAa0 DAa1 DAa2 DAa3 DAa4 DAb0 DAb1 DAb2 DAb3 DAb4 DAb5

$\overline{WE}$

DQM

Row Active (A-Bank)

Write (A-Bank)

Burst Stop

Write (A-Bank)

Precharge (A-Bank)

: Don't care

***Note :**

1. At full page mode, burst is finished by burst stop or precharge.
2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of tRDL.
   DQM at write interrupted by precharge command is needed to prevent invalid write.
   DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
3. Burst stop is valid at every burst length.

Burst Read Single bit Write Cycle @Burst Length=2

***Note :**
1. BRSW modes is enabled by setting A_9 "High" at MRS (Mode Register Set).
   At the BRSW Mode, the burst length at write is fixed to "1" regardless of programmed burst length.
2. When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated.
   Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command,
   the next cycle starts the precharge.

Active/Precharge Power Down Mode @CAS Latency=2, Burst Length=4

CLOCK 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

CKE tSS *Note 1 *Note 2 *Note 3 tSS tSS *Note 2

CS

RAS

CAS

ADDR Ra Ca

BA

A10/AP Ra

DQ tSHZ Qa0 Qa1 Qa2

WE

DQM

Precharge Power-down Entry

Precharge Power-down Exit

Row Active

Active Power-down Entry

Active Power-down Exit

Read

Precharge

: Don't Care

***Note :**

1. Both banks should be in idle state prior to entering precharge power down mode.
2. CKE should be set high at least 1CLK + tss prior to Row active command.
3. Can not violate minimum refresh specification. (64ms)

Self Refresh Entry & Exit Cycle

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

CLOCK

CKE

CS

RAS

CAS

ADDR

BA0~BA1

A10/AP

DQ

WE

DQM

*Note 1 *Note 2 *Note 3 *Note 4 *Note 5 *Note 6 *Note 7

tSS

tRCmin

Hi-Z Hi-Z

Self Refresh Entry

Self Refresh Exit

Auto Refresh

: Don't care

***Note : TO ENTER SELF REFRESH MODE**

1. CS, RAS & CAS with CKE should be low at the same clcok cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in self refresh mode as long as CKE stays "Low".
   cf.) Once the device enters self refresh mode, minimum tRAS is required before exit from self refresh.

TO EXIT SELF REFRESH MODE

4. System clock restart and be stable before returning CKE high.
5. CS starts from high.
6. Minimum tRC is required after CKE going high to complete self refresh exit.
7. 4K cycle(64Mb ,128Mb) or 8K cycle(256Mb) of burst auto refresh is required before self refresh entry and after self refresh exit if the system uses burst refresh.

Mode Register Set Cycle

0 1 2 3 4 5 6

CLOCK

CKE HIGH

$\overline{CS}$

*Note 2

$\overline{RAS}$

*Note 1

$\overline{CAS}$

*Note 3

ADDR Key Ra

DQ Hi-Z

$\overline{WE}$

DQM

MRS

New Command

Auto Refresh Cycle

0 1 2 3 4 5 6 7 8 9 10

CLOCK

CKE HIGH

$\overline{CS}$

tRC

$\overline{RAS}$

$\overline{CAS}$

ADDR

DQ Hi-Z

$\overline{WE}$

DQM

Auto Refresh

New Command

: Don't care

* All banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

MODE REGISTER SET CYCLE

***Note :** 1. $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, & $\overline{WE}$ activation at the same clock cycle with address key will set internal mode register.

2. Minimum 2 clock cycles should be met before new $\overline{RAS}$ activation.

3. Please refer to Mode Register Set table.