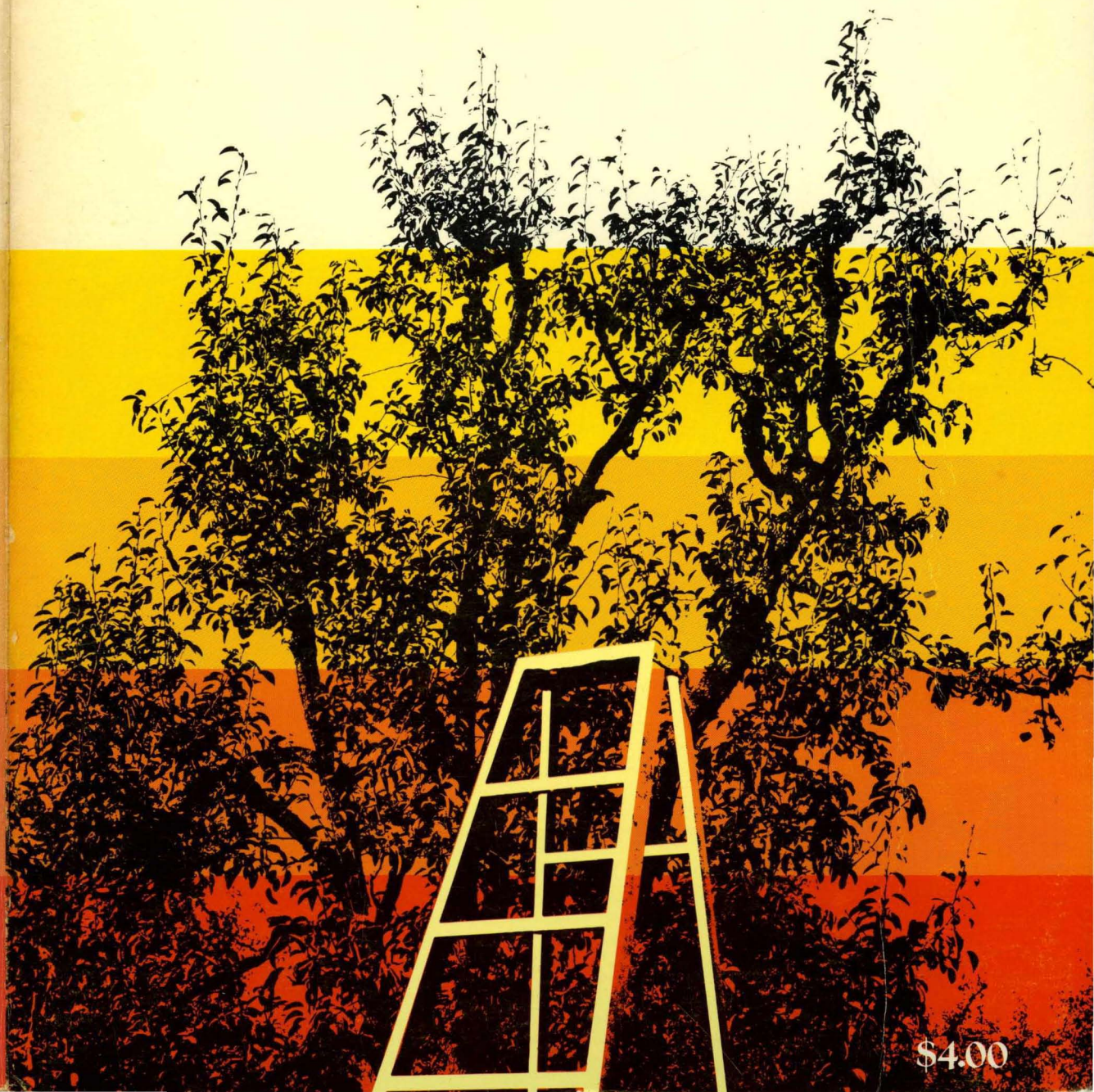
Siliconix

Analog Switches and Their Applications



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Siliconix incorporated, 1976

Preface

An abundance of literature is available on discrete semiconductor devices and integrated circuits, wherein the applications emphasis is mainly on linear and digital circuitry. Furthermore, most written information on sample-and-hold circuits, analog-to-digital and digital-to-analog converters, multiplexers and N-Channel filters tend to concentrate on systems considerations. Comparatively little has been written on the subject which bridges the linear and digital fields, namely analog switching and the effects that analog switches have on system performance.

The object of this book is to introduce the reader to FET analog switches and familiarize him with the way that the switch control or driver circuit affects switch performance. By developing an understanding of the circuit combinations that can be used for analog switching, the reader is then able to analyze the effects on system performance. With this objective in mind the contents are divided into seven chapters.

With the exception of chapters one and seven, all chapters are subdivided into two major sections. The first subsection is a theoretical discussion of analog switches. The second subsection is practical application circuits.

Chapter one is an introduction to the FET as a switch, the second chapter describes various driver circuits and their interaction with FET switches. The next four chapters are devoted to describing the performance of Analog Switches in four different fields of signal handling. Chapter seven contains a collection of applications material written by Siliconix personnel.

CONTENTS

Chapter 1

Introduction to FET Switches

1.1 INTRODUCTION

One of the most common control elements in electrical circuitry is the simple ON-OFF switch. This has evolved over the years from the manually operated circuit breaker of the early experimenters to the multiswitch integrated circuit of today. In every application, the function of the switch remains the same, viz. to isolate or connect two sections of an electrical circuit.

Until the advent of the thermionic valve, switching action was effected almost exclusively by the manual or electromechanical opening and closing of metal contacts. The operation of mechanical switches is easily understood and they require a very simple form of maintenance. However, with today's increasing demands of modern circuits, it has become evident that electromechanical switches alone cannot meet all requirements and that there are applications in which only electronic types are viable. By far the most popular of these is the semiconductor switch.

In recent years, semiconductor switches have made inroads into application areas that hitherto have been exclusively the domain of electromechanical devices. Solid-state switches are now used in sample-and-hold circuits; multiplexers; high power switching; chopper circuits etc., whereas in the past some form of electromechanical switch would have been used.

1.2 COMPARISON OF ELECTROMECHANICAL AND SEMICONDUCTOR SWITCHES

1.2.1 General

The types of electromechanical and semiconductor switches available are many and varied, each having some advantages and some disadvantages. The choice between a mechanical and semiconductor switch usually depends upon the application. The performance and major switching parameters of both types are compared in the following sections.

1.2.2 ON Resistance

Most electromechanical switches initially have very low ON-resistance, typically tens of milliohms. During their lifetime, however, wear at the switch contact surfaces can increase this resistance value by a factor of a hundred or more. Semiconductor switches have higher ON resistance but their resistance is constant over the switch lifetime. Field effect transistors are available with ON resistances of less than 2 ohms and some high power bipolar transistors can have collector-emitter saturation resistances of less than 100 milliohms. If the application required a switch with near zero ON resistance, the main contender would then be the electromechanical type, but if a constant ON resistance over the switch lifetime is of prime importance, then the semiconductor switch is far more preferable.

1.2.3 OFF Isolation

The maximum OFF resistance of electromechanical switches is limited by surface conduction along the package. This resistance is reduced considerably in moist environments or through careless handling. Nevertheless, extremely high OFF resistance is possible, and with specially treated reed switches this can be as high as 10^{12} ohms. The OFF resistance of semiconductor switches can have the same order of magnitude. The value of the semiconductor switch leakage current is roughly proportional to the square root of the voltage across the junction, and it increases with increasing temperature. Values of junction leakages can be less than one picoamp at 25°C for low power field effect transistor switches.

1.2.4 Switching Speed

Semiconductor switches comprise no moving parts, hence their switching speed is not limited by contact inertia. Consequently, switching times of nano-seconds are easily attainable and maximum switching rates are often in excess of 10^6 operations per second. By comparison electromechanical switches are slow indeed. Even the fastest of reed switches have turn-on/turn-off times measured in milliseconds, and maximum switching rates rarely exceed a few hundred operations per second.

1.2.5 Maximum ON Current

Power dissipation ratings limit the maximum currents that semiconductor devices are able to switch: collector currents of up to 100 amperes are possible with bipolars, while the largest field effect transistors at present have maximum drain currents in the region of 10 amperes. High power switches, with forced cooling, can conduct currents of up to 1000 amperes. Some electromechanical switches are capable of conducting currents of many thousands of amperes, but switching such high currents with these devices causes severe arcing and burning of contact faces. Electromechanical switches capable of conducting thousands of amperes are therefore normally switched when the load current is zero.

1.2.6 Maximum OFF Voltage

For electromechanical switches the maximum OFF voltage is limited by the voltage breakdown of the insulating dielectric. For large switches, with wide contact spacing, the maximum OFF voltage can be many hundreds of thousands of volts. The smaller electromechanical devices, reed switches, miniature relays etc. are capable of switching several hundreds of volts.

Operation of semiconductor switches relies on p-n junction action. Consequently the reverse biased breakdown voltage of the junction sets a limit to the maximum voltage that can be switched. Some thyristor devices have breakdown voltages as high as 1000 volts, while bipolar and field effect transistors can have maximum switching voltages in the region of 200 volts. It must be stressed that this is more than adequate to meet the needs of most semiconductor systems which normally run off supplies of less than 50 volts.

1.2.7 Minimum Analogue Voltage

The minimum analogue voltage switchable is determined by the total error signal contributed by the switch. One source of error in electromechanical devices is the

thermal EMF generated across the moving contacts. This can be tens of microvolts. A much larger error, prevalent in dry reed relays, results from the dynamic noise generated by contact bounce. This can be as high as 500 microvolts peak-to-peak initially, decaying to tens of microvolts after a few milliseconds.

Bipolar semiconductor switches require a finite collector-emitter voltage to maintain conduction. This voltage which is seldom less than a few millivolts, appears as an offset and severely limits the minimum value of analogue voltage that can be switched.

Field effect transistors have no such offset and are used extensively in low voltage switching applications. The thermal EMFs generated in field effect transistors are virtually zero, owing to their near symmetrical structure. Factors affecting the low level analogue switching voltage capability of FETS are switching transient breakthrough into the channel from the gate, and thermal noise due to the channel ON resistance. Both these topics are considered in detail in Chapters 2 and 3.

1.2.8 Drive Signals

Compatibility with existing circuits is an important consideration when deciding on a switch type. If, as is frequently the case, there is some degree of involvement with computers or other electronic systems which require standard logic control signals, then switching systems which respond to the same type of logic signals are desirable. The voltage levels required to operate electromechanical switches normally vary between 1 and 250 volts and most require a driving power greater than 50mW. Since logic driving circuits are limited in their power handling capability, this necessarily means that electromechanical switches usually require some form of interfacing with their logic control elements. Most semiconductor switches, owing to their lower drive power requirements, are directly compatible with transistor logic systems.

1.2.9 Switching Life

Since electromechanical switches comprise some moving parts, their operating life is affected by mechanical wear; in particular, wear at the contact surfaces. This can lead to an increase in ON resistance and the eventual welding together of the contacts. Figures for operating life times or switching cycles are difficult to assess since they depend on operating conditions. A dry reed relay switching at the rate of 100Hz would perform 10^8 switching operations in only 300 hours which is approximately the minimum expected lifetime of the relay.

This figure would be greatly reduced if the relay were switching into an inductive or capacitive load. Inductive loads produce arcing at the switch contacts because of the back EMF induced when the switch is opened. Capacitive loads accelerate contact wear due to current surges when the switch turns on. The switching life of a semiconductor device is not limited by mechanical wear and provided it is operated within its maximum specified ratings it can continue to switch almost indefinitely. For example, the mean time before failure (MTBF) of semiconductor devices is usually well in excess of 100,000 hours. Consequently, a semiconductor switch operating at 10^6 Hz could perform in excess of 3.6×10^{14} cycles during its operating life.

1.2.10 Reliability

In many applications the ability of a device to survive in adverse environments is most important. Military and space equipments need to withstand extremes of temperature, pressure, mechanical shock etc. without impairing operation. In general, semiconductor devices exhibit greater resistance to adverse environments than electromechanical types. Semiconductors are less susceptible to damage or change of state through shock, vibrations or high accelerations and do not suffer from sticking contacts due to freezing at very low temperatures. Their electrical characteristics are dependent on temperature and are somewhat prone to change when subjected to high energy radiation. However, this does not prevent their use in military equipment requiring an operating temperature range of -55°C to 125°C, or in satellite applications with the attendant high radiation environment.

1.2.11 System Size

Size, power consumption and weight of components become increasingly important as systems grow more complex. In this respect, the semiconductor switch has distinct advantages over its electromechanical counter part. The use of integrated circuits and modern fabrication techniques enable multiple switches to be contained in a single robust package. The Siliconix DG506, for example, has 16 switches with their binary decode circuitry in a 28 pin package measuring only 1.4 inches x 0.6 inches. An equivalent system using relays would be considerably more bulky.

1.2.12 System Costs

Total system costs should take into account not only the initial capital outlay but also factors such as maintenance costs, personnel training and the secondary costs resulting from system failures.

Switch for switch, the costs for electromechanical and semiconductor types are comparable, but as circuit complexity increases the cost per switch for semiconductor systems using integrated circuits falls, giving them a considerable price advantage over electromechanical types. Costly equipment down-time is also greatly reduced with semiconductor systems due to their higher reliability and longer lifetimes.

1.3 ELEMENTARY SEMICONDUCTOR THEORY

It is relevant at this stage to present a brief description of semiconductors and their application as switches.

Quantum mechanics shows that electrons in a solid can be represented as occupying discrete energy bands which are separated from each other by forbidden energy gaps.

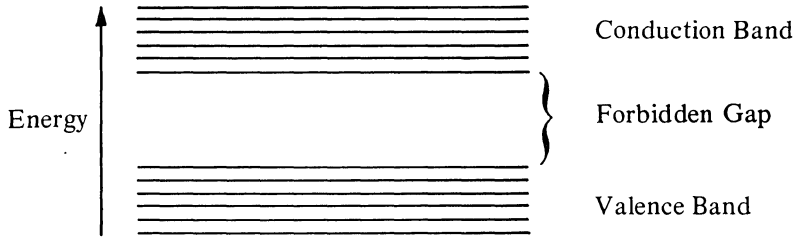


Fig. 1.1 **Comparative energy levels**

Fig. 1.1 represents the two outermost bands of any atom, the valence band and the conduction band, separated by a forbidden energy gap. It is the availability of electrons in the conduction band which determines the conductivity of a solid. Conduction can only occur if electrons arrive in the conduction band from the valence band. For this to happen, the electrons must receive sufficient energy to enable them to 'jump' the forbidden energy gap between the two bands.

If the forbidden energy band is wide, and prevents electrons appearing in the conduction band, the material is an insulator. Electrons will move from the valence to conduction band if sufficient energy is imparted to them. The application of a high electric field will do this. Thus, for all insulators, there is a specific voltage at which their insulating properties break down. In metals, the valence and conduction bands overlap with the result that electrons are freely available in the conduction band and can be persuaded to move between atoms when only a small voltage is applied. Thus, metals are good conductors of electricity.

In certain materials, the thermal energy imparted to some electrons at ambient temperatures is sufficient to enable them to cross the forbidden energy gap. For these materials there is a finite probability of electrons appearing in the conduction band. Therefore these materials will exhibit slight electrical conductivity which increases with increasing temperature. Such materials are referred to as semiconductors. Although many semiconducting materials exist, the two most widely used are silicon and germanium, with silicon being the more common of the two at present.

The width of the forbidden energy gap in pure silicon is of the order of 1.1 electron-volts at room temperature; the average thermal energy of the valence electrons is 0.025 electron-volts; thus, the probability of electrons appearing in the conduction band is small and the conductivity is very low. Conductivity can be increased if certain impurities are added to the semiconductor.

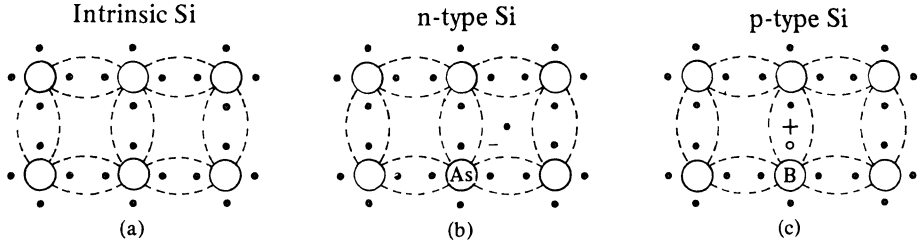


Fig. 1.2 **Schematic crystal structure of intrinsic and doped silicon.**

Both silicon and germanium have a valency of 4. This means that a pure or intrinsic semiconductor will have a crystal structure as in Fig. 1.2a. Each silicon atom binds with its neighbouring atom to produce a stable configuration of eight valence electrons associated with each nucleus. If an impurity atom, such as arsenic with a valency of 5 is introduced into the crystal structure (Fig. 1.2b), then a free electron results from the binding of the valence electrons. This electron can be easily elevated to the conduction band and, therefore, contribute to electrical conduction. The arsenic atom can be said to have donated a free electron to the semiconductor and for this reason the impurity atom is known as a donor atom. Obviously the greater the concentration of donor atoms, the greater will be the number of free electrons and the greater the conductivity. Semiconductors treated with donor impurities are known as **n** type. The existence of the free electrons does not constitute a net negative charge in the structure as associated with it is a localised positive charge on the arsenic atom. This positive charge also contributes to electric current but to a lesser extent. To distinguish between the two types of charge carriers in **n** type semiconductors, the free electrons are known as majority carriers and the positive charges as minority carriers.

If a trivalent impurity, such as boron or indium is introduced, the binding of the valence electrons results in a **space** or **hole** in the valence band (Fig. 1.2c). An electron from a neighbouring atom will move to fill the hole thereby causing a hole to appear in its place. The result is that a hole behaves similarly to a free electron but with a positive charge. It will contribute to electric current since a movement of holes in one direction is effectively the same as a movement of electrons in the opposite direction. Impurity atoms of this type are known as acceptor atoms and a semiconductor so treated is called **p** type. In a **p** type semiconductor, the **holes** are the majority carriers and the electrons are the minority carriers.

The process of adding impurities to semiconductors is known as doping. Impurity atoms may be either diffused into the pure semiconductor at high temperature or injected into the crystal structure using Ion Implantation techniques.

1.4 P-N JUNCTION

If **n** and **p** type semiconductors are joined, then at the junction the free electrons of the **n** type and the holes of the **p** type will be mutually attracted and will drift towards each other (Fig. 1.3b). Some will cross the junction producing a potential drop which tends to prevent any further flow of charge carriers across

the junction. This results in regions deficient in majority charge carriers on both sides of the junction. These regions act as insulating regions and are known as depletion layers (Fig. 1.3c).

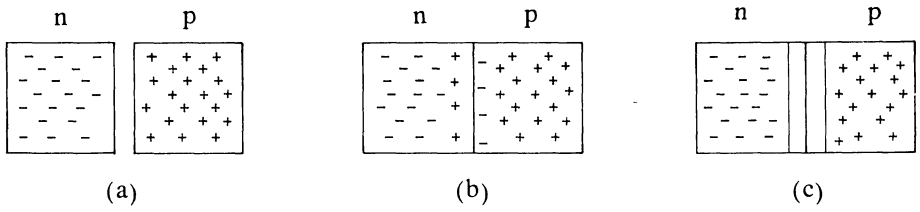


Fig. 1.3 **Showing formation of a depletion layer at a p-n junction.**

If a voltage supply is now applied to the junction with the negative terminal to the **n** type and the positive to the **p** type, it will oppose the inherent potential barrier already existing at the junction. If the applied voltage is greater than the potential barrier, it will cause more carriers to cross the junction and an electric current results. In this arrangement, the junction is said to be forward biased. If the voltage is applied with opposite polarity, then effectively the charge carriers in the **n** and **p** regions will be attracted away from the junction, resulting in an increase in the width of the depletion layer with an increase in potential drop across the junction which exactly opposes the applied voltage. Thus, very little current can flow and the junction is said to be reverse biased.

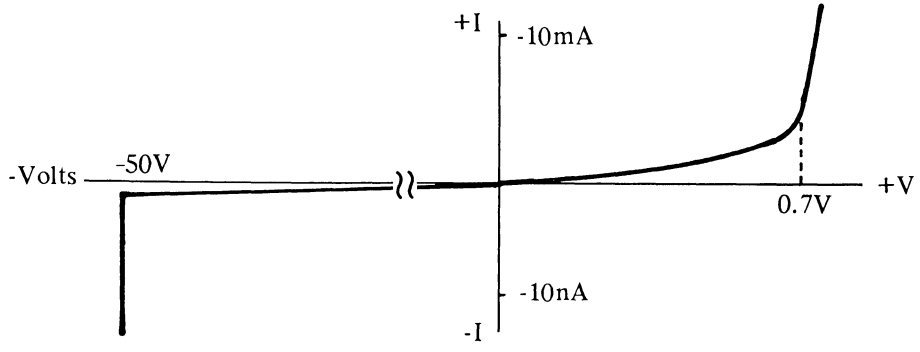


Fig. 1.4 **V/I characteristic for silicon p-n junction.**

A junction of **n** and **p** type semiconductors performs the function of a rectifying diode as shown by the voltage/current characteristic of Fig. 1.4. This reverse bias current is temperature dependent; its value for silicon approximately doubles for every 10°C increase in temperature. Other factors affecting the reverse current are dopant concentrations and junction area. The value is typically of the order of 1 nanoamp at 10 volts, but can be less than 1 picoamp. The reverse current increases sharply when the reverse voltage becomes sufficiently high. This is due to avalanche breakdown across the junction and to a large extent is dependent upon dopant concentration. A decrease in dopant concentration will result in an increased breakdown voltage. Breakdown voltages can be in excess of 1000V.

For a junction that consists of **n** and **p** conducting regions separated by an insulating depletion layer, there is associated with it a particular value of capacitance. This capacitance normally degrades the performance of semiconductor devices and efforts are usually directed at keeping the capacitance to a minimum. Factors affecting the value of junction capacitance are applied voltage, junction area, and impurity concentration. As the reverse bias voltage increases, so the width of the depletion layer increases thus reducing the capacitance.

A reduction in impurity concentration produces an increase in the depletion layer width for a given reverse bias voltage, and consequently a reduction in capacitance. Minimum junction capacitance is aimed for in most products, but varactor diodes make use of this voltage dependent characteristic and are designed for specific capacitance/voltage sensitivities. Values of junction capacitances can vary from less than 1 pico farad to greater than 10 nano Farads.

1.5 THE BIPOLAR TRANSISTOR

If a second p-n junction is added in close proximity to the first, a three terminal n-p-n or p-n-p device is produced. Such a device is the basis of a bipolar transistor. An n-p-n type bipolar schematic structure is shown in Fig. 1.5.

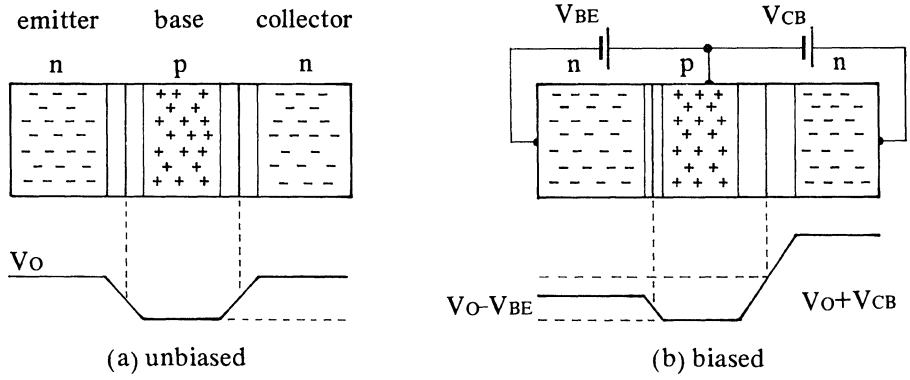


Fig. 1.5 **Bipolar schematic structure**

Fig. 1.5a shows the structure and potential distribution when no external voltages are applied. Under this condition the potential steps on each side of the centre or base region are equal and there is no net charge transfer across the junctions.

If external voltages are applied as in Fig. 1.5b, the base-emitter junction will be forward biased and the base-collector junction reverse biased. There will be a reduction in the base-emitter potential barrier and electrons will be injected into the base region from the emitter. These would normally recombine with holes in the base region, but if the width of the depletion layer of the reverse biased collector-base junction extends sufficiently into the base region, most of the electrons will be swept across to the collector where they recombine with holes to form collector current.

For a basic understanding of how the device operates, consider positive or negative charges (positive for a p-type emitter, negative for an n-type) flowing

from the emitter into the base region. A fraction x (say) of these recombine with charges of opposite polarity in the base region and so gives rise to base current. The remaining $(1-x)$ fraction of charges reaches the collector-base depletion region across which they are accelerated into the collector. The algebraic sum of collector and base currents is equal to the emitter current γI_E). The ratio of collector to base currents is $(1-x)I_E$: xI_E; that is, $(1-x)$: x. For a given bipolar transistor, x is practically constant at constant temperature, and for normal bipolar action is «1. Current amplification can therefore be effected: a small increase in base current results in a much larger increase in collector current.

For high current gain performance, the number of electrons arriving at the collector from the emitter must be maximised. Therefore, the collector-base depletion layer must be made wider by lightly doping the base, and the base thickness made as small as possible. The number of electrons emitted is maximised by heavily doping the emitter with respect to the base, which inherently results in a low base-emitter breakdown voltage. The collector is lightly doped near the junction but heavily doped at the point where metal contact is made to it, and sometimes in the regions away from the junction, to reduce saturation resistance. This gives the desired low contact resistance. It is implicit in the foregoing discussion that a bipolar will function with the collector and emitter interchanged. This is so, but only with a low inverse current gain and lower operating voltages.

1.6 THE FIELD EFFECT TRANSISTOR

Bipolar transistors are often termed minority carrier transistors by virtue of the minority carrier current through the base. However, the field effect transistor (FET) relies on majority carrier current for its operation. A FET consists essentially of an electrically conducting channel (either n- or p- type) whose conductivity may be controlled by applying a voltage to a controlling gate terminal. There are two distinct branches of the FET family—the JUNCTION FET and the INSULATED GATE FET, with further subdivisions as shown in Fig. 1.6. The two types will be reviewed in detail.

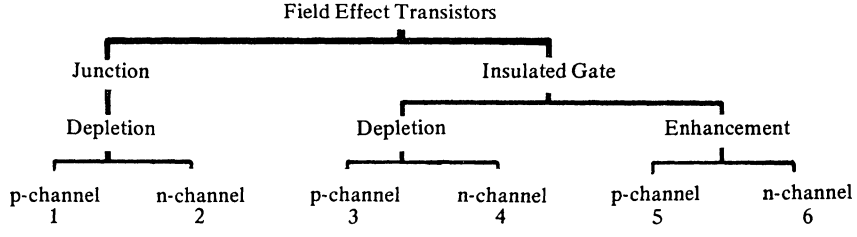


Fig. 1.6 **FET family tree**

1.7 JUNCTION FETS

1.7.1 General Layout and Characteristics

The JFET consists of a channel of n- or p- type semiconductor embedded in a semiconductor region of opposite polarity.

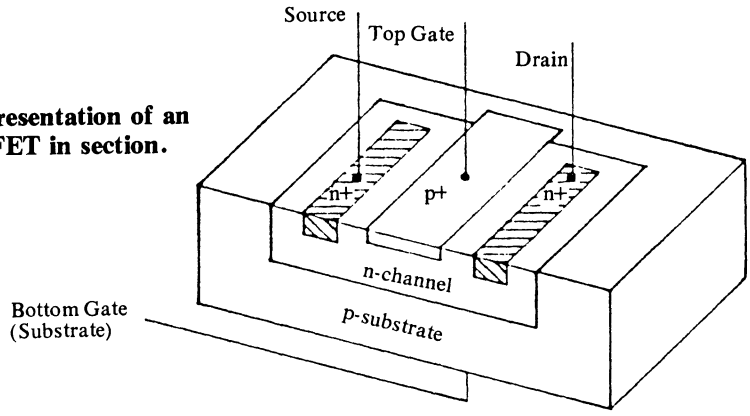


Fig. 1.7
Idealised representation of an n- channel JFET in section.

Fig. 1.7 shows an idealized n-channel JFET where the p-type region is the controlling gate and the n-type channel has electrical connections made at both ends (Source and Drain). Electrical connection to the gate is made at either the substrate or top gate contact. The controlling gate is isolated from the conducting channel by virtue of the reverse biased p-n junction. To understand how the JFET works, one must consider its operation under two distinct bias conditions.

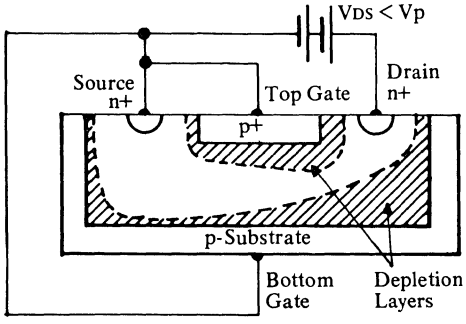
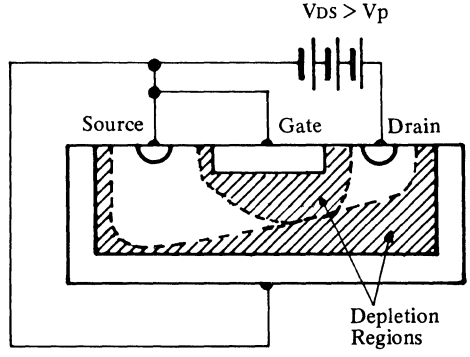


Fig. 1.8b
n-channel FET working in saturation region. n-channel is almost cut off between Drain and Source. (Only channel depletion regions are shown).

Fig. 1.8a **n-channel JFET working below saturation.** n-type conducting channel existing between Source and Drain. (Only channel depletion regions are shown).



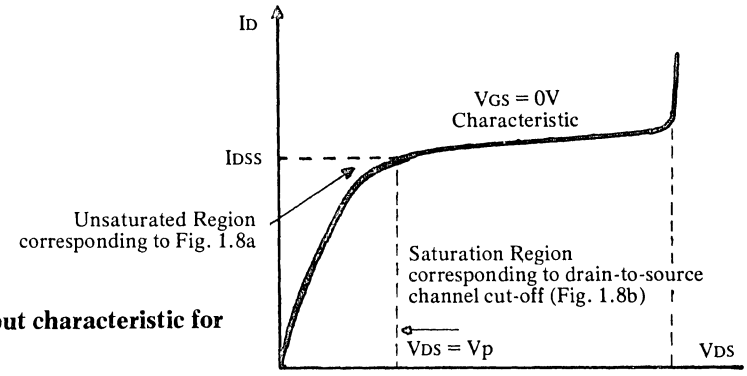


Fig. 1.8c **Output characteristic for $V_{GS} = 0V$.**

Fig. 1.8a illustrates the idealized cross sectional diagram of an n-channel JFET with a positive voltage V_{DS} applied between drain and source, and with the gate shorted to the source. Since the drain is positive with respect to source and gate, the drain-gate junction will always be reverse biased and practically no gate current will flow. A depletion region will form over the whole p-n junction area and this will be physically greatest at the high field regions between the drain and gate. The existence of the depletion region reduces the effective channel width and thereby increases the channel resistance. An increase in the value of V_{DS} increases the width of the depletion region. This results in a reduction of the channel cross-section and an increase in channel resistance. Above a certain V_{DS} value, the channel will no longer exhibit a resistive characteristic but reaches a state of saturation Fig. 1.8b where the channel current changes very little for a large change in V_{DS}. The JFET is then said to be saturated. This saturation current is given the symbol I_{DSS} which is an abbreviation for the drain to source current with the gate short-circuited. The I_D/V_{DS} characteristic at $V_{GS} = 0V$ is shown in Fig. 1.8c. Initially I_D increases almost linearly with V_{DS} until the depletion region begins to 'pinch-off' the channel, and the curve flattens out at the I_{DSS} value. The value of V_{DS} at which this takes place is termed the 'pinch-off' voltage and is given the symbol Vp.

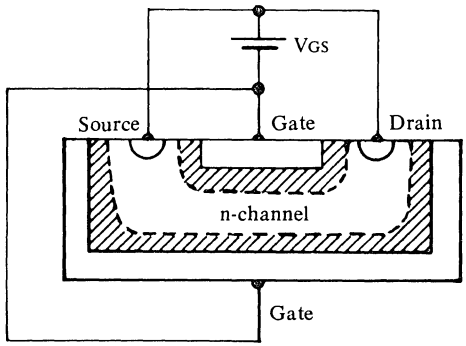


Fig. 1.9
n-channel JFET showing channel depletion layer when drain-source voltage V_{DS}=0V and V_{GS}=negative voltage.

Consider the case of Fig. 1.9 where $V_{DS} = 0V$ and a negative gate-source voltage (—V_{GS}) is applied. The depletion region is controlled mainly by the gate-source voltage V_{GS}: the depletion region widens as V_{GS} becomes more negative and

consequently the channel resistance increases. Therefore, for values of V_{DS} at or near to zero volts, the drain-source resistance is controlled by V_{GS}. As V_{GS} increases, the channel resistance increases until a voltage $V_{GS(off)}$ is reached, at which level the channel is completely 'pinched-off' and no drain current allowed to flow. This value of $V_{GS(off)}$ is equal in magnitude but opposite in polarity to Vp, and is usually referred to as the 'Gate Pinch-off' Voltage'. It also is given the symbol Vp.

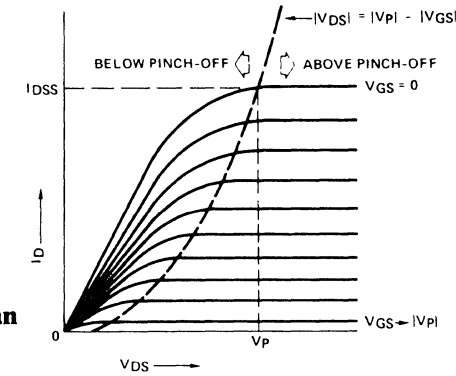


Fig. 1.10
Family of output characteristics for an n-channel JFET.

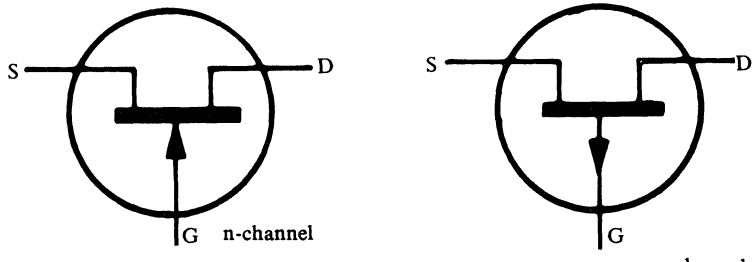
A combination of V_{DS} and V_{GS} bias conditions results in a family of characteristics (Fig. 1.10). From this it is seen that there are two important modes of operation for a JFET, namely:

1) Operation to the left of the pinch-off voltage locus. This is known as the unsaturated or triode region where I_D is governed by both V_{DS} and V_{GS}. As will be seen later, the triode region is most important when the JFET is used as an analogue switch.

2) Operating to the right of the pinch-off voltage locus. Here the JFET is in the saturated or pentode region and I_D is controlled almost entirely by V_{GS}. In this region, the JFET is most useful as a voltage amplifier.

The operation of a p-channel JFET is similar to the n-type except that voltage polarities and current directions are reversed. The symbols for both n and p channels are shown in Fig. 1.11. The arrows on the gate show the polarity of the gate-channel junction.

Fig. 1.11 **Symbols for Junction FETs**



The application of a negative voltage to the gate of an n-channel JFET increases the depth to which the depletion layer extends into the channel, and so reduces the conductivity of the channel. A small positive voltage on the gate has the

opposite effect. If the gate-to-channel voltage were sufficient to forward bias the p-n junction (approximately 0.6 volts) a significant current would flow from the gate (p-region) into the channel (n-region). For this reason, the n-channel JFET is normally operated with the gate at a negative voltage with respect to the channel. The JFET is therefore considered to be a DEPLETION mode device.

The foregoing applies equally to the p-channel JFET except that the voltage polarities are reversed.

1.7.2 JFET Fabrication

Junction FETs are usually manufactured using silicon planar technology. Figs. 1.12a—f illustrate the processing steps for fabricating an idealized n-channel JFET.

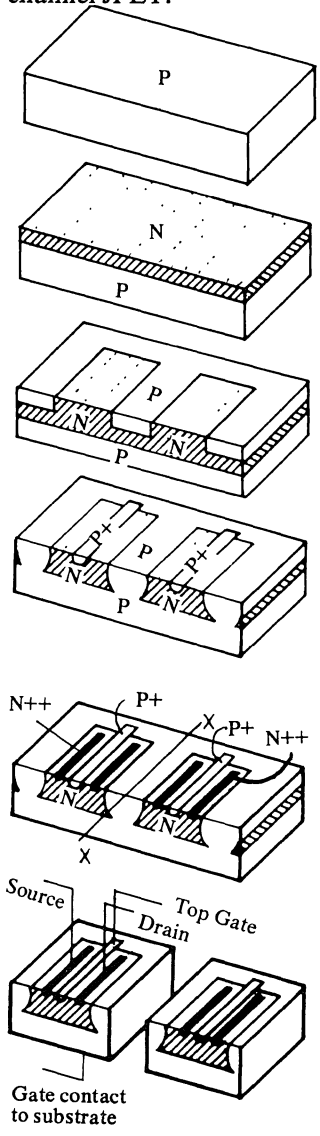


Fig. 1.12

a) **p**-type silicon wafer (substrate)

b) **n**-type silicon epitaxial layer grown on to **p**-substrate.

c) **p**-type acceptor impurity diffused in, to start isolation region.

d) **p+** impurity diffused in, to form top gate. Simultaneously, p region diffuses to complete isolation between the n islands.

e) **n++** type impurity diffused into **n**-type channel to form Drain and Source contacts. Physical isolation of each FET is achieved by scribing and breaking wafer along x-x axis

f) Formation of discrete **n**-channel FETS after 'scribing and breaking' procedure. Since the edges of the p+ regions of the top gate are diffused into the **p**-substrate, electrical contact is made to the top gate, via the p-substrate.

The process begins with a mono-crystalline substrate of p-type silicon in the form of a circular wafer $1^1/_2$ inches to 3 inches in diameter and approximately 0.010 inches thick. A thin layer of n-type silicon is then grown epitaxially on top of the substrate (Fig. 1.12b). The epitaxial process used to form the drain-source channel allows a fine control on dopant concentration and film thickness, important factors if consistent device performance is to be achieved.

A film of silicon dioxide is grown on the surface of the epitaxial layer. A photo-resistive material is applied to the oxide and the wafer is subsequently exposed to ultra violet light through a mask. Chemical solutions are then used to etch away the unexposed photo-resist and then the silicon dioxide. The photoresist that remains is then removed. An acceptor type impurity is diffused through the pattern in the oxide mask (Fig. 1.12c) to begin the formation of the isolation regions. Further oxide films are grown and subsequently selectively etched; another acceptor type diffusion is performed to produce the top p-type gate, and simultaneously complete the isolation of each n-type island on the substrate (Fig. 1.12d). By a similar process, a donor impurity is diffused into the n type islands to form the n++ Drains and Sources. Aluminium is then deposited on to the n++ diffusion regions to form the drain and source contacts. In most cases, the gate contact could be made via the substrate (Fig. 1.12f). The majority of devices have drain and source symmetry that allows complete electrical interchangeability of these two terminals. Depending on the type of FET and wafer size, more than 15,000 FETS can be fabricated on one wafer.

1.7.3 Assembly and Test

The same general processing and assembly techniques are applicable to both junction and MOS FET devices. The wafers are inspected visually for any obvious defects such as mask misalignment, poor metallisation etc. and then 100% probe tested on major electrical parameters. Any reject FET dice on the wafer are automatically ink marked by the probe tester. The impurities diffused into the back of the wafer during fabrication are removed by back lapping which also reduces the wafer to a convenient thickness. The wafer is then scribed and broken into individual die (Fig. 1.12e). Next, the dice are subjected to a further visual inspection prior to assembly. A typical discrete FET package is illustrated in Fig. 1.13. Here a JFET die is shown mounted on to a metal header. The die is eutectically bonded on to the header which is in electrical contact with one of the three external leads. In this instance, the backgate on the FET is used to make contact with the gate lead. The other two leads are embedded in glass that insulates them from each other and the header body. Attached to these leads are aluminium or gold wires to make connections to the source and drain terminals of the die.

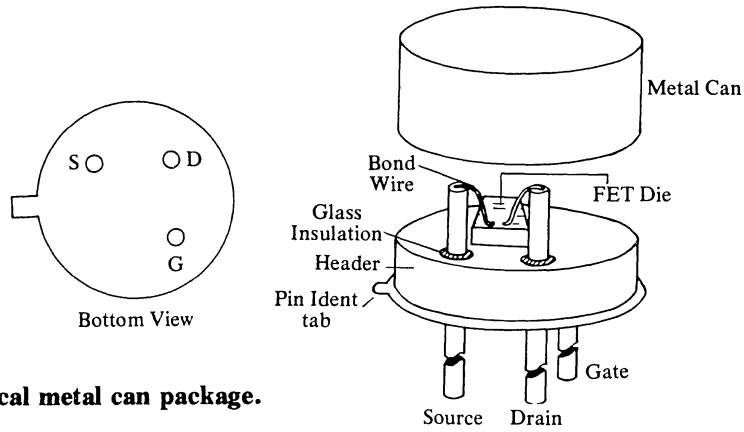


Fig. 1.13 **Typical metal can package.**

The header assembly is visually inspected and any defective devices rejected. Finally, the metal can is welded to the header in a dry nitrogen environment to form a hermetic seal. Other package options are available, including dual-in-line and flat pack types. Encapsulating materials most commonly used are metal-ceramic, plastic, or epoxy resin. Devices are available with a variety of process and screening options in accordance with military, industrial or consumer reliability specifications. Screening for high reliability devices usually includes a burn-in to eliminate infant mortality failures. Each device is tested on major electrical parameters. The good devices are then marked with the part number, manufacturer's symbol and the date of manufacture. Before leaving the plant each batch is sample tested to ensure conformance with specifications.

1.8 MOSFETS

The MOSFET or metal-oxide-semiconductor FET uses a film of high purity dielectric such as silicon dioxide or silicon nitride to insulate the gate from the channel. Due to the insulation properties of the MOS gate, both positive and negative gate voltages may be applied to unprotected MOSFETs (see Section 1.8.2). Four forms of MOSFET are possible:

a) n- Channel Depletion
b) p- Channel Depletion
c) n- Channel Enhancement
d) p- Channel Enhancement

1.8.1 Depletion MOSFETS

Fig. 1.14 shows the basic cross-section of an n-channel depletion mode MOSFET.

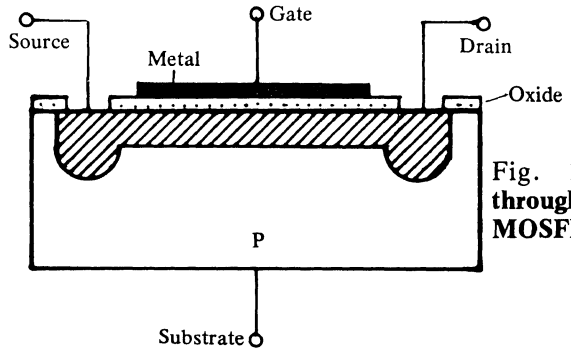


Fig. 1.14 **Idealized cross-section through an n-channel depletion mode MOSFET.**

In early MOSFETs, the formation of an n-channel relied upon the charge induced by the oxide impurities at the oxide-semiconductor interface. The repeatability, therefore, was not good. Present day MOSFETs are fabricated by much cleaner and repeatable processing. The introduction of an additional n-type region between n+ type source and drain forms the initial channel. This is enhanced or depleted according to the gate voltage applied.

In operation, a negative gate voltage must be applied to turn the channel off and in this sense the device behaves exactly as an n channel JFET. However, if a positive voltage is applied to the gate, additional negative charges will be attracted to the oxide/semiconductor interface thus increasing the channel conductivity. The device can therefore be operated in both depletion and enhancement mode. Fig. 1.15 shows the family of output characteristics for a typical n channel depletion MOSFET.

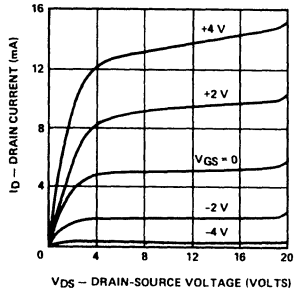
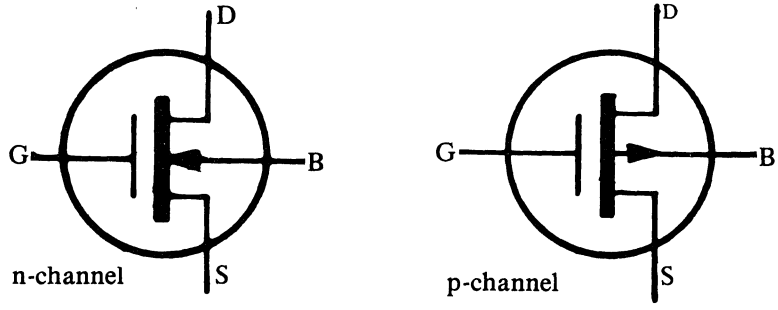


Fig. 1.15 **Family of output characteristics for the Siliconix 2N3631 n-channel depletion MOSFET.**

The manufacture of p-channel depletion types is possible if very clean processes are used but they are not available commercially in large quantities. The symbols for depletion MOSFETS are shown in Fig. 1.16.

Fig. 1.16 **Symbols for depletion MOSFETS**



1.8.2 Enhancement MOSFETS

Enhancement MOSFETS are normally OFF devices requiring the application of either a negative (for p-channel MOS) or positive (for n-channel) gate voltage before channel conduction is possible.

The operation of a p-channel enhancement MOSFET is illustrated in Figs. 1.17 to 1.19.

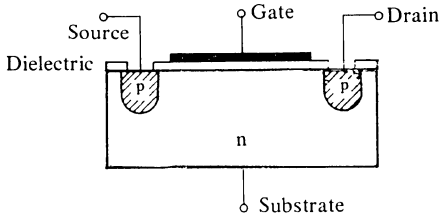


Fig. 1.17 **Idealised cross-section through a p-channel enhancement MOSFET** showing negative charge region existing at the oxide/semiconductor interface with no gate voltage applied.

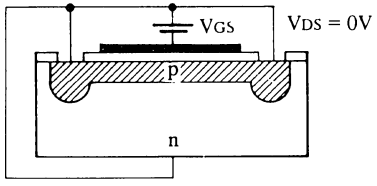


Fig. 1.18 showing induced p-channel when $V_{GS} \gg V_{GS(th)}$ ($V_{DS} = 0V$).

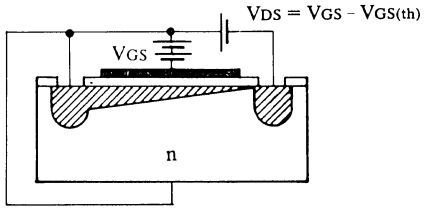


Fig. 1.19 showing the pinch-off of the p-channel as drain voltage increases negatively with respect to the substrate.

The device consists of an n-type substrate into which a p-type impurity is diffused to form separate sources and drains. The metal gate is insulated from the substrate by an oxide layer. As in the depletion MOSFET, free electrons are inherently attracted to the oxide/semiconductor interface to form an n-type layer, which has a higher concentration of negative charge carriers than the surrounding n-type substrate Fig. 1.17. When the gate-to-source voltage is zero, virtually no current can flow from source to drain or from drain to source as there is a reverse biased junction in each direction. Therefore, the device is normally OFF. If a negative gate-to-source voltage is applied, positive charges are attracted to the oxide/semiconductor interface where they recombine with free electrons. Increasing the gate voltage negatively causes more charge carriers to recombine until a voltage $V_{GS(th)}$ is reached, at which all the free electrons at the semiconductor/insulator surface have recombined. Any further increase in gate voltage produces a p-type layer beneath the gate thus forming a conducting channel between the source and drain (Fig. 1.18) whose conductivity increases with increasing V_{GS}. If a negative drain voltage is applied with respect to the source, the drain-gate differential voltage will now be reduced and consequently the channel narrows toward the drain. When V_{DS}-$V_{GS} = V_{GS(th)}$ the channel will be pinched off (Fig. 1.19) at the drain.

Any further increase in V_{DS} would have little effect on the value of channel unless V_{GS} were increased which would then require a greater V_{DS} for pinch-off current. Fig. 1.20 shows a family of output characteristics for a typical p-channel enhancement MOSFET.

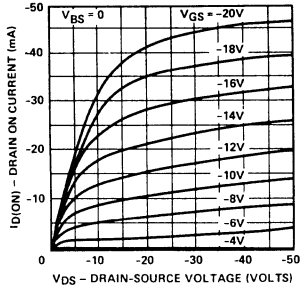
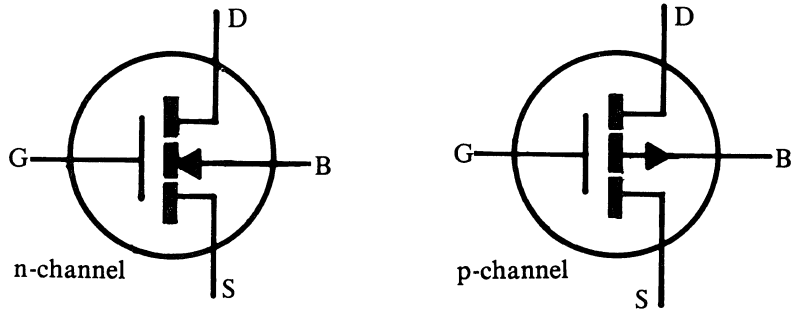


Fig. 1.20 **Family of output characteristics for the Siliconix 3N163 p-channel enhancement of MOSFET.**

The design and operation of an n-channel enhancement MOSFET is similar to the p-channel enhancement MOS but voltage polarities are reversed.

Fig. 1.21 **symbols for enhancement MOSFETs**



The extremely high gate-to-channel resistances in excess of 10^{15} ohms present a problem when handling MOSFETs. Electrostatic charge build-up at the gate can cause the gate-channel capacitance to charge up to voltages which can be in excess of the gate-to-channel dielectric breakdown. Permanent damage to the dielectric can therefore occur. To protect the gate dielectric, many MOSFETS are manufactured with an integrated zener clamp, which consists of a p-n junction, between the gate and substrate. The zener breakdown voltage is designed to be less than that of the gate dielectric but sufficiently high to prevent limitation of the operating voltage.

Since the zener diode is reverse biased during normal operation, the gate leakage current is almost completely determined by the diode leakage current. Dielectric leakage current is a minor factor in comparison. A protected MOSFET has inherently a much higher gate leakage current than an unprotected MOSFET.

1.9 THE FET AS A SWITCH

The high OFF-to-ON resistance ratio of field effect transistors makes them ideal components for use in switching applications. This section covers the major switching parameters of FETs and indicates the degree of performance achievable with commercially available devices.

1.9.1 ON Resistance

Switching applications usually require ON resistances to be as small as possible. The ON resistance of field effect transistors depends on the concentration and mobility of the charge carriers in the channel and the physical size of the conducting channel. n-channel devices have lower ON resistance than p-channel devices of similar channel dimensions because of the higher carrier mobility in n-type material.

Since the MOSFET has an extremely thin induced channel, it tends to have a higher ON resistance than a junction FET of similar size. Even so, the geometry of a conventional p-channel MOSFET can be tailored to give low ON resistance as in the case of the Siliconix 3N167 for which $r_{DS(ON)}$ is a maximum of 20 ohms. The DG515 integrated circuit contains a 6.25 ohm NMOS switch. The new MOSPOWER devices which utilise VMOS technology have resistances of less than 2 ohms.

1.9.1.1 Junction FET ON Resistance

For a junction FET operating in its saturation region, its output characteristic may be approximated by the quadratic function given in equation 1.1

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \qquad \text{eqn. 1.1}$$

In the saturation region, the value of I_D is essentially independent of V_{DS} and the device has a very high dynamic resistance $\frac{dV_{DS}}{dI_D}$

For the same FET operating in the non-saturated (triode) region, the output characteristic is given by equation 1.2

$$I_D = \frac{V_{DS}}{V_p} I_{DSS}\left[2\left(1 - \frac{V_{GS}}{V_p}\right) - \frac{V_{DS}}{V_p}\right] \qquad \text{eqn. 1.2}$$

From equation 1.2, the channel resistance r_{DS} in the triode region is found to be:

$$r_{DS} = \frac{V_{DS}}{I_D} = \frac{V_p^2}{2I_{DSS}\left(V_p - V_{GS} - \frac{V_{DS}}{2}\right)} \qquad \text{eqn 1.3}$$

In the triode region, a junction FET behaves as a resistor whose value is dependent upon V_{GS} and V_{DS}. Indeed for very low values of drain-to-source voltage, I_D is almost linear with V_{DS}, for a given V_{GS}. For this reason JFETs are widely used as voltage controlled resistors. Over a wider range of drain-to-source voltage, r_{DS} will also depend on V_{DS}; the I_D/V_{DS} relationship becomes non-linear as V_{DS} increases. This limits the useful range of V_{DS}. However, techniques exist which employ feedback between drain and gate to reduce the r_{DS} non-linearity and to extend the dynamic range of V_{DS}.

A junction FET operating under reverse biased gate-source conditions, exhibits minimum channel resistance r_{DS} when both V_{GS} and V_{DS} are zero. Under these conditions an n-channel FET with a Vp of 5V and an I_{DSS} of 100mA would, from equation 1.3, exhibit an $r_{DS(ON)}$ of 25 ohms. Such a FET would have an active area of about 0.15 square millimetres. To reduce ON resistance, one option is to increase the active area; for example, the Siliconix U290 n-channel JFET has an ON resistance of less than 2.5 ohms and has an active area of the order of 1 square millimetre.

The channel resistance of FETs is temperature dependent. This is due to two effects: a) charge carrier mobility reduces with increasing temperature and so tends to increase channel resistance, and b) the width of the gate-to-channel depletion region decreases with increasing temperature, tending to decrease the resistance. For low values of V_{GS}, the decrease in carrier mobility is the dominant factor and under these conditions junction FETs exhibit a positive temperature coefficient of resistance of about 0.7% per °C (Fig. 1.22).

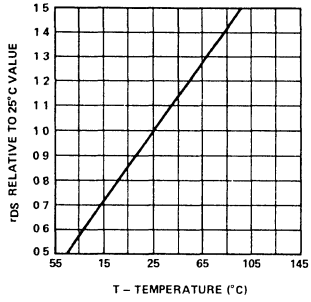


Fig. 1.22 **ON Resistance** vs. **Ambient Temperature for a typical n-channel JFET.**

As the gate-source voltage approaches the $V_{GS(off)}$ value, the percentage increase in channel resistance as the temperature increases is balanced by a decrease in resistance due to the decreasing width of the gate-to-channel depletion area. Thus, junction FETs can be biased to a point at which the resistance has a zero temperature coefficient, as illustrated for a p-channel JFET in Fig. 1.23.

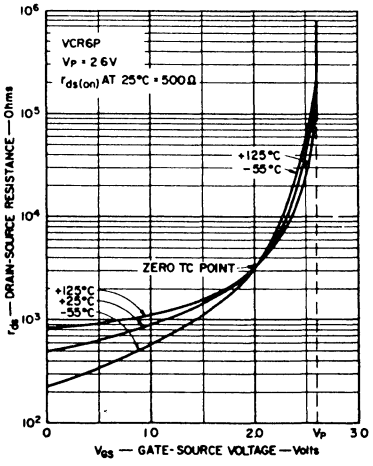


Fig. 1.23
r_{DS} vs. V_{GS} and Temperature for a p-channel JFET.

1.9.1.2. MOSFET ON-Resistance

Equation 1.4 is an approximation for the drain current flowing in a MOSFET when operated well into the saturation region. i.e. $|V_{DS}| > |V_{GS}| - |V_{GS(th)}|$

$$I_D = \frac{\beta}{2}(V_{GS} - V_{GS(th)})^2 \qquad \text{eqn. 1.4}$$

In this region, V_{DS} has little effect and I_D is almost entirely controlled by V_{GS}. The device constant β is a function of the geometry of the MOSFET and is given as

$$\beta = \mu \frac{e_o W}{To L} \qquad \text{eqn. 1.5}$$

where e_o = dielectric constant

μ = mobility of charge carriers

L = channel length from source to drain

W = channel width

To = thickness of gate dielectric.

In the unsaturated (triode) region, the drain current is approximated by Equation 1.6

$$I_D = \beta \left\{ V_{DS} \left[V_{GS} - V_{GS(th)} \right] - \frac{V_{DS}^2}{2} \right\} \qquad \text{eqn. 1.6}$$

Thus the ON resistance is given by:

$$r_{DS} = \frac{V_{DS}}{I_D} \approx \left\{ \beta \left(\left[V_{GS} - V_{GS(th)} \right] - \frac{|V_{DS}|}{2} \right) \right\}^{-1} \qquad \text{eqn. 1.7}$$

For n-channel and p-channel enhancement MOSFETS, $V_{GS(th)}$ is positive and negative respectively, whereas for depletion MOSFETS reverse polarities apply.

As with junction FETS, the r_{DS} of a MOSFET is dependent not only on V_{GS} but also upon V_{DS}, the minimum ON resistance occurring when $|V_{GS} - V_{DS}|$ is a maximum. Therefore, if MOS devices are used in switching circuits that have fixed gate voltages applied in the ON state, the channel resistance will be modulated by any variation in the analogue signal voltage. Fig. 1.24 illustrates how r_{DS} varies with analogue signal for a typical p-channel enhancement MOSFET.

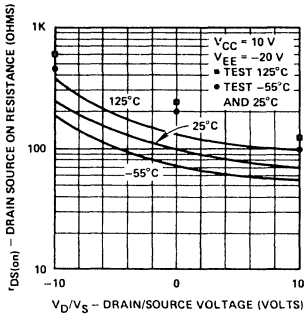


Fig. 1.24 r_{DS} vs. V_D **for a p-channel enhancement MOSFET.**

Clearly for p-channel devices, the minimum ON resistance is achieved when the analogue signal is at its most positive value, Fig. 1.24 shows that the resistance can vary by a factor of 3:1 over the analogue range —10V to +10V.

For those applications in which this variation in r_{DS} is unacceptably high, a junction FET having a constant ON resistance over the analogue range, would be more suitable. Alternatively, use could be made of n-channel and p-channel MOSFETs connected in parallel. A negative going analogue signal which causes an increase in the r_{DS} of the p-channel MOS, simultaneously causes a decrease in the r_{DS} of the n-channel MOS. Such complementary MOSFET arrangements are used extensively in integrated circuits.

The effects of temperature on channel resistance are similar in both MOS and junction FETs. An increase in temperature causes a reduction in the channel carrier mobility, and a reduction in the threshold voltage. The net effect is that MOSFET channel resistance exhibits a positive temperature coefficient of about 0.4% per °C for high values of V_{GS}. This coefficient falls with V_{GS} until a zero temperature coefficient point is reached (see Fig. 1.25).

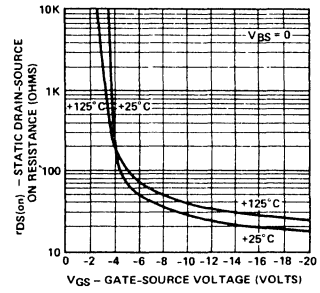


Fig. 1.25
$r_{DS(on)}$ vs. V_{GS} **and Temperature for Siliconix 3N167 p-channel enhancement MOSFET.**

1.9.2 Isolation

Both MOS and junction FETs exhibit extremely high OFF resistance. For most FETs this is greater than 10^{10} ohms and in some FETs can exceed 10^{13} ohms. In FET applications, the leakage currents $I_{S(OFF)}$ and $I_{D(OFF)}$ are a better measure of the OFF performance of a switch.

a) **Junction FET Leakage Currents**

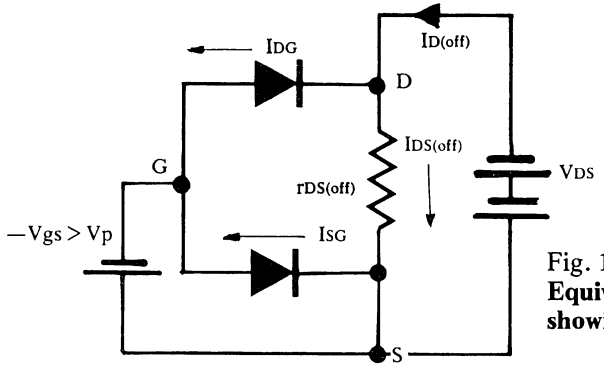


Fig. 1.26
Equivalent circuit of n-channel JFET showing OFF leakage paths.

Fig. 1.26 represents an n-channel JFET in the OFF state. The total drain current $I_{D(OFF)}$ is the sum of the drain-gate junction leakage I_{DG}, and the current $I_{DS(OFF)}$ flowing to the source through the high resistance of the OFF channel. The resistance comprises that of the depletion region, shunted by the package header resistance. Most metal-can headers have pin-to-pin resistances of greater than 3×10^{13} ohms and the FET depletion region resistance can be in excess of 10^{13} ohms. $I_{DS(OFF)}$ in most applications is therefore just a few picoamps. The leakage currents I_{DG} and I_{SG} will obey the p-n junction leakage relationship of equation 1.8.

$$I = Io\left[(\exp\left(\frac{Ve}{1kT}\right) - 1\right] \qquad \text{eqn. 1.8}$$

where V is the applied junction voltage, e is the electronic charge ($e = 1.602 \times 10^{-19}$C), T is absolute temperature, k is Boltzmann's constant ($k = 1.38 \times 10^{-23}$ j/^{0}K), and Io is the reverse saturation current. Thus for small applied junction voltages the leakage currents will increase exponentially with V, but for values of $V \gg \frac{kT}{e}$ the leakage tends towards the reverse saturation current Io; this then increases approximately as the square root of the applied voltage.

The temperature dependence of Io for silicon is given by the approximation Equation 1.9

$$Io = AT \exp\left(-\frac{1.12e}{2kT}\right) \qquad \text{eqn. 1.9}$$

where A is a constant.

Equation 1.9 indicates that Io doubles for approximately every 10°C rise in temperature. In practice, the leakage current increases at a slightly lower rate, as indicated by the graph of Fig. 1.27 which shows the gate-to-channel leakage currents I_{GSS} and $I_{D(OFF)}$ versus temperature for a typical n-channel JFET switch.

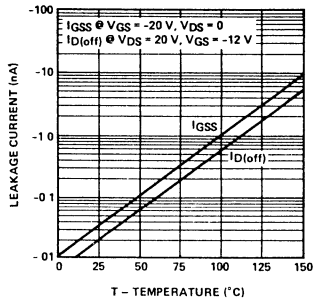


Fig. 1.27 **Leakage Current** vs. **Ambient Temperature for an n-channel JFET.**

Junction FETs are available with specified maximum OFF leakages ranging from nanoamps to less than one picoamp at 25°C. This wide range is due to the variation in the geometry and processing of different types. Low leakage FETS usually have the smallest geometry. For example, the Siliconix 2N4338 n-channel JFET has a maximum $I_{D(OFF)}$ of 50 picoamps at 25°C with V_{DG} = -20 volts and V_{GS} = -5 volts, and has an active area of about 0.02 square millimetres. The Siliconix U290 has a maximum $I_{D(OFF)}$ of 1nA at 25°C with V_{DS} = 5 volts, V_{GS} = -10 volts and an active area of about 1 square millimetre.

b) **MOSFET Leakage Currents**

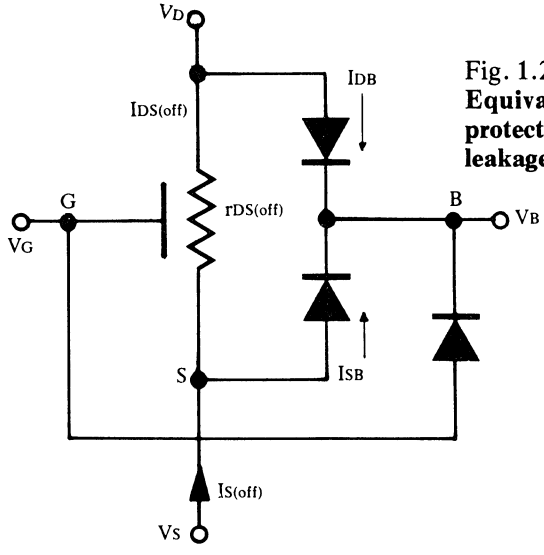


Fig. 1.28
Equivalent circuit of a p-channel protected MOSFET showing the OFF leakage paths.

The extremely high gate-to-channel resistance isolates any direct leakage paths from the channel into the gate. However, leakage paths exist from the source and drain (also from the gate in protected devices) into the substrate via the reverse biased junctions (Fig. 1.28). The leakage values are of the same order as those for junction FETs and have similar characteristics although the OFF leakages $I_{S(OFF)}$ and $I_{D(OFF)}$ show a greater dependence upon V_{DS}.

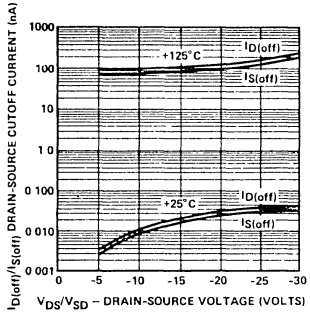


Fig. 1.29 **Variation of OFF leakages with applied voltage and temperature for the Siliconix 3N167 p-channel enhancement MOSFET.**

1.9.3 Offset Voltage

Unlike the bipolar transistor which exhibits a significant V_{CE} offset voltage, the V_{DS} offset for a FET in the ON state is usually negligible. All bipolar transistors have inherent potential barriers at the base-emitter base-collector junctions (Fig. 1.5) and these must be offset by a small V_{CE} voltage before conduction can occur. This offset voltage is rarely less than 10 millivolts making bipolar transistors unsuitable for switching applications involving low voltage analogue signals.

FET offset voltage results from thermoelectric EMFs generated between source and drain, also from the product of the gate leakage current and the ON resistance. In most applications, these are negligible.

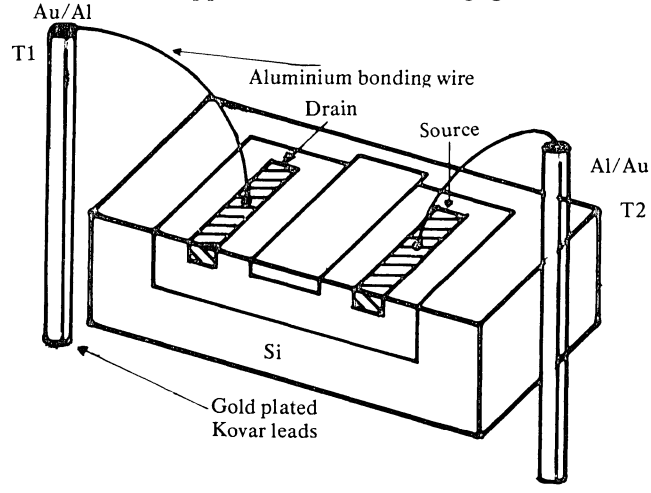


Fig. 1.30

The sources of thermoelectric EMFs for a FET are shown in Fig. 1.30. If, through localised heating on the chip, or through heat applied from external sources via the leads, a temperature gradient of T_1-T_2 is developed between drain and source, then the total thermal offset voltage will be:

$$\left[\underset{\textit{Gold/Aluminium}}{\text{Thermoelectric coefficient}} + \underset{\textit{Aluminium/Silicon}}{\text{Thermoelectric coefficient}}\right] \times (T_1 - T_2).$$

The thermoelectric coefficient for the aluminium-silicon junction is about 0.4 millivolts /°C, while for the gold-aluminium junction it is much less at 0.004

millivolts /°C. If it is assumed that the package leads are at constant temperature, any contribution from the gold—Kovar junction can be eliminated. Hence, the thermoelectric offset for FETs is about 0.4 mV/°C.
Usually for discrete FETS, due to the small size of the chip and symmetry in the drain-source layout, the T_1 and T_2 temperatures are nearly equal and the thermoelectric offset is very small—of the order of a few microvolts.
On a large integrated circuit some parts of the chip will dissipate more heat than others. It is therefore imperative when designing the layout to ensure that drain and source are both in areas which are subjected to the same amount of local heating. Thermoelectric EMFs also exist in bipolar transistors but these are negligible compared with the barrier offset. The offset voltage resulting from gate leakage current for an n-channel JFET is illustrated in Fig. 1.31.

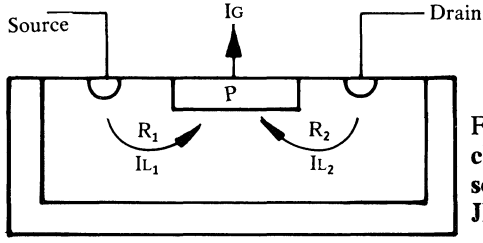


Fig. 1.31a **Gate leakage current x channel resistance adds to the drain source offset voltage for an n-channel JFET.**

The gate leakage I_G comprises leakage currents from the source and drain, I_{L_1} and I_{L_2} respectively. These leakage currents flow to the gate via sections of the channel with bulk resistances R_1 and R_2. Thus the offset due to gate leakage is $(R_1 \times I_{L_1}) - (R_2 \times I_{L_2})$. At room temperature, this voltage will be extremely small, of the order of 1 nano volt but since leakage currents increase with temperature, this offset voltage can be several microvolts at 150°C. A similar situation exists with MOSFETS, although the leakage is now from the source and drain to the substrate.

1.9.4 FET Capacitances

As mentioned in Section 1.4 all p-n junctions exhibit a value of capacitance which is dependent upon the area and depth of the depletion region. For field effect transistors there is a distributed capacitance between the gate and the channel whose value is determined by the FET geometry, the dopant levels, and the applied voltages. The gate-to-channel capacitance can be considered as two lumped capacitors, the gate-to-source capacitance (Cgs) and the gate-to-drain capacitance (Cgd). There is also a drain-to-source capacitance (Cds) which is largely the header capacitance but this is small (« 1.0 pico Farads) compared with the others and can usually be neglected.

An equivalent circuit of a junction FET is shown in Fig. 1.31b.

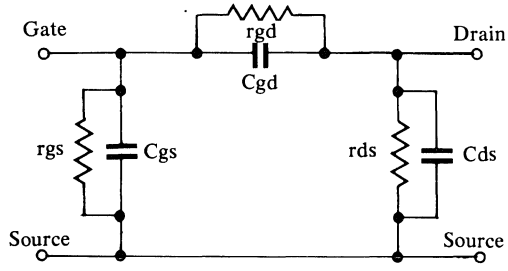


Fig. 1.31b
JFET a.c. equivalent circuit.

The junction capacitances are shown shunted by reverse biased junction resistances, rgs and rgd. These resistances are of such high values that for most purposes they may be ignored and the gate impedance considered as purely capacitive.

Most FET data sheets quote junction capacitances with relation to input and output, that is, C_{iss} and C_{rss}. The input capacitance C_{iss} is defined as the capacitance between gate and source when the drain is a.c. short circuited to the source. Analysis of Fig. 1.31 shows that C_{iss} is defined by equation 1.10.

$$C_{iss} = C_{gs} + C_{gd} \qquad \text{eqn. 1.10}$$

The output capacitance C_{oss} is the capacitance measured between drain and source with the gate shorted to the source. Thus C_{oss} is given by equation 1.11.

$$C_{oss} = C_{ds} + C_{gd} \qquad \text{eqn. 1.11}$$

Since C_{ds} is « C_{gd}, then $C_{oss} \cong C_{gd} \cong C_{rss}$. An alternative symbol for C_{gd} is C_{rss} which refers to the 'reverse' capacitance and is usually quoted in data sheets in preference to C_{gd} or C_{oss}.

For a p-n step junction, the capacitance is inversely proportional to the square root of the applied voltage and the variations of C_{iss} and C_{rss} for a typical n-channel JFET are given in Fig. 1.32.

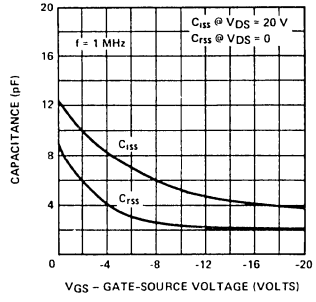


Fig. 1.32 **Common Source Capacitances** vs. **Gate-Source Voltage.**

Junction capacitance varies only slightly with temperature, there being a slight increase with increasing temperature due to a decrease in the junction barrier potential. The barrier potential varies by about —2.2 millivolts per °C. Thus, as V_{GS} increases, the temperature dependence becomes less pronounced. The physical size of the FET is a major factor in determining the value of its junction capacitances. The typical curves given in Fig. 1.32 relate to the Siliconix 2N4391 JFET which has an active area of about 0.15 square millimitres. The curves indicate a maximum C_{iss} of 12 pico Farads. For the Siliconix U290 n-channel JFET which has an active area of about 1 square millimetre, the typical maximum value of C_{iss} is 160 pico Farads.

In the case of MOSFETS, channel-to-body junction capacitance must also be considered. This can be treated in a similar manner to the gate capacitance of a JFET. For simplicity, this is considered as two lumped capacitances C_{db} and C_{sb}. Fig. 1.33 shows the variation of C_{db} and C_{sb} for a typical p-channel enhancement MOSFET.

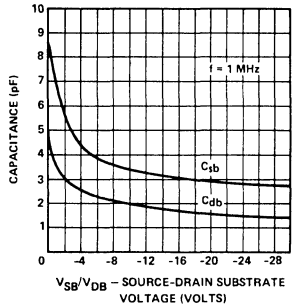


Fig. 1.33
Typical Substrate Capacitance vs. **Voltage for the Siliconix M103 p-channel enhancement MOSFET.**

MOS gate capacitance is a minimum when the device is OFF. When the device turns ON, the carrier concentration in the channel increases with a subsequent increase in gate-channel capacitance. Fig. 1.34 illustrates the sharp increase in Cgs and Cgd that occur when the gate-source voltage is close to $V_{GS(th)}$ for an enhancement MOSFET

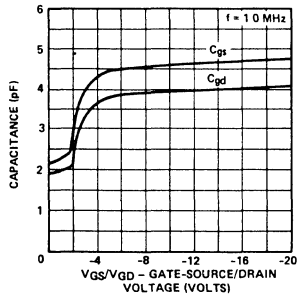


Fig. 1.34
Typical Gate Capacitance vs. **Voltage for the Siliconix M113 p-channel enhancement MOSFET.**

In switching applications the interelectrode capacitances should be kept as small as possible to minimise charge feed through of the gate signal into the channel. Since the channel turn-on switching time is largely determined by the gate capacitance, a low value of interelectrode capacitance is therefore required for fast switching times. Low capacitance is generally achieved by using smaller geometry FETs. This usually implies that the value of ON resistance is likely to increase. The following table of Siliconix n-channel JFETs illustrates the compromise which must be made between capacitance and r_{DS}.

Device	$r_{DS(ON)}$ max.	C_{iss} max.	C_{rss} max.
2N5432	5 ohms	30pF	15pF
2N4391	30 ohms	14pF	3.5pF
2N3966	220 ohms	6pF	1.5pF

Direct comparisons of the respective switching speeds are difficult to make because they are defined for specific circuit configurations and for specific values of load resistance values. However, as an indication of performance attainable, switching times of the Siliconix 2N4391 are given below

Device	td(max)	tr(max)	toff(max)	tf(max)	RL
2N4391	15ns	5ns	20ns	15ns	830 ohms

where t_d = turn-on delay. t_r = rise time. t_{off} = turn-off delay. t_f = fall time. R_L = load resistance.

1.9.5 Pinch-Off Voltage (Vp) and Threshold Voltage ($V_{GS(th)}$)

1.9.5.1 Pinch-off Voltage

In Section 1.7 the pinch-off voltage Vp of a junction FET was defined as the drain-to-gate voltage at which the channel begins to pinch-off. This voltage is largely determined by the depth of the channel and by the impurity concentration in the channel. Junction FETs of a given geometry are manufactured to various Vp ranges by controlling the depth of the gate diffusion into the channel.

A knowledge of Vp is important since most of the other parameters may be predicted from it. In particular, both I_{DSS} and $r_{DS(ON)}$ are functions of Vp. The expression 'begins to pinch-off" is an inexact definition and it becomes difficult to specify and test for Vp as a drain-to-gate voltage. For this reason, JFET data sheets specify $V_{GS(OFF)}$ which has the same magnitude but opposite polarity to the pinch-off voltage. $V_{GS(OFF)}$ is the gate-to-source voltage required to turn OFF the FET and is specified for a particular value of drain voltage and current. Fig. 1.35 shows the values of I_{DSS} and $r_{DS(ON)}$ plotted against $V_{GS(OFF)}$ for a typical n-channel JFET geometry.

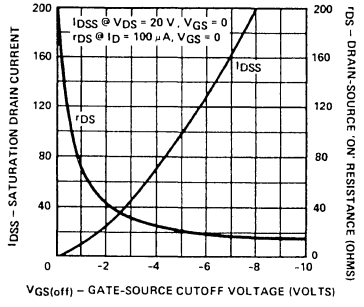


Fig. 1.35
r_{DS} and I_{DSS} vs. $V_{GS(OFF)}$ for an n-channel JFET geometry.

Measurements show that I_{DSS} is approximately proportional to $(Vp)^{1.5}$ and that r_{DS} is approximately proportional to $(Vp)^{-0.5}$.

Pinch-off voltage shows a slight increase with temperature. The voltage Vp, consists of the pinch-off potential Wo between gate and channel and the junction barrier potential ψ (equation 1.12)

$$Vp = Wo - \psi \qquad \text{eqn. 1.12}$$

Wo is constant with temperature, its value being determined by the charge carrier concentration and the square of the channel depth. The junction barrier potential decreases by about 2.2 millivolts /°C, so Vp will increase at the same rate.

1.9.5.2 Threshold Voltage

The threshold voltage of MOS devices depends upon the work functions between the metal gate-dielectric-semiconductor interfaces, also on the thickness and permittivity of the dielectric. Silicon MOS switches with silicon dioxide as the dielectric are manufactured using either high or low threshold processes, the basic difference between the two processes being in the choice of the silicon crystal orientation. The high threshold PMOS process uses a '111' orientation n-type substrate and has a threshold voltage of about 4 volts. For low threshold a '100' orientation is used giving a $V_{GS(th)}$ of about 2 volts.

If enhancement MOSFETS are used for analogue switching, a low threshold voltage is desirable to minimise the gate voltage excursion required. Thus, even with the low threshold processes, a minimum V_{GS} of 2 to 3 volts is required to turn the switch ON. This can be a disadvantage for applications involving low analogue signals, as considerable errors can be introduced by charge coupling through the gate-channel capacitance. FETS with a low $V_{GS(th)}$ (or Vp) are therefore preferable for such applications. The substrate bias has a considerable effect on the value of $V_{GS(th)}$ for, if the substrate-channel junction reverse bias is increased, a higher gate voltage is required to maintain conduction, Fig. 1.36.

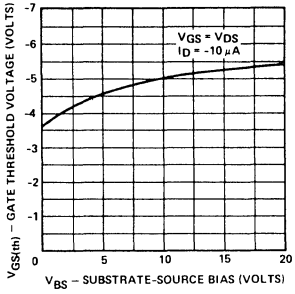


Fig. 1.36 **Gate Threshold Voltage** vs. **Substrate Bias for the Siliconix M103 p-channel enhancement MOSFET.**

Increasing temperature causes a reduction in $V_{GS(th)}$ by about 4 millivolts /°C for the high threshold process and about 2.7 milivolts /°C for low threshold devices. In addition, if the manufacturing process is not clean, a significant shift in $V_{GS(th)}$ can occur if the device is operated at high temperatures for any length of time. This shift is the result of a migration of impurity ions in the oxide which occurs at elevated temperature and under the influence of applied voltages. When the device returns to a normal working temperature the redistribution of charges in the gate oxide results in a change of threshold voltage. The impurities are normally positively charged sodium ions so that if the gate in a PMOS device is maintained at a negative voltage and at high temperature, the ions will be attracted away from the oxide/semiconductor interface with a consequent reduction in threshold voltage. The magnitude of the shift in $V_{GS(th)}$ due to this mechanism depends on time, temperature, impurity concentration and gate bias voltage.

1.9.6 Saturation Current IDSS

A knowledge of the maximum drain current that a FET can conduct is important in analogue switch applications. Ideally, an analogue switch should have constant ON resistance over the full signal range, so that for normal purposes the drain current should be considerably less than the saturation drain current. Also in applications involving sample-and-hold circuits the capacitor charging rate can be affected by the IDSS value.

Equation 1.1 showed how the drain saturation current of an n-channel JFET varied with gate-source voltage for a given Vp and IDSS, and this is illustrated graphically in Fig. 1.37.

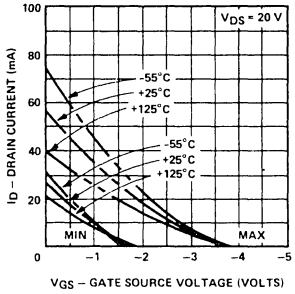


Fig. 1.37 **Drain Current** vs. **Gate-Source Voltage for a typical n-channel JFET.**

It can be seen in Fig. 1.37 that IDSS falls considerably with increasing temperature. This is due to a reduction in the channel carrier mobility. Junction FETS are presently available with IDSS values ranging from a few milliamperes to over 1 ampere. For MOSFETS the drain saturation current was given by equation 1.4 and a typical example is illustrated in Fig. 1.38.

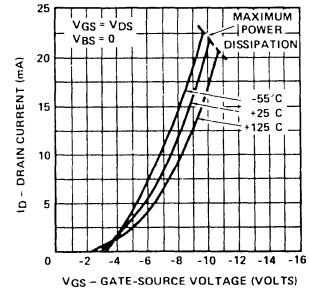


Fig. 1.38 **Drain Saturation Current** vs. **V_{GS} for a typical p-channel enhancement MOSFET.**

Since MOSFETS can operate in enhancement mode, the maximum drain saturation current is usually limited by the maximum power dissipation or gate breakdown voltages of the device.

1.9.7 Breakdown Voltage

The maximum analogue signal which may be switched is limited by the gate-to-channel breakdown voltage or the drain-to-source breakdown voltage. In junction FETS breakdown results from avalanche multiplication of carriers in the depletion region. On JFET data sheets this breakdown voltage is given the

symbol BV_{GSS}, that is, the breakdown between gate and source with the source and drain electrically short ciruited. Typical gate-to-channel breakdown voltages for junction FETs are in the range 30-100 volts, although for the Siliconix U328 n-channel JFET, BV_{GSS} is a minimum of —275 volts. The gate dielectric of MOSFETS usually has a breakdown voltage in excess of 100 volts. However, avalanche breakdown between the channel and body restricts the maximum drain-to-source voltage. The minimum drain-to source breakdown BV_{DSS} for MOSFETS is usually of the order of 30 volts. For high breakdown geometries, such as the Siliconix M119 p-channel enhancement MOSFET, minimum BV_{DSS} is -75 volts.

For 'protected' MOSFETS, the maximum analogue signal is also limited by the breakdown voltage of the gate-to-body diode BV_{GBS}. If this value is exceeded by the analogue-to-gate voltage, current will flow from the channel into the gate via the substrate. Data Sheets for most protected MOSFETS specify minimum values of BV_{GBS} in the range 30-40 volts although the Siliconix M119 has a minimum BV_{GBS} of —80 volts.

1.10 SUMMARY

This chapter has considered, in broad terms, the basic family of field effect transistors and their performance as analogue switches. The following chapter will deal with the wider range of integrated circuits and hybrids, including FET switches, drivers and driver-gate combinations which are presently available.

Chapter 2

Switch and Driver Circuits

2.1 In the previous chapter it was shown that FETs have many of the characterisitics that are desirable of a good switch. However, a switch has to be controlled; it has to be driven OFF or ON. The basic arrangement of any switch is shown in Fig. 2.1. In a rotary mechanical switch the driver is the spindle, in a relay the driver is a coil, and in a solid-state switch the driver is usually a semiconductor circuit. The driver circuit makes a significant contribution to the overall performance of the switch or gate.

Innumerable circuits have been designed to drive FET switches *(Ref. 2.1 & 2.2)* and about 10 of these have been adopted as industry standards. The mode of operation of these circuits will be described and the interaction between switch and driver discussed and analysed.

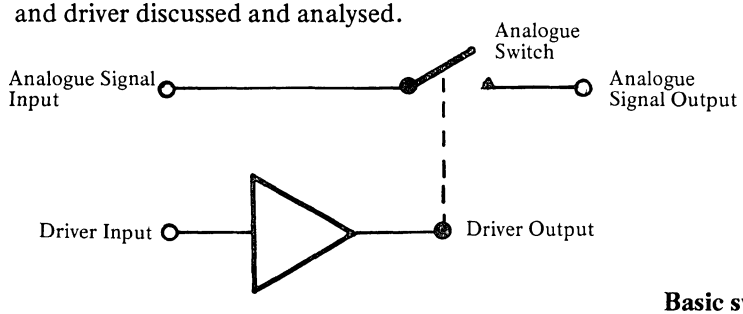


Fig. 2.1
Basic switch and driver

Although the analogue signal input and output terminals of the FET switch will frequently be referred to in the ensuing chapter as the source and drain, it will be on the understanding that the source and drain are interchangeable, because the majority of switching FETs are bilateral and symmetrical.

2.2 TYPES OF FET SWITCHES.

Before investigating the various types of driver circuits, the prime differences between JFET, PMOS (or NMOS) and CMOS which form the three families of FET switches should be stressed.

2.2.1 **JFET** The p- or n- channel JFET switch is a depletion mode device. To maintain it in the ON state the value of V_{GS} should be at or near zero volts. To implement the ON state, the gate-and-source or gate-and-drain can be connected together through a resistor, or the gate-to-channel diode can be slightly forward biased by the leakage current of a diode placed in the gate circuit. In either case, the V_{GS} will remain at or near zero volts for all d.c. levels of analogue signal. Consequently, the resistance of the FET is kept constant and equal to $r_{DS(on)}$ for all values of analogue signal.

2.2.2 **MOSFET** To maintain an n- or p- channel MOSFET switch in the ON state, the gate is usually held at some reference voltage which ensures that the V_{GS}

exceeds the threshold voltage of the MOSFET even when the analogue signal (V_A) is at the extremes of its dynamic range, hence keeping the MOSFET on for all values of V_A. However, since the r_{DS} of a MOSFET is related to V_{GS} by equation 1.7, the r_{DS} will vary as the analogue signal voltage level varies (Fig. 2.2).

The variation in ON resistance of the P and NMOS transistor with analogue signal is a serious limitation in some applications since it can cause distortion of the analogue output signal. This can be minimised if the load resistance is high compared with the switch resistance.

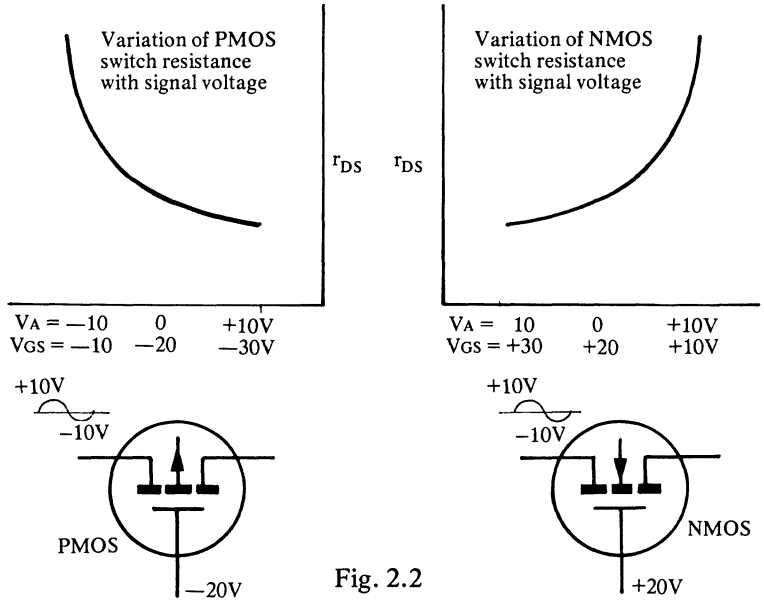


Fig. 2.2

2.2.3 **CMOS** For a CMOS switch, the ON resistance is that resulting from a parallel combination of n- and p- channel devices. The effective resistance is almost constant over a wide analogue signal range as shown in Fig. 2.3.

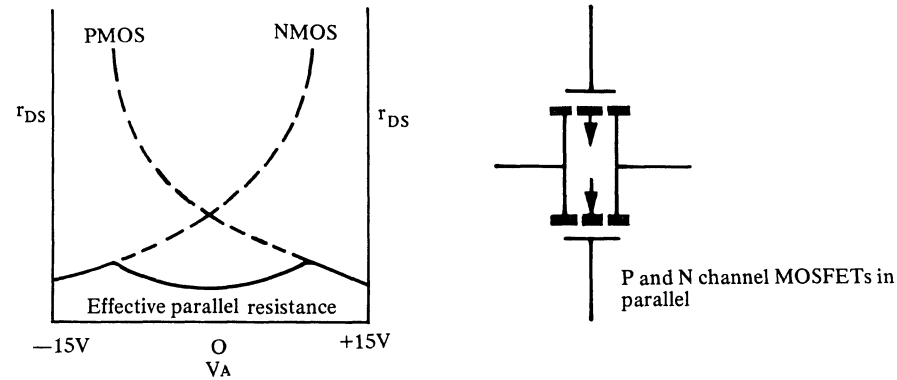


Fig. 2.3 **Graph of CMOS switch resistance vs. analogue signal**

2.3 DRIVER CIRCUITS

2.3.1 Shunt-Resistor Driver

Figs. 2.4 and 2.5 show the simplest form of driver circuits. In Fig. 2.4 the analogue switch is an n-channel JFET and in Fig. 2.5 the analogue switch is a p-channel MOSFET.

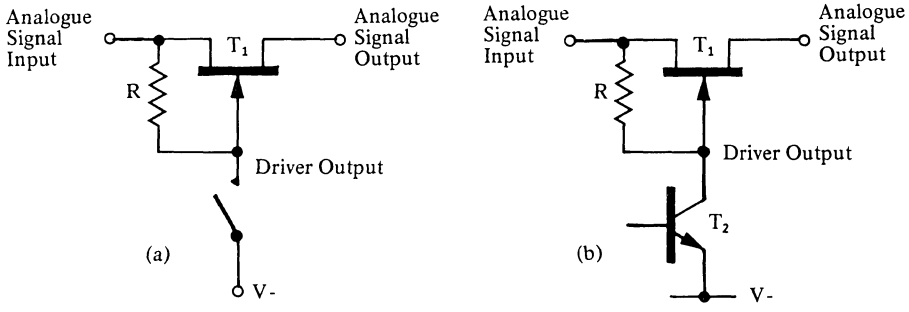


Fig. 2.4 **Simple JFET driver circuits**

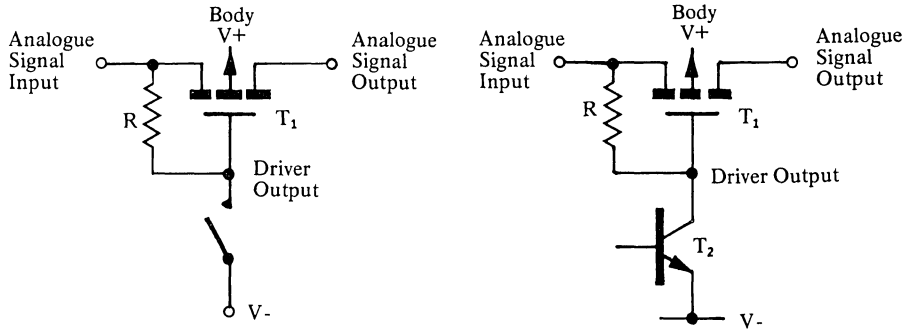


Fig. 2.5 **Simple MOS driver circuits**

The switch in the gate circuit of Fig. 2.4a or 2.5a could be a bipolar or a field effect transistor. A bipolar is shown for convenience in Figs. 2.4b and 2.5b. The switch in the driver circuit can be considered to be closed when T_2 is saturated and open when T_2 is OFF. For the JFET switches, Fig. 2.4b shows that when the bipolar T_2 turns ON, the gate voltage of T_1 is taken to the negative rail voltage. Consequently, switch T_1 will turn OFF, provided the analogue signal voltage level is always more positive than the negative supply rail by the $V_{GS(off)}$ value of T_1, i.e.

$$|\hat{V}_A| < |V-| - |V_{GS(off)}| - Vce(sat) \qquad \text{eqn. 2.1}$$

where $\hat{V}_A$ is the peak negative excursion of the analogue signal, V- is the negative supply voltage, $V_{GS(off)}$ is the pinch-off voltage of the JFET, and Vce(sat) is the saturation voltage of T_2. When T_2 is turned off, the gate voltage of T_1 is the same as the source voltage since the driver transistor's collector current and JFET gate current are negligible. Hence, the analogue switch is ON.

The peak negative analogue signal excursion is given by equation 2.1 The peak positive excursion of the analogue signal with this type of driver is determined by the collector breakdown voltage of T_2 (BVceo)* when the switch T_1 is ON, provided that there is no significant voltage drop across the switch terminals.

With T_1 OFF, the peak positive analogue signal excursion is determined by the gate-to-source and gate-to-drain breakdown voltages of the FET. Hence, with this simple driver the analogue signal range is determined by the choice of components, and since there are JFETs and bipolars available with breakdown voltages in excess of 200V, large analogue signals can be switched.

When the gate voltage of the MOSFET analogue switch T_1 is taken to the negative rail voltage (Fig. 2.5b), the switch is ON and will remain ON provided the peak value of negative analogue signal does not fall to within one $V_{GS(th)}$ level of the negative supply. In practice, the peak negative analogue signal should be at least $V_{GS(th)}$ + K volts more positive than the negative supply where K is the additional voltage required to ensure the MOSFET is fully ON. K is normally of the order of 2 or 3 volts. The greater the value of K, the lower the ON resistance of the MOS. The relationship between the above parameters can be expressed in equation form (equation 2.2).

$$\left| \hat{V}_A \right| < \left| V- \right| - \left| V_{GS(th)} \right| - K \qquad \text{eqn. 2.2}$$

When the switch in the driver circuit of Fig. 2.5 is off, the gate-to-source voltage is zero volts which will cause the MOSFET to turn OFF. In the ON and OFF conditions, the peak permissible positive analogue signal excursion is V+ to avoid forward biasing the drain-to-body and/or source-to-body diode (Fig. 2.5). It is not advisable to connect the body of T_1 to the source terminal in this type of application since it is possible that the source may under certain conditions be negative with respect to the drain and hence the drain to body diode would conduct. The body should, therefore, be connected to a supply voltage that is at least equal to the peak positive value of the analogue signal.

In both the circuits of Figs. 2.4 and 2.5 the main problem is that current is bled from the analogue signal path into the driver circuit. To reduce the amount of current bled, the value of R should be made as high as possible. However, if R is increased, the rise time of the gate voltage becomes greater. A high value of R poses another problem. At higher analogue frequencies, the gate-to-source voltage of the analogue switch can be modulated by the analogue signal.

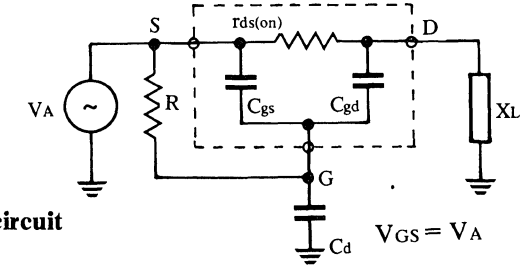


Fig. 2.6
JFET shunt driver HF equivalent circuit

* BVces may be considered if the base is connected to emitter in the OFF state, but this is not recommended.

2.3.1.1 Case 1. **JFET Switch resistance modulation by high frequency signals**

The equivalent circuit of the driver and JFET switch in the ON state is shown in Fig. 2.6. If $r_{DS(on)}$ is low compared with both the load impedance and the driver output impedance at the frequency of interest, and furthermore that the driver output impedance is effectively the output capacitance of the switch T_2 (Fig. 2.4) then:

$$V_{GS} = \frac{\left(\frac{RXgs\ Xgd}{RXgs + RXgd + Xgd\ Xgs}\right)}{\left(\frac{RXgs\ Xgd}{RXgs + RXgd + Xgd\ Xgs} + Xd\right)} \cdot V_A \qquad \text{eqn. 2.3}$$

Xgd, Xgs and Xd are the impedances of Cgd, Cgs and Cd respectively at the applied analogue signal frequency. Since Xgs = Xgd for switching FETS then:

$$Vgs = \frac{RXgd \cdot V_A}{Xd\,(2R + Xgd) + RXgd} \qquad \text{eqn. 2.4}$$

CHAPTER 2

Thus, we can see that a spurious value of Vgs is generated across the switch terminals due to V_A. The extent of the ON resistance modulation caused by this changing gate to source voltage can be calculated for a JFET from:

$$rds \approx \frac{rds(on)}{1 - \frac{V_{GS}}{Vp}} \qquad \text{eqn. 2.5}$$

For example, if f = 100kHz, Cgd = Cgs = 3pF, Cd = 1.0pF, R = 10^6 ohms, $r_{ds(on)}$ = 30 ohms Vp = 5V and V_A = 10V peak then from eqn. 2.4, Vgs = 1.16V, and

$$\Delta rds = 30 - \frac{30}{1 - \frac{1.16}{5}} \approx 9\Omega$$

at a frequency of f = 1MHz, Vgs = 0.13, V_A = 1.3V

$$\therefore \Delta\, rds = 30 - \frac{30}{1 - \frac{1.4}{5}} \approx 11.6\ \text{ohm}$$

It can be seen that the JFET ON resistance variation increases as the frequency increases.

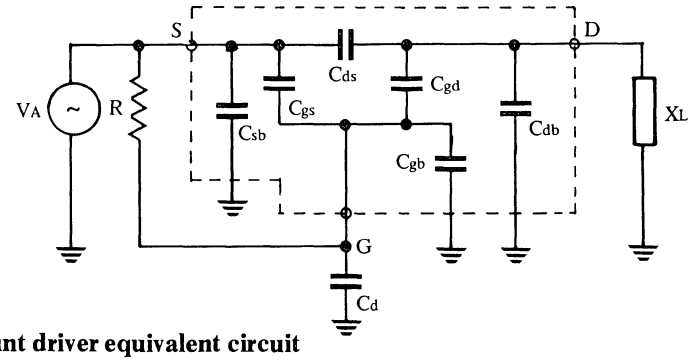


Fig. 2.7
MOSFET shunt driver equivalent circuit

2.3.1.2 Case 2. **MOSFET Switch resistance modulation by high frequency signals.**

In the circuit that utilises a MOSFET as the output switch, the result of this V_{GS} modulation due to the capacitive divider chain is very different. The Vgs voltage generated across R (Fig. 2.5b) can, if it becomes sufficiently large, cause the MOSFET to turn ON when it should be in the OFF state. The MOSFET high frequency equivalent circuit in the OFF state is shown in Fig. 2.7. Since Cds is usually much less than Cgd or Cgs, it can be neglected. Let X_Q be the impedance of Cgd in series with the parallel combination of Xdb and X_L so that

$$X_Q = \frac{X_L X_{db}}{X_L + X_{db}} + X_{gd}$$

$$\therefore Vgs = V_A \cdot \frac{\frac{X_{gs}R}{X_{gs}+R}}{\left(\frac{X_{gs}R}{X_{gs}+R}\right) + \left(\frac{X_d X_{gb} X_Q}{X_{gb}X_d + X_{gb}X_Q + X_d X_Q}\right)} \qquad \text{eqn. 2.6}$$

and if V_{GS} exceeds $V_{GS(th)}$ the switch till turn ON.

The low frequency errors due to leakage and ON resistance, and the high frequency isolation for this driver switch combination will be discussed later, since there are factors common to many types of drivers.

2.3.2 **Diode Coupled Driver**

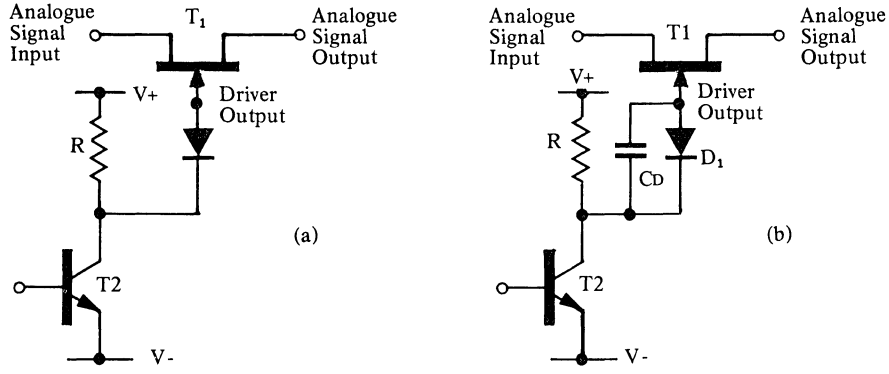


Fig. 2.8 **Simple diode coupled driver circuit without (a) and with (b) speed up capacitor**

Due to the large value of shunt resistance required by the shunt-resistor driver the switching speeds are slow. To attain a fast switching speed and yet prevent any current being bled from the analogue signal path, when using a JFET as the analogue switch, a diode circuit (Fig. 2.8) can be used to drive the switch *(Ref. 2.3)*. The load resistor R (Fig. 2.8a) is chosen such that T_2 saturates when turned on. The diode D_1 is forward biased during the transition and remains forward biased after the transition, although in the steady state it only conducts the gate leakage current of T_1. Consequently, the gate of T_1 is held at, or within a few hundred millivolts of the negative rail voltage V-. Only leakage current is bled from the analogue signal path in this state. When T_2 is turned off, the collector voltage rises to the positive voltage supply V+ and the diode will become reverse

biased if $V+ > \hat{V}_A$, where $\hat{V}_A$ is the peak positive value of the analogue signal. The reverse diode leakage current tends to forward bias the gate-to-channel junction of T_1 hence holding the FET switch ON. This diode leakage current is very low, less than 1 microamp, and consequently the gate to channel voltage is extremely small so that V_{GS} tends to zero volts. With this driver switch arrangement, the peak positive analogue signal that is permissible is V+ because the gate of T_1 is held at V+ and any positive analogue signal excursion above this value will cause T_1 to start turning off.

The peak negative analogue signal excursion permissible, $\check{V}_A$, is again determined by:

$$|\check{V}_A| \leqslant |V-| - |Vp| - Vce_2(sat) \qquad \text{eqn. 2.7}$$

During the transition from OFF to ON the total gate capacitance of the switch T_1 has to be charged by the leakage current of the diode, and because the leakage current is small, the charging time can be long. Therefore, it is common practice to speed up this circuit by shunting the diode with a speed up capacitor as in Fig. 2.8 b. The positive transition at the collector of T_2 is thus coupled on to the gate of FET T_1 so that the latter turns ON much more rapidly.

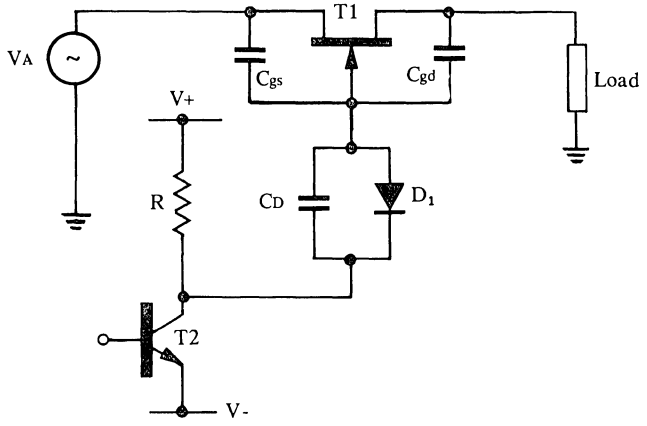


Fig. 2.9
Equivalent circuit of diode coupled driver and JFET

To maximise the fraction of the T_2 collector voltage swing that is coupled on to the gate of T_1, C_D has to be as large as possible. However, increasing this capacitor can cause modulation of the gate to source voltage by analogue signals of high frequencies and its value should be chosen carefully. Inspection of Fig. 2.9 shows that when T_2 is OFF and T_1 is ON, and provided that the resistance of T_1 is small in comparison with the load resistance, then

$$Vgs \approx \frac{\frac{Xgs \cdot Xgd}{Xgs + Xgd}}{R + Xd + \frac{Xgs\,Xgd}{Xgs + Xgd}} \cdot V_A \qquad \text{eqn. 2.8}$$

and if Xgs = Xgd

$$Vgs = \frac{Xgs \cdot V_A}{2\left(R + X_D + \frac{Xgs}{2}\right)} \qquad \text{eqn. 2.9}$$

Thus, when C_D is large in comparison with Cgs (and Cgd) then V_{GS} tends towards the value of V_A because R is relatively low in value to facilitate fast switching. To minimise the modulation of V_{GS} at higher frequencies, C_D needs to be low in value. However, C_D needs to be large to minimise the turn ON transition time of the switch. Therefore, a compromise has to be made.

As for the previous driver/switch combinations, the leakage and isolation performance will be discussed later since these factors are common to many other different types.

2.3.3 Isolated Gate Driver

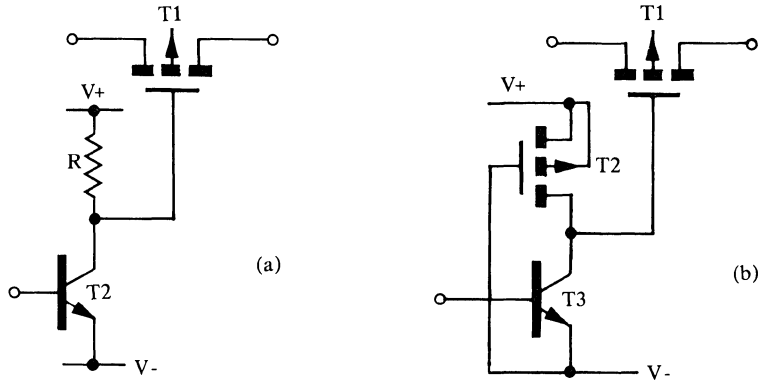


Fig. 2.10 **Driver for MOS switches**

When driving the MOSFET as an analogue switch it is possible to use the configuration shown in Fig. 2.10 a. This is a very simple and effective circuit. No current is bled from the analogue signal path, and since R can be relatively small in value as compared with R in section 2.3.1, the switching speed is quite good.

The resistor R can be changed for a MOSFET as shown in Fig. 2.10b. This is particularly advantageous when using this driver in monolithic ICs because the MOSFET takes up much less chip area than a resistor of equivalent resistance.

The peak negative signal excursion is again

$$|\hat{V}_A| < |V\text{-}| - |V_{GS(th)}| - K$$

—as was quoted in equation 2.2.

Modulation of V_{GS} by higher analogue signal frequencies is very small in these two circuits because R (or the resistance of T_2 when on) is small compared with the impedance of Cgs even for analogue signal frequencies in excess of 1MHz.

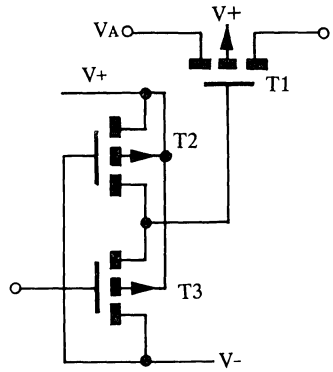


Fig. 2.11
All PMOS drivers and switch

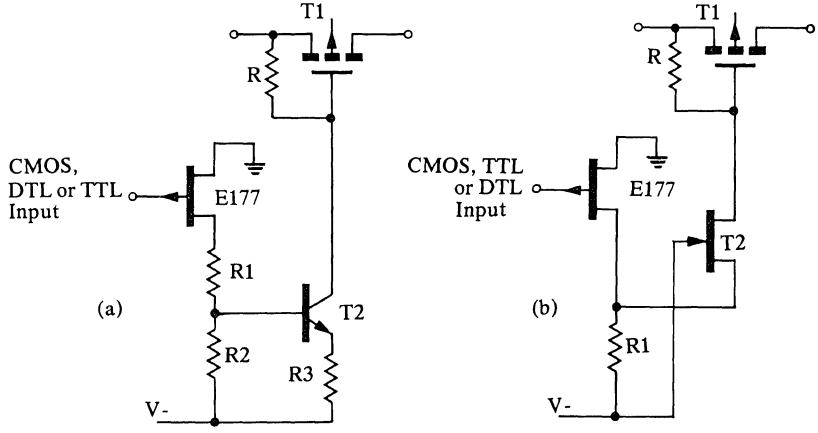
A logical extension of the circuit shown in Fig. 2.10 is the one shown in Fig. 2.11. This is now an all PMOS arrangement which lends itself to large monolithic IC arrays of switches such as the Siliconix DG501 and DG503.

The gate voltage of T_1 swings between V+ and $[(V-) + V_{GS(th)_3}]$ depending on the input voltage to the gate of T_3. If the voltage input to T_3 is low (V-), the drain voltage of T_3 falls to V- because the geometries of T_2 and T_3 are arranged such that T_3 will conduct more current under these bias conditions. When the gate voltage to T_3 is high (V+), it is in its high resistance state and therefore the drain voltage rises to (V+). The peak positive analogue voltage excursion for the circuits in Fig. 2.10 and 2.11 is V+ because if the analogue signal exceeds this value, the source to body and/or drain to body diode of T_1 will start to conduct.

2.3.4 The constant ON resistance PMOS driver

The variation in ON resistance which the PMOS switch usually suffers from, as described in section 2.2.2, can be overcome by driving the switch from a constant current source instead of connecting the gate to a constant voltage value. This is not a frequently encountered circuit but can be built with discrete components. Examples are shown in Figs. 2.12 a and 2.12 b.

Fig. 2.12 **Constant ON resistance PMOS drivers**



This circuit requires that the supply rail voltages be greater than the analogue signal voltage swing by the $V_{GS(th)}$ + K value (as specified in section 2.3.1) plus the voltage drop across the current source.

2.3.5 The Multi FET Driver

The driver shown in Fig. 2.13 is a fast switch with t(on) and t(off) approximately 150 nanoseconds. It exemplifies the problems of building a fast switch with discrete devices or multiple chips. It is expensive because of the increased number of components. Inevitably associated with high component count is a higher assembly cost, increased printed circuit board area and reduced reliability.

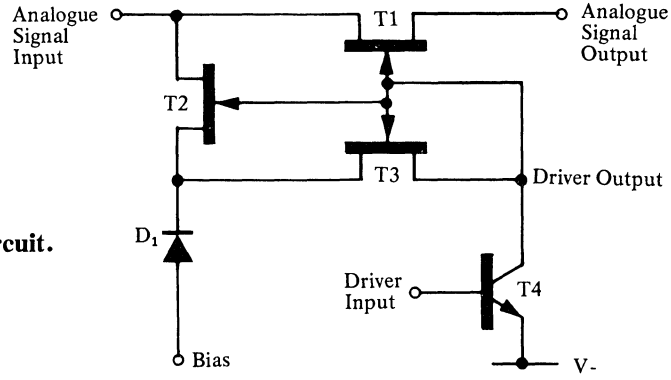


Fig. 2.13
Multi FET driver circuit.

The bias voltage is usually chosen to be approximately half way between V- and 0V. Hence when T_4 is ON (saturated), the gate voltages of T_1, T_2 and T_3 are within a Vce(sat) of the negative rail voltage (V-), so that T_1 is OFF if:

$$|V_A| < |V-| - |Vce(sat)_4| - |Vp_1| \qquad \text{eqn. 2.10}$$

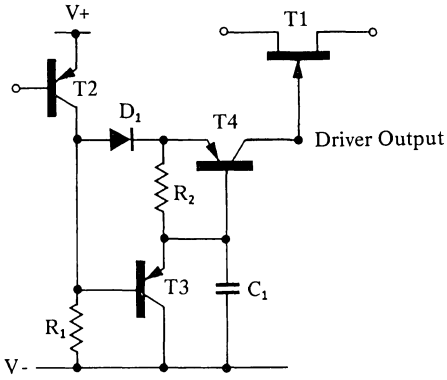
where Vp_1 is the pinch off voltage of T_1 and $Vce(sat)_4$ is the saturation voltage of T_4. Whilst T_1 is in this off condition T_3 is conducting at its I_{DSS} value. When T_4 turns OFF, the source and gate voltage of T_3 will rise towards Vbias. As soon as T_3 comes out of the saturation region,* T_2 gate and source are effectively connected together by the r_{DS} of T_3. Hence, the V_{GS} of T_2 will become zero volts and T_2 is then in its $r_{DS(on)}$ state. The gate and source terminals of T_1 are thus connected together via the $r_{DS(on)}$ of T_2 and T_3 in series. This provides a relatively low resistance path which keeps the modulation of V_{GS} down at higher frequencies. The diode D_1 blocks current flow from the signal path into the bias supply. To minimise the switching speed of this circuit, the base of T_4 should not be overdriven. This could be ensured by using a Schottky clamp.

2.3.6 The Charge Coupled Driver

It is apparent from the preceding sections that the simpler driver circuits with a low component count, do not maximise the standards of performance that can be achieved with FET switches. Better performance is obtainable from more complex circuits but the increased component count with its associated high cost, tends to prohibit the construction of the circuits from discrete components. The advent of ICs enabled sophisticated driver circuits to be designed offering improved performance at relatively low costs. One of the earliest circuits evolved, was the charge coupled driver shown in Fig. 2.14

*Note the different meaning of "saturation" in connection with FETs as opposed to bipolars (see Chapter 1, section 1.7)

Fig. 2.14
Charge coupled driver circuit



Analogue switches of this type use a hybrid technology. The output switches consist of discrete JFET chips, whilst the driver circuitry comprises an integrated circuit.

Turn ON. When T_2 is provided with sufficient base current to saturate, the diode D_1 conducts and C_1 is charged by the base current of T_4 and the current through R_2. During this time T_4 will conduct and some charge will be injected into the analogue signal path. The amount of charge is given $\beta_4 C_1 \Delta V$, where β_4 is the current again of T_4, and ΔV is the voltage transition on the plate of capacitor C_1. Eventually C_1 will be charged to within a Vbe drop of the emitter voltage of T_4, and T_4 will turn off. The capacitor will be trickle charged through R_2, so that the base of T_4 will remain within a diode voltage drop (D_1) plus the Vce(sat) of T_2 of the positive voltage supply. In this condition, the FET T_1 is held ON by the collector leakage current of T_4.

Turn OFF. When T_2 is starved of base current, T_2 turns off and its collector voltage falls towards V-. In doing so, T_3 is turned on and C_1 dumps its charge via T_3 to the negative rail. Hence, the base of T_4 is taken down to within one base emitter diode drop of V-. During this transition the collector base diode of T_4 is forward biased and hence the gate voltage of T_1 is taken to within a few hundred millivolts of the negative supply rail voltage. In this state T_1 is well and truly off, provided that:

$$|\check{V}_A| < |V-| - |Vp| - 500mV \qquad \text{eqn. 2.11}$$

The 500mV is a nominal value chosen to allow for the small voltage drops across the base emitter diode of T_3 and the collector base diode of T_4. The peak permissible positive analogue voltage transition is equal to V+. If the signal voltage were to exceed this the switch T_1 would start to turn off. This circuit overcomes the need for a large value of speed up capacitor which was necessary for the diode coupled arrangement and yet maintains a low level of V_{GS} modulation by HF analogue signals. The fact that C_1 has to be charged and discharged, and the bipolar transistors saturate, does mean that these circuits are not very fast with regard to switching speed. Furthermore, if the driver signal transition is very slow, then it is possible that C_1 will be charged through R_2 because the voltage drop across R_2 will never be large enough for T_4 to turn ON. Consequently, the driver output capacitance of the FET switch, will have to be charged by the base to collector leakage current of T_4. The turn-on of T_1 will therefore be extremely long. For instance, if the base collector leakage is 100nA and the driver output node capacitance is 7pF, the time taken to charge to 20 volts will be 1.4 millisecs. However, it is very rarely that one gets a sufficiently slow input transition for this effect to occur, and the normal switching speeds are 1μs (max) for t(on) and 2μs (max) for t(off).

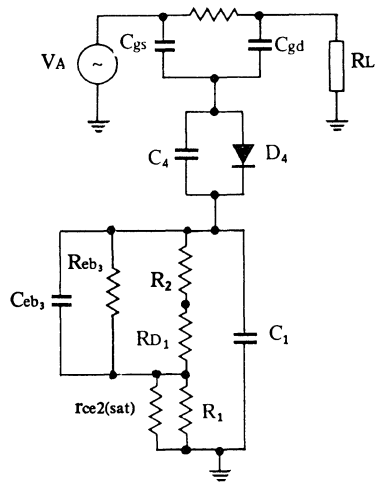


Fig. 2.15
Equivalent circuit of charge coupled driver and JFET switch.

The equation of the V_{GS} modulation by high frequency analogue signals for this circuit is very similar to that of the diode coupled driver (section 2.3.2). Fig. 2.15 is the equivalent circuit of Fig. 2.14. D_4 is the collector base diode of T_4, and C_4 is the associated capacitance. Reb_3 is the zero bias emitter-base resistance of T_3, and R_{D_1} is the resistance of the diode D_1 both are only conducting a trickle current and consequently appear as very high resistances, therefore $R_{D_1} \gg R_2$ and $R_{D_1} \gg R_1$. $r_{ce(sat)_2}$ is much smaller than R_1. By inspection of Fig. 2.15 and again assuming that $r_{DS(on)}$ is small in comparison with R_L and that Cgs = Cgd, we have

$$Vgs = \frac{Xgs2}{Xgs + X_4 + X_5} \cdot V_A \qquad \text{eqn. 2.12}$$

where X_4 is the parallel impedance of C_4 and R_{D_4}, and X_5 is the parallel impedance of C_1, R_{D_1}, Reb_3 and Ceb_3. At higher frequencies, the large resistive components can be ignored when compared with the capacitive components of impedance. The values of C_1, C_4 and Ceb_3 are low in comparison to the speed-up capacitor values required by the drivers of section 2.3.2. Hence, there is less modulation of the switch resistance.

The high frequency isolation of this circuit will be discussed later.

2.3.7 A High Speed Driver

A more recent addition to the range of JFET drivers offers faster switching speeds and introduce less V_{GS} modulation of the JFET switch by high frequency analogue signals. These circuits combine PMOS and Schottky clamped bipolars on the same chip.

However, when these circuits were designed, it was not easy to incorporate the JFET on the same chip. Consequently, these devices also comprise hybrid technology.

With this driver, all stage delays have been minimised to get the best speed performance and therefore the total circuit should be considered. This type of driver is used on the Siliconix DG180 and DG190 series of driver gates. Fig. 2.16 shows one channel of a fast driver circuit for JFET switches. The input stage is differential, and the collectors of the input transistors are restricted to a Vbe

voltage swing. Thus, the first stage can operate at high speed. The second stage uses Schottky transistors to prevent saturation, also feed forward capacitors to increase the speed of transition.

The transition speed of the second stage is further improved by using active PMOS loads which are driven in antiphase. When T_5 turns ON and T_7 turns off, T_4 changes from a low resistance to a very high resistance state. T_6 does the opposite which helps to reduce the time constant seen at the collector of T_7 and reduces the transition time at the collectors of T_5 and T_7.

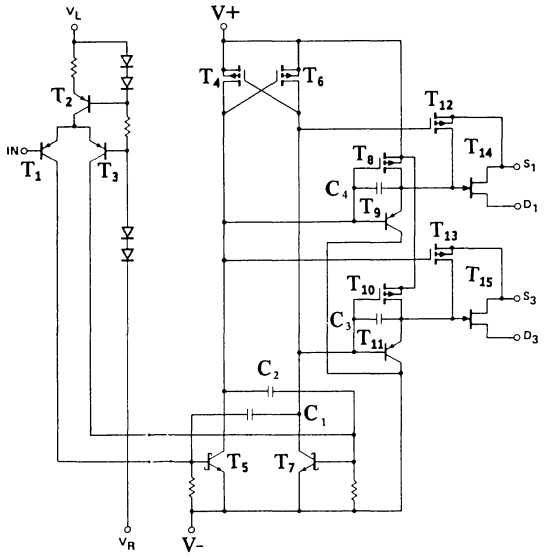


Fig. 2.16
One channel of a high speed driver and JFET switch.

When T_5 turns off and the collector voltage rises towards V+, T_{13} also turns off. T_{10} and T_{11} are driven by an antiphase signal and T_{10} turns ON whilst the emitter of T_{11} pulls the gate of T_{15} to within a Vbe drop of the collector voltage of T_7 which is within half a volt or so of the negative supply voltage. Hence, T_{15} is hard OFF for any analogue signal voltage V_A provided that:

$$|V_A| < |V-| - |Vp| \qquad \text{eqn. 2.13.}$$

Almost simultaneously, T_{14} turns on as T_{15} turns off. The gate voltage of T_{14} is controlled by the source voltage of T_4 through the base emitter voltage drop of T_9. If T_5 turns OFF, the source of T_4 approaches V+ turning T_8 and T_9 OFF. However, the source of T_6 is near V- when the source of T_4 is at V+ and therefore T_{12} is ON. T_{12} provides a low resistance path between the gate source of T_{14} and reduces V_{GS} to practically zero. Hence, T_{14} is held hard ON. The capacitor C_4 helps to accelerate the positive transition of the T_{14} gate voltage by feeding the base transition of T_9 on to the emitter of T_9. If C_4 were not present the voltage on the total stray capacitance at the gate of T_{14} would have to decay to the positive rail through T_8 which is OFF and the reverse leakage across the base emitter of T_9. This would be a long decay time. The overall effect of all these refinements is a very fast driver circuit.

The peak permissible negative excursion of the analogue signal has already been given in equation 2.13. The right hand side of the inequality should exceed the

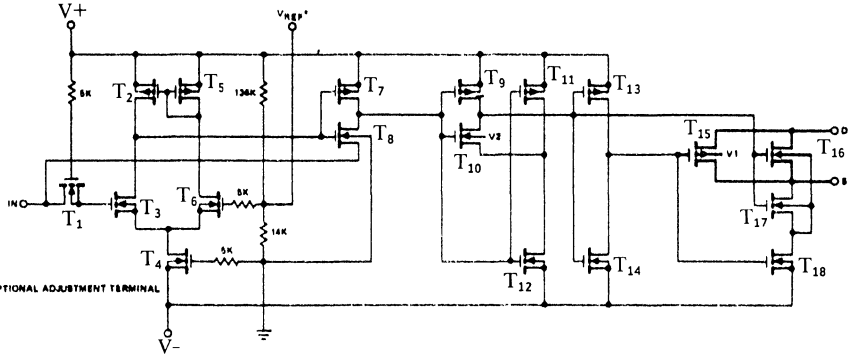
left hand side by at least half a volt. This allows for the voltage drop between the collector and emitter of T_5 or T_7 and the base emitter drops of T_9 and T_{11}.

The peak positive value of analogue signal is again equal to the positive supply voltage (V+).

Although there is a discussion on FET switch leakages later, it is worth noting here that the drain and source leakages of these devices are not equal. A MOSFET is connected to the source terminal of T_{14} and T_{15} (Fig. 2.16) and hence the source leakage is higher because of the additional leakage from the MOSFET drain into the body.

Modulation of the ON resistance at higher frequencies is very small because the source and gate of the JFET are connected together via the channel resistance of T_{12} (or T_{13}). The maximum value of the resistance is 6kohms and hence the Cgs, in the capacitive divider chain that usually causes the high frequency modulation, is shunted. The impedance of Cgs only begins to compare with the shunt resistance at around 10MHz analogue signal frequency. Switching speeds of typically 100ns can be achieved with the Siliconix version of this type of driver and in the case of the DG180 and 190 series of devices, a break-before-make switch action is guaranteed.

Fig. 2.17
CMOS switch and driver circuit (typical channel).



2.3.8 The CMOS Driver

A recent addition to the analogue switch range is the CMOS family of driver gates. The use of CMOS in the output switch gives far less variation in ON resistance over the analogue signal range than PMOS, as was shown in Fig. 2.3 section 2.2.3.

The driver stage is basically simple since the PMOS and NMOS switches are driven by complementary signals from the input and output nodes of an inverter (T_{13}, T_{14}) so that the p and n channel analogue switch FETs are ON or OFF together. In practice the analogue switch circuit is slightly complicated by the presence of 'body snatching' transistors T_{17} and T_{18} as shown in Fig. 2.17. These transistors serve to hold the body at a defined voltage which is essential to reduce leakage when the switches are OFF and also give repeatability in device behaviour. Transistor T_{17} shorts the body of the n-channel switch to the source when the switch is ON. Transistor T_{18} connects the body of the n-channel switch to the negative supply (V-) when the switch is OFF.

One of the major advantages of CMOS apart from the constancy of ON resistance is that the analogue signal can now equal the supply rails. This is unique to CMOS. There are some CMOS analogue switches manufactured in which the analogue signal can not equal the supply rail but this is a limitation imposed by the particular circuit technique or wafer processing used and not a limitation of the CMOS concept. Early CMOS circuits suffered from a latch-up phenomenon that has now been eliminated, and being a thing of the past will not be dwelt upon.

Because the gate to a.c. ground capacitance of both the n and p-channel FET switches is in parallel with the low resistances of the MOSFET driving the gate there is very little modulation of the ON resistance by high frequency analogue signals (Fig. 2.18).

This family of devices usually offers break-before-make action of the switches by ensuring that t(off) is less than t(on).

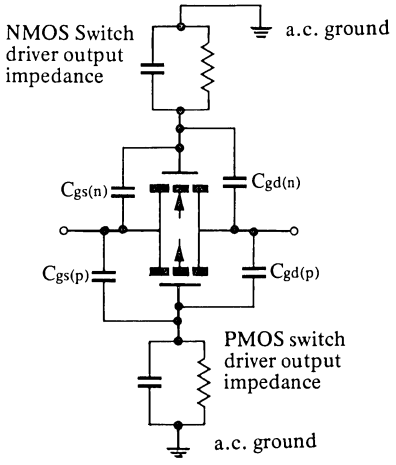


Fig. 2.18
CMOS switch equivalent circuit.

2.4 INTERFACE CIRCUITS

2.4.1 Bipolar Input Stages

Several different types of analogue driver circuits have been reviewed, but so far it has not been considered how the driver circuit can be made compatible with the available logic families such as TTL, CMOS, DTL or RTL. Although there are p channel junction FETs like the E177 that can handle small signals and be controlled directly from TTL, FET switches which handle signals of ±10V or more will require some interface circuitry. One of the simplest arrangements is shown in Fig. 2.19. The logic threshold is approximately (V_R + 0.7V)

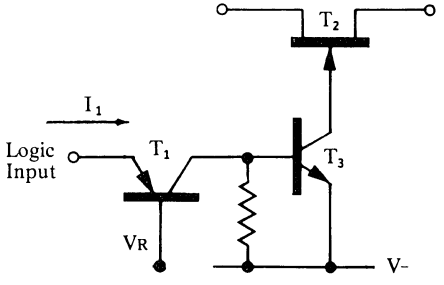


Fig. 2.19
TTL compatible driver.

If V_R is 0V then this circuit would be TTL, CMOS, DTL, and RTL compatible. The major disadvantage of this simple arrangement is the high level of input current (I_1) but it does have the advantage that only a single supply is required.

Another arrangement is shown in Fig. 2.20. The logic threshold level is now determined by the value of V_L and the resistors R_1 and R_2. The logic threshold voltage Vth is given as

$$Vth \approx V_L - V_{be} \left(\frac{R_1}{R_2} + 1\right) \qquad \text{eqn. 2.14}$$

Another commonly used input circuit to achieve logic compatibility is shown in Fig. 2.16. A variation on this is shown in Fig. 2.21. These are basically differential arrangements and the logic thresholds occur at $V_R + 2Vbe$ provided the diode drops are approximately equal to the Vbe drop at T_1.

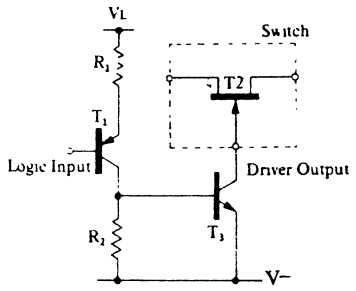


Fig. 2.20
Simple driver circuit compatible with TTL/DTL logic levels

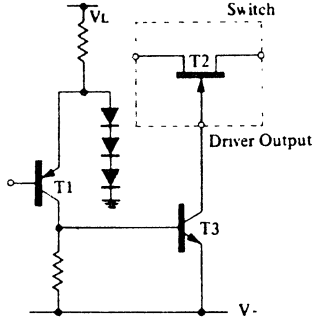


Fig. 2.21
TTL/DTL logic compatible driver

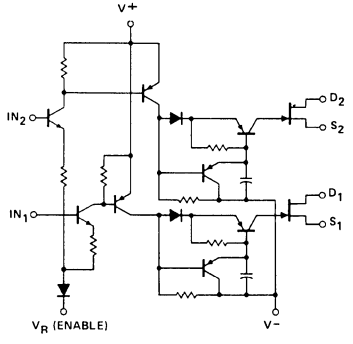


Fig. 2.22
Charge coupled driver with logic compatible input

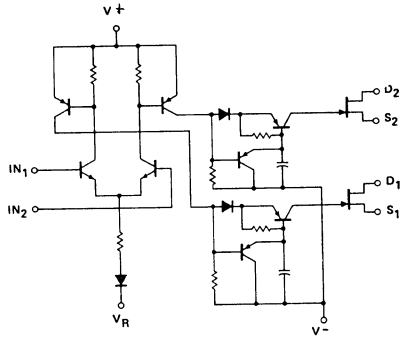


Fig. 2.23
Differential input driver and switch

Fig. 2.22 and 2.23 shows the arrangement used in the charge coupled drivers (e.g. DG133, DG144). In Fig. 2.22 the logic threshold voltage occurs at a level slightly greater than two diode voltage drops above V_R so that V_R can be used as an enable terminal. In Fig. 2.23 the input is truly differential.

2.4.2 PMOS FET Input Stages

The logic threshold level of the circuit shown in Fig. 2.24 is determined by the MOS process threshold voltage and the aspect ratios of the MOSFETS in the input stages. Examples of this are the Siliconix DG501 and DG503 which are TTL compatible.

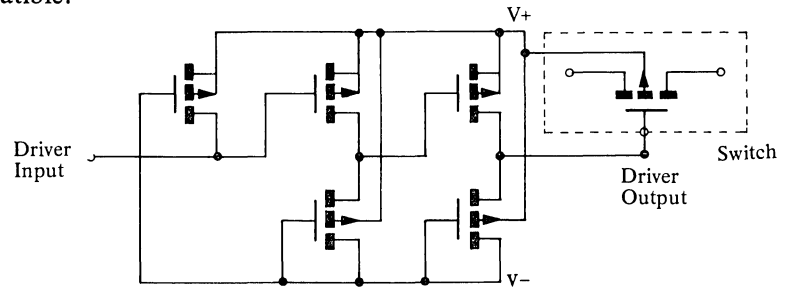


Fig. 2.24
Logic compatible PMOS driver switch.

2.4.3 CMOS Driver Input Stages

There are several ways to achieve compatibility between CMOS analogue switches and the more common logic families. One method is shown in Fig. 2.17 which is another circuit with differential input. An alternative method is shown in Fig. 2.25. The design and process parameters determine the logic threshold of this type of driver.

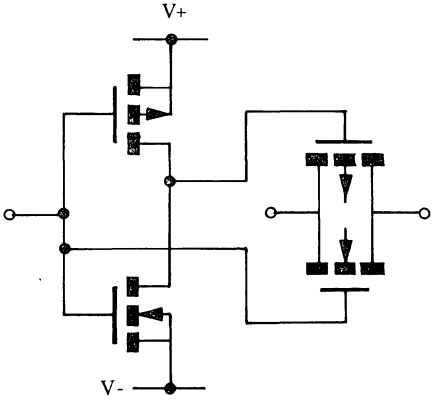


Fig. 2.25
Simple CMOS driver and switch.

2.4.4 JFET Driver Input Stages

These circuits have already been shown in Fig. 2.12 (a) and (b). They derive their logic compatibility from the $V_{GS(OFF)}$ value of the JFET chosen. The E177 type JFET is CMOS, TTL or DTL compatible.

Although the emphasis has been placed on TTL, DTL, CMOS and RTL logic family compatibility, most of the circuits shown can be made ECL compatible by adjustment of V_R and/or V_L. It should also be stressed that the same selection of drivers could be applied to control MOSFETS or JFETS.

2.5 SOME GENERAL COMMENTS ON DRIVER GATES

2.5.1 Range of Driver Gates

Table 2.1 gives a listing of some of the Standard IC analogue switches that are currently available, showing the key parameters and features of each type

Fig. 2.48.1 through to Fig. 2.48.26 show some of the combinations of standard switch functions that are available. This chart also shows that there are two categories of driver gates. The distinctions between the two categories are not always easy to define, and some devices could be classified as belonging to both categories.

The first category of devices embraces combinations of drivers and switches which are connected to give relay functions such as single-pole single-throw, (SPST) double-pole single-throw (DPST), single-pole double-throw (SPDT) or double-pole double-throw (DPDT) action. Usually in this category of switches, more than one switch in the array can be simultaneously closed.

The second category is referred to as multiplexers and there may be up to 16 switches in these arrays. These devices usually have the switch drains (or sources) commoned, and in many instances only one switch at a time in the array can be closed.

2.5.2 Break-before-make or Make-before-break Switch Action

Some applications require break-before-make switch action and some require make-before-break. Both types of switch action are available in the range of driver gates shown in Table 2.1 The former switch action is the more common requirement because in a simple multiplexing circuit as shown in Fig. 2.26, it could be damaging to the signal sources, or the switches if two largely differing voltages are connected together, with no current limiting factor other than the switch resistance.

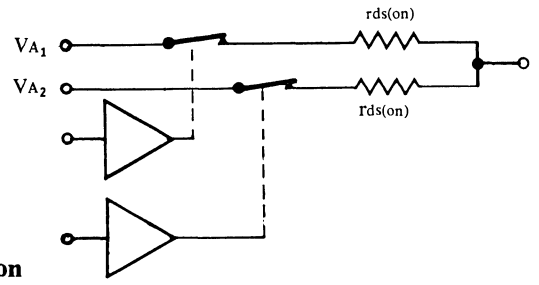


Fig. 2.26
Possible high current configuration if switching action is make-before-break.

If for example, we assume that V_{A_1} and V_{A_2} in Fig. 2.26 are +5V and -5V respectively, the switch resistances are 10 ohms, and the two switches are both closed for a small interval of time because they do not "break-before-make", then instantaneously 0.5A would flow from the +5V signal source into the -5V signal source. This level of current could be destructive for both the signal sources and the switches. Resistance placed in series with the switch would reduce the current but would also reduce output signal accuracy.

There are applications where make-before-break is essential. As an example, consider a multiplexed alarm system where several voltages have to be sampled in sequence. The alarm is triggered if any of the voltages applied are outside a pre-arranged voltage range. It is essential to use a make-before-break switch in this instance to ensure that the alarm is not falsely triggered by the absence of an input voltage for a short interval of time. Another example is the case where several signals are multiplexed into the summing node of an amplifier. Some amplifiers are unstable if the inputs are 'floating' and again make-before-break action is required.

2.5.3 Maximum Current through the Switch.

In section 2.5.2 an example was quoted where it was assumed that the resistance of the switch was constant even though the switch was conducting 0.5 ampere.

This assumption is not always valid for a FET switch. It was shown in Chapter 1 that the resistance of JFETS and MOSFETS increases as the current through the FET increases. When the FET is operating in the saturated region the drain current changes very little for substantial changes in V_{DS}. Thus, the FET switch is to some extent self protecting. It will limit its own drain and (source) current. Further, the drain current will decrease with increasing temperature as was described in section 1.9.6 which gives additional self protection.

Junction FET switches will restrict the current flow to their I_{DSS} value since V_{GS} is zero when the switch is ON. Low ON resistance JFET switches will have the highest I_{DSS} values.

Just as the ON resistance of MOSFET switches is modulated by the analogue signal voltage level, so is the drain current that flows when the drain to source voltage applied is large enough to cause the MOSFET to operate in the saturated region of its characterisitics (Ref. section 1.9.6). Whilst this feature of current limiting in FET switches has some advantage with respect to the device survival it can be a limitation in applications such as sample and hold circuits, where it may be required to charge a capacitor as rapidly as possible (see Chapter 4).

2.5.4 Power Supplies and Analogue Signal Range

The manufacturers specifications for many driver gates stipulate the supply voltages and analogue signal for which the performance characteristics are guaranteed. In general, these specifications are based on the assumption that the analogue signal voltage is required to swing about earth potential. However, IC analogue switches are not necessarily confined to operate within the specified signal range. If the analogue signal voltages diverge from those given in the standard specification, then it is frequently possible, by adjustment of the power supply voltages, to cater for these various signal requirements. Under these circumstances, it is recommended that the user should discuss his application with the analogue switch vendor to ensure that no maximum ratings are exceeded or safe operating condition contravened. As an example, the DG181 whose driver circuit is similar to that of Fig. 2.16 is specified to handle a ±7.5V signal when operating from V+ = +15V, V- = -15V, V_L = 5V and V_R = 0. If the DG181 were required to handle a -7.5V to +15V analogue signal, it could cater for this without even changing the supplies. If the analogue signal range were 0 to 25V, then this could be handled by changing V+ to 25V and V- to -7.5V, keeping

V_L = 5V and V_R = 0V. The choice of these supply voltage values satisfies equation 2.13 and does not contravene any of the device maximum ratings.

2.5.5 Power Consumption

The power consumption of most FET driver circuits is low and is rarely a factor that causes any concern except possibly when used in portable equipment. The maximum driver power consumption for the fast DG181 series is 120mW, whereas for the DG506 16-channel multiplexer the total power consumption is 300mW max. Devices like the 5-channel DG125 only consume 600μW when all the switches are OFF and 160mW with any one channel ON. Some CMOS circuits consume negligible power 5μW in the quiescent state but the consumption does increase rapidly as the switching frequency increases. The power dissipated in the switch is likely to exceed the driver power consumption. Low resistance switches used in conjunction with low load and analogue signal generator resistances can dissipate a significant amount of power and care should be taken not to exceed the maximum package power rating. As an example, the arrangement given in Fig. 2.27 shows that if V_{A_1} through V_{A_4} are a.c. signals of 7Vr.m.s., and the generators have zero internal resistance, then each switch will conduct a current of

$$\frac{7V}{60\,\text{ohm}} = 0{\cdot}117A$$

Total power dissipated in the switches will be $4(0.117)^2$ (10) = 0.544W. This dissipation could be beyond the capability of some packages in high ambient temperatures. In practice, if large voltages appear across the switch, the current will be limited to the I_{DSS} value of the FET switch. Hence, at the peaks of 7V a.c. signal, the FET will be operating in the saturation region of the V_{DS}/I_D characteristic.

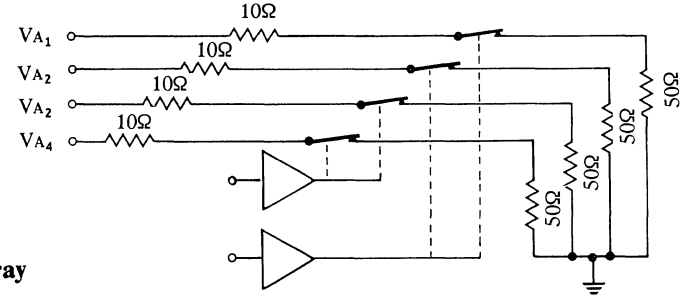


Fig. 2.27
Multiswitch array

2.5.6 Resistance matching

The resistance of monolithic analogue switches within a package will usually be matched to better than ±10%. However, there will be a greater spread on multichip switch arrays, typically 20%.

2.5.7 **Switch Noise**—In the ON state the switch noise will be the equivalent resistor noise given by $\bar{e}_n = \sqrt{4kTBR}$ volts where k is Boltzmann's constant, T the Absolute temperature, B the noise bandwidth and R the resistor. Thus a 50 ohm switch will contribute 0.9nV/$\sqrt{\text{Hz}}$. This will be discussed further in Chapter 3.

2.6 SOURCES OF ERROR

Since FETs are good switches, the errors that they introduce are quite small. The sources of these errors will now be investigated in order to understand the problems that could occur and hence enable a solution to be implemented, if necessary. The errors can be divided into two groups.

a) Low frequency or d.c. errors due to leakage currents and switch resistance.

b) High frequency errors due to device and stray capacitances.

2.6.1 Low Frequency Errors

2.6.1.1 Leakage Errors in the OFF state

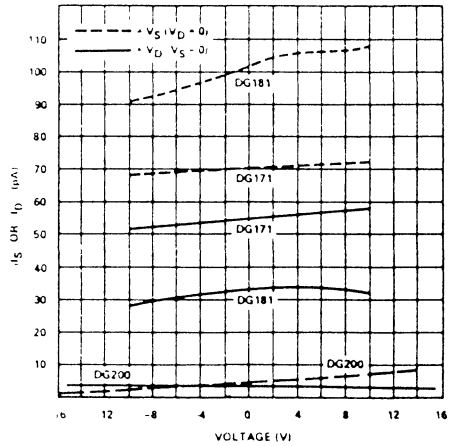


Fig. 2.28a
Leakage current values for different Siliconix analogue switches.

The graph in Fig. 2.28a gives the typical leakages for several Siliconix analogue switch device types. It shows that the typical leakages are substantially less than the maximum values quoted on data sheets. The maximum values of leakage currents quoted on data sheets are largely dictated by the limitations in automatic integrated circuit test equipment measurement capability and not by the device performance. Only for the DG181 family of devices is the source OFF leakage consistently higher than the drain leakage as was described in section 2.37. The drain terminals of devices such as the DG171 will of course have higher leakage than the source, because several drains are commoned.

As was seen in chapter 1, the main components of leakage currents in JFETs are gate-to-source or gate-to-drain leakage, there is very little leakage from source to drain or vice versa when the JFET is OFF. For a MOSFET in the OFF state, again the source to drain leakage current is extremely small. The leakage currents flow mainly from body to source or body to drain and not through the switch.

The equation defining leakage across a silicon p-n junction is

$$I = I_0\left[\exp\left(\frac{eVj}{kT}\right) - 1\right]$$

where e = electron charge, Vj = voltage across the junction, k = Boltzmann's constant, T = Absolute temperature, I_0 = reverse saturation current.

However, this equation is not always applicable when considering FETs under bias conditions because the bias voltage changes the effective junction areas and hence I_0. Additionally, package leakages must be taken into account. An adequate approximation for the relationship between junction leakage and junction voltage is that the leakage is proportional to the square root of the voltage.

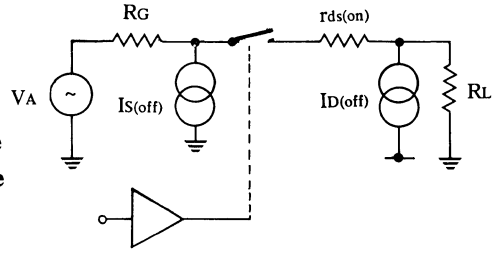


Fig. 2.28b **Driver-gate circuit in the OFF state**

The effect of OFF leakage can be assessed by considering a driver gate in the OFF state, having its source and drain connected as in Fig. 2.28b. The error voltage seen at the load due to switch leakage will be ($I_{D(OFF)}$ x R_L), and if R_L is 1.0kohm and $I_{D(OFF)}$ is 1nA, the error voltage at the load will be 1μV. The error at the input to the switch is $I_{S(OFF)}$ x R_G which is 50nV for a generator resistance of 50ohm.

2.6.1.2 Leakage Errors in the ON state

In the ON state there will be leakage current flowing from the switch channel into either the driver circuit if the switch is a JFET, or into the body if the switch is a MOSFET, see Fig. 2.29.

The maximum data sheet values for $I_{S(ON)}$ are usually in the 1 to 5nA region. Typical values are much less than this, but as was stated earlier, automatic integrated circuit test equipment limitations have in the past dictated the limit that could be specified.

Since the current I flowing through the switch into the load is given by

$$I = \frac{V_A}{(Rgen + r_{DS} + R_L)} \qquad \text{eqn 2.15}$$

Then, if we substitute some typical values such as V_A = 10V, Rgen = 50 ohm, r_{DS} = 100 ohm, R_L = 1k ohm into equation 2.15, we have

$$I = \frac{10}{1{,}150} = 8.7\text{mA}$$

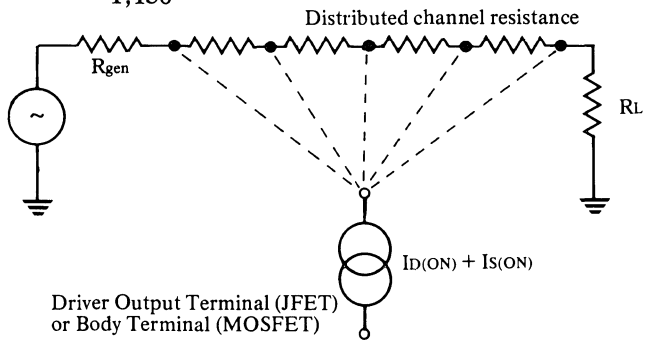


Fig. 2.29 **Distributed leakage from the channel**

consequently the $I_{D(ON)} + I_{S(ON)}$ of 1nA maximum bled from the signal path is usually insignificant compared to the analogue current (0.0000115%). If the input signal voltage is 0V then the error voltage due to $I_{D(ON)} + I_{S(ON)}$ is again the product of ($I_{D(ON)} + I_{S(ON)}$) and the parellel resistance of the load R_L and generator Rgen. This error is less than 0.15μV, if we use the same values as in the above example.

2.6.1.3 Resistance Errors in the ON state

The switch resistance is in series with the load and therefore causes some attenuation of the analogue signal. This can be a significant source of error if the load resistance is less than 100kohms (Fig. 2.30).

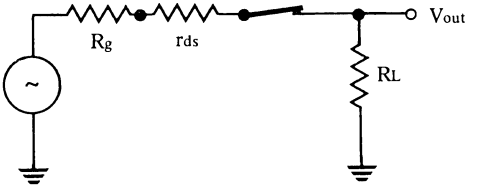


Fig. 2.30
Circuit showing possible error in output voltage due to switch resistance.

Referring to Fig. 2.30, $V_{out} = \frac{R_L . V_A}{r_{DS} + R_L + R_g}$ eqn. 2.16

If we substitute the values used in the previous example:

$$V_{out} = \frac{1000\ V_A}{1150} \qquad \text{i.e. an 8.7\% error}$$

or if R_L = 100kohm, then $V_{out} = \frac{100{,}000\ V_A}{100{,}150}$ i.e. a 0.15% error

With a JFET switch the rds = $r_{DS(on)}$ and is constant. The error due to $r_{DS(on)}$ can sometimes be compensated for in the succeeding amplifier stages. The rds of a MOSFET will vary according to the effective V_{GS} generated by the analogue signal level (Ref. section 2.2.2 of this chapter). Therefore, distortion as well as attentuation of the analogue signal can occur. As a typical example, the r_{DS} of the MOS switch could be 70 ohms at a V_A of + 10V, and 200 ohms at a V_A of -10V. Consequently, the change in signal attenuation over the ±10V range is from

$$\frac{(200\Omega)}{(R_L + 200\Omega)} \quad \text{to} \quad \frac{(70\Omega)}{(R_L + 70\Omega)}$$

If R_L is large in comparison with $r_{DS(on)}$, the effect of the r_{DS} variation is small. The effects of low frequency errors will be discussed further in relationship to particular application.

2.6.2 High Frequency Errors

2.6.2.1 Channel Resistance Modulation by High Frequency Analogue Signals

It has already been shown (section 2.3 of this chapter) when reviewing the various driver circuits that there can be modulation of switch resistance due to modulation of V_{GS} by high frequency analogue signals under certain circumstances. To eliminate this type of r_{DS} modulation it is essential to satisfy the following conditions for the switch:

JFET SWITCH. If the JFET is to be kept ON by the method of connecting a resistor between gate and source, the value of the resistor should be as low as possible. If the reversed biased diode leakage method is used, the capacitances between gate and a.c. ground must be much less than Cdg + Csg.

MOSFET SWITCH. The gate should be connected to the appropriate (positive for NMOS, negative for PMOS) supply rail through as low a resistance as possible when the FET is ON. To prevent the MOSFET turning ON when it should be in the OFF state, the gate should be connected to the appropriate supply voltage rail or source terminal through as low a resistance as possible (positive supply rail for PMOS, negative supply rail for NMOS).

2.6.2.2 High Frequency OFF Isolation

The high frequency equivalent circuits of the JFET and MOSFET in the OFF state are given in Fig. 2.31a and Fig. 2.31b, respectively.

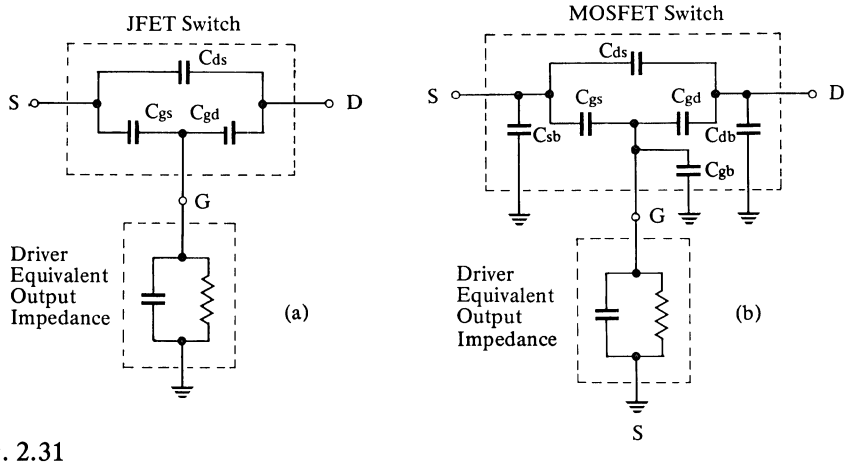


Fig. 2.31
JFET and MOSFET switch and driver high frequency equivalent circuit.

Since a typical value for Cds is 0.1pF whereas Cgs and Cgd are usually at least an order of magnitude higher, it is apparent that if the gate were left floating the majority of the signal feed-through from source to drain would be via Cgs and Cgd. Therefore, if the drain-to-source OFF isolation at high frequency is to be maximised, the driver circuit should present as low a resistance* as possible to a.c. ground so that any signal coming via Cgs will be shunted to ground. The only other component contributing to feed through would then be Cds and printed circuit board strays.

Csb and Cdb for the MOSFET are effectively in parallel with the generator and load resistance respectively and can be lumped with these impedances. Cgb is in parallel with the driver output capacitance and therefore they also can be lumped together. The equivalent circuit for both types of FET can be presented on an impedance basis (Fig. 2.32). To make the calculations more tractable, the gate-to-source and gate-to-drain impedances are assumed to be equal, which is a

*Low impedance to ground by using shunt capacitance would not be satisfactory since it would cause modulation of V_{GS} as described earlier.

reasonable approximation for switching FETS. Calculations based on a symmetrical gate source and gate drain impedances show very little divergence, unless the gate to source or gate to drain capacitances differ by more than 20%.

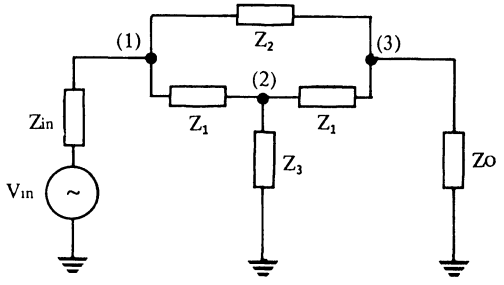


Fig. 2.32
Equivalent circuit in the OFF state

If we now apply nodal analysis and matrices to the network of Fig. 2.32, then

$$\begin{bmatrix} V_{in}\,Y_{in} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} \begin{bmatrix} (Y_{in}+Y_1+Y_2) & Y_1 & Y_2 \\ Y_1 & (2Y_1+Y_3) & Y_1 \\ Y_2 & Y_1 & (Y_1+Y_2+Y_0) \end{bmatrix} \quad \text{eqn. 2.17}$$

where V_1, V_2 and V_3 are the voltages at the corresponding nodes 1, 2 and 3. Y_1, Y_2, Y_3 etc. are the admittances of the impedances Z_1, Z_2, Z_3 etc.

Then using Cramer's Rule

$$V_3 = V_{in}\,Y_{in}\,\frac{\Delta_{13}}{\Delta_Y} \qquad \text{eqn. 2.18}$$

where Δ_{13} is the minor of the determinant Δ_Y.

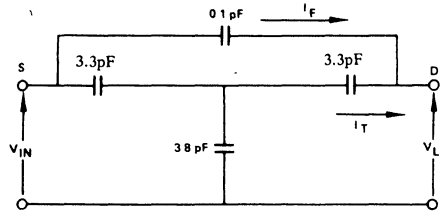
Then expanding the determinants

$$\frac{V_3}{V_{in}} = \frac{Y_{in}\,[Y_1^2 - Y_2\,(2Y_1+Y_3)]}{(Y_{in}+Y_1+Y_2)\,[(2Y_1+Y_3)(Y_1+Y_2+Y_0)-Y_1^2]} \qquad \text{eqn. 2.19}$$
$$-Y_1\,[Y_1\,(Y_1+Y_2+Y_0) - Y_1\,Y_2] + Y_2\,[Y_1^2 - Y_2\,(2Y_1+Y_3)]$$

$$\text{or} \quad \frac{V_3}{V_{in}} = \frac{Y_{in}\,[Y_1^2 - 2Y_1Y_2 - Y_2Y_3]}{4Y_1^2Y_2 + Y_1^2Y_0 + Y_1^2Y_3 + 2Y_1Y_2Y_3} \qquad \text{eqn. 2.20}$$
$$+Y_0Y_1Y_3 + 2Y_0Y_1Y_2 + Y_0Y_2Y_3$$
$$+Y_{in}Y_1^2 + 2Y_{in}Y_1Y_2 + 2Y_{in}Y_1Y_0$$
$$+Y_{in}Y_3Y_1 + Y_{in}Y_3Y_2 + Y_{in}Y_3Y_0$$

If we now substitute the relevant admittance values given in the equivalent circuits of the driver gates Figs. 2.33, 2.34, 2.35 and 2.36, we can calculate the isolation at any frequency.* The equivalent circuits of four common types of Siliconix analogue switches are shown. The isolation for these four circuits has been calculated and a comparison of measured and calculated results are shown in the graphs of Figs. 2.33, 2.34, 2.35, 2.36.

*Equation 2.20 simplifies considerably when these values are substituted, because numerous terms become negligible. It is further simplified if $Y_{in} = Y_{out}$.



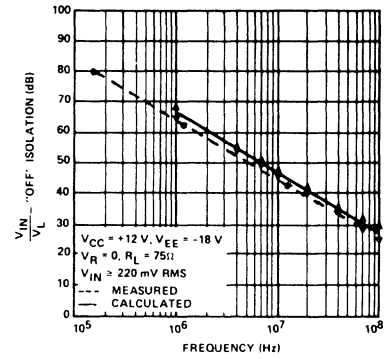
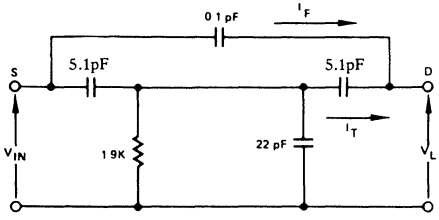


Fig. 2.33
DG133 Equivalent circuit and OFF isolation data



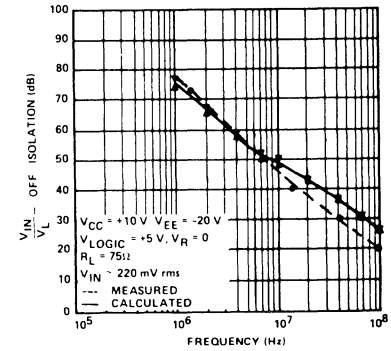
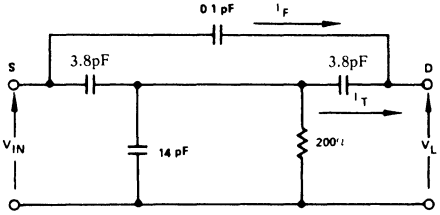


Fig. 2.34
DG171 Equivalent circuit and OFF isolation data



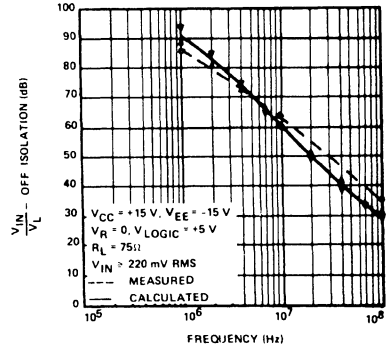


Fig. 2.35
DG181 Equivalent circuit and OFF isolation data

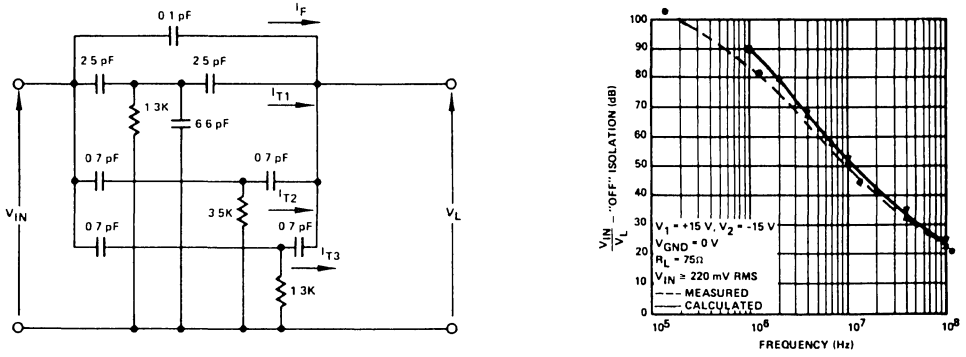


Fig. 3.36
DG200 Equivalent circuit and OFF isolation data

CHAPTER 2

2.6.2.3 Improving Isolation

If the OFF isolation of a single analogue switch is not adequate, it can be considerably increased by using series-shunt arrangements as shown in Fig. 2.37a. Switches A and B are driven in antiphase. When switch A is closed, B is open, and therefore B has little effect on the circuit. When A is open and B is closed, the output of A is now connected to ground potential via the switch B, so the two switches contribute to increase the attenuation.

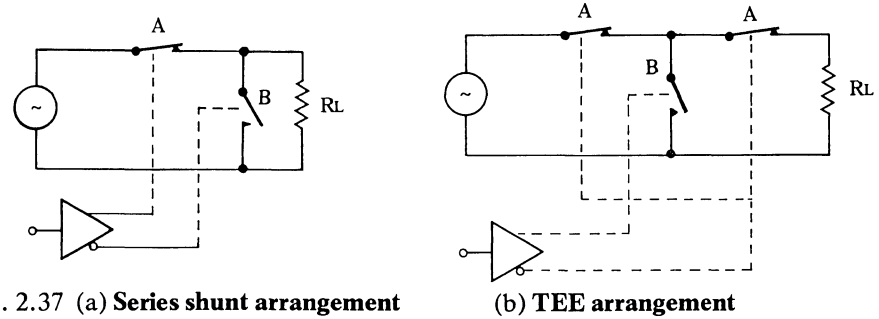


Fig. 2.37 (a) **Series shunt arrangement** (b) **TEE arrangement**

In some applications wherein RL must not be shunted, the arrangement shown in Fig. 2.37a cannot be used. The TEE arrangement of Fig. 2.37b achieves the improved isolation at the expense of increased switch series resistance. The isolation of these configurations is considered further in Chapter 3.

To maximise high frequency OFF isolation there are two points that cannot be overstressed

1. THE TOTAL CAPACITANCE BETWEEN THE DRAIN AND SOURCE TERMINALS OF THE SWITCH MUST BE MINIMISED. THE STRAY CAPACITANCES OF THE P.C. BOARD AND PACKAGE LEADS ARE IN PARALLEL WITH THE INTRINSIC DRAIN SOURCE CAPACITANCES OF THE FET SWITCH Cds. SINCE Cds IS SMALL, USUALLY LESS THAN 0.1pF, STRAY CAPACITANCES CAN CAUSE DRASTIC DETERIORATION OF HIGH FREQUENCY ISOLATION PERFORMANCE.

2. IN THE OFF STATE, THE GATE OF THE FET SWITCH SHOULD BE CONNECTED TO a.c. GROUND THROUGH AS LOW A RESISTANCE AS POSSIBLE TO ATTENUATE ANY SIGNAL FED TO THE OUTPUT THROUGH Cgs AND Cgd.

2.6.3 Charge Coupling

The voltage transitions that occur at the gate of a FET switch when it is turned ON or OFF are coupled into the analogue signal path via Cgs and Cgd and will appear as voltage spikes at the input and output of the switch.

The transient at the input is usually very small if the analogue signal source resistance is small and does not contribute any significant error to the switch performance. The transient at the output of the switch, however, can be detrimental to the system performance and will therefore be analysed. The equivalent circuits for the JFET switch in the ON and OFF states are shown in Figs. 2.38a and 2.38b. The same circuit can in fact be used for the MOSFET switch when considering these transients. Referring to Fig. 2.38c one can see that the drain-to-body capacitance can be lumped with the load capacitance. The source-to-body capacitance is connected across a low resistance voltage signal source and can therefore be ignored. Hence, Figs. 2.38c and 2.38d for the MOSFET can be simplified to Figs. 2.38a and 2.38b.

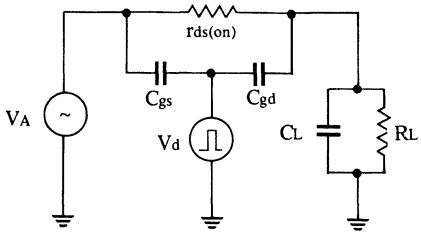


Fig. 2.38a
Equivalent circuit of JFET in the ON state

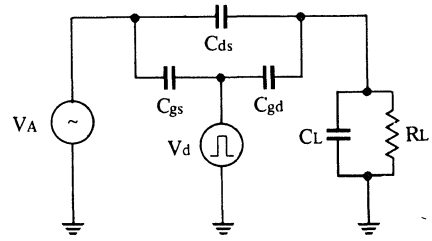


Fig. 2.38b
Equivalent circuit of JFET in the OFF state

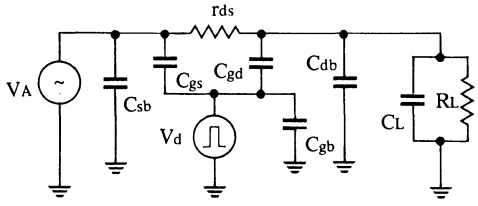


Fig. 2.38c
Equivalent circuit of MOSFET in the ON state

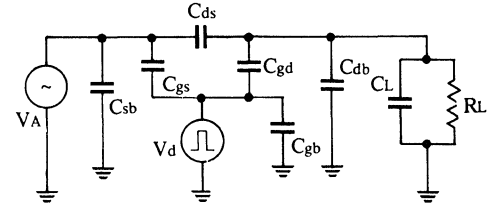


Fig. 2.38d
Equivalent circuit of MOSFET in the OFF state

The magnitude of the voltage spike at the load is dependent on numerous factors:

(a) The amplitude of the driver output voltage transition (Vd)
(b) The driver output voltage transition speed.
(c) The gate to drain and/or gate to source capacitances.

(d) The load impedance.
(e) The analogue generator impedance.
(f) Gate driver impedance.

It is extremely cumbersome to derive the exact expression for the signal seen at the load when the FET is switched. The expression is cumbersome because (a) the driver output voltage transition is complex—it is not a simple step or ramp, (b) the FET capacitances are a function of the junction bias voltages (see Chapter 1.) and (c) the FET resistance is a function of the gate to channel voltage. However, it is possible to get a very good approximation of the feedthrough transient by making some assumptions as shown in the following transient analysis. The same analysis can be applied to both the JFET and MOSFET switch. The only difference is that p- channel MOSFET switches will have a positive transition when going from ON to OFF whilst the n- channel JFET will have a negative transition and vice versa.

2.6.3.1 Turn OFF Case Analysis

We will assume that the driver output voltage is a ramp function for a defined period of time, reaching a constant value after time = τ as shown in Fig. 2.39.

$$\therefore V_d(t) = at \quad \text{for } 0 < t < \tau \qquad \text{eqn. 2.21a}$$

$$V_d(t) = at - a(t-\tau) \quad \text{for } t > \tau \qquad \text{eqn. 2.21b}$$

where 'a' is the ramp voltage slope, and τ is the duration of the ramp voltage. This function can be built up of two continuous ramps of equal and opposite slope, one starting at a time t=0 and the other at time t=τ. Thus, using the Shift theorem, we can write the Laplace Transform for this function as

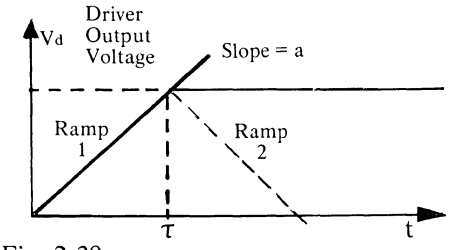


Fig. 2.39
Simplified driver output voltage vs. time

$$V_D(s) = \frac{a(1-e^{-\tau s})}{s^2} \qquad \text{eqn. 2.22}$$

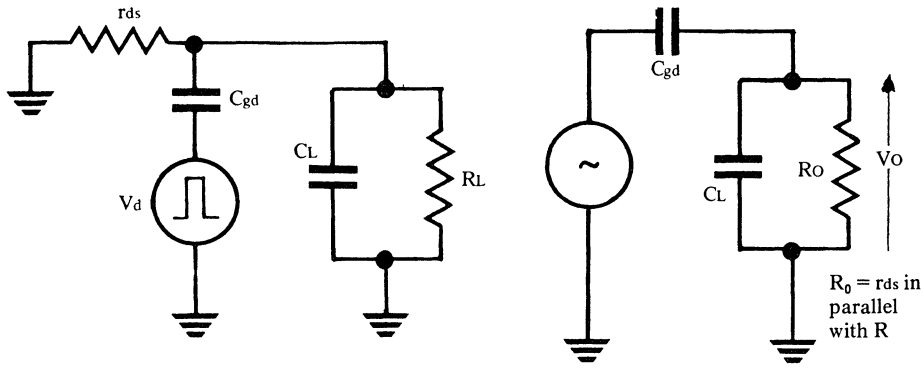
where s is the complex variable.

Figs. 2.38a and 2.38b show that if the analogue signal has zero source impedance, we can neglect Cgs because it contributes nothing to the output transient.

Since this analysis is only concerned with the transient due to the driver voltage, then using the superposition theorem we can eliminate V_A. The equivalent circuit of Fig. 2.38a can be redrawn as shown in Fig. 2.40a which reduces to Fig. 2.40b wherein Ro is the parallel resistance of R_L and r_{DS}. The transfer function for this circuit Fig. 2.40b expressed in complex impedance form is then :

Fig. 2.40

(a) **Simplified arrangement of Fig. 2.38a** (b) **Equivalent circuit of Fig. 2.40a**



$$\frac{Vo\,(j\omega)}{V_D\,(j\omega)} = \frac{\left(\dfrac{Ro\ \dfrac{1}{j\omega C_L}}{Ro+\dfrac{1}{j\omega C_L}}\right)}{\left(\dfrac{Ro\ \dfrac{1}{j\omega C_L}}{Ro+\dfrac{1}{j\omega C_L}}\right)+\dfrac{1}{j\omega Cgd}} \qquad \text{eqn. 2.23}$$

where ω is the angular frequency and $j = \sqrt{-1}$

$$\text{or}\quad \frac{Vo\,(j\omega)}{V_D\,(j\omega)} = \left(\frac{Cgd}{Cgd + C_L}\right)\frac{j\omega}{j\omega + \dfrac{1}{Ro(Cgd + C_L)}} \qquad \text{eqn. 2.24}$$

or in operational form

$$\frac{Vo(s)}{Vd(s)} = \left(\frac{Cgd}{Cgd + C_L}\right)\frac{s}{s + \dfrac{1}{Ro\,(Cgd + C_L)}} \qquad \text{eqn. 2.25}$$

We have already derived $V_D(s)$ in eqn 2.22 therefore if we substitute into eqn. 2.25

$$Vo(s) = \frac{Cgd}{Cgd + C_L} \cdot \frac{s}{s + \dfrac{1}{Ro(Cgd + C_L)}} \cdot \frac{a\,(1-e^{-\tau s})}{s^2} \qquad \text{eqn. 2.26}$$

which can be rewritten as

$$Vo(s) = \frac{a\,Cgs}{(Cgs + C_L)}\left\{\left[\frac{1}{s + \dfrac{1}{Ro\,(Cgs + C_L)}}\right]\left[\frac{1}{s}\right] - \left[\frac{e^{-\tau s}}{s + \dfrac{1}{Ro(Cgs + C_L)}}\right]\left[\frac{1}{s}\right]\right\}$$

If we now take the inverse Laplace Transform

$$Vo(t) = \mathcal{L}^{-1}Vo(s) = aR_0Cgs\left\{\left[1 - \exp\left(\frac{-t}{R_0(Cgs + C_L)}\right)\right] r(t) - \left[1 - \exp\left(\frac{-(t-\tau)}{R_0(Cgs + R_L)}\right)\right] r(t-\tau)\right\} \qquad \text{eqn. 2.27}$$

The term a.Ro.Cgs defines the aiming voltage and the terms in brackets define the decay rates. It should be stressed that the aiming voltage cannot change after the ramp ends.

The term r(t) is intended to represent the presence of the ramp function starting at t=0. The value of r(t) is unity for t>0. The term r(t-τ) represents the equal and opposite ramp function. It has zero value for t<τ and is unity for t>τ.

Throughout the preceding analysis Ro was treated as a constant. In practice this is not true. The switch resistance changes during the transition from possibly less than 50 ohms up to several Megohms. If we inserted r_{DS} as a function of time into the original equation then we would have an extremely cumbersome equation for which there is no exact mathematical solution. It would be necessary to use successive approximation techniques to arrive at an answer. However, this can be by-passed without significant error if we bear in mind that almost all FETs have turn OFF delays ranging from 5 to 30ns depending on the device size. Therefore we can assume that the FET resistance is relatively low for this period of time after the pinch-off voltage has been exceeded. The FET resistance changes rapidly after the initial delay since a depletion layer takes very little time to form, provided adequate current is available to charge the junction capacitance *(Ref. 2.4)*. Therefore, we can assume that the FET resistance will be high within a few nanoseconds after the FET turn OFF delay period td(off), provided the input ramp rate is sufficiently rapid for the gate-to-source voltage to have traversed the voltage range required to turn the FET off, i.e. Ro = R_L after time t_1, where t_1 = td(off). If the driver output ramp rate is not sufficiently fast to traverse this turn off voltage range $V_{GS(OFF)}$ within the turn OFF delay period td(off), then the transient at the output will only be significant after the switch has turned off, because the load capacitance will be discharged by the r_{DS} up until some time t_2, where $t_2 = \frac{V_{GS(off)}}{a}$.

As an example, let us consider the transient analysis of a device like the Siliconix DG181. On the data sheet there is a test configuration given for measuring the transients associated with switching. This is reproduced in Fig. 2.41. The following values are applicable for this circuit:

Va=0V, $r_{DS(on)}$ = 30ohms, R_L = 10kohms, C_L = 10pF, Cgd = 3.0pF under reverse bias of 20V, td(off) = 20ns, Vp = 5V.

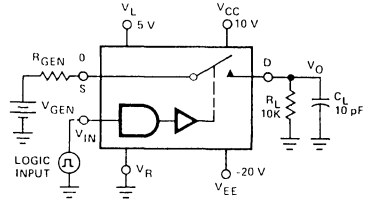


Fig. 2.41
Test configuration for transient measurement

The driver output waveform for this device is not a simple ramp but approximates to three ramps on both the rising and falling edges, as shown in Fig. 2.42a and 2.42b. We can still apply equation 2.27 to each of these six ramps and get the resultant output voltage from the sum of the corresponding output voltages.

For the falling edge, ramp 1 starts at time t=0 and ends at time t=35ns. Ramp 2 starts at time t=35ns and ends at time t=(35+40)ns. Ramp 3 starts at time

t=(35+40)ns and ends at t=(35+40+55)ns. The output voltage corresponding to ramps 1, 2 and 3 will be V_{01}, V_{02} and V_{03} respectively.

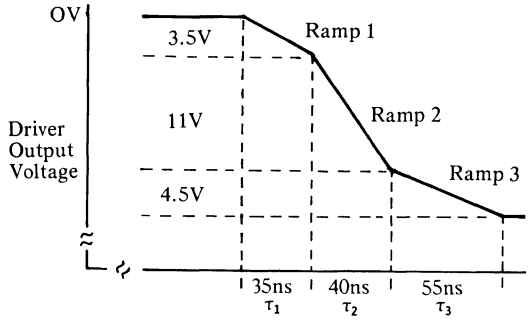


Fig. 2.42a
Falling edge of driver output

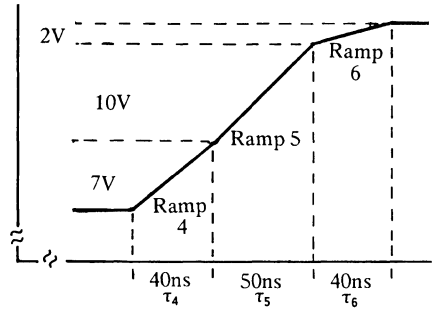


Fig. 2.42b
Rising edge of driver input

Referring to Fig. 2.42a the V_{GS} applied to the FET switch will be equal to the $V_{GS(OFF)}$ of 5V at a time t_x given by

$$t_x = \left(35ns + 1.5V \times \frac{40ns}{11V}\right) \approx 40.5\ ns$$

and the FET switch will be in the high resistance state after a time

$$t_{off} = t_x + td(off)$$
$$\therefore t_{off} = 40.5ns + 20ns = 60.5\ ns$$

The output voltage resulting from the three ramp voltages that approximate to the gate transition can now be calculated from equation 2.27.

Ramp 1

at t = 0 $\qquad V_{01} = 0.00V$

at t = 35ns the switch resistance is low and

$$V_{01} = \frac{3.5}{35} \cdot \frac{30 \times 3.0}{10^3}\left[1 - \exp\left(\frac{-35 \times 10^3}{30 \times 13.0}\right)\right]$$
$$= 0.01V$$

at t = 60ns the switch resistance is still low

$$V_{01} = \frac{3.5}{35} \cdot \frac{30 \times 3.0}{10^3}\left[1 - \exp\left(\frac{-60 \times 10^3}{30 \times 13.0}\right)\right]$$
$$= 0.01V$$

at t = 80ns the switch resistance is high and the rate of decay of the transient caused by ramp 1 will be slowed down. The aiming voltage cannot change after τ_1, for ramp 1, therefore :

$$V_{01} = \frac{3.5}{35} \cdot \frac{30 \times 3.0}{10^3}\left\{\left[1 - \exp\left(\frac{-80 \times 10^3}{10^4 \times 13.0}\right)\right] - \left[1 - \exp\left(\frac{-45 \times 10^3}{10^4 \times 13.0}\right)\right]\right\}$$
$$= 0.00V$$

Thus, the peak transient due to ramp 1 is negligible. This is intuitively obvious since the switch is in the low resistance state during the total transition of ramp 1.

Ramp 2

at t = 35ns, ramp 2 is just commencing, so that values of time pertaining to this ramp have to be delayed by 35ns when substituted in equation 2.27.

at t = 35ns

$$V_{02} = 0$$

at t = 60ns, the switch resistance is still low and

$$V_{02} = \frac{11}{40} \times \frac{30 \times 3.0}{10^3}\left[1 - \exp\left(\frac{-(60-35) \times 10^3}{30 \times 13}\right)\right]$$

$$= 0.02V$$

at t = 70ns, the switch resistance is high, and

$$V_{02} = \frac{11}{40} \times \frac{10^4 \times 3.0}{10^3}\left[1 - \exp\left(\frac{-(70-35) \times 10^3}{10^4 \times 13}\right)\right]$$

$$= 8.25\,(1-0.764) = 1.95V$$

at t = 100ns

$$V_{02} = \frac{11}{40} \times \frac{10^4 \times 3.0}{10^3}\left\{\left[1 - \exp\left(\frac{-(100-35) \times 10^3}{10^4 \times 13}\right)\right] - \left[1 - \exp\left(\frac{-(100-35-40) \times 10^3}{10^4 \times 13}\right)\right]\right\}$$

$$= 8.25\,(0.825 - 0.606) = 1.80V$$

at t = 125ns

$$V_{02} = 8.25\,(0.681 - 0.500) = 1.49V$$

at t = 150ns

$$V_{02} = 8.25\left\{\left[1 - \exp\left(\frac{-(150-35) \times 10^3}{10^4 \times 13}\right)\right] - \left[1 - \exp\left(\frac{-(150-35-40) \times 10^3}{10^4 \times 13}\right)\right]\right\}$$

$$= 8.25\,(0.562 - 0.412) = 1.23V$$

at t = 200ns

$$V_{02} = 8.25\,(0.3823 - 0.281) = 0.835$$

Ramp 3

at t = 75ns, ramp 3 is commencing so that all values of time substituted in the equation pertaining to this ramp will have to be delayed by 75ns.

at t = 75ns

$$V_{03} = 0$$

at t = 100ns

$$V_{03} = \frac{4.5}{55} \times \frac{10^4 \times 3}{10^3}\left[1 - \exp\left(\frac{-(100-75)\times 10^3}{10^4 \times 13}\right)\right]$$

$$= 2.45\,(1-0.825) = 0.43V$$

at t = 125ns

$$V_{03} = 2.45\left[1 - \exp\left(\frac{-(125-75)\times 10^3}{10^4 \times 13}\right)\right] = 2.45\,(1-0.681) = 0.78V$$

at t = 150ns

$$V_{03} = 2.45\left\{\left[1 - \exp\left(\frac{-(150-75)\times 10^3}{10^4 \times 13}\right)\right] - \left[1 - \exp\left(\frac{-(150-75-55)\times 10^3}{10^4 \times 13}\right)\right]\right\}$$

$$= 2.45\,(0.857 - 0.562) = 0.72V$$

at t = 200 ns

$$V_{03} = 2.45\,(0.583 - 0.3823) = 0.49V$$

Thus, up to a time t = 60ns the total output transient is very small (less than 30mV). However, after the switch resistance has changed state the transients become more significant.

at t = 60ns	$V_{01}+V_{02}+V_{03} = 0.03V$
at t = 70ns	$V_{01}+V_{02}+V_{03} = 1.95V$
at t = 100ns	$V_{01}+V_{02}+V_{03} = 2.23V$
at t = 125ns	$V_{01}+V_{92}+V_{93} = 2.27V$
at t = 150ns	$V_{01}+V_{02}+V_{03} = 1.95V$
at t = 200ns	$V_{01}+V_{02}+V_{03} = 1.33V$

These calculated figures correspond very well with measured results which exhibit a peak of 2.2V.

2.6.3.2 **Turn ON Case Analysis.**

A similar analysis can again be applied except that ramp voltages are now rising A similar analysis can again be applied except that the ramp voltages are now rising instead of falling. For the turn ON case the equivalent circuit of Fig. 2.38b still holds. The simplified equivalent circuit is then given by Fig. 2.43. Co is now Cds lumped with C_L and Ro is the parallel combination of the FET (OFF) resistance and load resistance.

Most of the transient voltage seen at the output will occur before the FET has turned ON. If the gate to source voltage of the FET is equal to the $V_{GS(OFF)}$ at a time t_y, then the FET switch will enter the low resistance state after a time

$$t_y + t_{d(on)}$$

Again, using the DG181 under the data sheet conditions as an example, we can calculate the transient at the output due to the positive driver output voltage transition. The driver waveform is shown in Fig. 2.42b, and again consists of three distinct regions designated ramp 4, 5 and 6. td(on) will be assumed to be 5ns and the other parameters will be as for the turn OFF case.

Ro = R_L until a time t_z, given by $[t_y + t_{d(on)}]$. Referring to Fig. 2.42b, it is seen that

$$t_y = \left(40ns + 7V.\frac{50ns}{10V}\right) = 75ns$$

$$\therefore t_z = 75 + 5ns = 80ns.$$

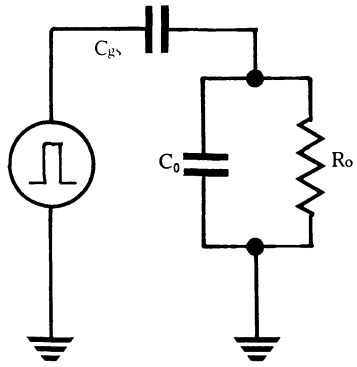


Fig. 2.43
Simplified equivalent circuit for switch and driver

Using equation 2.27 again and the same technique as used in the turn ON case,

Ramp 4

at $t = 0$ $V_{04} = 0$

at $t = 10ns$

$$V_{04} = \frac{7}{40} \times \frac{10^4 \times 3}{10^3}\left[1 - \exp\left(\frac{-10 \times 10^{-9}}{10^4 \times 13 \times 10^{-12}}\right)\right]$$

$$= 5.25\,(1 - 0.9259) = 0.388V$$

at $t = 20ns$

$$V_{04} = 5.25\left[1 - \exp\left(\frac{-20 \times 10^{-9}}{10^4 \times 13 \times 10^{-12}}\right)\right] = 0.748V$$

at $t = 40ns$

$$V_{04} = 5.25\left[1 - \exp\left(\frac{-40 \times 10^{-9}}{10^4 \times 13 \times 10^{-12}}\right)\right] = 1{\cdot}39V$$

at $t = 60ns$

$$V_{04} = 5.25\left\{\left[1 - \exp\left(\frac{-60 \times 10^{-9}}{10^4 \times 13 \times 10^{-12}}\right)\right] - \left[1 - \exp\left(\frac{-20 \times 10^{-9}}{10^4 \times 13 \times 10^{-12}}\right)\right]\right\} = 1.19V$$

at $t = 80ns$

$$V_{04} = 5.25\left\{\left[1 - \exp\left(\frac{-80 \times 10^{-9}}{40 \times 13 \times 10^{-12}}\right)\right] - \left[1 - \exp\left(\frac{-40 \times 10^{-9}}{30 \times 13 \times 10^{-12}}\right)\right]\right\} = 0.00V$$

at $t = 100ns$

$$V_{04} = 5.25\left\{\left[1 - \exp\left(\frac{-100 \times 10^{-9}}{30 \times 13\ 10^{-12}}\right)\right] - \left[1 - \exp\left(\frac{-60 \times 10^{-9}}{30 \times 13 \times 10^{-12}}\right)\right]\right\} = 0.00V$$

Ramp 5

at t = 40ns $V_{05} = 0.00V$

at t = 60ns

$$V_{05} = \frac{10}{50} \times \frac{10^4 \times 3}{10^3} \left[1 - \exp\left(\frac{-(60-40) \times 10^{-9}}{10^4 \times 13 \times 10^{-12}}\right)\right] = 0.86V$$

at t = 80ns

$$V_{05} = \frac{10}{50} \times \frac{30 \times 3}{10^3} \left[1 - \exp\left(\frac{-(80-40) \times 10^{-9}}{30 \times 13 \times 10^{-12}}\right)\right] = 0.02V$$

at t = 100ns

$$V_{05} = \frac{10}{50} \times \frac{10^4 \times 3}{10^3} \left\{\left[1 - \exp\left(\frac{-(100-40) \times 10^{-9}}{30 \times 13 \times 10^{-12}}\right)\right] - \left[1 - \exp\left(\frac{-(100-40-50) \times 10^{-9}}{30 \times 13 \times 10^{-12}}\right)\right]\right\}$$

$$= 0.00V$$

Ramp 6

at t = 100ns

$$V_{06} = \frac{2}{40} \times \frac{30 \times 3}{10^3} \left[1 - \exp\left(\frac{-(100-90)\,10^{-9}}{30 \times 13 \times 10^{-12}}\right)\right] = 0.0045\,(1-0) = 0.0045V$$

Therefore the total output voltage transition at different times is as follows:

at t = 0	$V_{04}+V_{05}+V_{06} = 0$
at t = 10ns	$V_{04}+V_{05}+V_{06} = 0.39V$
at t = 20ns	$V_{04}+V_{05}+V_{06} = 0.75V$
at t = 40ns	$V_{04}+V_{05}+V_{06} = 1.39V$
at t = 60ns	$V_{04}+V_{05}+V_{06} = 2.05V$
at t = 80ns	$V_{04}+V_{05}+V_{06} = 0.02V$
at t = 100ns	$V_{04}+V_{05}+V_{06} = 0.01V$

This waveform again corresponds well with measurements taken on a high bandwidth scope.

Since we know the cause of the transients we can take action to reduce them e.g. reduce driver signal voltage transition range, reduce gate-to-load capacitance, minimise load resistance etc.

There are other techniques available. Basically, these consist of generating an equal and opposite transient and applying this auxiliary transient to the output, to cancel the effects of the unwanted transient. This technique is quite widely used in sample and hold applications and will be described in more detail in Chapter 4. In sample and hold circuits, it is essential to accurately balance out the charge transferred to the load capacitor. The timing of the charge transfer is not usually critical. However, in switching applications, if noise due to switching transients is to be suppressed, a signal of equal and opposite magnitude must be applied simultaneously with the offending transient.

The preceding analysis could be applied to sample and hold techniques but since the output voltage changes very little during the switch transition (if the input signal is constant) and the output load resistance can be considered infinite, then some alternative assumptions may be made which will be dealt with in Chapter 4.

The equivalent circuit could be analysed with the inclusion of a finite driver generator resistance, however this is not a practical necessity if the time constant of the driver generator resistance (Rgen) and Cgd is small in comparison with the ramp duration time. This is usually the case. Fast drivers have to have low output impedance (or high drive current capability). For example, the DG181 driver output resistance Rgen is less than 300 ohms, therefore Rgen x Cgd = 1.14ns which is short in comparison to a ramp of 20ns. This point also clearly indicates that a slower driver output ramp will tend to reduce transients.

Whilst transients can be quite large, it is the bandwidth of the circuitry following the switches that dictates the significance of the transients. If this circuitry is slow the transient will be attenuated.

2.7 NOISE IMMUNITY

This is a subject rarely referred to in discussions or specifications of driver gates. In this context, any spurious signal such as "spikes" or voltage supply variations are treated as noise signals. The magnitude and duration of the noise signal required to cause spurious operation is defined as the noise immunity.

There are three sources of noise that could cause erroneous switching.

(1) Noise on the driver input or reference voltages.
(2) Noise on the supply voltage lines.
(3) Noise on the analogue signal.

The immunity of the driver gates to these noise sources will depend on the energy content, speed and duration of the noise transients. Some noise signals can be large in voltage amplitude but low in energy and consequently are not capable of changing the switch state, but could rupture a gate oxide. To reduce the number of variables we will assume the voltage transients have unlimited current capability, which is the worst case.

2.7.1. Noise on the Driver Input or Reference Voltages

Several driver circuits are described in sections 2.3 and 2.4. The noise immunity of these circuits to transitions that are slow in comparison with the circuit's switching speed can be derived from the transfer characteristic. For example, let us look at the transfer characteristic Fig. 2.44a of the circuit Fig. 2.44b. If the input to the driver is from free collector TTL logic, for which the specifications of worst case high level is assumed to be 4.5V and worst case low level is 0.8V, we can see that the noise margin is 2.2V for the low input logic state and 1V for the high input state. These are the voltages that have to be superimposed on to the input signal to cause spurious operation. The noise immunity of the driver gate will vary slightly, depending on the threshold voltage of the MOSFET gate or the pinch off voltage of the JFET gate.

If the noise signal present at the driver input is a fast transient, the driver gate may not be capable of responding rapidly enough to this input stimulus. The low frequency noise voltage margin is not applicable in this circumstance.

Fig. 2.44a
D125 Transfer Characteristic

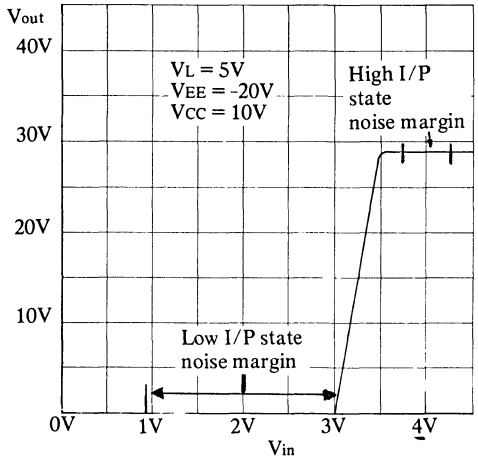
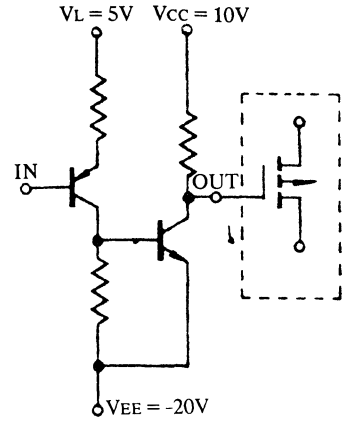


Fig. 2.44b
Single channel of D125 driver



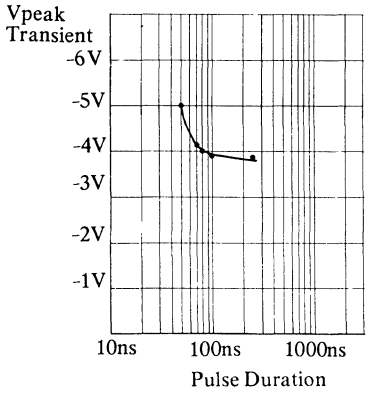
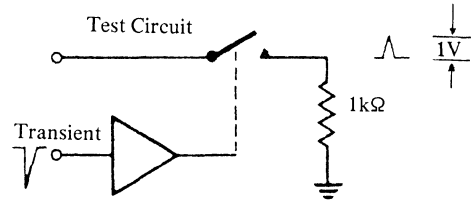


Fig. 2.45
Plot of Pulse Duration vs. Negative Transient on 5V Supply (VL) to turn DG184 switch ON



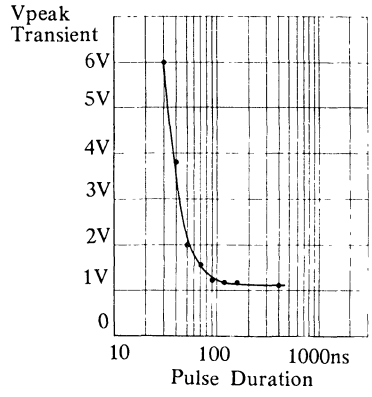
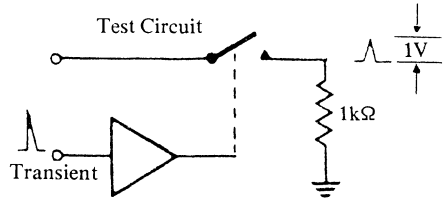


Fig. 2.46 **Plot of Pulse Duration vs. Positive Transient on Ground Line to turn DG184 Switch ON**



The best method of ascertaining noise immunity to fast noise transients is by practical measurement. As an example, the response of the driver to simulated noise transients at the input to a DG184 is given in Figs. 2.45 and 2.46.

2.7.2 Noise on the Supply Voltage Lines

The response of driver gates to noise on the supply lines varies according to the switch mode—depletion or enhancement. Therefore each will be considered separately

2.7.2.1 Depletion Mode Switch

Because of its greater popularity, the n-channel switch is considered but the same argument will apply for p-channel switches except that polarities will be reversed. n-channel depletion mode FETs are held in the OFF state when the gate voltage is taken to the negative rail voltage. Therefore any excursions of the negative supply line due to noise will only cause the device to stay OFF provided the breakdown voltage limits of the device are not exceeded.

Positive excursion of the negative supply lines on the other hand could cause the analogue switch to turn on, because the gate to source or gate to drain voltage has been diminished by the amplitude of the excursion. Most Siliconix IC driver gates incorporating JFET switches have 0.5V to 1.0V noise immunity to negative supply line changes even when the analogue signal is at the peak negative specified value. Positive excursion of the positive supplies do not affect the switch state provided the breakdown voltages are not exceeded.

Negative excursion of the positive supplies could cause the n-channel depletion mode switch resistance to increase if the analogue signal voltage becomes more positive than the supply voltage. In the extreme case a large negative excursion of the positive supply could cause the analogue switch to turn OFF. The shunt resistor driver circuit is not prone to this mechanism because it does not require a positive supply. The response to any fast stimuli on the negative or positive supply rail will depend on the switching speed of the JFET gate. The turn ON and OFF time of the switching FETs used are in the region of 5 to 50 ns. An empirical approach is the best to ascertain the noise immunity, and a curve for the DG184 is shown in Fig. 2.47.

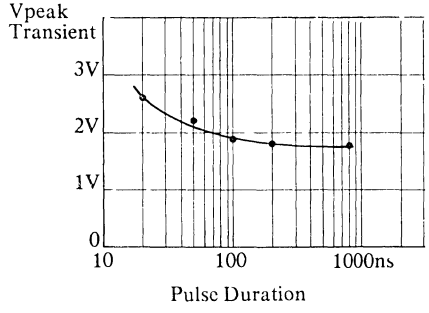


Fig. 2.47
Relationship between pulse transient width and amplitude on the negative supply line to cause spurious operation of the switch for the DG184.

There is no curve shown for transients on the positive supply because it was found that when the positive supply transient takes the body voltage of T_{12} in Fig. 2.16 below the analogue signal level on the source, the source to body and drain to body diodes of the MOSFET conduct. This does not necessarily turn the JFET switch off but is not a recommended operating condition.

2.7.2.2 Enhancement Mode FETs

The P channel MOSFET switch is considered, but similar arguments can be applied to the N channel gates provided polarities are reversed.

The gate voltage of the PMOS switch is held close to the negative rail voltage when the switch is ON. Consequently, a negative excursion of the negative supply will tend to reduce the switch resistance. In the extreme case a large positive excursion might turn the MOSFET switch OFF.

Positive excursion of the positive supply has little effect provided breakdown voltages are not exceeded, but negative excursions can be catastrophic. The body of the PMOS analogue switch is usually connected to the positive supply and consequently any negative excursion which takes the body more negative than the analogue signal voltage causes the source to body or drain to body diode to be forward biased. This could destroy the switch if the diode current flow is not limited to the device maximum ratings.

The effect of fast transients are again best analysed empirically.

2.7.3 Noise on the Analogue Signal

Noise on the analogue signal has a similar effect to noise on the supply lines. A negative noise transient on the analogue signal has a similar effect on the switch as a positive supply transient. A positive noise voltage transition on the analogue signal is equivalent to a negative transition of the positive and negative supplies.

The response to fast noise transients on the analogue signal is also similar to the inverse of these transients appearing on the supplies.

2.8 CHOOSING THE OPTIMUM DRIVER GATE

There is no simple, well defined path available for choosing the most suitable driver gate. There are many factors to be considered and the "weighting" given to each factor will depend on the application. However, a few guidelines can be laid down.

2.8.1 Discretes or Integrated Circuits?

In general, integrated circuits offer advantages in terms of reliability weight, bulk and ruggedness over discrete arrangements. These advantages become even more marked as the switching complexity increases. Discrete devices can, however, offer advantages at the two ends of the performance spectrum :

(a) At the top end, the flexibility available to the discrete circuit designer, enables him to design a circuit to meet a specific goal e.g. very fast switching or very high isolation.

(b) At the bottom end of the spectrum where the switch performance is not stringent an economical design can be achieved by using a simple driver and low cost FET.

2.8.2 JFET or MOSFET?

Again only rough guidelines can be offered since the full details of the application are necessary to make the best choice.

N channel JFET switches offer the lowest and most constant values of ON resistance. The driver circuits used in conjunction with these FETS offer fast switching and high isolation. However, these driver gates have in the past been built using hybrid techniques and consequently are more expensive. They are not yet available in complex arrays.

CMOS switches offer almost constant ON resistance and have the advantage of being able to handle analogue signals equal to the supply voltages. The problems of latch-up associated with CMOS processing in its infancy have now been eliminated.

Both the PMOS and CMOS processes lend themselves to large 8- and 16- channel multiplexing with binary decode circuitry incorporated on the chip in some instances. When one takes into account reliability, performance, size, weight, ruggedness and the cost of these arrays, the discrete approach to multiplexing cannot compete with the integrated circuit approach.

Table 2.1 Analog Switch Preferred Parts Selector Guide

ANALOG SWITCHES

Basic Part No.	Switch Type	$r_{DS(on)}$ Max (Ω) (Note 4)	Analog Voltage Range (V) (Note 4)	Switching Time (μsec) t_{ON}	Switching Time (μsec) t_{OFF}	Logic Levels (V) V_{INL}	Logic Levels (V) V_{INH}	Opt. Supply Voltage (V) (+) Sup. V_1	(−) Sup. V_2	Logic Sup. V_L	Ref. Sup. V_R	Comments
TWO CHANNEL SPST (See Analog Switch Configuration)												
DGM111	PMOS	75-200	+10 to −10	0 3	1 0	0.5	4 6	10	−20	5	–	
DG180	N-JFET	10	+10 to −12.5	0.3	0.25	0 8	2.0	10	−20	5	0	Break-Before-Make
		10	+15 to − 7.5	0.3	0 25	0.8	2.0	15	−15	5	0	15 V Supplies
DG181	N-JFET	30	+10 to −12.5	0 15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make
		30	+15 to − 7.5	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies
DG182	N-JFET	75	+10 to −15	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make
		75	+15 to −10	0.25	0.13	0.8	2 0	15	−15	5	0	15 V Supplies
DG200	CMOS	70	+15 to −15	1.0	0.5	0 8	2 4	15	−15	–	(Note 3)	
DG300	CMOS	50	+15 to −15	0.3	0.25	0.8	4 0	15	−15	–	–	Low Power, TTL In
DG304	CMOS	50	+15 to −15	0.25	0.15	3.5	11 0	15	−15	–	–	Low Power, CMOS In
FOUR CHANNEL SPST (See Analog Switch Configuration)												
DG172	PMOS	150-450	+10 to −10	0 3	0.75	0 8	2.0	10	−20	5	0	
DG201	CMOS	175	+15 to −15	1 0	0 5	0.8	2.4	15	−15	–	(Note 3)	
ONE CHANNEL SPDT (See Analog Switch Configuration)												
DG175	PMOS	75-200	+10 to −10	0.2	0.5	0.8	2.0	10	−20	5	0	
DG186	N-JFET	10	+10 to −12 5	0.3	0.25	0 8	2 0	10	−20	5	0	Break-Before-Make
	N-JFET	10	+15 to − 7.5	0.3	0.25	0.8	2.0	15	−15	5	0	15 V Supplies
DG187	N-JFET	30	+10 to −12.5	0.15	0.13	0 8	2 0	10	−20	5	0	Break-Before-Make
	N-JFET	30	+15 to − 7.5	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies
DG188	N-JFET	75	+10 to −15	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make
	N-JFET	75	+15 to −10	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies
DG301	CMOS	50	+15 to −15	0.3	0.25	0 8	4.0	15	−15	–	–	Low Power, TTL In
DG305	CMOS	50	+15 to −15	0.25	0.15	3.5	11 0	15	−15	–	–	Low Power, CMOS In
TWO CHANNEL SPDT (See Analog Switch Configuration)												
DG189	N-JFET	10	+10 to −12.5	0.3	0 25	0.8	2.0	10	−20	5	0	Break-Before-Make
	N-JFET	10	+15 to − 7.5	0.3	0.25	0.8	2.0	15	−15	5	0	15 V Supplies
DG190	N-JFET	30	+10 to −12.5	0.15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make
	N-JFET	30	+15 to − 7.5	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies
DG191	N-JFET	75	+10 to −15	0 25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make
	N-JFET	75	+15 to −10	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies
DG303	CMOS	50	+15 to −15	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power TTL In
DG307	CMOS	50	+15 to −15	0.25	0.15	3.5	11.0	15	−15	–	–	Low Power, CMOS In
THREE CHANNEL SPDT (See Analog Switch Configuration)												
DG170	PMOS	200-800	+10 to −10	0.3	0.4	0.8	2.0	10	−20	5	0	
TWO CHANNEL DPST (See Analog Switch Configuration)												
DGM122	PMOS	100-450	+10 to −10	0.3	2.0	0.4	1 mA (1)	10	−20	5	0	
DG183	N-JFET	10	+10 to −12.5	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make
	N-JFET	10	+15 to − 7.5	0.3	0.25	0.8	2.0	15	−15	5	0	15 V Supplies
DG184	N-JFET	30	+10 to −12 5	0 15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make
	N-JFET	30	+15 to − 7.5	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies
DG185	N-JFET	75	+10 to −15	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make
	N-JFET	75	+15 to −10	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies
DG302	CMOS	50	+15 to −15	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, TTL In
DG306	CMOS	50	+15 to −15	0.25	0.15	3.5	11.0	15	−15	–	–	Low Power, CMOS In
ONE CHANNEL DPDT (See Analog Switch Configuration)												
DG173	PMOS	150-450	+10 to −10	0.2	0.7	0.8	2.0	10	−20	5	0	2 Input "OR" Control
FOUR CHANNEL SPDT D/A CONVERTER SUMMING NODE SWITCHES (See Analog Switch Configuration)												
DG515	NMOS		(see comments)	0.12	0.17	0.5	7.5	8.0	0	–	–	R_1 = 6.25 Ω, R_2 = 12.5 Ω, R_3 = 25 Ω, R_4 = 50 Ω
TEN CHANNEL SPDT D/A CONVERTER SUMMING NODE SWITCHES (See Analog Switch Configuration)												
DG516	NMOS		(see comments)	0.12	0.17	0.5	7.5	8.0	0	–	–	R_1 = 100 Ω, R_2 = 200 Ω, R_3 = 400 Ω, R_4 = 800 Ω, R_5 = 1600 Ω, R_6 −10 = 3200 Ω

ABBREVIATIONS

Prop.	– propagation	Comp.	– complementary	NA	– not applicable
Chn.	– channel	Ind.	– independent	Trmnls.	– terminals
Sw.	– switch	Com.	– common	Diffrntl.	– differential
Drvr.	– driver	MUX	– multiplexer		

Table 2.1 Analog Switch Preferred Parts Selector Guide (Cont'd)

ANALOG MULTIPLEXERS

Basic Part No.	Process Type	$r_{DS(on)}$ Max (Ω) (Note 4)	Analog Voltage Range (V) (Note 4)	Transition Time (μsec) (Note 2)	Logic Levels (V) V_{INL}	Logic Levels (V) V_{INH}	Opt. Supply Voltage (V) (+) Sup. V_1	Opt. Supply Voltage (V) (–) Sup. V_2	Opt. Supply Voltage (V) Ref. Sup. V_R	Comments
EIGHT CHANNEL MUX + ENABLE (See Analog Switch Configuration)										
DG501	PMOS	150-250	+ 5 to – 5	1.5	0.6	3.5	5	–20	0	Logic Pullup Resistors
DG503	PMOS	150-800	+10 to –10	1.5	0.6	8.5	10	–20	0	
DG508	CMOS	400	+15 to –15	1.0	0.8	2.4	15	–15	—	Break-Before-Make
SIXTEEN CHANNEL MUX + ENABLE (See Analog Switch Configuration)										
DG506	CMOS	400	+15 to –15	1.0	0.8	2.4	15	–15	(Note 3)	Break-Before-Make
FOUR CHANNEL DIFFERENTIAL MUX + ENABLE (See Analog Switch Configuration)										
DG509	CMOS	400	+15 to –15	1.0	0.8	2.4	15	–15	—	Break-Before-Make
EIGHT CHANNEL DIFFERENTIAL MUX + ENABLE (See Analog Switch Configuration)										
DG507	CMOS	400	+15 to –15	1.0	0.8	2.4	15	–15	(Note 3)	Break-Before-Make

DRIVERS FOR FET SWITCHES

Basic Part No.	Inputs	Outputs	Function and Uses	ON Level $V_{(out)}$ ON – V_2 At Rated Current(s)	OFF Level $V_{(out)}$ OFF At Rated Current Or $I_{(out)}$ OFF At Rated Voltage	Input Logic for V_{OUT} (low)	Input Limits V_{INL} (V)	Input Limits V_{INH} (V) (I_{INH}) (mA)	Optimum Supply Voltages (V) V_1	Optimum Supply Voltages (V) V_2	Optimum Supply Voltages (V) V_L	Optimum Supply Voltages (V) V_R	Switching Time (μs) t_{ON}	Switching Time (μs) t_{OFF}
D125	6	6	Six Separate MOSFET-Drivers	0.4 V @ 5 mA	0.1 μA @ 10 V	0	0.5	4.6	(Note 5)	–20	5	—	0.6	1.2
D129	7	4	Four Channel (BV=50) MOSFET-Driver with Decode	0.7 V @ 10 mA	0.1 μA @ 10 V	1	0.7	2.2	(Note 5)	–20	—	—	0.25	0.8
D139	2	4	Dual High-Speed Drivers/with Complimentary Outputs	1.1 V @ 10 μA 1.5 V @ 2 mA	V_1 – 2 V @ 2 mA	Output and Compliment Available	0.8 0.8	2.0 2.0	10 10	–20 –20	5 5	0 0	0.17 0.17	0.2 0.2

MULTIPLE FET SWITCHES

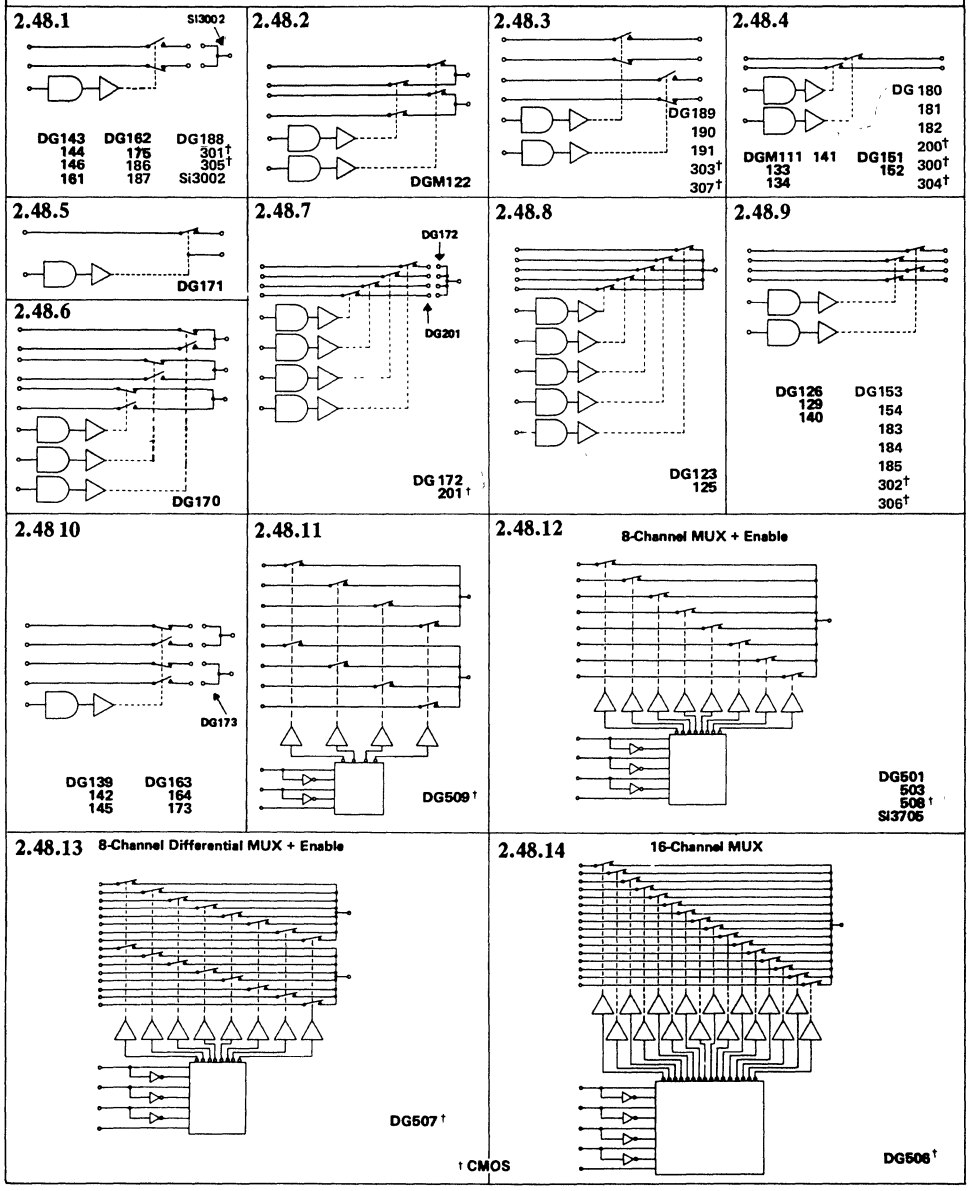
Basic Part No.	Sources	Drains	Gates	Switch Function	Switch Type	r_{DS} MAX (Ω) @ V_S = +10 V	r_{DS} MAX (Ω) @ V_S = –10 V	BV_{DSS}	$I_{S(off)}$ (nA)	$V_{GS(th)}$ Min	$V_{GS(th)}$ Max	
G115	6	1	6	SP6T	PMOS	100	450	–30	0.5	–1.5	–4.0	6 Switches, Common Out
G123	4	2	4	2XSPDT	PMOS	100	450	–30	0.5	–1.5	–4.0	4 Switches
G128	4	4	4	4XSPST	JFET	45	45	–40	0.1	($V_{GS(off)}$)	–1.0	4 Switches, Ind. Trmnls.

NOTES:

1. Current Driven Device – I_{INH} = 1 mA
2. The appropriate switching characteristic for multiplexers is $t_{TRANSITION}$, not t_{ON}, t_{OFF}.
3. V_{REF} = 1.5 V is used when supply voltages < ±15 V are used. Not needed when supply voltages of ±15 V are used.
4. Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, r_{DS} is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail. Values shown are for temperature suffix A.
5. Device normally operates with resistor to +10 V.

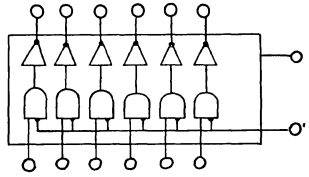
Figs. 2.48.1 to 2.48.13

Analogue Switch Combinations



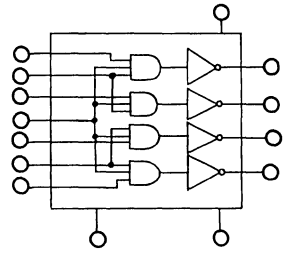
Figs. 2.48.15 to 2.48.24
Analogue Switch Combinations

2.48.15



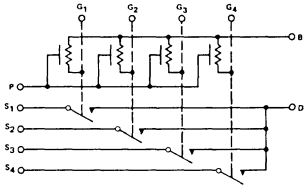
D125

2.48.16



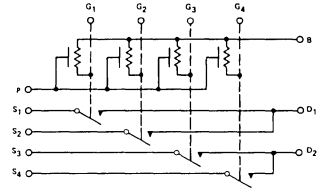
D129

2.48.17



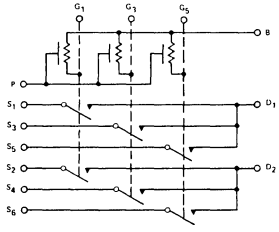
G124

2.48.18



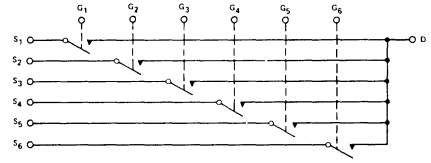
G123

2.48.19



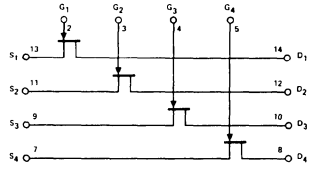
G119

2.48.20



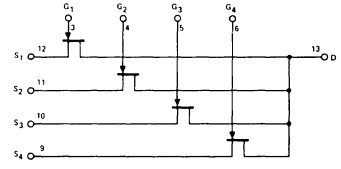
G118

2.48.21



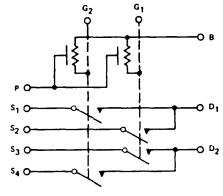
G125 through G128

2.48.22



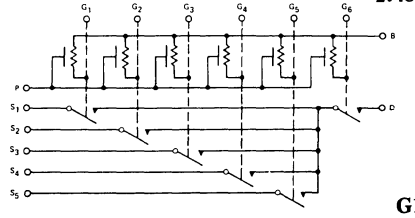
G129 through G132

2.48.23



G122

2.48.24

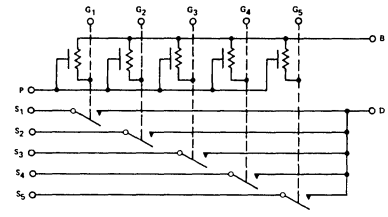


G117

Figs. 2.48.25 to 2.48.26

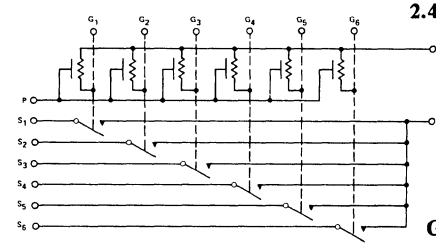
Analogue Switch Combinations

2.48.25



G116

2.48.26

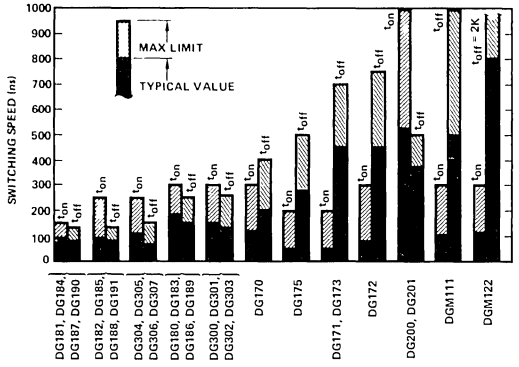


G115

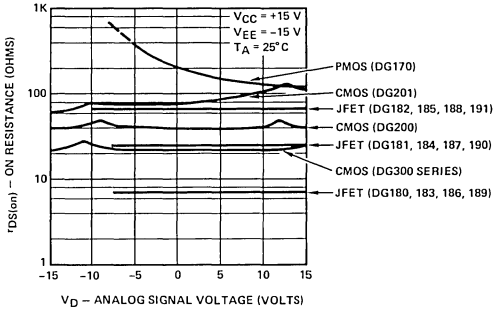
Fig. 2.49 Analog Switch Performance Guide Selector

TYPICAL PERFORMANCE CHARACTERISTICS

Typical t_{on}/t_{off}



Typical $r_{DS(on)}$ vs V_D



NOTE: The CMOS switches are the only ones capable of switching signals down to the negative supply.

CHAPTER 2

SELECTION GUIDE, LISTED BY PERFORMANCE:

$r_{DS(on)}$	
Device No.	(Ω)
DG180, DG183 DG186, DG189	10 Ω
DG181, DG184, DG187, DG190	30 Ω
DG300, DG301, DG302, DG303, DG304, DG305, DG306, DG307	50 Ω
DG200	70 Ω
DG182, DG185, DG188, DG191	75 Ω
DG171	40 to 100 Ω
DG175, DGM111	75 to 200 Ω
DG201	175 Ω
DG501*	150 to 250 Ω
DG172, DG173	150 to 450 Ω
DG506*, DG507* DG508*, DG509*	400 Ω
DG503*	150 to 800 Ω
DG170	200 to 800 Ω

t_{ON}/t_{OFF}	
Device No.	(ns)
DG181, DG184, DG187, DG190	150/ 130
DG182, DG185, DG188, DG191	250/ 130
DG304, DG305, DG306, DG307	250/ 150
DG180, DG183, DG186, DG189	300/ 250
DG300, DG301, DG302, DG303	300/ 250
DG170	300/ 400
DG175	200/ 500
DG171, DG173	200/ 700
DG172	300/ 750
DG200, DG201	1000/ 500
DGM111	300/1000
DGM122	300/2000

Analog Signal Range (with ±15 V supply)	
Device No.	(Volts)
DG200, DG201, DG506*, DG507* DG508*, DG509*	+15 to −15 V
DG300, DG301, DG302, DG303, DG304, DG305, DG306, DG307	+15 to −15 V
DG182, DG185, DG188, DG191	+15 to −10 V
DG180, DG181, DG183, DG184, DG186, DG187, DG189, DG190	+15 to −7.5 V
DG170, DG171, DG172, DG173, DG175, DGM111, DGM122	+15 to −5 V

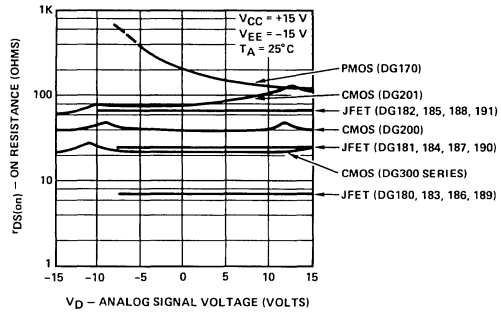
***Multiplexers**

Better performance than shown can be obtained from Siliconix analog switches by special sorting at customer request, or by using discrete FET devices chosen for optimal switching characteristics

2.9 APPLICATION CIRCUITS

2.9.1 Analog Switch Range Application Hints

Fig. 2.50
Analog Signal Range and Typical $r_{DS(on)}$ vs V_D



NOTE: The CMOS switches are the only ones capable of switching signals down to the negative supply.

JFET switches restrict the analog signal range a pinch-off voltage away from one rail. For the N-Channel JFETs, the analog signal must be more positive than the negative supply by an amount equal to the pinch-off voltage. (Refer to Section 2.3.7). The analog signal can go up to the positive supply. Maximum negative analog signal,

$$|V_A| < |V-| - |V_P| \qquad \text{eqn. 2.13}$$

Negative Supply	Maximum Negative Analog Signal	
	V_P = –7.5 V (10 Ω, 30 Ω)†	V_P = –5 V (75 Ω)††
–7.5 V	0 V	–2.5 V
– 12 V	– 4.5 V	– 7 V
– 15 V	– 7.5 V	– 10 V
– 20 V	–12.5 V	– 15 V

† DG180, 181, 183, 184, 186, 187, 189, 190 10 Ω and 30 Ω N-JFET switches have V_P = –7.5 V.

†† DG182, 185, 188, 191 75 Ω N-JFET switches have V_P = –5 V.

CMOS analog signal range is equal to the power supply rails, with ± 15 V supplies, signal range is ± 15 V.

CMOS Application Hints*

DG200-DG201 and DG506-DG509

V_1 Positive Supply Voltage (V)	V_2 Negative Supply Voltage (V)	V_{REF} Reference Pin Connection (V)	V_S or V_D Analog Voltage Range (V)
+15**	−15	Open	−15 to +15
+12	−12	Open or 1.4 V	−12 to +12
+10	−10	1.4 V	−10 to +10
+ 8***	− 8	1.4 V	− 8 to + 8
DG300-307† (as above, down to:)			
+ 5	− 5	—	− 5 to + 5

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Characteristics chart based on V_1 = +15 V, V_2 = −15 V, V_{REF} = Open.

***Operation below ±8 V is not recommended for DG200, DG201, DG506-509.

†Will also operate on a single supply; see Application Note AN76-6, page 7-88.

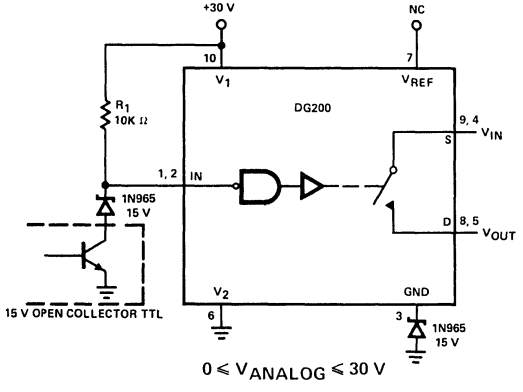
PMOS switches require enhancement; the analog signal must stay more positive than the negative supply by the threshold voltage. As shown on the graph on page 2-48, ON resistance increases for negative analog signals, and the usable threshold for the PMOS switches is ≈ 7.5 V.

2.9.2 **Single Supply Analog Switching for CMOS Analog Switches (Refer to AN75-1 and AN76-6)**

Analog signal range must be within the V_1 to V_2 voltages

$$V_1 \leq V_{ANALOG} \leq V_2$$

Fig. 2.51
Operation From a Unipolar Supply



DG200-201, DG506-509 CMOS family, requires offsetting of GND voltage.
NOTE: Pin connections shown for metal can package

DG200, 201, 506-509 CMOS family requires the GND terminal to be offset from V_2 by at least 8 volts. These devices will switch satisfactorily for $V_1 \geq 15$ V ($V_2 = 0$). Note that the logic input must operate from the offset GND and V_1.

DG300-307 CMOS family analog switches will operate with GND and V_2 at the same potential and with the logic input operating from ground toward V_1 (standard logic supplies will interface). The devices will operate with a single V_1 supply down to +5 V up to +25 V. However, the lower the supply the higher the $r_{DS(on)}$ and the slower the t_{ON} (refer to AN76-6, page 7-88).

Fig. 2.52
DG300-303 Single Supply

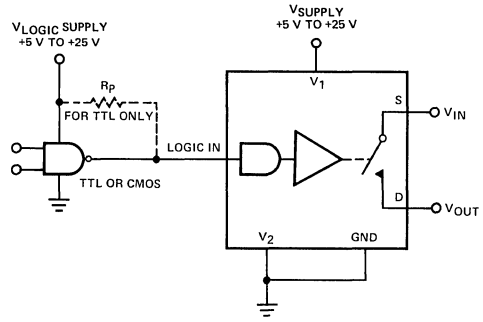
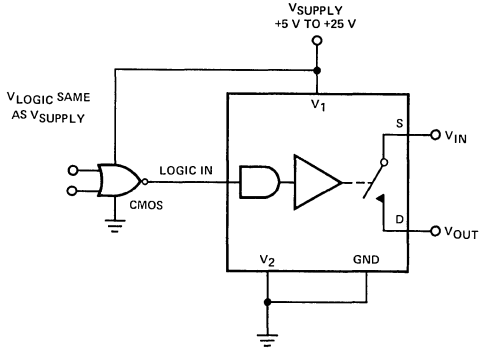


Fig. 2.53
DG304-307 Single Supply



2.9.3 Typical Analog Switch Application Circuits

The following is a list of applications pertaining to Chapter 2 which can be found in "Applications Information," Chapter 7. Please refer to the page number indicated.

.1 *A Resettable Integrator* – AN75-1, Page 7-68, Figure 10.

.2 *A Precision Amplifier with Digitally Programmable Inputs and Gains* – AN75-1, Page 7-67, Figure 8.

.3 *Low Power Non-Inverting Amplifier with Digitally Selectable Inputs and Gain* – AN76-6, Page 7-90, Figure 28.

.4 *Low Power Inverting Amplifier with Digitally Selectable Gain* – AN76-6, Page 7-90, Figure 29.

.5 *Polarity Reversing Low Power Amplifier* – AN76-6, Page 7-90, Figure 30.

.6 *Latching SPDT Switches* – AN75-1, Page 7-69, Figure 13.

.7 *4-Channel "Scope Extender" Multiplexing* – AN75-1, Page 7-66, Figure 6.

.8 *Active Low Pass Filter with Digitally Selected Break Frequency* – AN75-1, Page 7-67, Figure 7.

2.9.4 **Low Power Analog Switching (refer to AN76-6, pp. 7-79 to 7-92)**

.1 *Low Power Instrumentation Amplifier with Digitally Selectable Inputs and Gain* – AN76-6, Page 7-91, Figure 31.

.2 *Low Power Active Filter with Digitally Selectable Center Frequency* – AN76-6, Page 7-86, Figure 18.

2.9.5 **High Frequency Video Switching (Refer to AN73-3, pp. 7-15 to 7-26)**

.1 *Video Switch Block Diagram and Performance* – AN73-3, Page 7-20, Figures 8-13.

.2 *Video Switch with Very High OFF Isolation* – AN73-3, Page 7-26, Figures 30 and 31. Also AN75-1, Page 7-70, Figure 15 and Page 7-71, Figure 16.

2.9.6 **Charge Coupling Cancellation Circuits (Refer to AN74-2, pp. 7-57 to 7-62)**

.1 *Low Drift Compensated Sample and Hold* – AN74-2, Page 7-59, Figure 8.

.2 *DG201 Sample and Hold* – AN74-2, Page 7-60, Figure 10.

.3 *Switching Transients Attenuated by Synchronization of Switches* – AN74-2, Page 7-61, Figure 11.

.4 *Charge Compensated Sample and Hold* – AN74-2, Page 7-61, Figure 12.

2.10 REFERENCES

2.1 "ICs End the Driver Gap," Siliconix Application Note. (Refer to page 7-27 and 7-97.)
2.2 "Interface Circuits Drive High Level Switches From Low Level Inputs," Siliconix Application Note.
2.3 "Driving the JFET Switch," Siliconix Application Note. (Refer to page 7-27.)
2.4 "Physical Electronics and Circuit Models of Transistors," Gray, De Witt, Boothroyd & Gibbons. Wiley 1964.

Recommended Reading: Cobbold; "Applications and Theory of FETs." Wiley Interscience.

Chapter 3

Multiplexing

3.1 INTRODUCTION

Multiplexing is used where it is necessary to transfer information from many signal channels at a sending station to a "remote" receiving point. In this context, a remote point may be thought of as any point to which the cost of installing a separate line or radio path for each channel would be prohibitive. Several forms of multiplexing may be used and the principles as well described by Landon *(Ref. 3.1)*.

In general, there are two basic modes: **Time Division Multiplexing** (TDM) or **Frequency Division Multiplexing** (FDM).

The signals available to the input channels may be in two forms: analogue or digital, as shown in Figs. 3.1 and 3.2 respectively. Digital signals are obtained in various ways and may be the result of logical encoding of an analogue signal in an Analogue-to-Digital converter and will usually consist of pulses switching between two logic voltage levels: logic '0' and logic '1'. Analogue signals are normally continuously variable voltages (or currents) often obtained from transducers. The analogue signal may represent any physical phenomenon: temperature, pressure, velocity, light intensity, speech, etc.

Multiplexing occurs in many fields: industrial process control, medical electronics, aircraft systems monitoring, telemetry, and communications being but a few.

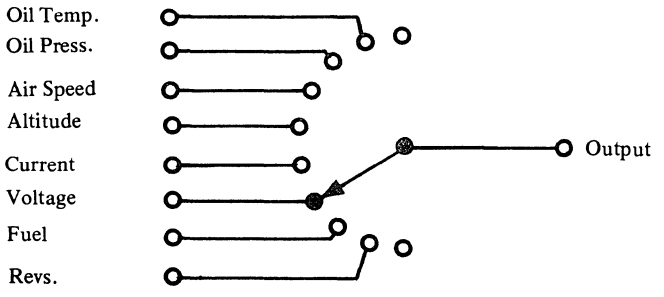


Fig. 3.1 **Basic Analogue Multiplexer**

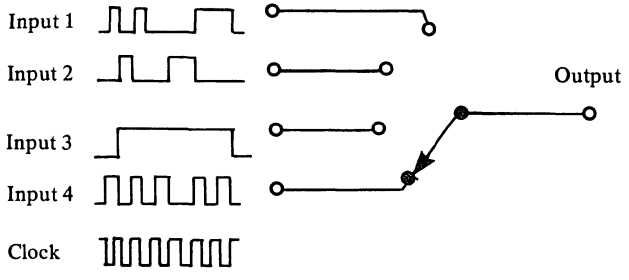


Fig. 3.2 **Basic Digital Multiplexer**

The channel sampler may, in its simplest form, be a motor driven commutator. At the receiving end, the reverse process would take place using an identical commutator, its speed and position being synchronised with the first. The commutation process has analogies in discrete electronic forms employing relays, valves, diodes, bipolar or field effect transistors as switching elements. However, modern technology has resulted in the production of integrated systems which are more compact, more reliable and as economical as the equivalent discrete circuit. For example, the DG506 is a monolithic 16-channel to one-channel multiplexer employing CMOS technology. It has logic decoder, drivers and 16 analogue switches on a silicon chip which is only 0.158 inches long and 0.083 inches wide.

These multichannel devices usually employ P-channel MOS (PMOS) or Complementary MOS (CMOS) technologies on a monolithic chip, and have switching times around 1μs (DG 506). For faster switching times, multichip hybrid devices using Schottky clamped bipolar, PMOS and Junction FET (JFET) processing could be used, and there are a number of these devices with switching times of less than 150ns (DG 181 series). Other technologies are also available which give improved speeds. In general, the faster devices are limited in the number of channels that are available per package.

3.2 FACTORS AFFECTING SYSTEM PERFORMANCE

In any multiplexing application, the following factors should be considered:

1) **System Attenuation** Includes loss in analogue signal due to the multiplexing and demultiplexing devices and the transmission path. This is a frequency dependent factor.
2) **Channel Isolation** At low frequencies, this is principally a function of channel OFF leakage currents, and at high frequencies is a function of device and system capacitances.
3) **Crosstalk** There are several sources of crosstalk, the main ones being overlap between switching channels due to imperfect break-before-make switching, switch leakages, OFF switch capacitances, inter-switch capacitances, stray circuit capacitances, distortion in the transmission medium etc.
4) **Noise** There are several sources of noise, including thermal or Johnson noise generated in any resistive components, crosstalk, leakages, switching transients, as well as thermal EMFs and transmission path pick-up.
5) **Switching Rates** These are important in sampling systems where they determine the maximum analogue signal handling frequency of the multiplexer and define crosstalk errors.

3.3 CONSIDERATIONS OF MULTIPLEXER ERRORS

3.3.1 Multiplexer Equivalent Circuits

Any multiplexer will introduce errors into the transmission path. These errors can be calculated from a knowledge of the equivalent circuits of the multiplexer in both the ON and OFF channel cases. The multiplexer equivalent circuit can be developed from a knowledge of the equivalent circuits of single switches in ON and OFF states.

3.3.2 Equivalent Circuit of a Single Switch in the ON State

The equivalent circuit of an ON switch varies from one type of driver circuit to another, and it will therefore be necessary to present specific examples. For this purpose, the Siliconix DG181 and DG171 output stages are presented. The DG181 circuit is shown in Fig. 3.3a and a JFET cross-sectional profile in Fig. 3.3b.

Fig. 3.3a **Output stage of DG181 with JFET switch**

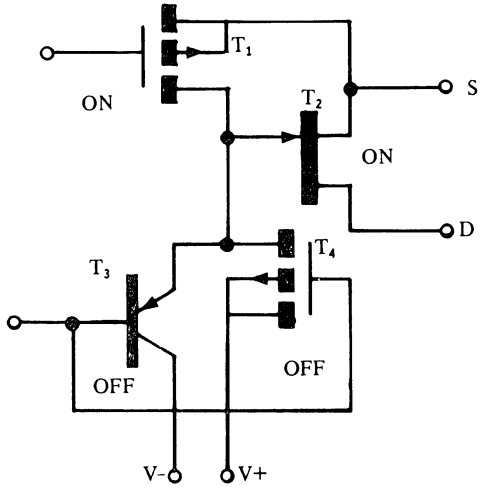
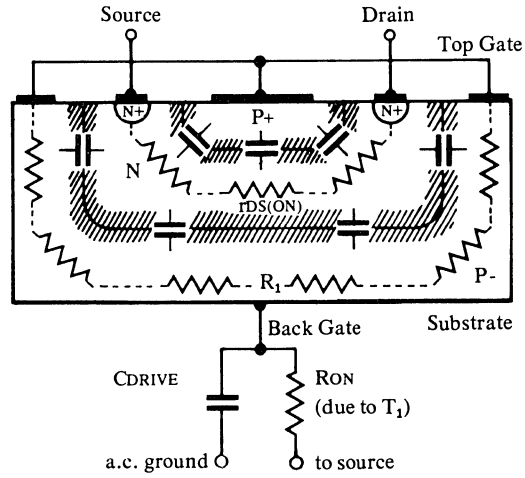


Fig. 3.3b
Cross-sectional profile of JFET in the ON state



The top gate and the back gate of the JFET are effectively connected via R_1, where R_1 is the distributed substrate resistance, and is usually a few ohms. R_{ON} and C_{DRIVE} are contributions from the driver circuit. The shaded areas indicate depletion regions. The capacitive and resistive components shown, may be "lumped" together to give the equivalent circuit shown in Figure 3.4.

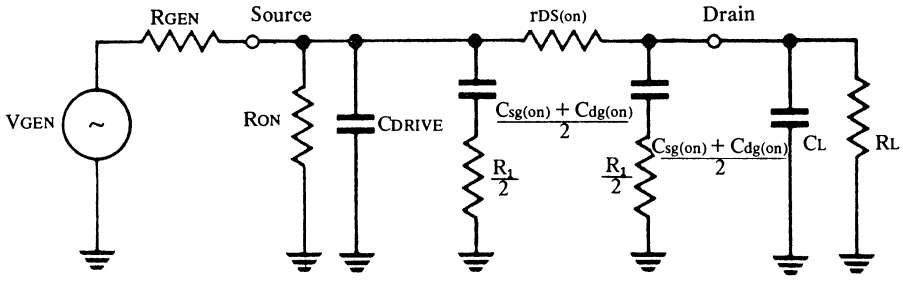


Fig. 3.4 **Lumped equivalent circuit of DG181 switch**

RON represents the ON resistance of the MOS driver circuit; RL and CL are assumed load conditions. Since the channel is ON, the drain and source are electrically connected via the low ON resistance of the channel. The drain-to-gate capacitance in the ON state will therefore be due to half the channel-to-gate capacitance, and the source-to-gate capacitance will account for the other half.

Because of the symmetrical geometry of most JFET chips, $C_{dg(on)}$ is approximately equal to $C_{sg(on)}$. As R_1 is so small, further approximation may be made to give the equivalent circuit of Fig. 3.5

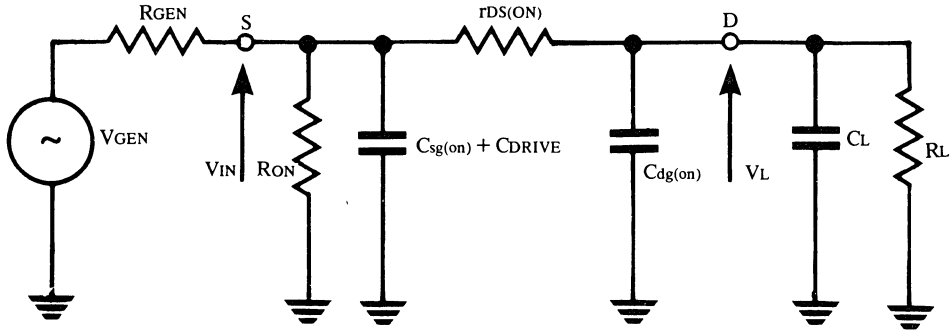


Fig. 3.5 **Simplified equivalent circuit of DG181**

For the DG171 PMOS switch, the output section is somewhat different, as shown in Figs. 3.6a and 3.6b.

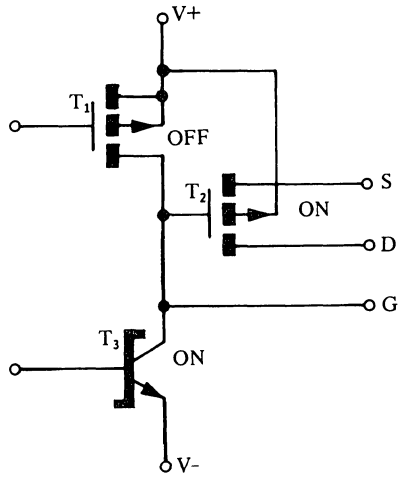


Fig. 3.6a **DG171 output with PMOS switch ON**

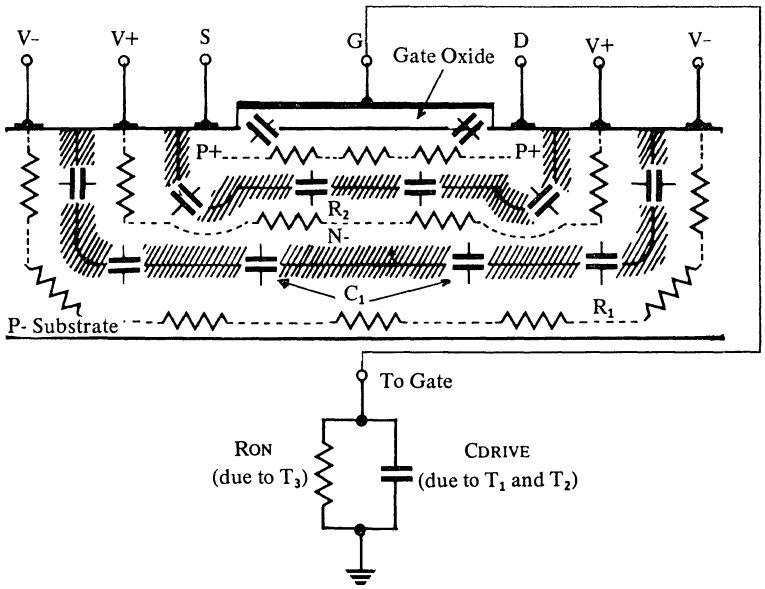


Fig. 3.6b **Cross section of DG171 PMOS output switch**

The p+ region lying between the source and drain is the channel. A discrete PMOS transistor has an n- substrate, but in the DG171 monolithic PMOS process, the MOSFETs are electrically isolated from each other by virtue of a p-type substrate. This results in additional R and C components as shown in Fig. 3.6b. The lumped circuit equivalent is shown in Fig. 3.7a. This reduces to that of Fig. 3.7b and further reduces to that of Fig. 3.7c.

Figure 3.7a **Lumped equivalent circuit of DG171**

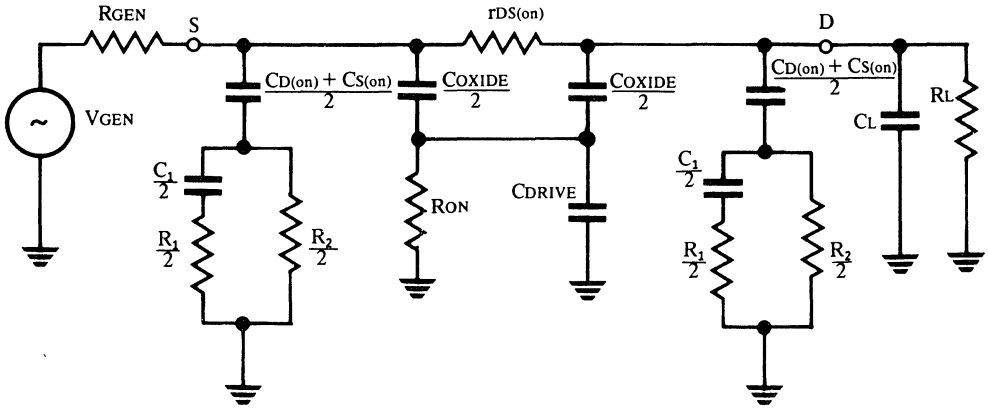


Figure 3.7b

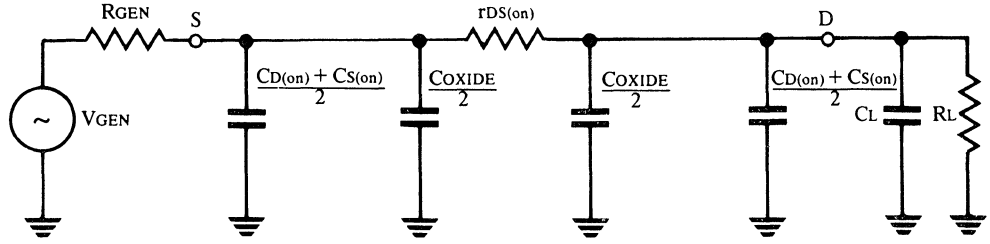
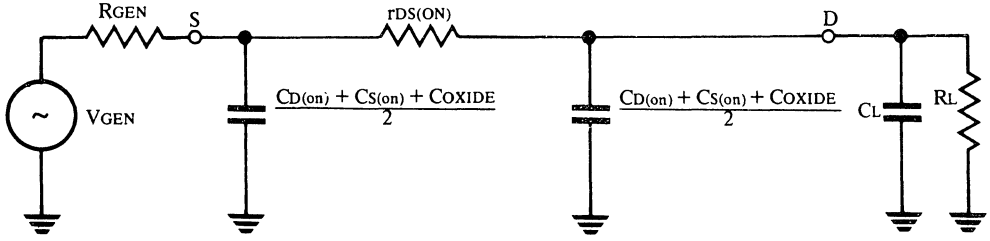


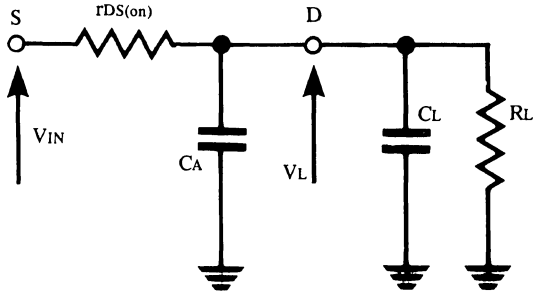
Figure 3.7c



$C_{D(on)} + C_{S(on)}$ represents the channel ON capacitance; C_{OXIDE} represents the channel-to-gate capacitance due to the gate oxide; R_{ON} and C_{DRIVE} represent the characteristics of the driver. R_1, R_2 and R_{ON} are small.

The circuits of Figs. 3.5 and 3.7c may be reduced further to that of Fig. 3.8, if the transfer function from source to drain only is under consideration.

Fig. 3.8 **Simplified equivalent circuit of DG171**



$$\text{Transfer Function} = \frac{V_L}{V_{IN}}$$

$$C_A = \frac{C_{D(on)} + C_{S(on)} + C_{OXIDE}}{2}$$

The simplified equivalent circuit of Fig. 3.8 may be used to represent devices utilising three different fabrication technologies, with the typical values of Table 3.1.

Table 3.1

Switch Technology	Switch Type	$r_{DS(ON)}$ (Ω)	C_A (pF)
PMOS	DG171	25-35	30-40
JFET	DG181	15-25	10-14
CMOS	DG200	45-60	18-24

This table refers to results obtained for small analogue inputs and with supply voltages as given in the Data Sheets.

CHAPTER 3

3.3.3 Equivalent Circuit of Single OFF Switch

A similar consideration to OFF channel conditions is given below for JFET and PMOS switch types DG181 and DG171, respectively. Fig. 3.9 shows the simplified cross-sectional profile of a DG181 JFET chip in the OFF state with distributed characteristics indicated (cf. with ON state, Fig. 3.3).

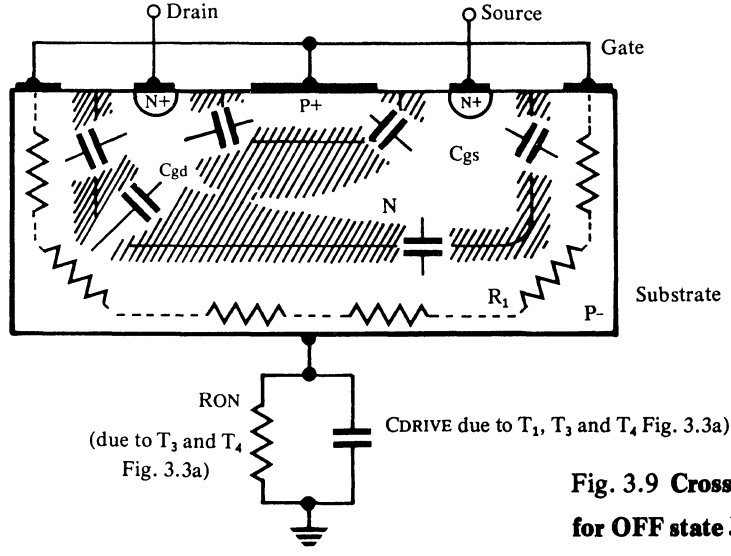
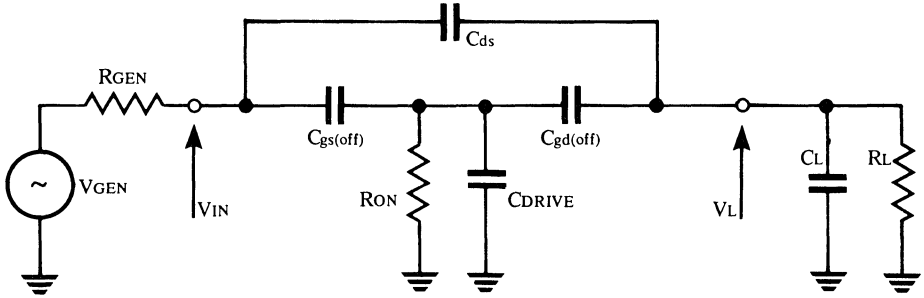


Fig. 3.9 Cross-sectional profile for OFF state JFET (DG181)

C_{gs} and C_{gd} are gate-source and gate-drain capacitances. RON and CDRIVE represent the driver impedance, and R_1 is the lumped resistance of the substrate. In addition to the OFF state capacitances C_{gs} and C_{gd}, account may also be taken of C_{ds} (approximately 0·1pF). R_1 is a few ohms and can be neglected, so the equivalent circuit reduces to that shown in Fig. 3.10.

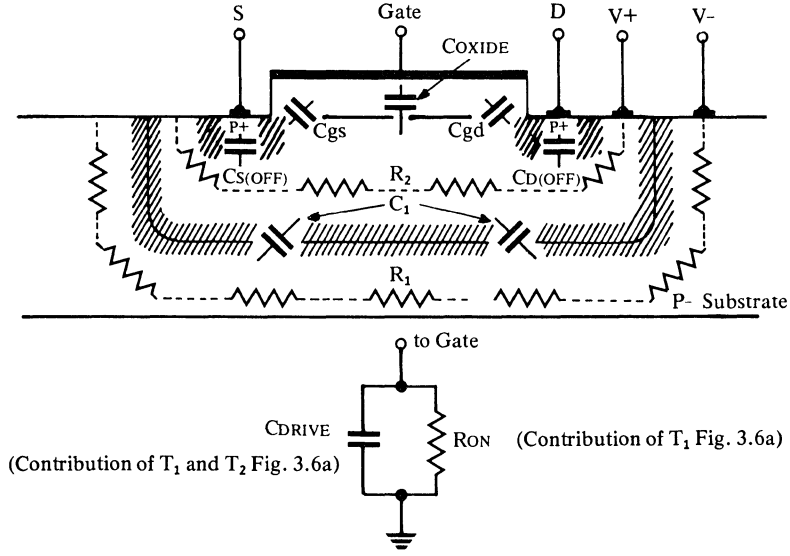
Fig. 3.10 **Equivalent circuit for OFF state JFET (DG181)**



RON and CDRIVE are very significant in determining OFF isolation.

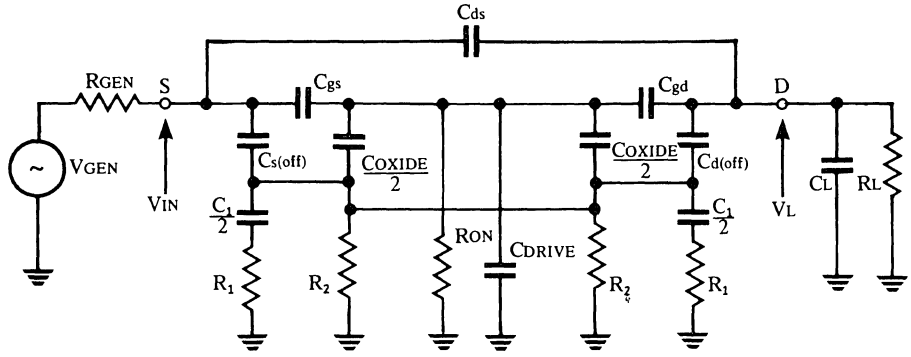
The simplified cross-sectional profile of the DG171 PMOS switch is shown in Fig. 3.11 (cf. with ON state in Fig. 3.6).

Fig. 3.11 **DG171 Switch in OFF state**



The lumped circuit equivalents are shown in Fig. 3.12a and the development of the equivalent circuit shown in Figs. 3.12b and 3.12c.

Fig. 3.12a **Equivalent circuit of DG171 output in the OFF state**



If R_1 and R_2 are small, Fig. 3.12a reduces to the form of Fig. 3.12b and thence to Fig. 3.12c.

Fig. 3.12b

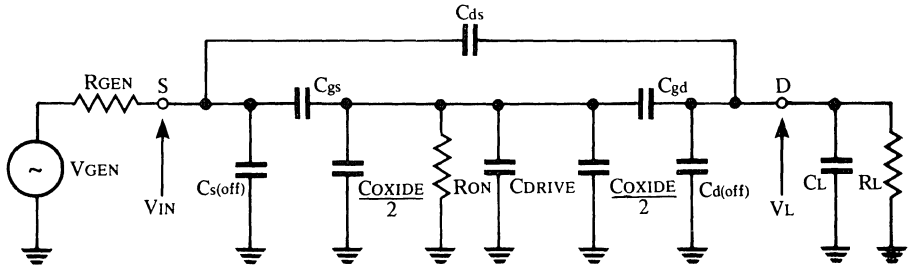
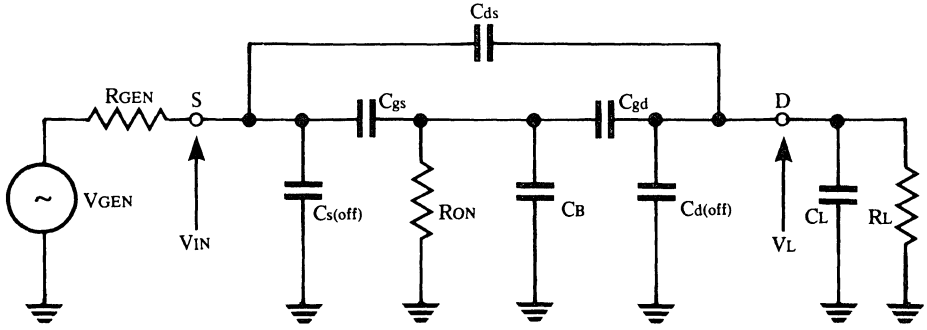


Fig. 3.12c



where $C_B = C_{OXIDE} + C_{DRIVE}$

Typical values for the components of Fig. 3.10 and 3.12c are given in Table 3.2 for the DG181 and DG171. The supply voltages for the DG181 are ±15V, and for the DG171 they are +10V, -20V.

Table 3.2

Device Technology	Device Type	Cgs (pF)	Cgd (pF)	Cds (pF)	C_B (pF)	R_{ON} (Ω)
JFET	DG181	4·5	3·8	0·1	14	200
PMOS	DG171	5	5·2	0·1	22	1·9k

The OFF equivalent circuit for a CMOS switch is more complicated, and an example is given in Chapter 2, section 2.6.2.2. The device type taken in that example is the Siliconix DG200. In every equivalent circuit, any additional strays between input and output must be accounted for and may be designated C_{STRAY} and shown in parallel with C_{DS}.

3.3.4 Equivalent circuit of an ON channel in an *N*-way Multiplexer

A multiplexer configuration consists of N switches with a common output such that only one switch is ON and only one signal is being transmitted at any instant. If N is large, the multiplexers will invariably have MOS outputs. The situation will be now considered where one channel is ON and the equivalent circuit of the ON channel derived.

The remaining N-1 OFF channels may be simplified by approximating each OFF channel to a single capacitor of value C_{EQ}. Furthermore, when account is taken of circuit strays, C_{STRAY}, the equivalent for each channel may be defined as C_T, where $C_T = C_{STRAY} + C_{EQ}$.

The multiplexer equivalent circuit is now shown in Fig. 3.13.

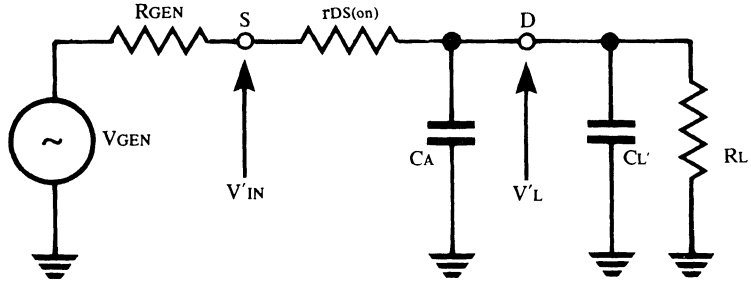


Fig. 3.13 *N*-way Multiplexer viewed from ON channel

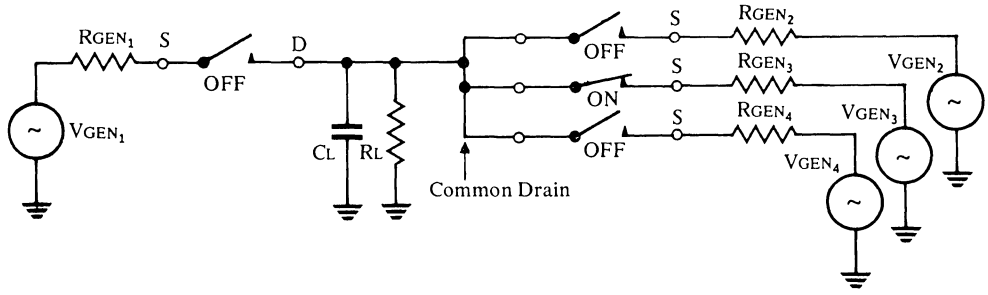
where $C_L' = C_L + (N\text{-}1).\ C_T$.

C_L is the load capacitance and $C_A = \frac{C_{D(ON)} + C_{S(ON)} + C_{OXIDE}}{2}$ as described in section 3.32.

3.3.5 Equivalent circuit of an OFF channel of an *N*-way multiplexer

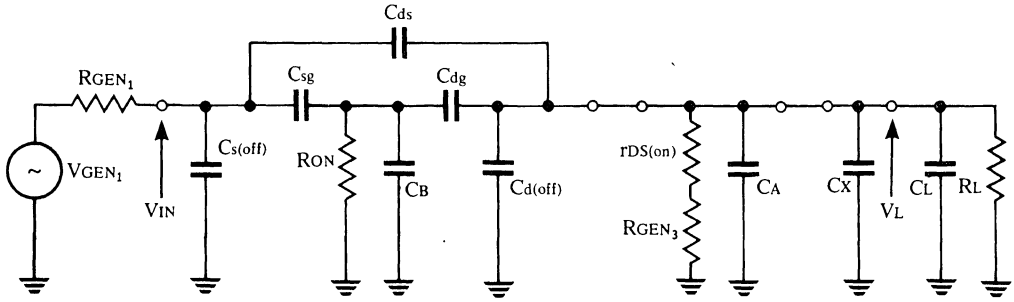
The case to be considered is that of the multiplexer as viewed from one of the OFF channels, as shown in Fig. 3.14 for a 4-channel unit.

Fig. 3.14 **4-Channel multiplexer viewed from an OFF channel**



The equivalent circuit reduces to the form of Fig. 3.15.

Fig. 3.15 **Equivalent circuit of Fig. 3.14**



where $C_x = (N-2)\ C_T$ and is entirely due to the remaining OFF channels.

The total load condition presented to the OFF channel can be obtained by reduction to a single RC combination R_L'' and C_L'', replacing R_L and C_L, such that

$$C_L'' = C_L + C_X + C_A$$
$$= C_L + C_A + (N-2).\ C_T$$

$$\text{and } R_L'' = \frac{R_L(r_{DS(on)} + R_{GEN_3})}{R_L + r_{DS(on)} + R_{GEN_3}}$$

From these equivalent circuits, it is possible to develop expressions for factors specifically relating to multiplexer performance, as indicated in section 3.2.

3.4 FET MULTIPLEXER PERFORMANCE

3.4.1 **Signal Attenuation due to ON switch.** This may be derived from examination of Fig. 3.13.

For d.c. or low frequency conditions the capacitive components of C_A and C_L can be neglected and attenuation is due to the resistance $r_{DS(ON)}$.

Hence multiplexer insertion loss at low frequencies may be given by :

$$\frac{V_{IN}' - V_L'}{V_{IN}'} = \frac{r_{DS(on)}}{R_L + r_{DS(on)}}$$

which in logarithmic form is

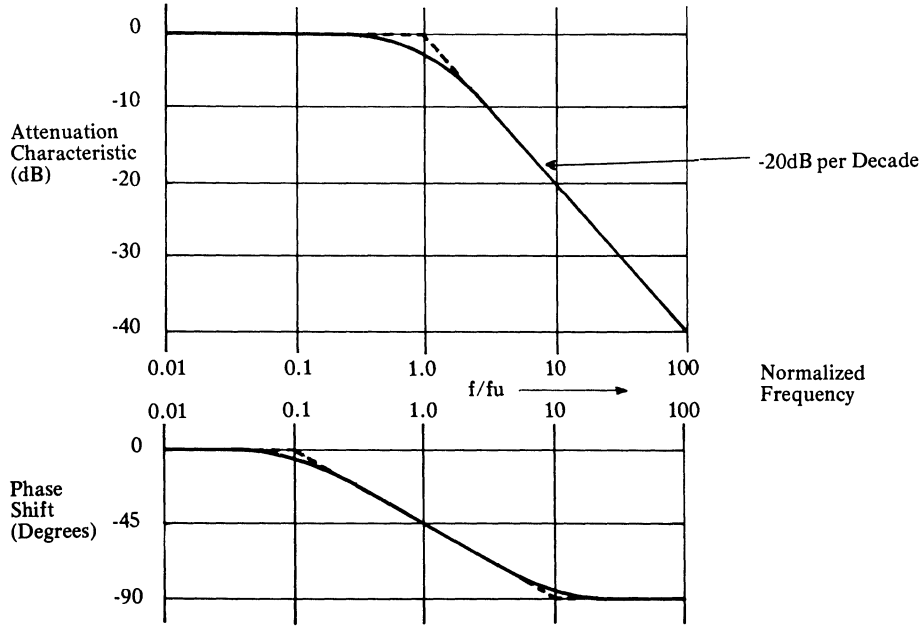
$$20\,[\log_{10} r_{DS(ON)} - \log_{10}(R_L + r_{DS(ON)})]\ \text{dB}$$

For example, if R_L = 10kΩ and $r_{DS(ON)}$ = 100Ω at d.c. then the insertion loss is 0·99%. One per cent error is a typical criterion for some high accuracy d.c. multiplexing applications.

For the JFET switch $r_{DS(ON)}$ max may be lower than 10 ohms at 25°C, as is the case for the DG180 two-channel switch with typical values of around 8 ohms. CMOS devices exhibit higher values of $r_{DS(ON)}$ e.g. the DG200 two-channel switch exhibits typically 50 ohms with analogue signals up to ± 10 volts. On the other hand, the DG506 sixteen-channel CMOS multiplexer exhibits 250 ohms typically for analogue signals of ± 10 volts. For CMOS devices, the channel resistance is subject to typically 20% overall variation throughout the entire analogue signal range. PMOS devices have a wide variation of $r_{DS(ON)}$ with analogue signal. Data sheets, therefore, usually give the values of $r_{DS(ON)}$ at three different analogue signal levels together with typical graphs. Further information on the $r_{DS(ON)}$ performance of switches may be found in *Ref. 3.3,* section 3.13.

At high frequencies, the contributions of capacitance become significant. Such considerations become important for applications involving the switching of RF, video, or pulsed signals. The switch of Fig. 3.6—a DG171—has first order attenuation and phase shift characteristics typical of a passive RC circuit, as shown in Fig. 3.16.

Fig. 3.16 **First order attenuation and phase characteristics**



The attenuation characteristic is given as

$20 \log_{10}\left(\frac{V_L'}{V_{IN}'}\right)$ where $\frac{V_L'}{V_{IN}'}$ represents the transmission function and is given by

$$\frac{V_L'}{V_{IN}'} = \frac{\frac{R_L}{R_L + r_{DS(on)}}}{1 + j\frac{f}{f_u}} \qquad \text{and } f_u = \frac{1}{2\pi \frac{R_L \cdot r_{DS(on)}}{R_L + r_{DS(on)}} \cdot (C_A + C_L')} \text{ Hz.}$$

Typical performance curves for single switches only are shown in Figs. 3.17, 3.18 and 3.19. The additional OFF channels in a multiplexer modifies the values of R and C as described earlier and the new break-point frequency may be computed simply from $f = \frac{1}{2\pi RC}$ Hz.

Fig. 3.17 **DG171 ON performance**

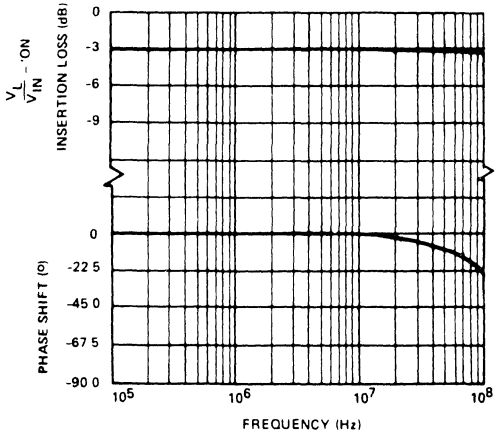


Fig. 3.18 **DG181 ON performance**

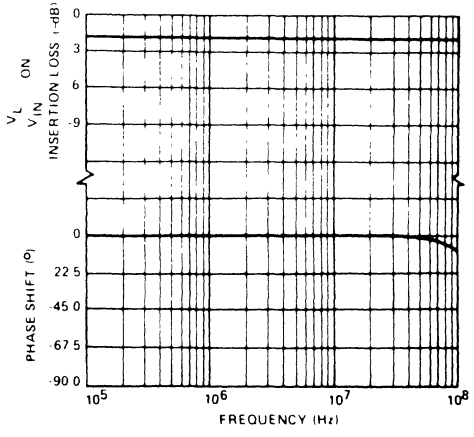
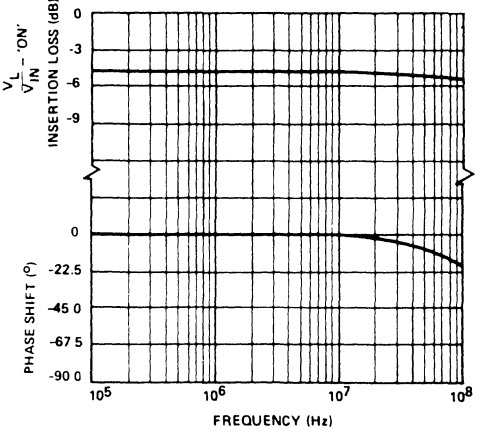


Fig. 3.19 **DG200 ON performance**



These loss effects will be experienced in both the multiplexer and its associated demultiplexer at the receiver end.

Figs. 3.17, 3.18 and 3.19 refer to 50Ω source and 75Ω load, and the measurements were made at low signal levels to eliminate r_{DS} modulation. Typical break frequencies are given in Table 3.3.

Table 3.3 Equivalent circuit values for three types of analogue switches

Switch Type	Device Number	f_u (min) (MHz)	Values Used			
			$r_{DS(on)}$ (Ω)	C_A (pF)	R_L (Ω)	C_L (pF)
PMOS	DG171	133	35	40	75	10
JFET	DG181	354	25	14	75	10
CMOS	DG200	140	60	24	75	10

Table 3.3 shows equivalent circuit values for single switches only. As mentioned earlier, multichannel multiplexers fabricated by the same process technology as a single switch will have larger $r_{DS(on)}$ and lower C_A values due to increased switch density on the silicon chips.

3.4.2 Channel Isolation

The subject of OFF isolation of single switches has been discussed in some detail in Chapter 2.

Isolation at low frequencies is defined by leakage components such as $I_{D(off)}$ and $I_{S(off)}$, while at higher frequencies it is principally dependent on capacitive coupling.

At low frequencies, error voltages will appear at the output due to the products of the OFF channel leakage currents and the load, and ON switch resistances.

Consider a two-channel multiplexer with one channel ON and one channel OFF, where the ON switch resistance is $r_{DS(on)}$, the load is R_L, and the signal source has resistance R_{GEN}. The leakage current from the OFF channel is split between R_L and ($r_{DS(on)}$ + R_{GEN}) as shown in Fig. 3.20

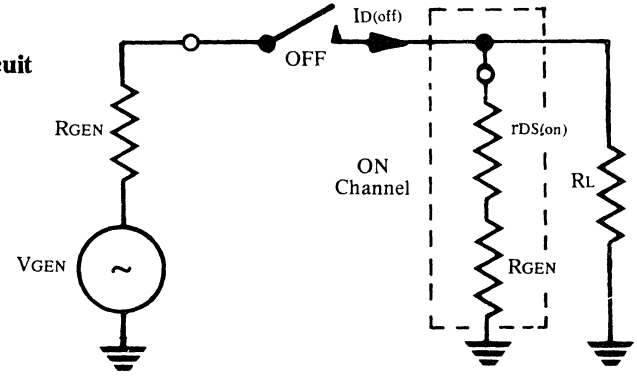


Fig. 3.20 **Equivalent circuit of OFF switch**

If $r_{DS(on)} + R_{GEN} \ll R_L$ (as is usually the case), then

$$V_{error} \approx I_{D(Off)} \cdot (r_{DS(on)} + R_{GEN}).$$

If $r_{DS(on)} + R_{GEN} \gg R_L$, then

$$V_{error} \approx I_{D(off)}. R_L.$$

If $r_{DS(on)} + R_{GEN} = R_L$, then

$$V_{error} = \frac{I_{D(off)} \cdot R_L}{2}$$

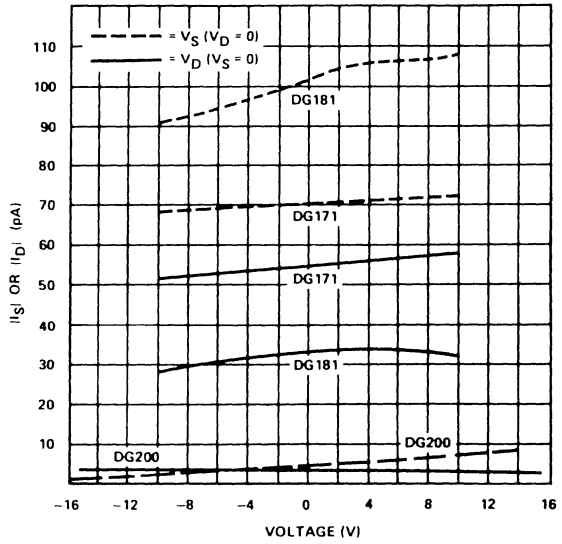
e.g. if $r_{DS(on)} = 100\Omega$, $R_{GEN} = 50\Omega$, $R_L = 10\Omega$, and $I_{D(off)} = I_{S(off)} = 1nA$ at 25°C, then under worst signal conditions,

$$V_{error} \approx (100 + 50) \times 10^{-9} \text{ volts} = 0.15\mu V.$$

For an output signal level of 15 volts this represents a low frequency crosstalk figure of —160dB.

Typical leakage performances for some single switches are shown in Fig. 3.21.

Fig. 3.21 **FET switch error currents**



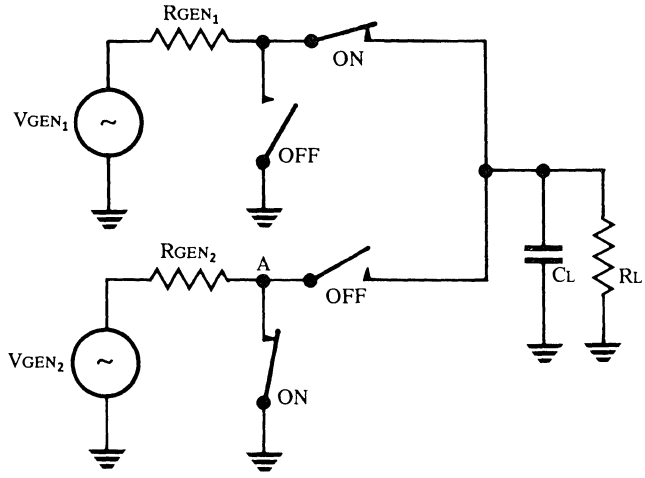
Where large numbers of channels are multiplexed, the leakage effects from all the OFF channels must be summed and the error signals can become significant, especially if devices are operated at high temperatures since leakage currents tend to double for every 10°C (approx.) rise in temperature.

At higher frequencies, the capacitive components define isolation, the leakage components being less significant. In addition, care must be taken with circuit layout to minimise capacitive strays between input and output terminals of the OFF channels. These strays may be combined to give a component C_{STRAY} appearing in parallel with C_{ds}, in Fig. 3.15, for the OFF switch. Inter-lead capacitances due to pin spacing on the package can be a significant contribution to C_{STRAY}.

In general, JFET switches tend to exhibit the best isolation performance, e.g. a single switch of the DG181 has about 60 dB typical isolation at 10MHz for a 50Ω source and 75Ω load. The CMOS DG200 and the PMOS DG 171 exhibit about 52dB and 48dB respectively, in the same circuit. Further data of ON and OFF performances together with equivalent circuit analyses are to be found in *Ref. 2.2,* section 3.13. In general, there is a trade-off involving the load resistor R_L. If R_L is decreased, OFF isolation is improved but there is an attendant increase in insertion loss.

Isolation may be improved by the use of multiple switch configurations. The simplest configuration to increase isolation is one which shunts all OFF channel analogue inputs to ground. This requires the shunt switches to be driven in antiphase to the main channel switches as shown in the two-channel example of Fig. 3.22—the 'L' configuration.

Fig. 3.22 **Inverted 'L' switching configuration**



In this situation, the analogue input to the OFF channel has been effectively shunted by a resistor of value equal to $r_{DS(on)}$ for the particular shunt switch used. The signal appearing at point A, therefore, becomes reduced to

$$\frac{r_{DS(on)}}{R_{GEN_2} + r_{DS(on)}} \cdot V_{GEN_2}$$

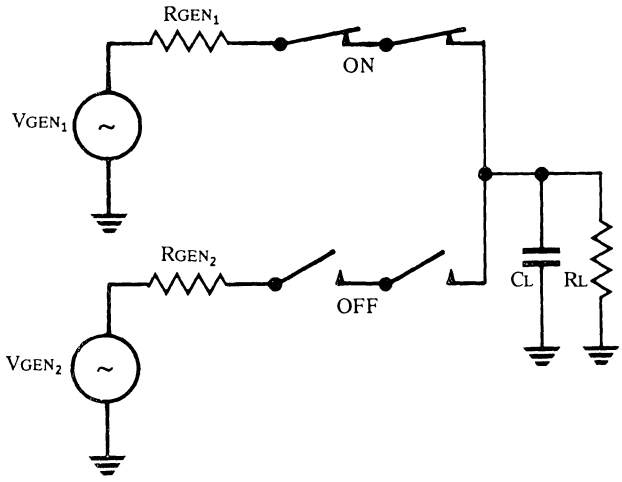
The ON channel switch characteristics are unaffected. This shunting principle may be used to great advantage where signals arrive at the switch inputs via transmission lines. The input impedance of an OFF switch is effectively infinite and as a result the transmission line may appear open. This implies unity reflection coefficient producing a switch input voltage of twice the generator voltage. The shunt configuration shown may be used to terminate the transmission line when the channel is open. Alternatively, if correct line matching is important, the shunt switch may have a resistor R_{PAD} in series with it so that

$$R_{PAD} + r_{DS(on)} = Z_0$$

where Z_0 is the characteristic line impedance, resulting in zero reflection coefficient and a switch input signal equal in level to the generator signal.

A greater improvement in isolation can be achieved by using two switches in series in each channel, the switches being operated in phase as shown in Fig. 3.23.

Fig. 3.23 **Circuit using two switches to improve isolation.**



Each ON channel now appears to have the equivalent circuit shown in Fig. 3.24 and each OFF channel has the form of Fig. 3.25. These forms must be taken into account when N channels are being multiplexed and adjustments made to the equivalent circuits of Figs. 3.8 and 3.12c which refer to PMOS technologies.

Fig. 3.24 **Equivalent circuit of two switches in the ON state**

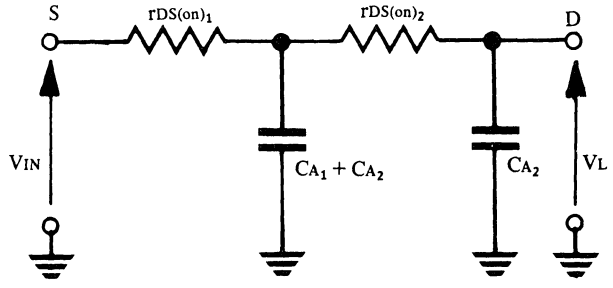
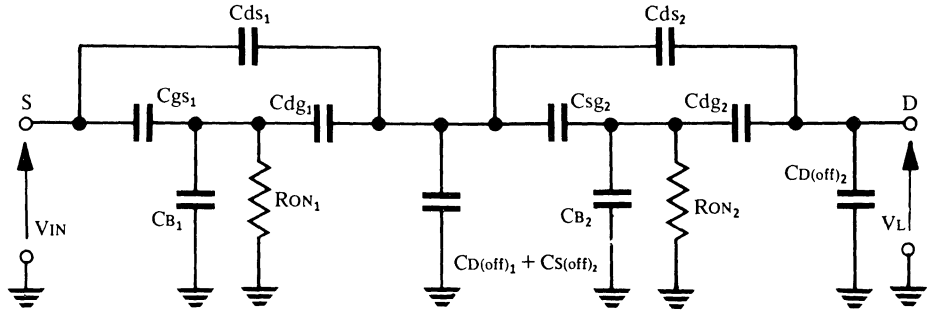
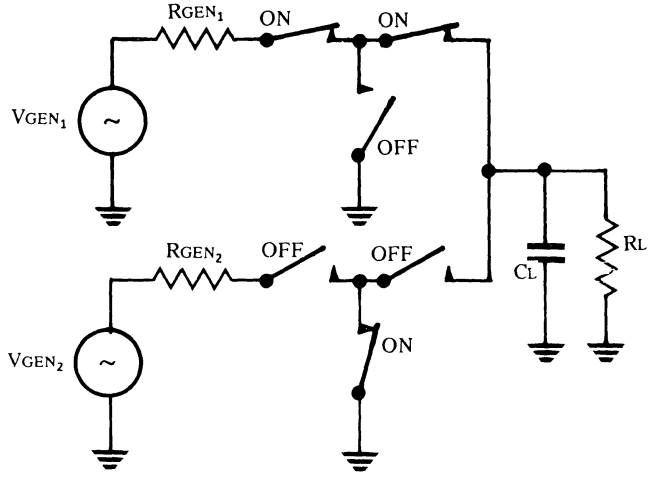


Fig. 3.25 **Equivalent circuit of two switches in the OFF state**



Even greater isolation may be achieved by use of a 'T' configuration as shown in Fig. 3.26. This requires 3 switches per channel.

Fig. 3.26 **'T' network switching configuration**



Even more complicated configurations can be envisaged but these are not commonly used because of increasing costs and complexity.

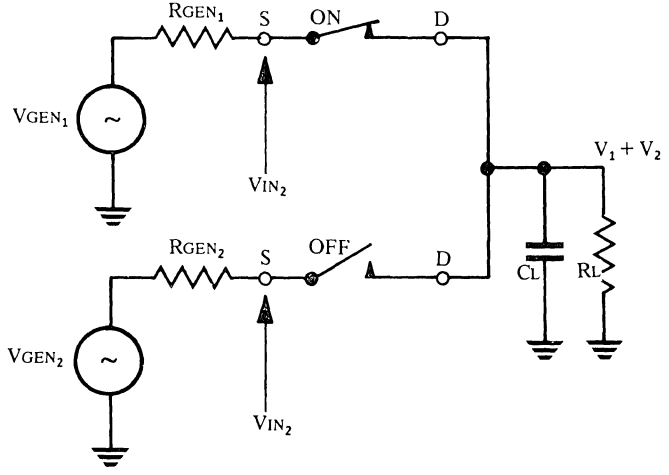
Large numbers of channels can be multiplexed using devices such as the DG506 16-channel CMOS multiplexer which has an integral decoder/driver arrangement, so that only one switch will be ON at any one time which precludes their use as multichannel shunt sections in the 'L' and 'T' configurations of Figs. 3.22 and 3.26.

3.4.3 Crosstalk Effects

Crosstalk occurs when spurious signals from OFF channels are superimposed on the wanted signal. There are several mechanisms which can cause this effect. A specific form of crosstalk is adjacent-channel crosstalk which, in a multiplexing context, occurs when unwanted components from one channel are superimposed on the signal of the channel which immediately precedes or follows it in the multiplexing sequence. The mechanisms are discussed in further detail below.

At d.c. and low frequencies, leakage paths through OFF channels exist primarily because of the finite OFF resistances of the switches. The value of $r_{DS(off)}$ may be very high—of the order of 10^{12} ohms. A more convenient way of quantifying this contribution is to define the leakage currents $I_{D(off)}$ and $I_{S(off)}$ through the switch. The error voltages producing crosstalk may then be determined as products of these leakages and circuit resistances, as shown in section 3.4.2. For low frequencies, an expression of crosstalk factor can be derived for the N channel multiplexer: a two-channel case is shown in Fig. 3.27.

Fig. 3.27 **Two channel multiplexer**



The OFF and ON switches may be represented by resistor values $r_{DS(off)}$ and $r_{DS(on)}$ respectively.

The desired signal V_1 appearing across the load due to V_{GEN_1} is given by

$$V_1 = \frac{V_{GEN_1} \cdot R_L \left(\frac{R_{GEN_2} + r_{DS(off)}}{R_L + R_{GEN_2} + r_{DS(off)} } \right)}{R_{GEN_1} + r_{DS(on)} + \frac{(R_{GEN_2} + r_{DS(off)}) R_L}{R_L + R_{GEN_2} + r_{DS(off)}}}$$

Because $r_{DS(off)}$ is very large, this expression can be simplified to

$$V_1 = \frac{V_{GEN_1} \cdot R_L}{R_{GEN_1} + r_{DS(on)} + R_L}$$

The undesired signal V_2 appearing across the load due to V_{GEN_2} is given by

$$V_2 = \frac{V_{GEN_2} \cdot R_L \left(\frac{R_{GEN_1} + r_{DS(on)}}{R_L + R_{GEN_1} + r_{DS(on)} } \right)}{R_{GEN_2} + r_{DS(off)} + R_L \left(\frac{R_{GEN_1} + r_{DS(on)}}{R_L + R_{GEN_1} + r_{DS(on)} } \right)}$$

The crosstalk factor is given by $\frac{V_2}{V_1}$, but further simplification may be made. Firstly, we can assume a crosstalk measurement with $V_{GEN_1} = V_{GEN_2} = V_{GEN}$ and $R_{GEN_1} = R_{GEN_2} = R_{GEN}$ and secondly, $r_{DS(off)}$ is large, so that

$$V_2 = \frac{V_{GEN} \cdot R_L \cdot \left(\frac{R_{GEN} + r_{DS(on)}}{R_L + R_{GEN} + r_{DS(on)}}\right)}{r_{DS(off)}}$$

Hence V_2/V_1 becomes

$$\frac{V_2}{V_1} = \frac{V_{GEN} \cdot R_L}{r_{DS(off)}} \cdot \frac{R_{GEN} + r_{DS(on)}}{R_L + R_{GEN} + r_{DS(on)}} \cdot \frac{R_{GEN} + r_{DS(on)} + R_L}{V_{GEN} \cdot R_L}$$

which gives

$$\frac{V_2}{V_1} = \frac{R_{GEN} + r_{DS(on)}}{r_{DS(off)}}$$

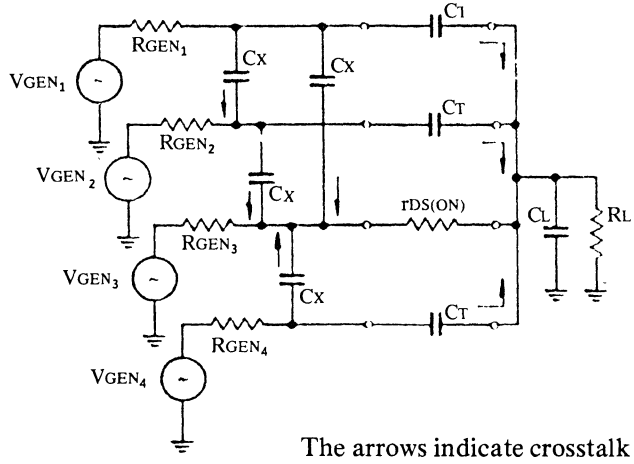
For a situation involving N channels, where $N > 2$, there will be $(N-1)$ OFF channels each assumed to have resistance $r_{DS(off)}$. The general approximation for the crosstalk factor then becomes

$$\frac{V_2 + V_3 + \text{----} V_N}{V_1} \simeq \frac{(N\text{-}1)\,(R_{GEN} + r_{DS(on)})}{r_{DS(off)}}$$

$r_{DS(off)}$ is not a normally specified parameter but the data sheet values for $I_{D(off)}$ and $I_{S(off)}$ may be used instead. If, for example, $I_{D(off)}$ is measured as 100pA for $V_{DS} = 10V$, the $r_{DS(off)}$ is 10^{11} ohms.

At higher frequencies, the capacitive effects discussed in section 3.3 become most significant. This includes the effective OFF switch capacitance C_{EQ} and circuit stray C_{STRAY}. In addition, there are capacitive effects between the channels which are functions of device geometry and the interpin capacitances of the device package. Additional capacitive components are due to circuit layout. These effects are shown in Fig. 3.28.

Fig. 3.28 **Crosstalk due to capacitive components**



The arrows indicate crosstalk leakage paths.

C_X and C_T are the capacitances which cause transmission of spurious crosstalk components into the input of the ON channel and the output path, respectively. In the majority of large scale multiplexing devices the input pins for many of the channels will be found adjacent to one another thereby contributing significant capacitive components. Some dual-in-line packages used for multiplexers can exhibit adjacent pin capacitances as high as 0·95pF. Some TO-100 metal-can packages, on the other hand, exhibit approximately 0·3pF between adjacent leads and can, therefore, be preferable for high isolation/low crosstalk applications.

A further cause of crosstalk exists in applications where the multiplexer is used as a sampler, i.e. the sampling theorem is being obeyed. The general statement of the Sampling Theorem is: "A signal whose highest frequency component is f_m may be accurately reconstituted from its samples provided that the samples occur at an average rate which is greater than or equal to $2f_m$".

For example, consider a 4-channel multiplexer sampling 4 signals of maximum frequency equal to 1kHz, then each channel must be sampled at a minimum rate of 2kHz resulting in multiplexer output samples at an 8kHz rate. In practice, the channel signal may have been applied to the multiplexer input via a filter and attenuated components may exist above 1kHz. Aliasing errors will, therefore, occur unless the sampling rate is, say, 2·5 kHz per channel.

The crosstalk mechanism is sample overlap between adjacent channels and comes from two primary sources. If the multiplexer does not exhibit perfect break-before-make switching action the rising and falling edges of the samples will overlap resulting in mutual interference between adjacent channels. In addition, even if multiplexer switching was "perfect", overlapping edges could still occur due to deficiencies in the transmission medium following the multiplexer. For example, the samples may be fed to a transmission line which has a Gaussian impulse response. If the samples are very narrow and the bandwidth of the line insufficient, the samples will be "smeared" according to the line response, and rising and falling edges may tend to overlap, resulting in crosstalk.

Straube *(Ref. 3.4)* has shown quantitatively how adjacent-channel crosstalk may be determined for sample-edge overlap and how the transmission system may be designed for a given crosstalk. A crosstalk figure of —60dB is usually an acceptable minimum.

3.4.4 Noise Effects

Many forms of 'noise' can occur in a multiplexing system and they are generated by a number of mechanisms. Any form of unwanted signal appearing at the multiplexer output may be considered as noise. Such unwanted signals may be thermal noise, crosstalk components, leakage currents, switching transients, thermal EMFs and transmission path pick-up.

3.4.4.1 Thermal Noise

Thermal or Johnson noise is generated by any resistance. The usual formula for

noise in resistance R is given by

$$\bar{e}_n = \sqrt{(4kTRB)} \text{ volts}$$

where k = Boltzmann's constant = 1.372×10^{-23} joules/°K

T = Absolute temperature

B = Noise bandwidth of measurement

In an *N*-channel switching system, the value of R will be due to the parallel arrangement of $r_{DS(on)}$ and (*N*-1) $r_{DS(off)}$, so R is approximately equal to $r_{DS(on)}$.

If $R = r_{DS(on)}$

$$\bar{e}_n = \sqrt{(4kTr_{DS(on)})} \text{ Volts}/\sqrt{\text{Hz}}$$

Hence for $r_{DS(on)}$ of 100Ω, at room temperature (T = 300°K)

$$\bar{e}_n \approx 1.28 \text{ nV} / \sqrt{\text{Hz}}$$

Integrating over a channel of noise bandwidth B_N = 40kHz gives

$$e_n \approx 0.26\mu\text{V}.$$

Noise bandwidth is related to the usual amplitude response bandwidth (i.e. bandwidth at — 3dB points) by the equation

$$B_N = \frac{\pi}{2} \cdot B_{-3dB}$$

3.4.4.2 **Isolation Effects**

Two other causes of noise, crosstalk and OFF switch leakages, are closely related and have been discussed earlier. These defects result in error voltages appearing on the multiplexed output signal.

3.4.4.3 **Switching Transients**

Other sources of noise are switching transients. These transients appear as spikes and can be transmitted into the analogue signal path. As mentioned earlier, a transmission medium can consist of a wideband line having a finite impulse response. Any spikes appearing on the line will be 'smeared' according to the line's impulse response and hence one spike can contribute errors to several adjacent channel samples. Switching transients are caused by charge transfer via the capacitive voltage dividers formed by circuit and device capacitances between the gate, source and drain terminals of the analogue switch, as indicated in the equivalent circuit diagrams. The usual cause of transients is due to the driver output signal at the gate terminals of the analogue switches (Chapter 2, section 2.6.3). Rapid changes in level at the source input of any analogue switch will also cause transients to be transferred to the output. Such changes are experienced when digital or video signals are being multiplexed. If ΔQ is the charge transferred out of the drain terminal into the load C_L then the magnitude of the transient at the load will be $\Delta V = \frac{\Delta Q}{C_L}$.

3.4.4.4 **Thermo-electric Effects**

Every electronic circuit will, of necessity, have a number of electrical 'joints'

many of which will consist of some form of bond between two dissimilar metals or metal alloys. Temperature differences will exist across the circuit and therefore a number of the joints will exhibit contact potentials and thermocouple effects. The voltages and currents so generated may give rise to errors if they lie in the signal path and therefore constitute a form of noise. The thermo-electric effects are dealt with in greater detail in Chapter 1.

3.4.4.5 Pick-Up

Pick-up in the transmission path is a further source of noise, e.g. if an unscreened transmission line is used it may run close to power lines and pick up 'hum' and spurious impulses.

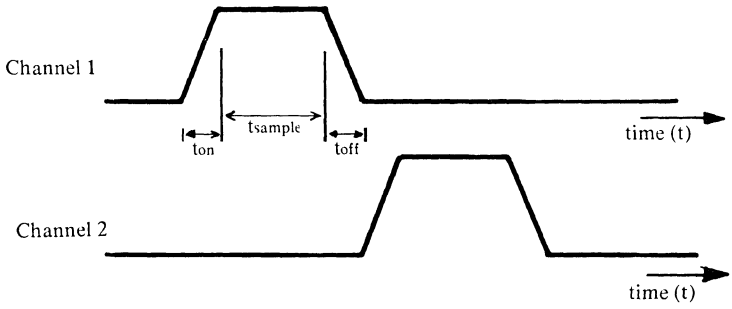
3.4.4.6 Clock-Jitter

Noise may also be transferred from the circuit generating the switching waveforms to the output of a multiplexer or demultiplexer. A pulse generator which is used to clock a multiplexer may exhibit "phase-jitter", i.e. frequency modulation noise sidebands. The output samples from the multiplexer will also display these noise sidebands.

3.4.5 Switching Speed

Fast switching operation may sometimes be difficult to achieve using the larger scale multiplexing devices. The greater the number of channels, the slower is the switching speed because of additional capacitance at the common node. Despite the slight reduction in speed and transmission efficiency the large scale switching devices are still attractive in terms of size, cost, and reduced system complexity. Switching speeds are important in multiplexing operation as the rising and falling edges of multiplexer output waveforms can, with slow devices, overlap to some extent resulting in adjacent-channel crosstalk similar to the line-contributed crosstalk discussed earlier. Commercially available multiplexers have t_{on} and t_{off} times of the order of 0.5μs. Channel switching rates must therefore be determined by three factors, t_{on}, t_{off} and t_{sample} as shown in Fig. 3.28.

Fig. 3.28 **Multiplexer switching waveforms**



$t_{on} = 1\mu s$; $t_{off} = 1\mu s$
and $t_{sample} = 1.3\mu s$ (according to application)

If, for example, t_{sample} is 1.3μs and t_{on} max and t_{off} max are 1μs each, then the maximum switching rate with no pulse-edge overlap is given as once every 3.3μs, or at a frequency of approximately 300kHz. For a multichannel system, this limits the number of channels and/or the maximum frequency components on any of the channel inputs, if the sampling theorem is to be obeyed. A higher switching rate may be employed if some adjacent-channel crosstalk can be tolerated.

The inherent slowness of the multichannel multiplexers can be overcome by using a multilevel switching technique known as supermultiplexing. This is referred to in *Refs. 3.6 and 3.7,* section 3.13, and will be discussed in further detail later.

3.5 PRINCIPAL APPLICATION AREAS OF MULTIPLEXERS

Multiplexer applications exist in many fields, but there are two principal categories of useage:

1) Communications—specifically communication involving voice and/or tone communication over lines or radiopaths.
2) Telemetry—including simple monitoring of system variables, local or remote, and process control which is a closed-loop operation requiring monitoring, decision making, and feedback control to alter system variables. This category also includes telemetry over lines or radiopaths. Telemetry is discussed in considerable detail in *Ref. 3.5,* section 3.13.

3.5.1 Communications Application

An example of a communications application involving multiplexing is the digital telephone system. In this system, a number of telephone channels carrying speech signals are multiplexed and fed to an Analogue-to-Digital converter which employs some form of PCM encoder. The voice signals may be bandwidth limited to 3·3kHz and therefore may be sampled at an 8kHz rate, i.e. one sample every 125μs. If there are, say 32 voice channels to be multiplexed, the maximum available aperture time (interval that a channel sample may occupy) will be 3·906μs. The PCM encoded output must occupy a time interval less than or equal to this aperture time. The reverse process would be performed at the receiver and the voice signals reconstructed from the analogue samples by low-pass filtering.

3.5.2 Telemetry Applications

Telemetry offers many applications for multiplexers. Consider, for example, a satellite telemetry system with basic transducers to measure outer skin and internal temperatures, solar battery voltage, fuel cell voltages, battery charge or discharge currents, cosmic ray intensity etc. The outputs of these transducers would be in analogue form and may require some preconditioning (filtering, rectifying, amplifying etc.) before multiplexing. The multiplexed samples may then be recorded on a FM tape recorder. At some later, pre-arranged time, when the satellite is within communicable range of a ground monitoring station, the information may be read off the tape at high speed (under ground station control) and the output samples used to frequency modulate a subcarrier of the main satellite signal.

At the receiving end, a frequency discriminator is used to extract the samples which are then demultiplexed to the correct output channels. This is a simple open-loop monitoring system.

A closed-loop telemetry system is, in essence, a process control system usually involving some form of decision maker within the loop. This decision maker may be anything from a simple go/no-go type of switching circuit to a continuously variable system under computer control. An example of such a system is a remote controlled pumping station, which may be on a gas, oil chemical, petroleum, or water pipeline. The functions being monitored in such a system may be, flow-rates, temperatures, viscosities, suction and discharge pressures at pumps, tank levels etc. Transducers are used to produce analogue signals which may be pre-conditioned prior to multiplexing. The multiplexed outputs may then be encoded into digital form by an A-to-D converter and transmitted via a line to a minicomputer. The computer will examine the data and make decisions dependent on the functions which must be controlled.

Control signals would be output by the computer in digital form and returned via a line to the remote site where a D-to-A converter would convert the signals into analogue form. These analogue samples would then be demultiplexed to various control points such as valves, coolant supplies, pumps etc. The number of possible applications for multiplexing in telemetry is very large, as indicated in *Ref. 3.5,* section 3.13. The following section will discuss methods of using analogue gates in multiplexing applications. Although multiplexing is dealt with specifically, demultiplexing is also implied as it simply requires the role of the multiplexer to be reversed.

3.6 PRIMARY REQUIREMENTS OF ANALOGUE SWITCHES AS MULTIPLEXERS

Analogue switches are available in a variety of configurations suitable for multiplexing. In applications where adjacent-channel crosstalk must be minimised, fast rise and fall times, and break-before-make switching action are essential.

Other desirable features are compatibility with existing logic families, wide analogue range, and low ON resistance for low errors and low noise. The application will decide the priority of these parameters.

3.7 ANALOGUE SIGNAL CHARACTERISTICS

The input analogue signals will often be produced by transducers of various forms; e.g. speech signals are produced by a microphone which may be a magnetic, piezoelectric, or capacitive device.

Common transducers employ a variety of principles such as resistance, inductance, capacitance, or reluctance variation.

The simplest resistance transducer is the strain gauge which measures structural strain. It is a wire element bonded to a structure so that any strain will alter its physical characteristics thereby producing a resistance change. The gauge may be connected in a bridge circuit which has a.c. or d.c. excitation. If resistance changes are small, the bridge will usually be an a.c. bridge, as the small output signals may easily be amplified.

Because of the wide variety of transducer types that are available, the input signals to the multiplexer may take many analogue forms e.g. high frequency or d.c., high level or low level, voltage or current etc., and may require some form of pre-conditioning to produce a signal acceptable for multiplexing.

3.7.1 Low Level Signals

Where low level d.c. signals are produced, some form of signal processing may be necessary. As mentioned previously, switching transients can result in error signals appearing at the multiplexer output. Therefore if the output signal monitor is sensitive to these transients it may be necessary to incorporate a filter at the multiplexer output. Alternatively, small d.c. signals could be amplified to such levels as to make these switching errors negligible. Different values of fixed gain may be used in each channel as this can be compensated for by equivalent attenuation at the demultiplexer output in the receiver. Where all the inputs are low level d.c. signals of the same order of magnitudes, it may be cheaper to employ post conditioning and reduce the error signals by the method(s) referred to in Chapter 4. Signals from transducers that produce a.c. outputs often require some filtering and/or amplification. In simple a.c. bridge circuits, the a.c. signal will be modulated at a low frequency dependent on the physical phenomenon being measured and the envelope of the signal will contain the required information. Any stages of gain are therefore followed by a rectifier-filter combination to produce a suitable analogue input to the multiplexer. The d.c. amplifiers will normally be more rigorously designed than the a.c. amplifier as factors such as drift and offset must be taken into consideration in d.c. amplifier design. The a.c. rectifier may often be a precision rectifier involving an operational amplifier with the rectifying element in the feed-back loop. A.C. amplification is generally more easily and cheaply achieved than d.c. amplification.

3.7.2 High Level Signals

The majority of existing PMOS IC multiplexers will switch analogue voltages in the range of +10 volts to —10 volts with the common line of the multiplexer considered as a zero reference. CMOS multiplexers will handle +15 volts to —15 volts. Typical devices are the DG503—an 8-channel PMOS multiplexer, the DG508—an 8-channel CMOS multiplexer and the DG506 which is a 16-channel CMOS multiplexer.

Larger signals must be attenuated prior to the multiplexer. This attenuation can be compensated for with an equal degree of gain after demultiplexing. From these points it is clear that high and low a.c. and d.c. signals may be handled by the same multiplexer with suitable signal processing.

3.7.3 Differential Signals

Signals produced by bridge circuits consist of two components, a common-mode signal which is large, and a difference signal which is small. The difference signal is the signal which conveys the measurement information and can be referred to the multiplexer ground reference point by means of a differential amplifier with single-ended output. The common-mode signal therefore becomes lost.

Where all the multiplexer inputs are from differential sources and of the same order of magnitude it could be prohibitive in terms of cost and circuit size to provide a separate pre-conditioning amplifier in each channel. An alternative method would be to use a differential multiplexer such as the DG507 8-channel CMOS device (16 analogue switches). The two output common lines may then be fed to a single post-conditioning differential amplifier.

Single-ended signal sources may still be accommodated by the differential multiplexer, one of the inputs being left open or connected to any suitable reference point such as ground.

3.8 TECHNIQUES USED IN MULTIPLEXING

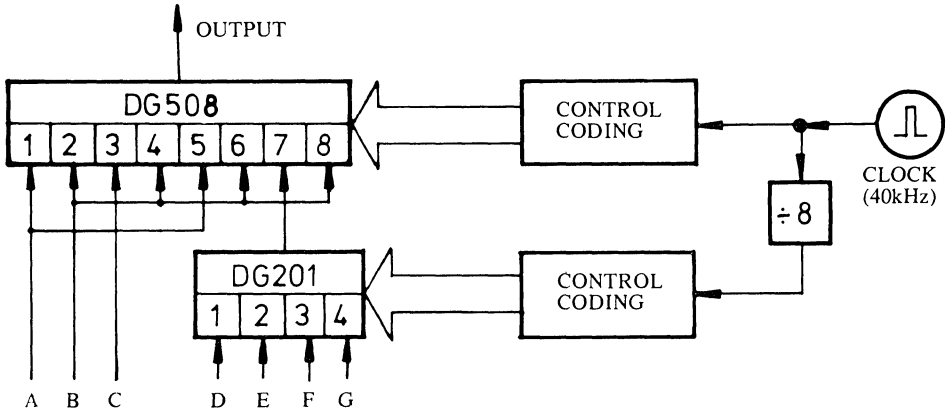
3.8.1 Simultaneous Monitoring using Multiplexing

The multiplexing process operates in "real-time", that is, samples are taken sequentially and represent the analogue input signal at the instant the switch is closed. In some applications, it may be necessary to monitor several signals simultaneously for comparison purposes. This may be achieved by using sample-and-hold circuits at each input channel to the multiplexer. One clock pulse may then be used to sample all the channels simultaneously. The samples are then held for the multiplex operation that follows shortly after. This is another form of pre-conditioning.

3.8.2 High and/or Variable Multiplexing Rates

In some multiplexing operations, it may be necessary to multiplex slowly varying signals and rapidly varying signals on to one common transmission line. For example, consider the case shown in Fig. 3.30.

Fig. 3.30 **Multiplexing system for multifarious signals**



Signals are presented at A, B, C, D, E, F, and G and there are twelve multiplexer inputs shown. The signal in channel B may have been band-limited to 8kHz and for the Sampling Theorem to be obeyed, should be sampled at a rate of at least 16kHz. Similary, A may have frequency components up to 4kHz; C up to 2kHz; and D, E, F, and G up to 500 Hz.

For both multiplexers, samples are taken from each input at a rate equal to the clock frequency divided by the number of multiplexer channels. Hence in Fig. 3.30 the sampling rates are 5kHz per channel for the DG508 and 1·25 kHz per channel for the DG201.

Signal C is sampled at the 5kHz rate, whereas signal A is being applied simultaneously to two inputs and is being sampled at a regular 10kHz rate. The

signal A is applied to the inputs 1 and 5 so that the sampling rate is uniform, that is, there is a constant time interval between each A sample. By the same method, signal B is being sampled at a regular 20kHz rate. In addition, signals D, E, F and G are being sampled at a 1·25kHz rate, which is also regular. The use of several inputs in parallel to increase the sampling rate results in no significant alteration to the multiplexing characteristics. However, the use of an additional multiplexer to reduce the sampling rate does have a significant beneficial effect. The use of "multilevel" multiplexing sometimes known as Supermultiplexing, is discussed in more detail later.

3.8.3 Multiplexing Pulsed Signals

Logically encoded signals, reference pulses or any similar types of signals may be multiplexed along with the usual analogue inputs. Such signals may have previously been obtained from say, a PCM encoder. The sampling aperture must be wide enough to embrace all the digital information and the switch must be able to handle the pulse edges or signal slew rate. This latter point is discussed in more detail in *Ref. 2.2.*, section 3.13.

3.8.4 Synchronisation and Channel Identification

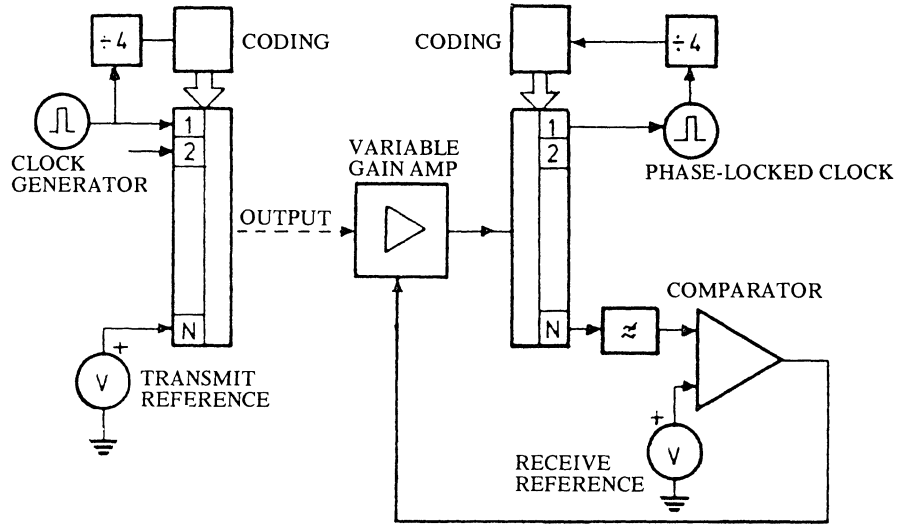
Synchronisation can be achieved by various methods. One simple method is to assign one multiplexer channel for synchronisation, the channel input being a train of clock pulses from the master clock. This constitutes a digital group which may be multiplexed in the same way as for a PCM code group. Every time the sync. channel is sampled, a "burst" of clock pulses is transmitted and used at the receiving end to phase-lock the receiver clock. Circuitry can be incorporated at the receiver to detect this group of pulses and assign it to the correct demultiplexer output channel, thus achieving channel identification. Another method involves assigning one or more input channels to carry "unique" signals. For example, if all the other channel inputs are positive voltages, the assigned channels may carry fixed negative voltage inputs. Circuitry at the receiver may be used to detect the occurrence of these unique samples, and their rate, and thereby achieve synchronisation and channel identification.

Synchronisation may also be achieved by phase-locking the transmitting and receiving clocks to a radio frequency standard. There are several such standards, e.g. Droitwich (UK) transmits on 200kHz, and commercial receiver units are available which use logic circuitry and phase lock techniques to produce TTL compatible outputs at useful reference frequencies such as 100kHz, 1MHz and 10MHz etc. In designing such a synchronised system account must be taken of delays over radio and line paths. The clock generators may be voltage controlled crystal oscillators followed by logic dividing/interfacing circuitry.

3.8.5 Calibration

Overall system calibration may be achieved by assigning one multiplexer channel to carry an accurate reference signal. A stable voltage level from say, a standard cell may be used. At the receiving end the demultiplexed reference signal may be compared with an identical voltage reference and any error may be compensated for by adjusting receiver channel gains. If the receiver demultiplexer is preceded by a buffer amplifier, the gain of which is variable, any attenuation errors in the whole system may be automatically compensated for by the use of feedback, as shown in Fig. 3.31.

Fig. 3.31 **Error compensation**



The schematic diagram shows an *N*-way multiplexer whose channel 1 input is taken from the "transmitter" clock. The clock rate is four times the multiplexing rate. Hence, during the channel 1 sampling interval, a group of four pulses appears at the output. At the receiving end, decoding logic may be used to detect this pulse group for defining the channel 1 synchronism and for locking the receiving clock frequency until the next pulse group appears.

The compensation method of Fig. 3.31 indicates a means of synchronisation described earlier. This method assumes that all the switches of the multiplexer and all those of the demultiplexer are identical in characteristics. Modern monolithic multiplexers are very good in this respect, as all the switch sections on a single multiplexer have the same geometrical characteristics and are formed simultaneously by the same diffusion processing. For example, typical DG506 samples show average $r_{DS(on)}$ values of around 250 ohms with spreads of around 6 to 8 per cent, for switches under identical bias conditions, as given in the data sheet.

3.8.6 Output Conditions

If the multiplexed output samples are low level, they may require amplification before being fed to a transmission path. Likewise, if a differential multiplexer was used, a differential amplifier may be required to interface the samples to a single line. The amplifier will be the multiplexer load and should exhibit a fast slew rate if adjacent channel crosstalk is to be minimised. In addition, the impulse response should be such that no "ringing" or "overshoot" occurs on the samples. If the multiplexer feeds a high accuracy PCM modulator, a fast sample-and-hold circuit may be necessary between the multiplexer and the modulator.

3.9 SUPERMULTIPLEXING (Multilevel multiplexing)

Supermultiplexing refers to a tandem arrangement of multiplexers, as shown in

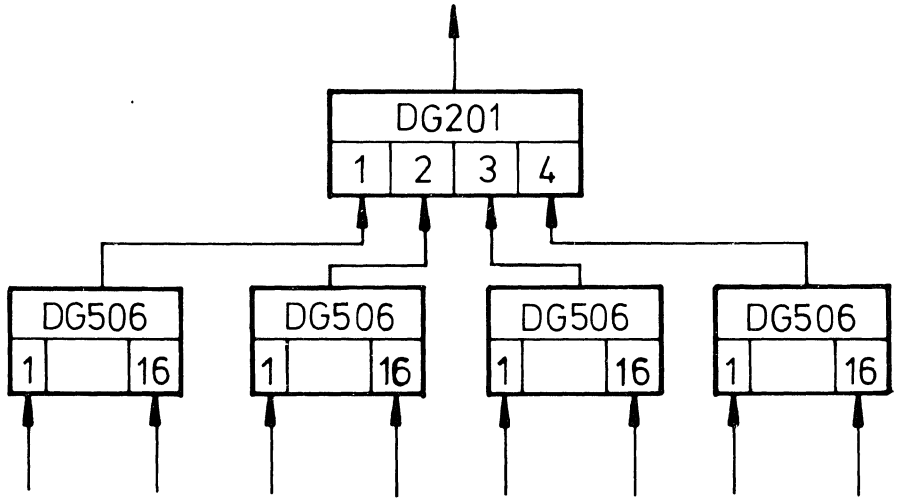
Fig. 3.32. There are a number of reasons why supermultiplexing might be employed to advantage:

1) to increase the number of channels which can be multiplexed,
2) to reduce loading effects of OFF channels where a large number of channels are multiplexed,
3) to increase the effective switching speeds of multichannel multiplexers and so increase efficiency,
4) to reduce crosstalk and
5) to increase isolation.

3.9.1 Increasing Channel Capability

Consider the situation shown in Fig. 3.32.

Fig. 3.32 **64-channel multiplexer using supermultiplexing**



The logic control circuitry is not indicated, for the sake of simplicity.

The system of Fig. 3.32 represents a 64-channel multiplexer achieved using four DG506s and only one other switching device, a DG201 which behaves like a "multiplexing buffer". The system could be achieved without using the DG201 and by combining the outputs of the DG506s, but this would give rise to a number of disadvantages which are made apparent in the following sections. The DG201 effectively isolates each DG506 from the others.

3.9.2 Reducing Loading Effects

The equivalent circuits of the N channel multiplexer, given in Figs. 3.13 and 3.15, show that in the view of the ON channel there is a load consisting of the normal R_L and C_L components and an additional capacitance equal in value to $(N\text{-}1)C_T$. For a 64-channel system this would be $63C_T$. For the DG506, C_T is approximately 5pF giving an additional node capacitance of approximately

160pF. By using a DG201 "buffer", as indicated in Fig. 3.32, each DG506 has its output node capacitance reduced to 40pF approximately, but the load capacitance, which defines switching speeds, will be only C_L + 14pF, where the 14pF represents a typical output node capacitance for the DG201.

3.9.3 Increasing Effective Switching Speeds and Efficiency

Section 3.9.2 indicates that an improvement in switching speed can be achieved by supermultiplexing. Consider the 32-channel system of Figs. 3.33a and 3.33b.

Fig. 3.33a **32 Channel Supermultiplexer**

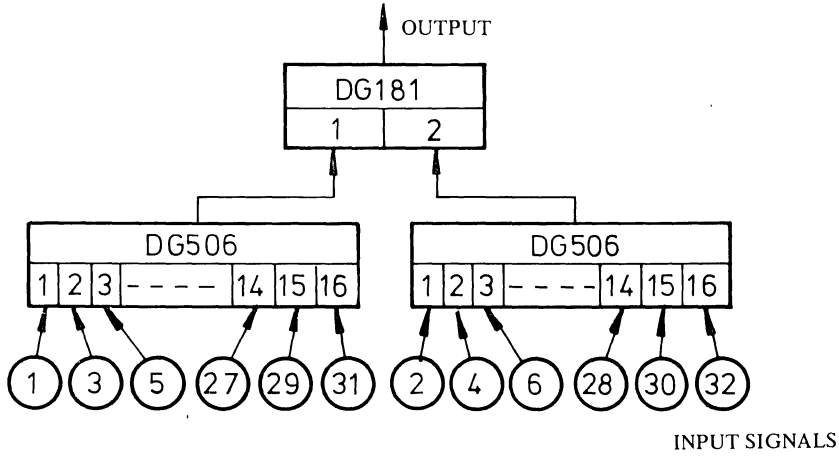
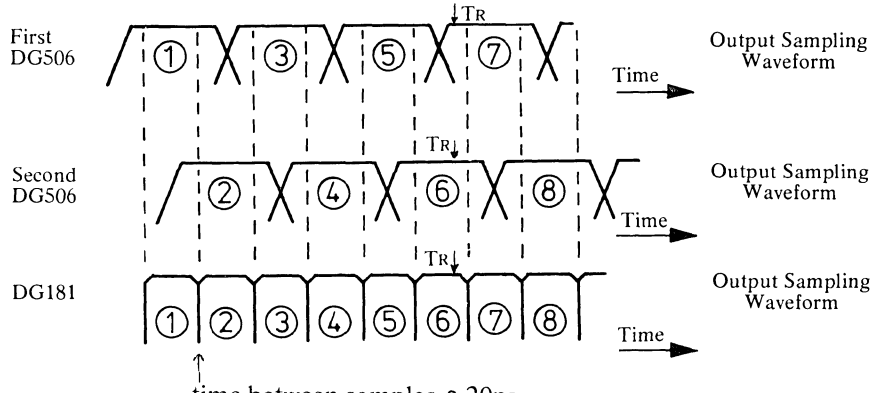


Fig. 3.33b **Switching waveforms** Edge slopes are exaggerated for clarity



The fast switching times and break-before-make action of the DG181 reduce the time between samples to approximately 20ns, as compared with the corresponding time in a single DG506 stage of up to 2μs. Hence, by using supermultiplexing, the effective multiplexer speed is increased and the efficiency is greatly improved. A measure of multiplexing efficiency may be developed from consideration of the switching waveforms of Fig. 3.34.

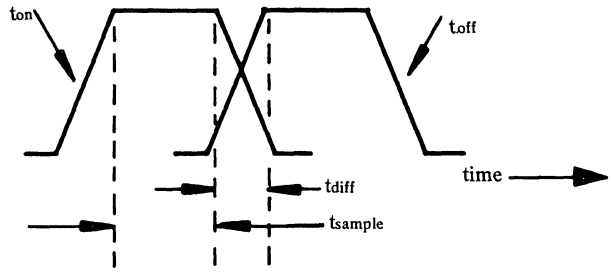


Fig. 3.34 **Switching efficiency of a multiplexer**

Efficiency may be defined as

$$E_{mux} = \frac{t_{sample}}{t_{diff} + t_{sample}} \times 100 \text{ percent}$$

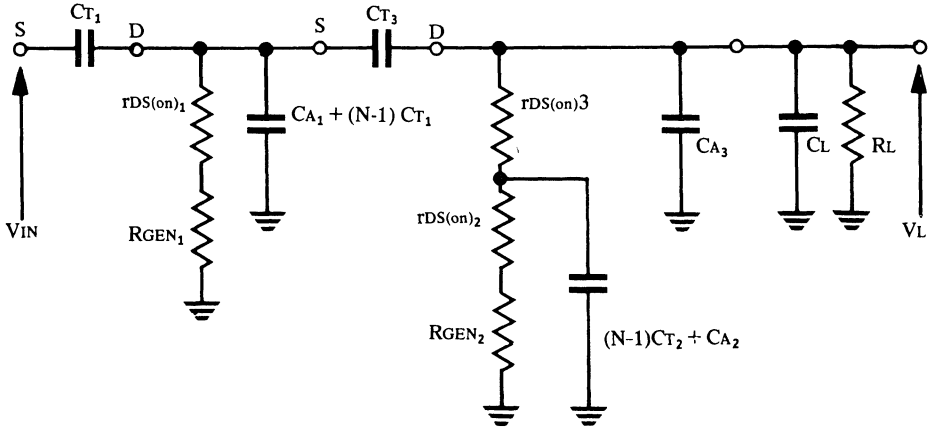
where t_{sample} is a system requirement. For two DG506s in a normal multiplexing mode with $t_{sample} = 4\mu s$ and $t_{diff} = 2\mu s$, then $E_{mux} = 67\%$. For two DG506s in Supermultiplexing mode with a DG181. $t_{sample} = 4\mu s$ and t_{diff} 20ns, then $E_{mux} = 99.5\%$.

The multiplexing efficiency of a supermultiplexing system is thus determined by the efficiency of the last "multiplexing buffer" stage.

3.9.4 Reducing Crosstalk

The various mechanisms contributing to crosstalk have been discussed previously in section 3.4.3. A simplified equivalent circuit for a supermultiplexer employing multichannel multiplexers, such as the DG506, and a JFET analogue switch, such as the DG181 is indicated in Fig. 3.35. The input voltage in this instance is applied to one of the OFF channels shown in Fig. 3.33a.

Fig. 3.35 **Equivalent circuit of Supermultiplexer viewed from OFF channel**



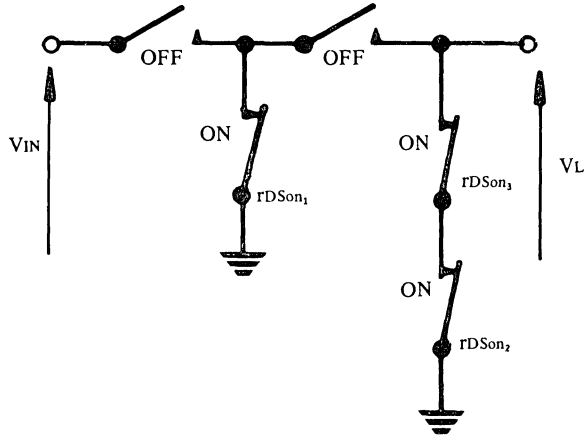
The equivalent circuit refers to the time interval over which switch conditions are static, e.g. at point T_R of Fig. 3.33b. It does not apply to the channel switching intervals (t_{diff}) of the DG506 or DG181 where crosstalk determination is extremely complicated.

The r_{DS}, R_{GEN}, C_A and C_T components shown are the effective contributions of the various channels as described in sections 3.2.4 and 3.2.5. $r_{DS(on)_1}$, R_{GEN_1}, C_{A_1} and C_{T_1} are due to one multiplexer and $r_{DS(on)_3}$, C_{A_3} and C_{T_3} are due to the DG181 switch. Their presence creates a shunting effect which helps to reduce crosstalk. R_{GEN_2} represents the signal source in the main ON channel. The usual capacitive strays are still present around the DG506 multiplexers but their effects are reduced because of the OFF stage isolation of the DG181. If the secondary multiplexer has additional channels, as does the DG201, further crosstalk would be caused by stray components in this device but the crosstalk arising from this mechanism would still be low because the DG201 is only a four channel device. The DG181 is a fast switch and sample overlap is negligible when this device is used in the manner described in section 3.9.3. Adjacent-channel crosstalk due to pulse overlap is therefore much reduced by supermultiplexing.

3.9.5 Increased Isolation

The circuit of Fig. 3.36 is the basic switch arrangement corresponding to the equivalent circuit of Fig. 3.35.

Fig. 3.36 **Switch arrangement viewed from supermultiplexer OFF channel**



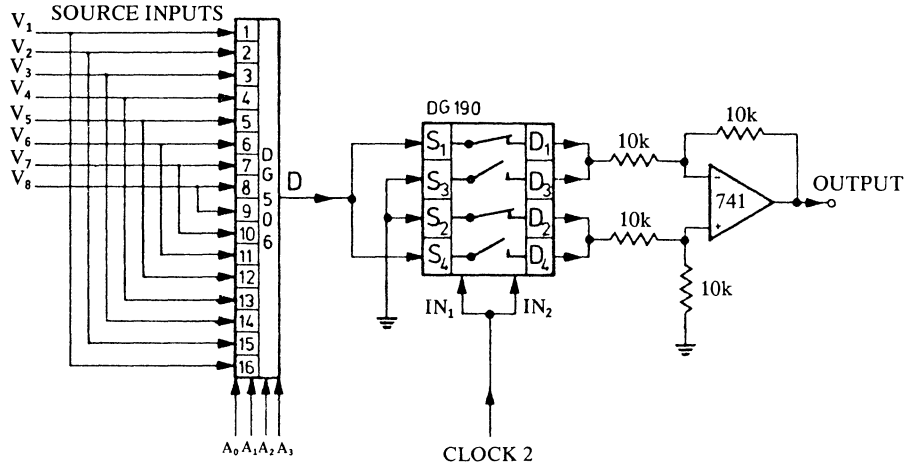
The equivalent switch arrangement represents the circuit of Fig. 3.33a and applies to the interval over which switch states are static (e.g. point T_R of Fig. 3.33b. This is simply a 'T' arrangement shunted at the load by the main signal ON channel. Isolation with this arrangement will be very high.

3.10 EXAMPLES OF MULTIPLEXER APPLICATIONS

3.10.1 A simple waveform synthesiser

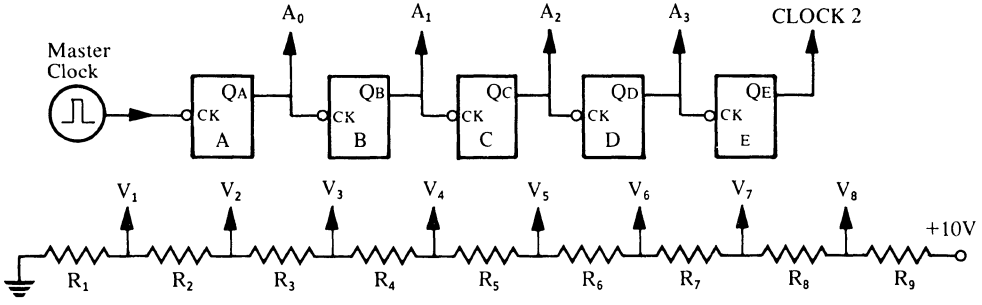
A simple illustrative example of the use of multiplexers is given in Fig. 3.37a. The configuration shows a waveform generator which gives a sinusoidal waveform approximated by 32 amplitude steps per cycle. Only 8 reference voltages are required for this function.

Fig. 3.37a **Simple sine function synthesiser**



The supplies for all devices are ± 15V and + 5V and 0V for logic references. The logic and analogue inputs are shown in Fig. 3.37b.

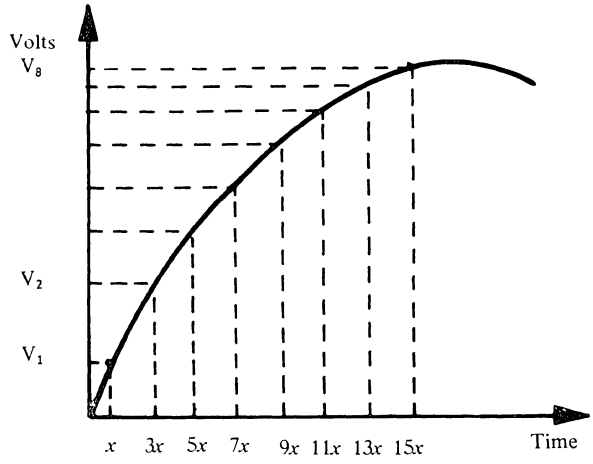
Fig. 3.37b **Logic and analogue references**



Devices A to E represent J-K flip-flops in a ripple-through binary divide configuration, i.e. J and K inputs at logic '1' and Q outputs toggling on negative-going edges of clock inputs.

With a regular master clock input applied the resistor values R_1 and R_9 must be adjusted to give the voltages shown in Fig. 3.38.

Fig. 3.38 **Sinewave reference points**



where x represents $\frac{\pi}{16}$ radians. The values for V_1 to V_8 are given in Table 3.4

Table 3.4

Analogue Input	Radian Reference	Sine Value	Input (volts)
V_1	$\frac{\pi}{16}$	0·0980	0·980
V_2	$\frac{3\pi}{16}$	0·2903	2·90
V_3	$\frac{5\pi}{16}$	0·4714	4·71
V_4	$\frac{7\pi}{16}$	0·6344	6·34
V_5	$\frac{9\pi}{16}$	0·7730	7·73
V_6	$\frac{11\pi}{16}$	0·8819	8·82
V_7	$\frac{13\pi}{16}$	0·9569	9·57
V_8	$\frac{15\pi}{16}$	0·9952	9·95

The 8 levels from $\frac{\pi}{16}$ to $\frac{15\pi}{16}$ radians in steps of $\frac{\pi}{8}$ are thus generated.

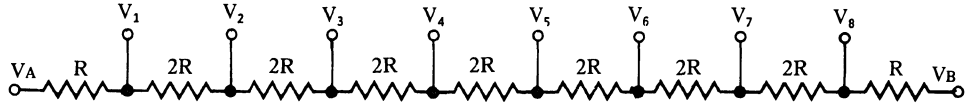
The source inputs are connected in the way shown in Fig. 3.37a to reverse these 8 steps over the region $\frac{17\pi}{16}$ to $\frac{31\pi}{16}$ radians. The DG190 then receives a clock input

signal which causes the inputs of the 741 buffer amplifier to be interchanged and the amplifier switches from non-inverting mode to inverting mode, and the sampling process is repeated over the region of $\frac{33\pi}{16}$ to $\frac{63\pi}{16}$ radians. In this way both positive and negative halves of a waveform may be generated.

With a regular sampling pattern and all 16 input levels defined various different repetitive waveforms may be generated. The DG506 will handle input samples in the range of ±15V and for the mode shown in Fig. 3.37a, the waveform repetition frequency will be given by the frequency of the clock divided by 32.

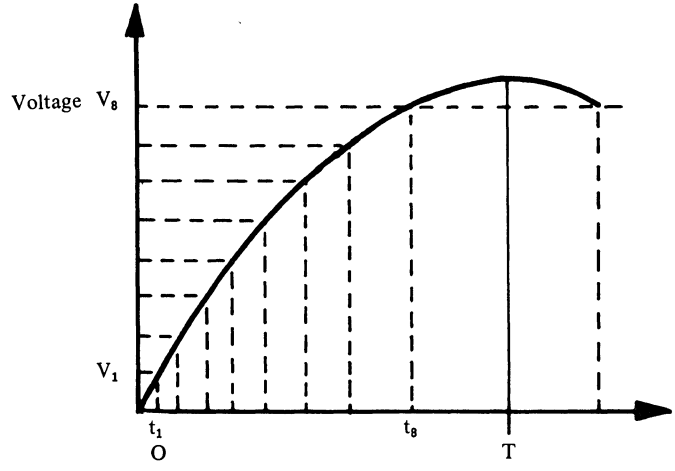
Simple experiments have been performed linking the basic unit of Fig. 3.37a to a computer to generate waveforms. A program was written for a mini-computer which generated well defined 'SYNC' pulses at user-definable intervals. The 8 reference levels V_1 to V_8 were obtained from a linear resistive divider as shown in Fig. 3.39 and the interval between these samples could be controlled by linking the 'SYNC' output of the computer to the master clock imput of the unit.

Fig. 3.39 **Linear voltage division**



If V_A = 0V and V_B = +10V a simple sinewave function can be generated by arranging the samples into the simple timing relationship of Fig. 3.39.

Fig. 3.40 **Sinewave reference points**



If the region of 0 to $\frac{\pi}{2}$ radians (0° to 90°) represents a unit time interval T, then t_1 to t_8 are given in Table 3.5 as decimal fractions of that interval.

Table 3.5

Time Point	Equivalent Value	Voltage Level (volts)
t_1	0·0441T	0·625
t_2	0·1261T	1·875
t_3	0·2039T	3·125
t_4	0·2952T	4·375
t_5	0·3820T	5·625
t_6	0·4857T	6·875
t_7	0·6063T	8·125
t_8	0·7783T	9·375

With 16 continuously variable input levels and a programmable computer clock input, a greater variety of different repetitive waveforms may be synthesised. If required, supermultiplexing may be used to give the advantages outlined in sections 3.9.1 to 3.9.3. A self-contained waveform synthesiser could be built using these techniques in conjunction with one of the many commonly available mircoprocessor integrated circuits.

3.10.2 Telephone Switching using a Supermultiplexer

A telephone switching application of multiplexing was briefly mentioned in section 3.5.1 and is discussed in detail in *Ref. 3.7*, section 3.13. The multiplexing system is required for feeding a Pulse Code Modulator which converts each signal sample into a digitally coded group. The sampling rate is determined by the input signal bandwidth and obeys the Sampling Theorem previously defined. The sample width will be determined by the sampling rate and the number of channels being sampled. If the sampling rate in each voice channel is 8kHz, then the sample frame time is 125μs and the sampling interval allowed for each channel is 125/32 or 3·906μs. Roberts and Jenkins *(Ref. 3.7)* used four DG501 8-channel multiplexers for the purpose. These devices have a relatively low multiplexing efficiency with a switching time between channels of the order of 1μs. In a sample interval of 4μs, this would probably result in a poor crosstalk performance. In addition to the slow switching speeds, there would be an additional switching delay caused by the increased output node capacitance resulting from combining the four DG501 outputs. For four DG501s, this additional delay would be about 0·2μs. The remedy for this problem is to use supermultiplexing with clock timing sequences arranged to give fast switching edges as described in section 3.9. Roberts and Jenkins employed two DG181 2-channel switches for the secondary multiplexing operation. The DG181 has switching speeds less than 150ns and gives a considerable improvement in crosstalk and multiplexing efficiency.

The basic schematic for the multiplexer is shown in Fig. 3.41 and the timing sequence given in Fig. 3.42. Further details may be obtained by consulting *Ref. 3.7*, section 3.13.

Fig. 3.41 **32 channel telephone switching network**

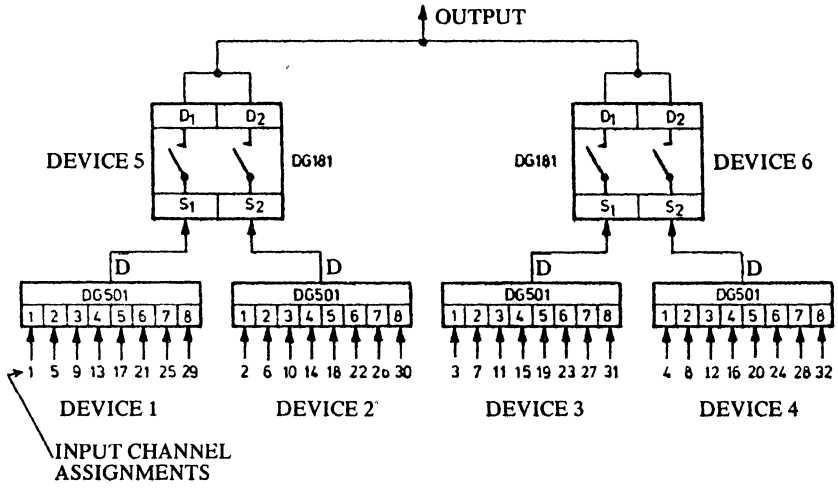
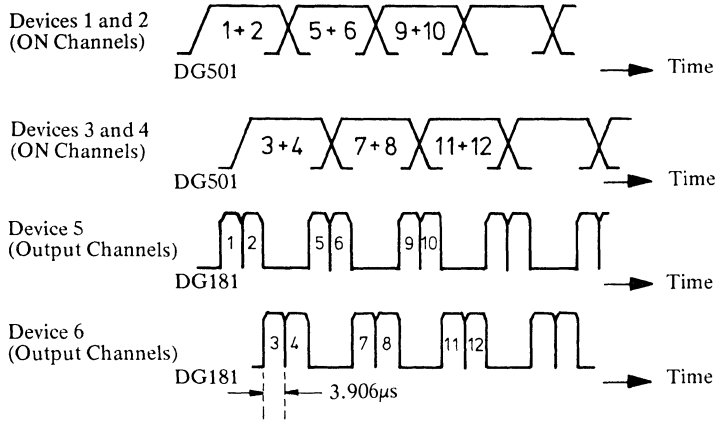


Fig. 3.42 **Timing sequence for Fig. 3.41**



The devices 1 and 2 have their BCD clock logic inputs wired in parallel as do devices 3 and 4. Complete logic and timing diagrams are given in *Ref. 3.7.*, section 3.13.

3.11 CONCLUSIONS

Modern techniques of integrated circuit manufacture have resulted in the production of a wide range of analogue switches specifically intended for use in multiplexing systems, with considerable advantages over discrete systems in terms of size, reliability and costs.

The various performance factors for multiplexer devices have been outlined and guidelines for application given to indicate their versatility.

3.12 APPLICATION CIRCUITS

The following is a list of applications pertaining to Chapter 3 which can be found in "Applications Information," Chapter 7. Please refer to the page number indicated.

3.12.1 Typical Multiplexer Applications

.1 *8 Input Sample and Hold* – AN75-1, Page 7-74, Figure 19.

.2 *64-Channel 2-Level Multiplexer* – AN73-2, Page 7-13, Figure 6. Also AN76-6, Page 7-84, Figure 14.

.3 *A One of 8-Channel Transmission System* – AN75-1, Page 7-72, Figure 17.

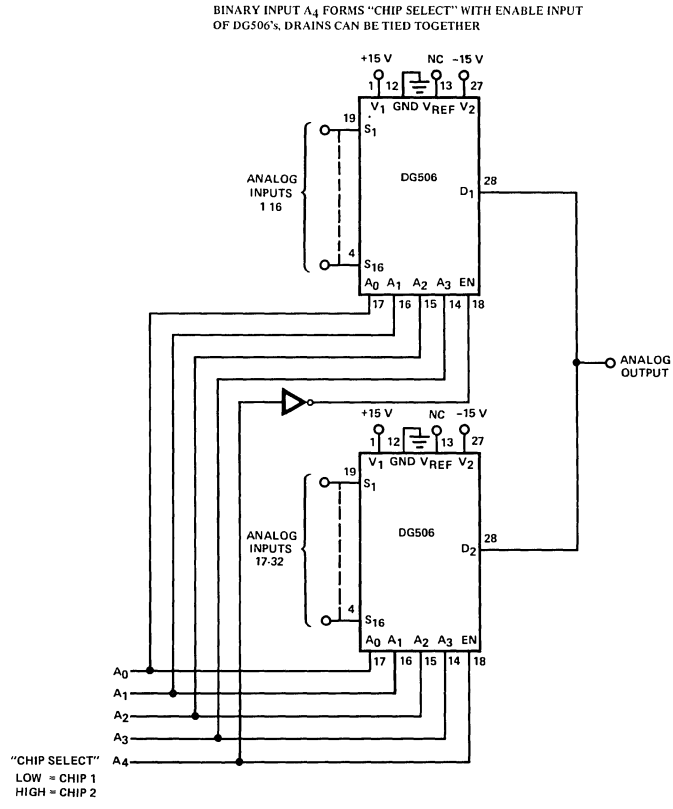
.4 *An 8-Channel Mux-Demux System* – AN75-1, Page 7-73, Figure 18.

.5 *A Thermocouple Multiplex System* – AN75-1, Page 7-77, Figure 24.

.6 *Thermister Differential Multiplexing* – AN75-1, Page 7-78, Figure 25.

3.12.2 Additional Multiplexer Application

Fig. 3.43
32 Channel 1 Level Multiplexer



3.13 REFERENCES

3.1 V.D. Landon, "Theoretical Analysis of Various Systems of Multiplex Transmission," RCA Review, Vol. 9, No. 2, pp. 287-351 and No. 3, pp. 433-482, 1948.

3.2 Dave Hage and Shelby Givens, "Switching High-Frequency Signals with FET Integrated Circuits," Siliconix Application Note, March 1973. (AN73-3, p. 7-15).

3.3 Shelby Givens, "FETs as Analog Switches," Siliconix Application Note, Sept. 1972. (AN72-2, p. 7-1).

3.4 H.M. Straube, "Dependency of Cross-talk on Upper and Lower Cut-off Frequencies in P.A.M. Time Multiplexed Transmission Paths," I.R.E. Trans. Comm. Sys., Sept. 1962, pp. 268, et. seq.

3.5 E.L. Gruenberg (Ed.), "Handbook of Telemetry and Remote Control," Chapter 9, McGraw-Hill, 1967.

3.6 J.O.M. Jenkins, "I.C. Multiplexer Increases Analog Switching Speeds," Siliconix Application Note, February 1973. (AN73-2, p. 7-9.)

3.7 J.A. Roberts and J.O.M. Jenkins, "Multiplexer Adds Efficiency to 32-Channel Telephone System," Siliconix Application Note, Jan. 1973. (TA73-1, p. 7-93.)

Chapter 4

Sample-and-Hold Circuits

4.1 INTRODUCTION

Sample-and-Hold systems are widely used in electronic systems where storage of analogue voltages is required. This chapter is intended to familiarize potential users with the application of FET and IC analogue switches in Sample-and-Hold applications.

4.2 SAMPLE AND HOLD BASICS

4.2.1 Basic Circuit

Analogue sample-and-hold circuits utilize the ability of a capacitor to store charge and hence a voltage according to the fundamental capacity equation Q = CV, where Q = stored charge, C = capacitance, and V = voltage across the capacitor. The voltage on the capacitor will decay at a rate determined by the leakage current flow into or out of the capacitor. Fig. 4.1 illustrates a very basic sample-and- hold circuit. The input voltage can be sampled and stored by closing, and subsequently opening switch SW1. In order to process this stored voltage, the capacitor must be strobed at some future period. To prevent decay of the sampled voltage during strobing, it is essential to connect a very high input impedance stage between the capacitor and the processing unit. In the capacitor 'hold' mode, with SW1 open, a capacitor voltage decay rate of ZERO would be achieved if the net sum of currents flowing into or out of the capacitor plates was zero.

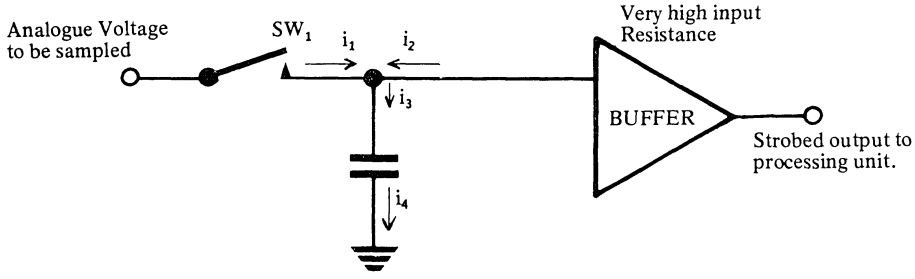


Fig. 4.1 **Basic sample-and hold system**

The net sum of current would be determined by the values of i_1, i_2, i_3 and i_4.

i_1 = Leakage current through OFF switch SW1.
i_2 = Leakage current into/out of buffer.
$i_3 = i_1 + i_2$, and
i_4 = Inherent leakage of capacitor.

In practice, the net sum of currents is seldom zero and there will either be a negative or positive voltage decay rate (droop rate) depending on whether positive charge flows into or out of the capacitor.

4.2.2 Definition of terms

The following terms are widely used when dealing with Sample-and-Hold circuits :

a) Hold time, b) Droop rate, c) Aperture time, d) Acquisition time.

They are defined as follows :

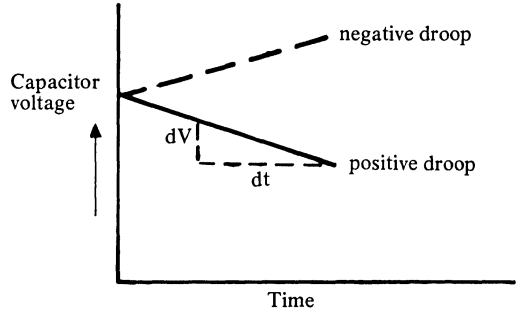
a) **Hold Time**

This is the time during which charge is held on the capacitor. This corresponds to the length of time that SW1 (Fig. 4.1) is open.

b) **Droop Rate**

Is a measure of the circuit's ability to hold the stored voltage over a defined period of time. Droop rate can be either positive or negative, and its magnitude is determined by the net current i_3-i_4 (Fig. 4.1).

Fig. 4.2 **Capacitor voltage change with time**



The capacitor charge/voltage equation is given by V = Q/C.

$$\therefore \text{Droop rate (volts/sec)} = \frac{dV}{dt} = \frac{1}{C} \cdot \frac{dQ}{dt}$$

where $\frac{dV}{dt}$ defines the incremental change in voltage with time across the capacitor (expressed in volts/sec), C is the capacitor value in Farads. $\frac{dQ}{dt}$ defines the instantaneous value of current, in amperes, into or out of the capacitor and is equal to $(i_3 - i_4)$.

$$\therefore \frac{dV}{dt} = \frac{1}{C} \cdot (i_3 - i_4)$$

If i_1 = 30pA, i_2 = 5pA and i_4 = -10pA, then i_3 will be 25pA into the capacitor. In this case, the capacitor voltage will increase positively with time when in the 'holding' mode.

c) **Aperture Time**

This is the time to turn the switch from ON to OFF. Mechanical contacts, although providing excellent OFF isolation and nearly zero ON resistance are limited in aperture time. This is not much less than a millisecond for the fastest electromechanical relays available.

Although discrete field effect transistors in the OFF state may exhibit somewhat lower off isolation, they have an aperture time of nano-seconds and have a much longer operating life than any electromechanical system, provided they are operated within their specified data ratings.

The IC analogue switch, due to its greater complexity and greater number of driver logic stages, has longer propagation delay times (delay time between logic input and switch output) than a discrete FET, but can still offer t(on), t(off) times which are appreciably less than 1μsec. This implies that the aperture time is at least a thousand times less than that of a relay.

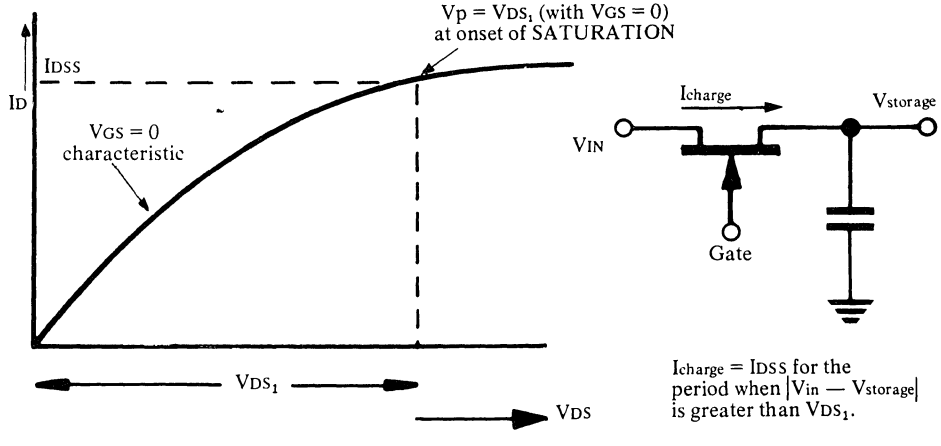
d) **Acqusition Time**

This is the overall time taken for the capacitor to charge to a specified percentage of the analogue signal value. This includes the t(on) time of the switch. The JFET and MOSFET can be assessed as follows :

Junction FET

Two parameters, other than the analogue source resistance, will determine the value of capacitor charging current and hence acquisition time. These are the saturation current I_{DSS} and on resistance $r_{DS(on)}$. Immediately after the JFET turns on, its drain- source current will be equal to its I_{DSS} provided the V_{DS} at turn-on exceeds its Vp value. When the capacitor has charged sufficiently to cause the drain-source voltage of the FET to fall to a value which is less than its Vp, the charging current will thereafter be determined by the overall sum of switch $r_{DS(on)}$ and analogue source resistance. Reference to Fig. 4.3 shows how the charging current is dependent on both I_{DSS} and $r_{DS(on)}$ of the FET.

Fig. 4.3 **n-channel Junction FET output characteristic**



MOSFET

For the MOS, the charging current after turn-on is dependent upon the effective gate-to-source voltage applied. Equation 4.1 shows that in the case of a p-channel MOS with a fixed negative voltage drive on the gate, the current when V_{IN} is positive can be considerably greater than that when V_{IN} is negative. The acquisition time is therefore correspondingly less, when V_{IN} is positive.

$$I_D = \beta \left\{ (V_{GS}-V_{GS(th)}) \cdot V_{DS} - \frac{V^2_{DS}}{2} \right\} \qquad \text{eqn. 4.1}$$

For a p-channel enhancement MOS :

V_{GS} = value of gate voltage referred to source (where source is taken as the most positive node).
$V_{GS(th)}$ = threshold voltage referred to source
V_{DS} = drain voltage referred to source.
β = a constant determined by device parameters.

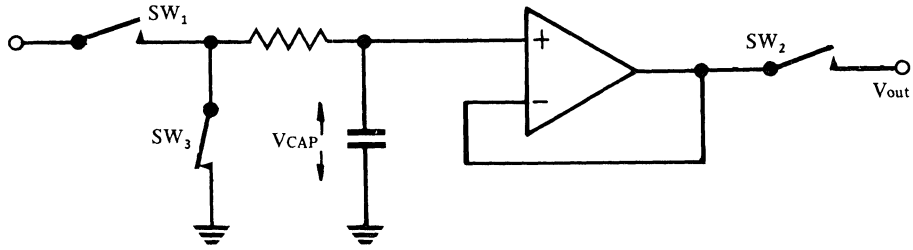
4.3 TYPES OF CIRCUITS

There are several arrangements of sample-and-hold circuits which can serve as basic building blocks. Some of these are presented. IC analogue switches can be usefully employed in several of the more practical arrangements.

4.3.1 Basic Type 1—Non-inverting Sample-and-Hold

Switch SW_1 (Fig. 4.4a) is initially open and SW_3 is closed. Capacitor C_1 will therefore be discharged through switch SW_3 so that the capacitor voltage will initially be zero. Upon closure of SW_1 and the opening of SW_3, capacitor C_1 charges to the analogue signal voltage value. SW_1 now opens, allowing C_1 to hold the sampled voltage. This voltage will be seen at the output of the unity gain amplifier which acts as a high input impedance buffer for the capacitor, also as a low output impedance voltage source. When SW_2 closes, the stored value is transferred to the subsequent circuitry.

Fig. 4.4a **Non-inverting sample-and-hold**



Sampled information can be stored for a predetermined time. If there is no charge loss from capacitor C_1, the magnitude of the output voltage at time t_1 will be the value of the sampled analogue signal at time t_0.

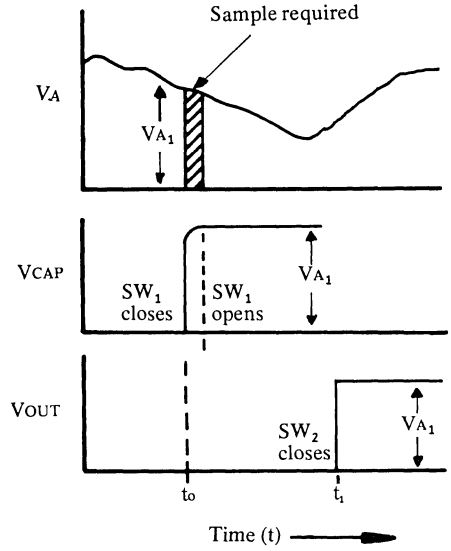
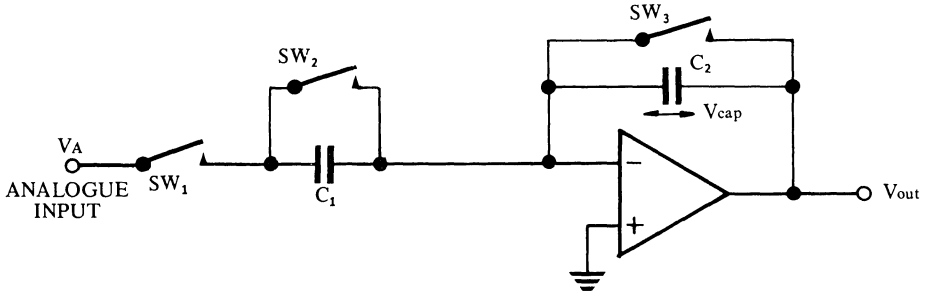


Fig. 4.4b
VOUT at time t_1 = sampled value of Vin at time t_0

4.3.2 Basic Type 2—Integrating Sample-and-Hold

At the beginning of the switching sequence, SW_1 (Fig. 4.5) is open and SW_2 and SW_3 closed. This allows C_1 and C_2 to discharge to zero volts so that Vout is also zero. SW_2 and SW_3 now open and SW_1 closes. Vout will settle at a value of $-\frac{C_1}{C_2} V_{A_1}$. SW_1 now opens and SW_2 closes, completely discharging C_1, whilst C_2 remains charged at the value $-\frac{C_1}{C_2} V_{A_1}$. During further sampling of the analogue input, SW_1 again closes causing the initial voltage on C_2 to be further increased by a value of $-\frac{C_1}{C_2} V_{A_2}$. SW_1 now opens and SW_2 again closes and the cycle is again repeated at the required period in time. After *N* samples of the analogue signal have been taken, Vout will be proportional to the sum of all the *N* samples taken.

Fig. 4.5a **Inverting sample-and-hold integrator**



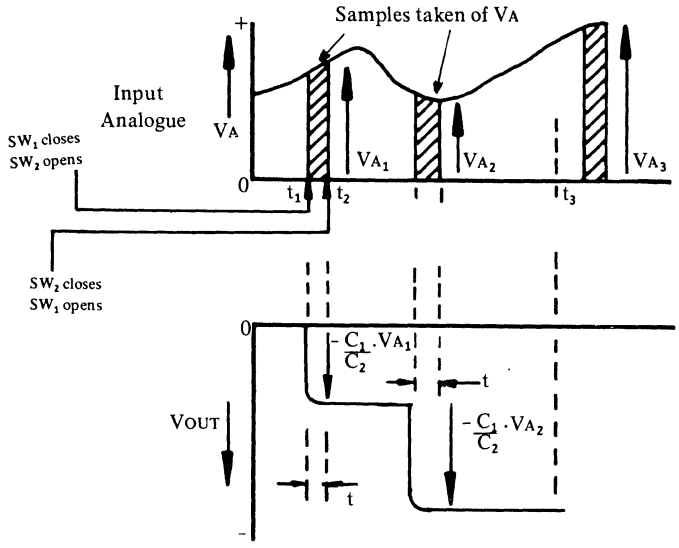


Fig. 4.5b
If sample period $t > 3C_1R$ then after N'th sample
$V_{out} = \frac{-C_1}{C_2}(V_{A_1} + V_{A_2} + \ldots + V_{AN})$

A number of samples taken over a period of time can be integrated so that the value of stored voltage after a time t (say) will be the sum of all samples taken previously at times t_1, t_2 ... t.

4.3.3 Basic Type 3—Peak detection

Initially SW_2 (Fig. 4.6) would be closed, and SW_1 open. This allows C_1 to discharge to zero volts. V_{out} will consequently be at zero volts. When SW_1 samples the analogue input, capacitor C_1 will charge up to the most positive voltage experienced during the sampling period. Any voltage which is more negative than the capacitor voltage will cause the diode to become reverse biased. In this case C_1 will retain the most positive value of analogue input applied. This basic circuit does suffer from slight inaccuracies in that the peak sampled voltage would be slightly less than the peak input analogue voltage, due to the forward diode voltage drop. There are ways available which compensate for this. This will be discussed under the next sub-section entitled More Detailed Circuits.

Fig. 4.6a **Non-Inverting positive peak detector**

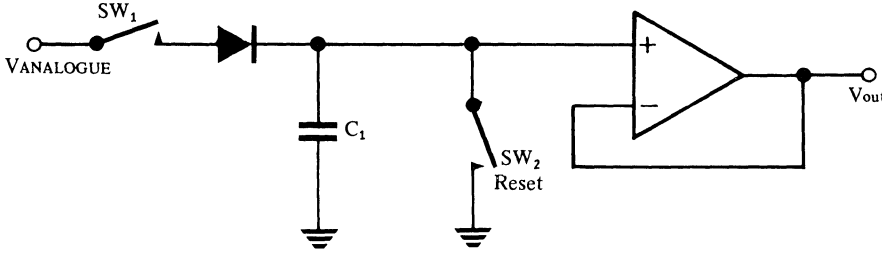
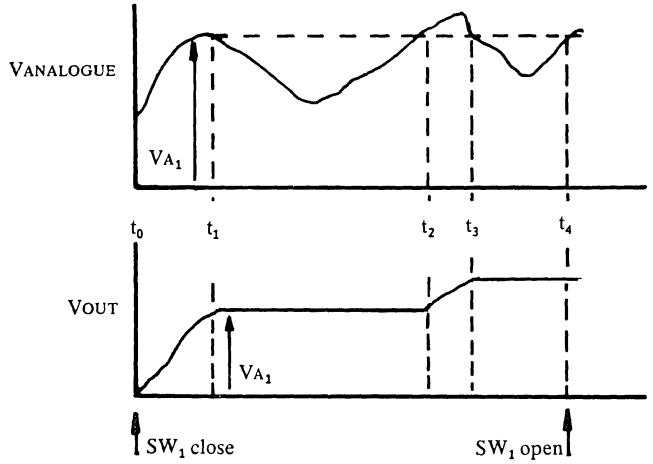


Fig. 4.6b **Voltages corresponding to Fig. 4.6a**



$V_{out} = \hat{V}$Analogue (during time interval t_0 to t_4).

The output of the sample-and-hold, V_{out}, will track the peak positive value of the analogue wave-form during period when SW_1 is closed.

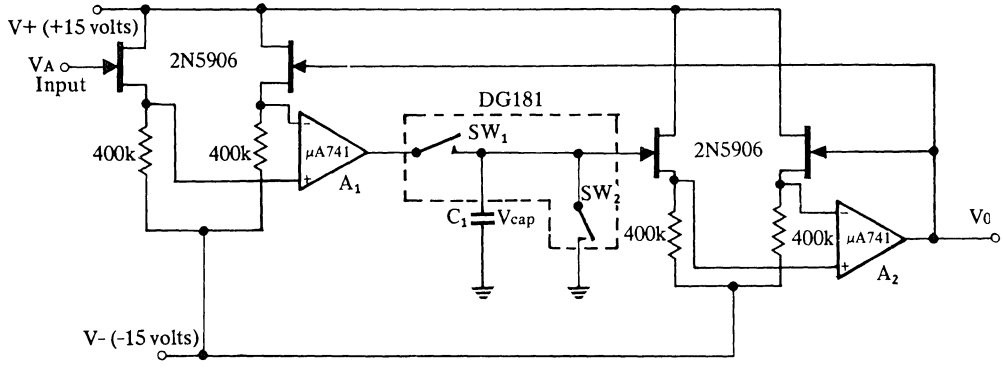
4.3.4 More Detailed Circuits

The previous circuits show some basic configurations. In practice, accuracy can only be achieved using higher complexity circuits. The electrical performance is improved by the addition of feedback loops, input buffer stages etc. Fig. 4.7 onwards illustrate the use of IC analogue switches in some of these configurations.

4.3.4.1 Type 1—Non Inverting Sample-and-Hold (Compare basic curcuit of Fig. 4.4)

Fig. 4.7 shows a more detailed arrangement of Fig. 4.4. SW_2 is incorporated so that the capacitor voltage can be reset to zero. SW_1 and SW_2 can be independently controlled. The total switching function may be performed simply with either a DG181 or DG182 IC analogue switch.

Fig. 4.7 **Non-inverting sample-and-hold with 2N5906 for high input impedance**



Use of 2N5906 dual n-channel junction FETS combined with DG181 analogue switches will give low capacitor droop rate. Input leakage of 2N5906 <1pA at 25°C.

Features of Circuit

1) The matched pair of n-channel Junction FETS at the front end of this circuit presents an exceedingly high input resistance to the analogue signal V_A. A 2N5906 matched pair will have a gate input leakage of <1pA at a V_{DG} of 15 volts and will therefore present the analogue signal with an effective load of $>10^{12}$ ohms.

2) The 2N5906 FETS are connected in a source follower configuration so that the input to the first op-amp will be $V_A - V_0$. If V_A is positive with respect to V_0, the feedback loop will ensure that the output of A_1 will swing positive causing C_1 to charge to a positive value. The voltage appearing across the inputs of the second operational amplifier A_2, will be $V_{cap} - V_0$ which will cause V_0 to swing positive. This output swing is fed back to the gate of the input pair of 2N5906. When the capacitor has charged to the value of the analogue input V_A, the polarity of V_0 will change, causing the output of A_1 to go negative. The operation of the closed loop will allow C_1 to settle to the value of V_A.

3) The output resistance of the input FET pair is very nearly $\frac{1}{g_{fs}}$. For the 2N5906, this means an output resistance of not more than 12 kohms. This is sufficiently low to ensure that A_1 does not load the source follower.

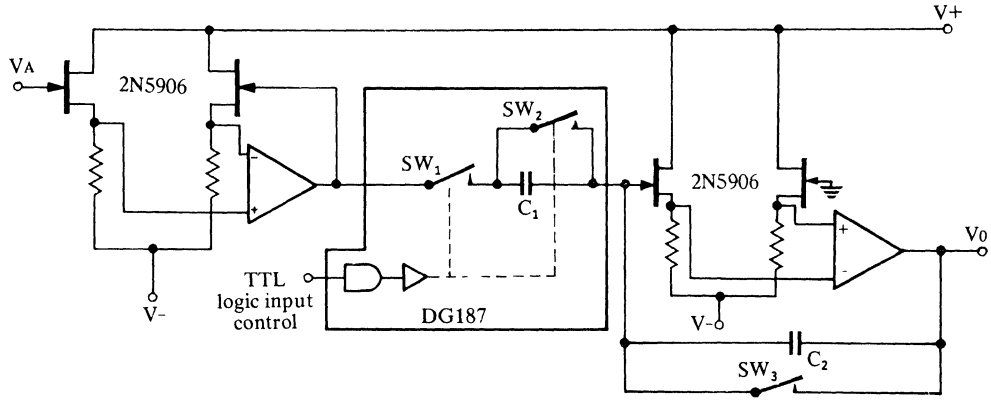
4) A_1 acts as a buffer, and having a fairly high output current capability allows C_1 to charge rapidly.

5) SW_1 consisting of a DG181 combined with the second buffer stage, which consists of another 2N5906, present an extremely high resistance which limits the leakage current flowing out of or into the capacitor. Droop rates can therefore be held to a very low value.

4.3.4.2 **Type 2—Integrating Sample-and-Hold** (Compare basic circuit of Fig. 4.5)

Fig. 4.8 shows a detailed arrangement of an integrating sample-and-hold circuit.

Fig. 4.8 **Integrating sample-and-hold using 2N5906 input FETS and DG187 type switches**



Features of Circuit

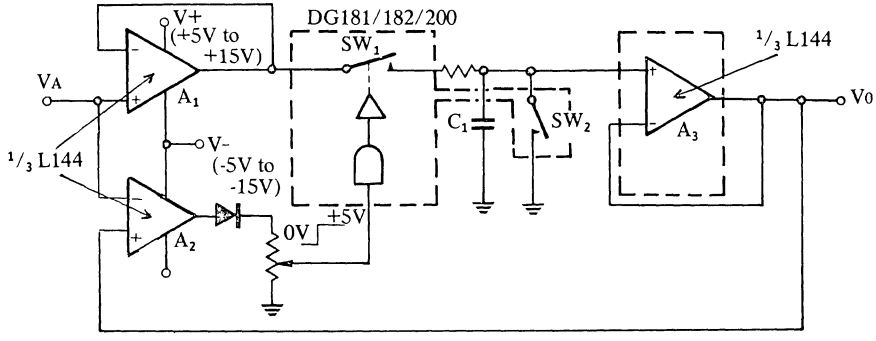
1) Input End—2N5906 Junction FETs to provide high input resistance.
2) SW_1, SW_2—2 channel DG187, break-before-make switching action.
3) SW_3—Reset switch—Any type of IC analogue switch. Alternatively, one DG190 could be used to provide all 3 switches.

4.3.4.3 **Type 3—Peak Detection** (Compare basic circuit of Fig. 4.6)

The use of semiconductor diodes in peak detection systems can lead to inaccuracies due to the diode's forward conduction characteristics. Feedback will eliminate these inaccuracies but simultaneously can introduce overshoot into the system, resulting in output values which are greater than the peak value measured. The errors can be a substantial percentage of the peak value when low analogue voltages are measured. Substituting the diodes with analogue switches can give increased accuracy. Fig. 4.9 shows how the switches could be utilized. A third operational amplifier acting as a comparator would provide the logic drive for operating SW_1.

The voltage V_0 at output of A_3 is fed back to the input of A_2. When V_A goes more positive than V_0, the output of A_2 goes negative, allowing the logic input to SW_1 to go to zero volts. With a DG182 or DG200 switch, a logic '0' input will close the switch allowing C_1 to charge up to the analogue input voltage and hence V_0 (since A_3 has unity gain). If V_A subsequently goes to any value which is more negative than V_{01} the output of A_2 will go positive. This allows a logic '1' to be applied to SW_1 control input turning SW_1 off. This prevents C_1 from charging to the new analogue value. The system will therefore store the most positive analogue input experienced.

Fig. 4.9 **Positive peak detection circuit**



Features of Circuit

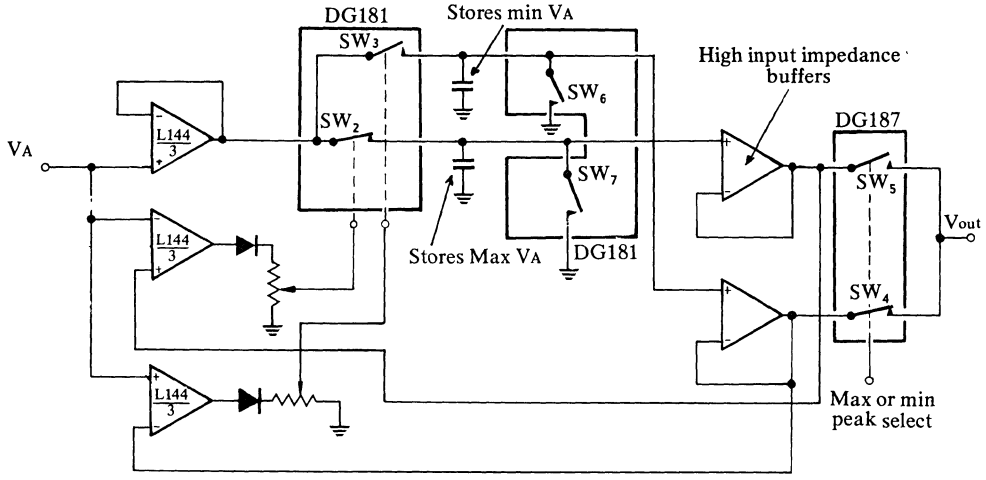
1) SW_1—Used instead of diode. This exhibits constant low on resistance for analogue voltages as low as millivolts.
2) SW_2—Reset Switch.

Switches could be provided in IC form; for example, DG181/182 with open/close time of 150ns or the less expensive monolithic types e.g. DG200 with an open/close time of $<1\mu s$. The three operational amplifiers could be a Siliconix triple L144 integrated circuit. This can operate with ± 5 volts supplies and will allow the logic input control of SW_1 to go directly to +5 volts.

4.3.4.4 Extension of Circuit for Positive and Negative Peak Detection

Figs. 4.10a/b show IC analogue switches in a positive and negative peak detection system. Operation is similar to that described in Fig. 4.9. The system will detect and store the maximum and minimum values of the analogue input.

Fig. 4.10a **Use of 1 x DG187, and 2 x DG181 in max/min peak detection system.**

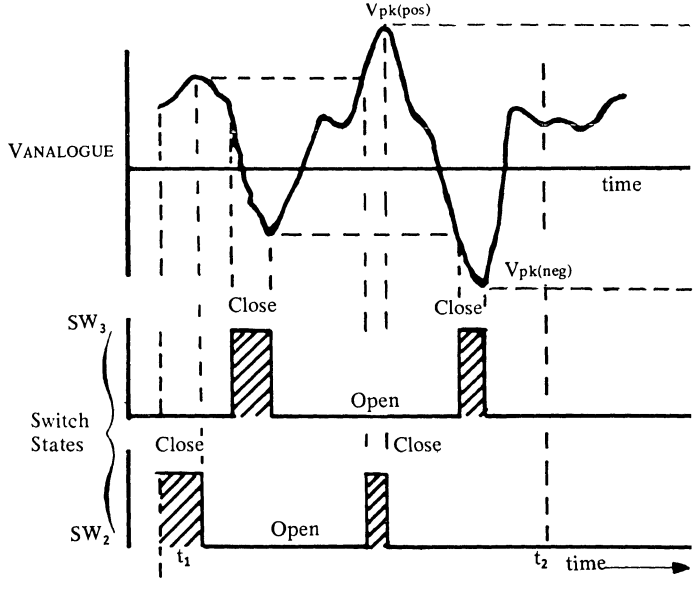


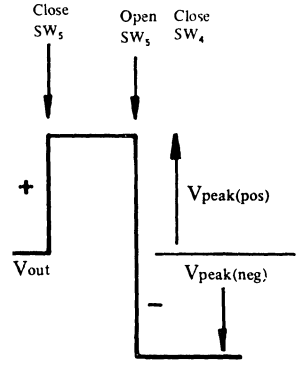
DG187/DG181 Switch Characteristics (Guaranteed)

1) 30Ω max $r_{DS(on)}$ giving low acquisition time. 2) Break-before-make switch action.

3) Maximum t_{on}/t_{off} times 150ns/130ns. 4) Maximum OFF leakage of 1nA.

Fig. 4.10b **Switch OPEN and CLOSE periods**





Sampled output giving maximum and minimum VA values reached during time interval t_1 to t_2.

4.4 SOURCES OF ERROR

The accuracy of the stored signal in a sample-and-hold system depends on a number of circuit parameters and must be considered under the following conditions :

4.4.1 Steady state conditions when switch is ON. *This has been discussed in Chapter 2.*

4.4.2 Transitional conditions when switching from OFF to ON. *This has been discussed in Chapter 2.*

4.4.3 Steady State OFF Conditions

The contribution to steady OFF state errors are due to the following :

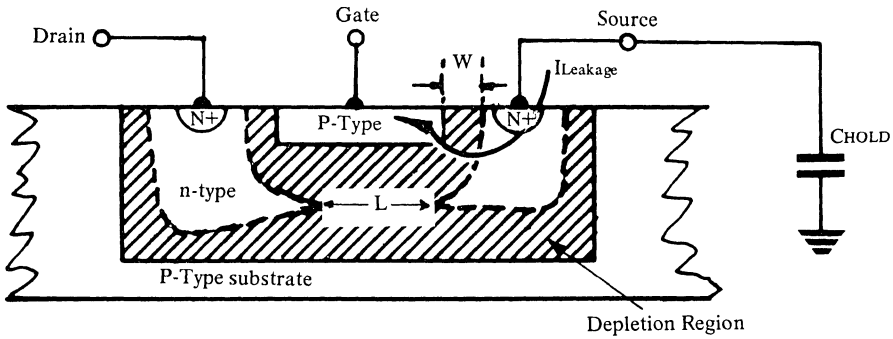
a) FET gate-source or gate-drain leakage currents in the OFF state.
b) Inherent capacitor leakage currents.
c) Buffer amplifier input leakage currents (Fig. 4.1).
d) Environmental conditions such as temperature, humidity, and leakage quality of the printed circuit board on which the circuit is mounted.

FET leakage current is a most important parameter that has to be considered in sample-and-hold circuits. This warrants a brief revision of JFET and MOSFET leakage currents.

4.4.3.1 Junction FET Leakage

The profile of a Junction FET in the OFF state is shown in Fig 4.11 below.

Fig. 4.11 **Idealized cross-section of a JFET showing depletion regions in the OFF state.**



The depletion region will extend through a large part L of the overall channel length, and being a region devoid of majority carriers, acts as an electrical insulator. The width 'w' of the depletion region at the surface (Fig. 4.11) will, for any JFET in the OFF state, be appreciably less than the depletion length L. This means that the major component of leakage current flowing into the source is between source and gate. Source-to-drain leakage will be relatively much less.

The gate of any N-channel JFET in the OFF state is more negative than its drain or source and so if C_{hold} is charged to a positive voltage, positive leakage current will flow out of the capacitor into the gate of the FET. This current, being p-n junction leakage, is approximately proportional to $\sqrt{V_R}$, where V_R is the reverse bias across the junction. The values of drain, gate and source voltages should therefore be considered when calculating capacitor droop rates. FET chip temperature is also critical since silicon p-n junction leakage approximately doubles for every 10°C rise in junction temperature.

4.4.3.2 MOSFET Leakage

The MOSFET is different in structure and its profile is shown in Fig. 4.12. For sample-and-hold circuits, the use of a MOSFET with an unprotected gate will reduce source-gate and drain-gate leakage current in the OFF state to a negligible value which can be less than 1pA. An unprotected MOSFET does not have the integrated zener voltage clamp that a protected MOSFET has; Fig. 4.12 shows this basic difference.

Fig. 4.12a **Diagrammatic profile of a p-channel MOSFET** (unprotected).

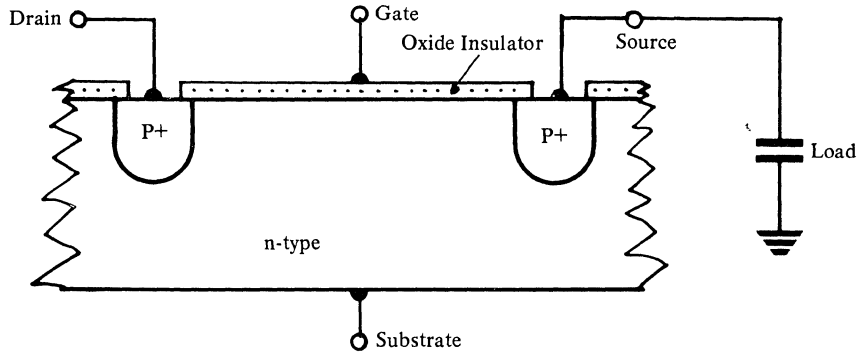
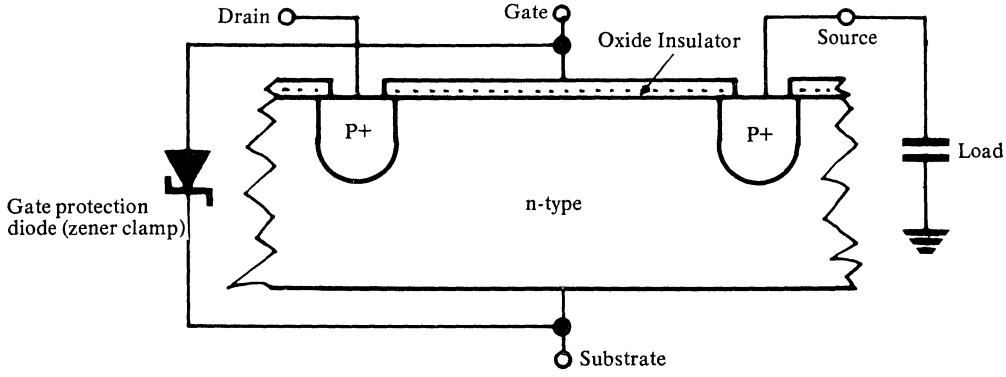


Fig. 4.12b **Profile of a p-channel MOSFET** (protected)



However, in both cases, substrate biasing is necessary to ensure that the substrate is always reverse biased with respect to source and drain. This unfortunately

implies that leakage current will flow from the p-type source and drain into the n-type substrate. The laws governing this p-n junction leakage are the same as those for the JFET. There are ways of using the MOSFET in sample-and-hold circuits such that the substrate-to-source voltage is always zero. The substrate-source leakage is consequently reduced to an extremely small value. Details are given in Fig. 4.15.

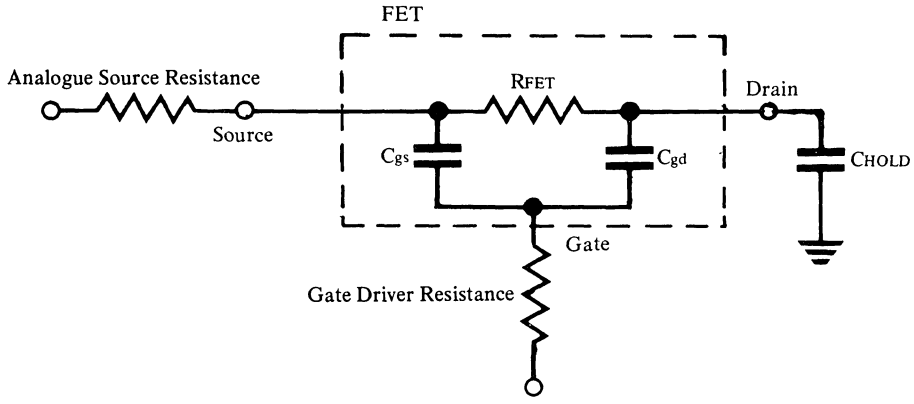
It is imperative, if good performance is to be achieved, to ensure that the board material used for mounting the components has high insulation qualities. Care should therefore be taken to choose the correct type of material. Fibreglass or Teflon are two materials which are ideal. It is important to ensure that board surfaces are clean.

Of course, the ideal solution is to arrange the layout so that the critical nodes contributing to the leakage problem do not make contact with the printed circuit board.

4.4.4 Transitional Conditions

Substantial voltage errors can be introduced into the hold capacitor when the FET is being turned OFF, and can be calculated by considering the FET equivalent circuit of Fig. 4.13.

Fig. 4.13 **JFET equivalent circuit**



A voltage transition at the gate of the FET will cause a voltage spike to appear in the analogue path, the magnitude of the spike being a complex function of circuit capacitances, resistances and magnitude and slewing rate of both the applied gate voltage and analogue signal voltage. An approximate value of generated voltage error appearing across CHOLD resulting from the on-to-off voltage transition at the gate is given approximately by the expression

$$\frac{C_{gd}}{C_{HOLD}} \cdot V_{\text{gate excursion.}}$$

A large reduction in error voltage can therefore be achieved by :

1) Reducing the ratio of FET capacitance to load capacitance.
2) Reducing the voltage excursion (V_{gate} excursion) at the gate.

Methods of eliminating errors are discussed in the next section.

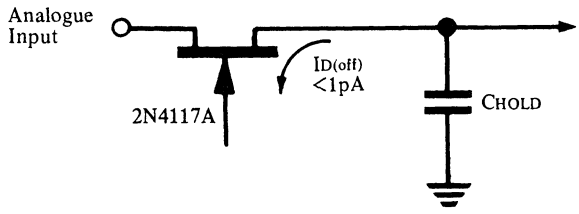
4.5 METHODS FOR REDUCING ERRORS

4.5.1 Reducing Steady State Errors

4.5.1.1 Use of Low Leakage FETs

The easiest way of reducing steady state errors is to employ low leakage junction FETs (Fig. 4.14) which have leakage values of less than 1 pA. To achieve low leakage, the FETs must have a small geometry which inherently gives a fairly large ON resistance. The Siliconix 2N4117A sub-picoamp FET will exhibit an ON resistance of 5kohms to 10kohms. The high ON resistance may result in an unacceptable acquisition time although the use of low leakage FETs would result in smaller capacitor droop rates and this could consequently allow the use of a smaller capacitor with an accompanying reduction in acquisition time.

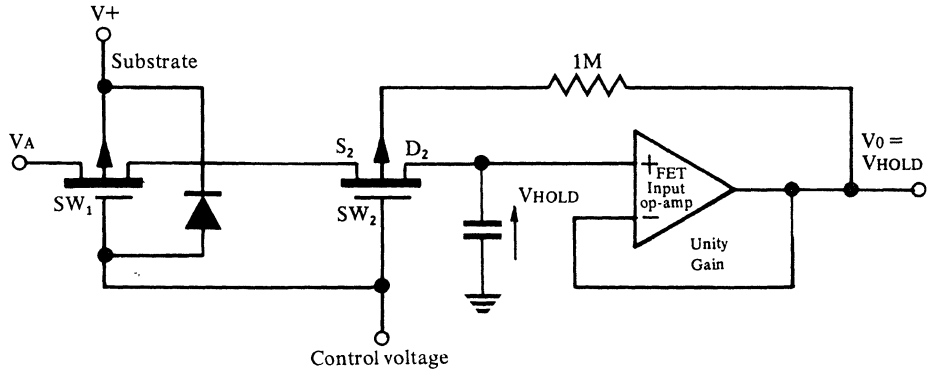
Fig. 4.14 **Main FET leakage current path in the OFF state.**



4.5.1.2 Use of Two Series Switches

Instead of low leakage junction FETs, an unprotected MOSFET with a very low (sub-picoamp) gate-drain and gate-source current could be used. Leakage current flowing out of the capacitor via the MOSFET substrate is prevented by the biasing technique given in Fig. 4.15. The two switches shown are MOSFET structures although SW_1 can be either a JFET or a MOSFET. SW_2 is an unprotected MOSFET which can be either a p-channel or an n-channel enhancement type.

Fig. 4.15 **Method of reducing drain-to-substrate leakage on a MOSFET.**

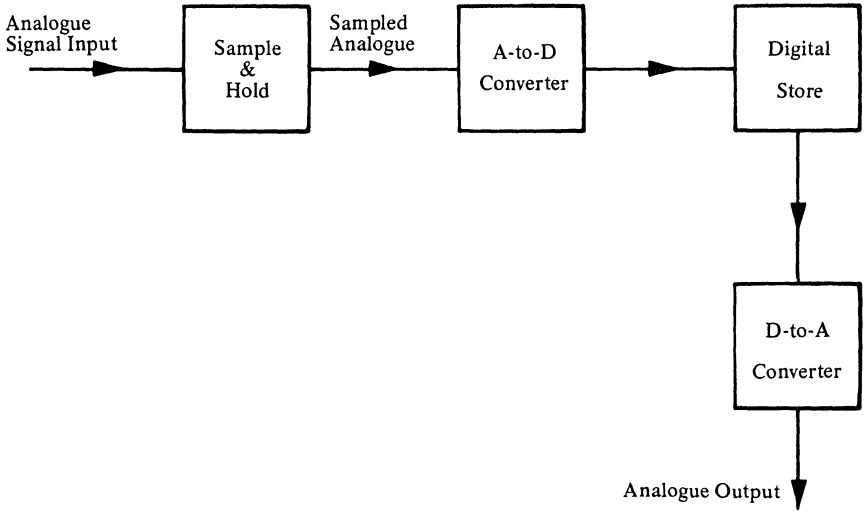


The substrate of SW_2, by virtue of the feedback loop, is at the same voltage as drain D_2. Reverse bias on the substrate-drain junction is therefore always zero volts and leakage current into the substrate from drain D_2 will be practically zero when the switch is OFF. As SW_2 is an unprotected MOSFET (no voltage clamp between gate and substrate), drain-to-gate leakage current is also exceedingly small. SW_1 is necessary to ensure that S_2 is isolated from the incoming analogue signal when the switches are turned OFF. If SW_1 were absent, positive analogue input signals which were more positive than V_{Hold}, would appear at the substrate of SW_2. The substrate-drain junction of SW_2 would then be reverse biased to a voltage of V_A—V_{Hold} causing leakage current to flow from the capacitor into the analogue signal source via the substrate of SW_2.

4.5.1.3 Use of Analogue-to-Digital Converter

Errors due to capacitor droop can be completely eliminated by converting the sampled analogue signal to a digital format which can then be stored permanently (Fig. 4.16). This allows an infinitely long storage time with zero droop. The signal can be converted back into the original analogue form by means of a digital-to-analogue converter. However, the electrical performance of this system has to be traded off with the much greater system cost involved.

Fig. 4.16 **Analogue-to-Digital converter for zero droop rate.**



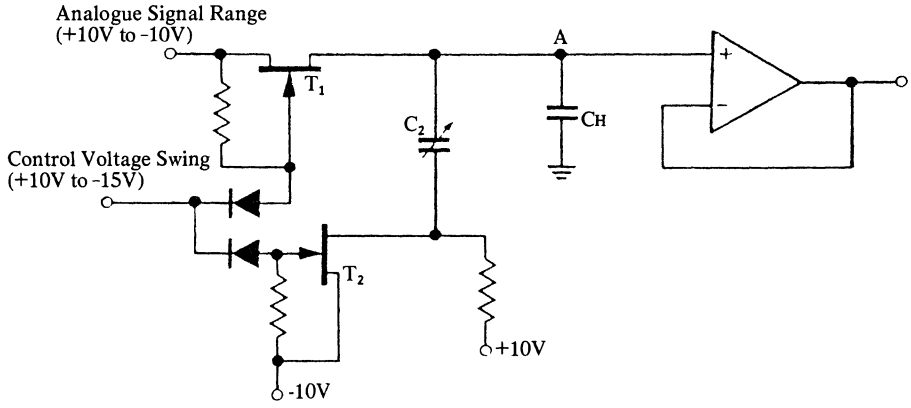
4.5.2 Reducing Transitional State Errors

4.5.2.1 Auxiliary Capacitor with Antiphase Drive *(Fig. 4.17)*

When the input control voltage goes negative, T_1 will turn OFF. The negative transition at the gate of T_1 will generate a negative spike in the analogue path which will add a negative error voltage to the sampling capacitor C_H. As T_1 turns OFF, T_2 also turns OFF so that its drain shows a positive transition. The

capacitor C_2 consequently feeds a positive spike into C_H. By adjusting the value of C_2 exact cancellation of the negative error voltage on C_H is obtained. The addition of C_2 to the critical node A can, however, provide an additional leakage path which might slightly degrade the droop rate. This method can be conveniently applied to both discrete FETs and ICs.

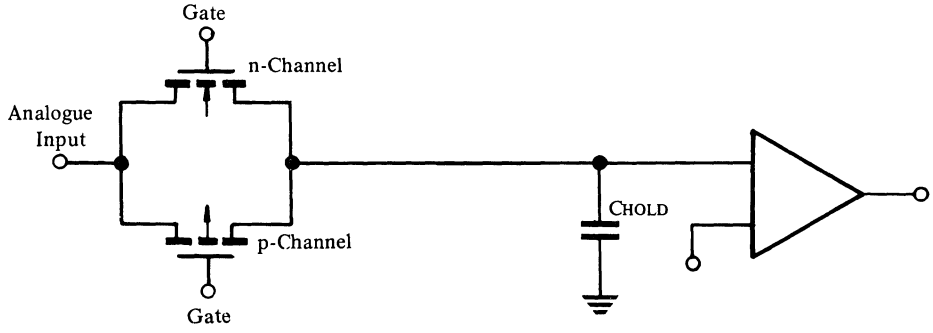
Fig. 4.17 **Reducing errors with antiphase drive.**

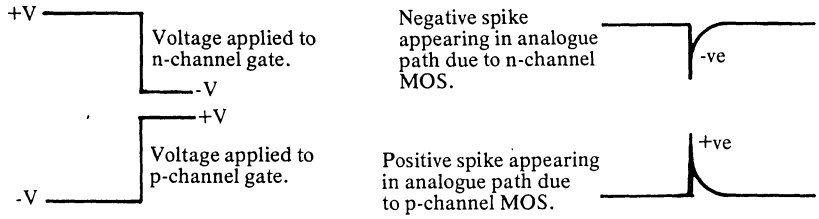


4.5.2.2 Use of Complementary MOS *(Fig. 4.18)*

The use of a parallel combination of n-channel and p-channel MOSFETs will require a positive going gate signal to turn the p-channel FET OFF and a negative going gate signal to turn the n-channel FET OFF. Provided both FETs have almost equal junction capacitances and their gate voltage swings are in antiphase with the same magnitude and slewing rate then the net charge transferred into C_H via each FET will be zero. Using discrete MOSFETs, a large error reduction is achievable. The CMOS integrated circuit version, due to slight differences in propagation delay times between the signals arriving at each of the p- and n- channel MOS gates, will exhibit a somewhat lower spike cancellation (around 50% error reduction). However, the IC is normally directly compatible with standard TTL, or CMOS logic control and is more convenient to use.

Fig. 4.18 **Reducing errors with CMOS switches.**

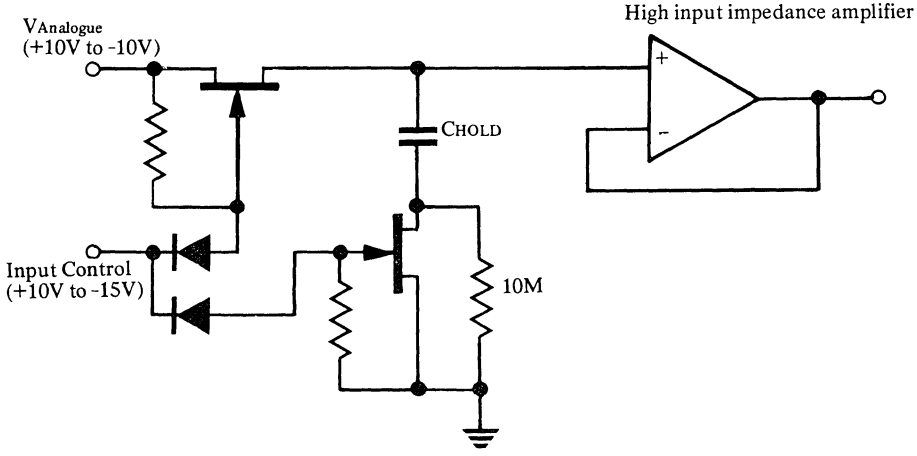




4.5.2.3 Use of Two JFETs *(Fig. 4.19)*

A positive input control signal will switch both FETs ON, allowing the capacitor to charge to the analogue voltage. On the other hand, a negative control signal will switch both FETs OFF. Negative spikes introduced simultaneously during the OFF transition into either side of the capacitor will tend to cancel. Fig. 4.19 below shows the circuit for a discrete FET system, but these could be substituted by an IC switch such as a DG133, DG181, or DG200. The 10Mohm refers the capacitor voltage to ground when both switches are OFF.

Fig. 4.19 **Reducing transitional errors with JFET switches**



4.5.2.4 A High Accuracy Sample-and-Hold System

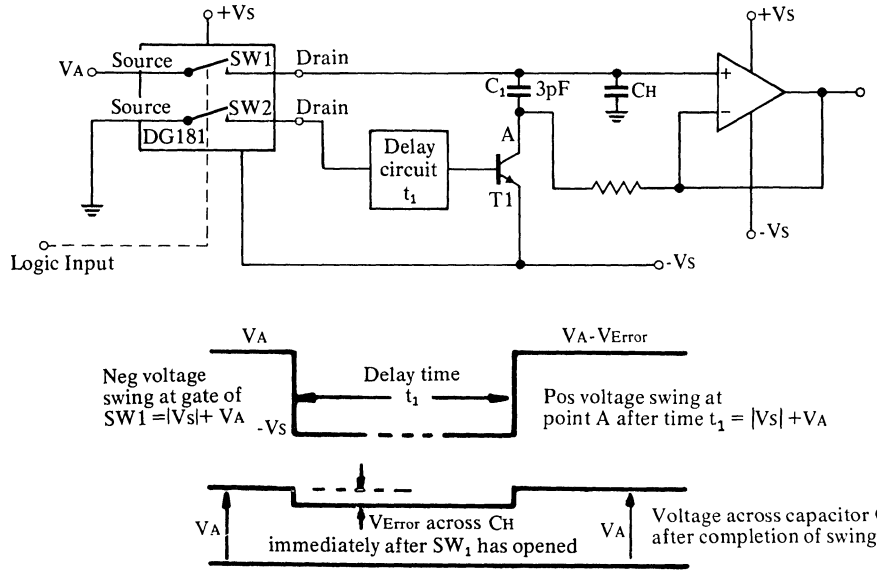
As mentioned previously, errors are introduced into the sampling capacitor during the switch turn-off transient. This error can be cancelled over the full analogue signal range, by using the circuit of Fig. 4.20 *(Ref. 4.1)*. An error compensating signal is applied after the analogue switch SW_1 has been switched OFF. The compensating voltage swing should be of equal magnitude but opposite polarity to the driving signal appearing at the gate of SW_1 and the compensating capacitor should be as near as possible to the value of the junction capacitance of the FET analogue switch. Fig. 4.20 shows a DG181 type switch, one half is used as the analogue switch, the other half as the switch which energises the compensating circuit. A simple delay circuit allows the voltage transition at point A to occur after switch SW_1 has opened.

During turn off, SW_1 and SW_2 open simultaneously (the DG181 will have both SW_1 and SW_2 drivers on a monolithic driver chip and both devices will exhibit practically the same t_{off}/t_{on} times). As SW_1 opens, a negative going error signal (V_{error}) of magnitude proportional to $-[|Vs|+ V_A]$ is introduced into the hold capacitor via the gate/drain capacitance of SW_1. The capacitor voltage, after SW_1 has opened, will therefore be $V_A - V_{error}$. Point A at this time will, due to T_1 being ON, be at -Vs volts. SW_2 however, opens simultaneously with SW_1 and after a short time delay will cause T_1 to turn OFF, thus bringing point A back to the value of the op-amp output i.e. V_A-V_{error}. The magnitude of the positive voltage swing at A will therefore be:

$$[|Vs|+ (V_A - V_{error})].$$

V_{error} is negligible compared with Vs and, therefore, the above can be considered as $|Vs|+ V_A$.

Fig. 4.20 **Cancellation of error in high accuracy sample-and-hold circuit.**



Since C_1 is approximately the same value as the junction capacitance of SW_1. there will be an equal and positive compensating charge introduced via C_1 into the hold capacitor (Fig. 4.20). Using a DG181, C_1 should have a nominal value of around 3pF. The most practical and by far the most convenient way of establishing this capacitance would be to employ the same geometry JFET (Fig. 4.21) as that used for the DG181 switch, e.g. a 2N4391 FET.

The FET will always be reverse biased. The source-gate and drain-gate capacitances of a JFET in the reverse biased mode will vary approximately inversely as the square root of applied junction voltage. So the compensating FET will exhibit practically identical capacitances to the switch capacitance over any value of analogue range. With both drain and source connected, the

compensating capacitance will be C_{gs} + C_{gd}. This value may be slightly over compensating so that the overall voltage swing at the gate may have to be reduced slightly. This is easily done by reducing the emitter voltage of the bipolar via a potentiometer.

Fig. 4.21 **Use of a JFET as a compensating capacitance.**

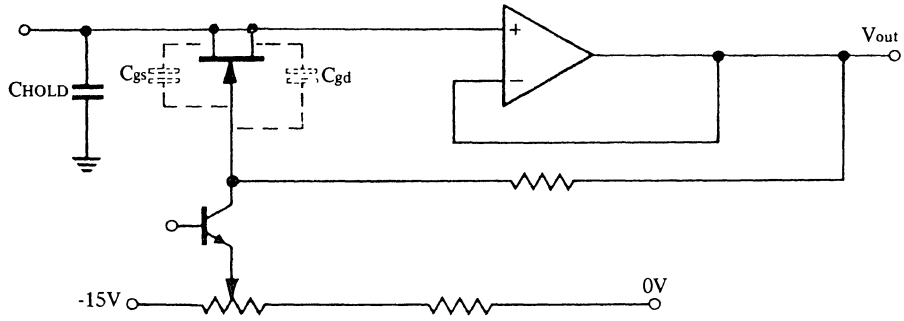
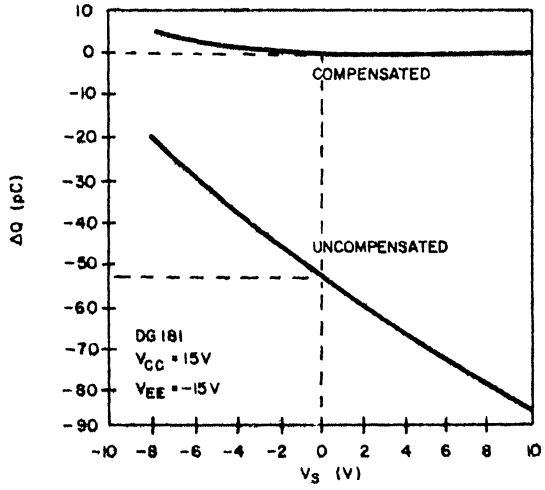


Fig. 4.22 compares the amount of net charge transferred into the hold capacitor in both uncompensated and compensated cases. The method would be extremely useful for low level analogue voltages. For example, with an analogue signal of a few tens of millivolts, and a 4700pF capacitor, the errors introduced would be practically zero in the compensated case. The uncompensated case would give approximately—10mV error.

Fig. 4.22 **Compensated and uncompensated charge transfer on DG181.**



Compensation with the circuit in Fig. 4.20 drastically reduces the change in transferred charge with signal level for the DG181, a 30-Ω JFET switch.

Referring to Fig. 4.22

E_{pk} (voltage error) $= \frac{Q}{C_{Hold}}$

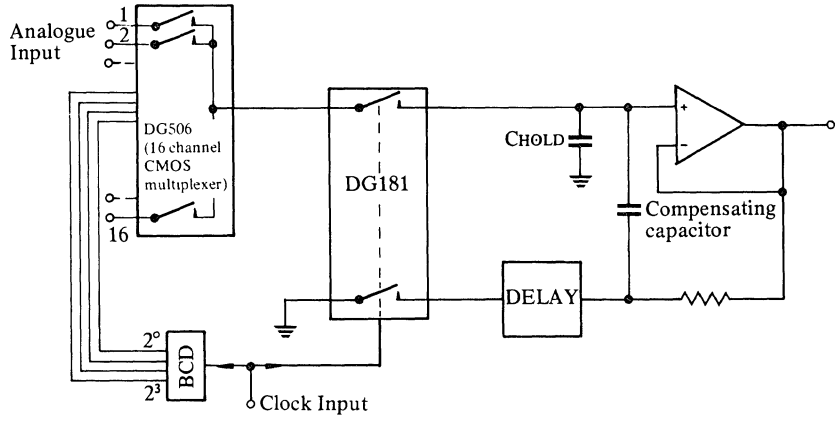
For ± 20mV analogue, $C_L = 4700pF$

E_{pk} (uncompensated) $= \frac{-53pC}{4700pF} = -10mV.$

E_{pk} (compensated) = 0mV

A multiplexing system for 16 channels, using the above technique is given in Fig. 4.23. As well as giving minimal offset error, the DG181 acts as a 'buffer' to reduce leakage between the capacitor and the 16 input channels.

Fig. 4.23 **Multichannel switching with compensation.**



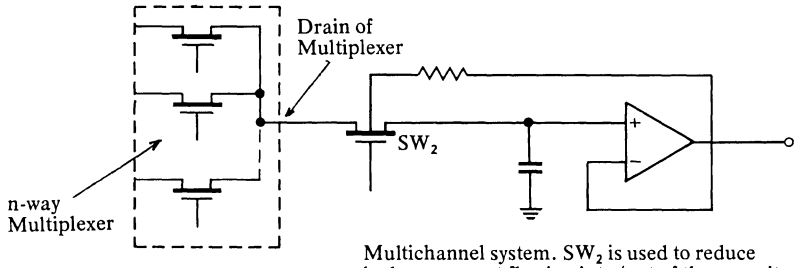
The leakage current flowing out of the capacitor into the 16 channels is therefore reduced to that obtainable on a single channel of a DG181. This reduces droop rate appreciably. The DG181 has a much faster t_{off} time than the DG506, this ensures that any additional voltage errors which would otherwise be generated across the load when the DG506 turns off are completely eliminated.

4.6 MISCELLANEOUS APPLICATIONS OF IC SWITCHES AND MULTIPLEXERS IN SAMPLE-AND-HOLD APPLICATIONS

4.6.1 Multichannel Systems

IC multiplexers are often more desirable than their discrete counterparts in systems involving a large number of channel selections. In the case of an *N*-way multiplexer where the common output line is connected to a sampling capacitor, considerable error can result due to leakage current flow out of, or into, the drain of the multiplexer. This current can be *N*-times that of a single channel and may result in unacceptable capacitor droop rates. A MOSFET placed in series with the multiplexer output (Fig. 4.24) drastically reduces the leakage current flowing out of the capacitor. This results in a much lower droop rate.

Fig. 4.24 **Reduction of leakage using an intermediate MOS stage.**



Multichannel system. SW_2 is used to reduce leakage current flowing into/out of the capacitor.

With the additional MOSFET, the leakage requirements of the multiplexer need not be critical, as leakage out of the capacitor into the multiplexer will now be entirely governed by the single MOSFET (SW_2). Any of the present range of Siliconix multiplexers could be used; e.g. the 4-channel DG172, 8-channel DG501, or 16-channel DG506.

4.6.2 Low Level Analogue Voltages

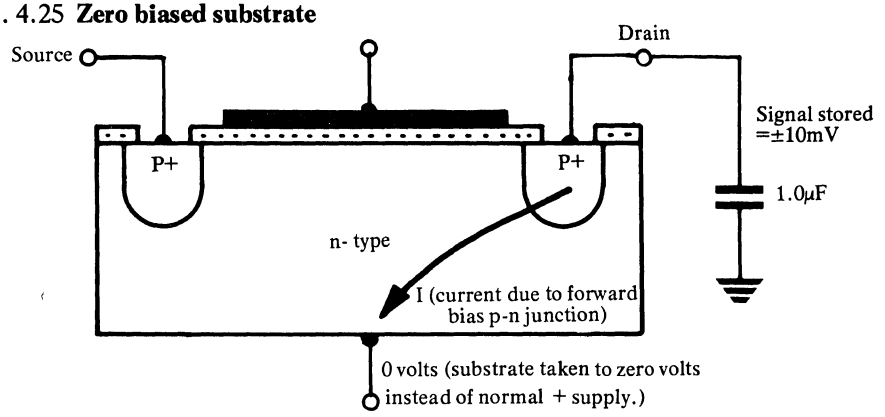
Many applications require the use of multiplexers for switching low level analogue signals down to tens of millivolts. In this case, the substrate of a PMOS multiplexer could be taken to zero volts instead of the normal positive voltage supply. Where the analogue voltage range is greater, it is necessary that the substrate be taken to a positive voltage which is at least equal to the peak value of the positive analogue signal. This ensures that substrate-source or substrate-drain does not become forward biased. With analogue signals of ± 10mV, and with the substrate grounded, the maximum amount of forward bias that the source/drain-substrate can be subjected to is 10mV. In this case, the amount of droop during the OFF state of the switch is governed by the current flowing out into the substrate via the forward biased drain-to-body junction.

The magnitude of this current can be calculated from the knowledge that (1) leakage current across a p-n junction is approximately proportional, at higher values of reverse bias voltage, to the square root of voltage, and (2) the current/voltage relationship for a p-n junction i.e.

$$I = I_0\left[\exp\left(\frac{eVj}{kT}\right) - 1\right]$$

For example, the drain-substrate current for a DG172 multiplexer is around 150pA for a reverse bias of -20 volts. For a forward bias of +10mV, the drain-to-body current will be approximately 20pA. With a 1.0μF capacitor (Fig. 4.25), this would give an initial droop rate of 20μV/sec; i.e., a loss in accuracy of 0.2%/sec for a 10mV signal.

Fig. 4.25 **Zero biased substrate**



This method automatically eliminates the need for a positive substrate supply. The Siliconix series of PMOS ICs and multiplexers would include the DG125, DGM111, DG170 and DG501 families.

4.6.3 **Time Compression of Analogue Samples.**

It is often necessary *(Refs. 4.2, 4.3)*, in order to reduce information processing time, to time-compress analogue samples when multiplexing on to a common line. It may also be required to delay these samples before they enter into the processing unit.

A typical problem which illustrates the use of a sample-and-hold system in a time-compression application is as follows :

Problem :

Assume 72 independent analogue channels are to be multiplexed into a processing unit (Fig. 4.26), with the following constraints :

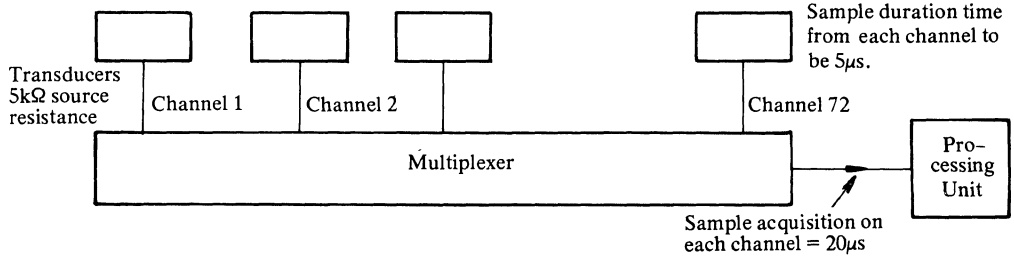
i) The analogue signal, acquired from each channel, be held for 20μs before further processing.

ii) Due to varying analogue signal value, individual channel sampling time must be limited to 20μs max; the analogue signal source resistance on each channel is 5kohms.

iii) The duration of each sample entering the processing unit must be 5μs with minimal redundancy time between each successive sample.

iv) Due to restriction in available space, the system must have a minimal number of packages.

Fig. 4.26 **Block diagram layout of 72-channel time compression system.**



Solution :

Sample Delay

The analogue samples from each channel must be stored for a period of 20μs with a minimum loss in accuracy. This involves the use of a capacitor arrangement for storing the information (Fig. 4.27). The maximum capacitor value allowable can be found from the 20μs (max) sampling time and the 5kohms source resistance:

For 99% accuracy, 4CR = 20μs.

$$C = \frac{20}{10^6} \times \frac{1}{4 \times 5k\Omega} = 1000pF$$

Minimal number of components

16-channel DG506s or 8-channel DG503s could be utilized to minimise the system's total package count. Fig. 4.27 shows the use of DG503 multiplexers which are available in 16-lead dual-in-line packages and are TTL input logic compatible.

Accuracy

Each sample has to be stored for 20μs without any appreciable loss in sample accuracy. The loss in accuracy will be determined mainly by capacitor droop rate which, as shown previously, is determined by the net leakage current flowing from the capcitor. With a DG503, the maximum leakage out of the capacitor into the common drain can be 8nA at 25°C. Simultaneously, the maximum capacitor value is limited to 1000pF. Initial droop rate will therefore be

$$\frac{dV}{dt} = \frac{8nA}{1000pF} = 8 \text{ volts/sec.}$$

Since the storage period on each capacitor is 20μs, the overall droop during this time will be 160μV.

The leakage through the remaining OFF switch (i.e. switch A, B etc.—Fig. 4.27) will be much less than 1nA provided the switch is a DG181 type, so that droop rate due to this 1nA leakage current is

$$\frac{dV}{dt} = \frac{1}{10^9} \div \frac{1000}{10^{12}} = 1 \text{ volt/sec.}$$

and in comparison with 8 volts/sec. can be neglected.

For small analogue signals, the above droop may be unacceptable. If required, this can be drastically reduced by including an additional single channel switch such as a DG181 between each capacitor and each drain of the DG503s.

Sample duration time with minimum redundancy time between samples *(Fig. 4.27 and 4.28).*

Switches A to I (SWA to SWI) should have very low t_{on}/t_{off} times, much less than 5μs. A DG181, for example, will give t_{on} and t_{off} times of 150ns and 130ns (max) respectively. This allows 5μsec samples to be extracted from each capacitor with negligible delay between samples.

Fig. 4.27 **A time compression system – 72 channels comprising nine DG503s (A to I).**

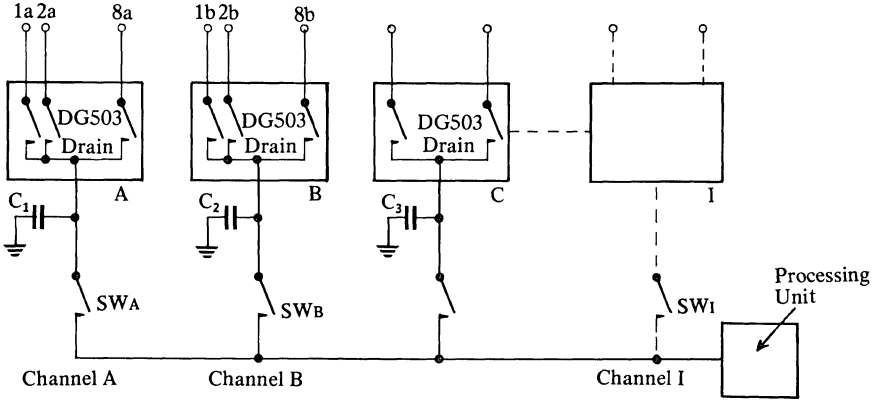
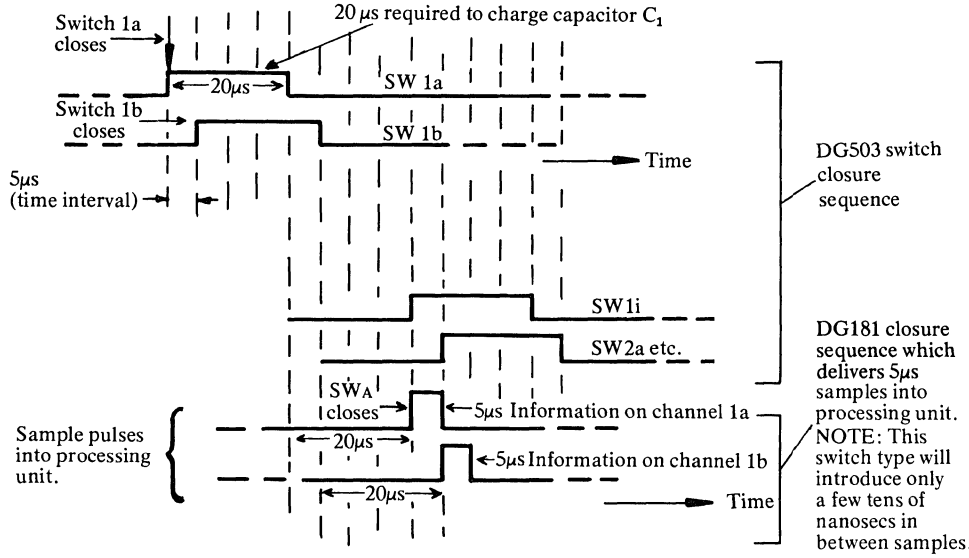


Fig. 4.28 **Switching waveforms for Fig. 4.27.**



4.6.4 Use of a 'Flying' Capacitor to eliminate Common Mode Signals

It is very often necessary to sample and store differential analogue voltages in the presence of a common mode voltage. A high common mode rejection amplifier is required, especially if the analogue signal is much less than the common mode voltage. In a sample-and-hold application, a second amplifier would be required as a buffer stage (Fig. 4.29).

An alternative that eliminates the need for a high CMRR amplifier is that using a Flying Capacitor technique. One capacitor and four break-before-make analogue switches would replace the high CMRR amplifier. Fig. 4.30 shows the layout of this alternative system.

Fig. 4.29 **System employing a high CMRR amplifier.**

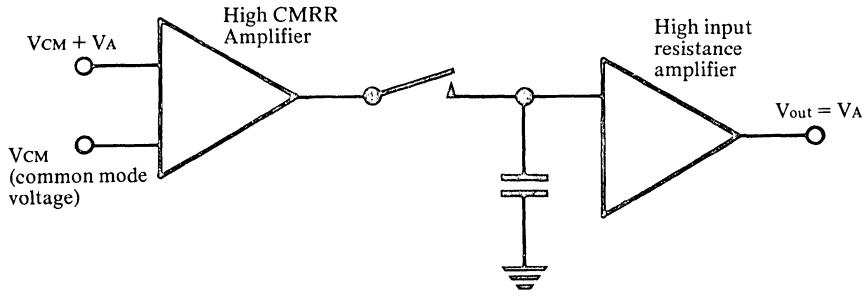
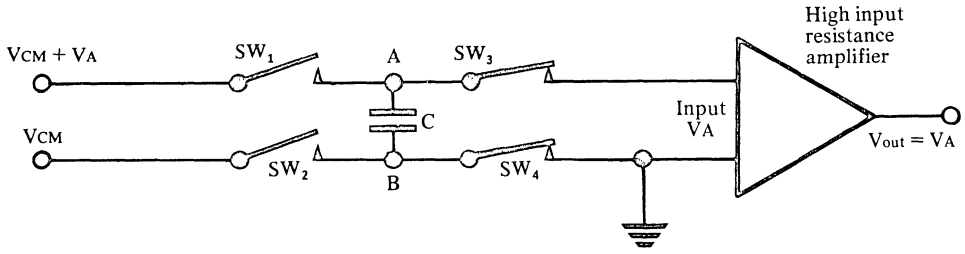


Fig. 4.30 **4-switch integrated circuit used to replace high CMRR amplifier.**



Operation :

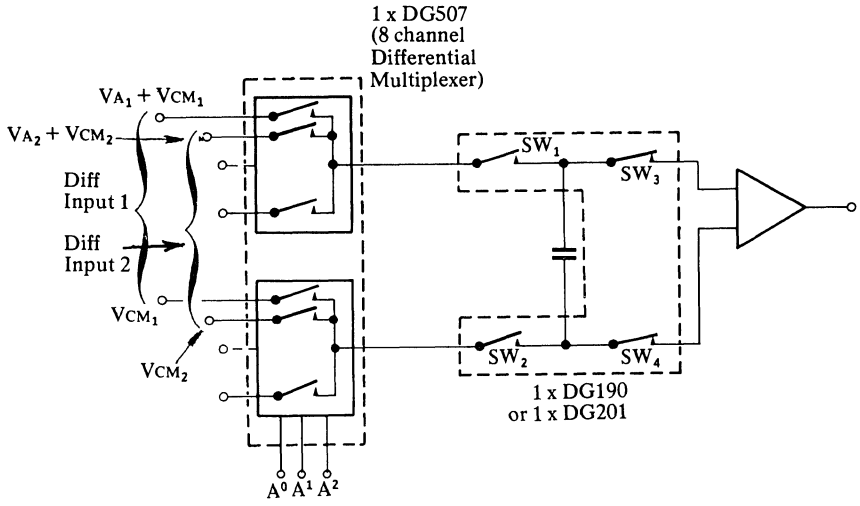
Switches SW_1 and SW_2 are normally open, and SW_3 and SW_4 normally closed. Switching action is such that SW_3 and SW_4 open before SW_1 and SW_2 close, i.e. break-before-make switching action. On receiving the appropriate logic control signal, SW_3 and SW_4 open, and SW_1 and SW_2 close. The capacitor charges up so that the true voltage at B is the common mode voltage (V_{CM}) and at A is $V_{CM} + V_A$. SW_1 and SW_2 are now opened and subsequently followed by closure of SW_3 and SW_4. The voltage appearing across the amplifier input (Fig. 4.30) when SW_3 and SW_4 close will be the differential voltage V_A only. This system will provide high rejection of the common mode voltage. The simultaneous turn off of SW_1 and SW_2, followed by the simultaneous turn on of SW_3 and SW_4, ensures that any voltage switching spikes generated, which otherwise might be stored as an error voltage across capacitor C, cancel one another.

Examples of switch types that could be used are Siliconix DG201 and DG190, each type provides 4 switches in a 16-lead dual-in-line package.

The elimination of the first amplifier stage also removes the source of error due to amplifier offset-drift. This would contribute to voltage errors across the capacitor.

The technique could be extended for use in a large scale multiplexing system. Fig. 4.31 shows the use of a DG507 8-channel differential multiplexer in conjunction with DG201 or DG190 analogue switches.

Fig. 4.31 **Use of 'Flying Capacitor' in a large scale multiplexing system.**



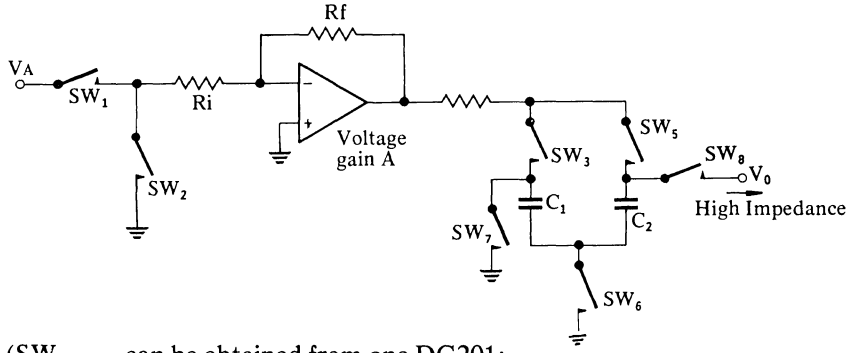
With a DG507, any one pair of 8 differential channels can be closed simultaneously depending on the state of the binary control inputs A_0, A_1, and A_2. SW_1, SW_2, SW_3 and SW_4 would operate simultaneously with any one pair of DG507 switches.

In this application, SW_1 and SW_2 are single switches, having independent drains/sources and therefore reduce leakage current between the capacitor and the *N* way multiplexer when they are OFF.

4.6.5 Reduction of Amplifier Offset and Drift

Output drift is one of the main parameters which can restrict the use of general purpose amplifiers in low d.c. analogue signal applications. The use of expensive chopper amplifiers is often necessary to achieve the low drift required. Combining FET switches with general purpose amplifiers in a sample-and-hold configuration (Fig. 4.32) can prove to be a very cost effective way of reducing amplifier drift.

Fig. 4.32 **Reducing amplifier drift and offset using a low cost Op-Amp together with integrated circuit analogue switches.**



($SW_{1,2,7,8}$ can be obtained from one DG201;
$SW_{3,5,6}$ can be obtained from a second DG201)

Operation :

The output voltage Vo is the amplified version of the input signal and is available as a rapid succession of samples whose magnitude are proportional to the analogue input. Each sampling cycle is determined by the charging times of the capacitors C_1 and C_2, and the response of the amplifier. With 0.1μF capacitors, the analogue input can be sampled at regular intervals of 0.5ms or so. The switching operation can be defined by the following steps :

At time t_1 close SW_2, SW_3, SW_6. C_1 charges up to amplifier's output offset voltage V_{offset}.

" t_2 open SW_2, SW_3, SW_6. C_1 is now charged up to V_{offset}.

" t_3 close SW_1, SW_5, SW_6. C_2 charges up to ($V_{OFFSET} - AV_A$)

" t_4 open SW_1, SW_5, SW_6. C_2 is now charged up to ($V_{OFFSET} - AV_A$)

" t_5 close SW_7, SW_8. Total voltage stored across C_1 and C_2 is :
($V_{offset} - AV_A$) - V_{offset} = - AV_A.

$$\therefore V_0 = -AV_A = -\frac{Rf}{Ri} . V_A$$

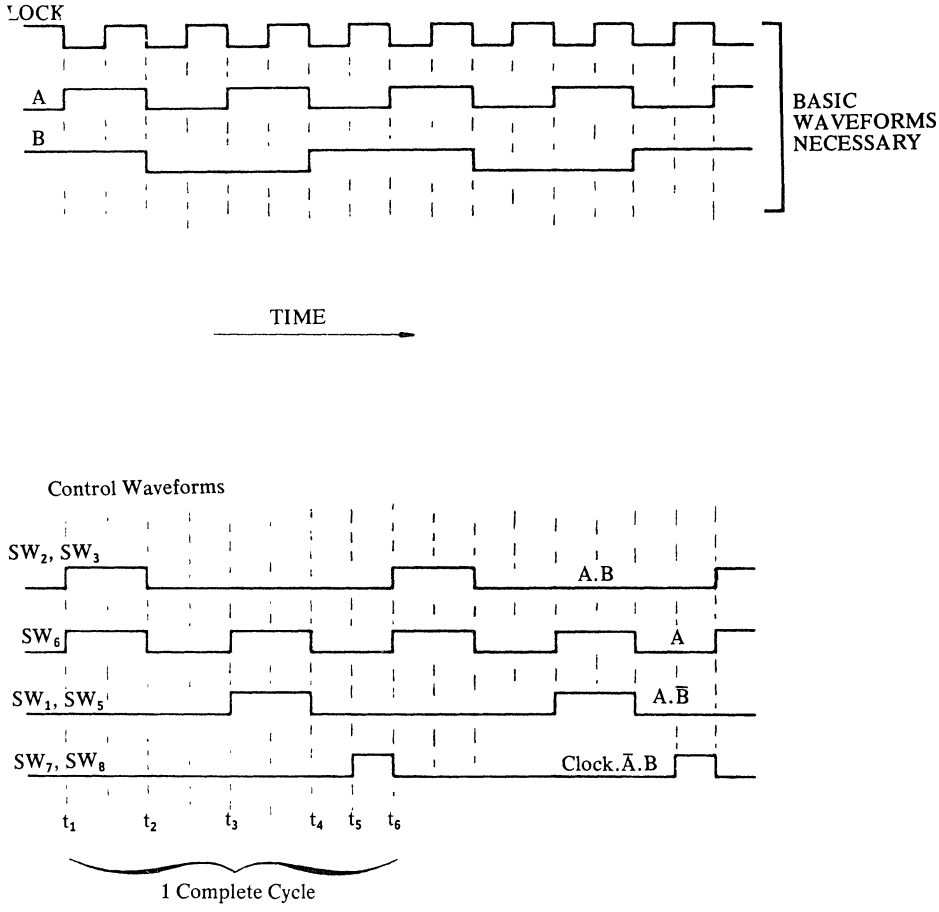
" t_6 open SW_7, SW_8

" t_6 close SW_2, SW_3, SW_6 etc.

The particular switching sequence explained in the above operation will reduce voltage errors that may be developed across C_1 and C_2 due to ON-OFF and OFF-ON switching transients. For example, SW_3 and SW_6 are identical and turn off simultaneously: the charge transferred into C_1 by SW_3 is cancelled by the charge transferred into the same capacitor C_1 by SW_6. Any error voltages due to switching transients would be practically constant with time and temperature. With $C_1 = C_2 = 0.1\mu F$, these could be kept to within tens of microvolts.

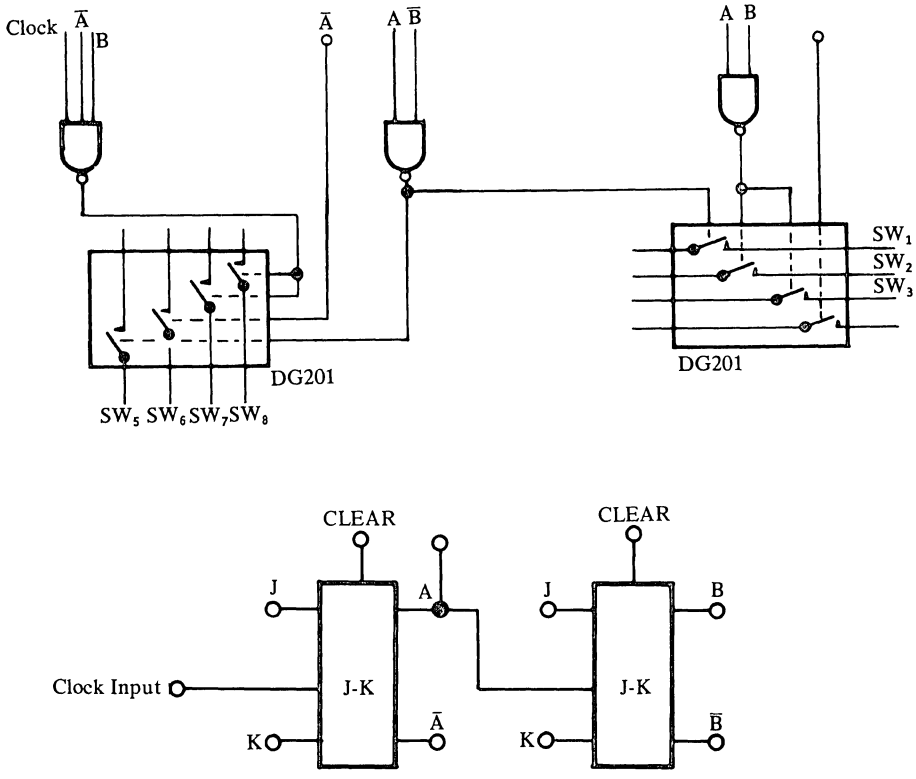
Figs. 4.33 and 4.34 show the corresponding switching waveforms and logic control required.

Fig. 4.33 **Control waveforms for Fig. 4.32**



The logic waveforms shown can be generated using the logic control shown in Fig. 4.34

Fig. 4.34 **Logic control circuit.**



Total Components
2 x DG201, 1 x triple 3 input NAND, 1 x dual J-K flip-flop

4.7 LOW LEVEL SAMPLE-AND-HOLD *(Ref. 4.4)*

Low level voltages are generated in many transducer applications. For such applications, involving sampling and holding of the analogue signal, it is necessary to know the error voltage established across the sampling capacitor due to feedthrough resulting from the on-to-off switch action. This section compares the accuracy achieved using integrated circuits and discrete devices and will aid the designer to choose the correct type of switch.

Many of the points that must be considered in order to decide whether to use discrete FET analogue switches or IC analogue switches, have already been discussed in Chapter 2, sections 2.8.1, 2.8.2.

The monolithic integrated circuit has many advantages and although extremely suitable for a large variety of sample-and-hold applications, does not exhibit as much flexibility in electrical performance as the hybrid IC. The latter can, by means of the appropriate selection of output FET during device fabrication, have much lower ON resistance and considerably lower leakage. The driver chip design of Fig. 4.35 which is basic to all Siliconix's DG180/190 family also provides a much lower propagation delay time than any of the monolithic ICs and therefore gives a considerably lower overall switching time.

In comparison, a correctly selected discrete junction FET, although requiring additional discrete driver circuitry, can nonetheless outperform even the hybrid, being capable of transmitting lower error voltages. It also has an inherently faster switching time. The accessibility of the gate of the discrete FET allows direct application of external control voltages to the gate. The magnitude and ramp rate can be adjusted to minimise error feedthrough into the sampling capacitor. The problem of charge feedthrough is of paramount importance in low level sampling applications. The finer points that one should be aware of when selecting hybrids or discretes are indicated in the following section.

A detailed analysis of transmitted error voltage into the sampling capacitor during turn-off is given in the Appendix. These results can be used to compare the performance between the hybrid IC circuit and any discrete junction FET.

Five different cases will be considered namely :

Case 1. Standard range of IC hybrid using 5 volt pinch-off junction FET switches e.g. Siliconix DG181.

Case 2. IC hybrid using 1 volt pinch-off JFET switches.

Case 3. Discrete n-channel JFET with 5 volt pinch-off, (same FET as used in the hybrid of Case 1). In this case the gate subjected to an adjustable ramp voltage.

Case 4. Discrete n-channel JFET with 1 volt pinch-off (same FET as used in the hybrid of Case 2). Again, the gate is subjected to an adjustable ramp voltage.

Case 5. Small geometry n-channel JFET having inherently low capacitance and low pinch-off.

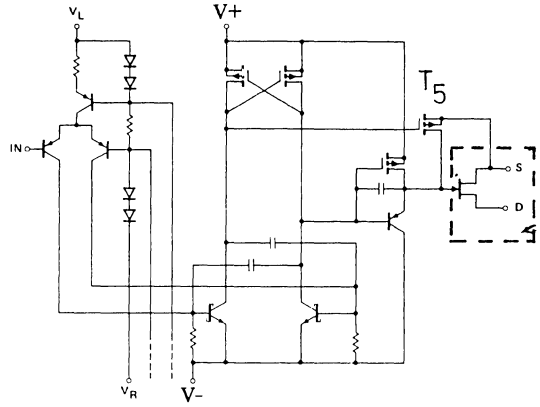
4.7.1 *Case 1.* **Standard IC hybrid using-5 volt pinch-off switching FETs.**

The standard Siliconix DG181 type hybrid integrated circuit will, with the appropriate logic input, give a negative transition at the output of the driver chip which will allow the n-channel JFET switch to turn off. This transition can be approximated to a negative going ramp having a gradient of -0.2 volt/nanosec. The output FETs will have a Vp of 5 volts.

For minimal voltage error feedthrough, the negative supply rail should be reduced to as low a value as possible. There is, however, a minimum limit to the negative supply rail voltage. It is necessary that this be a few volts more negative than the threshold voltage required to turn on the PMOS structures T_5 (Fig. 4.35). Since the minimum $V_{gs(th)}$ for T_5 is -2.4 volts (this is defined by the manufacturing process), it follows that an analogue signal of around zero volts

will require a negative supply rail of not less than -5.0 volts to ensure complete turn on of the MOSFET. In this case, however, the predominant factor governing the negative supply rail value will be the -5 volt pinch-off of the FET. It is therefore necessary to have a negative rail which is slightly more negative than this; e.g. -6 volts. The positive supply rail can be reduced to the value of the analogue signal, i.e. 0 volts.

Fig. 4.35 **Hybrid circuit showing bipolar MOSFET driver and discrete JFET output switch** (e.g. Siliconix DG181).



With a negative supply rail of -6 volts, a ramp rate of -0.2V/nanosec., and a low level analogue signal of a few millivolts, the OFF state of the switch will be achieved as the ramp reaches a negative value equal to the pinch-off voltage value. This will be achieved in

$$\frac{5 \text{ volts}}{0.2 \text{ volt/nanosec}} \quad \text{, i.e. 25 nanosecs.}$$

For the type of switching FET used in the DG181, the ON resistance corresponding to a Vp of 5 volts is 20 ohms and the typical C_{gs} is 4pF. With a sampling capacitor (load capacitance) of 10,000pF, both the exponential terms in equation A.4.6 of Appendix I can be calculated. The exponential terms are

$$\exp\left(\frac{t}{R_{on}(C_{gs}+C_H)} - \frac{Kt^2}{2R_{on}V_p(C_{gs}+C_H)}\right)$$

which must be calculated in order to find the error voltage established. In this equation, K is the gate voltage ramp rate.

It is unnecessary to use Simpson's Rule (see Appendix) for evaluating the integral which contains the above exponential term (equation A.4.6, Appendix I) since, the overall time t of the ramp is very much less than $R_{on}(C_{gs}+C_H)$, also t_2 is very much less than $2R_{on}V_p(C_{gs}+C_H)$. In fact the above exponential, is nearly $e^{0.1}$ which approaches unity.

With both the exponential terms of equation A.4.6 equal to unity, the error voltage (V_{error}) developed across the capacitor can be found simply from :

$$V_{error} = \frac{C_{gs}}{C_{gs} + C_H} \cdot \int_{t=0ns}^{t=25ns} k \cdot dt = \frac{4pF}{10{,}000pF} \times -0.2 \text{ volt/ns} \times 25ns$$

$$= \frac{4}{10000} \times 5 \text{ volts} = 2.0 \text{ millivolts.}$$

The 2 millivolts will be negative and will be the error introduced on to the sampling capacitor as the switch turns from ON to OFF.

Of course, this forms only part of the total error. The additional errors, which have not as yet been mentioned, are introduced into the sampling capacitor, when the ramp voltage exceeds the pinch-off voltage of the FET. In this particular case, the maximum magnitude of the ramp voltage (i.e. -6 volts) will be 1 volt more negative than the pinch-off voltage of the FET and this will incur an additional error of :

$$-(V - V_p) \cdot \frac{C_{gs}}{C_{gs} + C_H} = -(6.0 - 5.0) \times \frac{4}{1000} = -0.4 \text{ millivolts.}$$

The total error introduced into the sampling capacitor after the switch has turned off is therefore : -2.0mV -0.4mV = -2.4mV

Analysis of the above errors is given in Appendix I, section A.4.2.

4.7.2 *Case 2.* **IC hybrid using a-1 volt pinch-off JFET Switch.**

Using the same driver chip as Case 1 but with a lower pinch-off FET, the error can again be calculated. The ramp voltage will be -0.2 volt/nanosec. C_{gs} is 4pF and the $r_{DS(on)}$ corresponding to a 1 volt pinch-off is 60Ω. C_H = 10000pF. When these values are substituted into equation A.4.6, App. I, the exponential term again becomes practically unity, so V_{error} can again be calculated from :

$$V_{error} = \frac{C_{gs}}{C_{gs} + C_H} \cdot \int_{t=0ns}^{t=5ns} k \cdot dt = \frac{4}{10000} \times -0.2 \text{ volt/ns} \times 5 \text{ ns} = -0.4mV$$

This will be introduced on to the sampling capacitor as the FET turns OFF and corresponds to the input ramp going from 0 volts to -1 volt. As mentioned previously in section 4.7.1, the minimum negative supply rail (V-) for the DG181 type hybrid which we are considering here must not be less than -5.0 volts. So when turn-off occurs, the gate of the output FET will go to practically V- i.e. -5.0 volts.

This implies that an additional ramp excursion of —4.0 volts is applied to the gate of the FET after the FET has turned off. This will contribute an addition error of

$$\frac{C_{gs}}{C_{gs} + C_H} \times -(V - Vp) \text{ volts into the sampling capacitor i.e.}$$

$$\frac{4}{10000} \times -4.0 \text{ volts} = -1.6 \text{ millivolts.}$$

The total error introduced will be the sum of these two error components, and will be :

$$= -0.4mV - (V-Vp) \cdot \frac{Cgs}{Cgs + C_H}$$

$$= -0.4mV - 1.6mV$$
$$= -2.0mV$$

4.7.3 *Case 3.* **Discrete n-Channel JFET with —5 volt pinch-off.**

Here a direct comparison is made between the hybrid circuit of Case 1, where a low ON-resistance switching JFET is used in conjunction with an integrated driver, and the same FET used in discrete form with a discrete driver. In this case, an adjustable ramp can be applied directly to the FET gate. For a —6 volt ramp having a ramp rate of —0.2 volt/nanosec, the error will be exactly as in Case 1.

However, V_{error} may be found for any ramp rate. Consider a ramp of —1 volt/μsec, V_p and $r_{DS(on)}$ of the FET are 5 volts and 20Ω respectively, $C_{gs} = 4pF$ and $C_H = 10000pF$ as before. The exponential terms which were deduced from equation A.4.6, Appendix I are

$$\exp\left\{\frac{t.10^{12}}{(20)(10000)} - \frac{t^2 \cdot 10^6 \cdot 10^{12}}{2(20)(5)(10000)}\right\} = \frac{t.10^7}{2} - \frac{t^2.10^{12}}{2}$$

The overall time for the ramp to execute a transition between 0 volts and pinch-off of 5 volts is 5μ secs. The exponential term then becomes very much greater than unity and therefore the V_{error} may be found by evaluation of equation A.4.6, Appendix I, using Simpson's Rule for evaluating integrals.

The integral in the numerator becomes :

$$\int_{t=0}^{t=5\mu s} \left(\frac{t.10^7}{2} - \frac{t^2.10^{12}}{2}\right) dt$$

which when evaluated by Simpson's Rule is:

$$\frac{1}{3} \cdot \frac{(5\mu s - 0\mu S)}{N}\left[(X_1 + X_{N+1} + 4(X_2 + X_4 + ... + X_N) + 2(X_3 + X_5 + ... + X_{N-1})\right]$$

If the time interval of 5 μs is divided into ten equal parts, the value of N in the above expression will be 10.

Evaluation of the ordinates X_1, X_2 etc. can be found as follows :

$X_1 = 0$ since the value of error at t = 0 is zero.
X_2 (at t = 0.5μS) = exp (2.5-.125) = 9.97
X_3 (at t = 1.0μS) = exp (5.0 -0.5) = 9 x 10^1
X_4 (at t = 1.5μS) = exp (7.5 -1.25) = 6.65 x 10^2
X_5 (at t = 2.0μS) = exp (10.0 -2.0) = 2.98 x 10^3
X_6 (at t = 2.5μS) = exp (12.5 -3.1) = 8.1 x 10^3
X_7 (at t = 3.0μS) = exp (15.0 -4.5) = 3.63 x 10^4
X_8 (at t = 3.5μS) = exp (17.5 -6.125) = 5.98 x 10^4

X_9 (at t = 4.0μS) = exp (20.0- 8.0) = 1.62 x 10^5
X_{10} (at t = 4.5μS) = exp (22.5-10.1) = 2.42 x 10^5
X_{11} (at t = 5.0μS) = exp (25.0-12.5) = 2.68 x 10^5

Substituting these values of ordinates in eqn. A.4.7, the evaluated integral becomes :-

$$1/3 \times 0.5\mu s \left\{ 0 + 2.68(10^5) + 4[9.97 + 6.65(10^2) + 8.1(10^3) + 5.98(10^4) + 2.42(10^5)] + 2[9(10^1) + 2.98(10^3) + 3.63(10^4) + 1.62(10^5)] \right\}$$

This reduces to $1/3 \times 0.5\mu s \times 19.0(10^5)$

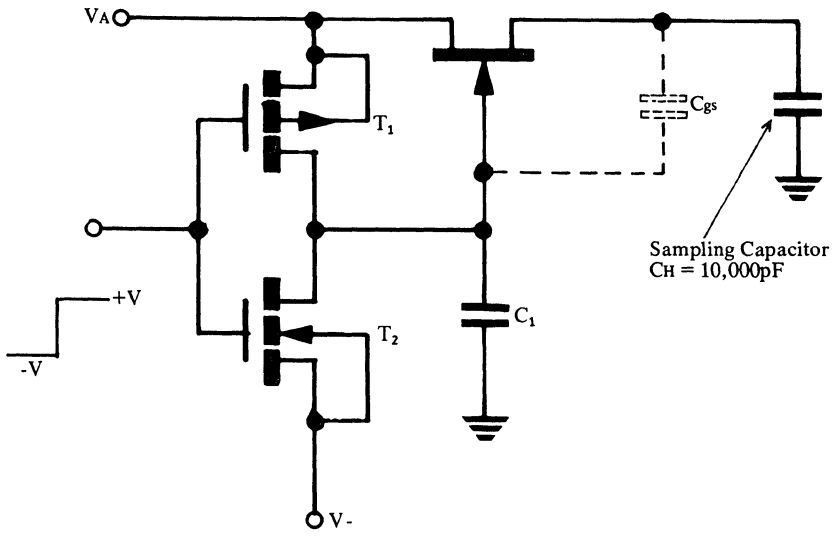
Combining this with equation A.4.6, Appendix I.

$$V_{error} = \frac{C_{gs}}{C_{gs} + C_H} . K \cdot \frac{1/3 \times 0.5\,\mu S \times 19.0 \times 10^5}{2.68 \times 10^5}$$

$$= \frac{4 \times -1 \text{ volt}/\mu s \times 1/3 \times 0.5\mu s \times 7.1}{10000} = -4.73 \times 10^{-4} = -0.47 \text{ millivolts}$$

To find the total error introduced into the sampling capacitor reference can be made to Fig. 4.36 which shows the Junction FET driven by a complementary pair of MOS structures.

Fig. 4.36 **Discrete JFET + Driver can be used for minimising feedthrough errors into capacitor.**



The capacitor C1 is incorporated to slow down the input ramp to the required value of 1 volt/μsec. For a FET with a Vp of -5 volts, it is advisable to take V- to a slightly more negative value than -5 volts. In this example, a negative rail of -6 volts is taken.

The total error transmitted into C_H during turn off will therefore be the sum of the error introduced as the ramp goes from 0 volts to the FET's Vp value of —5 volts and that introduced when the ramp goes from pinch-off to V-. The error will therefore be :

$$-0.47 \text{ millivolts} - (V - Vp)\ \frac{C_{gs}}{C_{gs}+C_H} = -0.47 - 1.0\ \frac{C_{gs}}{C_{gs}+C_H}$$

$$= -0.47 - 0.4 = -0.87 \text{ millivolts.}$$

4.7.4 *Case 4.* **Discrete n-Channel JFET with −1 volt pinch-off.**

To show how selection of pinch-off voltage affects the error introduced, the errors can be recalculated exactly as in Case 3, but with a FET having a Vp of —1 volt instead of —5 volts.

Here, the constants will be Vp = —1 volt, $r_{DS(on)}$ corresponding to Vp of 1 volt = 60Ω, C_{gs} = 4pF, C_H = 10000pF, K = —1 volt/μsec.

Using the same configuration as Fig. 4.36, the negative supply voltage need only be slightly more negative than the Vp of the FET, i.e. —1.5 volts say, so the total error transmitted into C_H will be :

$$-0.3 \text{ millivolts} - (V - Vp)\ \frac{C_{gs}}{C_{gs}+C_H} = -0.3 - (1.5 - 1.0) \cdot \frac{4}{10000}$$

$$= -0.3 - 0.2 \text{ millivolts} = -0.5 \text{ millivolts.}$$

4.7.5 *Case 5.* **Discrete n-Channel JFET (low OFF-leakage, low Cgs).**

If the application requires a very low OFF-leakage switch and can tolerate a reasonably higher ON resistance, a small geometry n-channel FET can be used e.g. a Siliconix NT geometry (2N4117) FET. This geometry also has an inherently small junction capacitance.

For an NT geometry FET with a -1 volt pinch-off $r_{DS(on)}$ is 7kΩ, and C_{gs} = 1pF. When this FET is used in the configuration of Fig. 4.36 with a —1.5 volt supply, a ramp of —1 volt/μsec., and C_H = 10000pF the total error can be calculated to be :

-0.1 millivolts (error due to gate swing from 0 volts to -1 volt) + error due to ramp exceeding the Vp value.

$$= -0.1\text{mV} - (V - Vp)\ \frac{C_{gs}}{C_{gs}+C_H} = -0.1\text{mV} - (1.5 - 1.0)\ \frac{1}{10000} = -0.15\text{mV}$$

4.7.6 **Hybrid IC or discrete Junction FET?**

Both the hybrid integrated circuit and the discrete JFET are preferable to discrete MOSFETs or IC MOSFETs in most applications where the analogue signal range is in millivolts, because of the smaller gate voltage drive required.

The magnitude of feedthrough error in sample-and-hold systems is related directly to many factors and may be minimised by :

a) Reducing the ratio of FET switch capacitance to load capacitance.

b) Keeping the ON-to-OFF voltage swing at the gate of the FET to the absolute minimum required.

c) Using as slow a gate-voltage ramp-rate as possible.

d) Using a low pinch-off JFET

e) Reducing the supply voltages to the minimum acceptable, compatible with the analogue signal range.

When using hybrid ICs with analogue voltages around zero, the negative supply can be reduced to a value which is well below that specified on the standard data sheets. Different types of hybrid ICs will operate with different minimum supply voltages. The customer should therefore seek the manufacturer's advice before use.

The discrete driver circuit with the correct selection of JFET will provide lower feedthrough than an uncompensated IC since the ramp rate in the former case is externally controlled. Of course, compensation techniques can be used with the IC to give practically zero feedthrough (refer to section 4.5.2.4). Hybrid ICs are obtainable with up to 4 switches in 16-lead dual-in-line packages.

The discrete FET will require a discrete driver for interfacing with the logic input control and in comparison with the IC, an overall set of 4 switches will therefore be much bulkier and probably more expensive. Selection of low pinch-off, low capacitance discrete JFETs can, however, give very low inherent feedthrough errors (Case 5 of section 4.7.5 shows that this could be much less than 150μV for an NT geometry JFET having a pinch-off of 1 volt, provided that the ramp rate of the applied gate control voltage, is slower than 1 volt/μsec). In some applications where it is essential to have extreme accuracy but unnecessary to have fast switching speeds, a discrete JFET combined with a discrete driver is certainly the better choice.

4.8 APPLICATION CIRCUITS

The following is a list of applications pertaining to Chapter 4 which can be found in "Applications Information," Chapter 7. Please refer to the page number indicated.

4.8.1 Simple Sample and Hold Circuits

.1 *8 Input Sample and Hold* – AN75-1, Page 7-74, Figure 19.

.2 *Inverting Sample and Hold Circuit* – AN74-2, Page 7-59, Figure 7.

4.8.2 Charge Coupling Compensated Sample and Hold Circuits

.1 *Improved Inverting Sample and Hold Circuit* – AN74-2, Page 7-59, Figure 8.

.2 *High-Performance Non-Inverting Sample and Hold Circuit* – AN74-2, Page 7-60, Figure 9.

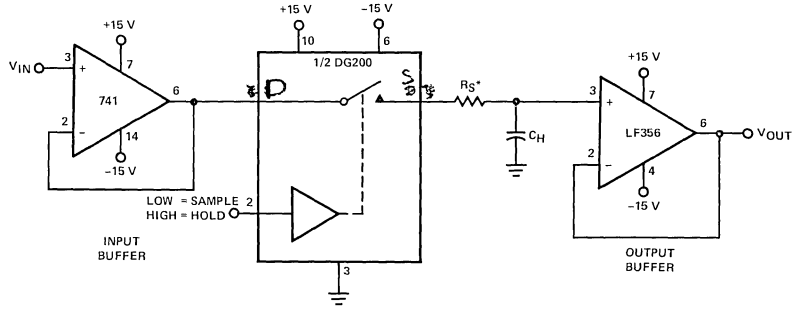
.3 *DG201 Sample and Hold* – AN74-2, Page 7-60, Figure 10.

.4 *DG303 Sample and Hold* – AN76-6, Page 7-82, Figure 11.

.5 *Charge Compensated Sample and Hold* – AN74-2, Page 7-61, Figure 12.

4.8.3 Additional Sample and Hold Circuits

Figure 4.37 **Single Switch Sample and Hold**



*If the signal source impedances are greater than 300 Ω or the analog signal range is restricted to less than ±5 V, R_S may be omitted

(Metal can pinouts given)

C_H	5 V Step Acquisition Time to 98% of Final Value	(With R_S = 0 Ω) Sample to Hold Offset	Droop Rate
0.001 μF	1.2 μsec	70 mV	≈ 60 mV/sec
0.0047 μF	3.6 μsec	16 mV	16.3 mV/sec
0.010 μF	4.6 μsec	7.5 mV	6.8 mV/sec
0.033 μF	7.8 μsec	2.5 mV	2.4 mV/sec
0.100 μF	35 μsec	1 mV	0.4 mV/sec

4.9 REFERENCES

4.1 James S. Sherwin, "Cut Transients in FET Analog Switches," Electronic Design 9, April 27, 1962

4.2 J.O.M. Jenkins, "IC Multiplexer Increases Analog Switching Speeds," Siliconix Application Note, Feb. 1973. (AN73-2, p. 7-9.)

4.3 Roberts – Jenkins, "Multiplexer Adds Efficiency to 32-Channel Telephone Systems," Siliconix Application Note, Jan. 1973. (TA73-1, p. 7-93.)

4.4 G. Dixon, "Analog Switches in Sample-and-Hold Circuits," Siliconix Application Note, May 1974. (AN74-2, p. 7-57.)

Chapter 5

N-path Filters

5.1 INTRODUCTION

The design of high selectivity bandpass filters using conventional analogue techniques is complicated by many factors. For example, with passive RLC filters, the circuit selectivity is largely dependent on the quality factor of the inductor. This means that for high Q applications an intolerably large and expensive inductor is required, particularly at audio and sub-audio frequencies. At these frequencies inductors also exhibit non-linearity and dissipate excessively high power.

Passive networks consisting of only resistors and capacitors are unsuitable since the poles of the network are always real whereas, to approximate any network with the least overall number of poles it is necessary to have complex poles. If inductors are used as network elements then complex poles are possible. This is why passive filters contain inductors in almost all cases.

One method of eliminating the inductor is, of course, to use an active element in conjunction with RC passive networks, in this way the poles of the network are not confined to the real axis. However, in many applications the stability and sensitivity problems associated with active RC networks can be a major disadvantage particularly when high selectivity bandpass or band reject networks are required. One way of reducing network sensitivity is to use the well known state variable techniques *(Ref. 5.1)* which enable low sensitivity, high performance filters to be readily designed *(Ref. 5.2)*. However, this approach has its limitations: the frequency dependence of the open loop gain of the active element introduces excessive phase shift which produces Q-enhancement and, ultimately, oscillation if the $Q\omega_0$ product is high, where $\omega_0 = 2\pi f_0$ and f_0 is the centre frequency. Although simple phase correction circuitry *(Ref. 5.3)* can be utilised, the nonlinear phase lag introduced by amplifier slew rate limiting drastically limits the operating frequency range. Quality factors of up to 1000 at low frequencies represents the practical performance limits of the state variable approach.

Another method of generating complex poles from RC passive networks is by the use of modulation and, in particular, the use of RC passive networks containing periodically operated switches. In this case the imaginary part of the complex poles generated by switching is directly related to the rate at which the switches are being operated so that sensitivity is reduced to the problem of providing a clock generator with a sufficiently stable output. Such networks are called N-path filters, in which N parallel RC lowpass sections each with an identical transfer function $H(j\omega)$. These are time division multiplexed into the signal path and were first described by Franks and Sandberg *(Ref. 5.4)*.

This type of filter has been found to provide many useful features:

a) Narrow-band bandpass and band elimination filters can be realised without the use of inductors.

b) Periodic filtering characteristics can be obtained over a limited frequency range which allows the simple realisation of comb filters without the use of distributed elements.

c) An exact lowpass to bandpass translated version of the constituent path network transfer function can be realised.

d) The bandwidth of the pass band is determined by the frequency response of the path networks and is therefore independent of centre frequencies.

e) The modulators can in most cases, be implemented with simple analogue switches. This allows the use of digital circuits to provide the necessary phasing and timing of modulating waveforms.

f) The centre frequency of the filter is determined by a clock oscillator and therefore electronic tuning can be easily realised.

Unlike the passive filter in which the inductive reactance determines the selectivity, in the N-path filter the values of R and C fix the bandwidth, and the frequency of the clock oscillator that drives the switches, determines the centre frequency. Therefore, the N-path filter eliminates the inductor and can provide extremely high values of Q.

5.2 BASIC N-PATH FILTER

The basic arrangement of the N-path filter is shown in Fig. 5.1. Each path contains an identical lowpass element H(jω), which, for the simplest case is the single pole RC section shown in Fig. 5.2. Note that the series resistor R can be combined with the input resistor R_1.

In operation, the N identical time invariant networks are cyclically switched into the signal path to provide the overall network with time-variable characteristics. Because low pass sections, whose time constants are arranged to be much greater than the switching period, are used for each of the H(jω) elements, the cyclical switching process causes a lowpass to bandpass transformation. The resulting transfer characteristic is symmetrical with respect to the switching frequency f_0.

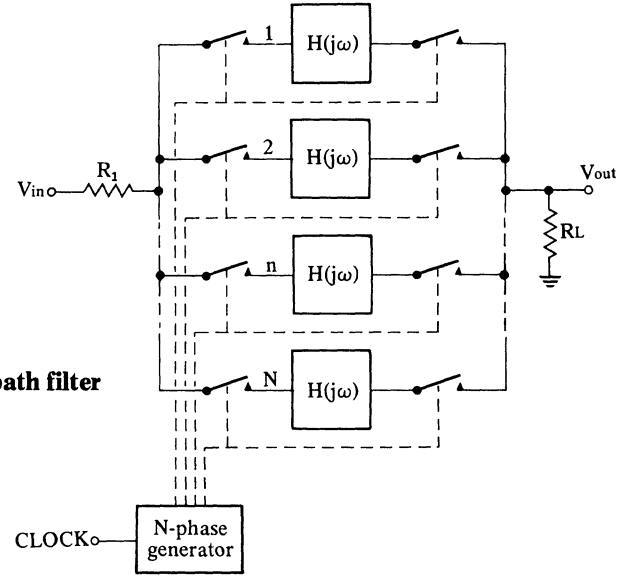


Fig. 5.1 **Basic N-path filter**

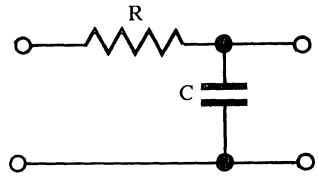


Fig. 5.2 **Single-pole RC section**

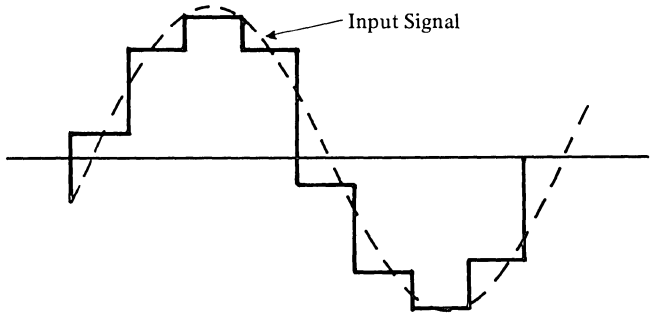


Fig. 5.3 **Typical input-output waveforms of a 4-path filter.**

For example, when a sine wave with a frequency identical to f_0 is applied to the input of the N-path filter , the capacitor in each of the paths is successively exposed to a segment of this input signal and the voltage on each capacitor ultimately reaches the average value of the applied signal *(Fig. 5.3)*. Each capacitor is switched into circuit for a period 1/N of each cycle and left floating for the remainder. The output at any given time is the voltage across the capacitor that is switched into the circuit at that time. Ideally, only when its associated switches are closed can a capacitor lose or gain charge.

In normal operation, the capacitors are switched at f_0. However, if the input frequency differs from f_0, the average value of the input voltage will differ for each successive time interval that the capacitor is connected. Because of the lack of synchronism between the input signal and the switching frequencies, the voltage across the capacitor varies at a rate dependent on the difference between the two frequencies. For large differences, the capacitors do not accumulate appreciable charge and the output voltage remains near zero. Since the charging rate is limited by the RC time constant which is large compared with the time that the switch is closed, the voltage across the capacitor becomes smaller, approaching zero as the difference between signal frequency and switching frequency becomes large. When the input and switching frequencies are in synchronism, each capacitor will, after several cycles, charge to the average sample value of the input signal. Since this happens to each capacitor, the synchronous sample and store action of each path produces an output which is a stepped approximation of the input waveform. A post lowpass filter or tuned circuit can be used to eliminate the sampling frequency components and the stepped appearance of the output signal. The resultant bandpass characteristic will be symmetrical about f_0.

The shape of this bandpass response is determined by the lowpass elements of each path. If each of the $(H(j\omega)$ elements has only one real pole (for example, see

Fig. 5.2) then the corresponding bandpass function will have a single pair of complex conjugate poles. Analogously, if active RC lowpass sections with conjugate complex pole pairs are used for the $H(j\omega)$ functions, the corresponding bandpass function will have twice as many pairs of conjugate complex poles. As we shall see in a later section, the selectivity or bandwidth depends on the number of paths and on the poles of $H(j\omega)$. Thus, by varying the centre frequency f_0, time variable bandpass characteristics with constant bandwidth can be obtained.

Due to the sampling action of the N-path system, output responses are obtained at zero frequency, at the centre (or sampling) frequency f_0 and at the harmonics of f_0. The response at zero frequency takes place only if energy is applied to the filter at this frequency. The overall form of the characteristic is typical of a sampled data system and the filter would have no response at Nf_0, $2Nf_0$, etc.

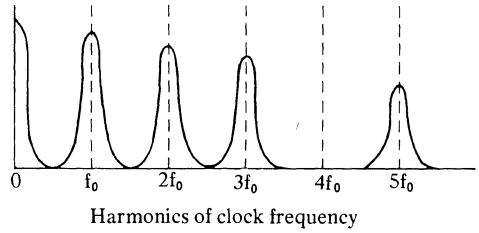


Fig. 5.4 **Output responses for 4-path filter**

Therefore, the output of the N-path system is a sequence of narrow passbands centred at multiples of ω_0 if the path networks have identical lowpass characteristics with a bandwidth small compared to ω_0. This feature, of course, provides useful comb filtering properties. When only a single passband is required, the N-path filter can be realised with a minimum of N = 3 if the input signal is bandlimited so that it does not exceed $\frac{Nf_0}{2}$. If this does occur then a form of distortion, known as aliasing *(Ref. 5.5)* can arise from undersampling. Aliasing results in a downward frequency translation. For example, in the particular case of a 4-path filter, an input signal applied at $3w_0$ would appear at the output translated to w_0. Since the filter samples at a frequency of Nf_0 (which is the clock frequency), then aliasing problems can be solved by limiting the input spectrum to less than or equal to $\frac{Nf_0}{2}$.

5.3 ANALYSIS

In this section the general input-output relationship for the N-path filter is derived. Moreover, by bandlimiting the input and output signals, a transfer function can be determined. The case for a second order bandpass filter is analysed in detail in the next section.

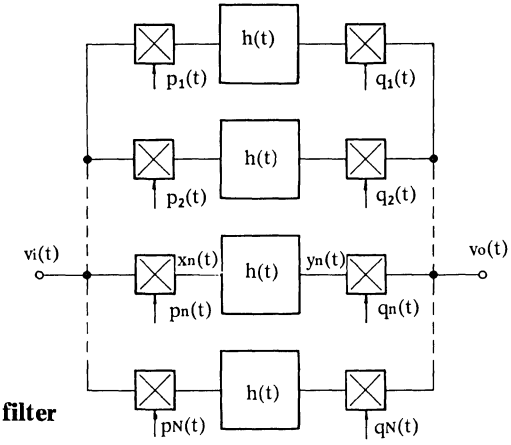


Fig. 5.5 **Block diagram of N-path filter**

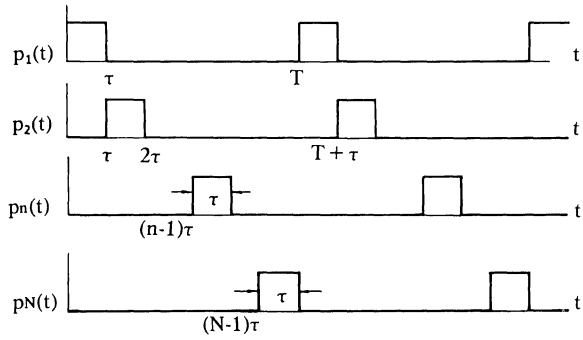


Fig. 5.6 **Modulator waveforms**

$\tau = \frac{T}{N}$

Expressing the modulator functions as a complex Fourier Series, we have

$$p(t) = \sum_{\alpha=-\infty}^{\alpha=\infty} P_\alpha \exp(j\omega_0 \alpha t)$$

$$q(t) = \sum_{\beta=-\infty}^{\beta=\infty} Q_\beta \exp(j\omega_0 \beta t)$$

where $\omega_0 = \frac{2\pi}{T} = \frac{2\pi}{N\tau}$ eqn. 5.1

$$\text{now } p_n(t) = p[t-(n-1)\tau] = \sum_{\alpha=-\infty}^{\alpha=\infty} P_\alpha \exp\left(j\omega_0 \alpha [t-(n-1)\tau]\right)$$

$$\text{and } q_n(t) = q[t-(n-1)\tau] = \sum_{\beta=-\infty}^{\beta=\infty} Q_\beta \exp\left(j\omega_0 \beta [t-(n-1)\tau]\right)$$

eqn. 5.2

From Fig. 5.6, we see that input modulator produces the following inputs to the N time invariant networks with impulse response h(t)

$$x_n(t) = v_i(t)\, p[t-(n-1)\tau] \qquad \text{eqn. 5.3}$$

Similarly, eqn. 5.4

$$v_0(t) = y_n(t)\, q\,[t-(n-1)\tau]$$

But multiplication in that time domain corresponds to convulation in the frequency domain so that

$$V_0(s) = \sum_{n=1}^{N} Y_n(s) \otimes Q_n(s) \qquad \text{eqn. 5.5}$$

Using the complex translation theorem (see Fig. 5.7) and equations 5.1, 2 and 4, we obtain

$$V_{0(s)} = \sum_{n=1}^{N} \sum_{\beta=-\infty}^{\beta=\infty} Q_\beta \exp(-j\omega_0(n-1)\beta\tau)\ \ X_n\,(s-j\beta\omega_0)\, H\,(s-j\beta\omega_0) \qquad \text{eqn. 5.6}$$

where $Y_n(s) = X_n(s).\ H(s)$
and $X_n(s) = V_i(s) \otimes P_n(s)$

Fig. 5.7 **Complex Translation Theorem**

$F(s) = \mathcal{L} f(t)$
$F(s+a) = \mathcal{L} f(t)e^{-at}$
$F(s-a) = \mathcal{L} f(t)e^{at}$

Now

$$X_n\,(s-j\beta\omega_0) = \sum_{\alpha=-\infty}^{\alpha=\infty} P_\alpha \exp(-j\omega(n-1)\alpha t)\, V_i[s-j\omega_0(\alpha+\beta)] \qquad \text{eqn. 5.7}$$

Substituting equation 5.7 into equation 5.5, we have

$$V_o(s) = \sum_{N}\sum_{\alpha}\sum_{\beta} P_\alpha Q_\beta \exp(-j\omega_0(\alpha+\beta)(n-1)\tau) V_i[s-j\omega_0(\alpha+\beta)]\, H\,(s-j\beta\omega_0) \qquad \text{eqn. 5.8}$$

The summation over n is the following geometric series

$$\sum_{n=1}^{N} \exp(-j\omega_0(n-1)(\alpha+\beta)\tau) = N \text{ for } \alpha+\beta = kN$$

where $k = \pm1, \pm2, \pm3 \ldots\ldots$ eqn. 5.9

The summation is zero for

$$\alpha + \beta \neq kN$$

Therefore, the only expressions of interest are where $\alpha + \beta$ are integer multiples of N. This is very important for the further evaluation of equation 5.8. Using equation 5.9 and substituting $\alpha = kN-\beta$, we can considerably simplify equation 5.8.

$$V_o(s) = N\sum_{k}\sum_{\beta} P_{kN-\beta}\, Q_\beta H\ (s-j\beta\omega_0)\, V_i\,(s-jkN\omega_0) \qquad \text{eqn. 5.10}$$

However, it is still necessary to sum equation 5.10 over two independent indices and the spectrum of V_0 contains an infinite number of overlapping terms. If the input signal is now fed via an ideal lowpass filter whose cut-off frequency is $\frac{N\omega_0}{2}$, then only the k = 0 term remains. Moreover, if a wideband bandpass filter, whose centre frequency is ω_0 (lower cut-off frequency $\omega_1 \geqslant \frac{\omega_0}{2}$ and upper cut off frequency $\omega_n \leqslant \frac{3\omega_0}{2}$) is connected to the output of the N-path filter, all terms except $\beta = \pm 1$ are eliminated. The output spectrum does no longer contain overlapping terms and a relationship between input and output spectrums can be derived

$$\frac{Vo}{Vi}(s) = N[P_{-1}Q_1 H(s-j\omega_0) + P_1 Q_{-1} H(s+j\omega_0)] \qquad \text{eqn. 5.11}$$

This expression represents the transfer function of the N-path network, whose frequency response is determined by the four-pole path networks, H(s), and the modulating frequency ω_0. The bandwidth of the passband depends entirely on the cut-off frequency of the path networks. If these networks are lowpass elements then from equation 5.11, a lowpass to bandpass transformation is evident.

To evaluate the Fourier coefficients P_α and Q_β, it is necessary to re-examine the modulating function shown in Fig. 5.8.

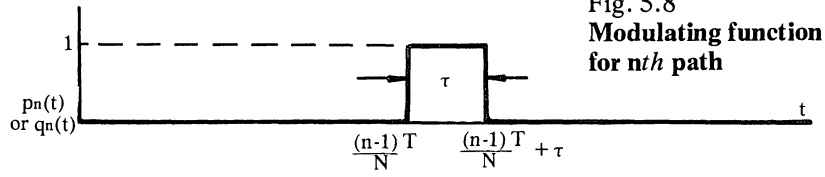


Fig. 5.8
Modulating function for n*th* path

We see that $p_n(t) = 1$ for $(n-1)\tau + (a+1)T \leqslant t \leqslant n\tau + (a-1)T$ eqn. 5.12
where $\tau = T/N$ and a = 1, 2, 3, ... and $p_n(t) = 0$ otherwise

$$\text{Now } P_\alpha = 1/T \int_0^\tau p(t) \exp(-j\omega_0 \alpha t)dt \qquad \text{eqn. 5.13}$$

$$= 1/T \int_0^\tau \exp\left(\frac{-j2\pi\alpha t}{N}\right)dt$$

From which we can obtain

$$P_\alpha = \exp\left(\frac{-j\alpha\pi}{N}\right) \cdot \frac{\sin\frac{\alpha\pi}{N}}{\alpha\pi} \text{ and similarly, } Q_\beta = \exp\left(\frac{-j\beta\pi}{N}\right) \cdot \frac{\sin\frac{\beta\pi}{N}}{\beta\pi}$$

$$\text{So that } P_1Q_{-1} = P_{-1}Q_1 = \frac{\sin^2\pi/N}{\pi^2} \qquad \text{eqn. 5.14}$$

and equation 5.11 becomes

$$\frac{Vo}{Vi}(s) = \frac{N \sin^2\pi/N}{\pi^2}[H(s-j\omega_0) + H(s+j\omega_1)] \qquad \text{eqn. 5.15}$$

Therefore, when a single passband is required the realisation can be accomplished with a minimum value of N = 3, since the transfer function relation is valid for $\omega < \frac{N\omega_0}{2}$. The band limiting filter required at the output can also provide a low frequency cut-off, so that the passband centred at d.c. can be eliminated.

5.4 BANDPASS FILTER ANALYSIS

Implementation of the transfer function of equation 5.15 with series sampling switches would require a current source at the input and negligible loading at the output. The analysis of a more practical circuit, including a source resistance R_1 and a load resistance R_2 is now examined.

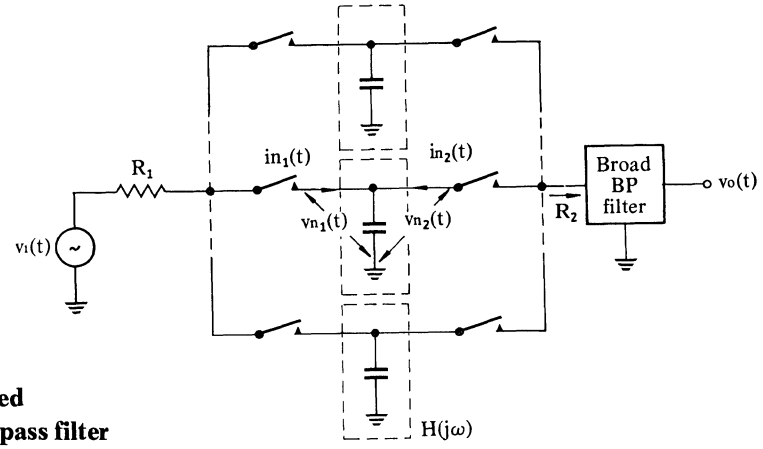


Fig. 5.9
Series switched narrow bandpass filter

By inspection of Fig. 5.9 we see that

$$i_{n_1}(t) = \frac{v_i(t) - v_{n_1}(t)}{R_1} \; p_n(t) \qquad \text{eqn. 5.16}$$

$$i_{n_2}(t) = \frac{-v_{n_2}(t)}{R_2} \; q_n(t) \qquad \text{eqn. 5.17}$$

$$I_{n_1}(j\omega) = \frac{1}{R_1} \sum_{\alpha=-\infty}^{\alpha=\infty} P_\alpha \exp(-j\alpha\omega_0(n-1)\tau) \; [V_i(j\omega - j\alpha\omega_0) - V_{n_1}(j\omega - j\alpha\omega_0)] \qquad \text{eqn. 5.18}$$

$$I_{n_2}(j\omega) = \frac{1}{R_2} \sum_{\beta=-\infty}^{\beta=\infty} Q_\beta \exp(-j\beta\omega_0(n-1)\tau) \; V_{n_2}(j\omega - j\alpha\omega_0) \qquad \text{eqn. 5.19}$$

Representing the component networks in terms of open-circuit impedance parameters.

$$V_{n_1}(j\omega) = Z_{11}(j\omega) \, I_{n_1}(j\omega) + Z_{12}(j\omega) \, I_{n_2}(j\omega) \qquad \text{eqn. 5.20}$$

$$V_{n_2}(j\omega) = Z_{21}(j\omega) \, I_{n_1}(j\omega) + Z_{22}(j\omega) \, I_{n_2}(j\omega) \qquad \text{eqn. 5.21}$$

Where $Z_{11} = \frac{1}{j\omega C}$ $Z_{12} = \frac{1}{j\omega C}$ $Z_{21} = \frac{1}{j\omega C}$ $Z_{22} = \frac{1}{j\omega C}$

The substitution of equations 5.18, 5.19 into equations 5.20, 5.21 results in infinite-order difference equations in V_{n_1} and V_{n_2}. However, choosing $H(j\omega)$ so that $H(j\omega) = 0$ for $|\omega| \geq \frac{\omega_0}{2}$

permits a considerable simplification of the equations since all terms other than $\alpha = 0$, $\beta = 0$ in the expressions involving V_{n_1} and V_{n_2} are eliminated

$$In_1 = \frac{1}{R_1} \sum_{\alpha} P_\alpha \exp\left(-j\omega_0\alpha\,(n\text{-}1)\,\frac{T}{N}\right) Vi(j\omega\text{-}j\omega_0\alpha) - \frac{P_0}{R_1} Vn_1(j\omega)$$

$$In_2 = -\frac{Q_0}{R_2} Vn_2(j\omega) \qquad \text{eqn. 5.22}$$

Rewriting equation 5.22 in terms of the open circuit parameters, we obtain

$$\left(1+\frac{Z_{11}}{R_1} P_0\right) Vn_1 + \frac{Z_{12}}{R_2} Q_0 Vn_2 = \frac{Z_{11}}{R_2} \sum_{\alpha} P_\alpha \exp\left(-j\omega_0(n\text{-}1)\,\frac{T}{N}\right) E_1(j\omega\text{-}j\alpha\omega_0) \qquad \text{eqn. 5.23}$$

$$\frac{Z_{21}}{R_1} P_0 Vn_1 + \left(1+\frac{Z_{22}}{R_2} Q_0\right) Vn_2 = \frac{Z_{21}}{R_2} \sum_{\alpha} P_\alpha \exp\left(-j\omega_0(n\text{-}1)\,\frac{T}{N}\right) E_1(j\omega\text{-}j\omega_0\alpha) \qquad \text{eqn. 5.24}$$

Eliminating V_{n_1} from equation 5.23

$$Vn_2(j\omega) = \frac{1}{P_0} G(j\omega) \sum_{\alpha} P_\alpha \exp\left(-j\omega_0\alpha\,(n\text{-}1)\,\frac{T}{N}\right) E_1(j\omega\text{-}j\omega_0\alpha) \qquad \text{eqn. 5.25}$$

Where

$$G(j\omega) = \frac{Z_{21}\,\frac{R_2}{Q_0}}{\left(Z_{11}+\frac{R_1}{P_0}\right)\left(Z_{22}+\frac{R_2}{Q_0}\right) - Z_{12}Z_{21}} \qquad \text{eqn. 5.26}$$

The output voltage of the N-path configuration is given by

$$v_0(t) = \sum_{n\text{-}1}^{N} v_n(t)\, q_n(t)$$

$$V_0(j\omega) = \sum_{n\text{-}1}^{N} \sum_{\beta=-\infty}^{\beta=\infty} Q_\beta \exp\left(-j\beta\omega_0(n\text{-}1)\,\frac{T}{N}\right) Vn_2(j\omega\text{-}j\beta\omega_0) \qquad \text{eqn. 5.27}$$

Substituting equation 5.25 into equation 5.27

$$V_0(j\omega) = \frac{1}{P_0} \sum_{n\text{-}1}^{N} \sum_{\alpha,\beta} Q_\beta P_\alpha \exp\left(-j\omega_0(\alpha+\beta)\,T/N\right) G(j\omega\text{-}j\beta\omega_0)\, Vi[j\omega\text{-}j\omega_0(\alpha+\beta)] \qquad \text{eqn. 5.28}$$

and summing over n as was done in equation 5.9

$$V_2(j\omega) = \frac{N}{P_0} \sum_{\beta} Q_\beta G(j\omega\text{-}j\beta\omega_0) \sum_{k} P_{k\text{-}\beta}\, Vi\,(j\omega\text{-}jkN\omega_0) \qquad \text{eqn. 5.29}$$

Now, if $Vi(j\omega)$ is bandlimited so that

$$Vi(j\omega) = 0 \text{ for } \omega \leqslant N\frac{\omega_0}{2} \qquad \text{eqn. 5.30}$$

and if the output is followed by a coarse bandpass filter that selects the passbands corresponding to $\beta = \pm 1$. Then

$$\frac{V_0}{Vi}(j\omega) = \frac{N}{P_0}\left[Q_1 P_{-1} G(j\omega - j\omega_0) + Q_{-1} P_1 G(j\omega - j\omega_0)\right] \qquad \text{eqn. 5.31}$$

where $P_0 = Q_0 = \frac{1}{N}$

Using equation 5.14, we have

$$\frac{V_0}{Vi}(j\omega) = \left(\frac{\sin \pi/N}{\pi/N}\right)^2 \left[G(j\omega - j\omega_0) + G(j\omega + j\omega_0)\right] \qquad \text{eqn. 5.32}$$

This expression is the general transfer function of the N-path filter and is equivalent to equation 5.15. The lowpass function $G(j\omega)$ is simply related to the lowpass characteristic of one of the path networks. Inspection of equation 5.26 shows that $G(j\omega)$ is simply the voltage transfer function of one of the component networks operating between a source resistance R_1 and a load R_2. For example, substituting equation 5.20 into equation 5.26, we have

$$G(j\omega) = \frac{\frac{NR_2}{j\omega C}}{\left(NR_1 + \frac{1}{j\omega C}\right)\left(NR_2 - \frac{1}{j\omega C}\right) - \frac{1}{\omega^2 C^2}}$$

when $R_2 \gg \left|\frac{1}{j\omega C}\right|$ then $\qquad G(j\omega) \approx \frac{1}{1 + j\omega N R_1 C} \qquad$ eqn. 5.34

Therefore

$$G(j\omega \pm j\omega_0) \approx \frac{1}{1 + (j\omega \pm j\omega_0) NR_1 C} \qquad \text{eqn. 5.35}$$

Substituting this result into equation 5.32, we have

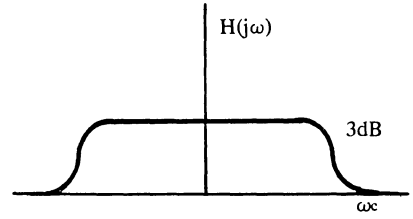
$$\frac{V_0}{Vi}(s) = \left(\frac{\sin \pi/N}{\pi/N}\right)^2 \left[\frac{1}{NR_1 C (s - j\omega_0) + 1} + \frac{1}{NR_1 C (s + j\omega_0) + 1}\right]$$

eqn. 5.36

The above expression is the transfer function of a low pass filter which has been translated in frequency. Thus, the commutated N-path network translates the lowpass characteristic of Fig. 5.9 and to the bandpass characteristic of Fig. 5.10 which has arithmetic symmetry about ω_0.

This characteristic is identical to the second-order bandpass response of a passive RLC or active RC filter.

Fig. 5.10 **Lowpass characteristic**



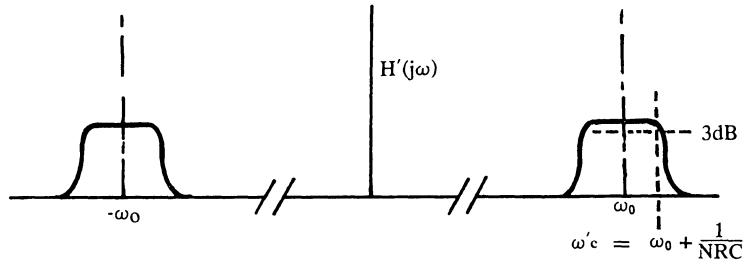
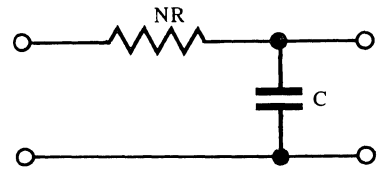


Fig. 5.11 **Bandpass characteristic formed by the frequency translated lowpass network of Fig. 5.12**

Fig. 5.12
Equivalent lowpass filter which determines bandwidth of bandpass response.



It is also evident that the bandwidth of the bandpass response is determined by the equivalent RC lowpass section of Fig. 5.11. From equation 5.36, we see that the 3dB bandwidth is

$$BW_{3dB} = \frac{2}{NR_1C} \qquad \text{eqn. 5.37}$$

Therefore

$$\boxed{Q = \frac{\omega_0 NRC}{2}} \qquad \text{eqn. 5.38}$$

Since the bandwidth of the output response is determined by passive components, the N-path filter is relatively free from the sensitivity problems associated with active RC realisations of high Q resonators. Furthermore, since the centre frequency is independent of R and C the stability of ω_0 is dependent on maintaining a constant clock period.

Another important parameter which is also determined by the lowpass path network is the phase response of the N-path system. From equation 5.35, the phase angle as a function of frequency is given by

$$\phi(\omega) = \tan^{-1}[NR_1C(\omega-\omega_0)] \qquad \text{eqn. 5.39}$$

from which the group delay τ_G, can easily be obtained

$$\tau_G = \frac{d\phi(\omega)}{d\omega} = \frac{NR_1C}{1 + [NR_1C\,(\omega-\omega_0)^2]} \qquad \text{eqn. 5.40}$$

Evaluating the group delay at the 3dB points, we have

$$\tau_{G3dB} = \frac{NR_1C}{2} = \frac{1}{3dB\ \text{bandwidth}} \qquad \text{eqn. 5.41}$$

It will be seen that these results are similar to a single RLC network. If, however, the path elements consist of several RC stages or a distributed network, the group delay can vary considerably from an RLC filter of the same bandwidth.

5.5 SHUNT-SWITCHED BANDPASS FILTER

The circuit arrangement shown in Fig. 5.1 is known as the series switched N-path filter. This arrangement has the advantage that multipole filters can be employed in each path. The resulting N-path filter can be designed, therefore, to have a very good skirt selectivity. If, however, the skirt selectivity performance is not critical the simpler shunt switch N-path filter shown in Fig. 5.13, can be used. This configuration halves the number of switches and enables one side of the switches to be connected to a common ground point.

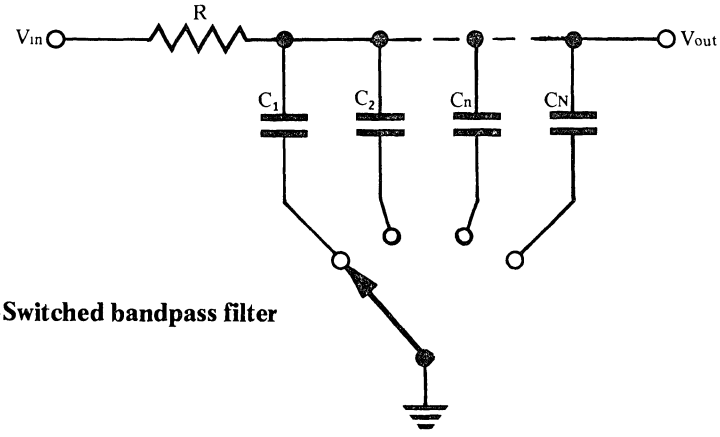
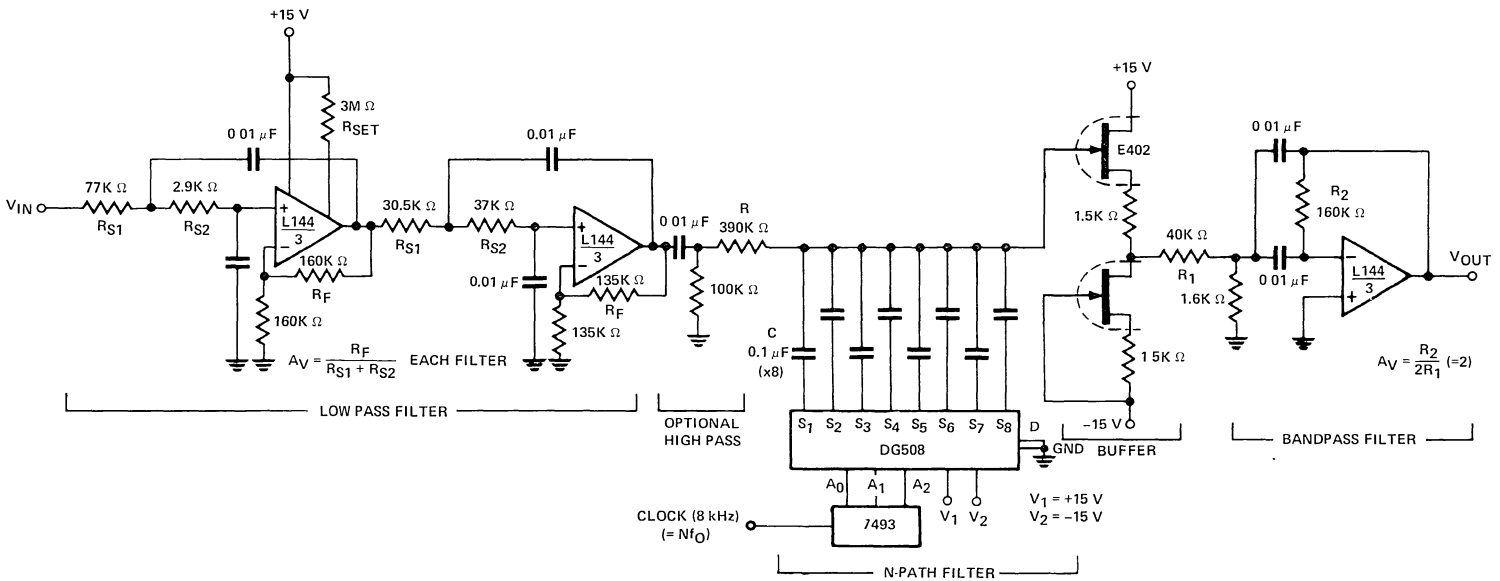


Fig. 5.13 **Shunt-Switched bandpass filter**

5.6 APPLICATIONS

5.6.1 Shunt-Switched Bandpass Filter

The main application of the N-path filter is the high Q bandpass filter which, in the simplest case is the shunt-switched filter. This configuration allows the use of multiplexers such as the DG508, a CMOS 8-channel device which has 8 separate connections and a common drain. This feature considerably simplifies the practical realisation of high selectivity N-path filters.



$Q = \pi F_O \times N \times R \times C$ (= 1000)

$f_O = \frac{\text{CLOCK}}{N}$ $(= \frac{8\text{ kHz}}{8} = 1\text{ kHz})$

Fig. 5.14
Shunt Switched Bandpass Filter

PERFORMANCE DATA:

Q = 1000
f_O = 1 kHz
N = 8
VOLTAGE GAIN ≈ 7

Fig. 5.15

Fig. 5.14 shows a practical circuit for a 1kHz bandpass filter with a Q of 1000. The input filter is a 4 pole, 2dB ripple Chebyshev network with a cut-off frequency of approximately 1·22kHz and a voltage gain of 4. This filter serves the dual purpose of bandlimiting the input signal $(\frac{N\omega_0}{2})$ to prevent 'aliasing' and providing amplification.

The N-path filter employs a DG508 CMOS multiplexer which combines the necessary analogue switches, interface circuitry and decode logic on a single chip. The DG508 can handle ± 15V analogue signals from ± 15V supplies and is fully CMOS, TTL, RTL and DTL compatible. A 7493 type TTL counter generates the 3-bit binary sequence from the clock.

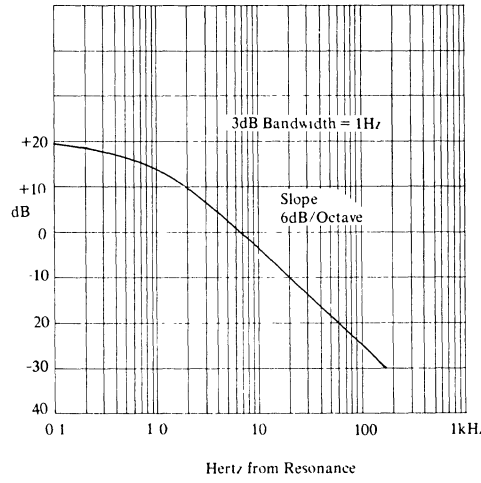


Fig. 5.16
Output Response of Shunt-Switched Bandpass Filter.

The output of the N-path filter is buffered by a source follower consisting of an E402 dual FET. This circuitry features unity gain, low offset that can be trimmed to zero, and high input impedance. The output of the source follower is fed into a low Q (approximately 3) 1kHz bandpass filter with a voltage gain of 2.

A simple RC highpass network preceding the N-path filter eliminates the passband centred at d.c.

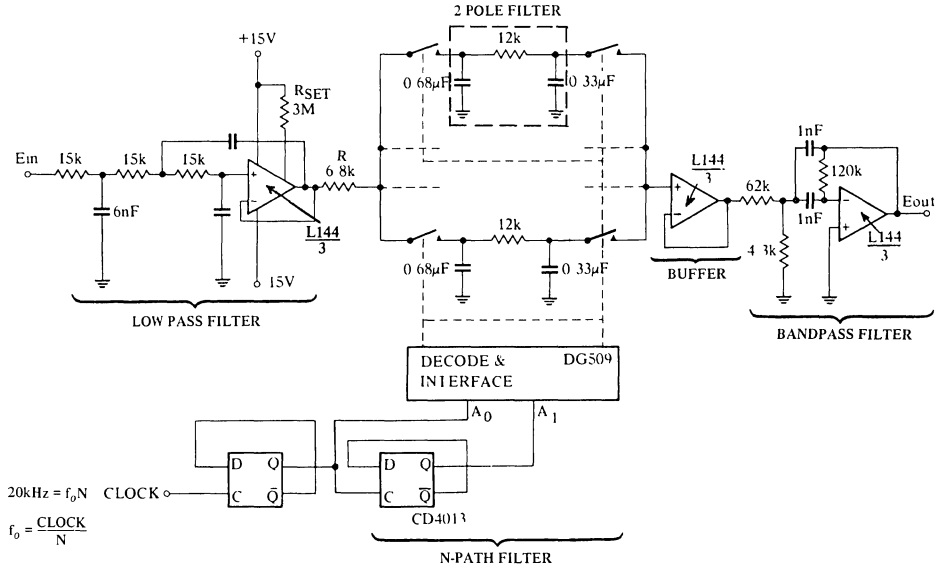
Figs. 5.15 and 5.16 show the output response of complete bandpass filter. It will be noted that the output is symmetrical about f_0 and has an asymptotic slope of 6dB/octave. The measured 3dB bandwidth was 1Hz yielding a Q of 1000.

The system described is capable of realising Q's up to at least 10^4. The DG508 can be used at centre frequencies up to 50kHz, although faster amplifiers will be necessary at these frequencies.

5.6.2 Series-Switched Bandpass Filter

An alternative method of achieving a bandpass response is to switch lowpass path elements with a series switch arrangement. If the path elements are single pole RC sections, then the series-switch filter would have the same frequency response as the shunt-switched filter shown in the preceding section. However, the series-switched filter allows multipole passive or active filters to be incorporated in each path which improves skirt selectivity.

Fig. 5.17
Series-Switched Bandpass Filter.



Performance Data
$f_0 = 5kHz$
$Q = 500$
Voltage Gain ≈ 2
$N = 4$

Fig. 5.17 shows a practical 4 path series-switched bandpass filter with a centre frequency of 5kHz. The path element is a two pole RC filter with a 3dB bandwidth of approximately 20Hz. The input filter is a 3 pole Chebyshev filter with a cut-off frequency of approximately 5·5kHz.

The N-path filter employs a DG509, 4-channel CMOS differential multiplexer which has the necessary pairs of analogue switches, interface circuitry and decode logic all on one chip. The DG509 has a ± 15V signal handling capability and is directly TTL,CMOS compatible. A dual D-type flip-flop (CD4013) generates the necessary 2-bit binary sequence from the 20kHz clock signal.

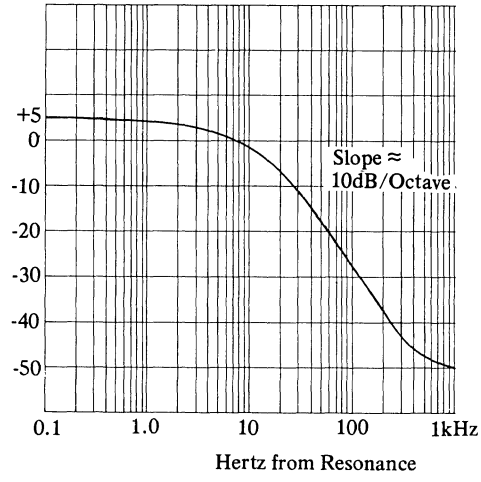


Fig. 5.18
Output Response of Series-Switch

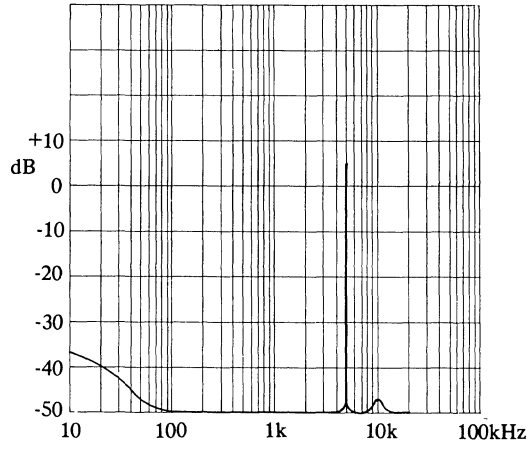


Fig. 5.19
Output Response of Series-Switched Filter

The output of the N-path filter is buffered by an L144 voltage follower and then post filtered by a 5kHz, low Q, bandpass filter. Figs. 5.18 and 5.19 show the output response of the complete bandpass filter. Comparing Fig. 5.18 with the corresponding response for a shunt-switched filter shown in Fig. 5.15 it will be seen that the roll-off of the former response is increased to 10dB/octave. Theoretically, this roll-off should be 12dB/octave but the capacitors acquire a residual charge when they are switched into circuit which tends to broaden the actual frequency response.

The spectrum of the filter output shows a response centred at d.c. which could be removed, if necessary, with a simple RC highpass filter, also a second harmonic response which is —52dB with respect to the fundamental. A lowpass filter with steeper roll-off characteristic could improve the out-of-band attenuation.

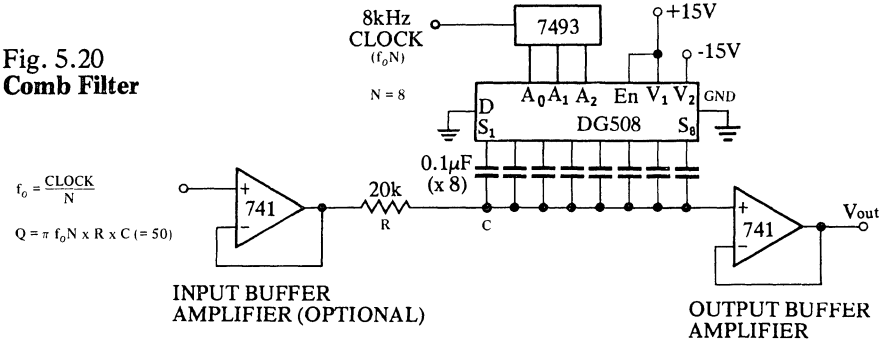
The measured 3dB bandwidth was 10Hz at 5kHz yielding a Q of 500. The overall voltage gain of the filter was approximately 2.

5.6.3 Comb Filter

One of the useful applications of the periodic response properties of the N-path filter is in selective filtering of periodic signals from a background of non periodic noise interference. If the path networks are lowpass filters with bandwidth small compared to $^1/_2T$, then the N-path filter response is a sequence of equally spaced passbands forming a comb which introduces little distortion to signals of period T, but substantially reduces the power of the interfering noise.

In the simplest case, the lowpass element in each path can be a single RC network which enables one side of the switches to be connected to ground. This allows the use of analogue multiplexers with a common drain terminal which considerably simplifies the practical implementation of comb filters.

Fig. 5.20
Comb Filter



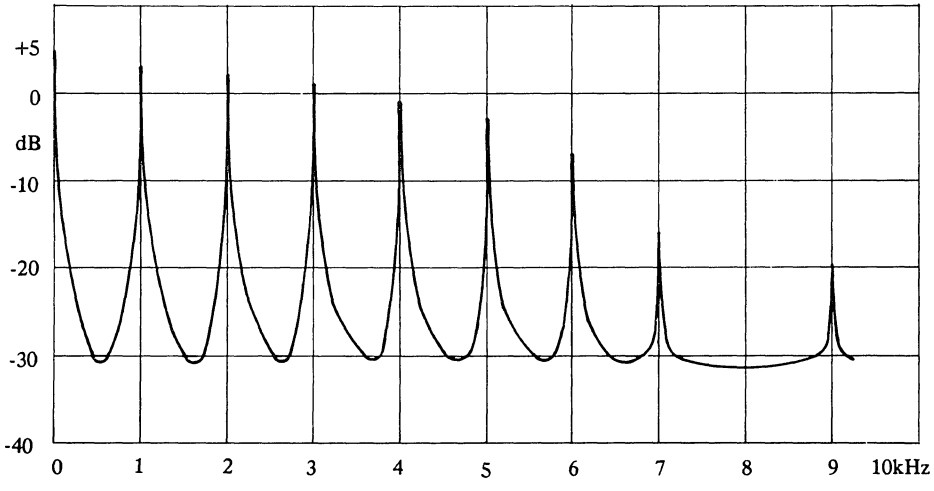


Fig. 5.21 **Comb Filter Response**

The circuit of Fig. 5.20, shows a DG508, an 8-channel CMOS multiplexer, used in a comb filter whose fundamental frequency is 1kHz. The frequency response of this filter is shown in Fig. 5.21. Because of the sampling action, a response is obtained at f_0 and at multiples of f_0. However, no response will be obtained at Nf_0, $2Nf_0$ etc. The relative amplitudes of the harmonic peaks as a function of harmonic number is given by:

$$A(n) = \left(\frac{\sin \frac{n\pi}{N}}{\frac{n\pi}{N}} \right)^2 \qquad \text{eqn. 5.41}$$

where A(n) = amplitude of response
n = harmonic of clock frequency
N = number of filter paths

The DG508 will accept analogue signals of up to ±15V with ±15V supplies. However, the signal handling capability of the filter is limited by the output voltage swing of the 741 buffer amplifiers.

A TTL binary counter (7493) provides the necessary 3-bit binary count sequence from the 8kHz clock. The DG508 may be used at frequencies up to 100kHz.

For applications requiring a higher number of passbands, the 16-channel DG506 may be used instead of the DG508. Where a lower signal handling capability (±5V) can be tolerated, the low cost DG501 (8 channels) can be used to advantage.

5.6.4 High-Q Notch Filter

By adding a summing amplifier to an N-path filter, it is possible to build a notch filter whose centre frequency is insensitive to component variations. The system Q, which can be extremely high, is adjusted with a single resistor and its variation does not affect the notch frequency.

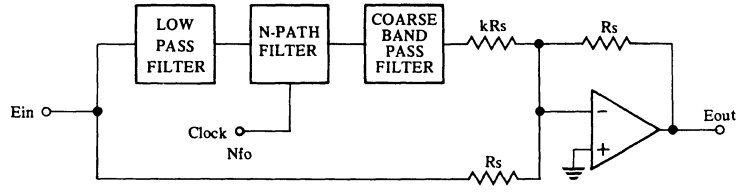


Fig. 5.22 **Notch filter block diagram**

The block diagram of the notch filter is shown in Fig. 5.22. The N-path filter together with its attendant low and bandpass filters provide a bandpass output. The lowpass filter is designed to introduce a 180° phase shift at frequency f_0. The amplifier sums the original signal and the phase shifted bandpass output from the N-path filter. The bandpass signal component at f_0 cancels those present in the original signal to produce the desired notch characteristic.

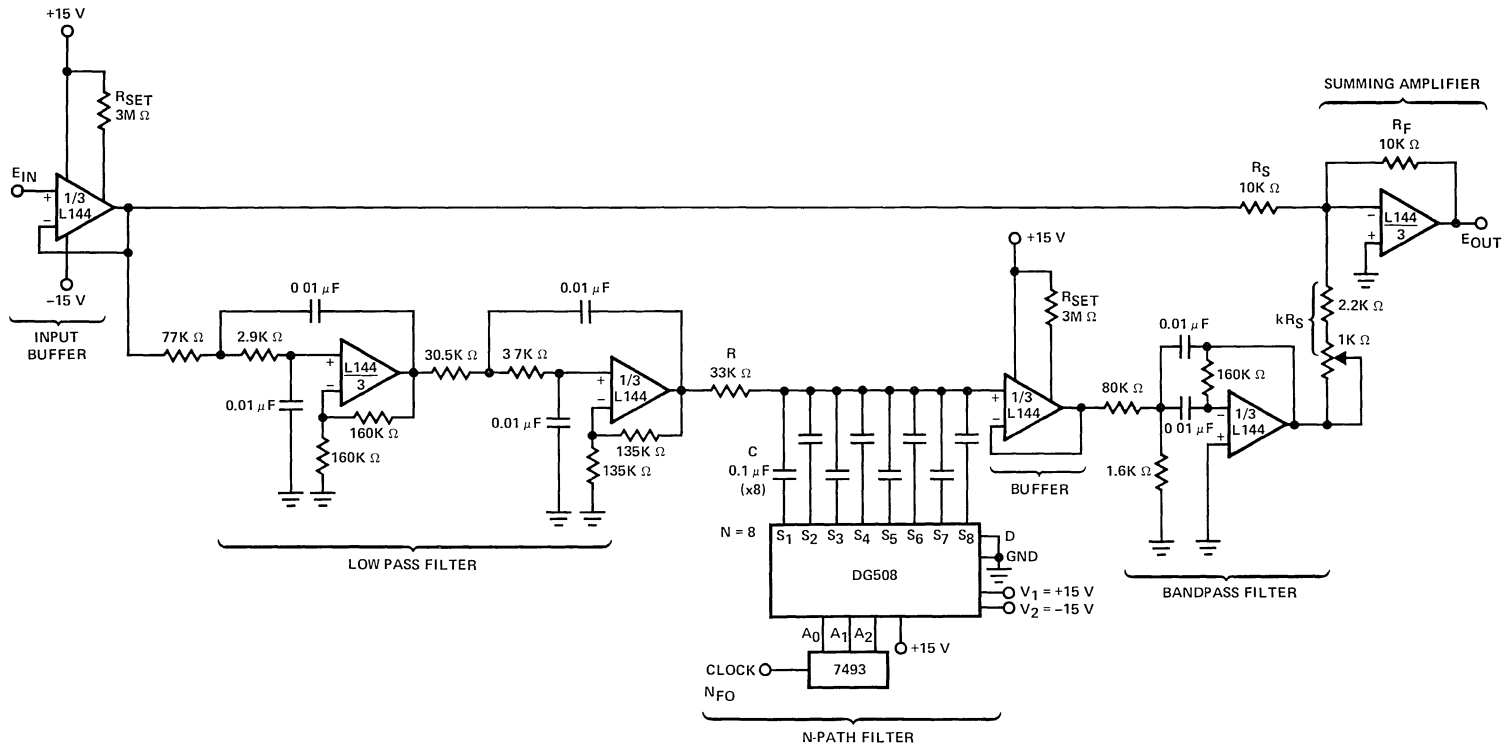


Fig. 5.23 Notch Filter

$$Q = \pi F_O \times N \times R \times C$$

$$k = \frac{1}{\text{VOLTAGE GAIN IN FILTER PATH}}$$

Fig. 5.23 shows the practical realisation of a 1kHz notch filter. The lowpass network is a 4 pole, 2dB ripple Chebyshev filter which is designed to have a cut-off frequency of approximately 1·220kHz. This value of cut-off frequency ensures that the filter will introduce 180° phase lag at 1kHz. Since the N-path filter and the second order bandpass filter exhibit zero phase shift at their centre frequencies then the overall phase shift will be —180°.

The lowpass filter has an overall voltage gain of approximately 4 at 1kHz. From equation 5.41, the gain of the N-path filter is found to be 0·95. The post bandpass filter has unity voltage gain. Therefore, at 1kHz the overall N-path transfer function is: 4 x 0·95 = 3·8.

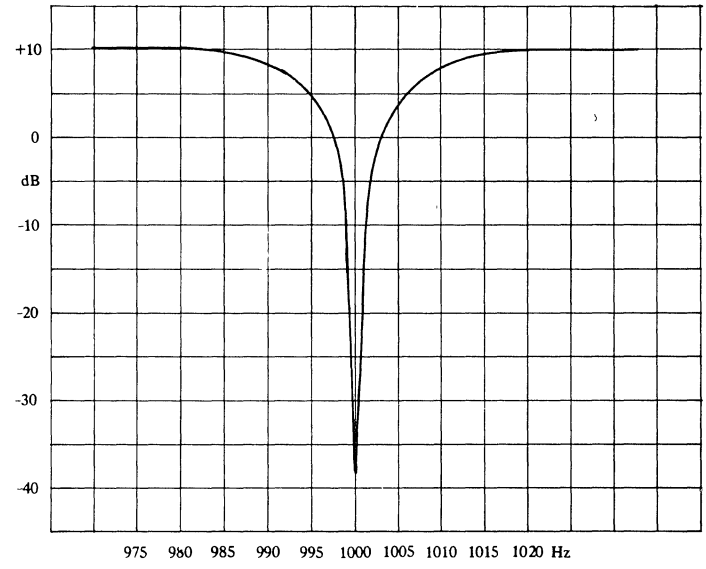


Fig. 5.24
Notch Filter Response

The summing resistor Rs is chosen to cancel E_{in} at 1kHz. On a normalised basis $K = \frac{1}{3 \cdot 8} = 0 \cdot 263$. Selecting a 10kohms feedback resistor for the amplifier, the two summing resistors are 10kohms and 2·63kohms. Therefore the nearest preferred value of 2·2kohms is selected and a 1kohm potentiometer is included to provide for fine adjustment.

The summing amplifier is chosen to pass the highest frequency components of E_{in}. For frequencies below 10kHz, the L144 will suffice. However, the DG508 is suitable for centre frequencies up to 50kHz.

Fig. 5.24 shows the notch response. The 3dB bandwidth is approximately 0·75Hz, which yields a Q of 1330.

5.7 SUMMARY

This chapter has shown that N-path filters provide a valuable alternative approach to both classical and active filter design. In particular, comb filters and very high Q bandpass filters can be realised without the stability and sensitivity problems associated with conventional analogue filters.

5.8 *REFERENCES*

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5.2 K. Davies 'Active Biquadratic Filter Design using L144 Low Power Triple Op Amp'. Siliconix App. Note AN74-6.

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5.4 L. E. Franks, I. W. Sandberg 'An Alternative Approach to the Realisation of Network Transfer Functions', The N-path Filter Bell System Technical Journal, Vol. 39, Sept. 1960.

5.5 E. M. Bliss, 'Watch out for hidden pitfalls in Signal Sampling', Electronic Engineering, March 1973.

Chapter 6

Signal Conversion using Analogue Switches

6.1 INTRODUCTION

Digital techniques are becoming more widespread in electronic equipment, ranging from digital wristwatches and pocket calculators to pulse coded modulation communications systems and large computers. The advantages of digital techniques are high speed, and noise immunity. Rapid developments in integrated circuit processing have made available large quantities of digital logic and computing power in small economic units. State-of-the-art in this field is a complete micro-processor or micro-computer in one small package.

The natural world presents characteristics such as pressure, temperature, and voltage in analogue form; thus, where the natural world has to interface with digital equipment, translative interfaces are required. For instance, in a process control system, analogue information from sensors has to be converted into digital form for manipulation by a computer based controller. The controller's digital instructions are then translated to analogue form to actuate devices controlling the environment being monitored.

These translative interfaces are called digital-to-analogue (D-A) and analogue-to digital (A-D) converters. Increased use of digital techniques to replace analogue systems has resulted in the evolution of a multiplicity of D-A and A-D converter types. Despite the numbers and varieties of standard units available, there are still occasions where non-standard digital codes or analogue voltages are required. This often happens in the aircraft and telecommunications industries. In circumstances such as these, the designer has two options: he can either design his own converter, or modify a commercially available unit. Both these courses can be taken by using integrated driver gates for switching.

This chapter introduces the basic switching techniques used in D-A and A-D converters. Considerable reference is given to switching techniques in chopper amplifiers which can form an essential part of the overall A-D converter system.

6.2 D-to-A CONVERTERS

6.2.1 Weighted Network Converter

The majority of D-to-A converters available today are based on the weighted network principle.

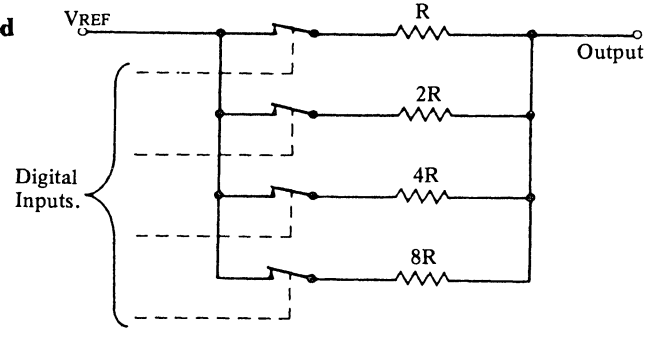


Fig. 6.1 **Binary weighted resistor D-A converter**

An example of this in binary form is shown in Fig. 6.1. Weighted currents are summed at the output node of the network. The currents are produced from a voltage reference source via an analogue switch and a resistor. The value of the resistor depends on the "weighting" of the digit driving it. In the above example, the current produced when the most significant bit is energised is $\frac{V_{REF}}{R}$.

The second most significant bit operation produces a current $\frac{V_{REF}}{2R}$.

and the third most significant bit operation produces a current $\frac{V_{REF}}{4R}$.

It can be seen that the currents are binary weighted. If the resistor values were in decade ratios the currents would also be in decade ratios. The main drawback of this system is the large values of resistances that may be necessary. For instance, for a 10 bit binary weighted network with R = 1 kohm, the 10th bit has a value 1k x 2^{10} = 1·024 Mohms. To maintain the accuracy of the conversion over a temperature range, the resistor ratios must track. This is extremely difficult over resistor ratios of 1000 to 1. Also the impedance of the network varies with the input code and this can upset the offset and drift of any following amplifier, and hence system accuracy.

6.2.2 Ladder Network Converter

A resistor system that achieves the same "weighting" performance without the large range of values described is the ladder network (Fig. 6.2).

Fig. 6.2 **Ladder network D-A converter**

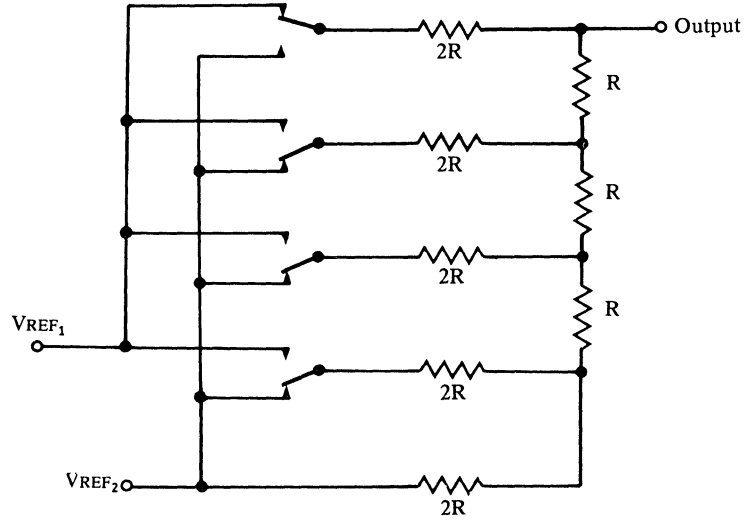
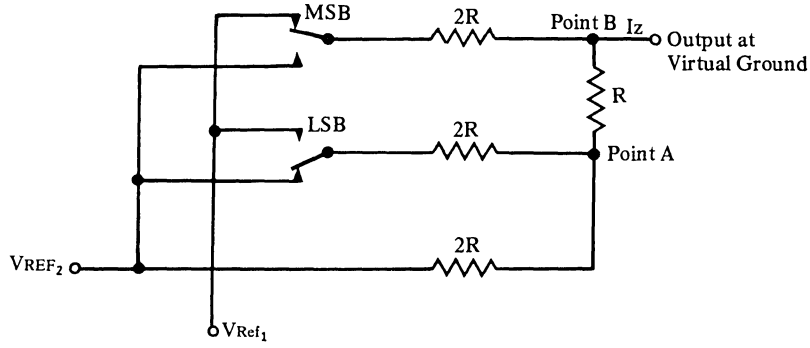


Fig. 6.2 shows a binary weighted ladder network with switches. The resistor values have only 2:1 ratios but it is now necessary to use two switches per bit instead of one. The operation of the ladder network can be understood by considering a simple two-bit converter with V_{REF_2} equal to zero volts (Fig. 6.3).

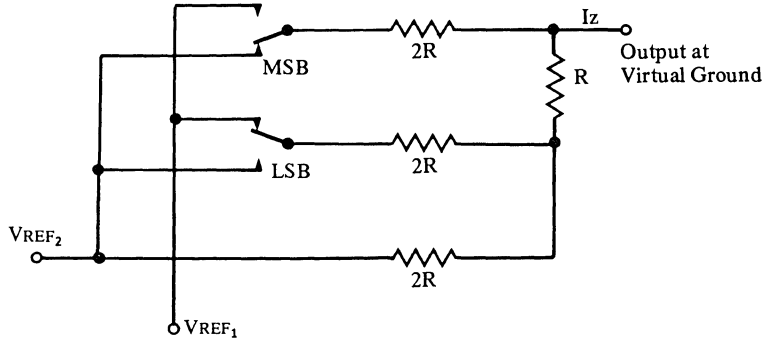
Fig. 6.3 **Operation of 2 bit converter based on ladder network principle.**



Case 1

Consider Fig. 6.4, with the most significant bit (M.S.B.) equal to logic '1' (V_{REF_1}) and the least significant bit (L.S.B.) equal to logic '0' (V_{REF_2} = 0 volts). The output current Iz will be : $\frac{V_{REF_1}}{2R}$

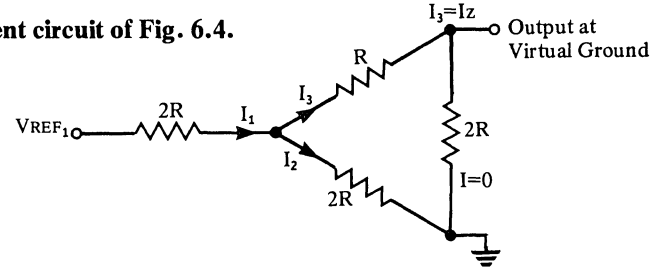
Fig. 6.4 **D-A converter with MSB operating.**



Case 2

Consider Fig. 6.4, with MSB = logic '0' and LSB = logic '1' (V_{REF_1}), the output current Iz can be calculated using Kirchoff's equations for the equivalent circuit shown in Fig. 6.5.

Fig. 6.5 **Equivalent circuit of Fig. 6.4.**



$$I_1 = I_2 + I_3 \qquad 2RI_2 = RI_3 \qquad I_2 = \frac{I_3}{2} \qquad I_1 = \frac{3I_3}{2}$$

$$2RI_1 + 2RI_2 = V_{REF}, \quad R3I_3 + RI_3 = V_{REF}, \text{ hence } Iz = I_3 = \frac{V_{REF}}{4R} = {}^1/_2 \text{ MSB}.$$

Thus I_2 is now half the value observed in Case 1. This approach can be repeated for any number of bits.

Since the ratio of resistor values need only be 2:1, good temperature tracking can be achieved relatively easily. Furthermore, the ladder network has the advantage of constant output resistance. With reference to Figure 6.2, the resistance at point A, looking back into the two 2R resistors in parallel, is R. From point B, this impedance is in series with R, giving total 2R. Progressing towards the output node, this 2R in parallel with another 2R, gives R again. Repeating this for any number of bits will show that the impedance of the network at the output is a constant value, R, independent of the input code. This permits the addition of precision gain amplifiers to the converter to produce voltage outputs. The amplifier feedback resistor can be part of the resistor network to produce precise thermal tracking.

Present state of the art in D-toA converters includes complete units on one silicon chip. The more precise converters have thin film resistor networks on the surface of the chips. The low power types comprise monolithic complementary MOS circuits.

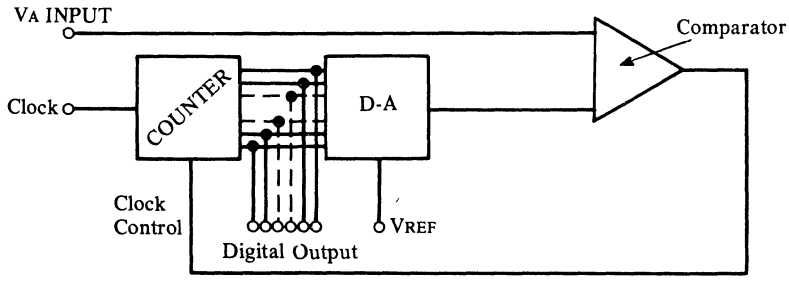
6.3 A-to-D CONVERTERS

Since A-to-D converters are more widely used than D-to-A converters there is a wider variety of designs commercially available. Different system requirements dictate the use of different A-to-D conversion techniques.

6.3.1 Parallel A-to-D Converter

The medium to high speed A-to-D system is generally based on a D-to-A converter with logic and a comparator as shown in Fig. 6.6.

Fig. 6.6 **Successive approximation A-D converter**



When the analogue input, V_A equals the output of the D-to-A converter, the comparator stops the clock, the read-out of the digital input to the D-to-A at this time being the digitised value of the V_A input.

The control logic can be a simple up-counter which has to count through full

scale for every negative increment of analogue input and is, therefore, slow to convert decreasing signals. Alternatively, an up-down counter which can track the change in direction of the input could be used. This type of converter can be fast, with clock rates above 1MHz but becomes relatively expensive for accuracies better than 0·1%.

There are many other types of converter systems *(Refs. 6.1 and 6.2)* all of which utilize analogue switches.

6.3.2 Recirculating A-D Converter

Fig. 6.7 **Recirculating A-D converter.**

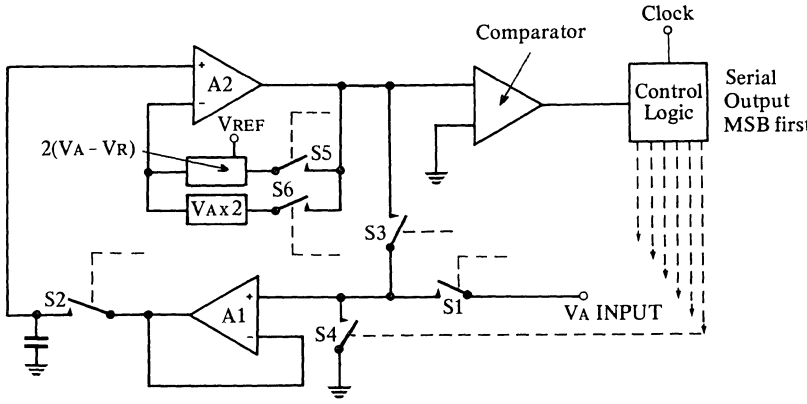


Fig. 6.7 is but one example of a binary A-to-D converter based upon operational amplifiers and FET analogue switches.

The principle of operation is relatively simple:

Step 1. The input V_A is sampled when switches S_1 and S_2 are closed and S_3 and S_4 are open.

Step 2. The sample is applied to the amplifier A2 which is in its reference mode.

a) If V_A is greater than V_{REF}, the control logic output is a logic '1' and the amplifier will subtract V_{REF} from V_A and multiply the result by 2. This result is then recirculated via switches S_3 and S_2 and treated as a new input.

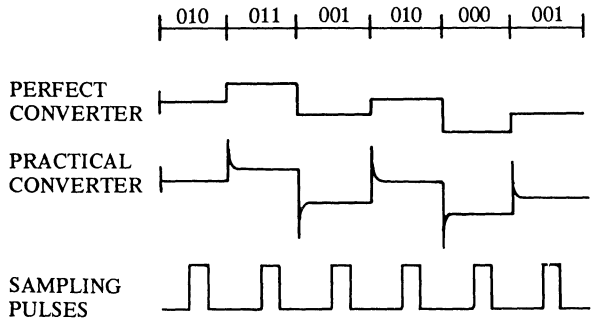
b) If the input is less than V_{REF}, the logic is a '0' and the amplifier will be switched to multply the V_A signal by 2 and this output signal is then recirculated as a new input. This would be repeated over a number of cycles up to the resolution capability of the unit, at which time S_1 will open to input a new sample.

The resolution of the converter may be improved by generating more cycles between signal sampling intervals. Switching spikes, which are created when the analogue switches in the system are closed, can cause inaccuracies. The overall accuracy is critically dependent on the precision of the analogue amplifiers, and the present limit on accuracy is about 0·1% and 10 bits on resolution. The previously mentioned A-D converter of Fig. 6.6 where the analogue signal manipulation consists only of comparator monitoring, is available in 16-bit form and 0·005% accuracy. The design of Fig. 6.7 is suitable if small size and medium

accuracy are the requirements. The output will be in serial form but can, by the addition of a serial-to-parallel converter, be in parallel form. This design has in fact been fabricated in monolithic PMOS form. To compensate for MOS amplifier drift, the converter has an auto zero mode which is introduced prior to each input sample. In this mode, the input is grounded via S_4 (Fig. 6.7) and the output added to the analogue amplifier reference for the next series of conversion cycles.

6.4 DEGLITCHING

Fig. 6.8 **Sample-and-Hold waveforms.**



When the input digital code changes in a D-A converter some switches turn ON and others turn OFF. The number of switches operated depends on the exact code change. However, since all types of switches have different turn-on to turn-off responses, there will be rapid changes through many varying codes during the short transitional period. This results in transient spikes or "glitches", Fig. 6.8. The magnitude of the glitch that can be tolerated depends on the overall system accuracy required. A low pass filter would reduce the glitches, but for high accuracy, a sample-and-hold circuit is often placed after the converter output.

The sample-and-hold switch is controlled by a pulse lying within the digit period, such that the sample is taken between transients, when the output is stable. Sample and hold circuits employing integrated switches and operational amplifiers have been described in Chapter 4.

In circumstances where the input signal to an A-D converter may be changing by a value which is more than the least significant bit, during a complete conversion cycle, it is possible to use a sample-and-hold before the converter to provide a stable input.

6.5 CODING

An alternative method to using low pass filters and sample-and-hold systems is to use Grey Code digital inputs. Table 6.1 shows the Grey-to-Decimal code conversion. Grey Coding introduces only a one digit change between consecutive numerals. However, this means that only one switch transition will occur for any increment or decrement in output. For large changes this has similar problems to binary and BCD codes.

Table 6.1 **Code Conversion**

Binary	Grey	Decimal
0000	0000	0
0001	0001	1
0010	0011	2
0011	0010	3
0100	0110	4
0101	0111	5
0110	0101	6
0111	0100	7
1000	1100	8
1001	1101	9

6.6 RANGING (See also 6.15.3)

The trend towards simplifying the operation of modern measuring instruments has led to the adoption of automatic polarity and ranging techniques.

Auto-ranging in both D-A and A-D converters can be accomplished using analogue switches, controlled by digital signals, to switch the ranging resistors. Figs. 6.9 and 6.10 show two methods of doing this.

Fig. 6.9 **Inverting auto-ranging system.**

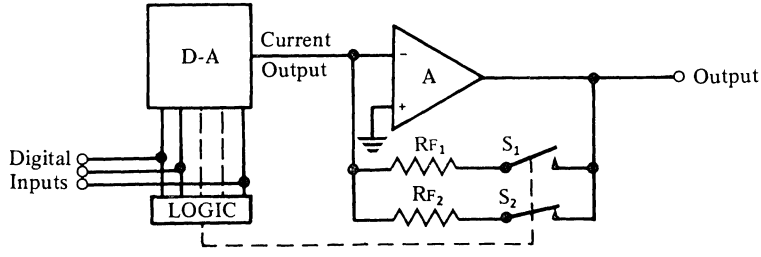
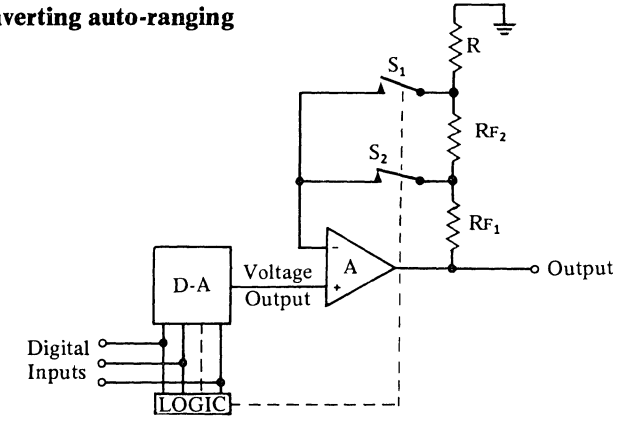


Fig. 6.10 **Non-inverting auto-ranging system**



In Fig. 6.9, the selection of feedback resistors R_1 or R_2 can be controlled by the digital inputs. The disadvantage of this system is that the variation in switch resistance affects the amplifier gain.

Fig. 6.10 is an improved gain switching system where a non-inverting amplifier configuration is acceptable. Here, the switch resistance does not affect the gain because it is in series with the amplifier input impedance.

6.7 MULTIPLYING CONVERSION

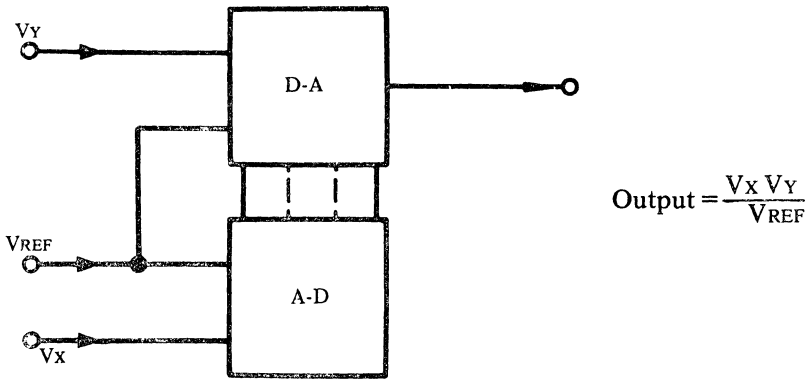
The D-A converter based upon the ladder network can be considered to be an attenuator. The output is a fraction of the reference voltage, and is determined by the digital input. If the reference, instead of being static, was a varying analogue signal, the output would be an attenuated version of this signal. The majority of D-A converters are very limited in the range of reference voltages that can be used (normally ±5 volts). However, the converter shown in Fig. 6.2 references up to ±15 volts at frequencies up to and in excess of 1MHz, if the DG200 series of CMOS analogue switches is used.

The concept can be developed further to produce a high accuracy, low conversion-time analogue multiplier. Fig. 6.11 is a schematic of this. A high performance A-D converter takes the V_X analogue input and converts it to digital form as V_X/V_{REF}. This then enters the digital inputs of the D-A converter with V_Y as its reference. The output of this is $\frac{V_X V_Y}{V_{REF}}$.

There is a variety of monolithic analogue multipliers in existence, but most are restricted to ±10 volts signal range and overall accuracies of 0·5%. This system can give an order of magnitude improvement in accuracy, and accepts signals of ±15 volts. An extension to the use of the circuit in Fig. 6.11 is to inter-change V_X and V_{REF} in which case the system becomes a precision analogue divider.

$$\text{i.e. Output} = \frac{V_Y V_{REF}}{V_X}$$

Fig. 6.11 **Analogue multiplier using D-A and A-D converters.**

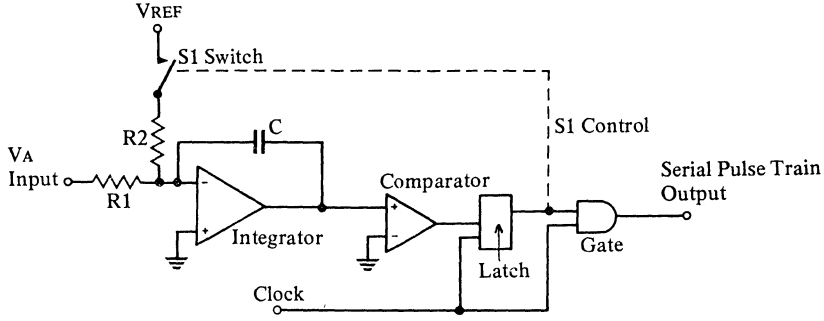


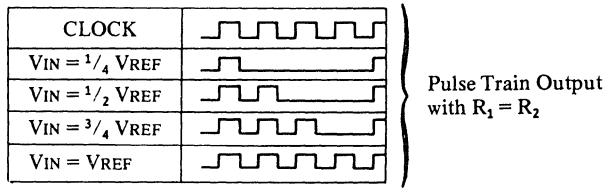
Considering Fig. 6.15, it is possible by reversing the relative positions of the resistor network and switches, with reference to point A, to accommodate reference voltages in excess of ±15 volts. However, in this configuration switching spikes would have more effect on the output than they do in the circuit of Fig. 6.15 and so the transposition of resistor network and switches is not recommended for high accuracy conversion.

6.8 DELTA-SIGMA MODULATION

Another system for A-D and D-A conversion that has merits in remote sensing applications and which finds a ready use for integrated analogue switches, this is called Delta-Sigma modulation and demodulation *(Ref. 6.3)*. The analogue input is applied to an integrator (Fig. 6.12) which is also supplied with a switched reference VREF. Switch S_1 is controlled by the latch. The output of the integrator is applied to a comparator which produces digital output pulses in phase with the clock, in a serial pattern dependent on the ratio of the analogue input to the reference.

Fig. 6.12 **Delta-Sigma modulator**





The overall resolution of the converter is determined by the values of R and C, the comparator resolution and the clock frequency. This system will give high performance with a minimum of components. The D-A section of the system is a synchronous demodulator. The reference voltage is switched into the integrator by the incoming pulse train in synchronism with the clock. Fig. 6.13 shows the decoder and Fig. 6.14 the analogue output for a particular pulse train input.

Fig. 6.13 **Delta-Sigma demodulator**

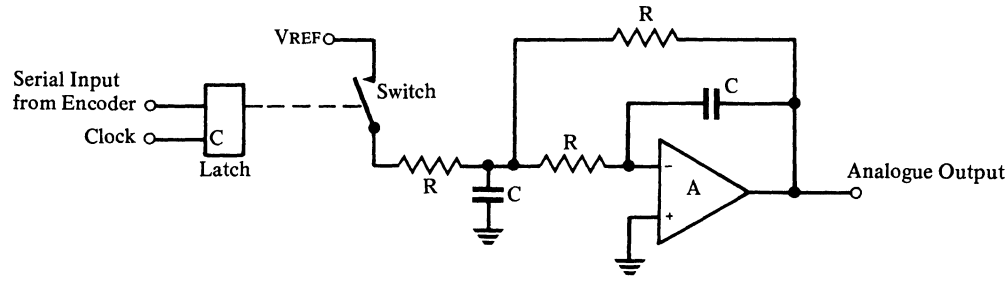
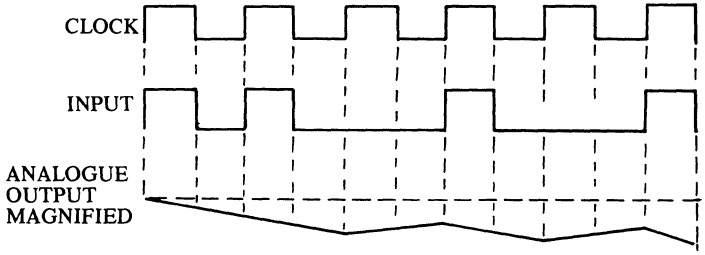


Fig. 6.14 **Delta-Sigma system waveforms**



The non-linearity of the analogue output is a function of integration time constant and clock rate. It can be made insignificant within the overall system accuracy by proper consideration of these two factors.

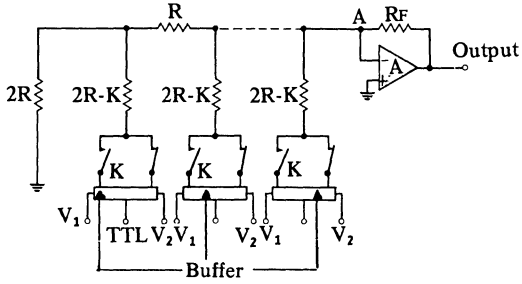
The selection of an analogue switch for this application is relatively easy when one considers:

1) The analogue signal seen by the switch is constant (VREF); therefore, even switches that suffer ON resistance modulation can be used (section 6.8).
2) The ON resistance of the switch can be accounted for in the value of the resistor in series with it, so that ON resistance is not critical.
3) The turn-on and turn-off times of the device should be at least an order of magnitude less than the period of the clock to maintain overall accuracy. This is because the finite switching time of the analogue switch can be considered to cause an analogue offset, by charge transfer. Its effect on linearity will depend on the value of signal.

6.9 SWITCH PARAMETERS

A study of the use of FET analogue switches in a typical D-A converter will serve to illustrate the relevant switch parameters of importance.

Fig. 6.15 **D-A converter using integrated analogue switches.**



Consider Fig. 6.15. There are three main factors that affect the performance of the converters:

1) Stability and accuracy of reference voltages V_1 and V_2.
2) Accuracy of resistor network ratios, including switch resistance.
3) Temperature tracking of R_F and R.

The generation of stable reference voltages is beyond the scope of this book.

6.9.1 **Resistor accuracy and tracking** is achieved using thin film manufacturing techniques, so that error contributions other than from the switches are negligible. The ratio $\frac{R}{2R-K+r_{DS(on)}}$ determines the accuracy of the binary weighting (Figs. 6.3, 6.4, 6.5). K is the adjustment made to the value of 2R, to compensate for the switch resistance $r_{DS(on)}$. It is made equal to the nominal value of the ON resistance of the switch. Since the ladder network resistors R and 2R are usually designed to track, the temperature performance of the term $\frac{R}{2R-K+r_{DS(on)}}$ will depend on the resistance characteristics of R_{on}. Some typical performance figures are listed in Table 6.2.

Table 6.2

Device	$r_{DS(on)}$ (Typical)	$\Delta r_{DS(on)}$ (Typical)	Temp Coefficient (Typical) % per °C	**Maximum Converter Reference Voltage
DG180A	7 ohms	±20%	0·5	+15V, -10V
DG190A	24 ohms	±20%	0·5	+15V, -7.5V
DG200A	60 ohms	±10%	0·4	±15V
DG201A	150 ohms	±10%	0·4	±15V
DGM111	*50 ohms 150 ohms	300%	0·5	+15V, —10V
DG133A	24 ohms	±20%	0·5	+15V, -7.5V
DG141A	7 ohms	±25%	0·5	+15V, -7.5V

*Value varies with Analogue signal: with 15V reference, $r_{DS(on)}$ = 50 ohms, with -10V reference, $r_{DS(on)}$ = 150 ohms.

**±15 volts supplies.

The deviation in $r_{DS(on)}$ from its nominal value due to production spreads, as shown in Table 6.2, also affects the accuracy of the term $\frac{R}{2R-K+r_{DS(on)}}$.

The effect of these variations on the accuracy is shown in the following example.

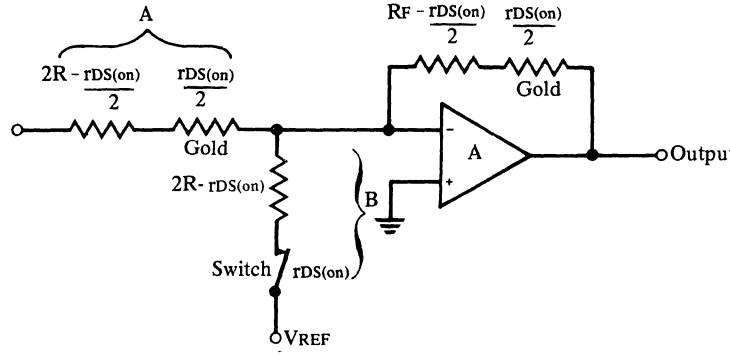
A common value of R in thin film networks is 10kohms. For a 10-bit converter with an overall accuracy of 0·05% ($^1/_2$ least-significant bit), the accuracy of the most significant bit is required to be better than 0·025%. (±2·5 ohms). The allowed accuracy for each successively less significant bit is doubled in a binary converter; therefore, the accuracy of the second and third most significant bit are ±5 ohms and ±10 ohms respectively.

With this requirement in mind, inspection of Table 6.2 highlights the suitability of different IC analogue switches for the MSB in this application. The DG141A and DG180A, having typically 7 ohms ON resistance, come close to requiring no compensation in the 2R resistor value (i.e. K=0). The DG190A and DG133A which have typically 24 ohms ON resistance also fit the requirement very well as does the DG200A. The DG201 is not suitable for the most significant, but is adequate for any less significant bits. The DGM111 in common with all PMOS switches is the least suitable for this application. This is because switch resistance of all PMOS IC analogue switches varies with applied signal voltage (Chapter 2, section 2.2.2). However, it might be used with positive and ground references because the variation in ON resistance in that case is reduced.

6.9.2 Switch Temperature Compensation

A converter has to maintain its accuracy over a range of temperatures. Thin film resistors have much lower temperature coefficients than semiconductors and it is the temperature coefficient of the switch resistance that controls the overall temperature performance. For a 50°C increase in temperature there will be approximately a 27% increase in switch resistance $r_{DS(on)}$. This would not be significant for the DG141A in a 10-bit system due to its low ON resistance. The use of any other analogue switch in Table 6.2 would, however, introduce inaccuracy. Such inaccuracy can be partially overcome by introducing in series with resistor R, a small gold resistor equal to one half the typical value of the switch resistance (Fig. 6.16).

Fig. 6.16 **Switch temperature coefficient compensation**



This is relatively simple, since gold is often used for contacts in the fabrication of the resistor network, and has a +0·4% per °C temperature coefficient of resistance. The thin film resistor temperature coefficient is approximately 0·005% per °C which is negligible compared with the switch temperature coefficient. Thus, as temperature varies, R increases by the same percentage as 2R, and accuracy is maintained.

Referring to Fig. 6.16, over a 50°C range $\frac{r_{DS(on)}}{2}$ (gold) increases by 20% and $\frac{r_{DS(on)}}{2}$ switch by 27%. The binary ratio is given by:

$$A/B = \frac{R - \frac{r_{DS(on)}}{2} + \frac{1.2\, r_{DS(on)}}{2}}{2R - r_{DS(on)} + 1.27\, r_{DS(on)}} = \frac{R + 0.10\, r_{DS(on)}}{2R + 0.27\, r_{DS(on)}}$$

If R = 10kohms, $r_{DS(on)}$ = 50ohms, this term equals 0·499913 which is an error of 0·0174%. The resolution of a converter may be extended at the most-significant bit end of the network. Accuracy here is most critical and the MSB of a 10-bit unit will not be accurate enough for 12-bits. The inclusion of 0·012% accuracy resistors and switch combinations in front of the MSB would allow 12-bit operation.

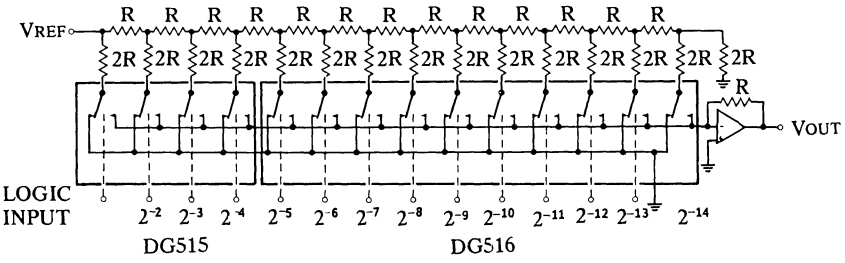
6.9.3 Specialised Switches

Switch arrays such as the DG515, DG516 are designed specifically for use in D-A converters. These are arrays of n-channel FET switches complete with complementary MOS interface drivers. The four main requirements in such a switch array are :

1) Low Power Consumption. This is achieved by the use of CMOS switch drive circuits described earlier. Both DG515 and DG516 dissipate 40 microwatts in the quiescent state.
2) Low Switch ON Resistance. The use of n-channel MOS switches provides a low value of resistance. In the DG515 the most significant bit switches have resistances of only 6·25 ohms. The value doubles for each less significant bit position.
3) High matching accuracy between switches for each bit. This is achieved by virtue of the monolithic process giving better than 20% resistance match between the switches.
4) High Switching Speed. The simplicity of the CMOS switch driver results in a short propagation delay. This gives high operating speed capability (t_{on} and t_{off} are less than 200 nanosecs).

The use of a resistor ladder network with a value of R = 25 kohms makes possible a 14 bit D-A converter using the DG515 and DG516 (Fig. 6.17). If the ladder resistances R and 2R have been adjusted to compensate for the nominal switch resistance R_{on}, it will be the mismatch between the devices in a switch pair which will reduce overall accuracy.

Fig. 6.17 **14 bit D-A converter employing DG515 and DG516**



For example:

If mismatch = 20% of 6·25 ohms = 1·25 ohms, inaccuracy = $\frac{1 \cdot 25}{25{,}000} = 0 \cdot 005\%$

This alone is sufficiently accurate for a 14 bit converter (14 bit ± $^1/_2$ bit accuracy = 0·00625%). However, extreme care is needed to reduce all other possible errors in the system to this level.

The DG516 alone enables an economic 10 bit D-A converter to be produced. In this device, the lowest switch resistance is 100 ohms.

The DG515 and DG516 are both designed to be used in circuits terminated at the summing node of an amplifier. This configuration reduces the effective reference voltage seen by the switches and eases the design of a multiplying D-A converter where the reference voltage terminal receives the analogue signal.

6.10 ADVANTAGES GAINED BY THE USE OF FET SWITCHES

The main advantage of using FET switches over other forms of static switches in A-D and D-A converters is the possibility of employing larger than normal reference voltages, hence reducing the significance of switching spikes and other noise voltages. With both current steering switches and inverting bipolar saturated switches, reference voltages above 5 volts are difficult to handle. In the case of current steering switches, power dissipation becomes excessive unless one uses large values of resistors, which is undesirable in normal monolithic construction. Where inverted bipolar saturated switches are used, the BV_{ebo} now becomes the BV_{cbo} of the switch. Only in specially made devices, usually p-n-p bipolars, is this value greatly above 5 volts. Thus, it requires more sophisticated techniques to handle references above this value.

The use of ±15 volt reference improves system performance. The amplifier closed loop gain can now be reduced because the input signal amplitude is greater. This results in a better overall noise performance, and increases the system bandwidth. From Table 6.2, it can be seen that the DG200A and DG201A are the most suitable devices, capable of handling the largest references. Commercially available D-A units have limitations when used in high voltage digitally programmable power supplies requiring 0·1% accuracy. These units normally employ reed relay switches which are a reliability problem. The inclusion of semiconductor switches would improve the speed, ruggedness and above all the reliability of the equipment. Such a programmable power supply could use a DG200A to switch the most significant bit followed by a DG201A in the next two bits and DG201C in the remaining bits. The references could be ±15 volts.

6.11 SUMMARY OF A-D and D-A CONVERSION APPLICATIONS

There are many techniques of D-A and A-D conversion. The selection of a technique and the hardware to realise it requires an understanding of all the considerations of system space, weight, cost, speed, accuracy and characteristics of the components such as integrated analogue switches. The question "To Build or Buy?" is always present but the modern integrated analogue switch with the right technique offers many benefits especially where standard conversion blocks are unsatisfactory.

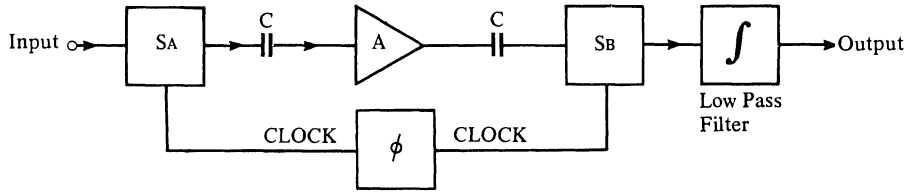
6.12 CHOPPING

There are many applications in measurement where either the analogue signal is below the resolution of an A-D converter or is so low as to be rendered inaccurate by temperature and long term drift effects in the system. In such cases the signal has to be amplified before conversion or transmission.

Many sophisticated techniques have been employed to reduce temperature and

long term drift in amplifiers and one method is to use the chopper stabilised amplifier. The basic form of this is shown in Fig. 6.18. The analogue signal is converted by switch S_A into a pulse train, the amplitude of the pulses being equal to the signal value. These pulses are then amplified by an a.c. amplifier which has inherently less drift than a d.c. amplifier. The amplified pulses are demodulated by switch S_B, and then low-pass filtered to give an amplified form of the analogue input signal.

Fig. 6.18 **Typical schematic of a chopper amplifier**



The offset and drift performance of the overall system, shown in Fig. 6.18 is determined by the switch parameters and in particular those of switch S_A. A study of available integrated switches will enable selection of the most economic type for the required overall performance.

There are three basic forms of chopper switch configuration in common use, namely "Series", "Shunt" and "Series-Shunt". All three types introduce attenuation into the amplifier system but this is easily compensated for by means of gain adjustment. Deviations of the device parameters from the typical values are the main cause of errors and, therefore, must be minimised to achieve the optimum performance.

The inherent characteristics of FET switches make them well suited for use in chopping systems where the important characteristics are ON resistance, OFF leakage and gate-to-channel capacitance.

FET IC switch performance and selection criteria are presented in the following sections.

6.13 PERFORMANCE and SELECTION of FET SWITCHES for CHOPPERS

6.13.1 Temperature Effects on Leakage and Resistance

The variation of ON resistance and OFF leakage currents with temperature are common problems that require compensation . Fig. 6.19 shows the typical variation of OFF leakage current with temperature for a JFET. As leakage current approximately doubles for every 10°C increase in temperature a 10pA leakage at 25°C becomes 10nA at 125°C. This is significant if the system employs large resistor values. The variation of ON resistance with temperature has been discussed in Chapter 1, section 1.9.1.1.

6.13.2 Low Frequency Performance of FETs as Chopper Switches

6.13.2.1 Series Chopper

Figs. 6.20, 6.21 and 6.22 show a FET series chopper and the d.c. equivalent circuits.

Fig. 6.19 **Temperature variation of JFET switch leakage current.**

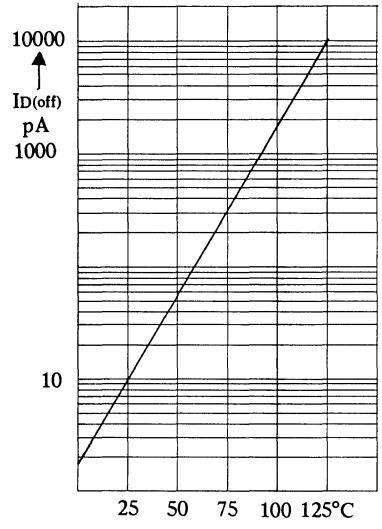
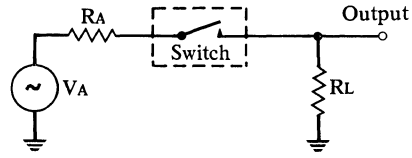


Fig. 6.20 **Series chopper schematic.**



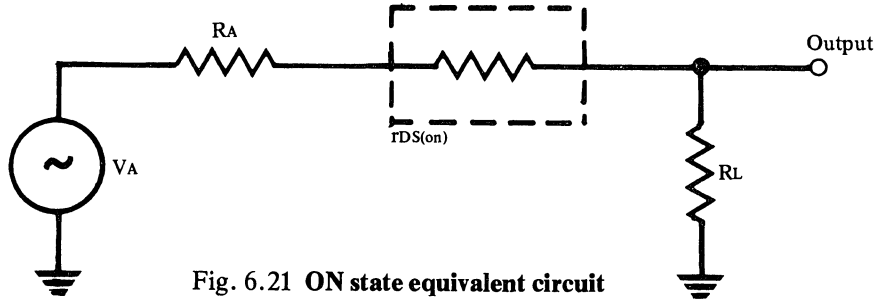


Fig. 6.21 **ON state equivalent circuit**

System error incurred due to switch resistance in the ON state $= \frac{r_{DS(on)}\, V_A}{R_L + r_{DS(on)} + R_A}$

Example: If R_A = 1kohm (Fig. 6.21), R_L = 10kohms, $r_{DS(on)}$ = 50 ohms

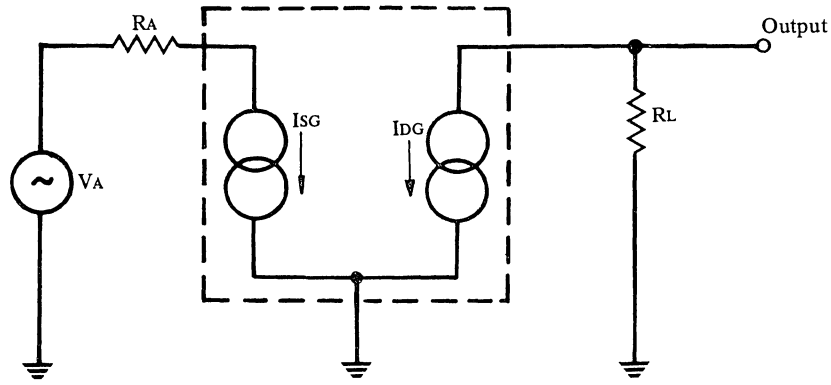
$$\text{Error voltage} = \frac{50\, V_A}{11 \cdot 050} = 0 \cdot 5\% \text{ of } V_A$$

This ON state error can be compensated for by gain adjustment in the amplifier. However, there will be additional contributions to the ON state error due to:

1) An uncertainty of +70% to —50% in the value of $r_{DS(on)}$ due to ambient temperature variation from 125°C to —55°C respectively.
2) The variations in $r_{DS(on)}$ due to production spreads. This could be ±10 ohms.

These two effects combine so that compensation calculated for 25°C will not in fact be better than 1% at temperature extremes with production spreads in $r_{DS(on)}$. This can be calculated using the equation in the above example.

Fig. 6.22 **OFF state equivalent circuit**



The switch drain leakage current I_{DG} produces an offset when flowing through the load resistance R_L (Fig. 6.22). The source leakage current merely flows through the signal source impedance and produces no offset at the output.

If $I_{DG} = 50pA$ at 25°C and $R_L = 10kohms$

at 25°C: Error voltage $= \frac{-50}{10^{12}} \times 10^4 = -0{\cdot}5\mu V$

at 125°C: Error voltage $= \frac{-50}{10^9} \times 10^4 = -0{\cdot}5mV$

It is obvious that for a system with $10\mu V$ signals, an error of 0·5 millivolts is completely unacceptable. This is the major reason why the series chopper technique is rarely used.

6.13.2.2 Shunt Chopper

Figs. 6.23, 6.24 and 6.25 show a FET Shunt Chopper and its d.c. equivalent circuits.

Fig. 6.23 **Shunt chopper schematic**

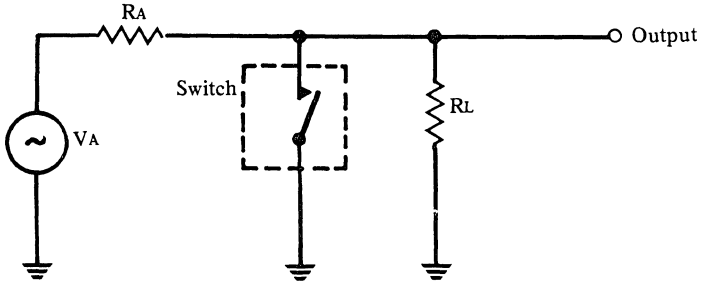
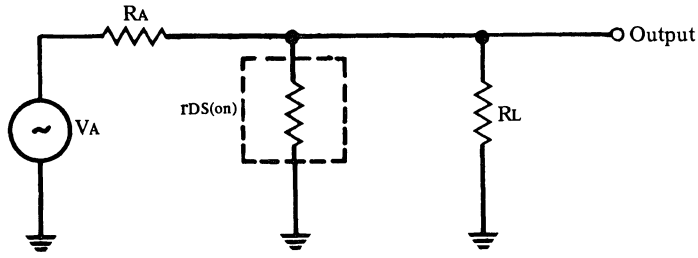


Fig. 6.24 **ON equivalent circuit.**



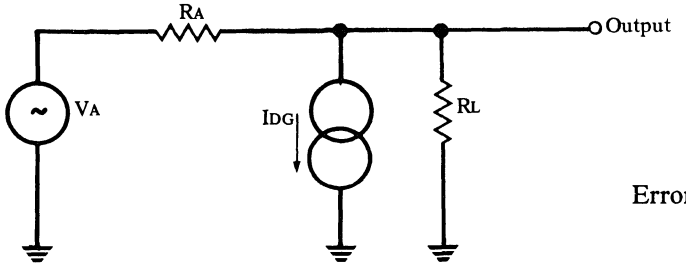
The error voltage at the output can be calculated assuming the values used in the following example, in conjunction with Fig. 6.24 and 6.25.

Example: R_A = 1kohm, R_L = 10kohm, $r_{DS(on)}$ = 50 ohms. Since $r_{DS(on)} << R_L$

$$\text{Error Voltage} = \frac{r_{DS(on)}\, V_A}{r_{DS(on)} + R_A} = 5\%\ V_A$$

This error could again be compensated for in the amplifier at 25°C but it is the variation in $r_{DS(on)}$ with temperature that is the real problem. Production tolerance on $r_{DS(on)}$ will allow variations of ±20%, and the overall error due to this alone would be ±1%. The temperature variation of $r_{DS(on)}$ will vary the error by +70% to —50% so that at worse, compensation for a 5% error at 25°C could still be 2·5 to 3·5% incorrect at temperature extremes. This, however, is much better than the series switch where the error could swamp the signal.

Fig. 6.25 **OFF state equivalent circuit.**



$$\text{Error Voltage} = \frac{I_{DG} R_L R_A}{R_L + R_A}$$

In the OFF state the shunt-switch parameter of importance is the drain gate leakage current I_{DG}. The switch source is grounded and so the source leakage current I_{SG} flows into ground and has no effect on the circuit.

If I_{DG} = 50pA at 25°C, R_L = 10kohms and R_A = 1kohm,
at 25°C: Error Voltage = -0·05μV.
at 125°C: Error Voltage = -50μV.

While this seems a significant improvement over the series circuit, it must be remembered that the values of source and load impedances have a controlling effect.

6.13.2.3 Series-Shunt Chopper

A combination of the series and shunt chopper circuits offers significant improvement in both ON and OFF conditions. Figs. 6.26, 6.27 and 6.28 show the configuration and its equivalent circuits for both the ON and OFF states.

Fig. 6.26 **Series-Shunt chopper.**

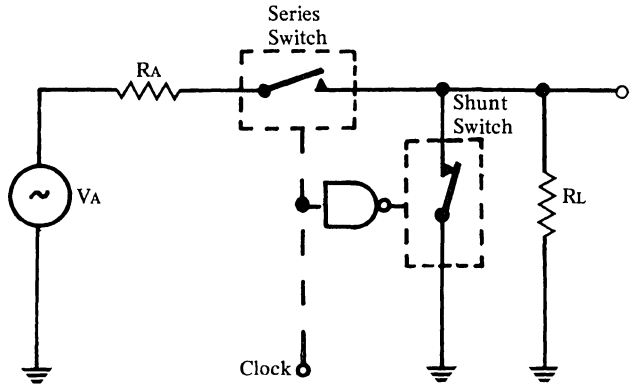
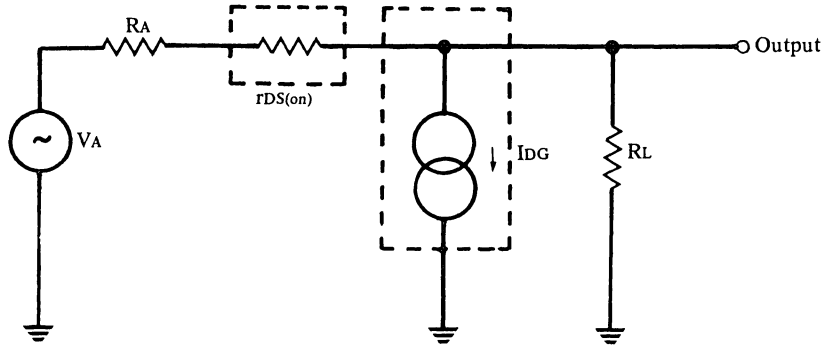


Fig. 6.27 **Series ON, Shunt OFF equivalent circuit.**



The error in output voltage due to signal loss across the series switch plus the offset caused by shunt switch leakage is:

$$\frac{r_{DS(on)} \cdot V_A}{R_L + R_A + r_{DS(on)}} + I_{DG} \frac{(R_A + r_{DS(on)})(R_L)}{R_A + r_{DS(on)} + R_L}$$

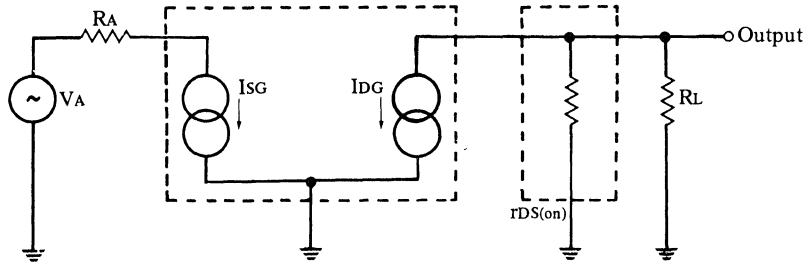
Using the same values as in previous examples:

at 25°C: Error Voltage $= \frac{50V_A}{11 \cdot 05k} + 50 \frac{(1k + 50)(10k)}{11 \cdot 05k} = 0 \cdot 5\%\ V_A + 0 \cdot 05\mu V.$

at 125°C: Error Voltage $= 1 \cdot 0\%\ V_A + 50\mu V$

This is an improvement on the shunt circuit OFF condition.

Fig. 6.28 **Shunt ON, Series OFF equivalent circuit**



The output error voltage is due to the series switch leakage generating an offset voltage across the parallel combination of $r_{DS(on)}$ (shunt) plus R_L:

$$\text{Error voltage} = I_{DG} \frac{r_{DS(on)} \cdot R_L}{r_{DS(on)} + R_L}$$

Substituting the same values as before,

at 25°C: Error Voltage = $\frac{50 \times 50 \times 10k}{10^{12} \quad (50 + 10k)} = \cdot 0025\mu V$

at 125°C: Error Voltage = $5\mu V$.

Fig. 6.29 **Series-Shunt chopper output waveform**

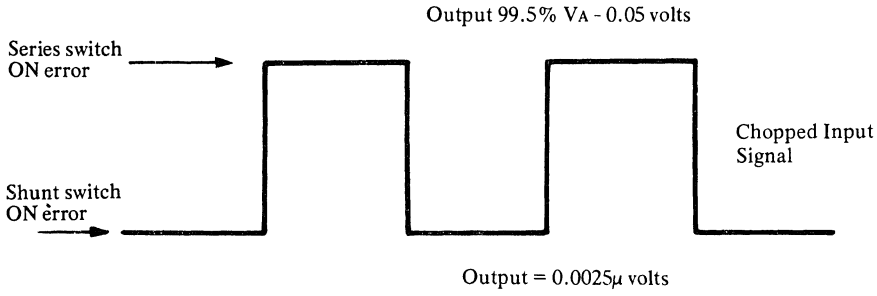
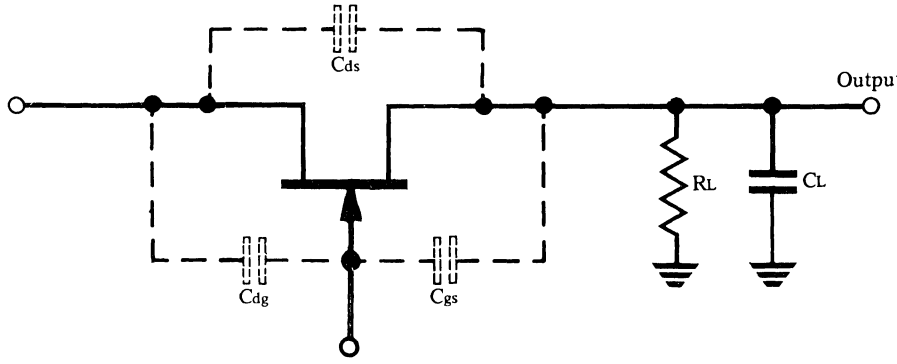


Fig. 6.29 shows the effect of these errors on the chopped input signal. From the three cases analysed, it is obvious that the Series Shunt Chopper offers the best performance under static conditions. However, in the transient state, when the switching system is changing from one condition to another the Series-Shunt Chopper offers even more advantages.

6.13.2.4 Dynamic Performance of FETS as Chopper Switches

Fig. 6.30 is the equivalent circuit of a FET switch showing the basic capacitances that exist. These capacitances couple transients to the signal line from the control gate when the device is switched between states.

Fig. 6.30 **FET switch capacitances.**



At the frequencies normally found in chopper applications (about 200 Hz), C_{ds}, typically 0·1pF, can be ignored; the most important capacitances being C_{dg} and C_{sg}.

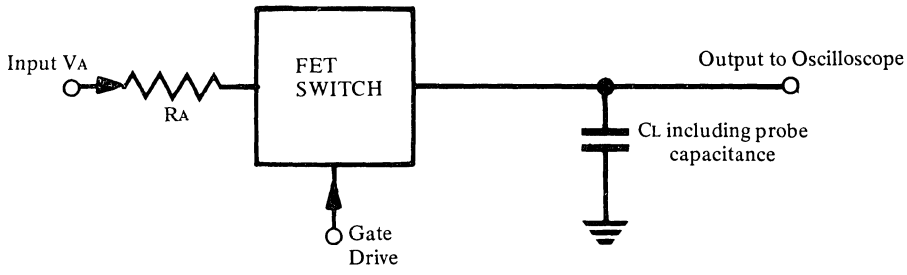
Any change in the control voltage on the gate terminal is coupled directly into the analogue signal path via these capacitances, and this is referred to as charge transfer from the gate circuit to the load. The charge transfer is given by:

$$\Delta Q = \Delta V C_L$$

where ΔQ is the charge transferred between gate and load capacitance (C_L), and ΔV is the resultant error voltage.

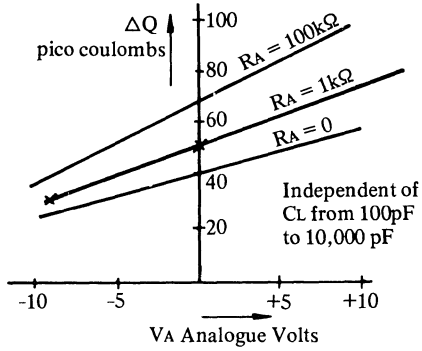
Figure 6.31 shows a simple experimental set up to measure ΔQ *(Ref. 6.5).*

Fig. 6.31 **Charge transfer measurement**



Figs. 6.32, 6.33 and 6.34 show results for integrated analogue switch types DG190, DG172 and DG200. In chopper applications, the V_A signal level is very low and can be assumed equal to zero for deriving the value of ΔQ.

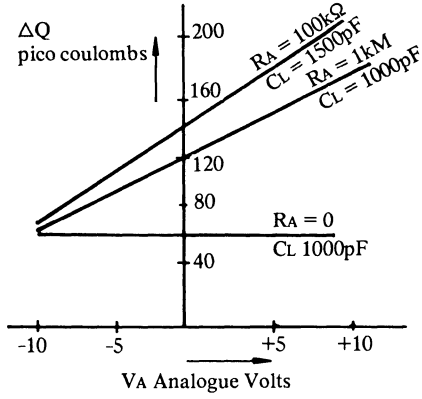
Fig. 6.32 **Charge transfer in JFET switch.**



$\Delta Q = 50$ pico coulombs
therefore, for a C_L of 1000 pF

$$\Delta V = \frac{\Delta Q}{C_L} = 50\text{mV}$$

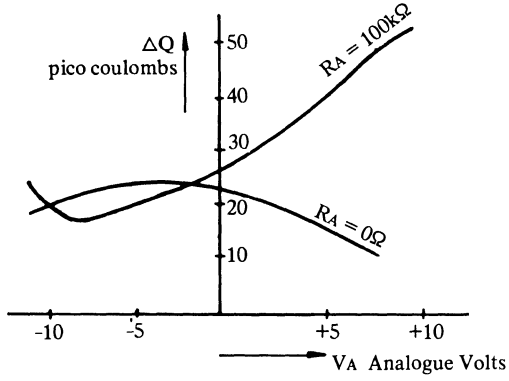
Fig. 6.33 **Charge transfer in PMOS FET switch.**



$\Delta Q = 120$ pico coulombs
therefore, for a C_L of 1000pF

$$\Delta V = \frac{\Delta Q}{C_L} = 120\text{mV}$$

Fig. 6.34 **Charge transfer in CMOS FET switch.**



$\Delta Q = 25$ pico coulombs
therefore, for a $C_L = 1000$pF

$$\Delta V = \frac{\Delta Q}{C_L} = 25\text{mV}$$

The charge transfer figures given in Figs. 6.32, 6.33 and 6.34 above refer to a single switch arrangement. In the case of the Series Shunt combination, which has many d.c. advantages, the presence of the second switch operating in

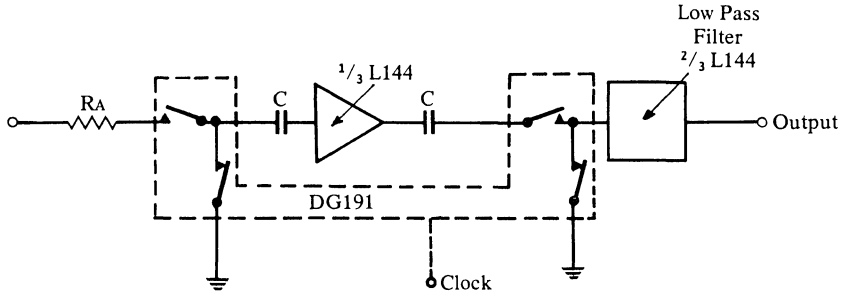
antiphase provides charge compensation resulting in a net ΔQ of the order of 10pico coulombs.

The values of switch capacitances are fixed by the device characteristics. In selecting a switch for a chopping application one has to compromise between d.c. and a.c. performance to obtain an optimum economic solution.

There are techniques available for charge transfer minimisation and transfer cancellation which are discussed in Chapter 4.

The best performance is obtained with the Siliconix DG180/190 series. This offers low $r_{DS(on)}$, low C_{gd} and can operate from low voltage supplies. Its low t_{on} and t_{off} times allow high frequency chopping and up to 4 switches per package are available. It is possible to couple the DG191 with low power amplifiers such as the L144 so that the whole system, including the TTL clock driver, can handle +5 to —2V signals with ±5V rails. Fig. 6.35 is a schematic of such a system.

Fig. 6.35 **Chopper amplifier**



The typical performance for this configuration is as follows:

The equivalent input noise voltage of the L144 over the bandwidth 0·1Hz to 100Hz is 2 microvolts. The pulse breakthrough is approximately 20 millivolts and the low-pass filter has a roll off of 12dB/octave with a 3dB point at 100Hz. The switch is driven from TTL at 1kHz clock frequency.

6.14 SUMMARY of CHOPPING APPLICATIONS

There are a variety of ways of realising low drift chopper amplifiers. Techniques range from small electro-mechanical through discrete transistor, to integrated semiconductor switches. There may be some cases where the older established electro-mechanical seem to yield an effective approach, but with the trend towards higher reliability, increased packing density, lower power consumption and higher speeds the integrated analogue switch is coming more and more into favour.

6.15 APPLICATION CIRCUITS

The following is a list of applications pertaining to Chapter 6 which can be found in "Applications Information," Chapter 7. Please refer to the page number indicated.

6.15.1 Digitally Selectable Amplifier Control Circuits

.1 *Low Power Inverting Amplifier with Digitally Selectable Gain* – AN76-6, Page 7-90, Figure 29.

.2 *Polarity Reversing Low Power Amplifier* – AN76-6, Page 7-91, Figure 30.

.3 *A Precision Amplifier with Digitally Programmable Inputs and Gain* – AN75-1, Page 7-67, Figure 8.

.4 *Low Power Binary to 10^n Gain Low Frequency Amplifier* – AN76-6, Page 7-86, Figure 17.

6.15.2 D to A Converters (Refer to Section 6.2)

Figure 6.36 **6-Bit A/D Converter**

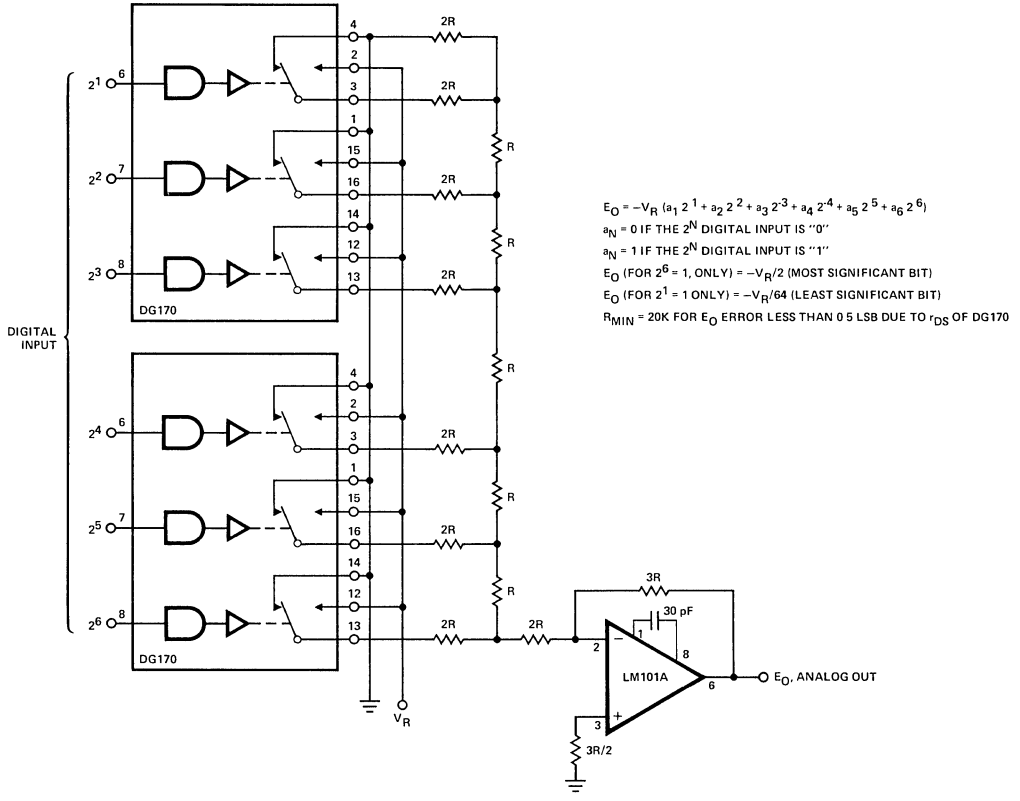
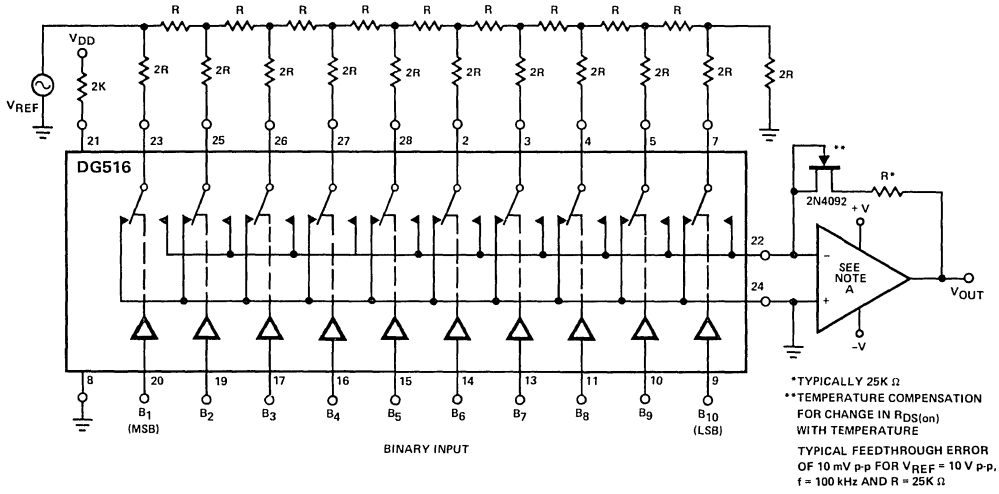


Figure 6.37 10-Bit D/A Converter



Unipolar Binary Operation

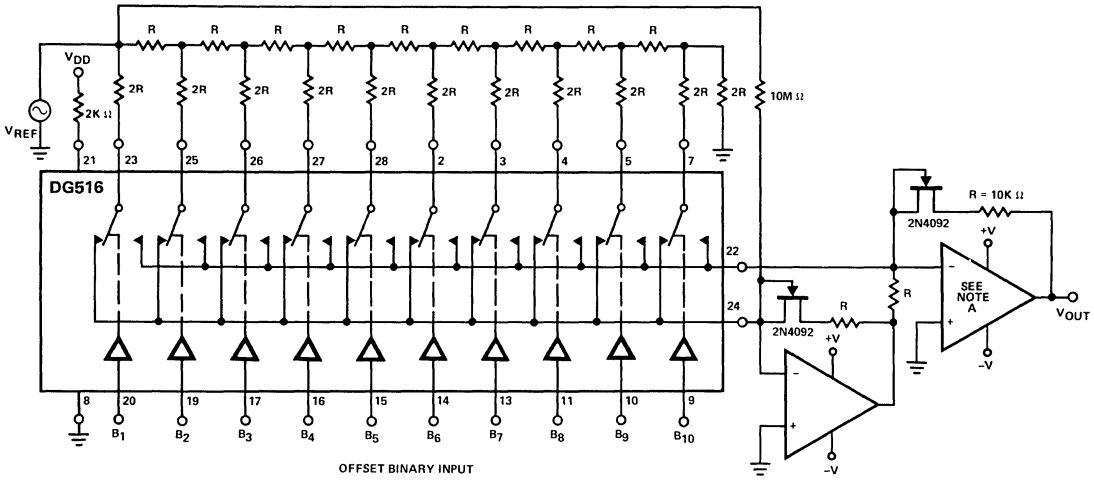
DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1-2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(1/2+2^{-10})$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}(1/2-2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

NOTE:

A. Op-Amp characteristics effect D/A accuracy and settling time. The following Op-Amps, listed in order of increasing speed, are suggested:

1. LM101A
2. LF156A
3. LM118

Figure 6.38 10-Bit, 4 Quadrant Multiplying DAC
(Offset Binary Coding)



Bipolar (Offset Binary)* Operation

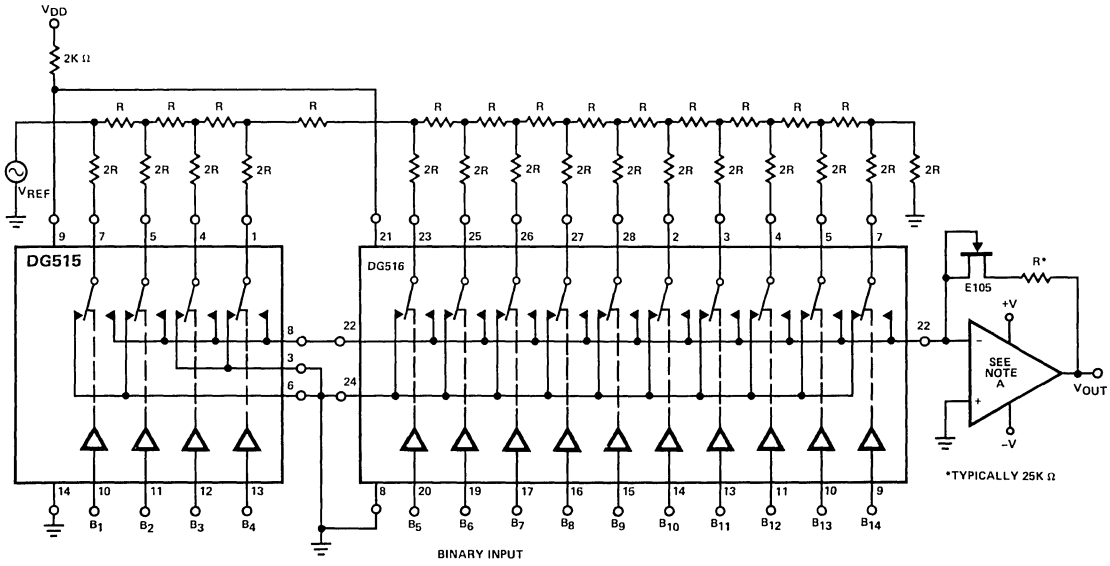
DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\,(1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\,(2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}\,(2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}\,(1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}
NOTE: 1 LSB = 2^{-9} V_{REF}	
*Complementing B_1 (MSB) will give 2's complement coding	

NOTE:

A. Op-Amp characteristics effect D/A accuracy and settling time. The following Op-Amps, listed in order of increasing speed, are suggested:

1. **LM101A**
2. **LF156A**
3. **LM118**

Figure 6.39 14-Bit Binary DAC (Unipolar)



CHAPTER 6

Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-14})$
1 0 0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (1/2 + 2^{-14})$
1 0 0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
0 1 1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1/2 - 2^{-14})$
0 0 0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-14})$
0 0 0 0 0 0 0 0 0 0 0 0 0 0	0

NOTE:

A. Op-Amp characteristics effect D/A accuracy and settling time. The following Op-Amps, listed in order of increasing speed, are suggested:

1. **LM101A**
2. **LF156A**
3. **LM118**

6.15.3 Digitally Controlled Attenuators in A/D Converter Autorange Systems

The following circuits use analog switches as input ladder attenuating switches. The switches are controlled by digital logic which detects overrange and underrange information from the A/D converter and closes the appropriate switch for necessary attenuation. The attenuating ladder is a resistive divider, 10M Ω input and 1M Ω to 1K Ω on the ladder. Note that the 1K Ω must be adjusted to include the $r_{DS(on)}$ of the switch.

Two circuits are shown for autoranging. The first (suitable for the Siliconix LD110/111 or LD111/114 – refer to Ref. 6.6) uses underrange and overrange information in the form: $\overline{D_1 + D_2 + D_3 + D_4}$ (all four digit lines simultaneously low) and underrange = $B_4 \times D_4$. The circuit shows the logic interface and the underrange and overrange pulse inputs to the shift register.

The second circuit is shown for both the DG201 and DG304. This autorange circuit (suitable for the Siliconix LD130 – refer to Ref. 6.7) uses overrange and underrange information as: underrange = D_1 x pulse input, overrange = D_2 x pulse input. The point where the underrange and overrange input to the flip flop is shown for use in other A/D systems which decode overrange and underrange differently.

Figure 6.40 **DVM Autorange Circuit for A/D Systems without Interdigit Blanking (Such as Siliconix LD110/111, LD111/114)**

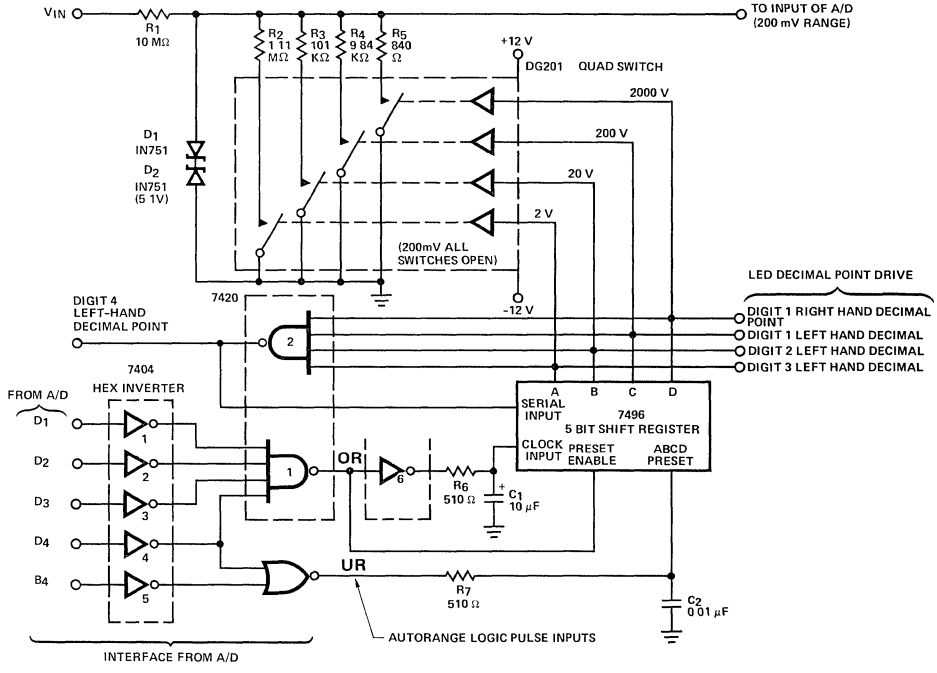
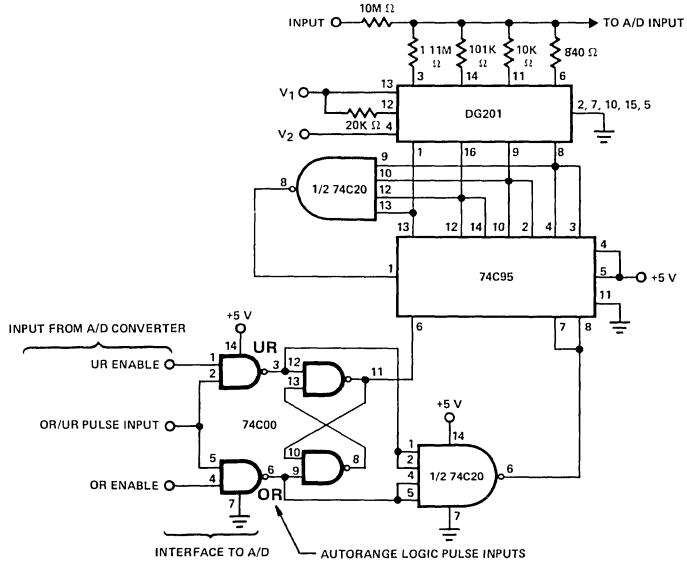
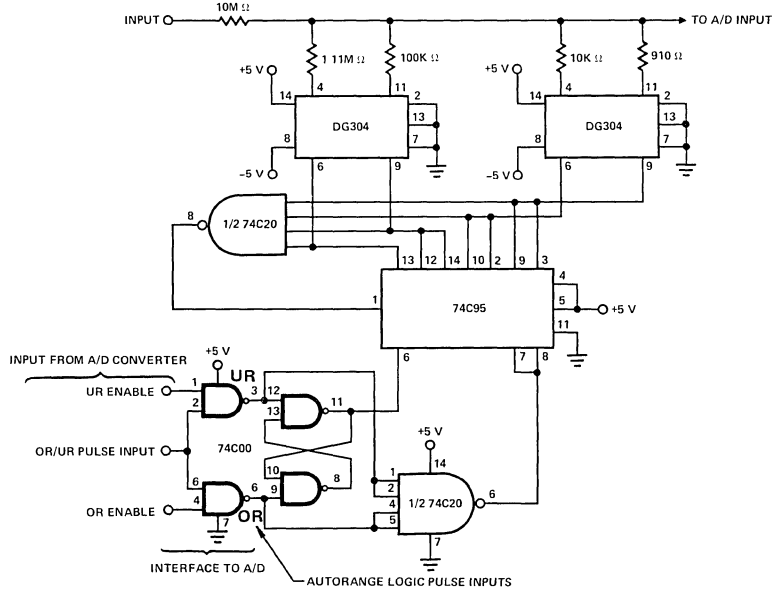


Figure 6.41a **DG201 DVM Autorange Circuit for A/D Systems with Autoranging Pulse Outputs (such as Siliconix LD130, see Ref. 6.7)**



6.41b **DG304**



Note: See Design Aid DA76-3 for DVM circuit detail. (Ref. 3)

6.16 REFERENCES

6.1 David F. Hoeschele Jr., "Analog-to-Digital and Digital-to-Analog Conversion Techniques," Wiley & Sons, 1968.

6.2 Hermann Schmid, "Electronic Design Practical Guide to D/A and A/D Conversion." Electronic Design, Oct. 1968.

6.3 Richard E. Defreitas, "DELTAVERT TM – Signal Transmission and Data Conversion," EPN Seminar Proceedings, Paris, April 1974.

6.4 Richard S. Cobbold, "Theory and Applications of Field Effect Transistors." Wiley & Sons, 1970.

6.5 Gary Dixon, "Analog Switches in Sample-and-Hold Circuits," Siliconix Application Note. (AN74-2, p. 7-57.)

6.6 Gary Grandbois, "Function and Application of 3½ Digit A/D Converter Set," Siliconix Application Note, AN74-1.

6.7 Gary Grandbois, "Applying the LD130 ±3 Digit A/D Converter," Siliconix Application Note, AN76-5.

Chapter 7

Applications Information

7.1 FETs as Analog Switches (AN72-2)

September 1972

INTRODUCTION

The past few years have seen a pronounced growth of analog/digital systems which employ integrated circuits. One of the interface elements in such a system is the digitally-controlled analog switch. As more and more applications arise for the analog switch, especially in the areas of industrial processing and control, the question is often asked: "Which is the best switch for my application?"

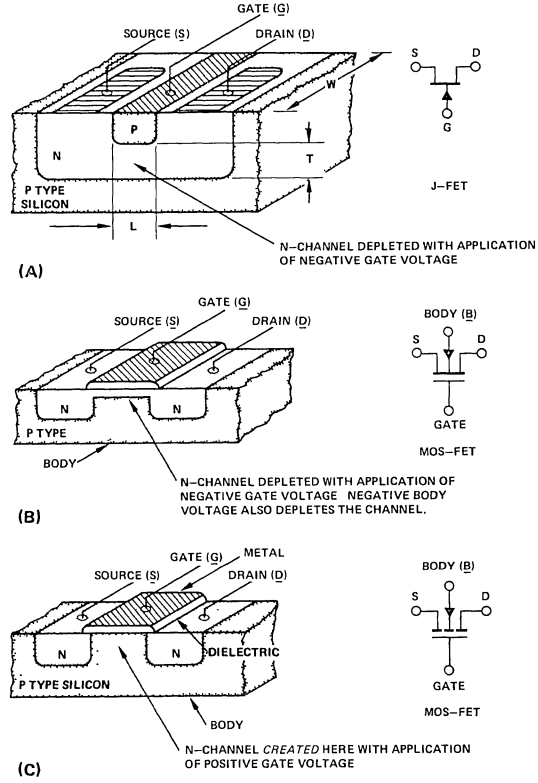
The sheer variety of applications precludes any pat answer to this question; however, the user of analog switches can gain valuable insight on the subject through an understanding of the nature of solid-state switches. Areas which require exploration include:

(1) Basic factors affecting switch performance.
(2) Details of switch-driver circuit design.
(3) Total switching characteristics of driver circuits and switches.
(4) Characterization of the analog switch at high frequencies.

The intent of this Application Note is to consider (1) above, in detail, with minor attention to the other areas. Other Application Notes in this series will handle subjects (2) through (4) in greater depth.

Field-Effect Transistor Operation

The field-effect transistor (FET) is in effect a conductor whose cross-sectional area may be varied by the application of appropriate voltages. When the conducting area (the channel) is maximum, conductance is also maximum (minimum resistance). When the conducting area is minimum, conductance is minimum (maximum resistance). This phenomenon makes possible the use of FETs as analog switches. When conductance is maximum, the switch is in the ON state; when conductance is minimum, the switch is in the OFF state. In the ON state, an N-type channel contains N-type carriers; similarly, P-channel FETs contain P-type carriers. Cross-sections for three types of N-channel FETs are shown in Figure 1.



N-Channel FET Cross-Sections
Figure 1

P-channel FET cross-sections are quite similar, except that the channel contains P-type carriers and the voltage polarities are reversed. Depletion-mode devices are shown in Figures 1A and 1B; these FET types have high channel conductance (are ON) with zero gate-channel voltage, and are characterized as "normally-ON" switches. An enhancement-mode FET is shown in Figure 1C. This device requires that voltage be applied to the control gate to create a conducting channel – the ON state. Enhancement-mode FETs are said to be normally-OFF.

For enhancement-mode devices, channel conductance (g_{DS}) is a function of length (L), width (W), thickness (T), carrier mobility (μ), and mobile carrier concentration (Nc):

$$g_{DS} = K_1 \frac{WT}{L} \mu Nc$$

Effective channel thickness and carrier concentration are functions of the electric field in the channel. Voltage on the control gate changes the field, and hence the channel conductance, g_{DS}.

The gate voltage is applied with respect to the channel (source or drain). In most devices, the function of the source and drain can be interchanged, because of symmetrical FET geometry. By convention, however, voltage is specified between gate and source, V_{GS}. Figure 2 shows the variation of g_{DS} with V_{GS} for both N- and P-channel devices. In all cases, $g_{DS} = 1/r_{DS}$.

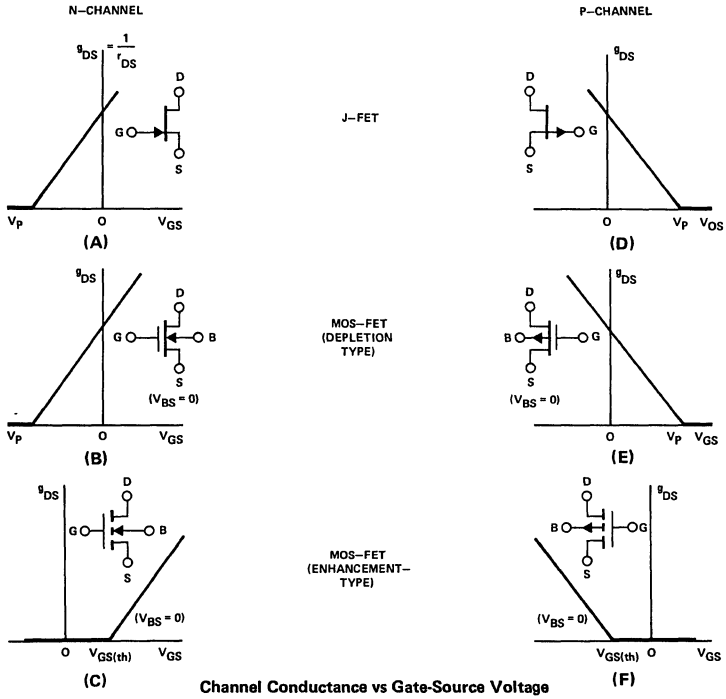
Note that the slopes ($\Delta g_{DS}/\Delta V_{GS}$) for all three types of N-channel FETs are constant and positive, while the slopes for the P-channel devices are constant and negative. N- and P-channel depletion-mode FETs are ON when $V_{GS} = 0$, while enhancement-mode devices of both types are OFF when $V_{GS} = 0$. Typically, the cut-off voltage, $V_{GS(off)}$, is designed to fall in the 1-to-10 volt range, while the gate-to-source threshold voltage, $V_{GS(th)}$ – that amount of voltage applied to the point where the device begins to conduct – falls in the 1-to-5 volt range. Figure 2 also demonstrates that g_{DS} is approximately a linear function of V_{GS}, with zero g_{DS} occuring at $V_{GS(off)}$ or $V_{GS(th)}$, as follows:

$$g_{DS} = K_2 |V_{GS} - V_{GS(off)}| \qquad \text{(depletion)}$$

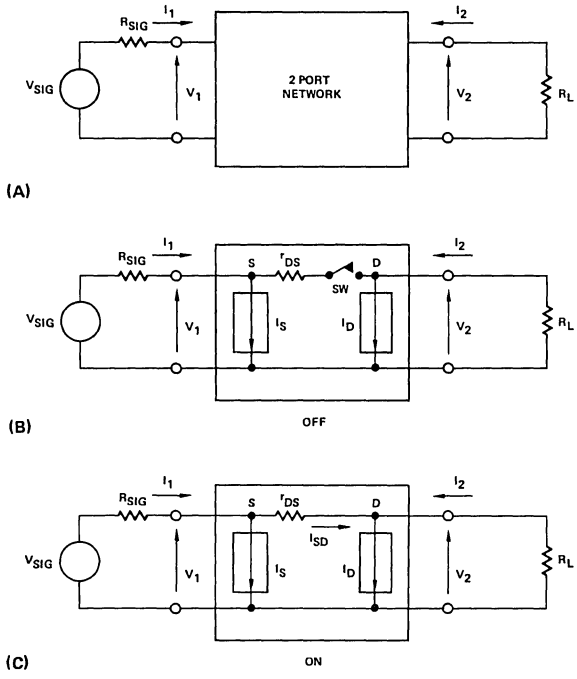
$$g_{DS} = K_2 |V_{GS} - V_{GS(th)}| \qquad \text{(enhancement)}$$

For a given active area, a junction FET (JFET) will have a higher conductance slope than a MOS FET. Additionally, N-channel carriers have higher mobility than P-type carriers. Thus, all things being equal, N-type FETs have higher g_{DS} ($= 1/r_{DS}$) than P-type devices. If the active area of the device is increased to raise the g_{DS} level, three other FET parameters will also be increased: leakage, capacitance, and cost. The design tradeoffs of these latter parameters are discussed in this Application Note.

When a FET is used as an analog switch, the drain-to-source voltage, V_{DS}, may be either positive or negative. In the OFF state, a typical switch may have $V_{DS} = \pm 20$ V. In the ON state, current flows equally well from drain to source or from source to drain (the channel is a resistor). For most applications, the voltage across the switch will be small.



Channel Conductance vs Gate-Source Voltage
Figure 2



D-C Equivalent Circuits
Figure 3

DC Equivalent Circuits

The perfect switch would have infinite resistance (zero conductance) when open and zero resistance (infinite conductance) when closed. While the FET is not a perfect switch, there are many applications where this deviation from perfection is unimportant. This statement can be justified by an analysis of the implications of the circuits shown in Figure 3.

The general two-port network in Figure 3A couples the signal source, V_{SIG}, to a resistive load, R_L. The network can be characterized by its terminal voltages and currents, V_1, V_2, I_1, and I_2. Figure 3B shows the equivalent circuit of a FET switch in the OFF state. In this condition, the "source" and "drain" are not connected to one another; however, two leakage current sources, I_S and I_D, are present. The same device is shown in the ON state in Figure 3C. The following typical values are assumed for the circuit:

$V_{SIG} = 10$ V (full scale)

$I_S = I_D = 1$ nA

$r_{DS} = 100\ \Omega$

$R_L = 200\text{K}\ \Omega$

$R_{SIG} = 10\ \Omega$

In the following calculations, leakage current (deviation from the state of a perfect switch) is expressed in terms of error percentage.

OFF Condition Calculation

(1) $I_1 = I_S = 1$ nA

$$V_{SIG} - V_1 = I_1 \cdot R_{SIG} = (1\text{ nA})(10\ \Omega) = 10\text{ nV}$$

$$\%\text{ Error in } V_1 = \frac{(10^{-8}\text{ V})(10^2)}{10\text{ V}} = 1 \times 10^{-7}\%$$

(2) $I_2 = I_D = 1$ nA

$$V_2(\text{off}) = I_2 R_L = (1\text{ nA})(200\text{K}\ \Omega) = -200\ \mu\text{V}$$

$$\%\text{ Error in } V_2(\text{off})^* = \frac{(2 \times 10^{-4})(10^2)}{10} = 0.002\%$$

ON Condition Calculation

$$I_1 = I_S + I_D - I_2$$

$$I_2 = \frac{V_2}{R_L} \cong \frac{V_{SIG}}{R_L + R_{SIG} + r_{DS}}$$

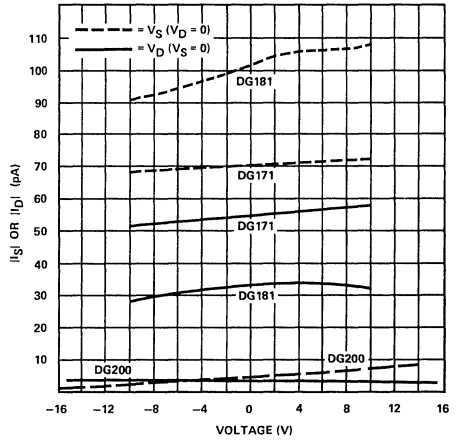
$$V_{SIG} - V_2 \cong (50\ \mu\text{A})(110\ \Omega) = 5.5\text{ mV}$$

$$\%\text{ Error in } V_2^* = \frac{(5.5 \times 10^{-3})(10^2)}{10} = 5.5 \times 10^{-2} = 0.055\%$$

*Referred to V_{SIG} (full scale)

The foregoing calculations indicate that for all but the most critical applications the performance of the FET equivalent circuits in Figure 3 is a good approximation of the perfect switch. In particular, the OFF condition leakage currents contribute only a negligible portion of total error.

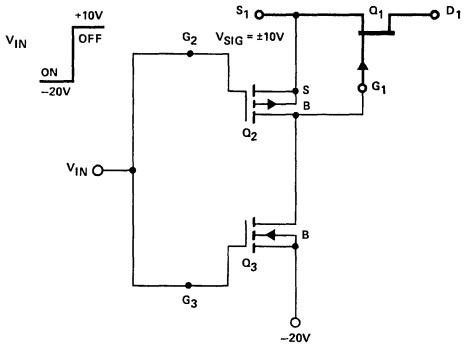
The actual error currents of three different types of FET switches are shown in Figure 4. The measured error is much lower than the 1 nA (1000 pA) obtained from the sample calculations. These data are taken from a MOS FET, an N-channel JFET, and a complementary MOS (CMOS) combination including a P-channel device and an N-channel device diffused onto the same substrate. The behavior of these FETs as elements of analog switching integrated circuits will be dealt with in detail elsewhere in this Application Note.



FET Switch Error Currents
Figure 4

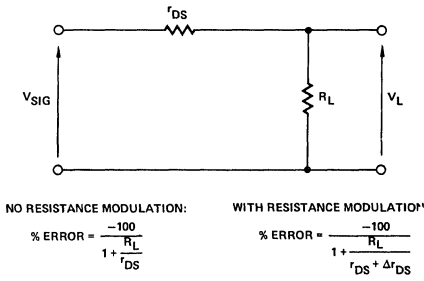
The JFET as a Switch

A suitable driving circuit must be considered when assessing the performance of the JFET as a switch. Such a circuit is shown in Figure 5.



JFET Switch Control Circuit
Figure 5

Note that Q_1 is an N-channel JFET, Q_2 is an enhancement-mode P-channel MOS FET, and Q_3 is an enhancement-mode N-channel MOS FET. From Figure 2, V_{IN} of −20 V will turn Q_2 ON and Q_3 OFF, so that S_1 and G_1 are connected (V_{GS} = 0 V) and Q_1 is ON. If V_{GS} is allowed to vary, g_{DS} (= $1/r_{DS}$) will also vary. This variation in resistance appears as a source of error when the switch is ON, and the error is defined as resistance modulation. In Figure 6, the error percentage in the case of resistance modulation is greater than that which occurs when Δr_{DS} = 0.

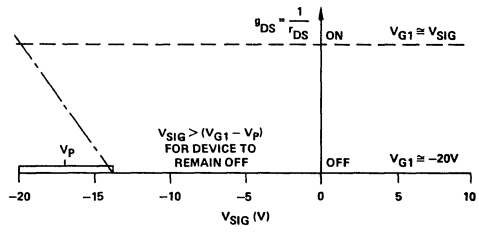


Error Due to Switch ON Resistance (r_{DS})
Figure 6

The suggested driving circuit of Figure 5 eliminates Δr_{DS} at low frequencies. The typical positive supply voltage is +10 V and the typical negative supply voltage is −20 V. In order for V_{GS} to change, current must flow through Q_2, which is ON. There are only two possible current paths through Q_2; (1), through Q_3, which is OFF and subject only to variations in leakage current, or (2), into the gate of Q_1, which is also subject to leakage current. Since both paths through Q_2 provide only negligible changes in V_{GS}, their effect in the circuit may be ignored. As the switching frequency is increased, capacitive reactance will provide lower impedance paths, so that some degree of Δr_{DS} is possible. Thus two conditions contribute to Δr_{DS} = 0 in the circuit. First, $V_{SIG} \cong V_{G1}$, due to the low impedance between these points. Second, the output impedance of Q_3 (driver output) is very large when compared to the R_{ON} of Q_2.

When V_{IN} is +10 volts, Q_2 is OFF and Q_3 is ON; G_1 is at −20 volts and Q_1 is OFF. In Figure 7, note that Q_1 will remain OFF only so long as $V_{SIG} > (V_{G1} - V_{GS(off)})$. $V_{GS(off)}$ is a *negative* voltage for an N-channel FET; thus the negative analog signal is limited by the $V_{GS(off)}$ of Q_1 and the negative supply ($V_{G1} \cong -20$ V).

The ON condition is also shown in Figure 7. g_{DS} is constant because with $V_{G1} \cong V_{SIG}$ imposed by the switch control circuit, $V_{GS} \cong 0$.

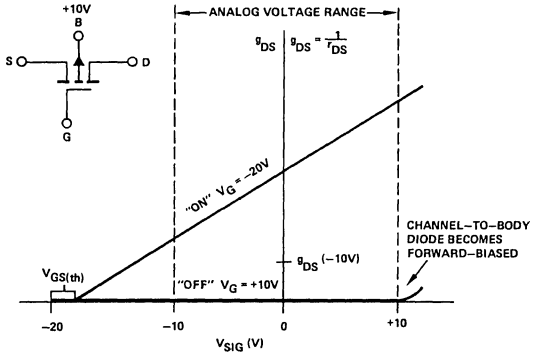


Switch ON Condition
Figure 7

The MOS FET as a Switch

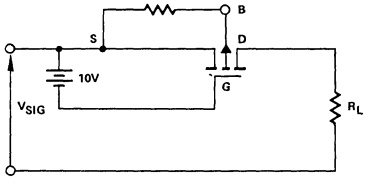
The P-channel enhancement-mode MOS FET is currently used in more applications than its N-channel counterpart. The consideration of MOS FET switch performance will thus center on P-channel devices.

The ON and OFF conditions of the MOS FET are analyzed in Figure 8. When the device is in the ON stage, note that the FET begins to turn ON when V_{SIG} (V_S or V_D) becomes $V_{GS(th)}$ volts more positive than V_G (= –20 V).



PMOS Channel Conductance (r_{DS}) vs Signal Voltage
Figure 8

Figure 8 also indicates that at any given point along the g_{DS} vs V_{SIG} curve, a unique value of g_{DS} will be obtained. Assume that a battery is inserted between the source and the gate, with the source clamped to the body as shown in Figure 9.



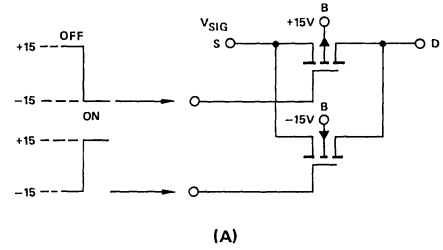
"Floating" Battery and Clamped Source
Figure 9

A constant voltage between source and gate will produce a constant value of g_{DS} vs V_{SIG}, provided that the body-to-source voltage is also constant. In a MOS FET, variation of the body-to-source voltage will also cause a modulation of g_{DS}. To further complicate the picture, several MOS FETs will have a common body when they are integrated on a single chip. Finally, the construction of a "floating battery" circuit is difficult. Thus MOS FET switch designers currently cope with the problem of Δr_{DS} by specifying r_{DS} for a given switch at several points over the entire analog voltage range.

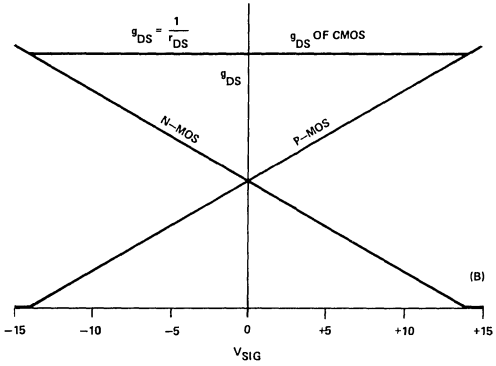
Referring to the switch in the OFF condition (V_G = +10 V), it is apparent that no problem will exist until the source-to-body or drain-body diode becomes forward-biased.

The CMOS Switch

As noted previously, the typical PMOS switch circuit will exhibit a variation in ON conductance as the analog voltage is varied. This undesirable characteristic can be overcome by paralleling P- and N-channel FETs, as shown in Figure 10A. For the ON state, the N-channel gate is forced positive and the P-channel gate is forced negative. Figure 10B shows the combined conductance of the two FET switches. The integrated combination of N-channel and P-channel devices on a common substrate is referred to as complementary MOS (CMOS).

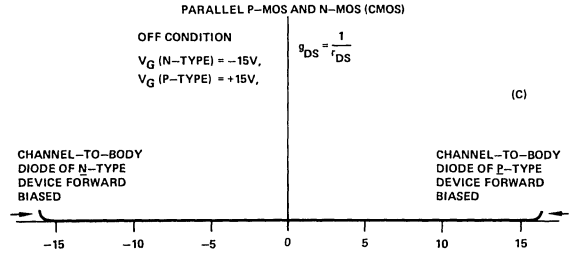


(A)



	P–MOS	N–MOS	
V_G	–15V	+15V	ON
V_G	+15V	–15V	OFF

(B)



(C)

Characteristics of CMOS Devices
Figure 10

CHAPTER 7

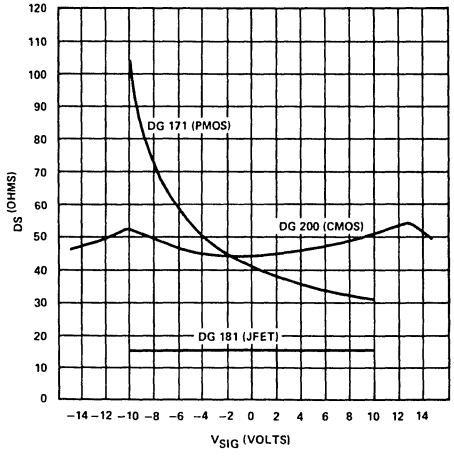
The OFF condition for the CMOS device will be maintained so long as the channel-to-body diodes do not become forward-biased, as shown in Figure 10C.

The major advantages the CMOS construction technique makes to analog switching are:

- Lower r_{DS} variation with analog signal characteristics, similar to the performance of a junction FET.
- Analog signal range extends to + and – supply voltages. For instance, using the same ±15 V supplies typical of operational amplifiers, the signal-handling capability of the system is limited by the op amp, *not by the switch.*

Summary of FET Switch Performance and Tradeoffs

Figure 11 compares the performance of three switch types with respect to $r_{DS(on)}$ vs V_{SIG}. If one examines the r_{DS} characteristics of the integrated switching circuits DG171 and DG181, there may be a tendency to dismiss the DG171 on the basis of its apparent inferior performance.

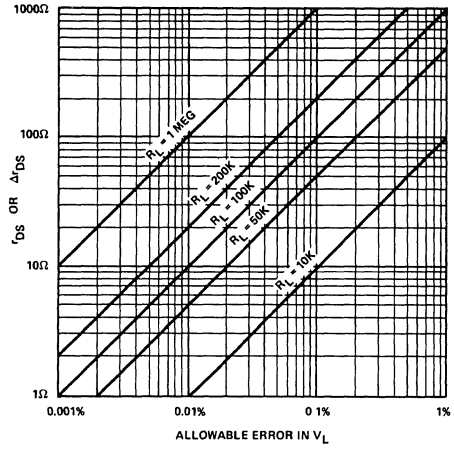


Performance of Three FET Switches
Figure 11

In reality, the comparison between the monolithic DG171 and the hybrid DG181 is not clear-cut. Initial circuit design considerations must determine what degree of error can be tolerated by the application in terms of Δr_{DS} and r_{DS}. Once this error factor has been determined, the designer should contact a switch manufacturer for applications assistance in selecting the best switch for his purpose, in terms of both r_{DS} *and* cost. From this viewpoint, the single-chip DG171 will perform creditably in applications where Δr_{DS} and r_{DS} error are not critical, and the device costs considerably less than the DG181.

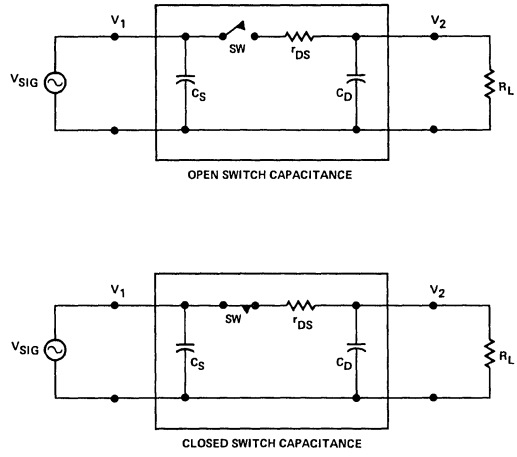
To amplify the preceding point, consider the definition of the tolerable level of Δr_{DS} and r_{DS}.

The curves in Figure 12 define the maximum r_{DS} (or Δr_{DS}) which can exist for a given allowable error percentage with a fixed value of R_L. Recall that in the circuit in Figure 3, a resistive load of 200K Ω was assumed. If it is also assumed that an error level of 0.1% is tolerable, then r_{DS} = 200 Ω is the maximum allowable switch resistance. On the other hand, if settling time is not critical, then an R_L of 1 megohm, yielding r_{DS} = 1K Ω is permissible.



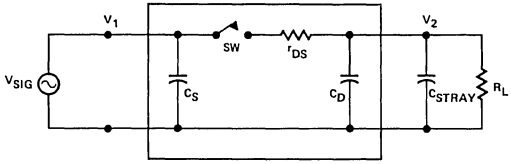
Tolerable Level of Δr_{DS} and r_{DS}
Figure 12

In situations where settling time is indeed a design consideration, the circuits in Figure 13 will provide an overview of the exact nature of settling time for V_2 (=V_L) at turn-OFF and turn-ON. For a turn-ON signal, C_L charges through r_{DS}. During turn-OFF, C_L discharges through R_L. For a system error level of 0.1%, R_L = 1000 r_{DS}; therefore, the maximum settling time for V_2 occurs during turn-OFF.

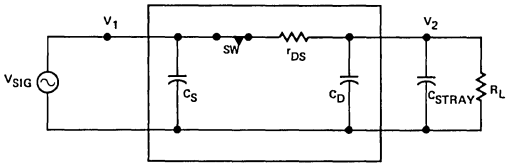


Switch Settling Time Equivalent Circuits
Figure 13

(Cont'd)



OPEN SWITCH CONTAINING STRAY CAPACITANCE
$C_L = C_D + C_{STRAY}$



CLOSED SWITCH CONTAINING STRAY CAPACITANCE

Switch Settling Time Equivalent Circuits
Figure 13

Consider a switch with $C_S = C_D = 3$ pF, for an application requiring 0.1% accuracy with 5 μsec settling time. A typical stray capacitance (C_{IN} for an op amp) may be 6 to 7 pF. Therefore, $C_L = 3$ pF + 7 pF = 10 pF. Resistance loads, R_L, of 100K Ω, 50K Ω, and 25K Ω are considered for the switch. The time required for an RC system to settle to within 0.1% of its final value is 6.9 time constants (6.9 RC). Table I shows the R_L and r_{DS} values necessary to satisfy a number of settling time specifications. From Table I, it is apparent that so long as $R_L \leqslant 72K\ \Omega$, the desired settling time of 5 μsec will be achieved.

TABLE I

R_L (Ω)	r_{DS} (Ω)	C_L (pF)	t_{ON} (V_2)** (0.1% settling time) (nsec)	t_{OFF} (V_2)** (0.1% settling time) (μsec)
25K	25	10	1.72	1.72
50K	50	10	3.45	3.45
*72K	72	10	5.00	5.00
100K	100	10	6.90	6.90

*Maximum R_L for $t_{set} = 5$ μsec

**Does not include delay times

If cost is a design constraint, it is wise to make a close analysis of actual system switch requirements. Too often, designers buy unnecessary performance capability. In Table I, the switch with $r_{DS} = 25\ \Omega$ costs nearly twice as much as does the switch with $r_{DS} = 50\ \Omega$, yet either switch will meet the 5 μsec settling time specification.

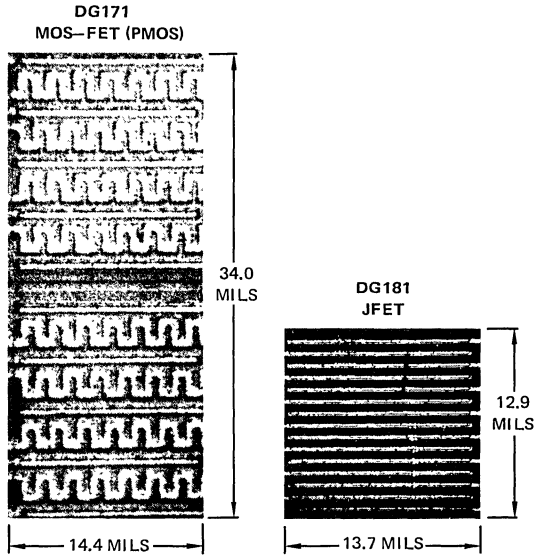
Switch Capacitance

In general, the lower the switch capacitance the better the switching time and high-frequency isolation performance. The subjects of switching time and high-frequency isolation are covered in other Application Notes in this series.

The simplified representation of switch capacitance shown in Figure 13 can be used to provide a very good estimate of what problems (if any) will be caused by switch capacitance in a given application.

In general, capacitance is proportional to the active area in a FET chip, prior to bonding onto a header. Additional stray capacitances are introduced when the leads are brought out through the device package. Thus, as lower r_{DS} (higher g_{DS}) is required, the active area is generally increased to obtain that parameter. The increase in area leads to an increase in capacitance.

The foregoing statements are true so long as one is dealing with a given device type. However, in transition from a JFET to a PMOS device, a significant difference will be observed in the active areas required for a given r_{DS}. Figure 14 compares the area of a JFET (from the hybrid DG181 circuit) and the monolithic PMOS circuit of the DG171. Note that the r_{DS} for the JFET is approximately one-third that of the PMOS device, while the active PMOS area is almost three times greater than that of the JFET. Yet the ratio of PMOS-to-JFET capacitance is almost 2:1.



Active Area Comparison of PMOS and JFET Switches
Figure 14

CHAPTER 7

Switch Comparison

A comparison between the characteristics of the three types of JFET switches is made in Table II.

This Application Note has surveyed the characteristics of FET switches and their associated drivers. In considering the FET as an analog switch, discussion has largely centered on the devices themselves, including specific load problems and applicable driver circuits. Total switch performance is a function of the switch *and* the switch driver. Typically, high-performance switch drivers require numerous switching transistors. When discrete devices are considered, the total parts count will be high and the cost will be prohibitive. From the standpoint of cost, improved performance, and smaller size, the integrated circuit FET switch and driver is often the superior choice.

TABLE II

Switch Type	Analog Signal Range	r_{DS}	Δr_{DS}	Leakage, I_D or I_S
PMOS	$(V_- - V_{GS(th)}) < V_{SIG}$*	High	High	Low
JFET	$(V_- - V_{GS(off)}) < V_{SIG}$*	Low	Low	Low
CMOS	$V_- \leqslant V_{SIG} \leqslant V_+$	Medium	Medium	Low

*Both $V_{GS(th)}$ (for PMOS) and $V_{GS(off)}$ (for N-channel JFET) are *negative* voltages.
V_+ is defined as positive supply voltage.
V_- is defined as negative supply voltage.

7.2 I.C. Multiplexer Increases Analog Switching Speeds (AN73-2)

J. O. M. Jenkins
Revised April 1976

INTRODUCTION

A two-level IC multiplexing system, that has significant advantages over conventional single-level systems, can improve effective switching speeds of analog systems by approximately one order of magnitude.

Analog multiplexing is the simultaneous transmission of two or more analog signals on to a single transmission line. Time-division multiplexing is widely used, each analog input being sampled sequentially and conveyed into a common output line. The signals can be transmitted directly in their analog form or they can be digitally coded by means of A/D converters and then transmitted. The latter method is used in applications requiring a very high degree of transmission accuracy.

In a system having 'n' analog inputs, a multiplexing/demultiplexing system will generally require 1/n of the total transmitting and receiving circuitry of a nonmultiplexed system. Hence, system cost is reduced drastically in the former case.

Present-day requirements for analog multiplexers have necessitated the development of special circuits. These incorporate multichannel FET multiplexers which are now available in integrated-circuit form, and which possess numerous advantages over their discrete counterparts:

(1) The use of IC's introduces a higher degree of circuit reliability;

(2) Switch for switch, IC's are much more compact;

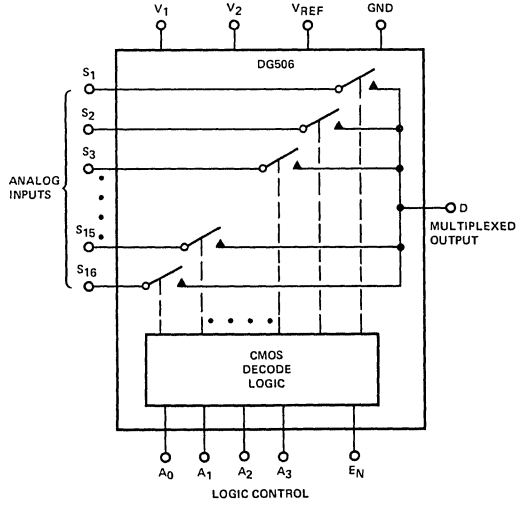
(3) System layout cost is less;

(4) The cost per switch is approximately the same as for a discrete FET switch.

Single-Level Multiplexing System

Fast IC multiplexers, having rapid open and close switch times, are required in many applications in which rapid sampling of analog signals is required. In any application in which it is necessary to sample analog signals and convey them at maximum transmission rates, the ratio of t_1:t_2 must be as small as possible (where t_1 represents the time between samples and t_2 the sample duration time).

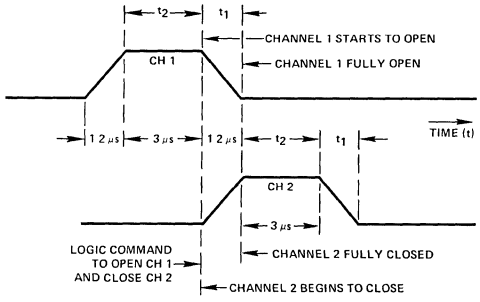
Applications requiring microsecond sample times clearly present considerable difficulty, because IC multiplexers which are commercially available have t_{ON} and t_{OFF} times in the region of 1-2 μs. When used in the conventional single-level mode, a substantial loss in transmission efficiency results. Figure 1 shows a simple single-level system for analog multiplexing.



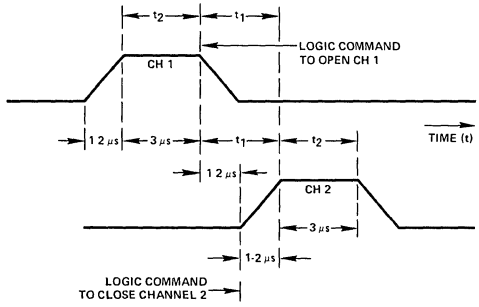
DG506 Used as a Single-Level Multiplex System
Figure 1

CHAPTER 7

With a single-level system one can obtain either (a) the waveforms shown in Figure 2(a), and be faced with inter-channel interference due to overlapping samples or, (b) the waveforms of Figure 2(b) which result in delayed channel switching, in order to eliminate interference between channels.



Overlapping Channels
Figure 2(a)



Delayed Channel Switching
Figure 2(b)

If the analog sample time needed is 3 µs, for example, system 2(a) would not be a practical proposition. System 2(b) would certainly be practical but would introduce a large wastage of transmission time due to the large ratio of t_1:t_2 (Figure 2(b), in fact, indicates a 50% loss in transmission efficiency).

This problem is manifest in all commercially available IC multiplexers used in single-level systems. Other problems that result from using a single-level system are:

(1) With a large number of separate analog inputs, the leakage currents through the OFF switches can introduce an appreciable percentage voltage error into the common output line. This is important if the analog signal being conveyed through the closed switch is in the millivolt range.

(2) The common node output capacitance increases with the total number of analog channels being multiplexed. With 64 channels (i.e., 4 x 16 channel DG506), the common node output capacitance will be typically 160 pF.

The charging time (t_1) necessary for the analog signal to reach 0.25% of its final value (six time constants) will then be approximately

$$6 \times C_{OUT} (R_{ds(on)} + R_{ANALOG\ SOURCE}) \quad (1)$$

If the source resistance is 1K Ω, t_1 will be

$$6 \times (160 \times 10^{-12}\text{pF}) \times (400\ \Omega + 1\text{K}\ \Omega) = 1.35\ \mu\text{sec} \quad (2)$$

This decreases the effective switching speed of the multiplexer.

Two-Level Multiplexing System

These problems can be overcome if a two-level multiplexer is used, which inherently provides a much faster switching system. Figure 3 shows an example of a two-level system capable of 32 channels. The first level consists of 16-channel DG506 multiplexers, the use of which offers the advantages stated in the introduction. The second level consists of two or more single channels of a DG181; this has switch open and close times of, typically, 100 ns, and has a break-before-make switching action. The DG181 is available as an integral dual-in-line package.

The two-level system uses the bank of high speed DG181 switches at the output to sequentially switch between the outputs of the DG506's. Each DG506 is able to switch channels during the time the others are being interrogated. It contributes capacitance and leakage at the output only when it is switched into the output bus by a DG181.

The use of the two-level system achieves the following:

(1) Effectively reduces the common output node capacitance of the system. It will consist of a single multiplexer output, DG506 (40 pF) and several DG181's (6 pF OFF, 15 pF ON). For a 64-channel 2-level system, for example, the output capacitance is reduced to 72 pF, compared to 160 pF of the single-level system.

(2) Reduces the amount of error voltage developed as a result of leakage current flow through the OFF switches into the common output node. The leakage through the OFF switch of Figure 3 into the common output node is effectively that of a single OFF channel of the DG181 (from ±40 nA to ±10 nA in a 64-channel system).

(3) Allows the system to operate in such a way that the ratio t_1:t_2 is very small. In the example, t_1 = 200 ns and t_2 = 3µsec.

The switching speed of the system is dependent on the DG181, which is a high-speed 2-channel SPST ($t_{ON} \approx 100$ nsec). The slower switching time of the DG506 (≈ 1 µsec) is not important because this switching transition can take place while the other DG506's are being interrogated.

With the two-level system design, more data can be transmitted with a very fast multiplex system utilizing a large number of low-cost, moderate-speed multi-channel multiplexers and several high-speed SPST switches.

Details of the System

A 32-channel two-level multiplexing system is shown in Figure 3. Figure 4 shows the analog switching waveforms, including the segments of the multiplexer outputs being sampled. Notice that as one multiplexer is being sampled, the other is switching. The example of the output samples shows the edge-to-edge sampling achieved by the two-level system. The logic timing diagram for the system of Figure 3 is shown in Figure 5. This illustrates the timing used by the DG181 switches to give the two-level multiplexing.

Logic Control System

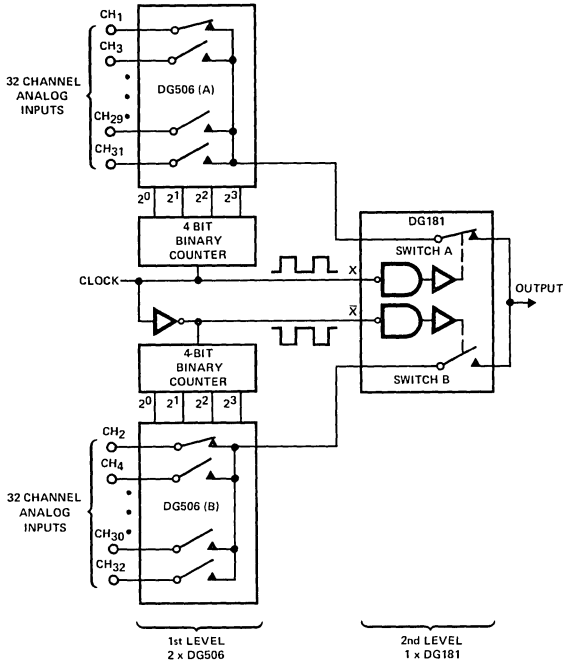
The digital control logic consists of a multi phase clock generator and recirculating binary counters. The number, N, of clock phases and binary counters necessary is equal to the number of multiplexers used in the first level of the system. With 16-channel DG506's, 4-bit binary counters are needed (such as TTL DM7493) to give addressing to all 16-channels.

64-Channel Two-Level Multiplexer

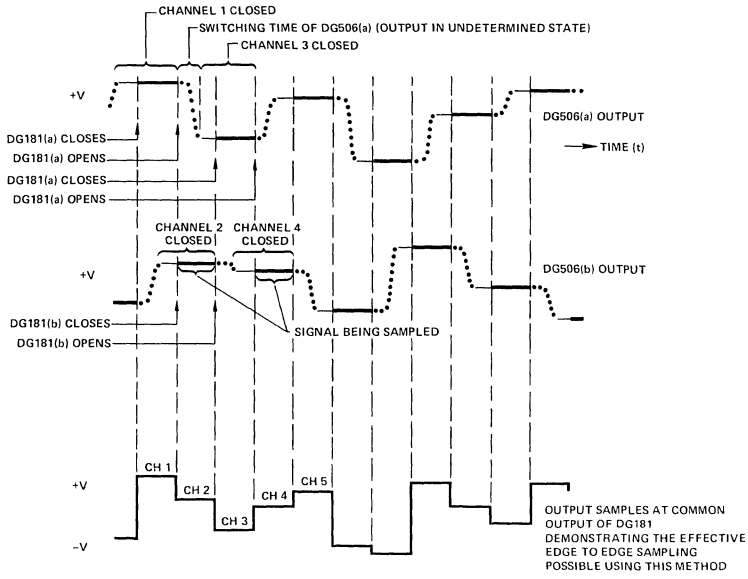
Figure 6 shows a complete 64-channel two-level multiplex system. For the 64-channel system, N = 4 and the four clock phases are generated with a two-bit counter and decoding logic (these four phases are also shown in Figure 6). Two J-K flip-flops (TTL DM7473) are connected as a two-bit counter and toggle on the high-to-low clock edge. The NAND gates (DM7400) decode the flip-flop outputs into the four clock phases shown. The low state of the clock phase is the ON state of the corresponding DG181 switch. As a clock phase goes from a low-to-high state, the DG181 it feeds turns off and the corresponding 4-bit binary counter (DM7493) is triggered to its next address state. This causes the multiplexer to change as the output of the next multiplexer is being sampled at the output. For synchronization there is a reset available to set the system to start on the first channel when power is first applied.

CONCLUSION

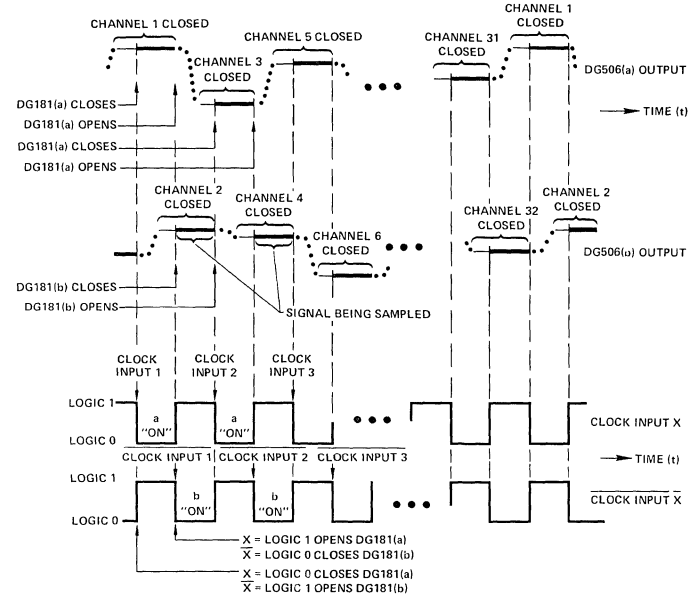
This system may be used for increasing data transmission rates in analog switching systems. One particular application is found in telephone switching where, for instance, it is necessary to multiplex 32 or more channels of analog information in the form of 4 μs samples (edge-to-edge) on to a common output line.



32 Channel, Two-Level Multiplex System, Comprising Two DG506's in the First Level, and a DG181 in the Second
Figure 3



Two-Phase Timing Method That Eliminates the Switching Delays of the 16-Channel Multiplexers in a 32-Channel System
Figure 4



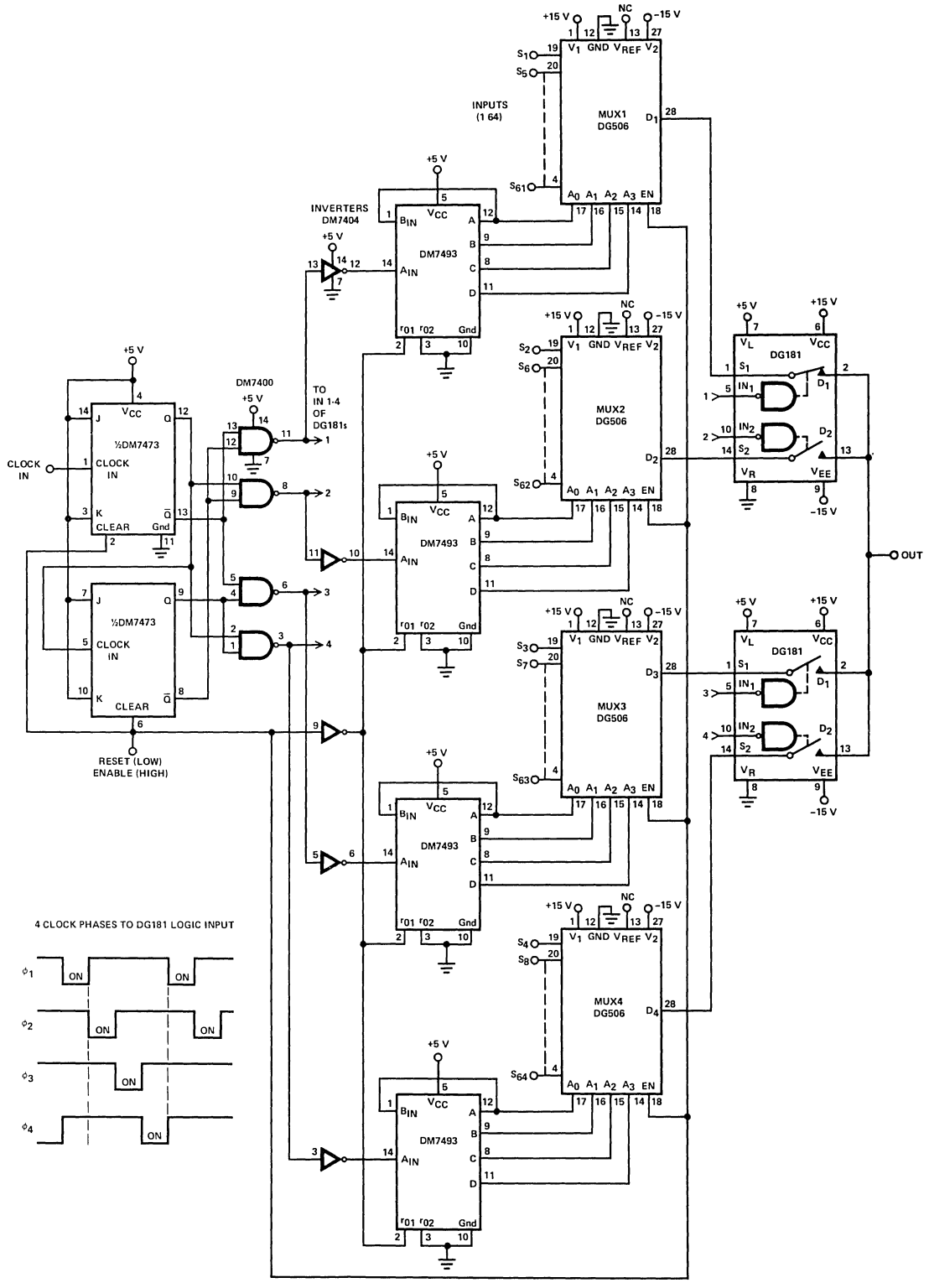
Output States of 4 Bit Counter

	2^3	2^2	2^1	2^0
Initial State	0	0	0	0
Clock Input 1	0	0	0	1
Clock Input 2	0	0	1	0
Clock Input 3	0	0	1	1
Clock Input 15	1	1	1	1
Clock Input 16	0	0	0	0

Clock or $\overline{\text{clock}}$ Inputs to 4 Bit Counters (Waveforms X, $\overline{X}$)

Recycling Count of 16

Logic Timing Diagram Showing Waveform Timing Sequences for a 32-Channel System
Figure 5



64-Channel 2-Level Multiplex System
Figure 6

CHAPTER 7

7.3 Switching High-Frequency Signals with FET Integrated Circuits (AN73-3)

Revised January 1976

INTRODUCTION

A number of available integrated circuits employing FET switches with their associated drivers can be used to switch high-frequency signals with greater convenience than other types of RF switches, such as PIN diodes or electromechanical devices. Wideband RF signals, to 100 MHz, can be switched with excellent OFF isolation and small ON insertion loss. FET analog switches also permit direct interface with 5 V computer logic, including TTL and CMOS. No external interface elements are required. FET analog switches have high reliability, long life, low power dissipation, and are quite small. Attractive DC properties of these devices include very low leakage, zero offset voltage, and large signal voltage ranges.

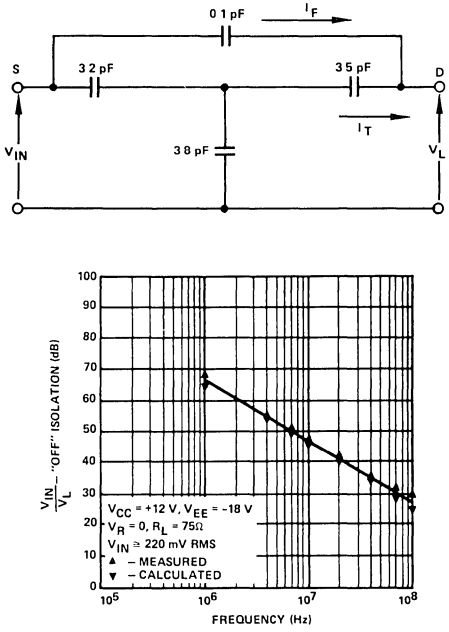
Effective RF switching concerns the control of RF signals, and not high-speed switch actuation. The point of major interest is switch RF performance in the static OFF and ON states. A number of standard FET analog switches can qualify as good RF switches; four specific types will be used as examples, since each type represents a different IC structure. Typical devices include the DG133, an N-channel junction FET switch with bipolar driver; DG171, a P-channel MOS FET switch with PMOS/bipolar driver; DG181, an N-channel junction FET switch with PMOS/bipolar driver; and the DG200, a monolithic CMOS switch with CMOS driver. However, the DG180-190 series and the DG200-201 take advantage of newer technologies and therefore have the best performance/cost tradeoff available.

Elements of OFF Isolation

Most RF applications involving high-frequency switching are frequency-limited due to reduction in OFF isolation, rather than to degradation in ON performance. Generally, the quality of OFF isolation depends on three factors: selection of the appropriate analog switch, the magnitude of load resistance, and the amount of external stray (wiring) capacitance present in the circuit. Usually two of these elements can be controlled by the circuit designer, i.e., switch selection and stray capacitance.

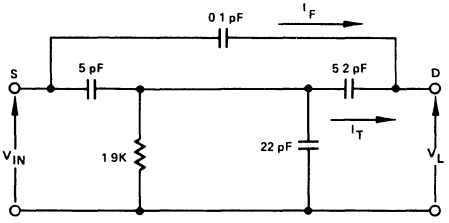
Probably the most important factor affecting OFF isolation is selection of the appropriate analog switch. As a rule, information available to the designer in the form of product specifications does not provide OFF isolation data in sufficient depth to make switch selection easy. There are three major actions which may be taken to overcome this lack of data. They include measurement of actual isolation performance (see footnote,* page 2); analysis of equivalent circuits to predict isolation (see Appendix); and simplification of the analysis to produce a useable set of design aids.

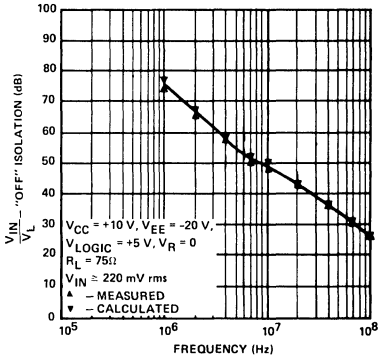
Measured data, calculated data, and equivalent circuits are presented in Figures 1 through 4.



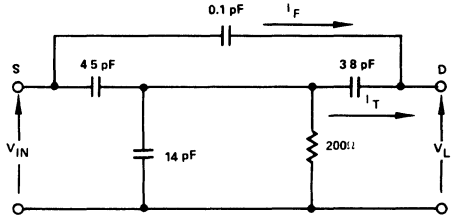
DG133 Equivalent Circuit and OFF Isolation Data
Figure 1

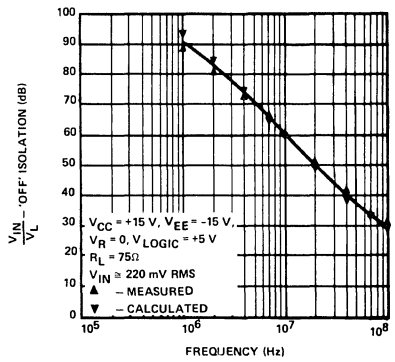
CHAPTER 7



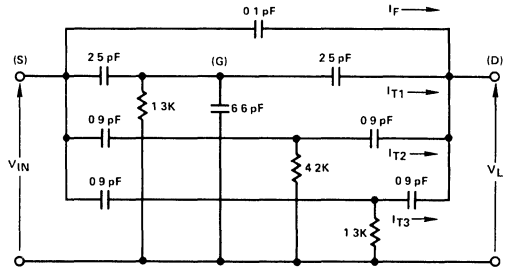


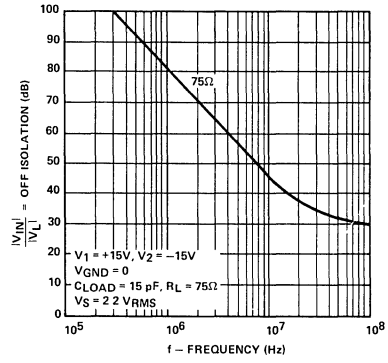
DG171 Equivalent Circuit and OFF Isolation Data
Figure 2



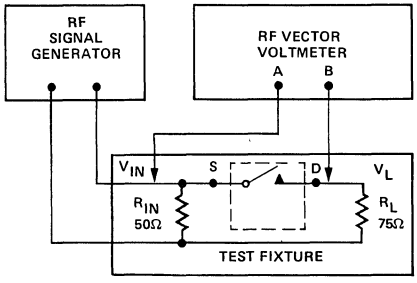


DG181 Equivalent Circuit and OFF Isolation Data
Figure 3





DG200 Equivalent Circuit and OFF Isolation Data
Figure 4



Isolation Test Circuit
Figure A

*Data was taken for each switch in a special test fixture (Figure A). In the test fixtures, inputs were shielded from outputs, and RF decoupling was provided on all DC connections. Great care was taken in the mechanical layout of fixtures, to minimize stray capacitance. The characteristic impedance of video transmission lines, 75 Ω, was issued as the value of load resistance. Voltage measurements were made with an RF vector voltmeter, H/P Model 8405A.

Plots of switch OFF isolation vs frequency performance are quite similar. OFF isolation reduces with increasing frequency at rates from 20 dB to 40 dB per decade. A small capacitance in series with R_L has a similar response, except that the OFF isolation reduces at a fixed rate of 20 dB per decade. If the equivalent circuit models of Figures 1 through 4 are replaced with a single capacitance, $|C_{Eq}|$, (which varies uniquely with frequency for each switch structure) the rather formidable equivalent circuits can be ignored. (See Appendix for discussion of $|C_{Eq}|$).

An additional capacitance path from input to output is through C_{STRAY}.

To show the magnitude of a potential source of capacitance, two parallel conducting strips were etched on a piece of 2-oz. copper-clad terminal board. The strips were 50 mils wide, with 100 mils center-to-center separation (which is essentially the same spacing as adjacent leads in a TO-116 dual in-line package). Measured strip to-strip capacitance was 0.9 pF per inch. It is obvious that stray capacitance is the direct result of circuit layout. Because of the dramatic influence of stray capacitance in OFF isolation, great care must be taken in the layout of PC boards in a circuit (see Appendix for example).

In Figure 5, a graphic design aid (derived from the simple $|C_{Eq}|$ model) is presented to simplify the analysis of OFF isolation in a variety of analog switches and resistive loads. Since C_{Eq} is dependent somewhat on R_L, this design aid is only approximate for $R_L > 150\ \Omega$.

In Figure 5, only those RF signals of a sinusoidal nature are considered. Certain other signals, such as video, may be more conveniently viewed as having a pulse characteristic. Thus Figure 5 is modified as Figure 6 to yield a design aid useful in making analyses of pulse isolation.

Crosstalk

Crosstalk is also of concern to the RF circuit designer. Crosstalk is basically channel-to-channel isolation, and may be analyzed with the tools presented in Figure 5 and 6. It occurs in either of two circuit configurations.

The first instance (Figure 7A) comes about when several switches are arranged in a circuit to feed a common load (or when one signal source is used to feed multiple loads). The total effect of crosstalk from Switch 1 to Switch 2 is found by summing I_L' (due to isolation parameter of Switch 1) with I_C (the capacitive coupling between Switch 1 and Switch 2). If C'_{STRAY} is small, then the crosstalk effect will be negligible. C'_{STRAY} must be minimized with the same care indicated for C_{STRAY}.

The second configuration (Figure 7B) includes loads which are independent of one another. In this case, the major coupling from Switch 1 to the output of Switch 2 is through C'_{STRAY}. In general, the crosstalk generated by the circuit in Figure 7B should be less than that which occurs in Figure 7A.

Actual RF Switching Application

How well does a high-performance RF switch work in an actual application? Figure 8 is a block diagram of a switching circuit which controls a video monitor. The video signal is switched ON and OFF by a DG190, a 2-channel SPDT member of the DG181 family. Then a 75 Ω attenuator was cycled between 0 dB and 40 dB. Results of the experiment are shown in Figures 9 through 13, with attenuation occuring at 0 dB, 20 dB, and 40 dB.

For an even more critical switch application, consider switching a monitor between two cameras in a high-resolution closed-circuit TV system. Each camera has a signal bandwidth of 32 MHz, and a signal-to-noise ratio of 30 dB. OFF isolation must be at least 36 dB to prevent more than 1 dB degradation of the system signal-to-noise ratio. The resistive load, R_L, is 75 Ω.

The technique for selection of the proper switch for such an application, using the graphic design aid presented in Figure 5, is as follows:

(1) From Figure 5A, required $R_L \times C_I$ is approximately 80 Ω – pF.

(2) Dividing by R_L, $C_{I(max)}$ is determined to be 1.06 pF.

(3) Planned C_{STRAY}, using careful board layout, is ≤ 0.2 pF. Thus $|C_{Eq}| \leq 1.06\ pF - 0.2\ pF = 0.86\ pF$.

(4) Transfer this value of $|C_{Eq}|$ to Figure 5B. It is apparent that the only available switch which will satisfy the maximum capacitance criteria is a DG181, with $|C_{Eq}| = 0.59$ pF.

(5) Having selected the DG181 as the proper switch, one now works backward on the design aid to predict an OFF isolation of 38 dB.

The example illustrated requires the best FET switch (DG181) and fairly small C_{STRAY}. If the same degree of OFF isolation is required with a larger R_L, or a higher operating frequency, multiple switches must be used.

Several multiple switch configurations may be used to achieve an impressive increase in OFF isolation under otherwise difficult conditions. The simplest multiple switch configuration is the shunted load, shown in Figure 14.

The load resistance, R_L, is shunted by a second switch, S_2, which operates out of phase with the primary switch, S_1. This has the effect of reducing R_L to r_{DS2}. Switch ON characteristics are not affected. This configuration should be used only when the load can be shunted without introducing unwanted side effects.

Probably the most effective multiple switch configuration is the tee, which is shown in Figure 15. In the tee, S_2 operates out of phase with S_1 and S_3, and provides two stages of isolation. The input to S_3 is the isolation leakage of S_1 working into an $R_L = r_{DS2}$. This multiple switch arrangement can bring about a considerable degree of OFF isolation, but only at the expense of doubling switch ON resistance, which increases the ON insertion loss.

HOW TO USE:

(1) Find required OFF isolation[1] at required frequency on Figure 5A

(2) Find $R_L \times C_I$ on vertical axis of 5A

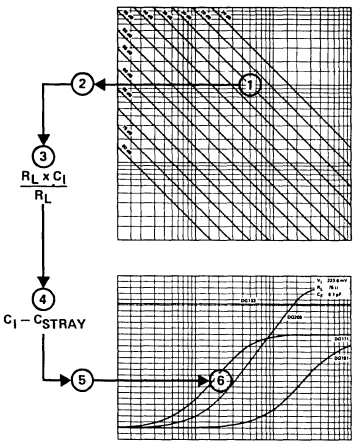
(3) Divide $R_L \times C_I$ by R_L to obtain C_I

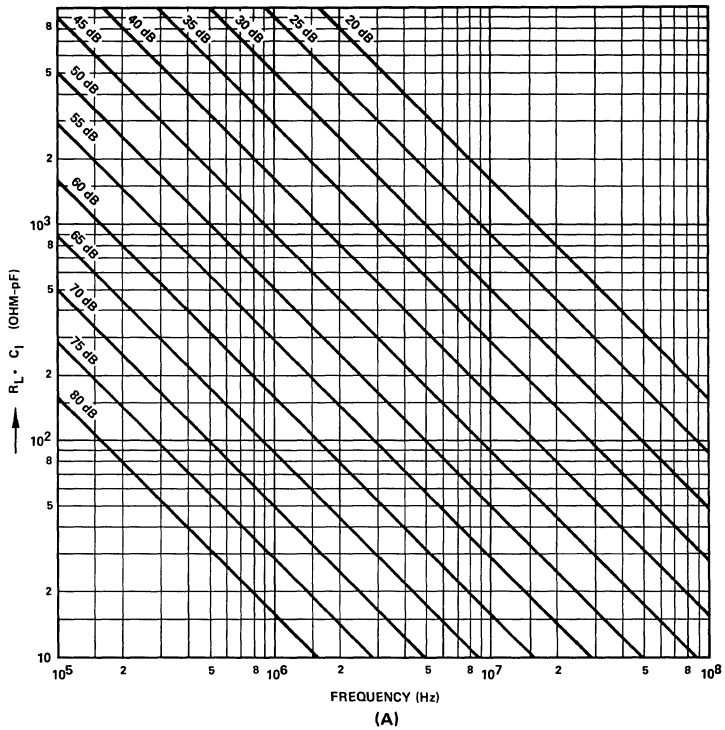
(4) Subtract C_{STRAY} from C_I to obtain $|C_{Eq}|$

(5) Find $|C_{Eq}|$ on vertical axis of Figure 5B

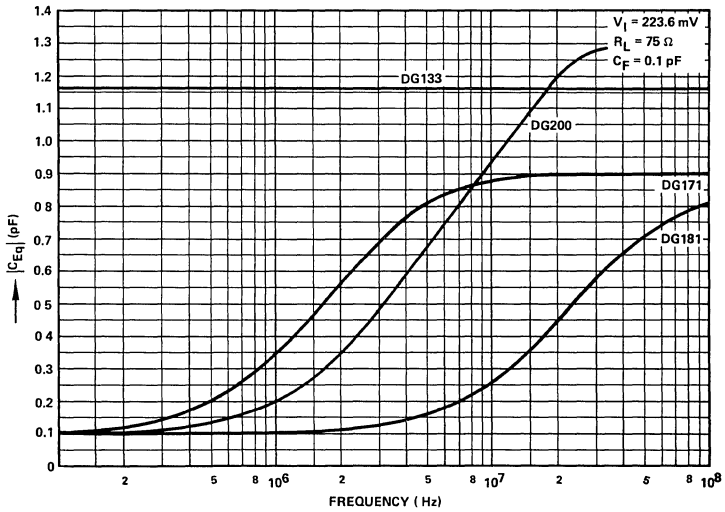
(6) Locate intersection of $|C_{Eq}|$ with required frequency on 5B

(7) Select switch below or to the right of intersection of $|C_{Eq}|$ and f on 5B. If no switch is shown, multiple switches must be used.





(A)



(B)

NOTES:

1. OFF ISO = 20 log $\frac{V_{IN}}{V_L}$

2. V_{IN} is voltage at switch input terminals

Isolation Design Aid (Sinusoidal Signals)
Figure 5

HOW TO USE:

(1) Determine $\frac{\Delta V}{\Delta T}$[(1)] of input pulse

(2) Find required maximum peak pulse output at $\frac{\Delta V}{\Delta T}$ on Figure 6A.

(3) Find $R_L \times C_I$ on vertical axis of 6A.

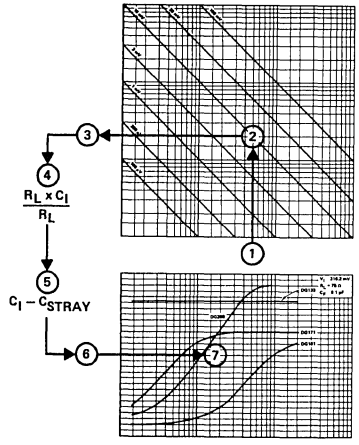
(4) Divide $R_L \times C_I$ by R_L to obtain C_I

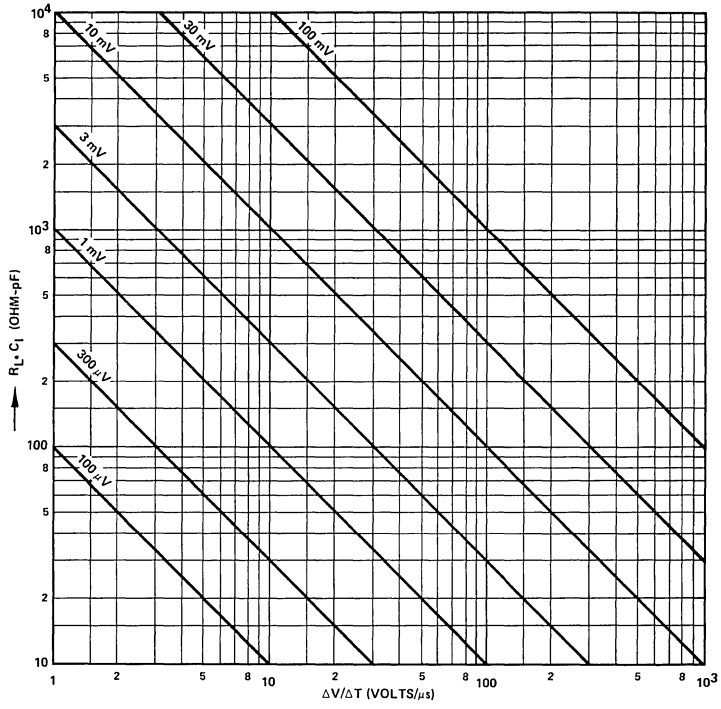
(5) Subtract C_{STRAY} from C_I to obtain $|C_{Eq}|$

(6) Find $|C_{Eq}|$ on vertical axis of Figure 6B

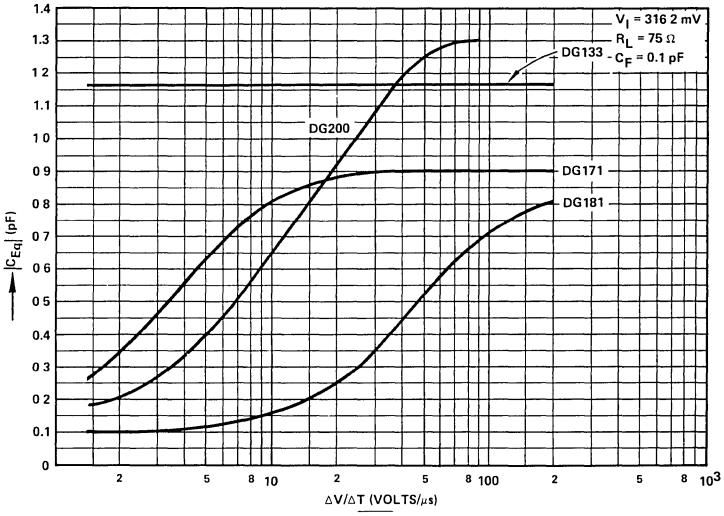
(7) Locate intersection of $|C_{Eq}|$ and $\frac{\Delta V}{\Delta T}$ on 6B

(8) Select switch below or to right of intersection on 6B. If no switch is shown, multiple switches must be used





(A)

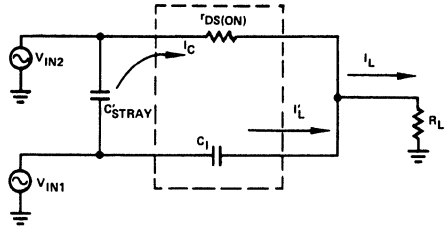


(B)

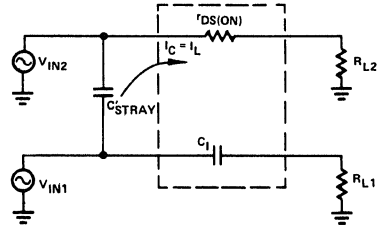
NOTE:

1. $\frac{\Delta V}{\Delta T} = \frac{V_{PEAK}}{\Delta T}$

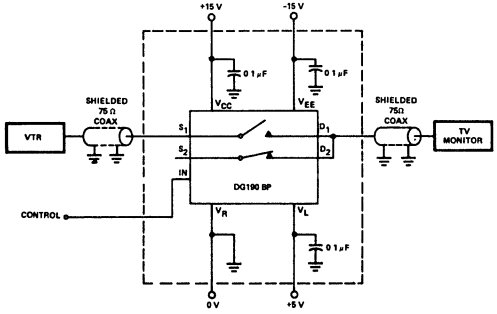
Isolation Design Aid (Pulse Signals)
Figure 6



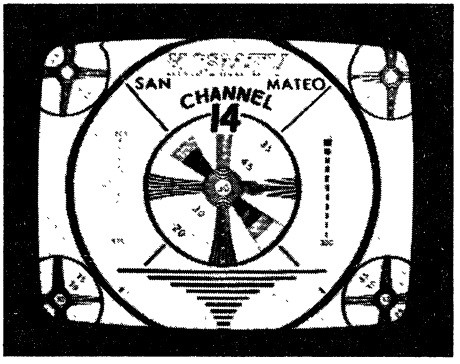
Crosstalk with a Common Load
Figure 7A



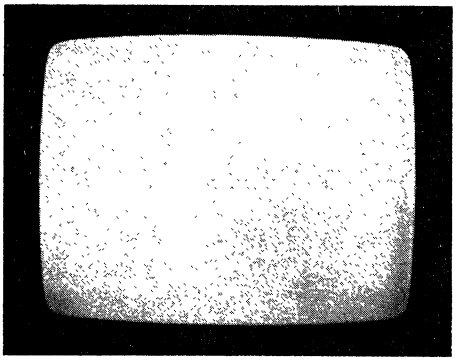
Crosstalk with Independent Loads
Figure 7B



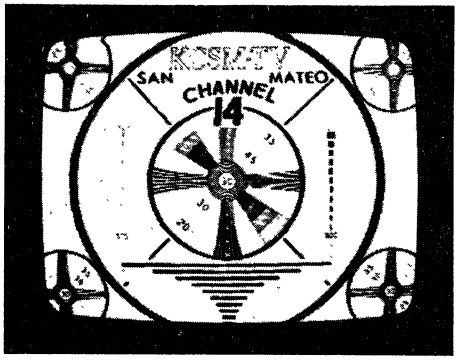
Video Switch Block Diagram
Figure 8



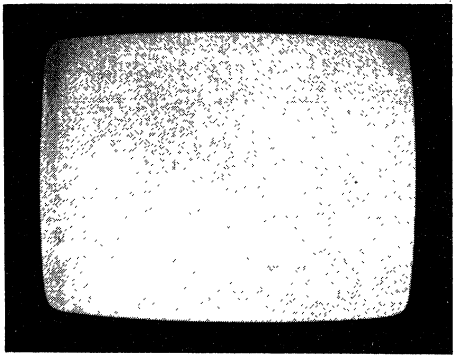
Switch ON
Figure 9



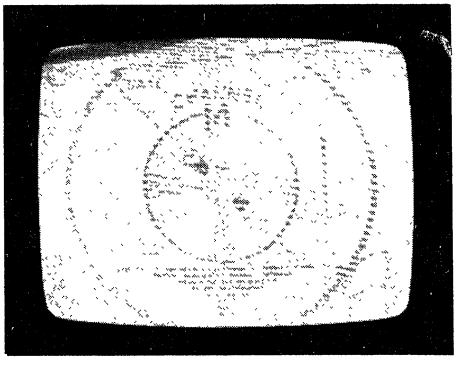
Switch OFF
Figure 10



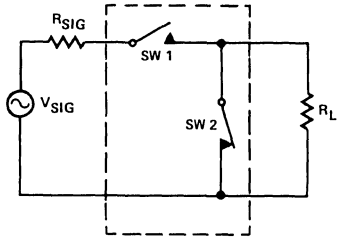
Attenuation = 0 dB
Figure 11



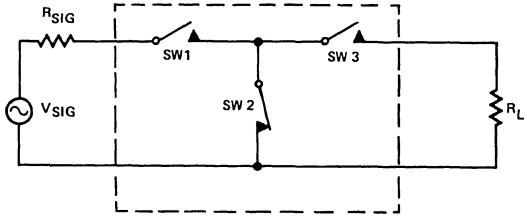
Attenuation = 40 dB
Figure 12



Attenuation = 20 dB
Figure 13

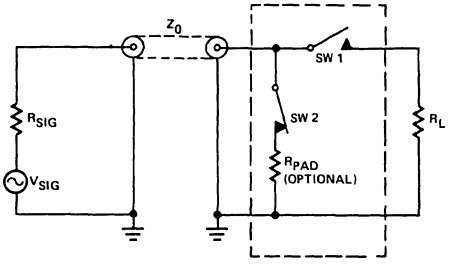


Shunted Load for Isolation Improvement
Figure 14



TEE for Isolation Improvement
Figure 15

A third multiple switch arrangement may be used to improve OFF isolation if the input signal is presented to the switch via a transmission line. The input impedance of an OFF switch is essentially infinite. The result of this condition is a reflection coefficient of 1, which means that the switch input voltage is twice as large as the voltage at the signal source. This switch configuration is shown in Figure 16, where the additional switch, S_2, operates out of phase with the primary switch, S_1, to terminate the transmission line.



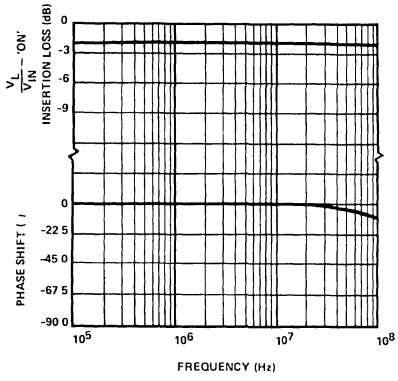
Transmission Line Isolation Improvement
Figure 16

A padding resistor, R_{PAD}, can be used to assist in matching the characteristic transmission line impedance Z_O. The value of R_{PAD} can be determined from the term $Z_O \cong r_{DS2} + R_{PAD}$. Note that the reflection coefficient is now nearly zero, and thus the switch input voltage is approximately equal to V_{SIG}.

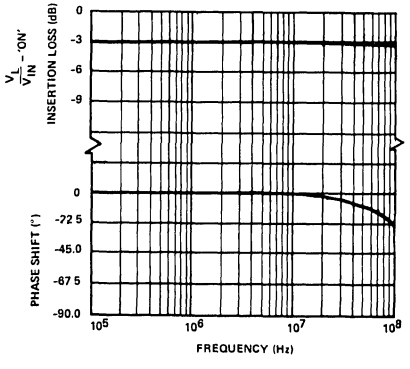
"ON" Switch Characteristics

Behavior of the switch in the ON condition is simple. ON performance is essentially independent of frequency for any load capacitance likely to be used. The ON resistance, $r_{DS(on)}$, causes an insertion loss which is basically constant; phase shift is negligible.

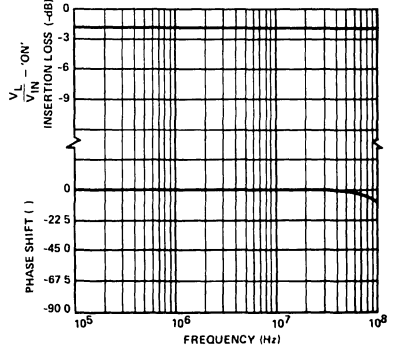
With the test fixture described in Figure A, measured ON performance was observed as shown in Figures 17 through 20.



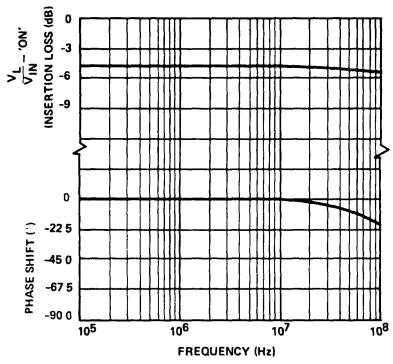
DG133 ON Performance
Figure 17



DG171 ON Performance
Figure 18



DG181 ON Performance
Figure 19



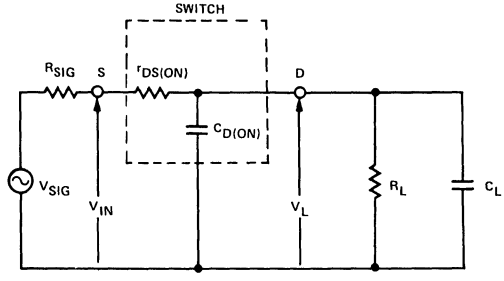
DG200 ON Performance
Figure 20

The ON state equivalent circuit for any of the four switches discussed in this Application Note is a series resistance, shunt capacitance ($r_{DS(on)}$, $C_{D(on)}$) model, as shown in Figure 21. The range of element values for each is given in Table I.

Table I

Value of Equivalent Circuit Elements

Switch Type	$r_{DS(on)}$ (Ω)	$C_{D(on)}$ (pF)
DG133	15-25	4-6
DG171	25-35	30-40
DG181	15-25	10-14
DG200	45-60	18-24



ON Equivalent Circuit
Figure 21

The transfer function for the ON switch is

$$\frac{V_L}{V_{IN}} = \frac{\dfrac{R_L}{R_L + r_{DS(on)}}}{1 + j f \left\{ 2\pi \left[\dfrac{R_L \; r_{DS(on)}}{R_L + r_{DS(on)}} \right] \left[C_{D(on)} + C_L \right] \right\}} \quad (1)$$

Insertion loss is computed from the numerator as

$$\text{ON insertion loss, dB} = 20 \log_{10} \frac{R_L}{R_L + r_{DS(on)}} \quad (2)$$

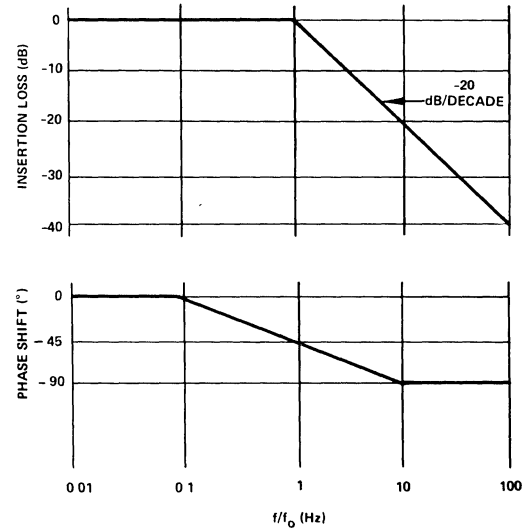
Table II lists the insertion loss, OFF isolation, and ON/OFF ratio for each switch, over a range of load resistance.

Table II

Switch Performance Summary

Switch	$r_{DS(on)}$ (Ω)	R_L (Ω)	Insertion Loss (dB)	OFF Isolation (dB) f = 10 MHz C_{STRAY} = 0.1 pF	ON/OFF (dB)
DG133	25	100	2.0	42.7	40.7
		75	2.5	45.2	42.7
		50	3.6	48.7	45.1
DG171	35	100	2.6	45.2	42.6
		75	3.3	47.7	44.4
		50	4.6	51.2	46.6
DG181	25	100	2.0	55.9	53.9
		75	2.5	58.4	55.9
		50	3.6	61.9	58.3
DG200	60	100	4.1	43.8	39.7
		75	5.1	46.3	41.2
		50	6.8	49.8	43.0

The frequency response of the ON transfer function has the normalized form shown in Figure 22.



ON Frequency Response
Figure 22

Computing the minimum break frequency, f_o, for each switch discussed reveals that the DG171 has the lowest f_o, 133 MHz. Table III lists $f_{o(min)}$ for each switch.

Larger R_L will decrease f_o only slightly, while larger C_L will decrease f_o considerably. However, 10 pF is a fairly liberal load capacitance.

Table III
Minimum Break Frequency

Switch Type	$f_{o(min)}$ (MHz)	$r_{DS(on)}$ (Ω)	Values Used $C_{D(on)}$ (pF)	Values Used R_L (Ω)	C_L (pF)
DG133	530	25	6	75	10
DG171	133	35	40	75	10
DG181	354	25	14	75	10
DG200	140	60	24	75	10

CONCLUSIONS

Comparison of the OFF and ON performance of the four switches discussed shows that a tradeoff exists involving the load resistance, R_L. If R_L is decreased, isolation improves, but there is an attendant increase in insertion loss. The best compromise (greatest ON/OFF ratio) is with small R_L (see last column of Table II). Insertion loss of 2 to 5 dB indicates that the FET switches are probably not suitable for applications which require minimum signal loss as a primary design criteria.

FET analog switches – especially those in the DG181/DG191 family – have excellent RF switching capability. Any of the switches considered will satisfy the great majority of video requirements. FET integrated circuit analog switches offer simplicity and convenience in circuit design.

APPENDIX – Analysis of OFF Isolation

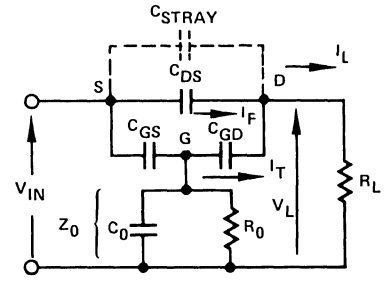
Switch Performance Ranking

OFF isolation data taken at 10 MHz establishes the following order of performance for the four switches discussed in this presentation:

DG181 (JFET)
DG171 (PMOS)
DG200 (CMOS)
DG133 (JFET)

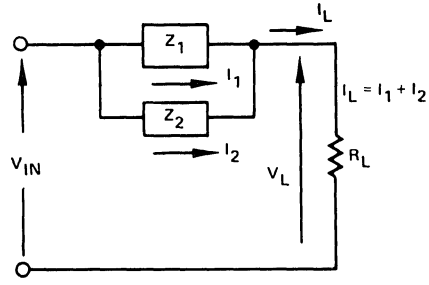
It is somewhat surprising that the best performer and the poorest performer are both junction FET analog switches; however, analysis of their equivalent circuits will provide an explanation for the performance differences. A general equivalent circuit for a JFET switch is shown in Figure 23.

In Figure 23, two separate paths exist between source (S) and drain (D). They are (1), the path through C_{DS} and C_{STRAY}, and (2) the path which passes through the gate circuit on its way to the drain. For full understanding of the circuit it must be assumed that I_F (current through C_{DS}) and I_T (the current flowing out of the tee network) are independent of one another.



JFET Equivalent Circuit
Figure 23

While in fact this assumption is not entirely valid, in those cases where OFF isolation is greater than or equal to 20 dB ($V_{IN} = 10\ V_L$) it yields excellent agreement with measured results. Before considering the transfer functions of I_F and I_T, it will be helpful to analyze the errors caused by the assumption that I_F and I_T may be derived independently. Figure 24 may be used to analyze the magnitude of error as $V_{IN}/V_L = 10$ (20 dB) is reached.



Error Analysis Equivalent Circuit
Figure 24

The *exact solutions* to I_1 and I_2 are given by

$$I_1 = \frac{V_{IN}}{Z_1} \cdot \frac{1}{1 + \frac{R_L}{Z_1} + \frac{R_L}{Z_2}} \qquad (1)$$

and

$$I_2 = \frac{V_{IN}}{Z_2} \cdot \frac{1}{1 + \frac{R_L}{Z_1} + \frac{R_L}{Z_2}} \qquad (2)$$

The *approximate solutions* for I_1 and I_2 are given by

$$I_1 \cong \frac{V_{IN}}{Z_1} \cdot \frac{1}{1 + \frac{R_L}{Z_1}} \qquad (3)$$

and

$$I_2 \cong \frac{V_{IN}}{Z_2} \cdot \frac{1}{1 + \frac{R_L}{Z_2}} \quad (4)$$

The approximation is valid when both Z_1 and $Z_2 >> R_L$. For a given value of I_L/V_{IN} the error is maximum when $I_1 = I_2$. From Equations (1) and (2) one can conclude that the condition $I_1 = I_2$ implies that $Z_1 = Z_2$. Thus the exact solution for I_L becomes

$$I_L = 2I_1 = \frac{V_{IN}}{Z_1} \cdot \frac{2}{1 + \frac{2R_L}{Z_1}} \quad (5)$$

and solving for V_L/V_{IN} (since $V_L = I_L R_L$),

$$\frac{V_L}{V_{IN}} = \frac{R_L}{Z_1} \cdot \frac{2}{1 + \frac{2R_L}{Z_1}} \quad (6)$$

when $V_{IN}/V_L = 10$ (in equation 6), then $R_L/Z_1 = 1/18$.

Referring to Equations (3) and (4),

$$I_L \cong \frac{V_{IN}}{Z_1} \cdot \frac{2}{1 + \frac{R_L}{Z_1}} \quad (7)$$

and

$$\frac{V_L}{V_{IN}} \cong \frac{R_L}{Z_1} \cdot \frac{2}{1 + \frac{R_L}{Z_1}} \quad (8)$$

Thus, when $R_L/Z_1 = 1/18$, Equation (8) yields $V_L/V_{IN} = 1/9.5$ ($V_{IN}/V_L = 9.5$). In other words, when V_{IN}/V_L is equal to 10, the approximate solution yields only 5% error.

Since the circuit in Figure 23 is used to describe isolations greater than 20 dB ($V_{IN}/V_L = 10$), the results thus obtained are valid quantitatively while retaining physical insight. The transfer functions for I_F and I_T are given in Equations (9) and (10):

$$I_F = \frac{j\omega C_{DS} R_L}{1 + j\omega C_{DS} R_L} \quad (9)$$

and

$$I_T = \frac{j\omega C_{GS} V_{IN}}{1 + \frac{R_L}{R_O} + \frac{C_{GS} + C_O}{C_{GD}} + j\frac{R_L}{R_O}\left\{\omega R_O (C_{GS} + C_O) - \frac{1}{\omega R_L C_{GD}}\right\}} \quad (10)$$

R_O and C_O are the output resistance and capacitance of the FET driver circuit. An inspection of Equation (10) will show that as $R_O \rightarrow 0, I_T \rightarrow 0$. This is desirable since an ideal switch allows zero current to flow when the switch is open (off). It is thus possible to reduce R_O and make I_T an arbitrarily small value; however, I_F remains to be dealt with. Actually, I_F is the *sum* of the currents through C_{DS} (device capacitance) and C_{STRAY} (additional wiring capacitance, etc.); moreover, I_F may be the dominant current at certain frequencies. Table IV shows that I_F is dominant at 1 MHz and I_T is dominant at 100 MHz.

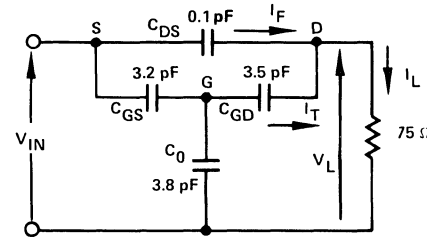
Table IV

Variations in Current with Frequency for DG181

f (MHz)	I_F	I_T	I_L	$\lvert V_{IN}/V_L \rvert$ (dB)	$\lvert C_{Eq} \rvert$ (pF)
1.0	141 ∠90° nA	30.3 ∠178° nA	145 ∠102° nA	+86	0.103
4.0	563 ∠90° nA	481 ∠173° nA	784 ∠128° nA	+72	0.139
10.0	1.41 ∠90° μA	2.91 ∠163° μA	3.58 ∠141° μA	+58	0.254
40.0	5.63 ∠90° μA	31.9 ∠128° μA	36.5 ∠123° μA	+38	0.648
100.0	14.1 ∠90° μA	99.6 ∠101° μA	113 ∠100° μA	+28	0.803
V_L = 224 mV	R_L = 75 Ω	C_{DS} = 0.1 pF	C_{STRAY} = 0		

NOTE The equivalent circuit shown in Figure 26 was used to calculate the results shown in Table IV.

The separate expressions derived for I_F and I_T make it relatively simple to evaluate the effect of varying certain parameters to minimize I_L (maximize isolation).



f = 10 MHz; V_1 = 224 mV

$I_F = 1.41 \angle 90°$ μA

$I_T = 13.3 \angle 90°$ μA

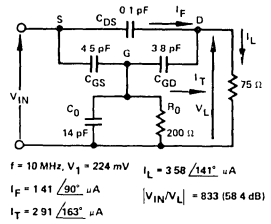
$I_L = 14.7 \angle 90°$ μA

$|V_{IN}/V_L| = 204$ (46.2 dB)

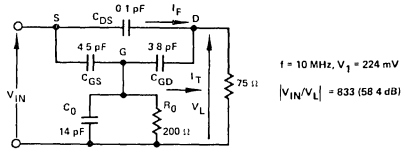
DG133 OFF Isolation
Figure 25

The isolation characteristics shown in Figures 25 and 26 dramatically illustrate the effect that variations of Z_O can have on OFF isolation. Note that C_{DS}, C_{GS}, and C_{GD} are approximately equal for both the DG133 and the DG181; however, Z_O of the DG181 is significantly lower than that of the DG133. The result is an improvement of 12 dB in OFF isolation at 10 MHz.

Figure 27 shows the effect of varying R_O between 200 Ω (the output resistance of the DG181 driver) and 0 Ω. Note that the DG181 is only 8 dB lower in OFF isolation than is



DG181 OFF Isolation
Figure 26



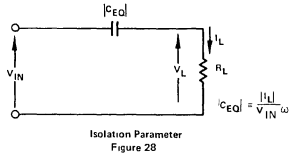
R_O	I_F	I_T	I_L	$\lvert V_{IN}/V_L \rvert$ (dB)
0	1.41 ∠90°μA	0	1.41 ∠90°μA	66.5
200	1.41 ∠90°μA	2.91 ∠163°μA	3.58 ∠141°μA	58.4

Comparison of Ideal Driver Case (I_T = 0) with Actual Performance of DG181 Analog Switch
Figure 27

the case with an ideal switch. This represents an excellent tradeoff, since R_O = 0 Ω would increase the power required by the analog switch.

Isolation Parameter

From a design viewpoint, analysis of the circuit shown in Figure 23 does not permit an easy comparison of different types of analog switches. In addition, the designer must be aware that the switch OFF isolation will degrade because of stray capacitance *outside* the body of the switch. Thus it becomes necessary to define an isolation parameter, as shown in Figure 28.



Isolation Parameter
Figure 28

The magnitude sign is used in Figure 28 because the OFF isolation parameter has the dimensions of capacitance; however, the phase shift through the circuit is not necessarily 90° (see I_L vs frequency in Table IV). The phase shift through the network is unimportant for this discussion, because consideration centers on the feedthrough signal being *less than* some allowable magnitude. Equation (11) defines the *total* isolation parameter, C_1, as

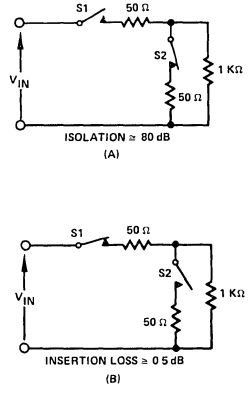
$$C_I = C_{STRAY} + |C_{Eq}| \qquad (11)$$

where C_{STRAY} = total stray capacitance *external* to the analog switch itself. To obtain an order of magnitude for this stray capacitance, a test PC board yielded a measured 0.9 pF per inch for the TO-116 package. To fully appreciate this problem, consider the OFF isolation at 10 MHz for the DG181, with only 0.5 in of adjacent line external to the switch. C_{STRAY} = 0.45 pF and $|C_{Eq}|$ = 0.25 pF; thus C_I = 0.7 pF, for an OFF isolation of 50 dB (a *loss* of 8 dB of isolation).

Extending the Range of the Design Aids

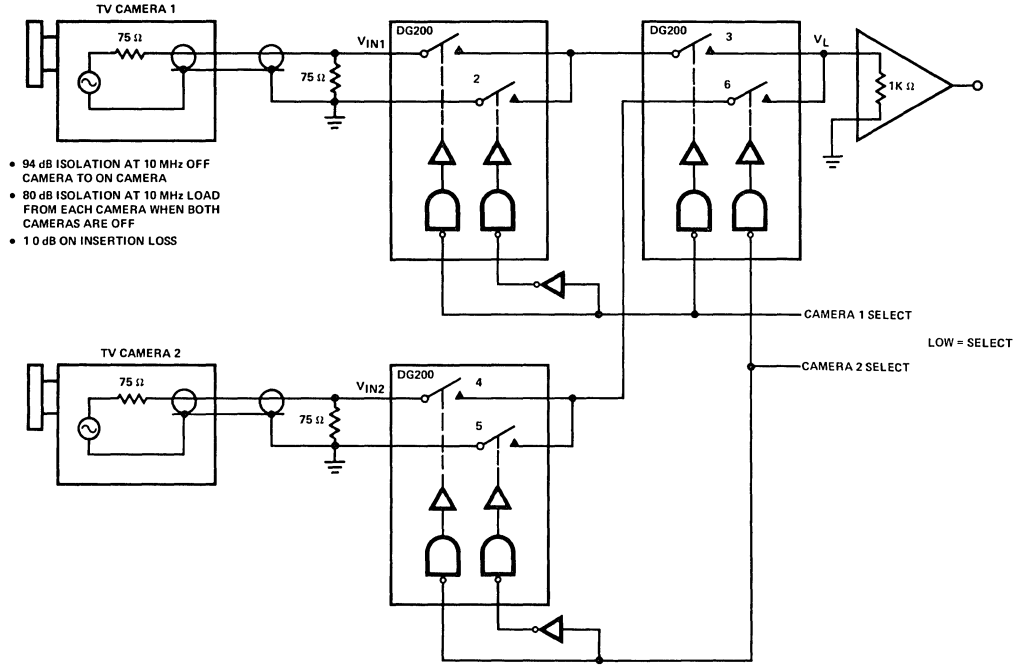
The body of this application note explains the general use of the design aids for high-frequency isolation (sinusoidal) and pulse feedthrough isolation (see Figures 5 and 6). However, there are cases where the identification of the proper analog switch for a circuit lies beyond the range of the design aid. For example, the design aid may be extended to solve for $C_I \cong |C_{Eq}|$ where f = 2 MHz, R_L = 1K Ω, and desired isolation is 80 dB. The 80 dB isolation curve does not have an R_LC_I product on the graph at 2 MHz. However, R_LC_I for 60 dB at 2 MHz is 80 Ω - pF. Since R_LC_I (80 dB) = 0.1 R_LC_I (60 dB), then R_LC_I (80 dB) = 8 Ω - pF. R_L = 1K Ω and C_I = 8 Ω - pF ÷ 1K Ω = 0.008 pF. No single switch will satisfy the isolation requirement. But if one uses a multiple switch configuration, as in the series shunt circuit shown in Figure 29, it is possible to obtain the required isolation, since $R_L \cong$ 50 Ω and C_I = 0.16 pF. Thus two DG181 analog switches will do the job, since $C_I \cong$ 0.12 pF at 2 MHz.

The same type of extension can be applied to the pulse feedthrough design aid shown in Figure 6.

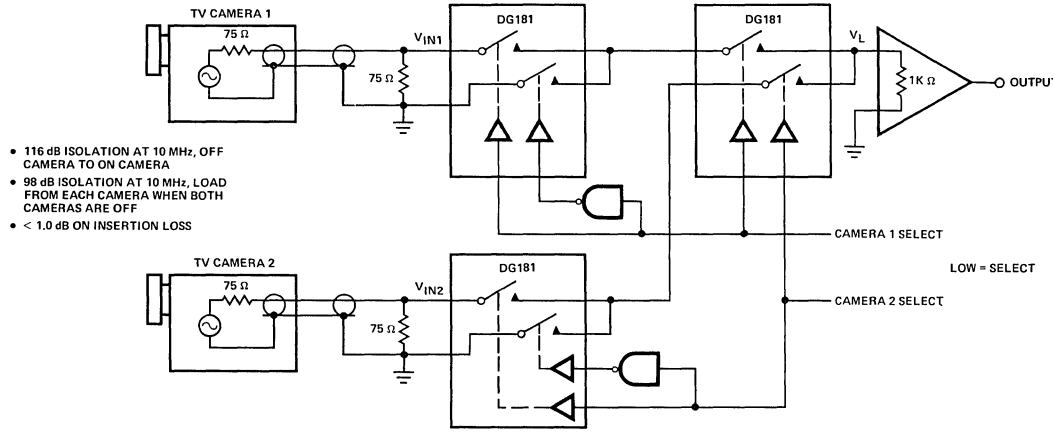


Series Shunt Circuit
Figure 29

Additional Application Circuits:



Video Switch with Very High OFF Isolation
(f = DC to 10 MHz)
Figure 30



Video Switch with Very High OFF Isolation
(f = DC to 10 MHz)
Figure 31

7.4 Driver Circuits for the JFET Analog Switch (AN73-5)

August, 1973

INTRODUCTION

Both junction field-effect transistors (JFETs) and metal-oxide-silicon (MOS) FETs may be used as analog switches, but the JFET offers the advantages of lower ON resistance ($r_{DS(on)}$), and a constant ON resistance vs signal level characteristic.(1) However, these attributes of the JFET switch can only be realized through design of a suitable driver circuit for the transistor. Design of proper driving circuits presents a number of subtle problems, and overall performance of the analog switch is primarily limited by the characteristics of the driver. This Application Note deals with the design considerations encountered in drivers for FET switches.

Before exploring the problems of driver circuit design, it will be well to define the tasks that an analog switch may be expected to perform. Analog signal processing may be divided into two broad categories:

(1) Handling DC and low-frequency AC signals, and
(2) Handling high-frequency AC signals.

If one is to multiplex a large number of DC or low-frequency AC signals onto a common bus, the major concern will be centered around rapid switching (typically 1 μsec or so). On the other hand, if high-frequency AC signals are to be processed, good ON/OFF ratios are a prime consideration, and switching speed is relatively unimportant (typically tens to hundreds of microseconds). In other words, a single switch will not usually be called upon to perform both high-speed switching and high-frequency signal processing. Of course, if both tasks can be performed by a given type of analog switch, then a user can realize economy by procuring large quantities.

Primary speed limitations on complete analog switch circuits are imposed by the switch driver circuits themselves. An example of this limiting effect is shown in Table I, where a 2N4392 (discrete JFET) is compared with several analog switching integrated circuits.

Table I
Effect of Driver Circuit on Switch Speed

Device	t_{on} (ns)	t_{off} (ns)	$r_{DS(on)}$ (Ω)
2N4392(1)	20	55	60
IH5007(2, 3)	500	1,000	80
AH0126(2, 3)	800	1,600	80
DG126(2, 3)	600	1,600	80
DG182(2, 3)	250	130	75

(1) The 2N4392 is a discrete JFET, driven from a 500 ps pulse generator with 50 Ω source impedance.
(2) These analog switches contain, in addition to an IC driver circuit, chips for 2N4392 JFETs.
(3) These analog switches have TTL-compatible control inputs. The discrete 2N4392 does not.

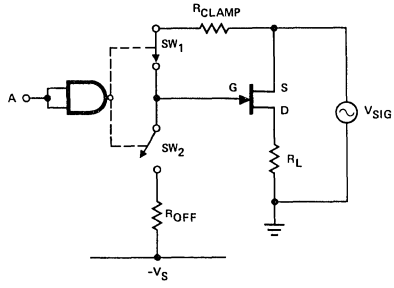
Table I makes two major points. First, the discrete JFET, by itself, has a considerably faster switching time than that of the analog switch containing the FET chip plus a driver. Second, the DG182 is a much faster analog switch integrated circuit than are the other three similar devices. The evolution of the DG182 switch/driver will be observed as the design details of four analog switch circuits are explored in depth.

The four basic driver circuits considered in this presentation will show the evolution of junction FET drivers from the fairly simple forms of several years ago to the complex integrated circuit drivers of today. The four circuit types include (1) resistor-coupled, (2) diode charge transfer, (3) transistor charge transfer, and (4) switched-resistor. They will be covered in terms of circuit operational theory, performance comparison, and the economics of make-or-buy decisions.

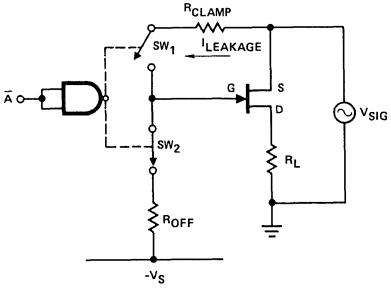
The junction FET is ON when V_{GS} = 0 volts, and this state may be achieved by placing a resistance between the gate and the source. So long as the current through this resistance

is zero, the gate-to-source voltage will also be zero (care must be taken that the gate-to-source diode is not forward-biased during the analog signal excursion). The functional diagram for an ideal JFET driver is shown in Figure 1. Figure 1A considers the ON case, and helps establish desirable characteristics for the driver under ON conditions. Since both gate and source will follow the analog signal, the impedance from gate to ground must be very large, to prevent current from flowing through R_{CLAMP}. In Figure 1B, the switch is in the OFF state, and the gate is clamped to the negative supply (V_2) through R_{OFF}. SW_1 should be open, since leakage will be small under these conditions. When processing high-frequency signals, R_{OFF} should have a small value.(2)

One additional point: the logic input levels are typically zero to 5 volts, while the switch driver output will range from the negative to the positive supply voltages. The positive supply voltage must at least equal the peak analog signal (typically +10 volts), and may even be higher.



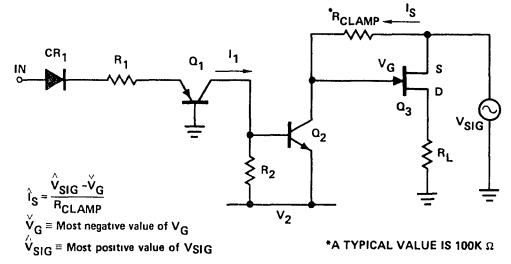
ON Condition for JFET
Figure 1A



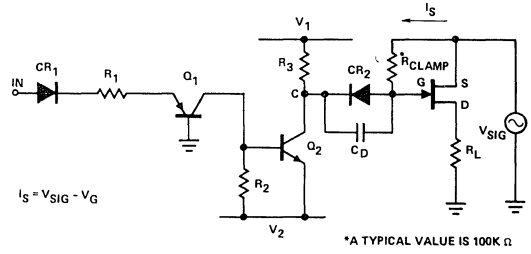
OFF Condition for JFET
Figure 1B

RESISTOR-COUPLED AND DIODE CHARGE TRANSFER DRIVERS

The simplest driver circuit is the resistor-coupled arrangement shown in Figure 2. Recall that in the circuit in Figure 1, SW_1 is permanently closed. In addition, Q_2 (in Figure 2), assumes the role of SW_2 in the ideal circuit (Figure 1). Q_2 (ON) presents a low impedance to AC ground and Q_2 (OFF) presents a high impedance to AC ground. The operation of the diode charge transfer circuit in Figure 3 is similar, in that SW_1 is permanently closed and SW_2 (Q_2 and CR_2) is the only JFET control.



Resistor-Coupled Driver
Figure 2



Diode Charge Transfer Driver
Figure 3

In Figure 2, assume that V_{IN} is 5 volts. Q_1 is ON, and I_1 turns Q_2 ON, which pulls its collector to V_2 (typically −15 volts). Since the gate of Q_3 is tied to the collector of Q_2, then V_G is also at V_2. In this condition, Q_3 is OFF and will remain OFF so long as the *most negative value* of V_{SIG} (= V_{SIG}) is greater than (V_G − $V_{GS(off)}$). If $V_{GS(off)}$ is assumed to be −3.5 V, then

$$V_{SIG} = -15\text{ V} - (-3.5\text{ V}) = -11.5\text{ V}$$

If the rated V_{SIG} is 10 V, then I_S will flow when V_G is at −15 V (Q_3 is OFF). This value of I_S depends on R_{CLAMP} and introduces a conflict between switching time and leakage current (I_S). The data in Table II emphasizes the magnitude of this conflict. The following voltages were used to establish performance of the resistor-coupled driver circuit:

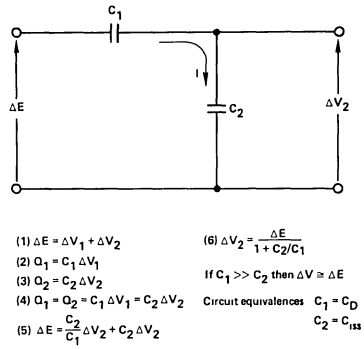
(1) V_{SIG} = 10 V
(2) V_G = −15 V (Eq = V_{SIG} − V_G = 25 V)
(3) V_O = 500 mV (Insures that devices with $|V_{GS(off)}|$ = 1 V will turn ON).

Table II
Performance of Resistor-Coupled Circuit

R_{CLAMP} (Ω)	t_{on} (μs)	I_S (μA)
1 M	82.1	25
100 K	8.21	250
10 K	0.821	2,500
Q_2 = 2N4400, $C_{OB} \cong 5$ pF Q_3 = 2N4393, $C_{iss} \cong 16$ pF $C = C_{OB} + C_{iss} = 21$ pF		
Note 1: $R_{CLAMP} C \ln Eq/V_o$, where Eq is the initial voltage (t = 0) on C and V_o is the instantaneous voltage at time t. Note 2: $Eq/V_o = 25\ V/0.5\ V = 50$ in the above t_{on} calculations.		

Operation of the diode charge transfer driver circuit (Figure 3) is similar to that of the resistor-coupled circuit. Assume that Q_2 is ON ($V_C \cong -14.3$ V). Thus $V_{SIG} - V_G = 24.3$ V, and Eq/V_O remains essentially the same as in the resistor-coupled circuit. Additionally, C_{OB} of 6 pF is replaced by the capacitance of CR_2 (about 2 pF), and total circuit capacitance thus reduces from 21 pF to 17 pF, with a corresponding reduction in turn-ON time.

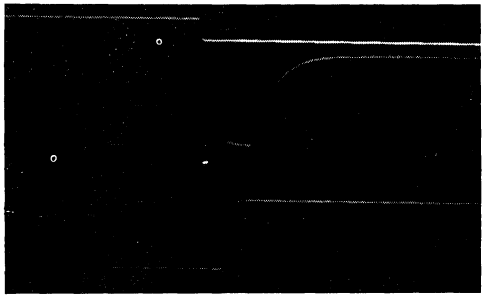
At first glance, this reduced turn-ON time appears to offer very little improvement over the resistor-coupled circuit. However, the capacitance labeled C_D in the circuit in Figure 3 contributes to a significant difference in turn-ON time; Figures 4A and 4B demonstrate this difference.



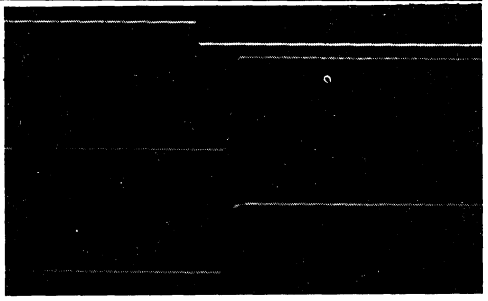
Analysis of Charge Distribution Between Two Capacitor in Series
Figure 5

Analysis of the equivalent circuit shown in Figure 5 shows why the variation of 0 to 160 pF in C_D causes the reduction in turn-ON time.

In Figure 5, the voltage across C_2 ($= C_{iss}$) is affected as C_1 ($= C_D$) is varied. Note that ΔE and ΔV_2 change at the same rate, since the total series circuit is capacitive. (Figure 4B also illustrates this condition).



R_{CLAMP} = 100K, C_D = 0, V_{SIG} = +10 V DC
TOP: V_{IN}
MIDDLE: V_D 4(A)
BOTTOM: V_C
SCALES:
Horizontal = 1 μs/div
Vertical = 5 V/div*



R_{CLAMP} = 100K, C_D = 160 pF, V_{SIG} = +10 V DC
TOP: V_{IN}
MIDDLE: V_D 4(B)
BOTTOM: V_C
SCALES:
Horizontal = 1 μs/div
Vertical = 5 V/div*

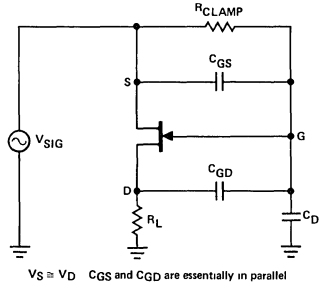
*Refers to V_D only, as V_{IN} and V_C are shown for timing information only; note t_r of $V_C \cong$ 200 ns in each instance

Effect of C_D on Turn-ON Time
Figure 4

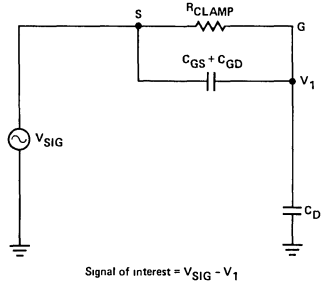
The diode charge transfer driver circuit (Figure 3) produces an analog switch which can be turned ON in less than 1 μs and which has an I_S of 243 μA. The resistor-coupled driver circuit in Figure 2 has an I_S value of 250 μA but requires 8 μs to turn ON. What happens if one tries to pass high-frequency signals through the ON switch of the diode charge transfer driver? Figure 6 shows the progression of an actual circuit (6A) to an intermediate equivalent circuit (6B) to a final circuit (6C), which solved for V_{GS}:

$$V_{GS} = \frac{j\,\omega R_{CLAMP}\,C_D\,V_{SIG}}{1 + j\,\omega R_{CLAMP}\,(C_D + C_{iss})} \qquad (1)$$

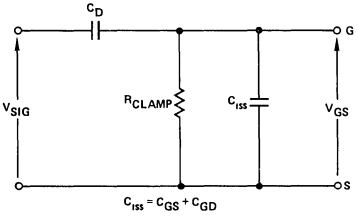
Equation (1) defines the peak voltage which will develop across R_{CLAMP} as the frequency is varied. The frequency at which a particular junction FET will pinch itself off is a function of the $V_{GS(off)}$ of that device, as well as V_{SIG}.



6(A)



6(B)

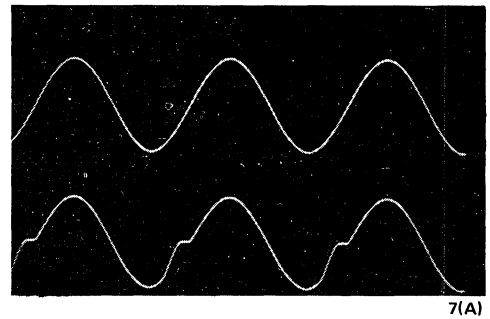


6(C)

Equivalent Circuit for ΔV_{GS} Analysis at "High" Frequencies
Figure 6

Figure 7A shows the cut-off phenomenon occuring at 1.4 kHz, (a low frequency).

Measured $V_{GS(off)}$ of the device, in Figure 7A, is –1.6 V (I_D = 1 μA). The calculated value of V_{GS} is 1.39 V. In Figure 7B, the switch is passing 500 kHz, no matter whether R_{CLAMP} is 100K Ω or 1M Ω. Thus if one wants to pass signals of relatively high frequency, and switching speeds of tens of microseconds can be endured, then the circuit condition with $C_D \longrightarrow 0$, should be used. On the other hand, if the data to be passed is at a frequency below 1 kHz, and fast switching speed is mandatory, then the C_D = 160 pF condition will suffice. The important point is: the diode charge transfer driver will not handle both problems with the same C_D condition.

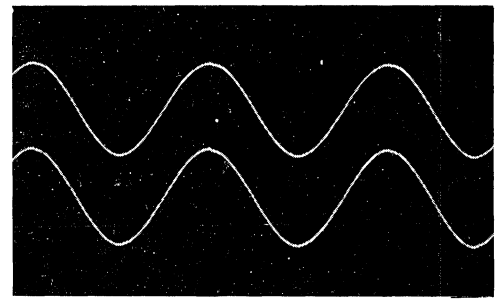


7(A)

R_{CLAMP} = 100K Ω, C_D = 160 pF, C_{iss} = 16 pF,
V_{SIG} = 20 V P-P, R_L = 2.2K Ω

SCALES:
Horizontal = 200 μs/div
Vertical = 10 V/div
f = 1.4 kHz

TOP: Input
BOTTOM: Output



7(B)

R_{CLAMP} = 100K Ω to 1M Ω, C_D = 0 pF, C_{iss} = 16 pF
V_{SIG} = 20 V P-P, R_L = 2.2K

SCALES:
Horizontal = 500 ns/div
Vertical = 10 V/div
f = 500 kHz

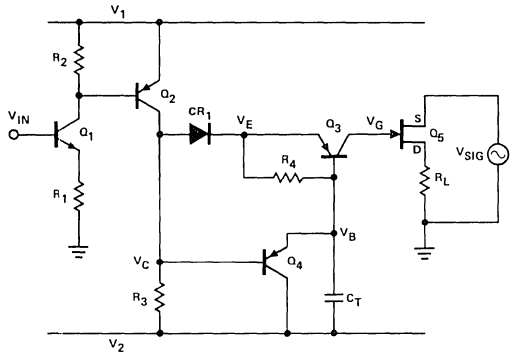
TOP: Input
BOTTOM: Output

NOTE:
Self-pinchoff occurs when $\frac{\delta}{\delta t}(V_{SIG})$ is max, not when V_{SIG} is max.

AC Performance of Diode Charge Transfer Driver Circuit
Figure 7

TRANSISTOR CHARGE TRANSFER DRIVER

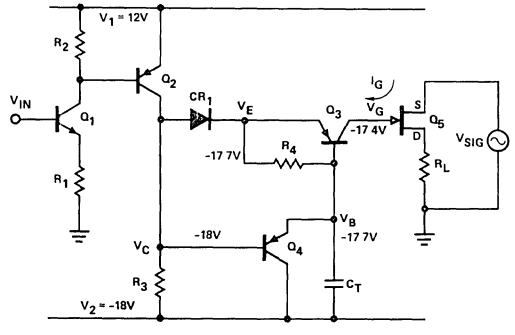
The use of the capacitor, C_D, in the diode charge transfer driver circuit suggests a more sophisticated charge transfer method. Figure 8 shows a transistor charge transfer driver circuit, in which the diode is replaced by a transistor. Since the charge transfer occurs in the collector circuit of transistor Q_3, then the required C_T is reduced in value by the β of Q_3.



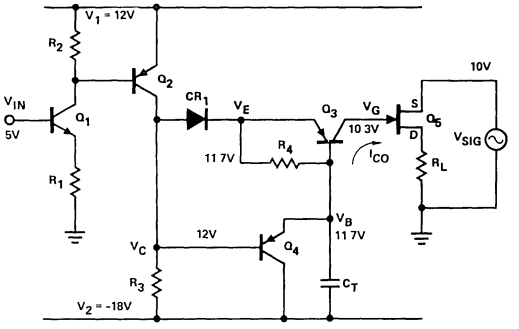
Transistor Charge Transfer Driver Circuit
Figure 8

Before the operation of the transistor charge transfer circuit is discussed in detail, an overview is in order. Transistors Q_1 and Q_2 provide gain and voltage translation to drive the charge control transistors Q_3 and Q_4. In turn, Q_3 transfers the charge necessary to turn JFET Q_5 (the switch) ON, and Q_4 provides a low impedance path to discharge C_T and turn Q_5 OFF.

Figures 9A and 9B provide additional insight into the operation of the transistor charge transfer driver. Q_5 (the JFET switch) is OFF because the gate voltage is negative (9A). This condition causes a reverse leakage current, I_G, (from Q_5) to flow through the collector-base junction of Q_3 and the emitter-base junction of Q_4. If the value of I_G is in the order of 1 nA (10^{-9} amperes), the junction drops will be approximately 300 mV. Note that V_C (the base of Q_4) is at −18 V, because when $V_{IN} = 0$, Q_1 and Q_2 are turned OFF. V_B and V_C are 300 mV and 600 mV respectively above V_C. Further, since $V_E = V_B$ then Q_3 is also OFF.



Transistor Charge Transfer Circuit in OFF Condition
Figure 9A



Transistor Charge Transfer Circuit in ON Condition
Figure 9B

Figure 9B shows the analog switch in the ON condition. It is assumed that the analog signal voltage is 10 V, the I_{CO} is approximately 1 nA, and that V_G is approximately 300 mV above V_{SIG}. Since V_{IN} is at 5 volts, then Q_1 and Q_2 are turned ON, and V_C is essentially at +12 V. I_{CO} flows through CR_1, and thus V_E is 300 mV below V_C.

The performance of the circuit during turn-ON is of interest. When V_{IN} goes to +5 volts, turning Q_1 and Q_2 ON, V_C begins to rise from −18 V (Figure 9A). V_B cannot follow this excursion instantaneously, due to C_T, and thus Q_4 is turned OFF. V_C rises sufficiently to forward-bias CR_1 and the emitter-base voltage of Q_3. This condition continues to hold Q_4 OFF and to force the charging current flowing into C_T to flow through R_4 and the base of Q_3. If $\Delta V_C/\Delta T$ is large enough, most of this charging current flows through the base of Q_3. The circuit is designed so that rise times of 1 μs or less will provide for satisfactory circuit operation. Since most digital circuits switch in tens of nanoseconds, this 1 μs design constraint will not give rise to switching speed problems. The current in the collector of Q_3 is β times the base current; thus the change in charge in the collector circuit is β times the change in charge in the base. Hence, C_T is effectively multiplied by β for purposes of charging the input capacitance of Q_5. This technique permits the use of transistors for Q_3 with β as low as 10, and capacitance, C_T, as low as 5 pF, to control JFETs with $C_{iss} \cong 20$ to 30 pF. One further advantage: Q_3 is OFF during both steady-state conditions. This allows the collector of Q_3 to follow the analog signal when Q_5 is ON, and to present a very small capacitance to ground. Thus the transistor charge transfer driver does not have the self-cutoff problem found in the diode charge transfer circuit.

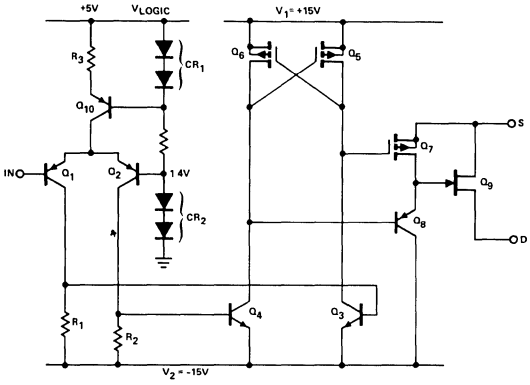
Finally, $V_{IN} \rightarrow 0$ volts turns Q_1 and Q_2 OFF, pulling V_C and V_B negative. In this way, Q_4 rapidly discharges C_T, and by placing forward bias on the collector-base junction of Q_3, turns Q_5 OFF.

Using the terminology from Figure 1, the transistor charge transfer circuit includes both SW_1 and SW_2, cut R_{CLAMP} and R_{OFF} are both large resistors, in the megohm region. When Q_5 is on, the gate-to-channel diode is forward-biased by I_{CO} (Figure 9B), which is in the order of 1 nA. R_{CLAMP} is the equivalent resistance of a forward-biased junction

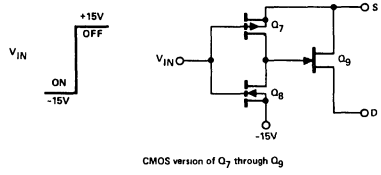
with $I_F \cong 1$ nA (i.e. $R_{CLAMP} \cong 26M\ \Omega$). Similarly, R_{OFF} is the equivalent resistance of two forward-biased junctions (Figure 9A), with I_F also $\cong 1$ nA (i.e., $R_{OFF} = 52M\ \Omega$).

THE SWITCHED-RESISTOR DRIVER

When compared to the ideal JFET driver circuit shown in Figure 1, both the diode charge transfer and transistor charge transfer circuits have several shortcomings. However, a circuit which approaches the performance of the ideal JFET driver is shown in Figure 10, and is known as a switched-resistor driver.



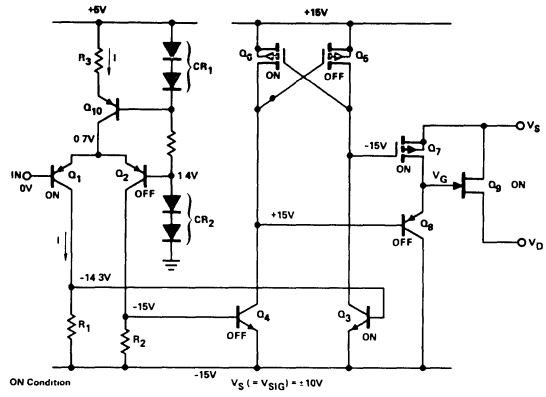
Switched-Resistor Driver Circuit
Figure 10A



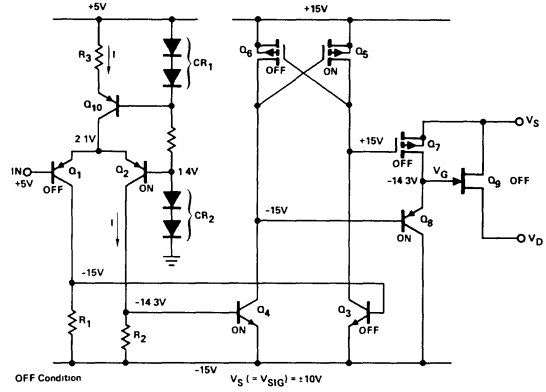
CMOS Version of Q_7 through Q_9
Figure 10B

An overview of the performance characteristics of this circuit shows that when Q_9 is ON, Q_7 is ON, clamping the gate to the source, and Q_8 is OFF. Thus the gate of Q_9 sees a high impedance to ground when it is ON. Assuming that Q_9 and Q_7 are OFF and Q_8 is ON, the gate of Q_9 sees a low impedance to ground (R_{OFF}) when the device is OFF. This circuit has low leakage currents in both the ON and OFF state, because the V_{GS} clamp is itself a switch, and *not* a fixed resistor.

Figure 11A shows details pertinent to the switched-resistor circuit when JFET Q_9 is ON. Q_1 is ON, and provides a base current for Q_3, which is also ON. The collector of Q_3 is at -15 V, and turns Q_7 (SW_1 in the ideal JFET switch driver) ON. Q_7 thus turns Q_9 ON, since $V_{GS} = 0$ V. In addition, since Q_3 is ON, Q_6 is turned ON; on the other hand, Q_2 is OFF, and Q_4 is thus turned OFF, clamping the collector of Q_4 to +15 V through Q_6. Since the gate of Q_5 is at +15 V, it is also OFF. Under the conditions shown in Figure 11A, Q_8 is OFF, since its emitter-base diode is reverse-biased (SW_2 in Figure 1 is open).



Switched Resistor Circuit Conditions When Analog Switch is ON
Figure 11A

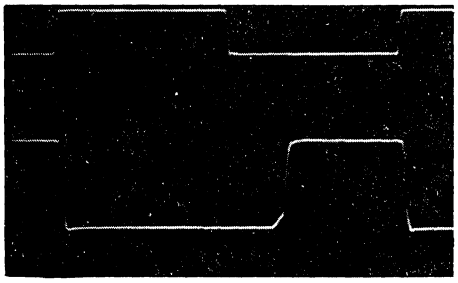


Switched Resistor Circuit Conditions When Analog Switch is OFF
Figure 11B

Figure 11B is derived from Figure 11A by reversing the roles of the transistors – the ON transistors become the OFF transistors, and vice versa. Note that Q_8 is the ON state presents a low impedance to ground (R_{OFF} in Figure 1). The switched-resistor driver design is also conservative of power; both Figures 11A and 11B have open circuits between the +15 V and –15 V supplies.

PERFORMANCE COMPARISONS OF DRIVER CIRCUITS

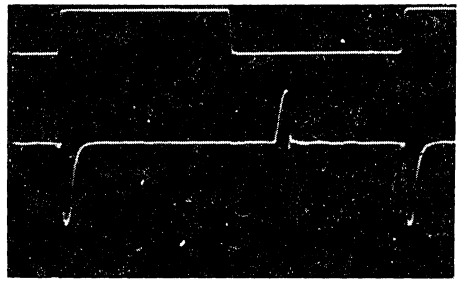
Figures 12 through 15 and Table III summarize performance characteristics of three of the four types of JFET driver circuits which have been discussed in this presentation – diode charge transfer, transistor charger transfer, and switched-resistor drivers. Figures 12, 13 and 14 compare switching speeds, and the switched-resistor circuit is obviously the top performer.



GROUND

Vertical = 5 V/div
V_{SIG} = +10 V

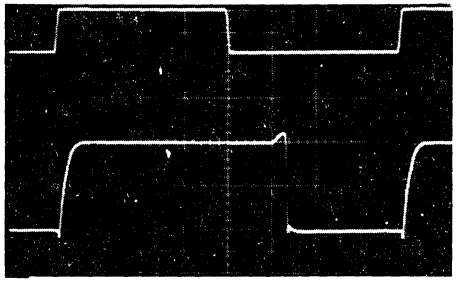
A



GROUND

B

Vertical = 1 V/div
V_{SIG} = 0 V



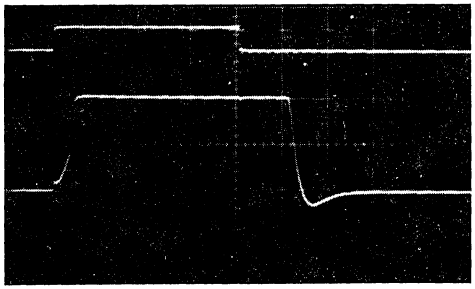
GROUND

C

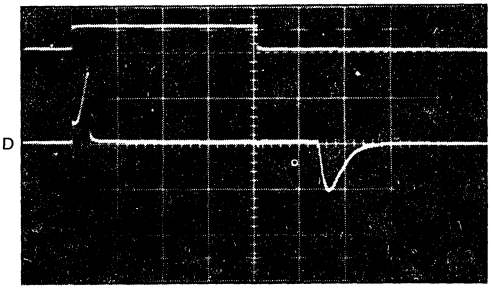
Vertical = 5 V/div
V_{SIG} = −10 V

- Horizontal = 500 ns/div for all waveforms
- Top waveform is logic input for timing purposes only. When logic input is low, switch is ON.
- Same circuit as Figure 4B

Diode Charge Transfer Driver Circuit Switching Performance
Figure 12



GROUND



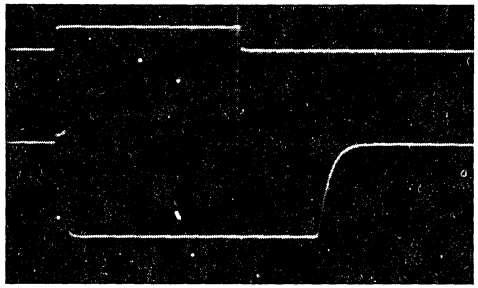
GROUND

Vertical = 5 V/div
V_{SIG} = 10 V DC

A

B

Vertical = 2 V/div
V_{SIG} = 0 V



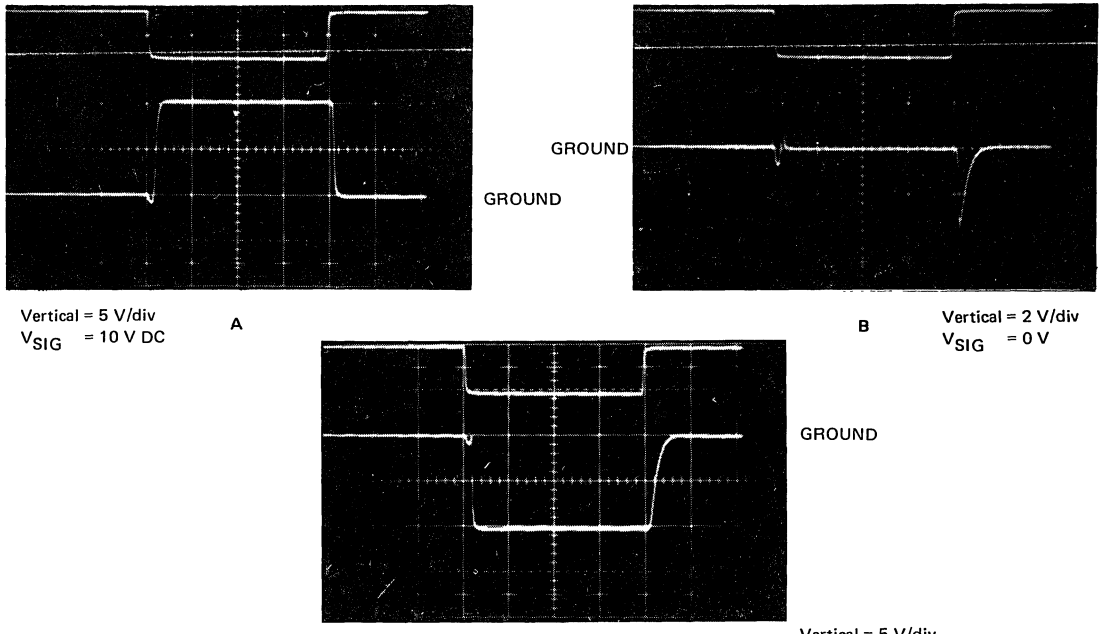
GROUND

C

Vertical = 5 V/div
V_{SIG} = 10 V DC

- Horizontal = 500 ns/div for all waveforms
- Top waveform is logic input for timing purposes only. When logic input is high, switch is ON

Transistor Charge Transfer Driver Circuit Switching Performance
Figure 13



- Horizontal scales = 500 ns/div for all waveforms
- Switching control (top waveform) is for timing purposes only. Switch is ON when switching control is low

Switched Resistor Driver Circuit
Switching Performance
Figure 14

The switched-resistor driver design is the same as that used in the Siliconix series DG181-DG191 analog switches. In addition to the obviously superior switching speed of this circuit, the DG181-DG191 family can handle high-frequency signals (to 100 MHz) with excellent OFF isolation. Details of high-frequency performance of this group of devices are presented in the Siliconix Application Note "Switching High-Frequency Signals With FET Integrated Circuits."

To compare the large signal handling capability of the three types of JFET driver circuits, data was taken at 500 kHz and 20 volts peak-to-peak analog signal range. Performance of the transistor charge transfer and switched resistor driver circuits is compared to Figure 15.

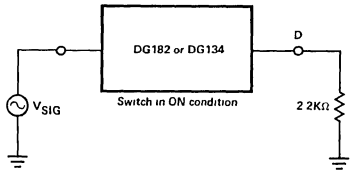
Data on performance of the diode charge transfer driver was presented in Figure 7B. Note that large signal high-frequency capability must be sacrificed if the diode charge transfer circuit is to perform at switching speeds comparable to the transistor charge transfer and switched-resistor circuits.

Table III summarizes the results presented in Figures 7B, 12, 13, 14 and 15. Leakage currents and average dissipation of the three analog switch circuits is compared.

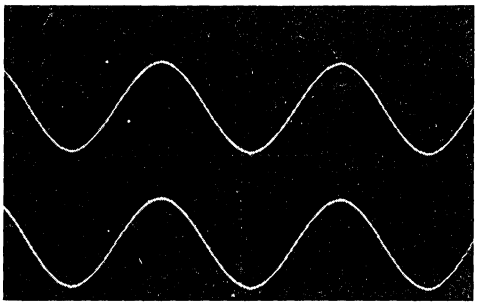
Table III
Comparison of Leakage Current, Switching Time, High-Frequency Signal Handling and Power Dissipation

Characteristic	Diode Charge Transfer	Transistor Charge Transfer	Switched-Resistor
$I_{S(off)}$ (μA)	243(1)	0.001	0.001
t_{on} (ns)	800	200	150(2)
t_{off} (ns)	200	1,200	100(2)
f (cut-off) (kHz)(3)	1.4(1)	>500	>500
P_d (channel) (mW)(4)	166	17	60

NOTE 1: R_{CLAMP} = 100K Ω, C_D = 160 pF
NOTE 2: V_{SIG} = +10 V DC, R_L = 10K Ω
NOTE 3: V_{SIG} = 20 V P-P, R_L = 2.2K Ω
NOTE 4: Switch is ON 50% of time



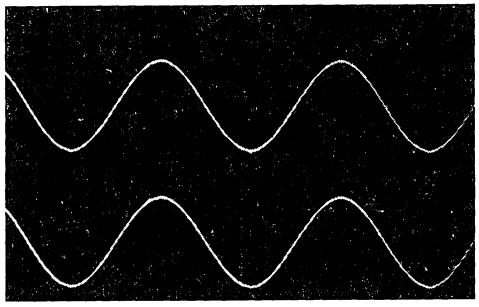
TEST CIRCUIT



A

TRANSISTOR CHARGE TRANSFER DRIVER

Top Waveform: V_{SIG}
Bottom Waveform: V_{DRAIN}
Voltage = 10 V/div
Time = 500 ns/div



B

SWITCHED-RESISTOR DRIVER

Top Waveform: V_{SIG}
Bottom Waveform: V_{DRAIN}
Voltage = 10 V/div
Time = 500 ns/div

Large Signal Performance at High Frequency
Figure 15

MAKE OR BUY?

When the driver circuits which have been analyzed are compared, it is apparent that there is a close correlation between improved performance and increased circuit complexity. For instance, if discrete components were used in the switched-resistor circuit, the increased complexity of the circuit would make costs prohibitive. Fortunately, the switched-resistor driver circuit is available as a monolithic integrated circuit and costs are considerably lower than the same circuit constructed with discrete components. Thus the diode charge transfer driver (a discrete component circuit) is apparently inexpensive because of its simplicity. Is it really true? In reality, the real comparison is made when evaluating *total* costs to produce both the diode charge transfer circuit and the switched-resistor circuit. Table IV compares actual costs with parts costs.

Note that testing cost is calculated as 120% of the manufacturing cost. The rationale for this figure is the labor differential between production and technician help, *plus* additional time spent locating and replacing faulty components. For example, less time (less money) is spent replacing a faulty integrated circuit than is required to locate and replace a bad component in a discrete circuit. Additionally, the versatility of the analog switch integrated circuit permits its use in many applications, tending to increase the quantity purchased and thus reducing the cost.

Table IV
Comparison of Circuit Manufacturing and Parts Costs

Cost Item	Diode Charge Transfer Circuit	Switched-Resistor Circuit
Parts	$0.89	$2.81(1)
Assembly(2)	2.23	0.69
Pre-Test Total	$3.12(3)	$3.50
Testing	2.68	0.83
Total Production	$5.80(4)	$4.33

Note 1: Pre-channel cost in large quantities.

Note 2: Includes labor costs and pro-rated costs of PC board "real estate."

Note 3: Pre-test cost of the diode charge transfer circuit is 89% of that of a high-performance IC.

Note 4: Total production cost for the diode charge transfer circuit is 134% of that of a high performance IC.

Note 5: Above manufacturing cost data obtained from a local OEM electronics firm (non-military).

Designing a circuit such as the switched-resistor driver is a relatively complicated affair. In the early days of semiconductor technology, when discrete components were widely prevalent, the cost for such a circuit would have been difficult to justify. But today's advanced integrated circuit technology removes this cost obstacle. In short, the user of IC analog switches can procure high performance at low cost, and be relieved of the concerns associated with the manufacture of the circuit with discrete components.

REFERENCES

(1) "FETs as Analog Switches," Siliconix inc., Application Note, Sept. 1972.

(2) "Switching High-Frequency Signals with FET Integrated Circuits," Siliconix inc., Application Note, March, 1973.

7.5 An Introduction to FETs (AN73-7)

Revised April 1976

INTRODUCTION

The basic principle of the field-effect transistor (FET) has been known since J.E. Lilenfeld's patent of 1925. The theoretical description of a FET made by Schockley in 1952 paved the way for development of a classic electronic device which provides the designer with the means by which he can accomplish nearly every circuit function. The field-effect transistor earlier was known as a "unipolar" transistor, and the term refers to the fact that current is transported by carriers of one polarity (majority), whereas in the conventional bipolar transistor carriers of both polarities (majority and minority) are involved.

This Application Note provides an insight into the nature of the FET, and touches briefly on its basic characteristics, terminology and parameters, and typical applications.

The following list of FET applications indicates the versatility of the FET family:

Amplifiers	*Switches*	*Current Limiters*
Small Signal	Chopper-type	*Voltage-Controlled*
Low Distortion	Analog Gate	*Resistors*
High Gain	Commutator	*Mixers*
Low Noise		*Oscillators*
Selective		
D.C.		
High-Frequency		

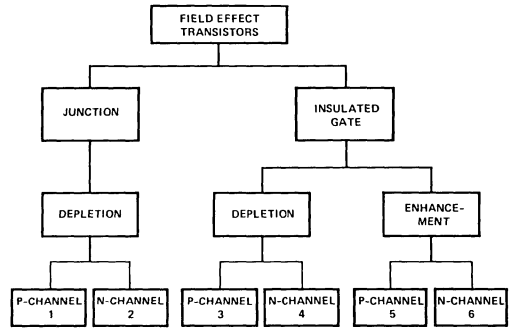
This very wide range of FET applications by no means implies that the device will replace the more widely-known bipolar transistor in every case. The simple fact is that FET characteristics – which are very different from those of bipolar devices – can often make possible the design of technically superior (and sometimes cheaper) circuits. This comment applies not only to networks employing discrete devices and conventional components such as resistors and capacitors, but also extends to both linear and digital integrated circuits.

In fact, FET technology today allows a greater packaging density in large-scale integrated circuits (LSI) than would ever be possible with bipolar devices.

(Although there is no industry-accepted definition of LSI, apparently when the equivalent circuit of an IC contains more than 1,000 active elements (500 gates) or is "very complex", the end product may be called LSI. With a typical LSI chip measuring less than 200 x 200 mils, this is high-density packaging indeed.)

The family tree of FET devices (Figure 1) may be divided into two main branches, junction FETs (JFETs) and Insulated Gate FETs (or MOSFETs, *metal-oxide-silicon field-effect transistors*). Junction FETs are inherently depletion-mode devices, and are available in both P- and N-Channel configurations. MOSFETs are available in both enhancement or depletion modes, and exist as both N- and P-Channel devices. The two main FET groups depend on different phenomena for their operation, and will be discussed separately.

CHAPTER 7

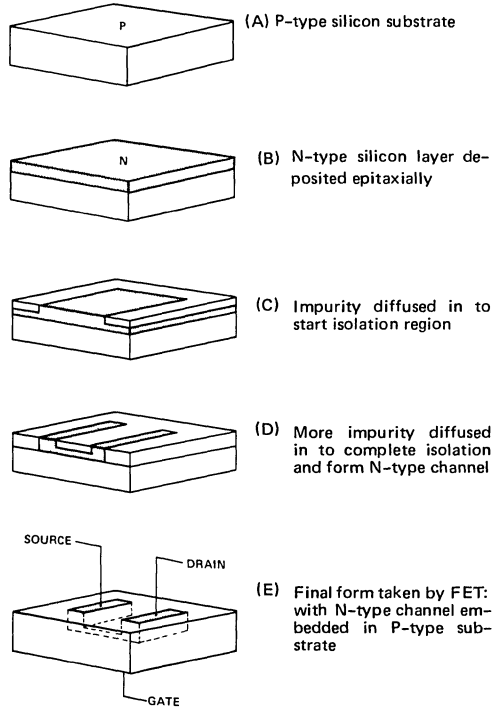


FET Family Tree
Figure 1

Junction FETs

In its most elementary version, this transistor consists of a piece of high-resistivity semiconductor material (usually silicon) which constitutes a channel for the majority carrier flow. The magnitude of this current is controlled by a voltage applied to a *gate*, which is a reverse-biased PN junction formed along the channel. Implicit in this description is the fundamental difference between FET and bipolar devices: when the FET junction is reverse-biased the gate current is practically zero, whereas the base current of the bipolar transistor is always some value greater than zero. The FET is a high input resistance device, while the input resistance of the bipolar transistor is comparatively low. If the channel is doped with a donor impurity, N-type material is formed and the channel current will consist of electrons. If the channel is doped with an acceptor impurity, P-type material will be formed and the channel current will consist of holes. N-Channel devices have greater conductivity than P-Channel types, since electrons have higher mobility than do holes; thus N-Channel FETs tend to be more efficient conductors than their P-Channel counterparts.

Junction FETs are particularly suited to manufacture by modern planar epitaxial processes. Figure 2 shows this process in an idealized manner. First, N-type silicon is deposited epitaxially (single-crystal condensation surface) onto monocrystalline P-type silicon, so that crystal integrity is maintained. Then a layer of silicon dioxide is grown on the surface of the N-type layer, and the surface is etched so that an acceptor-type impurity can be diffused through into the silicon. The resulting cross-section is shown in Figure 2C, and demonstrates how a P-type annulus has been formed in the layer on N-type silicon. Figure 2D shows how a further sequence of oxide growth, etching, and diffusion can produce a channel of N-type material within the substrate.



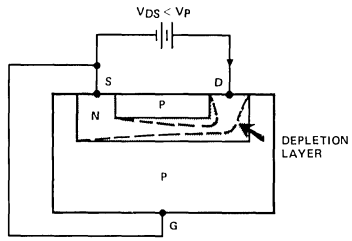
Idealized Manufacture of an N-Channel Junction FET
Figure 2

In addition to the channel material, a FET contains two ohmic (non-rectifying) contacts, the *source* and the *drain*. These are shown in Figure 2E. Since a symmetrical geometry is shown in the idealized FET chip, it is immaterial which contact is called the source and which is called the drain; the FET will conduct current equally well in either direction and the source and drain leads are usually interchangeable.

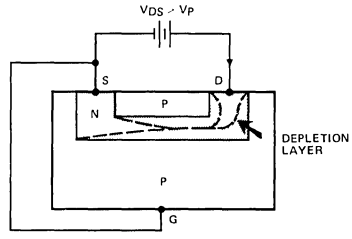
(For certain FET applications, such as amplifiers, an asymmetrical geometry is preferred for lower capacitance and improved frequency response. In these cases, the source and drain leads should not be interchanged.)

Figure 2E also shows how the N-Channel is embedded in the P-type silicon substrate, so that the gate above the channel becomes part of this substrate. Figure 3 shows how the FET functions. If the gate is connected to the source, then the applied voltage (V_{DS}) will appear between the gate and the drain. Since the PN junction is reverse-biased, little current will flow in the gate connection. The potential gradient established will form a *depletion* layer, where almost all the electrons present in the N-type channel will be swept away. The most depleted portion is in the high field between the gate and the drain, and the least-depleted area is between the gate and the source. Because the flow of current along the channel from the (positive) drain to the (negative) source is really a flow of free electrons from source to drain in the N-type silicon, the magnitude of this current will fall as more silicon becomes depleted of free electrons. There is a limit to the drain current (I_D) which increased V_{DS} can drive through the channel. This limiting current is known as I_{DSS} (*Drain-to-Source* current with the gate *Shorted* to the source). Figure 3B shows the almost complete depletion of the channel under these conditions.

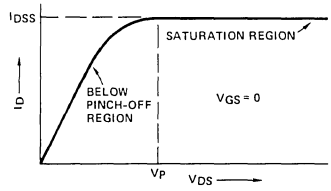
Figure 3C shows the output characteristics of an N-Channel JFET with the gate short-circuited to the source. The initial rise in I_D is related to the buildup of the depletion layer as V_{DS} increases. The curve approaches the level of the limiting current I_{DSS} when I_D begins to be *pinched off*. The physical meaning of this term leads to one definition of *pinch-off voltage*, V_P, which is the value of V_{DS} at which the maximum I_{DSS} flows.



(A) N-channel FET working below saturation (V_{GS} = 0). (Depletion shown only in channel region).



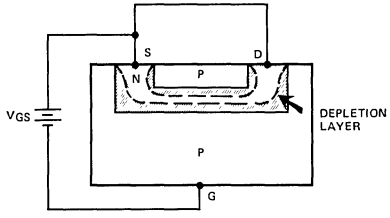
(B) N-channel FET working in saturation retion (V_{GS} = 0)



(C) Idealized output characteristic for V_{GS} = 0.

Figure 3

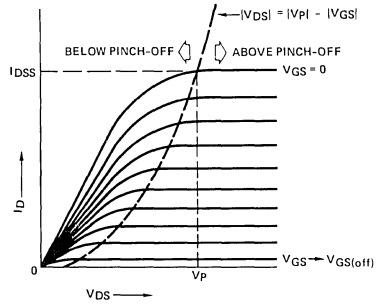
In Figure 4, consider the case where $V_{DS} = 0$, and where a negative voltage V_{GS} is applied to the gate. Again, a depletion layer has built up. If a small value of V_{DS} were now applied, this depletion layer would limit the resultant channel current to a value lower than would be the case for $V_{GS} = 0$. In fact, at a value of $|V_{GS}| \geq |V_P|$ the channel current would be almost entirely cut off. This cutoff voltage is referred to as the gate cutoff voltage, and may be expressed by the symbol V_P or by $V_{GS(off)}$. V_P has been widely used in the past, but $V_{GS(off)}$ is now more commonly accepted since it eliminates the ambiguity between gate cut-off and drain pinch-off. $V_{GS(off)}$ and V_P, strictly speaking, are equal in magnitude but opposite in polarity.



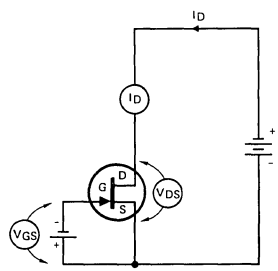
N-channel FET Showing Depletion Due To Gate-Source Voltage (V_{DS} = 0)
Figure 4

The mechanisms of Figure 3 and 4 react together to provide a family of output characteristics as shown in Figure 5A. The area below the pinchoff voltage locus is known as the triode or "below pinchoff" region; the area above pinchoff is often referred to as the pentode or saturation region. FET behavior in these regions is comparable to that of a power grid vacuum tube, and for this reason FETs operating in the saturation region may be used as excellent amplifiers. Note that in the "below pinchoff" region both V_{GS} and V_{DS} control the channel current, while in the saturation region V_{DS} has little effect and V_{GS} essentially controls I_D.

Figure 5B relates the curves of Figure 5A to the actual circuit arrangement, and shows the number of meters which may be connected to display the conditions relevant to any combination of V_{DS} and V_{GS}. Note that the direction of the arrow at the gate gives the direction of current flow for the forward-bias condition of the junction. In practice, however, it is always reverse-biased.



(A) Family of output characteristics for N-channel FET



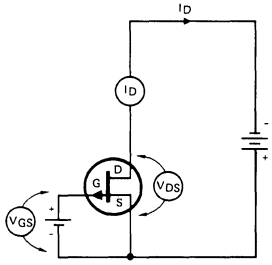
(B) Circuit arrangement for N-channel FET

Figure 5

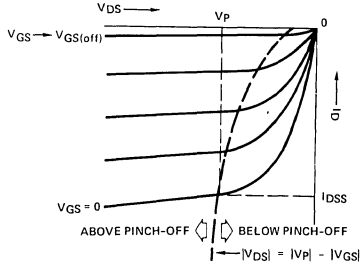
The P-Channel FET works in precisely the same way as does the N-Channel FET. In manufacture, the planar process is essentially reversed, with the acceptor impurity diffused first onto N-type silicon, and the donor impurity diffused later to form a second N-type region and leave a P-type chan-

nel. In the P-Channel FET, the channel current is due to hole movement, rather than to electron mobility. Consequently, all the applied polarities are reversed, along with their directions and the direction of current flow. Figure 6A shows the circuit arrangement for a P-Channel FET, and Figure 6B shows the output characteristics of the device. Note that the curves are shown in another quadrant than those of the N-Channel FET, in order to stress the current directions and polarities involved.

In summary, a junction FET consists essentially of a channel of semiconductor material along which a current may flow whose magnitude is a function of two voltages, V_{DS} and V_{GS}. When V_{DS} is greater than V_P, the channel current is controlled largely by V_{GS} alone, because V_{GS} is applied to a reverse-biased junction. The resulting gate current is extremely small.



(A) Circuit arrangement for P-channel FET

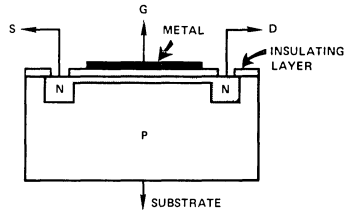


(B) Family of output characteristics for P-channel FET

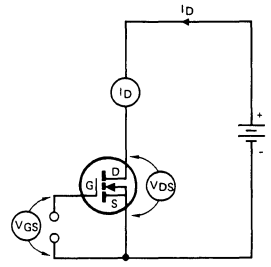
Figure 6

MOSFETs

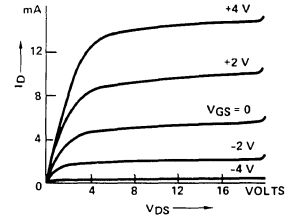
The metal-oxide-silicon FET (MOSFET) depends for its operation on the fact that it is not actually necessary to form a semiconductor junction on the channel of a FET in order to achieve gate control of the channel current. Instead, a metallic gate may be simply isolated from the channel by a thin layer of silicon dioxide, as shown in Figure 7A. Although the bottom of the insulating layer is in contact with the P-type silicon substrate, the physical processes which occur at this interface dictate that free electrons will accumulate at the interface, spontaneously forming an N-type channel. Thus a conducting path exists between the diffused N-type source and drain regions. Further, the MOSFET will behave



(A) Idealized cross-section through an N-channel depletion-type MOSFET



(B) Circuit arrangement for N-channel depletion MOSFET



(C) Family of output characteristics for the Siliconix 2N3631 N-channel depletion MOSFET

Figure 7

in a manner similar to the N-Channel junction FET when a voltage of the correct polarity is applied to the channel, as in Figure 7B.

Output characteristics of an N-Channel MOSFET are shown in Figure 7C. Because there is no junction involved, V_{GS} can be reversed without engendering a gate current; the gate may be made either positive or negative with respect to the source. Under these circumstances, still more free electrons will be attracted to the channel region, and I_D will become greater than I_{DSS}. This mode of operation is represented by the higher members of the family of ourput characteristics. Because the application of a negative gate voltage causes the channel to be depleted of free electrons – thus reducing I_D – the device just described is called a *depletion-mode* MOSFET.

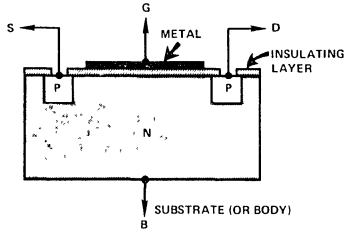
The foregoing has established that the depletion-mode MOSFET is a "normally-ON" device: when $V_{GS} = 0$, a conducting path exists between source and drain. In many circuits a "normally-OFF" device would be useful, a condition which leads to the concept of an *enhancement-mode* MOSFET. In the latter device, an increasing voltage applied to the gate will enhance channel conduction, and depletion will never occur, I_D being zero when $V_{GS} = 0$.

A P-Channel enhancement-mode MOSFET is shown in Figure 8. Here, an acceptor impurity has been diffused into an N-type substrate to form P-type source and drain regions. No conducting channel exists between the source and the drain, because no matter how the drain-source voltage is applied one of the PN junctions will always be reverse-biased. On the other hand, if a negative voltage is applied to the gate, a field will be set up in such a direction as to attract holes into the upper layer of the substrate and produce a P-type channel. A family of output characteristics for a typical Siliconix MOSFET (3N163) is shown in Figure 8C. The idealized cross-section illustrated in Figure 8A may be used to show how the characteristics of Figure 8C come about. Refer to Figure 9 for an extension of this phenomenon.

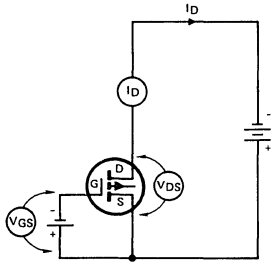
If a constant (negative) gate voltage, ($V_{GS(K)}$) is applied, then an essentially-uniform P-Channel depletion layer will be induced, as in Figure 9A. If a negative drain voltage is applied, then current, I_D, will flow through the drain. As $|V_{DS}|$ increases, I_D also increases. However, the voltage between the drain and the gate decreases, so that the thickness of the channel at the drain end is reduced as in Figure 9B. Therefore, the relationship of I_D versus V_{DS} will eventually reach a limiting value when $V_{DS} = V_{GS}$, and the channel becomes pinched off. This condition is shown in Figure 9C.

Different values of V_{GS} give rise to limiting values of I_D, so that the characteristic family of output curves which was shown in Figure 8 is realized. Characteristics of depletion-mode MOSFETs also come about for the same reason, except that members of the output characteristics family also exist for V_{GS} values of zero or reversed polarity. The P-Channel enhancement-mode MOSFET is currently the most popular member of the FET family and is in fact the basic element in many LSI integrated circuits.

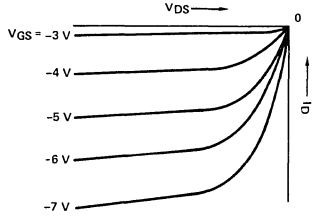
In principle, it is possible to manufacture the remaining two members of the MOSFET family, the P-Channel depletion-mode and the N-Channel enhancement-mode devices. Because of the spontaneous formation of an N-Channel at a silicon/silicon-dioxide interface, the fabrication processes involved become quite difficult on a volume production basis. Much work has gone into the development of practical MOSFET processes for these devices, and N-Channel depletion-mode types are now becoming generally available.



(A) Idealized cross-section through a P-channel enhancement MOSFET

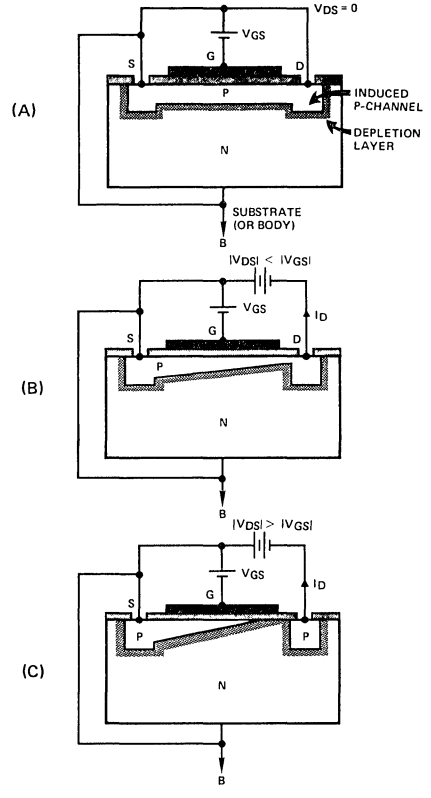


(B) Circuit arrangement for P-channel enhancement MOSFET



(C) Family of output characteristics for a P-channel enhancement MOSFET

Figure 8



Idealized approach of pinch-off,
(A) $V_{DS} = 0$, (B) $|V_{DS}| < |V_{GS}|$, (C) $|V_{DS}| > |V_{GS}|$

Figure 9

FET Characteristics

The FET enjoys certain inherent advantages over bipolar transistors because of the unique construction and method of operation of the field-effect device. These characteristics include:

- Low noise
- No thermal runaway
- Low distortion and negligible intermodulation products
- High input impedance at low frequencies
- Very high dynamic range (> 100 dB)
- Zero temperature coefficient Q point
- Junction capacitance independent of device current

The transfer function of a FET approximates to a square-law response, and the second and higher-order derivatives of g_m are near zero; thus strong second and negligible higher-order harmonics are produced. Intermodulation products are extremely low.

The input impedance of a FET is simply the impedance of a reverse-biased PN junction, which is on the order of 10^{10} to 10^{12} Ω. In practice, the input impedance is limited by the value of the shunt gate resistor used in a self-bias common-source circuit configuration. At RF frequencies, the input impedance drop is proportional to the square of the frequency; for example, in a 2N4416 FET, the input impedance would be 22K Ω at 100 MHz. Also, the input susceptance increases linearly with frequency, since it is a simple parasitic capacitance.

The FET has very high dynamic range, in excess of 100 dB. Thus it can amplify very small signals because it produces very little noise, or it can amplify very large signals because it has negligible intermodulation distortion products. It also has a zero temperature coefficient bias point (zero TC point) at which changes in temperature do not change the quiescent operating point.

Junction FET capacitances are more constant over wide current variation than are the same parameters in a bipolar device. This inherent stability allows high-frequency (VHF through L-band) oscillators to be built which are far more stable than oscillators using low-frequency crystals and multiplier stages.

FET Terminology and Parameters

Any introduction to the nature, behavior, and applications of field-effect transistors requires that certain questions be answered on FET electrical quantities and parameters – in particular, the most important parameters, and the means by which they can be measured. The following discussion will define specific FET parameters and their associated subscript notations, and present basic test circuits and results.

Major parameters include:

- I_{DSS} – Drain current with the gate shorted to the source
- $V_{GS(off)}$ – Gate-source cutoff voltage
- I_{GSS} – Gate-to-source current with the drain shorted to the source
- BV_{GSS} – Gate-to-source breakdown voltage with the drain shorted to the source
- g_{fs} – Common-source forward transconductance
- C_{gs} – Gate-source capacitance
- C_{gd} – Gate-drain capacitance

Special attention should be given to the subscript "s" because it has two different meanings and three possible uses. In FET notations, an "s" for the first or second subscript identifies the source terminal as a node point for voltage reference or current flow. However, when using triple subscript notation, an "s" for the third subscript does not refer to the FET source terminal. It is an abbreviation for "shorted", and signifies that all terminals not designated by the first two subscripts must be tied together and shorted to the common terminal, which is always the second subscript. Therefore, the term I_{GSS} refers to the gate-source current with the drain tied to the source.

Because of the typical low input and output admittance of the FET, four-pole admittance equations are commonly used to describe electrical characteristics of the FET:

$$I_1 = Y_{11}\ V_{11} + Y_{21}\ V_{22} \tag{1}$$

When Y_{11}, Y_{21}, Y_{12} and Y_{22} are defined as the input, reverse transfer, forward transconductance, and output admittances respectively, Equation 1 reduces to

$$\begin{aligned} i_1 &= y_i\ v_{11} + y_r\ v_{22} \\ i_2 &= y_f\ v_{11} + y_o\ v_{22} \end{aligned} \tag{2}$$

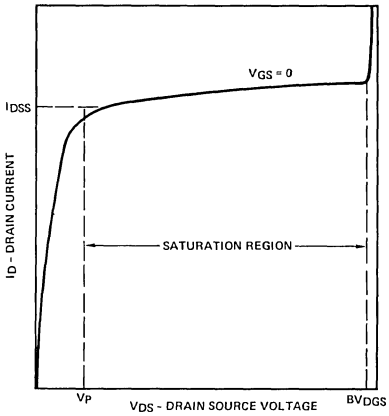
For a three-lead FET, 11 usually corresponds to the gate-source terminal and 22 corresponds to the drain-source terminal (i.e., the device is connected in the common-source mode). Thus

$$\begin{aligned} i_i &= y_{is}\ v_{gs} + y_{rs}\ v_{ds} \\ i_o &= y_{fs}\ v_{gs} + y_{os}\ v_{ds} \end{aligned} \tag{3}$$

Here, the second subscript for the y parameters designates the source lead as the common or ground terminal.

I_{DSS} – Drain Current at Zero Gate Voltage (I_D at $V_{GS} = 0$)

By itself, I_{DSS} merely refers to the drain current that will flow for any applied V_{DS} with the gate shorted to the source. However, when a particular value for V_{DS} is given, equal to or greater than V_P (see Figure 10), I_{DSS} indicates the drain saturation current at zero gate voltage. Some FET data sheets label I_{DSS} for V_{DS} greater than V_P as $I_{D(on)}$.



FET Characteristic at $V_{GS} = 0$
Figure 10

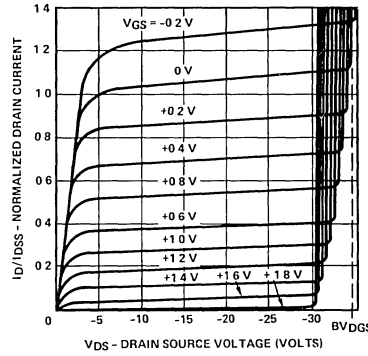
$V_{GS(off)}$ – Gate-Source Cutoff Voltage

The resistance of a semiconductor channel is related to its physical dimensions by $R = \rho L/A$, where

ρ = resistivity
L = length of the channel
A = W x T = cross-sectional area of channel

In the usual FET structure, L and W are fixed by device geometry, while channel thickness T is the distance between the depletion layers. The position of the depletion layer can be varied either by the gate-source bias voltage or by the drain-source voltage. When T is reduced to zero by any combination of V_{GS} and V_{DS}, the depletion layers from the opposite sides come in contact, and the a-c or incremental channel resistance, r_{DS}, approaches infinity. As earlier noted, this condition is referred to as "pinch-off" or "cutoff" because the channel current has been reduced to a very thin sheet, and current will no longer be conducted. Further increases in V_{DS} (up to the junction reverse-bias breakdown) will cause little change in I_D. Accordingly, the pinch-off region is also referred to as the pentode or "constant-current" region.

In Figure 10, pinch-off occurs with $V_{GS} = 0$. In Figure 11, V_{GS} controls the magnitude of the saturated I_D, with increases in V_{GS} resulting in lower values of constant I_D, and smaller values of V_{DS} necessary to reach the "knee" of the curve. The current scale in Figure 11 has been normalized to a specific value of I_{DSS}.



FET I_D vs V_D Output Characteristics
Figure 11

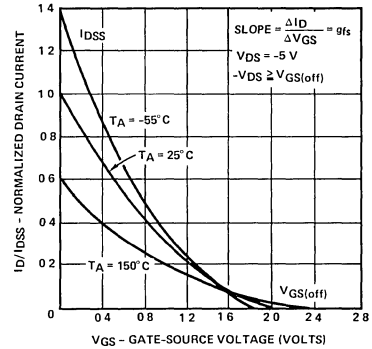
The knee of the curve is important to the circuit designer because he must know what minimum V_{DS} is needed to reach the pinch-off region with $V_{GS} = 0$. When appropriate bias voltage is applied to the gate, it will pinch off the channel so that no drain current can flow; V_{DS} has no effect until breakdown occurs. The specific amount of V_{GS} that produces pinch-off is known as the gate-source cutoff voltage, $V_{GS(off)}$.

$V_{GS(off)}$ Test Procedure

Although the magnitude of $V_{GS(off)}$ is equal to the pinch-off voltage, V_P, defined by the pinch-off knee in Figure 10, rapid curvature in the area makes it difficult to define any precise point as V_P. Taking a second derivative of V_{DS}/I_D would yield a peak corresponding to the inflection point at the knee, which approximates V_P. However, this is not a simple measurement for production quantities of devices. A better measure is to approach the cutoff point of the I_D versus V_{GS} characteristic. This is easier than trying to specify the location of the knee of the I_D versus V_{DS} output characteristic.

A typical transfer characteristic I_D versus V_{GS} is shown in Figure 12. The curve can be closely approximated by

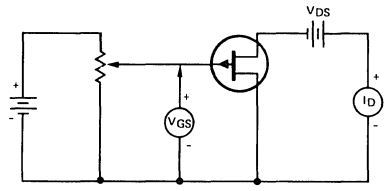
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 \qquad (4)$$



Typical I_D vs V_{GS} Transfer Characteristic
Figure 12

Equation 4 and Figure 12 indicate that at $V_{GS} = V_{GS(off)}$, $I_D = 0$. In a practical device, this cannot be true because of leakage currents. If I_D is reduced to less than 1 percent of I_{DSS}, V_{GS} will be within 10 percent of the $V_{GS(off)}$ value indicated by Equation 4. If I_D is reduced to 0.1 percent of I_{DSS}, the indicated $V_{GS(off)}$ error will be reduced to about 3 percent. For a true indication of $V_{GS(off)}$, and a realistic picture of the parameters of Figure 12, care must be taken that leakage currents do not result in an error in the $V_{GS(off)}$ reading. Typically, at room temperature, 1 percent of I_{DSS} is still well above leakage currents but is low enough to give a fairly accurate value of $V_{GS(off)}$.

A typical circuit for measuring $V_{GS(off)}$ is shown in Figure 13. At $V_{GS} = 0$, the value of I_{DSS} can be measured. Then, by increasing V_{GS} until I_D is 0.01 percent of I_{DSS}, the value of $V_{GS(off)}$ is obtained. From a production standpoint, it is more convenient to specify I_D at some fixed value (such as 1 nA), rather than as a certain percentage of I_{DSS}. Thus a pinchoff voltage specification may be given as indicated in Table I.



Circuit for Measuring $V_{GS(OFF)}$
Figure 13

Table I
Typical Pinch-Off Voltage Specification

Characteristic		Min	Max	Units
$V_{GS(off)}$	Gate-source pinch-off voltage of $V_{DS} = -5$ V, $I_D = -1$ μA	1	4	Volts

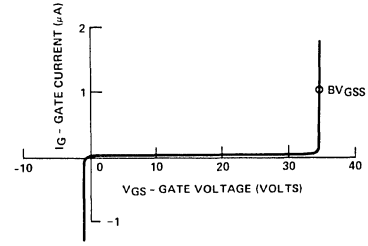
Another method which provides an indirect indication of the maximum value of $V_{GS(off)}$ is shown in Table II. The characteristic specified is $I_{D(off)}$, whereas the parameter of interest is $V_{GS} = 8$ volts. The specification does say that the maximum $V_{GS(off)}$ is approximately 8 volts, but no provision is made for stating a *minimum* $V_{GS(off)}$, as was done in Table I. Therefore, another test must be made if $V_{GS(off)\ (min)}$ is to be specified.

Table II
Indication of Maximum V_P

Characteristic		Test Conditions	Min	Max	Unit
$I_{D(off)}$	Pinch-off drain current	$V_{DS} = -12$ V, $V_{GS} = 8$ V		-10	μA

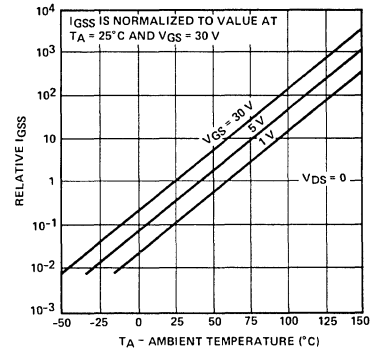
I_{GSS} – Gate-Source Cutoff Current

The input gate of a P-Channel FET appears as a simple PN junction; thus the input d-c input characteristic is analogous to a diode V-I curve, as is shown in Figure 14.



P-Channel FET Input Gate Characteristic
Figure 14

In the normal operating mode, with V_{GS} positive for a P-Channel device, the gate is reverse-biased to a voltage between zero and $V_{GS(off)}$. This results in a d-c gate-source resistance which is typically more than 100M Ω. The gate current is both voltage- and temperature-sensitive. Figure 15 shows this relationship for I_{GSS} versus temperature and V_{GS}.



I_{GSS} vs Temperature
Figure 15

If the gate-source junction becomes forward-biased, (negative voltage in a P-Channel device) or if V_{GS} exceeds the reverse-bias breakdown for the junction, the input resistance will then become very low.

The FET is normally operated with a slight reverse bias applied to the gate-source; hence a good measure of the d-c input characteristic is to check the gate current at a value of gate-channel voltage that is below the junction breakdown rating. In device evaluation, there are three common measurements of gate current: I_{GDO}, I_{GSO}, and the combined measurement I_{GSS}. These measurement circuits are shown in Figure 16.

The question is, should I_{GDO} and I_{GSO} be measured separately, or will one measurement of I_{GSS} suffice? One thing is certain: $I_{GSO} + I_{GDO} > I_{GSS}$, because the drain and the source are not completely isolated. They are, in fact, electrically connected via channel resistance. For most FETs, if V_G is greater than $V_{GS(off)}$, the difference between $(I_{GSO} + I_{GDO})$ and I_{GSS} is small; therefore, the measurement of I_{GSS} is a realistic means of controlling both I_{GDO} and I_{GSO}.

In a circuit, V_{GD} may be biased between zero and BV_{GDS}, while V_{GS} will be between zero and $V_{GS(off)}$: therefore, I_G is not necessarily the same as I_{GSS}.

BV_{GSS} – Gate-Source Breakdown Voltage

FET input terminals have been previously described as having NP or PN junctions, depending on the channel material. As such, the junction breakdown voltage is a necessary parameter.

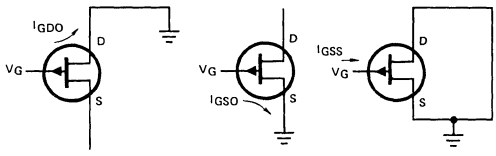
A useful equivalent circuit for a FET is the distributed constant network shown in Figure 17, for a P-Channel FET. If an N-Channel device is being evaluated, the diodes would be reversed. In most applications, the gate-drain voltage is greater than the gate-source voltage; thus the gate-drain breakdown rating is most important. However, it is also possible to consider the gate-source junction breakdown and the apparent drain-source breakdown (i.e., in Figure 17, when a high negative voltage is applied from drain to source, CR_1 will break down while CR_n becomes forward-biased).

Some device manufacturers use a BV_{GDO} rating, which means they are only checking diode CR_1. A better method is to use a BV_{GSS} rating (gate-source breakdown with the drain shorted to the source), because it checks both CR_1 and CR_n, in addition to exposing the *weakest* breakdown path along the entire gate-channel junction. The BV_{GSS} test also allows the user to interchange source and drain lead connections without worry about device breakdown ratings.

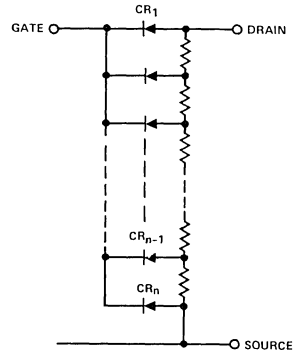
Admittedly, a BV_{GSS} test will reject some units which might pass a BV_{GDO} test; the number rejected, however, will be insignificant compared to the advantage of providing symmetrical operation.

Test Procedures for BV_{GSS}

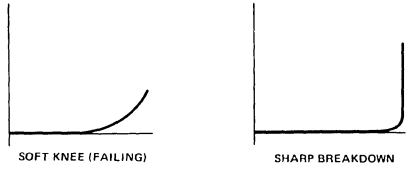
Junctions may break down softly or sharply; junctions with soft knee breakdown are undesirable. Without examining each individual unit on a curve tracer, devices with a soft knee may be eliminated by selecting a low current level for breakdown measurement (see Figure 18).



Three Common Measurements of Gate Current
Figure 16



A Useful FET Equivalent Circuit
Figure 17



Examples of Soft Knee and Sharp Knee Breakdown
Figure 18

g_{fs} – Transconductance

Transconductance, g_{fs}, is a measure of the effect of gate voltage upon drain current:

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}, \quad V_{DS} = \text{constant} \tag{5}$$

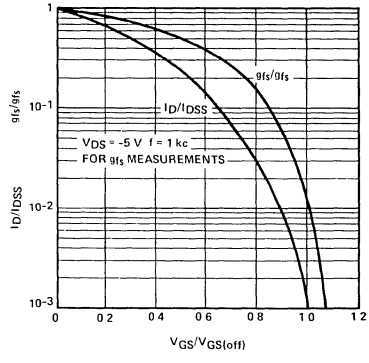
The interrelation of g_{fs} to the parameters I_{DSS} and $V_{GS(OFF)}$ should be noted. Equations 4, 6 and 7 describe the value of I_D and g_{fs} in a FET for any value of V_{GS} between zero and $V_{GS(OFF)}$.

$$g_{fs} = g_{fso}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) \tag{6}$$

$$g_{fso} = -\frac{2I_{DSS}}{V_{GS(off)}} \tag{7}$$

where g_{fso} is the value of g_{fs} at $V_{GS} = 0$ and I_{DSS} is the value of I_D at $V_{GS} = 0$. With these equations, the value of g_{fs} can be calculated with a fair degree of accuracy (20 percent) if I_{DSS} and $V_{GS(off)}$ are known.

Figure 19 shows normalized curves for I_D and g_{fs} as functions of V_{GS} in a P-Channel FET. These curves were obtained from actual measurements on typical diffused channel FETs, such as the 2N2608. The curves agree very well with Equations 4 and 6 until $V_{GS(off)}$ is approached. For these curves, $V_{GS(off)}$ was assumed to be the value of V_{GS} where $I_D/I_{DSS} = 0.001$.



Normalized Curves for I_D and g_{fs} as Functions of V_{GS}
Figure 19

The drain current of a JFET operating in the triode (below pinch-off) region can be accurately predicted by using Equation 8, where

$$I_D/\text{triode} = I_{DSS}\left(\frac{V_{DS}}{V_{GS(off)}}\right)^{1/2} \tag{8}$$

Specifications for g_{fs} are shown in Tables III and IV. Note that there is a difference in the test conditions specified for the N-Channel 2N3823 and the P-Channel 2N3329. The gate voltage for the 2N3823 is established as zero. This means that g_{fs} is measured at $I_D = I_{DSS}$, as in Table III.

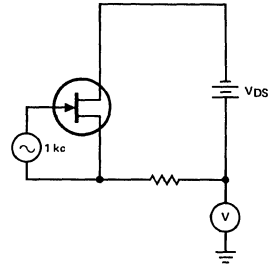
Table III (2N3823)

Characteristic	Test Conditions	Min	Max	Unit
g_{fs} Small-signal common-source forward transconductance	V_{DS} = 15 V, V_{GS} = 0, f = 1 kHz	3,500	6,500	μmho

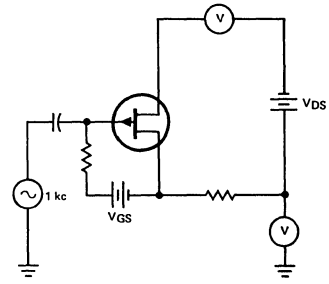
Table IV (2N3329)

Characteristic	Test Conditions	Min	Max	Unit
Y_{fs} Common-source forward transfer admittance	V_{DS} = −10 V, I_D = −1 mA f = 1 kHz		20	μmho

The test conditions shown in Table IV specify a certain value for I_D (−1 mA for the 2N3329). This means that for each unit tested, V_{GS} is adjusted until I_D equals the specified value. The conditions specified in Table III simplify testing of the g_{fs} parameter by eliminating the necessity of adjusting V_{GS}. Figures 20 and 21 show typical test setups for the two methods.



Test Circuit for g_{fs} with $V_{GS} = 0$
Figure 20



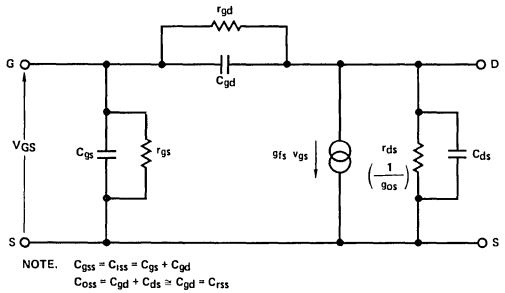
Test Circuit for g_{fs} with I_D Specified
Figure 21

Junction FET Capacitances

Associated with the junction between the gate and the channel of a FET is a capacitance whose value and geometric distribution are functions of the applied voltages V_{GS} and V_{DS}. Because of the complexity of dealing with such a distributed capacitance, a simplification is made so that two lumped capacitances, C_{gs} and C_{gd}, exist between the gate and the source and drain, respectively. (A much smaller capacitance, C_{ds}, also exists between the drain and the source, stemming mainly from the device package; this header capacitance is small enough so that it can be ignored for most purposes.)

Data sheets quote C_{gs} and C_{gd} (or other capacitances from which they may be derived) for specified operating conditions. Occasionally, graphs are included which show the variations of C_{gs} and C_{gd} as the result of changing conditions of V_{DS}, V_{GS} and temperature. If these data are not presented, an estimate of inter-electrode capacitance values may be made by assuming that these values vary inversely with the square root of the bias voltage. The temperature variations will be very small, because they depend on the −2.2 mV/°C change in junction potential difference.

Assuming that the FET is properly biased – that is, that the d-c conditions are met by the external circuitry – it is possible to construct an incremental equivalent circuit from which the small-signal or a-c performance may be predicted. Such an equivalent circuit is shown in Figure 22.



Incremental Equivalent Circuit for the Junction FET
Figure 22

The equivalent capacitance from the gate to the source, C_{gs}, is shunted by a very large input resistance, r_{gs}, with both of these parameters being characteristic of a reverse-biased junction. Similarly, the equivalent capacitance from the gate to the drain is shunted by the very large resistance r_{gd}. (For most purposes, r_{gs} and r_{gd} may be neglected, and the gate impedance of the FET treated as pure capacitance). At the drain side of the equivalent circuit the small capacitance C_{ds} – which stems from the header material – is shunted by the incremental channel resistance, r_{ds}. This resistance is capable of wide variations, depending on bias conditions. Since the equivalent circuit is fundamentally relevant to the pinch-off or saturated condition, r_{ds} will be on the order of megohms.

The incremental channel current is given by the transconductance, g_{fs}, multiplied by the incremental gate voltage. For the small signal, v_{gs}, this is manifested in the equivalent circuit by the current generator $g_{fs}v_{gs}$. Notice that the conventional direction of flow of this current is such that i_d flows into the FET, in a "positive" direction.

Many circuits can be designed around the equivalent circuit for the junction FET. The actual values of g_{fs} adn r_{ds} can be measured as previously mentioned; there remains only the requirement to establish the methods of determining C_{gs} and C_{gd}.

First, assume that the FET is in operation and that the drain is connected to the source via a large capacitor, i.e., the drain and source are short-circuited to a-c. Under these circumstances, a capacitance measurement between the gate and the source will give

$$C_{gss} \text{ (or } C_{iss}) = C_{gs} + C_{gd} \tag{9}$$

Second, assume that the gate and source are short-circuited to a-c in a similar manner. A capacitance measurement between the drain and the source will now give

$$C_{dss} \text{ (or } C_{oss}) \approx C_{gd} \tag{10}$$

The alternative symbols C_{iss} and C_{oss} simply refer to measurements made at the input (gate) and the output (drain) respectively. An alternative symbol for C_{gd} is C_{rss}, which refers to the "reverse" capacitance.

In data sheets, it is customary to state (= C_{iss}) C_{gss} and C_{dss} (= C_{oss}). C_{rss} is often given in place of C_{oss} because if $C_{ds} \ll C_{oss}$, which is usually the case, then $C_{rss} \cong C_{oss}$. Equations (9) and (10) can be used in those instances where it is necessary to extract C_{gs} and C_{gd}, as in

$$C_{gs} = C_{iss} - C_{gd} = C_{iss} - C_{rss} \tag{11}$$

and

$$C_{gd} = C_{rss} \tag{12}$$

Remember that all capacitance measurements should be made at the same bias levels, since the capacitances are functions of applied voltages. To indicate the order of the capacitances to be found in a junction FET, consider the values given in the data sheet for the Siliconix E202 N-channel FET. They are given as

C_{iss} (at V_{DS} = 20 V and f = 1 MHz) = 5 pF max.

and

C_{rss} (at V_{DS} = 20 V and F = 1 MHz) = 2 pF max.

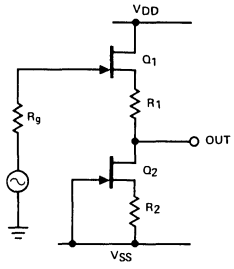
Hence, at a drain-source voltage of 20 V and a frequency of 1 MHz, C_{gs} = 5 - 2 = 3 pF maximum. Even though the FET is physically symmetrical, bias conditions have forced the capacitances to be unequal.

GENERAL APPLICATIONS FOR FETS

Applications for the versatile field-effect transistor are literally too numerous to mention. Some idea of the near-universality of the FET may be gained by considering the following circuits, all of which use FETs to perform a unique function. Because of space limitations, no attempt has been made to provide a design rationale for the specimen circuits, or to establish component values.

Dual FETs as Source Followers

Siliconix dual FETs may be used in a low-offset source follower configuration to form an impedance transformer with power gain. Such a circuit, shown in Figure 23, may be used to match a high-impedance transducer to a cable or transmission line; as an input circuit or interface for an amplifier; as a unity-gain level shifter; or as a pulse amplifier which maintains input pulse shape and d-c levels.



Low-Offset Source Follower
Figure 23

In the circuit, Q_2 forms a constant-current source which feeds Q_1. For zero offset the output is taken from the drain of Q_2. However, a non-zero-offset output may be taken from the drain of Q_1. The only other components required for the circuit are two matched resistors. To determine the values of R_1 and R_2, the value of the quiescent current must be established. This should be set to a value which gives the required g_{fs}. For maximum dynamic range at the output, the d-c output voltage is set midway between V_{DD} and V_{SS}. At the source of Q_1, the output resistance is $1/g_{fs}$. If the output is taken from the drain of Q_2 then:

$$R_o = \frac{1}{g_{fs}} + R_1 \qquad (13)$$

Drift is defined as

$$\frac{\Delta V_{GS1} - \Delta V_{GS2}}{\Delta T} \qquad (14)$$

Drift in this circuit will be according to this definition, assuming that zero temperature-coefficient resistors are used. Table V shows results obtained with several Siliconix dual FET packages. Voltage gain of the source follower is near-unity. The larger the g_{fs}, the nearer the gain approaches unity. In the circuit shown A_V is > 0.98. Changes in temperature from $-50°C$ to $+125°C$ changed the gain by $>>0.5$ dB. Frequency response is determined by the input and output time constants. If the generator impedance is increased from 50 Ω to 1K Ω, the bandwidth will fall by approximately 80%.

Table V
Temperature Drift (mV)

Device	Temperature °C				
	-60	25	65	85	125
2N5519	+ 0.2	- 4.7	- 6 5	- 7.2	- 8.4
U235	+12.8	+16.4	+18 1	+18.7	+19.8
U257	+11.3	+12.5	+12 7	+12.7	+12.7

FETs as Analog Switches

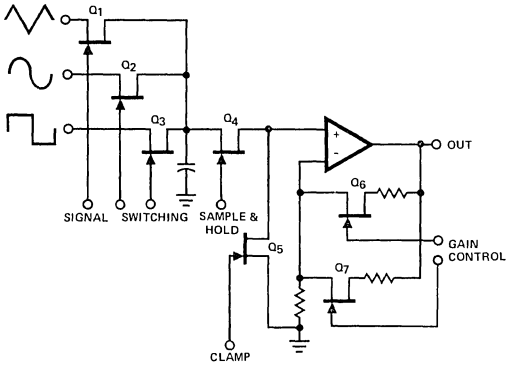
The FET is in effect a conductor whose cross-sectional area may be varied by the application of appropriate voltages. When the conducting area (the channel) is maximum, conductance is also maximum (minimum resistance). When the conducting area is minimum, conductance is minimum (maximum resistance). These phenomena make possible the use of FETs as analog switches. When conductance is maximum, the switch is in the ON state. When conductance is minimum, the switch is in the OFF state. At least 50 percent of all applications for FETs are for analog or digital switching. The reasons for using a transistor in place of a mechanical switch are obvious: small size for high-density packaging; remote operation, with no mechanical linkages to jam; and the inherent reliability of solid-state devices.

All of these advantages apply to bipolar transistors as well as to FETs, but the field-effect transistor offers several additional advantages. These include:

- High ON to OFF ratios
- Bilateral operation for large analog signal swing
- No offset current – may be used to switch microvolt signals without error
- Low power drive due to voltage-control action

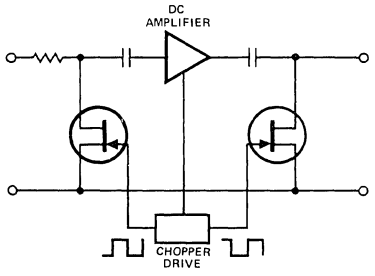
Two types of FETs are used for switching applications. These include the depletion-mode junction FET, and the enhancement-mode MOSFET. The junction FET offers lowest ON resistance and most accurate signal handling with a minimum of distortion. The JFET operates as a normally-ON device. The MOSFET is normally OFF and offers the advantage of simple drive circuitry by trading off increased ON resistance and conductivity modulation with signal swing.

FETs fill literally hundreds of switching applications, and several of the more common switching functions are shown in the circuit in Figure 24. Q_1 through Q_3 perform as analog switches, and Q_4 is a sample-and-hold switch. Q_5 functions as a signal clamp with zero reference, and Q_6-Q_7 are in a gain switching circuit.



FET Switching Circuits
Figure 24

Another major use of FET switches is to replace mechanical and photochoppers in chopper-stabilized amplifiers. The FET offers the advantages of long life (as opposed to mechanical choppers) and an ON/OFF ratio which a photochopper would be hard-pressed to meet. Figure 25 shows two FETs connected as the modulator and demodulator of a chopper-type d-c amplifier, driven in anti-phase so as to simulate the action of the double-pole electromechanical chopper.



DC Amplifier Using FET Choppers
Figure 25

Because of the widespread acceptance of the FET as a switch, the device has been incorporated into many types of hybrid and monolithic (single chip) integrated circuits. Not only can the user obtain an array of devices (as in Q_1-Q_3 in Figure 24), but he also has available complete circuits with drivers and FET switches combined for maximum switching efficiency and speed. These integrated circuits come in dozens of configurations, ranging from a replacement for a single-pole, single-throw mechanical switch to multi-channel multiplex switches for use in many data processing and communications systems.

FETs as Voltage-Controlled Resistors

A voltage-controlled resistor (VCR) may be defined as a three-terminal variable resistor where the resistance value between two of the terminals is controlled by a voltage potential applied to the third. A JFET may be defined as a field-controlled majority carrier device where the conductance between the source and drain channels is modulated by a transverse electric field. The field is controlled by a combination of gate-to-source bias voltage, V_{GS}, and the net drain-to-source voltage, V_{DS}.

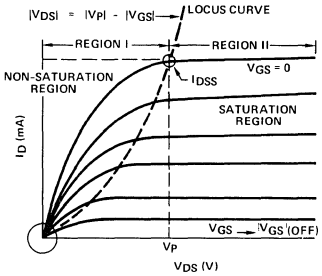
Under certain operating conditions, the channel of a JFET will behave as an almost pure ohmic resistor, whose value is the function of the gate voltage, V_{GS}. Maximum drain-to-source current, I_{DSS}, will exist when the gate-to-source voltage is equal to zero volts ($V_{GS} = 0$). If the negative gate voltage is increased to a point where the FET is no longer conductive, the cut-off voltage level, $V_{GS(off)}$ is reached. Thus the device can function as a voltage-controlled resistor.

Figure 26A details the typical operating conditions of a FET. As has been observed, most amplification or switching operations of FETs occur in the constant-current (saturated) region, shown as Region II. An inspection of Region I (the unsaturated or pre-pinch-off area) will reveal that the effective slope indicative of conductance across the channel from drain to source is different for each value of bias gate voltage. The slope is relatively constant over a range of applied drain voltages, so long as the gate voltage is also constant and the drain voltage is low. Hence the ability of a FET to serve as a voltage-variable resistor.

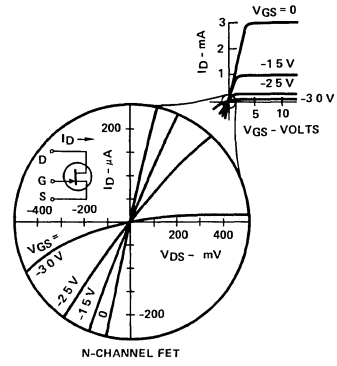
The unique resistance-controlling properties of FETs can be deduced from Figure 26B, which is an expanded-scale plot of the encircled area in the lower left-hand corner of Figure 26A. The output characteristics all pass through the origin, near which they become almost straight lines so that the incremental value of channel resistance, r_{ds}, is essentially the same as that of d-c resistance, r_{DS}, and is a function of V_{GS}. Figure 26C extends these FET characteristics to a comparison with the performance of four fixed resistors. Note the pronounced similarity between the two types of devices.

FETs are ideal for use as VCRs in applications requiring high reliability, minimum component size, and circuit simplicity. The FET VCR will conveniently replace numerous elements of conventional resistance-control systems, such as servomotors, potentiometers, idler pulleys, and associated linkage. FET power consumption is minimal, packages are very small, and cost comparisons with conventional control schemes are most favorable.

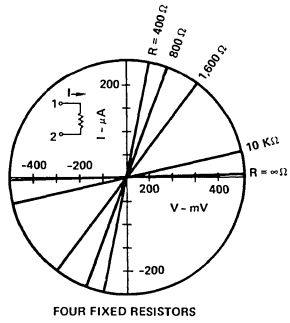
A variety of FETs in VCR circuits are shown in Figure 27 through 34.



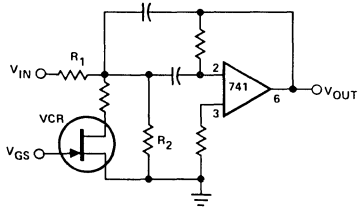
Behavior of a FET as a VCR
Figure 26A



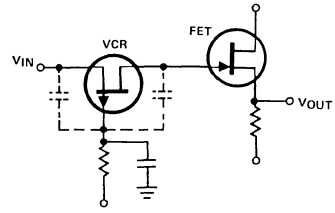
Behavior of a FET as a VCR
Figure 26B



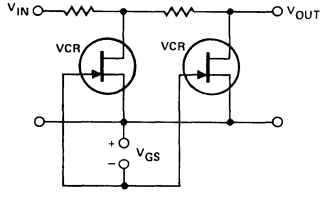
Behavior of a FET as a VCR
Figure 26C



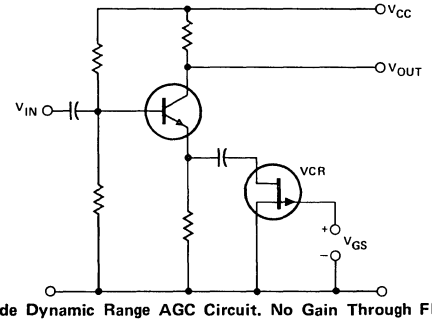
Voltage-tuned Filter Octave Range With Lowest Frequency at JFET $V_{GS(OFF)}$ and Tuned by R_2. Upper Frequency is Controlled by R_1.
Figure 27



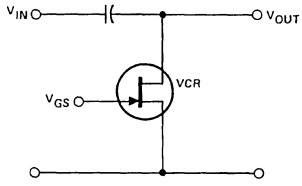
Tunable Low-Pass RC Pi-Filter. Voltage-Tunable Over 100:1 Range. Frequency Range Changed By Shunting Gate And Source With Fixed Capacitors
Figure 28



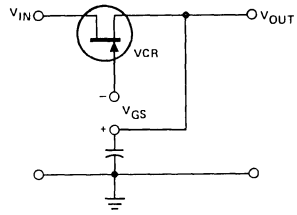
Cascaded VCR Attenuator
Figure 29



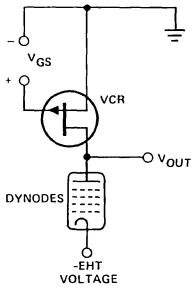
Wide Dynamic Range AGC Circuit. No Gain Through FET With Distortion Proportional to Input Signal Level.
Figure 30



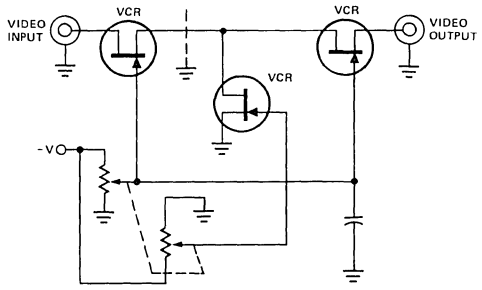
VCR Phase Advance Circuit
Figure 31



VCR Phase Retard Circuit
Figure 32



P-Channel VCR Photomultiplier Load. Required Low Photomultiplier Anode Current (Usually <1 μA) Implied That VCR Will Always Perform In Linear Region Near Origin.
Figure 33



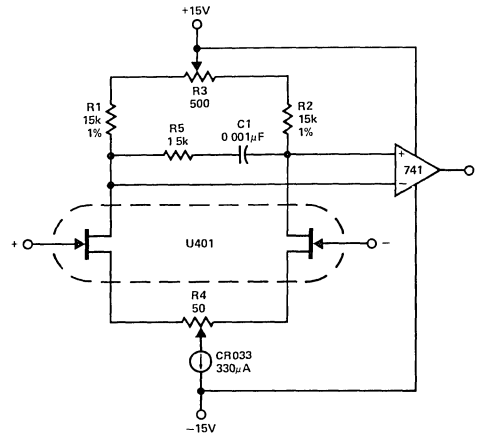
Voltage Controlled Variable Gain Amplifier. The Tee Attenuator Provides For Optimum Dynamic Linear Range Attenuation.
Figure 34

Dual FETs in FET Input Op Amps

A high quality FET input op amp may be constructed with a dual FET acting as a preamp for a standard bipolar op-amp such as a 741. Using a dual FET allows good thermal tracking, while biasing the FETs near their zero drift point, I_{DZ} (equal to the drain current when $V_{GS} = V_{GS(off)} - 0.63$ V), results in low drift. Many dual FETs designed for low drift preamp applications have an I_{DZ} near 200 μA, so this makes a good design value.

Figure 35 shows a typical FET input op amp. The U401 is a monolithic dual JFET with a maximum initial offset of 5 mV and a maximum offset drift of 10 μV/°C. Both of these parameters may be improved by trimming the circuit. R_4 should be used to null out initial offset, while drift can be minimized by adjusting R_3. (This requires heating the amplifier.)

The CR033 is an N-Channel JFET internally connected as a current source. It provides 330 μA of current with an extremely low temperature coefficient of 0.025%/°C (typical). The drain current per side of the U401 is therefore 165 μA, which is sufficiently close to the 200 μA design ideal. R_1 and R_2 should have low temperature coefficients to minimize their influence in the circuit. A good choice is 1% low TC metal film.



A JFET Input Operational Amplifier
Figure 35

CHAPTER 7

RF APPLICATIONS FOR FETs

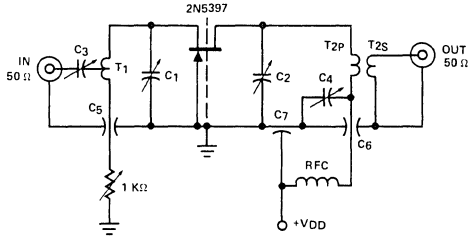
FETs are ideal in RF applications since they have an inherently good high frequency response and their square law transfer characteristic results in low harmonic and intermodulation distortion. The following is a potpourri of RF circuits which have been developed.

UHF FET for Common-Gate 450 MHz Amplifier

High-performance FETs may be used to advantage in UHF amplifiers because of the inherent dynamic range, low noise, and excellent reverse isolation characteristics of the devices

when used as active elements. Circuits employing a common-gate, tuned-source, tuned-drain configuration require no neutralization because reverse isolation is a function of the drain-source capacitance and output conductance. Typical C_{ds} for a FET such as the Siliconix 2N5397 is less than 0.01 pF, and therefore capacitive feedback through the device is very low.

The UHF amplifier in Figure 36 is designed for a 450 MHz center frequency, with a 3 dB bandwidth of 6 MHz. The amplifier stage is compatible with a 50 Ω system. It may be used as a receiver front-end, with excellent reverse isolation characteristics which reduce local oscillator radiation from the antenna. Applications include fixed or mobile service, aeronautical navigation, UHF-TV, police and fire communications, paging systems, and amateur radio. The amplifier uses a Siliconix 2N5397 N-Channel junction FET.



C1-2 - 0 8 - 10 pF JFD model MVM 010W
C3-4 - 8 - 35 pF Erie series 539-002D
C5-6 - 5,000 pF Erie (2443-000)
C7 - 1,000 pF ALLEN-BRADLEY type FA5C
RFC - 33 μH MILLER type (9230-30)
T1 - one turn, #16 copper wire, ¼" I D (Air Core) tapped 1/3 turn from top
T2P - one turn, #16 copper wire, ¼" I D (Air Core)
T2S - one turn, #16 copper wire, ¼" I D (Air Core)

Common-Gate 450 MHz Amplifier
Figure 36

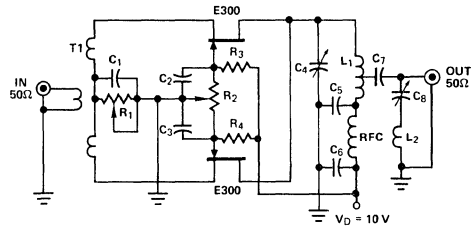
A FET Frequency Doubler

The transfer curve of the FET approximates to a square-law response, as noted earlier, and produces a strong second and negligible higher-order harmonic output. The FET is thus useful in frequency-doubler circuits.

In the past, most solid-state frequency multipliers have employed Schottky-barrier (hot carrier) diodes in balanced full-wave circuits, primarily because of the low threshold state of the Schottky devices. These achieve only about 8% multiplying efficiency. Further, the Schottky diodes have expotential transfer characteristics which require multiple traps to suppress the higher harmonics and maintain output waveform purity.

In contract, a FET frequency multiplier circuit requires only one trap for effective harmonic suppression, and operates up to 100% efficiency.

The multiplier circuit shown in Figure 37 uses two matched FETs as common-gate amplifiers in a balanced push-push configuration. The Siliconix E300 FETs in this application exhibit a high forward transconductance of 7,000 μmho, and can be well matched in relation to transfer curves. Matched 2N5397s are also suitable, as are dual VHF FETs such as the U257, E420 or the 2N5911. A common-gate configuration is used because the g_{ig} (common-gate impedance) of the devices closely matches the secondary impedance of available wideband transformers. The Relcom BT-9 input transformer is used because of excellent bandpass, 8:1 impedance ratio, and isolated secondary.



C1, C5, C6 – 1500 pF
C2, C3 – 1000 pF
C4 – 8 35 pF
C7 – 30 pF
C8 – 2 3-20 pF
R1 – 1KΩ
R2 – 10KΩ
R3, R4 – 220KΩ, ¼W
L1 – 4T #18 AWG, 5/16 DX 5/16 LG TAPPED 3/4T FROM COLD END
L2 – 2T #16 AWG 5/16 DX 3/16 LG
RFC – 1 2 μHy
T1 – RELCOM BT 9 50Ω IN-400CT-400Ω OUT

FET Frequency Doubler Circuit
Figure 37

The series-tuned output trap C_8L_2 increases rejection of third-order harmonics to > 70 dB. An unfiltered output would show 50 dB third-order rejection! A positive bias voltage of 0.5 V is applied to the FET gates to permit inclusion of a balance control in the circuit. The doubler exhibits a gain of about 1 dB, with +10 dBm input at 50 Ω on the primary.

Selective VHF Amplifier

Sharp selectivity of RF signals requires resonators with near-unity ratio of loaded Q to unloaded Q (Q_L/Q_U). Selectivity is dependent on the number of elemental poles (6 dB rejection/unit bandwidth), whereas insertion loss depends on the ratio of Q_L/Q_U. Field-effect transistors may be used in sharp-selectivity VHF amplifiers to avoid design problems encountered in conventional loose-coupled low-impedance circuits. In the past, these circuit compromises have involved poor impedance match and high system noise.

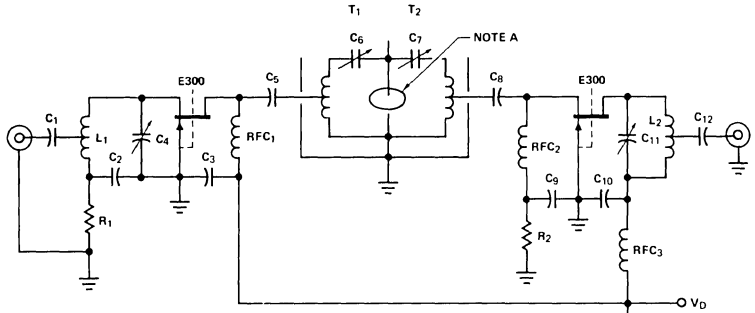
FET characteristics of high drain impedance, wide dynamic range, and excellent intermodulation product rejection mean that FETs may be used as buffers in selective VHF amplifiers. As such, they enhance selectivity and contribute to impedance match and a low noise figure, while working to preserve a near-unity Q ratio. A typical application circuit would be as a color signal booster in a fringe TV reception area.

In Figure 38, E300 FETs are used as buffers between a low-impedance 50 Ω input and a near-unity Q ratio resonator. The circuit is a conventional VHF amplifier, capacitively-coupled to a two-pole helical coil resonator. The compact resonators offer unusually-high unloaded Q, often exceeding 1,000 in the VHF spectrum. Impedance match between resonator input and output is achieved by tapping up on the helix. The amplifier is stagger-tuned to provide a 4.5 MHz (Channel 10 video) and has 15 dB gain with a noise figure < 4 dB. The amplifier is adjustable to receive a good quality color picture from Channel 10, a fringe area station located more than 100 miles from the receiver, and nestled between two strong adjacent local channels. Selectivity for other fringe area frequencies is achieved simply by tuning the amplifier to the desired fringe channel frequency.

JFETs for Ultra-Wideband UHF Amplifiers

Junction field-effect transistors may be used as active elements in multi-octave wideband distributed amplifiers with the same degree of success of earlier designs using conventional vacuum tubes and bipolar transistors, which have achieved bandwidths of several decades.

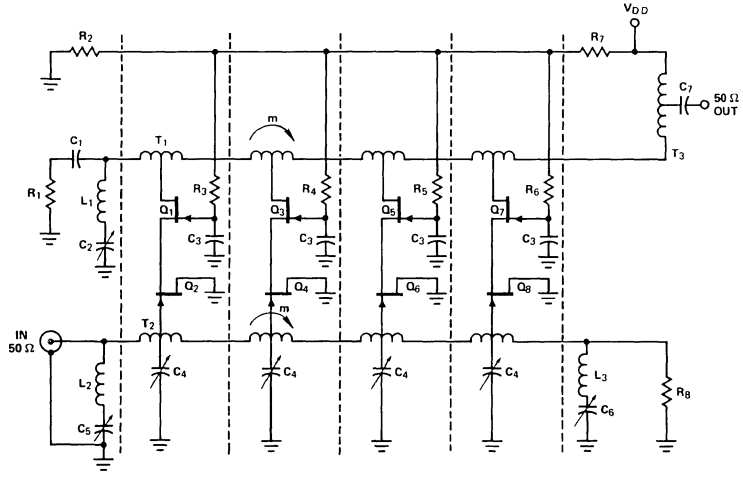
The design of distributed amplifiers basically involves the configuration chosen for the input and output transmission (delay) lines. A number of designs are possible, but the simplest is the image-parameter m-derived low-pass filter shown in Figure 39, which offers excellent group delay characteristics across a major area of the passband.



C_1	– 220 pF	$RFC_{1,2}$	– 1.1 μHy
$C_2, C_3, C_9, C_{10}, C_{13}$	– 1000 pF	RFC_3	– 2 μHy
C_4, C_{11}	– 8 – 35 pF	L_1	– 4T #18 AWG 1/8 DIA x 1/4 \ TAPPED 1 1/2 T FROM TOP
C_5	– 75 pF		
C_6, C_7	– 8 – 10 pF JFD	L_2	– 3 T #16 AWG 1/4 DIA x 1/4 \ TAPPED 1/4 T FROM COLD END
C_8	– 200 pF		
C_{12}	– 100 pF	T_1, T_2 (CH10)	– 5 1/2 T #12 AWG 5/8 I D x 1 1/4" LONG IN 1 1/4" SQ x 2" CANS TAPPED 1/2 T FROM COLD END
R_1, R_2	– 100 Ω 1/4 W		

NOTE A Inductive loop adjusted for optimum response

Selective VHF Amplifier Circuit
Figure 38



C_1, C_7, C_3 – 270 pF	R_1 300 Ω
C_2, C_5, C_6 – 8 – 10 pF	R_8 · 50 Ω
L_1 · 170 nHy	$R_2, R_3, R_4, R_5, R_6, R_7$ 10 KΩ
L_2, L_3, 12 nHy	T_1 - Broadband Toroidal Output Transformer - n = 6 1
$Q_1 \rightarrow Q_8$ · Siliconix E300	

Multi-Octave Wideband Amplifier
Figure 39

The transmission line and its characteristic impedance need not be equal between input and output, but it is important that the phase velocity of both lines be equal. For the image-parameter low-pass filter,

Cutoff Frequency: $f_c = \frac{1}{\pi\sqrt{LC}}$

Characteristic Impedance: $Z_O = \sqrt{\frac{L}{C}}$

Phase Constant: $\beta = \omega\sqrt{LC}$

The phase constant of each transmission line must match, and it is also important to establish the characteristic line impedance for convenience in matching. The two transmission lines are designed by iteration. Table VI provides typical values of inductance and capacitance for a cutoff frequency of 300 MHz. Any line selected from this group will have a matched phase constant.

Table VI

Z_o (Ω)	C (pF)	L (nHy)
50	21.2	53
75	14.1	80
100	10.6	106
200	5.4	210
300	3.5	320
450	2.4	480

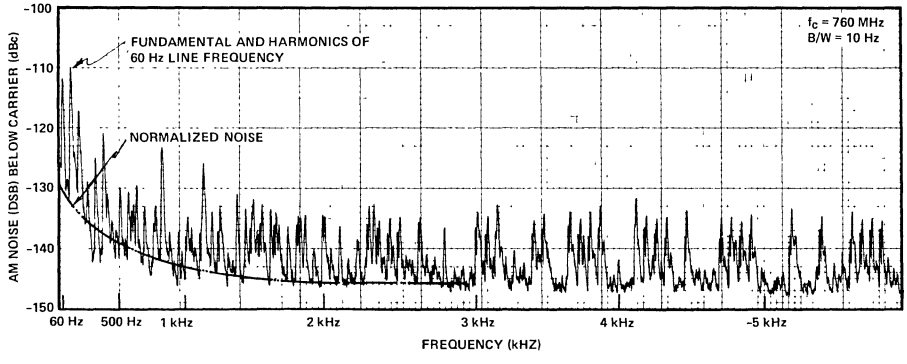
The amplifier is designed for a 50 Ω input impedance and 300 Ω drain line impedance. This value of drain line impedance assures a reasonable voltage gain, and limits the shunt transmission capacitance to the FET capacitance (C_{rss}). A broadband 6:1 output transformer allows the 300 Ω to 50 Ω match. FETs in the amplifier are arranged in cascode to insure low input conductance and good stability. Measured gain is 5.2 dB, and with two amplifiers cascaded, overall gain of 10 dB is achieved across the 50 to 300 MHz passband. Flat group delay is nearly 90% of the total passband.

High Performance FETs in Low-Noise VHF Oscillators

Most communications receivers are limited in their dynamic range because of saturation in the early stages of RF amplifiers or mixers. In advanced receivers, this limitation may be largely overcome by using parametric amplifiers and converters to achieve spectacular increases in dynamic range. Even with these innovations, certain limitations in dynamic range will remain, usually due to the heterodyning of noise sidebands which appear on the receiver local oscillator, entering the passband through strong interfering signals.

A reasonable differentiation of various types of noise may be gained from a knowledge of the Gaussian distribution of noise about an RF carrier. These types of noise are low-frequency noise (1/f); thermal noise (4kTRB); and "shot noise" (i_n), and may be identified through their relationship to the main RF carrier. Low-frequency noise predominates very close to the carrier, and becomes insignificant when displaced more than 250 Hz from the carrier. Thermal noise becomes a factor in the region from the 1/f decay point to 20 kHz from the carrier. Noise appearing beyond the 20 kHz level is known as "shot noise"; because of its relatively uniform distribution it is also referred to as "white noise."

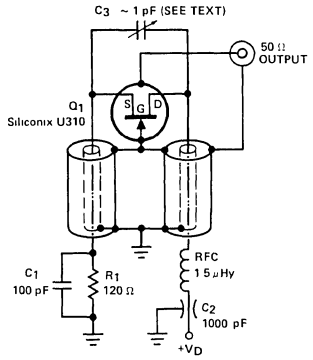
Although an oscillator tends to produce a wave that is nearly sinusoidal, there are other fluctuations present. When the energy in the frequency domain is observed on a spectrum analyzer, noise appears as a modulation phenomenon. Without a doubt, the major component of AM noise is the contribution of low-frequency noise. A graph of AM noise versus frequency removed is shown in Figure 40.



AM Noise vs Frequency Removed from the Carrier
Figure 40

When FETs are used in VHF oscillators, best performance will be obtained if the FET has high forward transconductance, if the gate is maintained at ground potential, and if a high unloaded tank Q is obtained. High transconductance is necessary to reduce effective noise resistance. The grounded gate reduces the noise voltage contributions to those of the gate leakage current and the series gate resistance. The high tank circuit Q serves as an effective filter for the sideband noise energy.

The oscillator circuit shown in Figure 41 includes a Siliconix U310 FET, which has a forward transconductance value greater than 18 mmho at zero bias (V_{GS} = 0). The oscillator consists of two coaxial resonators, one for the FET source and the other for the drain. Oscillation is achieved by capacity coupling between the two resonators; output coupling is derived from the magnetic coupling which exists at the open ends of the resonators. Best resonator Q is achieved by designing the coaxial resonators for a characteristic impedance of 75 Ω. Measured performance of the oscillator is shown in Table VII.



Oscillator Circuit
Figure 41

Table VII

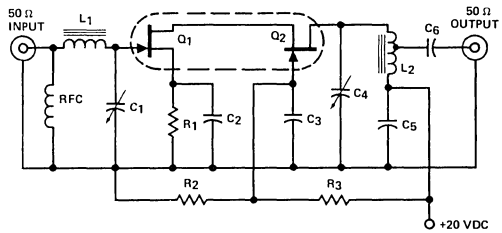
Oscillator Measured Performance at 25°C				
V_D(V)	+10	+15	+20	+25
I_D(mA)	15	16.2	18.2	21
P_{out}(dBm)	+6.6	+15.2	+18.3	+20
f (MHz)	725	742.7	754.7	762.9

Low-Cost Dual FETs in Low-Noise VHF Preamplifiers

Epoxy-encapsulated dual JFETs offer the designer the ultimate in stability and high gain in low-noise (< 1.5 dB) direct-coupled VHF cascode amplifiers. Cost-effectiveness is an attractive feature of epoxy FETs, since the price of the average epoxy device is at least 50% lower than the cost of its metal-can (TO-5 type) counterpart.

A further advantage in working with cascode-coupled amplifiers is the option offered the designer in establishing gain by AFC action, if the second gate (the output stage) is used as the control. This feature, combined with the inherent stability and high gain typical of junction FETs, results in a circuit which will outperform amplifiers which use conventional dual-gate MOS FETs, because of a substantially-lower noise figure.

In cascode circuits, it is important that the output FET have a drain saturation current, I_{DSS}, which is equal to or greater than that of the input FET, since neither device will operate with a forward-biased gate. Thus many cascode amplifiers employ complex a-c coupling techniques and used discrete (unmatched) FETs to avoid the problem. Matched I_{DSS} parameters are available in dual FETs such as the Siliconix E420, and the two transistors may be direct-coupled without encountering the forward-bias condition.



L1, - 1.7 μHy 22T #24 AWG enamel on Micrometals T50-10 toroidal core
L2 - 1.5 μHy 20T #24 AWG enamel on Micrometals T50-10 toroidal core tapped 7 turns from cold end
C1, C4 - 2-20 pF
C2, C3, C5, C6 - 0.01 μF
R1 - 390 Ω
R2 - 10K Ω
R3 - 30K Ω
Q1, Q2 - Siliconix E420
RFC - 30 μHy Delvan choke

Cascode 30 MHz Intermediate Frequency Amplifier
Figure 42

The prototype circuit shown in Figure 42 is a low-noise, high-gain IF amplifier which operates at 30 MHz in a 50 Ω system. Noise performance of the amplifier is less than 1.5 dB, and gain is in excess of 20 dB. The circuit has no critical adjustments. For maximum performance, short leads are required (point-to-point wiring is preferred). The two toroidal coil transformers should be located at right angles to one another to avoid the possibility of infringing magnetic fields and to eliminate the need for shielding to obtain stable operation. The prototype circuit is unshielded, and employs an input "el" match to transform the 50 Ω to the optimum

value of source impedance necessary to achieve the best noise figure. The E420 dual FET used in the amplifier displayed best performance with a source impedance value of 1.8K Ω. The FETs were selected at random, providing a noise figure "window" between 0.9 dB and 1.2 dB; gain was reasonably stable at 20 dB. Gain as high as 28 dB can be obtained if the tap on the output tank is removed, but shielding will probably be required for stable operation. Measured performance of the amplifier is shown in Table VIII.

Table VIII

Measured Performance	
Frequency	30 MHz
Bandwidth	5.5 MHz at 3 dB
Gain	+20 dB
Noise Figure	1.2 dB
Output Impedance	50 Ω
Input Impedance	50 Ω
V_{DD} = +20 Volts at 3.5 mA	

FETs in Active Balanced Mixers

When high-performance, high-frequency JFETs are used in the design of active balanced mixers, the resulting mixer circuit demonstrates superior characteristics when compared to passive mixers using Schottky diodes or bipolar transistors. A typical active mixer using FETs is shown in Figure 43.

The inherent square-law transfer characteristics of the FET insure high intermodulation intercept and signal desensitization. The grounded-gate connection is very stable, while source injection of both the signal and local oscillator make for easy impedance matching into the FETs. Balanced configuration reduces local oscillator radiation from the signal port and suppresses the generation of even harmonics (which help to reduce intermodulation). The FET used in the mixer circuit is the Siliconix U310, which typically has C_{gs} = 1.9 pF. Such low gate capacitance is required for wide mixer bandwidth. The U310 also has typical g_{fs} of 14,000 μmho, for useful conversion gain. Dynamic range is bracketed by the lowest drain current for an acceptable noise figure and the maximum drain current – typically I_{DSS} = 40 mA.

Performance comparison of the active balanced mixer to passive mixer is made in Table IX.

CONCLUSION

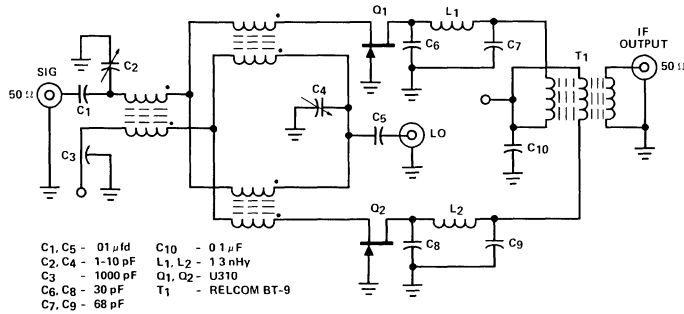
This Application Note has considered the field-effect transistor as a classic electronic component with near-universality of applications, and has touched briefly on FET basic characteristics, terminology and parameters, and typical applications.

For additional information on these unique devices, including data sheets, applications assistance, and detailed information on specific parts, contact Applications Engineering, Siliconix, Inc. 2201 Laurelwood Road , Santa Clara, CA 95054, or your nearest Siliconix area sales office.

Table IX
50-250 MHz Mixer Performance Comparison

Characteristic	JFET	Schottky	Bipolar
Intermodulation Intercept Point	+32 dBm	+28 dBm	+12 dBm†
Dynamic Range	100 dB	100 dB	80 dB†
Desensitization Level (the level for an unwanted signal when the desired signal first experiences compression)	+8 5 dBm	+3 dBm	+1 dBm†
Conversion Gain	+3 dB*	–6 dB	+18 dB
Single-sideband Noise Figure	6 5 dB	6 5 dB	6 0 dB

†Estimated *Conservative minimum



Active Balanced Mixer Using FETs
Figure 43

7.6 Analog Switches in Sample and Hold Circuits (AN74-2)

Gary Dixon
Revised January 1976

INTRODUCTION

In many cases the designers of sample-and-hold circuitry have relied upon "cut-and-try" methods to achieve good circuit performance. This Application Note provides analytic design information regarding sample-and-hold circuitry and practical design examples.

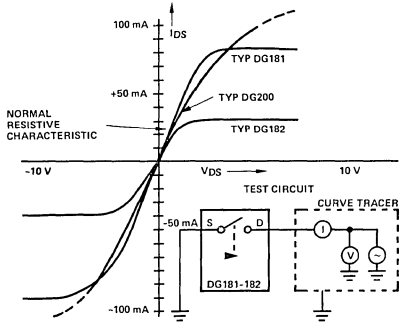
FET analog switches will meet the basic performance requirements for sample-and-hold circuitry. The criteria for choosing a given FET analog switch may seem rather simple since many of the D-C data sheet parameters are similar from one switch or from one technology (JFET, PMOS, or CMOS) to another. However, the dynamic features of a switch are the primary characteristics that must be examined. This task is not easy since any measurement assumes a given set of conditions and circuitry. This Application Note will consider two major characteristics of FET analog switches. The first area is that of the large current-handling characteristics of various switches, which can have a pronounced effect on circuit settling times. The second subject involves the offset characteristics of sample-and-hold circuits which may affect the basic accuracy of system design.

For high-speed sample-and-hold circuits, the large current handling capabilities of the switch can play an important role in determining settling time. As a rule, the data sheet specifications for switch ON resistance are made at low current levels, such as those found in analog signal coupling circuits. When an analog switch is required to charge a capacitor, the switch may be required to handle large instantaneous currents and voltages. The switch dynamic characteristics will vary depending upon the type of switch and the drive circuitry used.

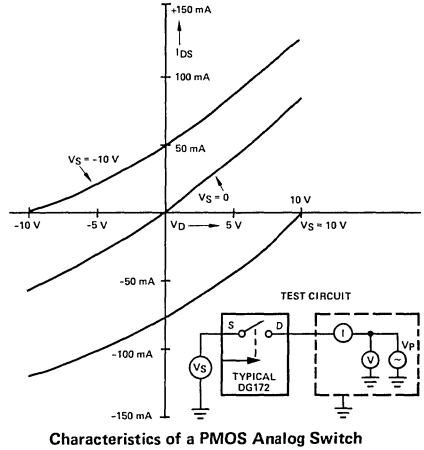
Of the many JFET switches, the DG181-191 series is recommended for its low ON resistances and its easily-determined high-current characteristics. Figure 1 illustrates that the DG181, a 30 Ω device, typically enters I_{DSS} limiting at 80 mA. Further investigation indicates the DG182, a 75 Ω device, typically encounters current limiting at 30 mA. If we compare the DG181 with a CMOS device, the DG200, we will find the DG200 has a somewhat more resistive characteristic.

Figure 2 shows the resistance characteristics of a PMOS switch, the DG172. The average ON resistance for settling purposes may be assumed to be between the minimum resistance at the most positive signal excursion and the maximum ON resistance at the most negative excursion.

CHAPTER 7



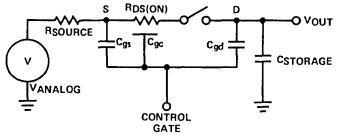
Current Characteristics of a JFET Analog Switch, The DG181, and a CMOS Switch, the DG200
Figure 1



Characteristics of a PMOS Analog Switch
Figure 2

Figure 2 is based on a negative supply voltage to the DG172 of −20 V. If the supply were −15 V, the currents through the switch would decrease, which is a disadvantage of PMOS. The DG181 current is independent of supply voltage, while the DG200 is designed to work with ±15 V supplies.

Let us now turn to the second subject to be covered, that of switch charge transfer. In the past, this subject has been called switching transients, "glitches", and various other names. Switching transients affect the intrinsic accuracy of any sample-and-hold design. During the sample interval, the capacitor charges to the sample voltage. Then during the transition from sample to hold, an offset voltage is introduced into the charged capacitor. The major phenomena is that of a capacitive voltage divider formed by the capacitive coupling between the control gate with its associated switch terminals and the storage capacitor, as shown in Figure 3.



Equivalent Switch Circuit
Figure 3

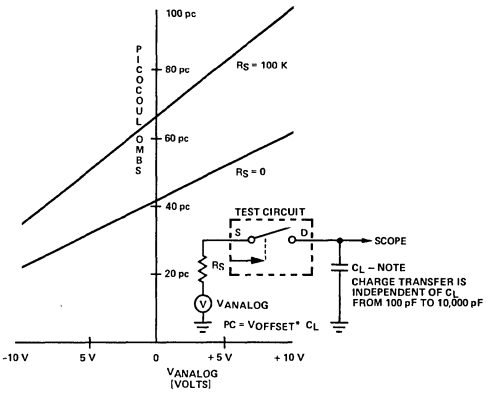
Charge transfer characteristics will vary to quite an extent, depending upon various switch and circuit configurations. To provide a method of comparison for various switches, the preferred terminology is charge transfer presented in pico coulombs.

Charge transfer (Pico Coulombs) = Voltage offset x Hold capacitance (Pico Farads).

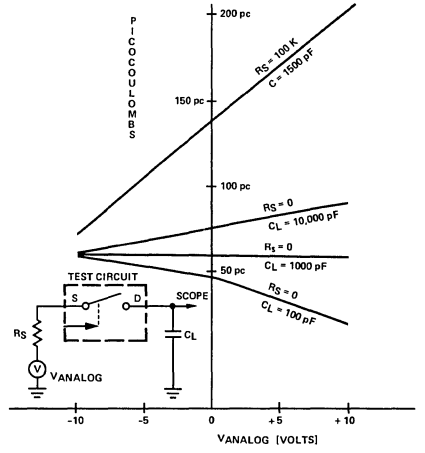
The DG181 series of JFET switches provides very good transient coupling characteristics. One of the reasons for this performance is the decrease in gate voltage swing, because the FET Gate is initially clamped at the analog voltage. The JFET construction also provides an optimization of low coupling capacitance along with low ON resistance. If we now compare a PMOS switch with the JFET characteristic we are able to see a major difference.

As may be seen from the two curves of Figures 4 and 5, the charge transfer characteristics for the DG181 and DG172 are similar at C_L = 100 pF and R_S = 0. It should be noted, however, that the DG172 has a typical ON resistance of 200 Ω – an increase in ON resistance of 6 times more than that of the DG181. For values of capacitance greater than 100 pF in the charge transfer characteristics of the DG172 are seen to be inferior to those of the DG181. The major factor which causes the storage capacitance to be value-dependent is the large distributed gate-to-channel capacitance, plus the related circuit time constants.

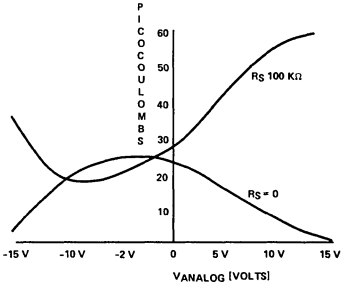
CMOS devices provide an improvement over the JFET and PMOS devices since two gates with complementary control signals are involved. The two resulting "glitches" tend to cancel each other. The transient is therefore greatly reduced but is not eliminated due to design compromises. This is shown in Figure 6.



Typical Charge Transfer Characteristic of the DG181 JFET Switch
Figure 4



Typical Charge Transfer Characteristics of the DG172 PMOS Switch
Figure 5



CMOS Charge Transfer Characteristics
Figure 6

When the various tradeoffs are considered, the DG181-191 family of JFET switches provides the best overall performance for critical sample-and-hold designs. This is due in large part to their fast (150 nsec) switching speeds, which allows a fast aperture time. The CMOS DG200 series comes in a close second, but they have somewhat slower switching times (1000 nsec). PMOS switches cost the least, and are useful in general purpose applications.

Inverting DG181 Sample-and-Hold Circuit

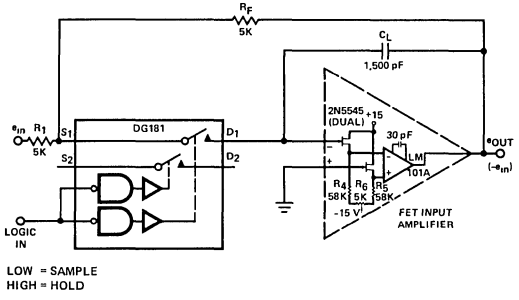
The inverting sample-and-hold circuit has several inherent advantages over the other design approaches. The switch operates at a constant voltage each time, thus reducing the aperture time jitter considerably. The input configuration reduces surge currents that are usually supplied by the signal source. A slight disadvantage of this circuit is the requirement that the two feedback resistors be matched to obtain reasonable accuracy. The feedback resistance value must be carefully chosen so that the amplifier output does not enter a current-limiting mode. General purpose amplifiers with a 20 mA limit will operate with a 5K Ω feedback network. The linear time response of the circuit is determined by the time constant $(R_f + 2R_{SW})C_L$. In this example $r_{SW} < R_f$; therefore, the settling time is determined by the feedback resistance. This circuit is current-limited by the amplifier and the feedback resistance, so the large current characteristics of the switch are of little importance. The circuit is also limited by the slew rate of the amplifier. If a 1500 pF storage capacitor is used, the amplifier slew rate should be greater than 2.7 V/μS. If, as shown in Figure 7, an LM101A op amp is used (with a slew rate of 0.5 V/μS), an additional 25 μS will be required during slew rate limiting. For the circuit shown, an acquisition time of 98 μS was measured for a swing of 20 volts settling into a 1 mV error band. If we now turn the task of determining the sample-to-hold offset, we must first examine the charge transfer characteristics of the switch. Since the source resistance is 5K Ω; which is much greater than the 30 Ω $R_{DS(on)}$, we must examine the characteristics near the high impedance curves (R_S = 100K Ω) on the charge transfer chart of Figure 4. The DG181 provides an offset voltage of 43 mV. The DG200 may be used in this circuit with a voltage jump of 18 mV. If a DG172 switch is used a 91 mV jump should be expected.

Improved DG181 Inverting Sample-and-Hold Circuit

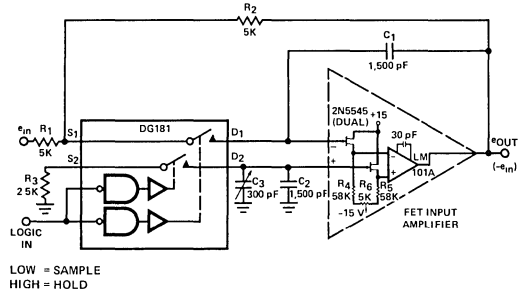
If these foregoing charge transfer errors are too large for practical use, several methods of reducing the charge transfer are possible. The first method involves increasing the capacitor size which improves the droop rate, but also requires a direct trade-off of accuracy vs speed. A second method involves reducing the size of the switching FET, which also decreases charge transfer but increases the ON resistance. This method also requires that a trade-off be made due to the relationship of speed versus accuracy. A third and more practical method is to compensate for the charge transfer. Many circuits have been proposed in the past which vary from simple capacitors in logic circuitry to rather complex systems. The inverting sample-and-hold circuit is rather easy to compensate since it operates at a single voltage level. The basic concept involves an equal but opposite charge transfer and may be implemented by coupling to a level changer which provides transitions in the opposite direction of the FET gate voltage. A rather unique circuit using this principle uses the two switches normally found in analog switch packages.

The compensation circuit shown in Figure 8 employs three additional components (R_3, C_2 and C_3) to provide total offset errors which are adjustable to much less than 1 mV. One feature that the DG181 device offers is a 20% larger charge transfer from the D_2 terminal. This actually makes compensation much easier since only one side of the network must be adjusted. With other switches (such as the DG200) parameter variations may require that hold capacitors of two different sizes be used to provide adjustability. An added feature of this circuit configuration of Figure 8 is a net reduction in the system droop due to a balancing effect of the leakage currents.

CHAPTER 7



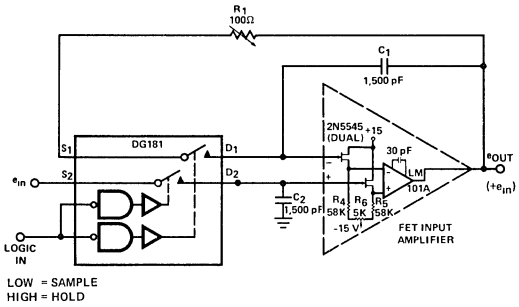
Inverting Sample & Hold Circuit
Figure 7



Improved Inverting Sample & Hold Circuit
Figure 8

High Performance DG181 Non-Inverting Sample-and-Hold Circuit

For those designers who require much faster settling times, the high-performance sample-and-hold circuit shown in Figuse 9 should be used.



High Performance Non-Inverting Sample-and-Hold Circuit
Figure 9

As mentioned previously the DG181 JFET switch provides the best combination of settling speed and inherent charge transfer accuracy.

A typical DG181 analog switch is capable of charging a 1500 pF capacitor in 500 ns to within a 1 mV error band for a 20 volt swing. This statement assumes that the signal source is able to supply the capacitor charging current of 80 mA (zero source impedance).

The offset is adjusted to zero offset for zero analog signal by changing R_1, which also provides a normalization for both source impedance and the differential charge transfer characteristic between switches. The offset varies with analog voltage from +1.4 mV at 5 V to -1.5 mV at -5 V. This reduction provides an order-of-magnitude improvement over an uncompensated circuit. In general, for the faster sample-and-hold circuits which use the non-inverting technique, the charge transfer may be adjusted to zero at one voltage only. The compensated inverting sample-and-hold approach will provide much better offset characteristics, but at a sacrifice in overall speed. The non-inverting sample-and-hold circuit, however, has the disadvantages of CMRR gain errors and the source may be loaded with large sampling-surge currents.

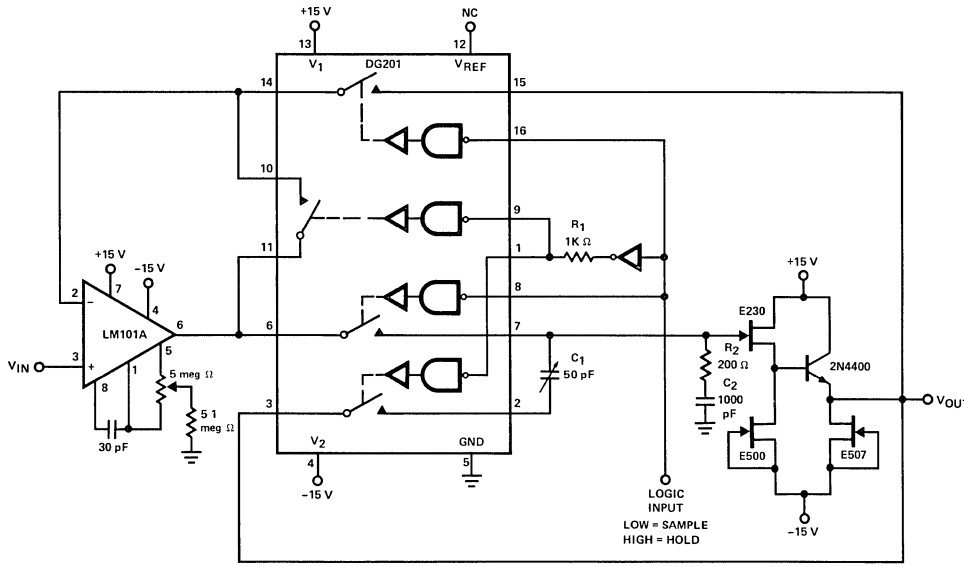
High-Quality DG201 Sample-and-Hold

Figure 10 shows a high-quality sample-and-hold using a DG201.(1) The DG201 has a higher ON resistance than the DG200 (175 Ω vs 70 Ω) but this does not affect the overall speed. The LM101A provides gain and buffers the input from storage capacitor C_2. R_2 adds a zero in the open loop response to compensate for the pole caused by the switch resistance and C_2, improving the closed loop stability. R_1 provides a slight delay in the digital drive to pins 1 and 9.

C_1 provides concellation of coupled charge, keeping the sample-to-hold offset below 5 mV over the analog signal range of -10 to +10 V. Aperture time is typically 1 μsec, the switching time of the DG201. Acquisition time is 25 μsec, but this can be improved by using a faster slewing op amp. Droop rate is typically less than 5 mV/sec at 25°C.

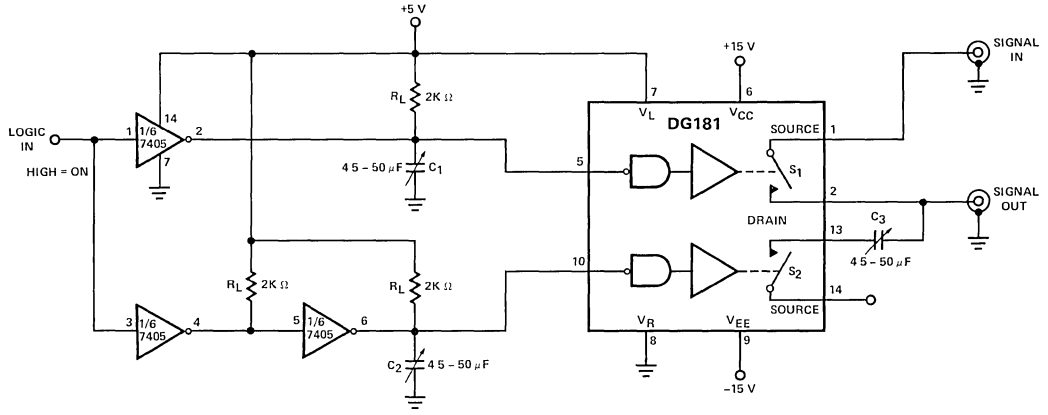
REFERENCES

(1) Lee Shaeffer, "CMOS Analog Switches – A Powerful Design Tool," Siliconix Application Note AN75-1, July 1975.



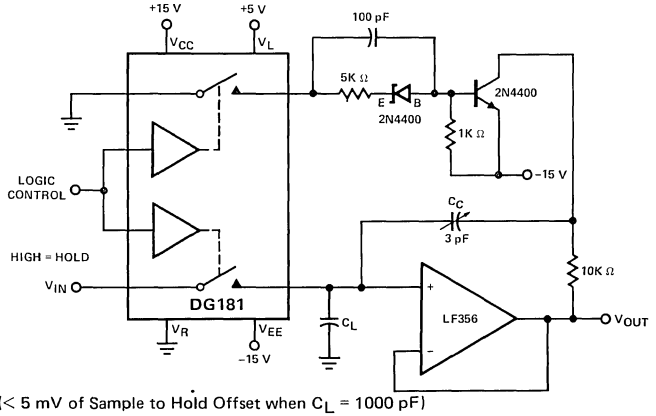
DG201 Sample-and-Hold
Figure 10

Additional Application Circuits:



Switching Transients Attenuated by Synchronization of Turn-On and Turn-Off of One Switch with Those of Another. (Refer to "Electronics," Oct. 3, 1974, pg. 108, "Attenuating Transients in Analog FET Switches.")

Figure 11



(< 5 mV of Sample to Hold Offset when C_L = 1000 pF)

Charge Compensated Sample and Hold, < ±5 pC Charge Transfer (< 5 mV Sample to Hold Offset when C_L = 1000 pF). (Refer to "Electronic Design," April 27, 1972, "Cut Transients in FET Analog Switches.")

Figure 12

7.7 CMOS Analog Switches – A Powerful Design Tool (AN75-1)

July 1975
Lee Shaeffer

INTRODUCTION

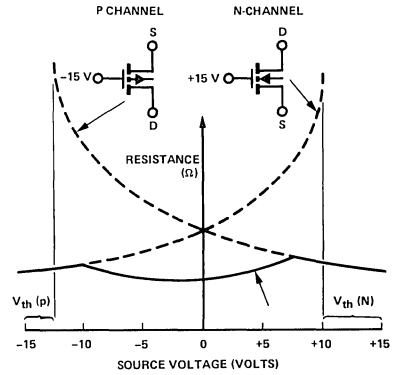
Siliconix CMOS analog switches combine large voltage handling capability, low power dissipation, low leakage, and direct TTL/CMOS interface capability for maximum design flexibility. In addition, a family of multiplexers are available which provide binary decoding on the chip for system simplicity. This application note describes the Siliconix CMOS switch family and offers circuits which illustrate their capabilities.

Properties of CMOS

CMOS (Complementary Metal-Oxide-Semiconductor) combines P-channel and N-channel enhancement-mode FETs in a common substrate. P-channel enhancement-mode FETs have a negative threshold voltage (the gate must be several volts more negative than the source or drain in order for current to flow between the source and the drain), while N-channel FETs have a positive threshold (Figure 1). When a P-channel FET is used as a switch (standard PMOS devices), the gate is held at the negative supply when in the ON condition, and the FET conducts for most voltages applied to the source. However, when the source voltage approaches the negative supply, the resistance approaches infinity. The result is a dead-band equal to the threshold voltage of the FET.

This problem is overcome by connecting an N-channel FET in parallel with the P-channel device. The N-channel gate is tied to the positive supply, and the FET is turned on hardest when the source is most negative. The resistance curve of the P-channel and N-channel FETs in parallel is shown in Figure 1.

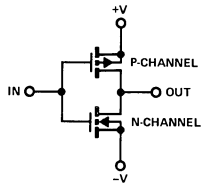
The resistance curve is nearly flat for $V^- \leqslant V_S \leqslant V^+$ (only CMOS is capable of this) but some resistance variation is normal. 20% peaking is typical for ±15 volt power supplies, with greater peaking at lower supply voltages. If the P- and N-channel FETs have different thresholds the peaks will not be symmetrical. As the switch heats up the resistance increases 0.5%/°C.



Resistance vs Source Voltage of P-channel and N-channel FETs
Figure 1

Because the gates of the P- and N-channel FETs are internally switched to opposite supply voltages, one would expect that leakage currents and switching glitches would cancel when $V_S = 0$. This would indeed be true if the FETs were identical except for polarity. However, because the conductance of the N-doped silicon is 2.5 times greater than that of equally doped P-type silicon, it is a practical impossibility to make the leakage currents and capacitances equal for FETs of equal resistance (the P-channel is physically 2.5 times larger than the N-channel). The cancellation therefore takes place at some intermediate voltage. Because the measured leakage is the P-channel leakage minus the N-channel leakage, small variations in the absolute value of either can make a large change in the difference. Since small amounts of impurities can greatly influence the leakage, both the magnitude and polarity of the leakage measured at the source or drain will vary greatly from unit to unit, and will depend on the analog voltage and the temperature. Even though the leakage is unpredictable, it is still less than a comparable PMOS or bipolar switch.

In addition to a large analog voltage capability, a second advantage of CMOS is low power dissipation. Figure 2 shows a digital inverter with virtually no static power dissipation. When the input is pulled high, the N-channel turns ON and the P-channel OFF. Thus the output is tied to the negative supply through $r_{DS(on)}$ of the N-channel FET, while the P-channel device draws no current. If the input is changed to a negative voltage the state of the FET is reversed, pulling the output high. When a CMOS device is turned ON, the load is turned OFF; this overcomes a major disadvantage of PMOS structures, where the load is ON at all times and considerable power is drawn when the FET is ON.

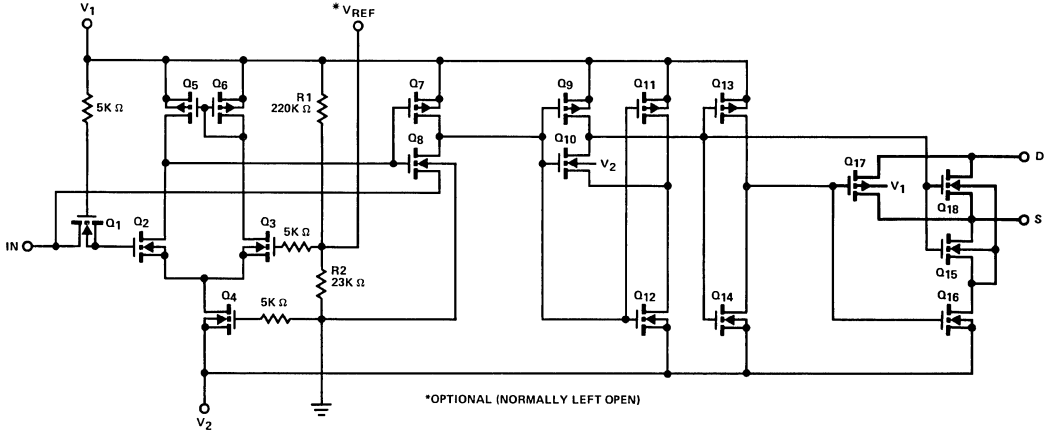


A CMOS Inverter
Figure 2

Figure 3 shows the schematic of the DG200 and DG201, typical Siliconix CMOS switches. Q_2, Q_3 and Q_4 form a differential amplifier with active loads Q_5 and Q_6. Q_1 provides input protection for the gate of Q_2, while the gate of Q_3 is connected to the logic threshold voltage established by the $R_1 - R_2$ voltage divider. The differential input stage allows a low and repeatable switching threshold voltage (1.4 V) independent of the threshold voltages of the FETs. The source of Q_8 is connected to the input to "bootstrap" the $Q_7 - Q_8$ inverter, making the switching threshold sharper. $Q_9 - Q_{10}$ and $Q_{13} - Q_{14}$ are also inverters, while $Q_{11} - Q_{12}$ level-shift the logic from 15 to 30 V p-p. Q_{15} and Q_{16} switch the body of Q_{18} to either the negative supply (in the OFF state) or the source (when the switch is ON). The result of a positive clamp of the body to the source is a low ON threshold voltage which is not modulated by the analog voltage. In the OFF condition the isolation and breakdown voltage are high and the leakage is low when the body is firmly clamped to the negative supply. Because the clamping FET causes the switching glitches to be greater at the source than at the drain, it is good practice to connect the source to the actual signal source, or to the lower impedance point in the circuit.

An adjustable switching threshold is available on most Siliconix CMOS analog switches. As shown in Figure 3, V_{REF} is connected to the junction of two resistors which act as a voltage divider, dividing the +15 V supply down to +1.4 V. This voltage is connected to the differential input amplifier and establishes the switching threshold at 1.4 V. Normally V_{REF} is left open. If operation at reduced supply voltage is desired, however, the switching threshold will be lowered, resulting in less noise immunity. By connecting a resistive divider to V_{REF}, the threshold may be raised back up to 1.4 V. Operation is possible down to ±8 V on the supplies.

All of the multiplexers (DG506, DG507, DG508 and DG509) contain decode circuitry enabling a binary logic input to select one of 4, 8, or 16 channels. Each multiplexer also contains an ENABLE-INHIBIT control, which shuts the device off when in the INHIBIT mode. This allows the common connection (drains) of several multiplexers to be paralleled, and the units can then be enabled one at a time. This is useful when more than 16 channels are involved. Also, when the device is inhibited, its power dissipation is typically less than one-fourth the normal dissipation, for low total system power dissipation.



Schematic of a Typical CMOS Switch Channel
(DG200 and DG201)
Figure 3

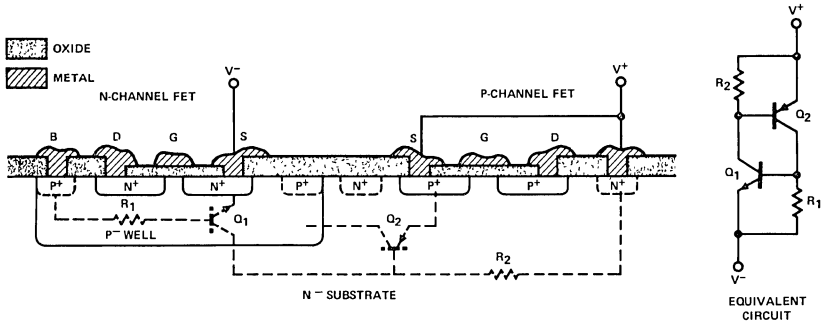
Latch-Proof Operation

Latchup had been a thorny problem in first-generation CMOS switches. A cross section of two CMOS FETs (Figure 4) shows both a PNP and an NPN structure, which is connected as an SCR (PNPN). Under abnormal conditions, one or more of the PN junctions becomes forward biased, activating the bipolar transistor. This in turn activates the SCR, which appears as a short between the substrate (positive supply) and ground or V^-. Since the product of the NPN and PNP Betas is often greater than 1000, this short would persist until power was removed or until the device burned up. When 200 Ω resistors were placed in series in the power supply leads, device destruction was prevented; however, only removal of the power supply would return the circuit to normal operation.

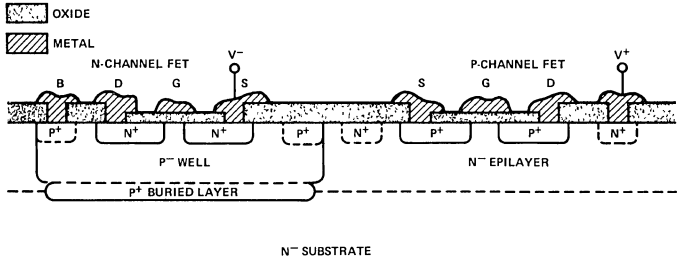
By using a "buried layer" configuration, (patent pending, Figure 5) Siliconix has reduced the product of the NPN and PNP betas to less than one, making latch-up impossible under any circumstances. The switches retain their desirable features such as low leakage, high OFF isolation, and high breakdown voltage. In addition, the latch-proof switches now have a much higher current capability (20 mA continuous, up to 100 mA peak on the DG200).

General Switching Applications

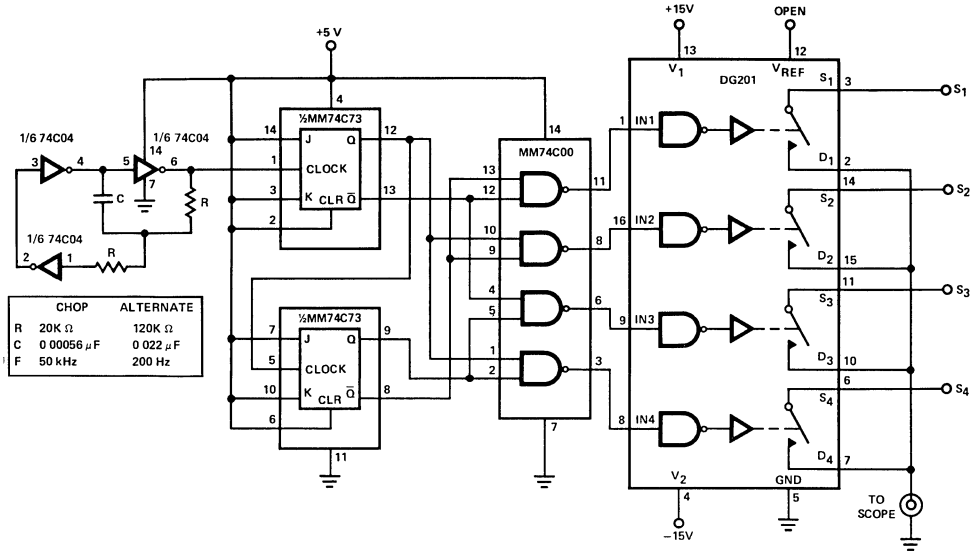
One of the significant advantages of the CMOS structure is in its ability to handle large analog voltages, since only CMOS can allow signal swings to the power supplies. A logical application is switching the outputs of operational amplifiers. The entire system can be run on ±15 V, and the full output of the op-amps (typically ±14 V) can be used. In most cases it is advantageous to switch at the relatively low-impedance output of an op-amp rather than at the summing junction, to minimize the effects of switch capacitance and leakage.

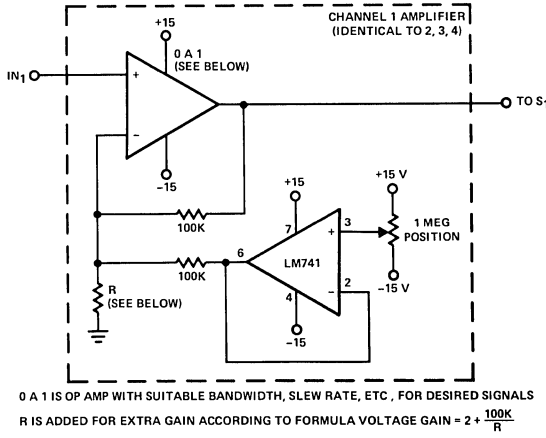


A Cross Section of Two CMOS FETs Showing the Parasitic Transistors, and Equivalent Circuit
Figure 4



A Cross Section of the Siliconix "Buried Layer"
Figure 5





The "Scope Extender" Which Displays 4 Channels Simultaneously on a Single Trace Scope
Figure 6

Figure 6 shows a novel multiplexing application, It is an adapter that allows 4 inputs to be displayed simultaneously on a single trace scope. For low-frequency signals (<500 Hz) the adapter is used in the "chop" mode at a frequency of 50 kHz. The clock may be run faster, but switching glitches and the actual switching time of the DG201 limit the maximum frequency to 200 kHz. High frequencies are best viewed in the alternate mode, with a clock frequency of 200 Hz. When the clock is below 100 Hz, trace flicker becomes objectionable. One of the 4 inputs is used to trigger the horizontal trace of the scope.

Figure 7 shows a variable low-pass filter with break frequencies at 1, 10, 100 Hz and 1 kHz. The break.frequency is

$$fc = \frac{1}{2\pi R_3 C_X} \quad (1)$$

The low frequency gain is

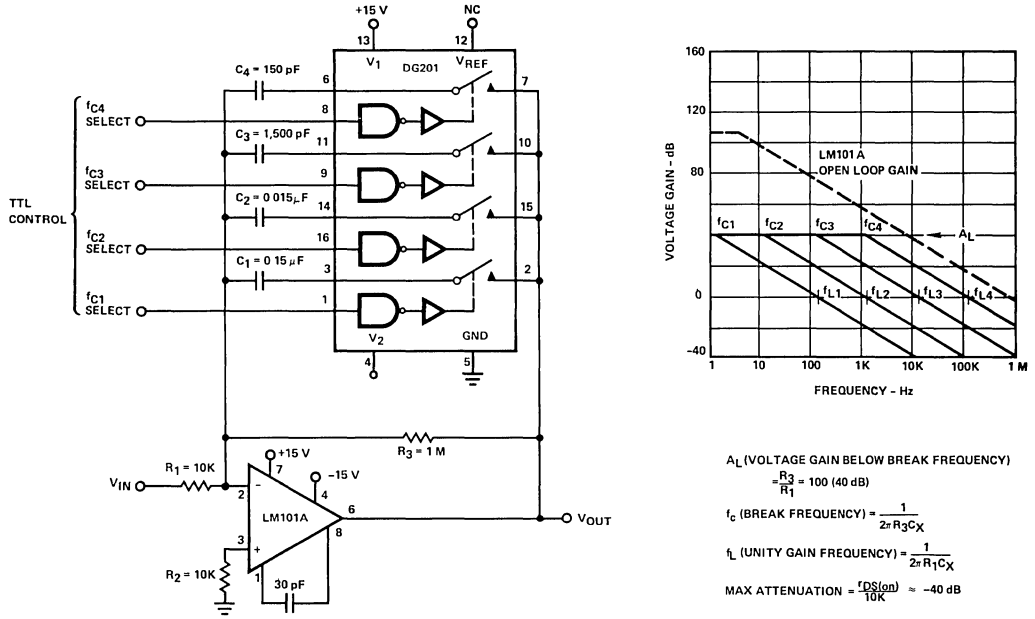
$$A_L = \frac{R_3}{R_1} = 100\,(40\text{ dB}) \quad (2)$$

A second break frequency (a zero) is introduced by $r_{DS(on)}$ of the DG201, causing the minimum gain to be

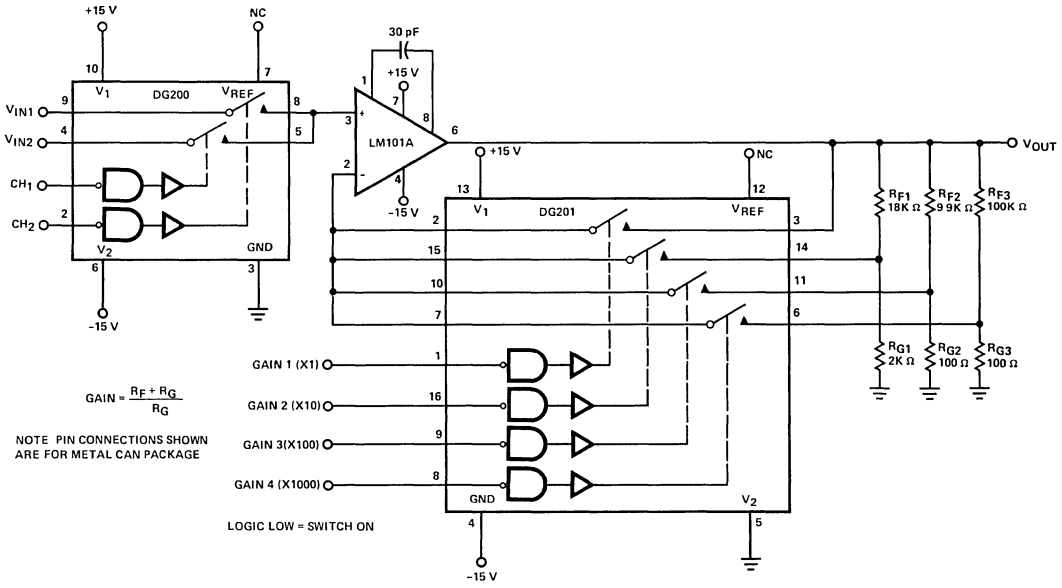
$$A_{MIN} = \frac{r_{DS(on)}}{R_1} \approx \frac{100}{10K} = .01, \quad (3)$$

a maximum attenuation of 40 dB (80 dB relative to the low frequency gain).

The amplifier shown in Figure 8 has digitally-programmable gain and inputs. The DG200 "looks" into the high input impedance of the op-amp, so the effects of $r_{DS(on)}$ are negligible. The DG201 is also connected in series with r_{IN} and is not included in the feedback dividers, thus contributing negligible error to the overall gain. Because the DG200 and DG201 can handle ±15 V, the unity gain follower connection (x1) is capable of the full op-amp output range (±12 V).



Active Low Pass Filter with Digitally Selected Break Frequency
Figure 7



A Precision Amplifier with Digitally Programmable Inputs and Gains
Figure 8

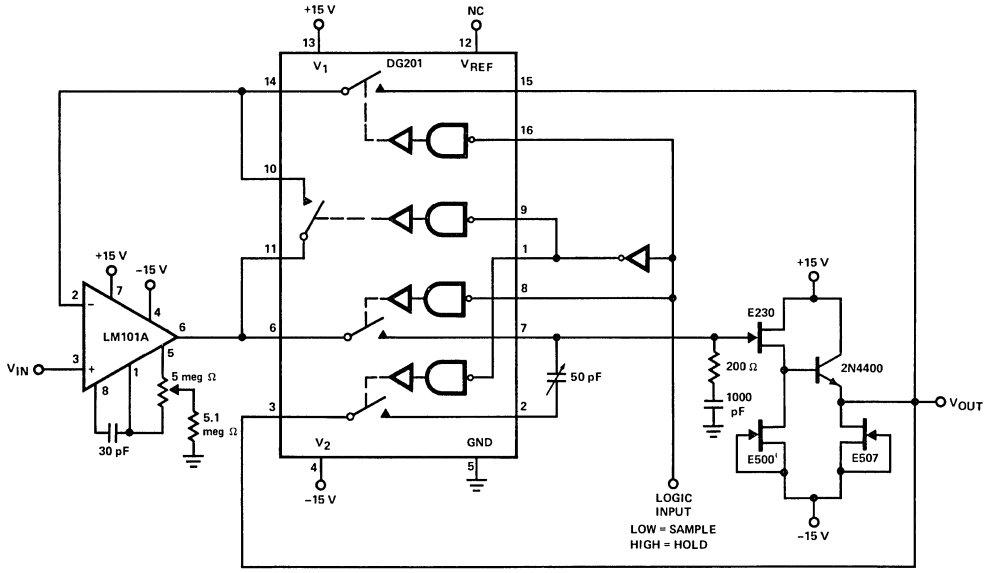
CHAPTER 7

A single DG201 contains all the switches necessary for the sample-and-hold circuit shown in Figure 9. Switch 4 provides cancellation of coupled charge (glitches), keeping the sample-to-hold offset below 5 mV over the analog voltage range (–10 to +10 V). Aperture time is typically 1 μsec. Acquisition time is 25 μsec, but this can be improved by using a faster slewing op-amp. Droop rate is typically less than 5 mV/sec at 25°C.

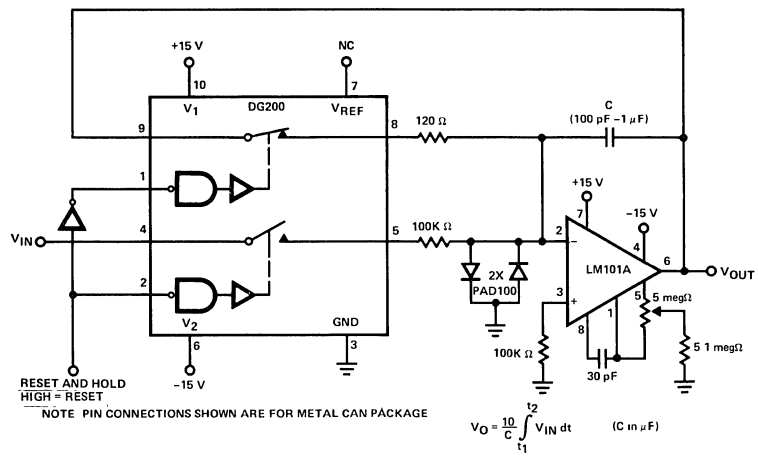
The low $r_{DS(on)}$ and high peak current capability of the DG200 makes it ideal for discharging an integrator capacitor (Figure 10). A HIGH logic input pulse disconnects the integrator from the analog input and discharges the capacitor. When the logic input is returned to low the integrator is triggered, having the transfer characteristic,

$$V_{OUT} = \frac{1}{10^5 C} \int_{t_1}^{t_2} Vi\, dt \qquad (4)$$

D_1 and D_2 prevent the capacitor from charging to over 15 V.

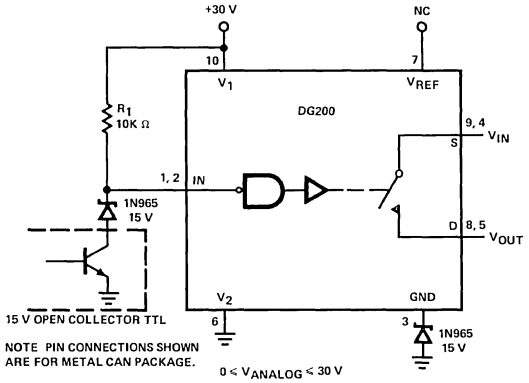


DG201 Sample and Hold
Figure 9



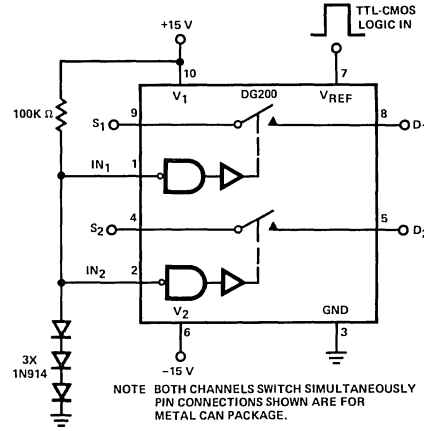
A Resettable Integrator
Figure 10

It is possible to operate a CMOS switch from a single supply by shifting the ground and logic inputs to an intermediate voltage, as shown in Figure 11. This allows an analog voltage range of 0 to +30 volts.



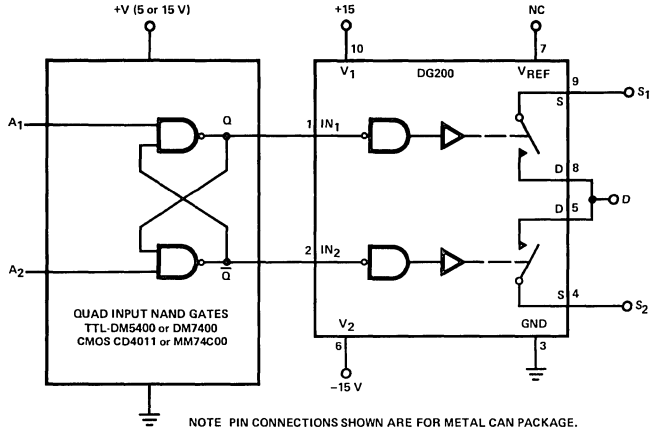
Operation from a Unipolar Supply
Figure 11

Active HIGH (inverted) operation is possible by connecting the input pin to a reference and applying the logic signal to the V_{REF} pin, as shown in Figure 12. Since both switches are connected internally to V_{REF}, they will switch simultaneously. It is therefore easy to make a DPDT (in conjunction with a second DG200 connected the standard way) without an external inverter.



Inverted Operation (Logic 1 = ON)
Figure 12

A latching SPDT switch is shown in Figure 13. This is recommended when the switch is activated by a peak or limit detector, or with mechanical switches (to eliminate contact bounce). The inputs are normally low, and the switches are held in predetermined states. When either A_1 or A_2 receive a HIGH pulse, the switches assume the states given in the truth table. Simultaneously holding A_1 and A_2 HIGH will cause both switches to be OFF; the last input to go low upon release of the commands will determine the eventual states of the switches.



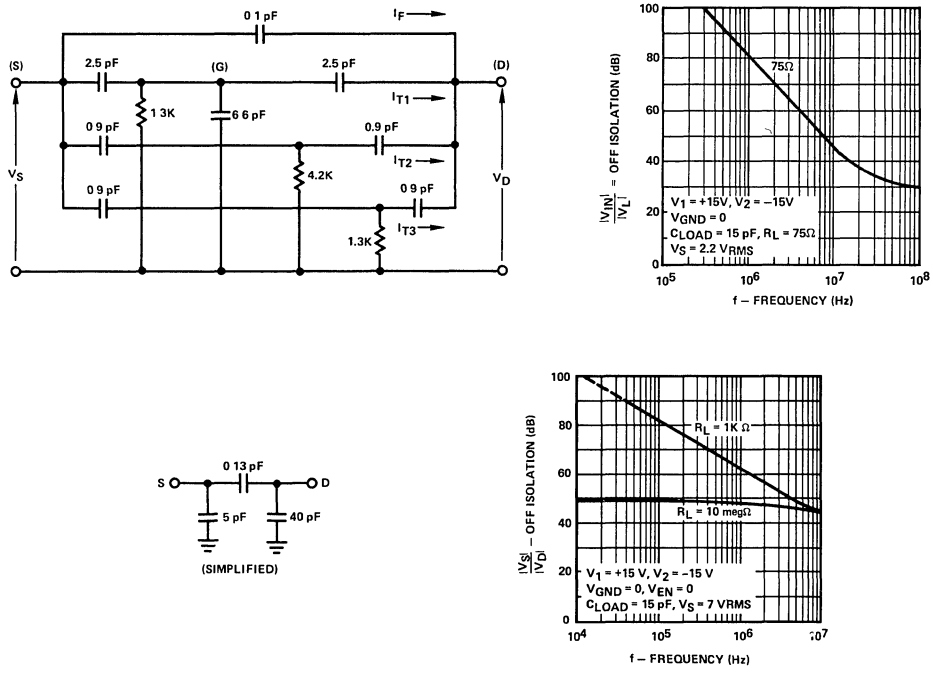
TRUTH TABLE

COMMAND		STATE OF SWITCHES AFTER COMMAND	
A_2	A_1	S_2	S_1
0	0 (normal)	same	same
0	1	OFF	ON
1	0	ON	OFF
1	1	INDETERMINATE	

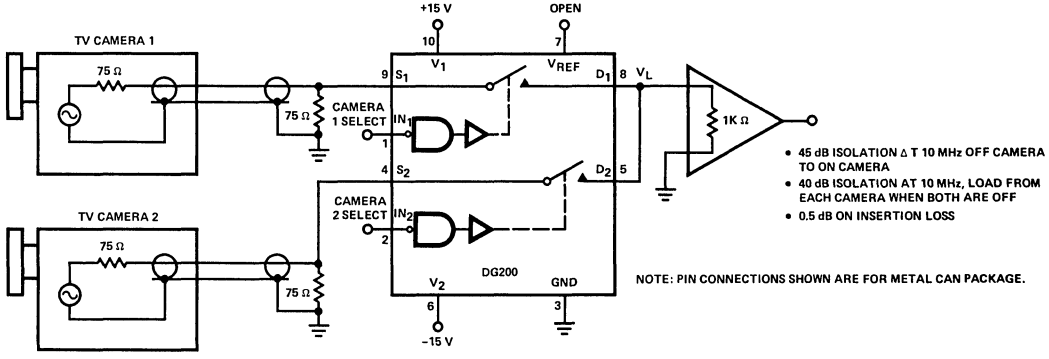
A Latching SPDT
Figure 13

CHAPTER 7

When switching high frequency signals (>100 kHz), some knowledge of the OFF characteristics are helpful. Figure 14 shows the equivalent OFF circuit of a DG200 and the accompanying graph gives the isolation under the conditions specified. 40 dB isolation at 6 MHz is good for general purpose video switching. A DG200 can achieve this easily, using the circuit shown in Figure 15 (assuming careful P.C. board layout). When greater isolation is needed, the circuit shown in Figure16is recommended. The "T" configuration provides over 40 dB more OFF isolation with only a slight increase in ON insertion loss.



Equivalent "OFF" Circuits and OFF Isolations of the DG200 and DG506
Figure 14



General Purpose Video Switch
(f = DC to 10 MHz)
Figure 15

Figure 14 also shows the high frequency characteristics of the DG506 and a simplified OFF equivalent circuit. The DG506 has OFF isolation which is constant when working into a capacitive load, allowing the designer to model the OFF DG506 as a capacitor of nominal value 1.13 pF. Not all sources have equal OFF isolation, however. S_9 has the greatest isolation, while S_8 is worse due to its proximity to the drain. Grounding the metal lid on the package (it normally floats) increases the isolation an average of 3 dB.

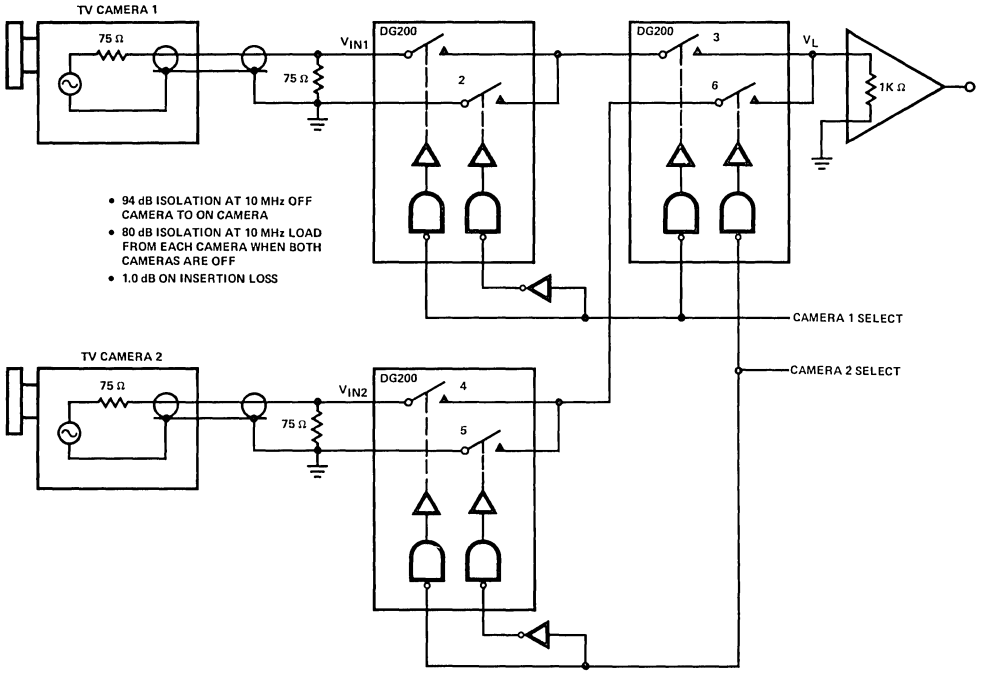
An in-depth study of switching high-frequency signals is presented in Siliconix applications note AN73-3, "Switching High Frequency Signals with FET Integrated Circuits."

Multiplexing

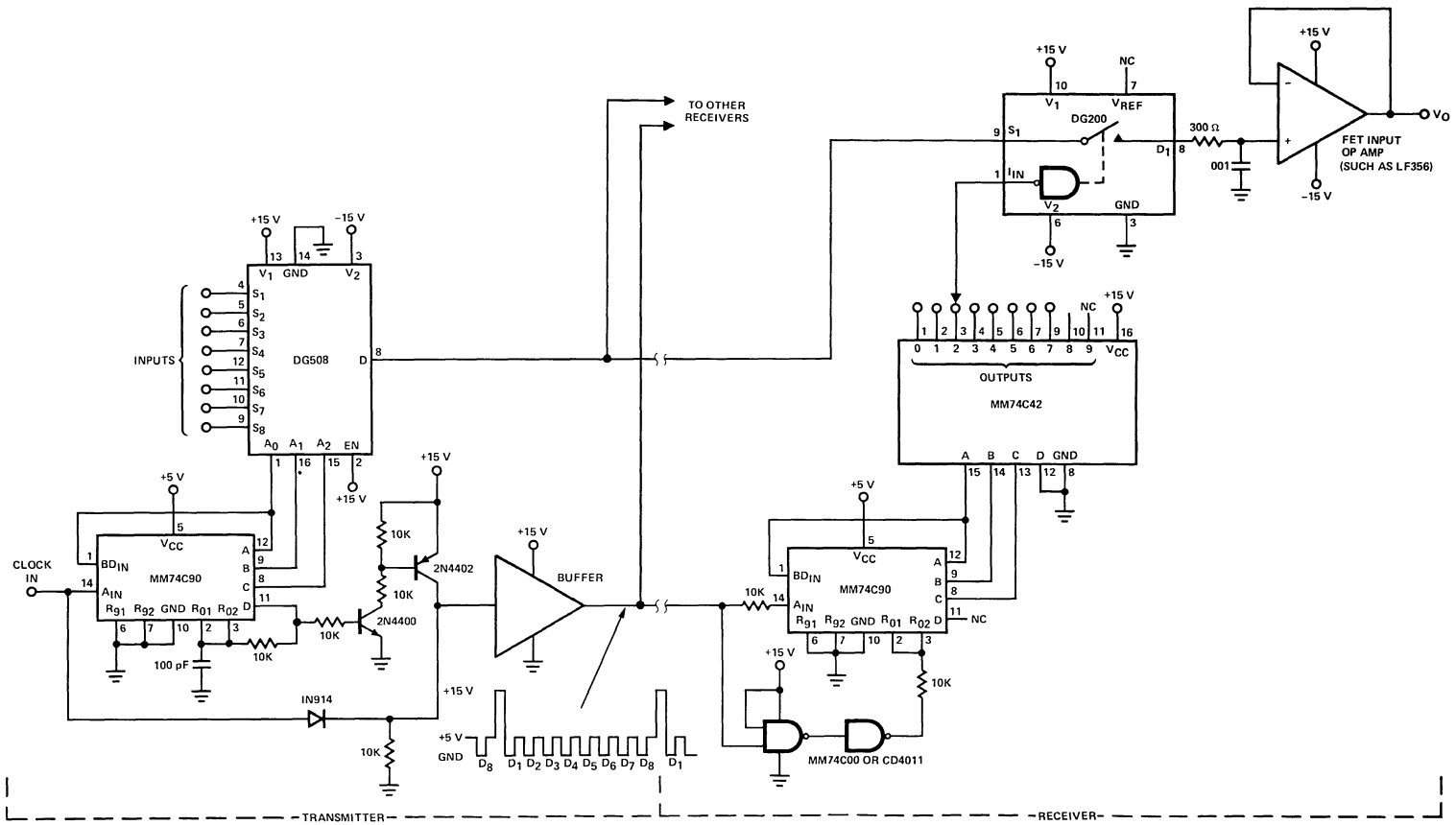
Multiplexing allows a number of signals to be processed simultaneously through a single cable, amplifier, and data conversion system. Numerous industrial and commercial uses include factories and warehouses where conditions at remote parts of a building can be monitored and sent to a central control point over a single cable. Airplanes take great advantage of multiplex systems, both receiving and transmitting information from central points with a minimum of wire. Many hotels and motels pipe up to 16 channels of music to each room. The music desired is selected by the guest in the room. When digitizing information, the economies are readily apparent between using a $50 multiplex system and a single A to D converter, as compared to employing a separate expensive A to D converter for each of several channels.

Figure 17 shows a typical multiplex system intended to carry one of 8 inputs into a remote location. A 5 V pulse train is sent down a separate channel to perform timing and synchronizing functions. A 15 V reset pulse is superimposed on the 5 V clock, which is detected by the MM74C00 in the receiver. Using this system, many remote points can be monitored, one at a time, at any of several locations.

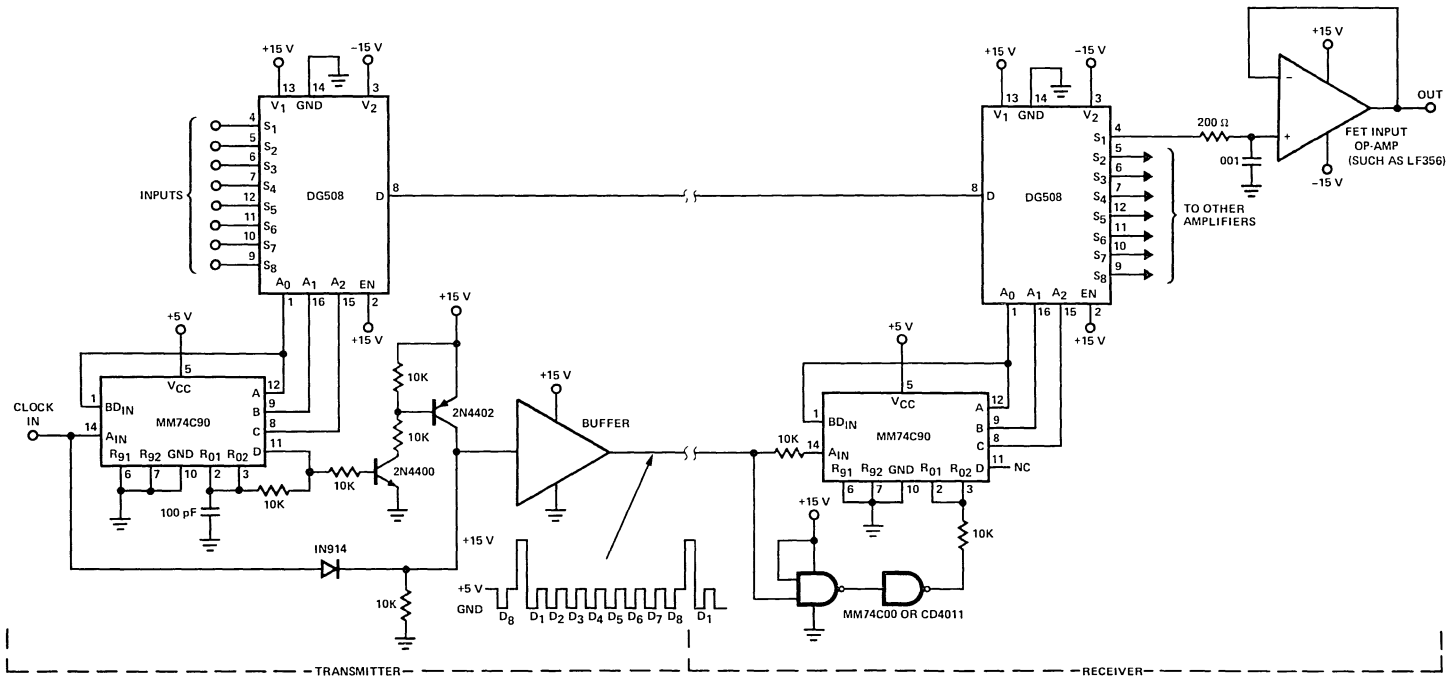
A number of signals may be sent between two points simultaneously by making a slight modification in the receiver circuit (Figure 18). A second DG508 is used as a demultiplexer, allowing all 8 channels to be monitored continuously.



Video Switch with Very High OFF Isolation
Figure 16



A One of 8-channel Transmission System
Figure 17



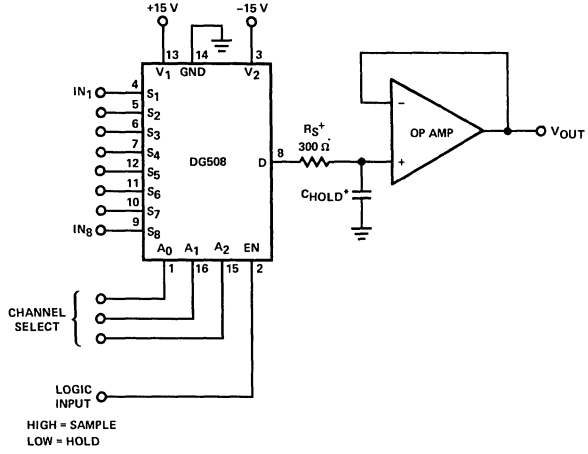
An 8-channel Mux/Demux System
Figure 18

Often information is multiplexed into a conversion system which has a relatively slow processing time, necessitating a sample-and-hold after the multiplexer. Using the DG508 as a sample-and-hold switch combines both functions, as shown in the "one of eight sample-and-hold" circuit (Figure 19).

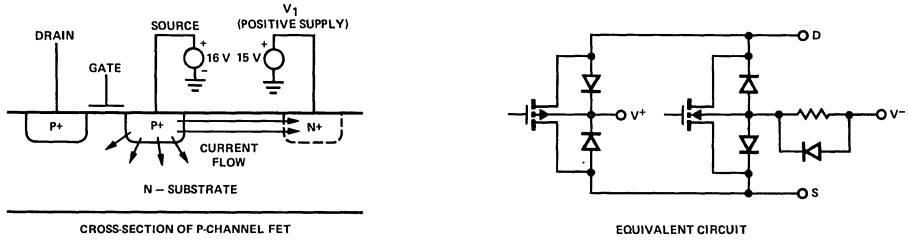
Overvoltage

In certain applications the analog signal may exceed ±15 V, or be present when the power supplies are off. This is a condition known as overvoltage, and it can present problems unless certain precautions are taken.

When the analog voltage exceeds the supply voltage, the source-body junction will forward bias, as shown in Figure 20. Current will flow from the signal source into the supply. If the current source capability of the signal source and the current sink capability of the power supply are each greater than 20 mA, a resistor should be connected in series with source to limit the current.



A One of 8-channel Sample and Hold
Figure 19



Current Paths During an Over-voltage Condition
Figure 20

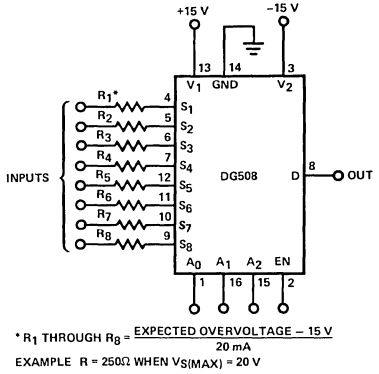
If the analog signal is present when the supplies are off, diodes in series with the supplies will allow the supply pins to float and prevent excessive current from flowing. A DG508 with full overvoltage protection is shown in Figures 21a and 21b.

2-Level Multiplexing

When a large number of channels are multiplexed, the outputs of two or more multiplexers can be connected together and each multiplexer sequentially enabled. In the INHIBIT mode the multiplexer draws less power and its output and inputs act as open circuits. Theoretically, an infinite number of channels can be accomodated in this way; in practice the accumulated output capacitance and leakage of many paralleled multiplexers limits the speed and accuracy of the system. A much better method is the two level multiplex system, shown in Figure 22. The two-level system has a bank of high speed switches at the output which sequentially switch between the 4 DG506's. Each DG506 is able to switch during the time the other 3 are being interrogated, and they contribute leakage and capacitance at the output only when they are switched on by the DG181 (¼ of the time). This circuit has several important advantages over a multi-unit single-level system, such as:

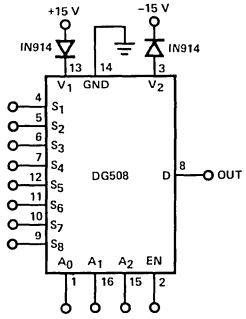
1. The switching speed of the system is dependent on the DG181, which is a high-speed 2-channel SPST ($t_{ON} \approx 150$ nsec). The slower switching time of the DG506 ($\approx$ 1 μsec) is not important because this switching transition can take place while the other DG506's are being interrogated. In this way a very fast multiplex system can be made with a large number of low-cost, moderate-speed multi-channel multiplexers and several high speed SPST switches.
2. The output capacitance of the 2-level system is much lower than that of the single level. It consists of a single DG506 (40 pF) and several DG181's (6 pF OFF, 15 pF ON) which is much less than several DG506's in parallel. If 64 channels are multiplexed, for instance, C_{OUT} of the 2-level system would be 72 pF, vs 160 pF for the single-level system.
3. The output leakage current is reduced by a similar amount. (From ±40 nA to ±10 nA in a 64-channel system).

The two level multiplex system is very useful in communications links, high speed interfacing with comparators, or wherever a large number of channels must be multiplexed at high speeds.[1]



(A)

A DG508 protected against analog signals which exceed 15V.

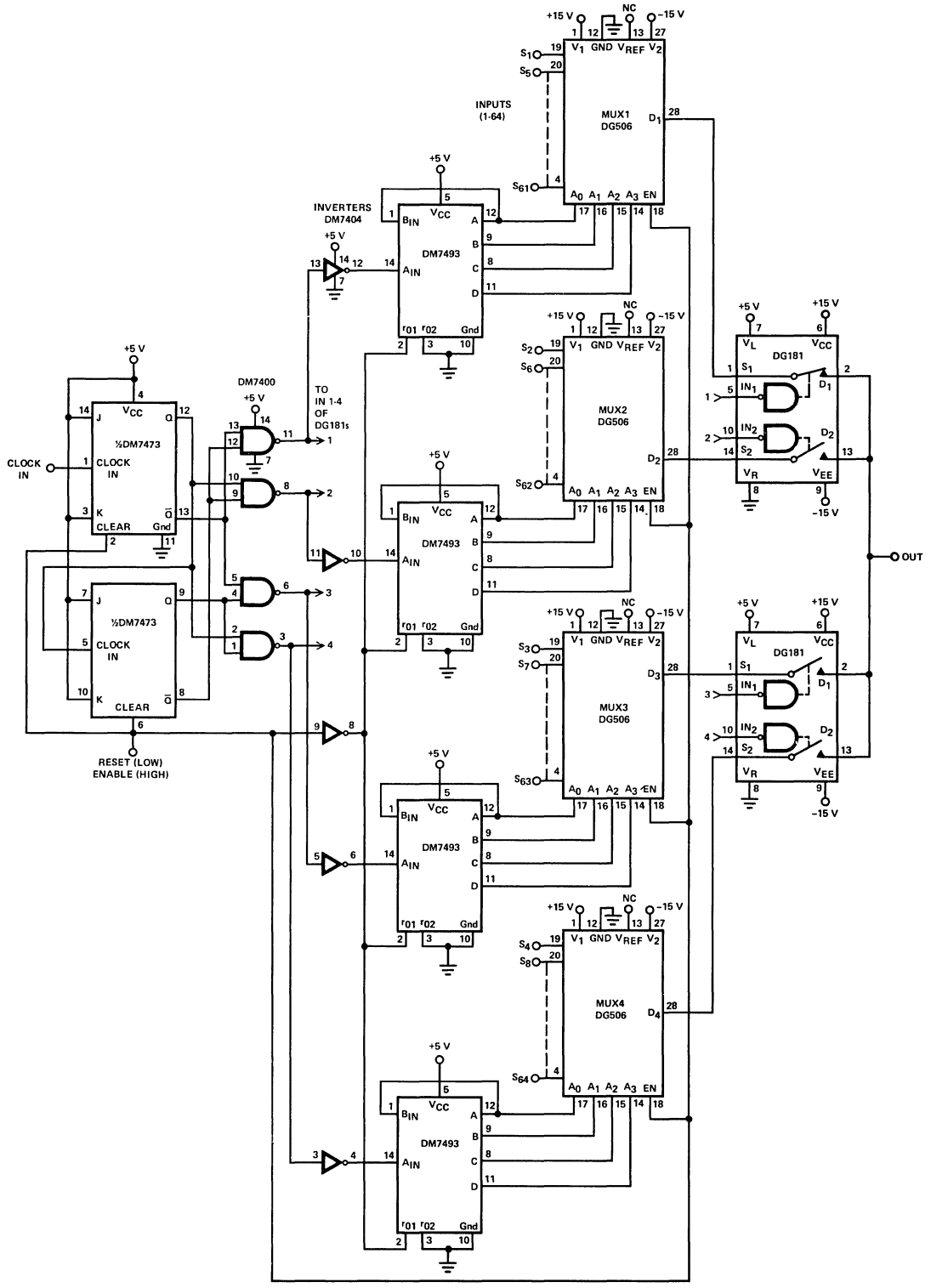


(B)

A DG508 protected against analog voltages being present when the power supplies are off.

Over-voltage Protection (shown for DG508) is Normally Used Only When the Analog Voltage Exceeds the Power Supply Voltages, and the Signal Source is Capable of Generating Greater Than 20 mA

Figure 21



64-Channel 2-Level Multiplex System

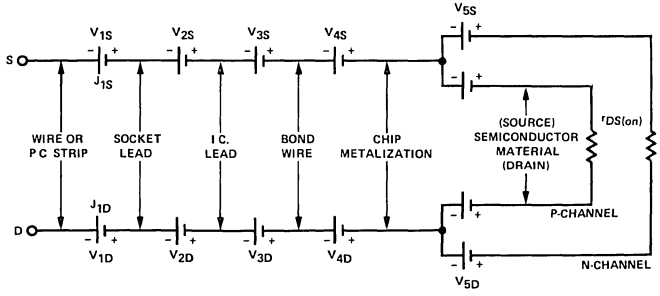
Figure 22

Low Level Multiplexing

When multiplexing low level signals, extra care must be used because the signal may be masked by A.C. noise pickup and D.C. voltages generated by thermocouple effects at the connections of dissimilar metals. Much greater accuracy is obtained if the signal is handled differentially, so that A.C. noise and D.C. thermocouple effects appear as common-mode signals which can eventually be rejected. For this reason a line of differential multiplexers is available which allows improved thermal tracking and differential cancellation of leakage and switching glitches.

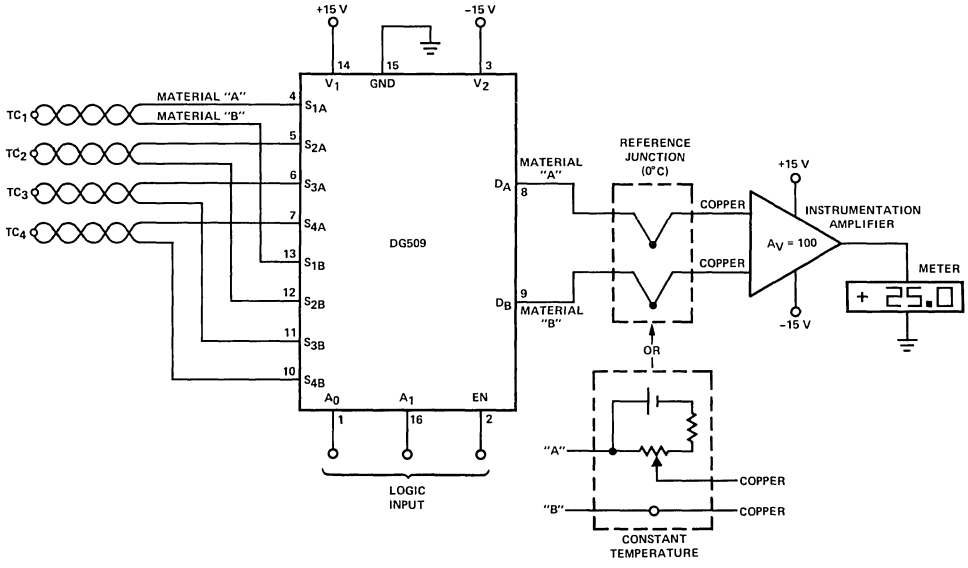
Figure 23 shows a thermocouple representation of a typical multiplexer mounted in a socket. If connection J_{1S} is at the same temperature as connection J_{1D}, then $V_{1S} = V_{1D}$. If all "S" junctions are at the same temperature as the corresponding "D" junctions, the total voltage across the multiplexer is zero. Conversely, if a temperature imbalance exists between side "S" and side "D" then the voltages will not exactly cancel and a net error voltage will appear. For this reason the multiplexer and associated connections should be mounted in a thermally-stable environment, away from hot components and with as few drafts around the chip as possible. When a DG509 is mounted in a thermally-stable environment, the typical error developed across the switch is about ±3 μV over the operating temperature range of the device. In free air, with random room drafts, it can be as high as 7 to 10 μV. When heated with a thermal probe at 85°C (resulting in uneven temperatures across the device) the absolute voltage across a switch is about 100 μV with a 30 μV differential error. I.C. multiplexers are therefore ideal in low level applications if care is exercised to insure an even temperature.

Figure 24 shows a DG509 thermocouple multiplexer. To decouple the sensors from the meter amplifier, either a



Thermocouple Representation of a Typical Multiplexer Switch

Figure 23



A Thermocouple Multiplex System

Figure 24

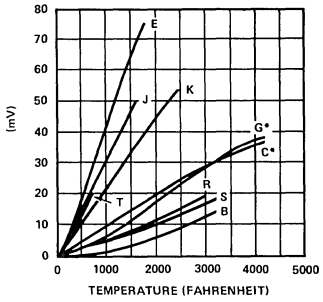
reference junction at 0°C or a bucking voltage set at room temperature may be used. The latter method is simpler, but is sensitive to changes in ambient temperature. Table I shows the output of several common types of thermocouples vs temperature.[2]

REFERENCES

(1) J.O.M. Jenkins, "IC Multiplexer Increases Analog Switching Speeds," Siliconix Application Note AN73-2, February 1973.

(2) The Omega Temperature Measurement Handbook (1975), Omega Engineering, Inc., Stamford, Conn.

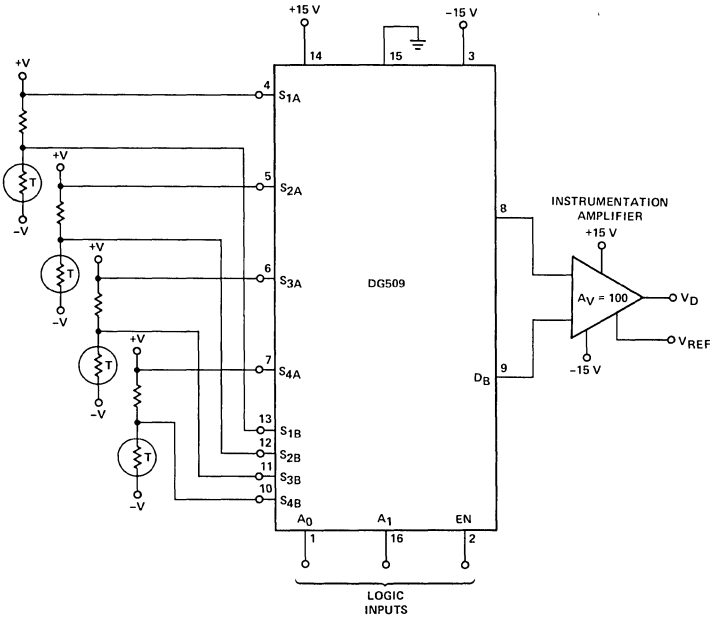
Table 1
Output Voltage vs Temperature of Several Common Thermocouples



ANSI SYMBOL	
T	Copper vs Constantan
E	Chromel vs Constantan
J	Iron vs Constantan
K	Chromel vs Alumel
G*	Tungsten vs Tungsten 26% Rhenium
C*	Tungsten 5% Rhenium vs Tungsten 26% Rhenium
R	Platinum vs Platinum 13% Rhodium
S	Platinum vs Platinum 10% Rhodium
B	Platinum 6% Rhodium vs Platinum 30% Rhodium

*Not ANSI Symbol

Used with permission of Omega Engineering, Inc., Stamford, Conn., 06907



Thermister Differential Multiplexing
Figure 25

7.8 DG300 Series Analog Switch Applications (AN76-6)

October 1976
Thomas J. Mroz

INTRODUCTION

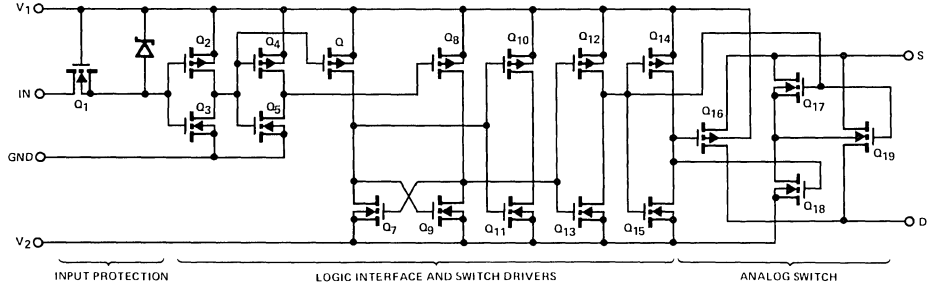
To round out its analog switch line, Siliconix has introduced the DG300 to DG307 analog switch family. The DG300 to DG307 switches were designed to approach the industry standard DG180 family of JFET switches in performance while keeping the economy and low power of CMOS circuitry, and offer fast switching (typically < 150 ns) and low ON resistance (< 50 Ω). Four switch functions, (dual SPST, SPDT, dual DPST, dual SPDT) are offered with TTL or CMOS compatible logic input options. The low ON resistance, fast switching speed and low power of these switches makes the DG300 family an excellent choice for sample and hold, Digital-to-Analog Converters, and multiplexing elements as well as other applications requiring low offsets, fast charging of capacitors and fast switching of analog signals. The SPDT functions offer break-before-make action which aids in simplification of system design.

DG300 Family Switch Structure

Figure 1 shows a partial schematic of a DG300 switch.

Device Q_1 along with the zener diode provide the input protection. This is accomplished by Q_1 being turned off whenever the input voltage exceeds the positive supply (V_1) and by the zener breakdown whenever the input goes more negative than $V_1 - V_{ZENER}$. Q_2 and Q_3 form the first input buffer and are designed to set the proper input threshold. The DG300 to DG303 thresholds are typically between 1.5 and 2.5 volts and are designed to interface with TTL gates employing pullups to +5 V. These switches can also be driven from CMOS gates using 5 to 15 volt supplies. If 15 volt CMOS drive is available, faster switching can be accomplished by using the CMOS input DG304 to DG307 switches.

DG304 to DG307 switch inputs have thresholds typically between 4 volts and 6 volts with ±15 V supplies and are designed to interface with inputs switching between ground and the +15 V supply. Q_4 through Q_{15} form additional buffers and create the necessary driving voltages for the switch devices, Q_{16} through Q_{19}. Q_{17} and Q_{18} are referred to as being body snatchers, not because of midnight escapades, but because they connect the body of Q_{19} to either its source or the negative supply. This reduces the ON resistance and the OFF leakage of this device.

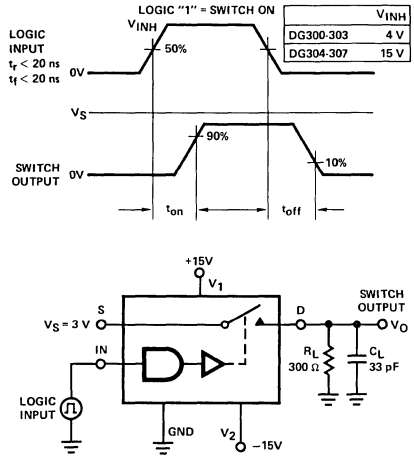


Partial Schematic of Typical Switch
Figure 1

PERFORMANCE CHARACTERISTICS

Switching Time

In measuring switching time it is important to remember that the turn-off time as seen at the load is highly dependent on the load time constant. The switching time test circuit is shown in Figure 2 below.

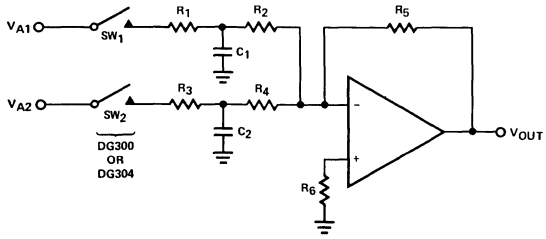


Switching Time Test Circuit
Figure 2

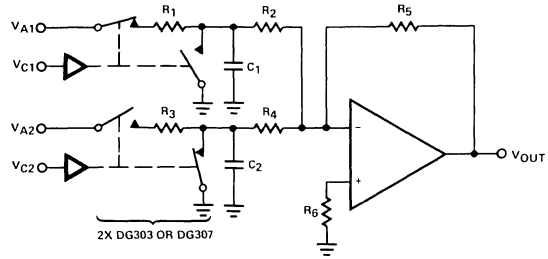
Turn-on time in the circuit shown in Figure 2 is governed primarily by the logic delay path and the $r_{DS(ON)}$ of the switch. The $r_{DS(ON)}$, C_{LOAD} time constant is normally shorter than the R_LC_L time constant. The two time constants are:

$$\frac{r_{DS(ON)} \times R_L}{r_{DS(ON)} + R_L} \times C_L \text{ for } t_{ON} \text{ and } R_L \times C_L \text{ for } t_{OFF}$$

These two time constants determine rise and fall times of the analog switch. When the switch is driving a high impedance, high capacitance load such as that shown in Figure 3, which is the input of a summing amplifier having some noise filtering, it may be necessary to add a second switch (Figure 4) for rapid discharge of the filter capacitor thus preventing offsets from occuring at the summing amplifier output.



Summing Amplifier
Figure 3

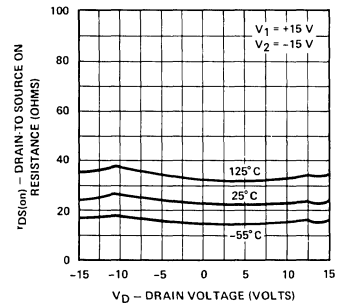


Improved Summing Amplifier
Figure 4

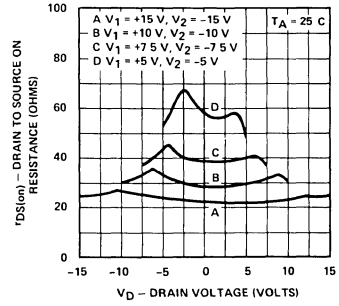
Channel ON Resistance

Another important specification of an analog switch is the channel ON resistance, $r_{DS(ON)}$. The $r_{DS(ON)}$ of the DG300 family of switches is typically below 40 ohms over the operating temperature range.

The two figures below show variations of $r_{DS(ON)}$ with respect to temperature (Figure 5) and supply voltage applied to the switches (Figure 6).



$r_{DS(on)}$ vs V_D and Temperature
Figure 5



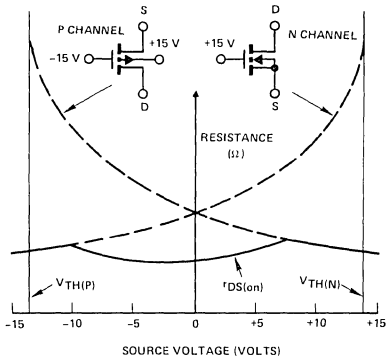
$r_{DS(on)}$ vs V_D and Power Supply Voltage
Figure 6

As shown by Figure 5, $r_{DS(ON)}$ increases as temperature increases. This is a typical FET characteristic due to the decreasing conductivity of silicon as temperature increases.

This decrease in conductivity is due to the shortening of the mean free path seen by the majority carriers of the device. The change of switch resistance with respect to temperature is approximately 0.1 Ω/°C.

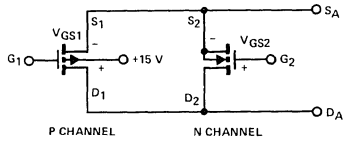
Figure 6 also shows $R_{DS(on)}$ variations with respect to analog signal voltage as a function of supply voltages. Supply variations are important because the maximum gate drive available for the switch output devices is determined by the supply voltages. Thus the change in $r_{DS(ON)}$ is proportional to the change in supply voltage.

The variation of $r_{DS(ON)}$ with respect to the analog voltage is due to the variation in the gate-source voltage of the "ON" switches as shown in Figure 7.



Resistance vs Source Voltage of P-Channel and N-Channel FETs
Figure 7

In Figure 8, the complementary output pair (for illustrative purposes) is shown in a very basic schematic. When the switch is ON, G_1 is tied to the negative supply and G_2 is tied to the positive supply. $V_{D1} = V_{S1} = V_{D2} = V_{S2}$. In order to understand the variation of $r_{DS(ON)}$ with respect to analog voltage, the complementary pair will be broken apart and the $r_{DS(ON)}$ of each device with respect to analog voltage examined.



Complementary Output Devices (Simplified)
Figure 8

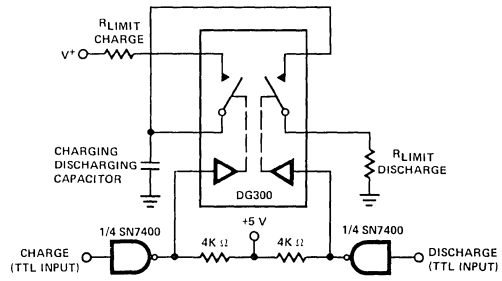
As Figure 7 indicates, the N-channel device with its gate tied to +15 V, begins to turn ON as its source voltage drops a threshold voltage below +15 volts. Thus as the analog voltage decreases from +15 volts to −15 volts, V_{GS} increases from 0 volts to 30 volts increasing the channel conductivity. The P-channel device has its gate tied to −15 volts, thus as the analog signal increases from −15 volts to +15 volts, its V_{GS} goes from 0 volts to −30 volts. This results in a decreasing channel resistance. The switch resistance is the parallel combination of these two devices and the bottom curve in Figure 7 results.

APPLICATIONS

The DG300 series of analog switches having fast switching and low $r_{DS(ON)}$ lend themselves to applications such as sample and hold and high speed multiplexing. Low $r_{DS(ON)}$ also means small offsets when switching integrators or amplifiers. Nearly constant ON resistance also means lower distortion when switching into lower impedance loads.

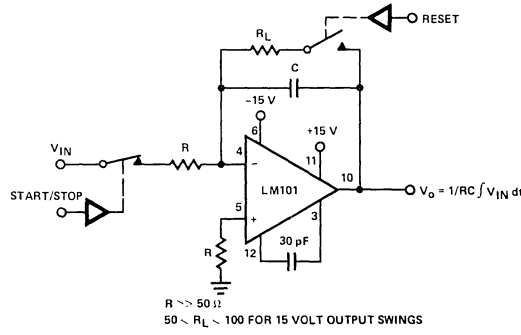
Charging and Discharging Capacitors

When charging or discharging capacitors, it is important not to exceed maximum ratings of the switch. Current through the switch must be limited to 30 mA continuous or a 100 mA pulse for 1 millisecond or less having a 10% duty cycle. Exceeding maximum ratings could mean poorer reliability than could otherwise be expected. One method of preventing excessive current is by using current limiting resistors in series with the switch as shown in Figure 9. If voltage differentials between the switch input and the capacitor are small, these resistors may not be necessary because the switch resistance itself would be sufficient to limit current.



Using Current Limiting Resistors in Capacitive Charge/Discharge Circuits
Figure 9

In the integrator of Figure 10, R_L controls the discharge rate of the capacitor. During reset to zero volts, the reset switch is closed and the start/stop switch is open. Opening the start/stop switch with the reset open will hold the output of the integrator at its present value.



Integrator With Analog Reset and Start/Stop Capability
Figure 10

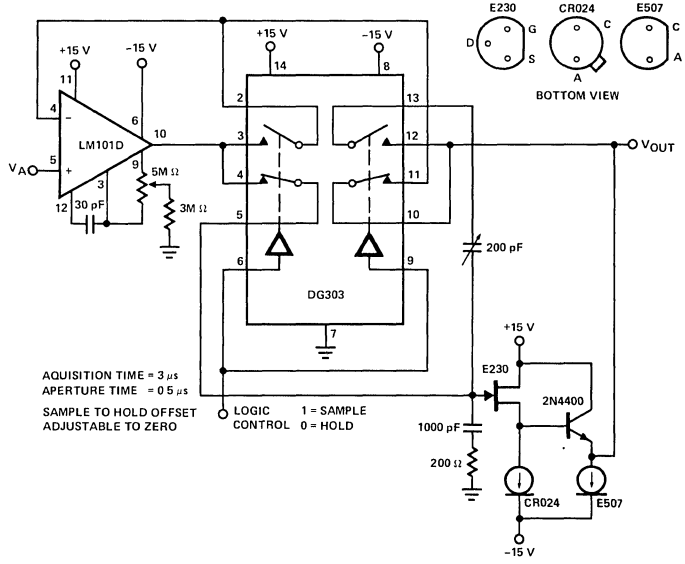
Charge Cancellation

Figure 11 shows a sample and hold circuit using the DG303 dual SPDT switch. Any analog switch when opened will inject charge into the source and drain nodes due to gate to source and gate to drain capacitance. This charge when injected into a sample and hold capacitor will create offset errors in the sample and hold output during hold. This error can be eliminated using another switch to inject charge into a small storage capacitor (200 pF) during the sample period which is then subtracted off during the hold period.

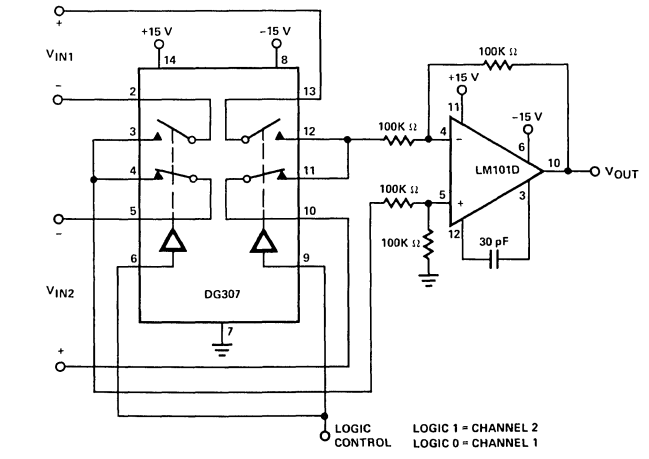
Fast switching times and low $r_{DS(ON)}$ of the DG303 allow fast data aquisition with aquisition times of 3 μs possible.

Fast Data Multiplexing

Having high switching speed, the DG300 series switches are ideal for fast multiplexing of data. Figures 12, 13, and 14 are applications of various DG300 switches employing their high speed in switching data.



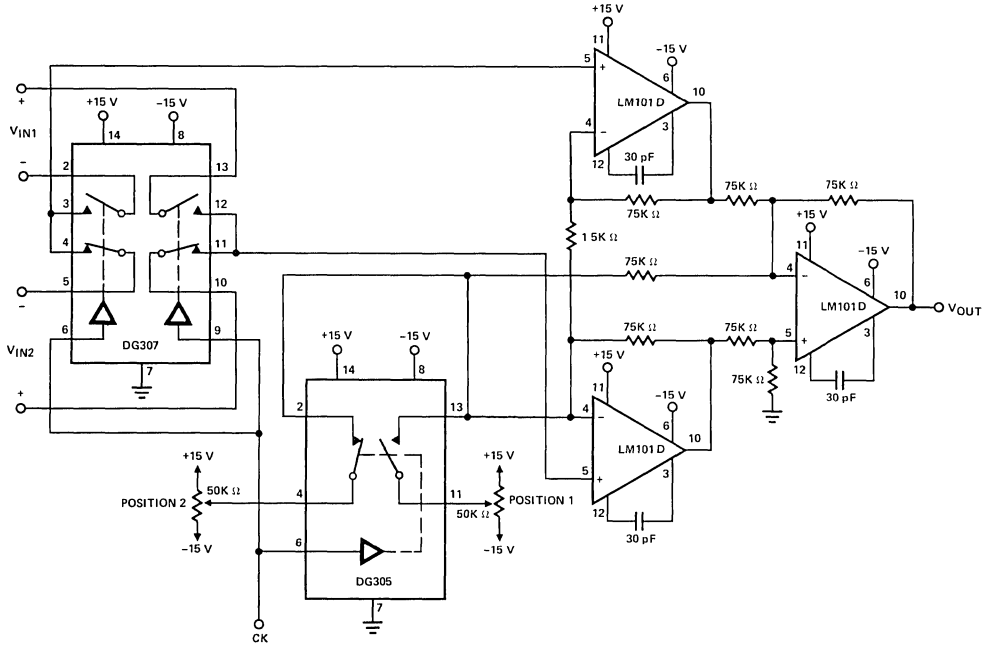
Sample and Hold
Figure 11



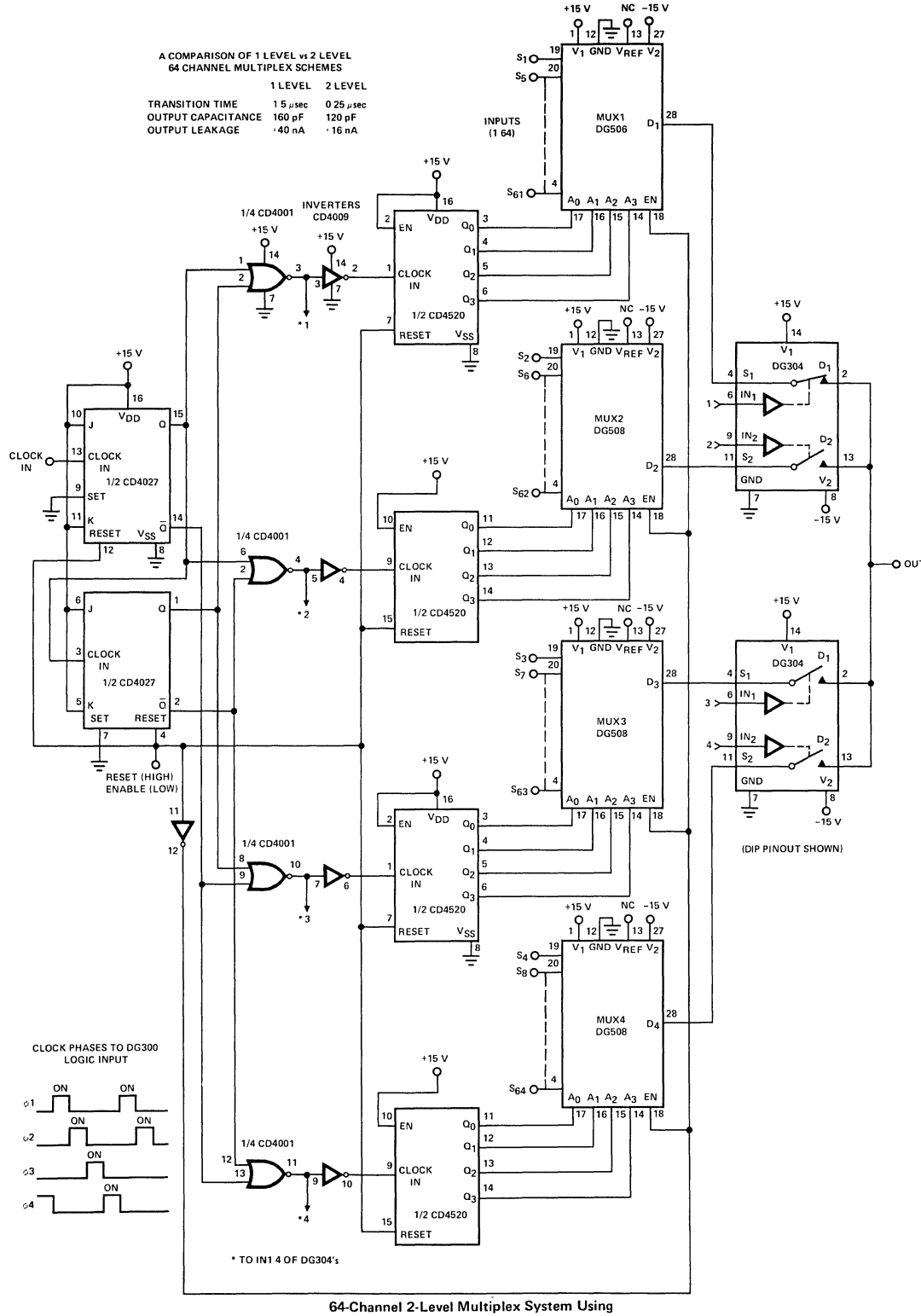
Basic Switched Differential Amp
Figure 12

The high switching speed of the DG304 is taken advantage of in the 64-channel two level multiplex system of Figure 14. This circuit employs 4 each DG506 16-channel multiplexers as the first MUX level and uses the high speed DG304's in the second level to switch between DG506 outputs. CMOS digital logic forms the address logic for the multiplexers as well as the DG304's.

As one multiplexer is being sampled at the output, the other multiplexers are being switched to the next address line. This allows the overall system transition time to be shortened from 1.5 μsec to 0.25 μsec. The two level system also lowers output node capacitance and output leakage (refer to Reference 5 for details).



2-Channel to 1-Channel Chopping Differential Amplifier With Position Adjustment
Figure 13

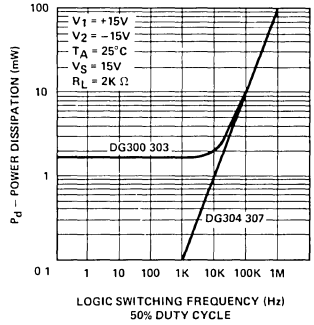


64-Channel 2-Level Multiplex System Using DG304 as High Speed Switches
Figure 14

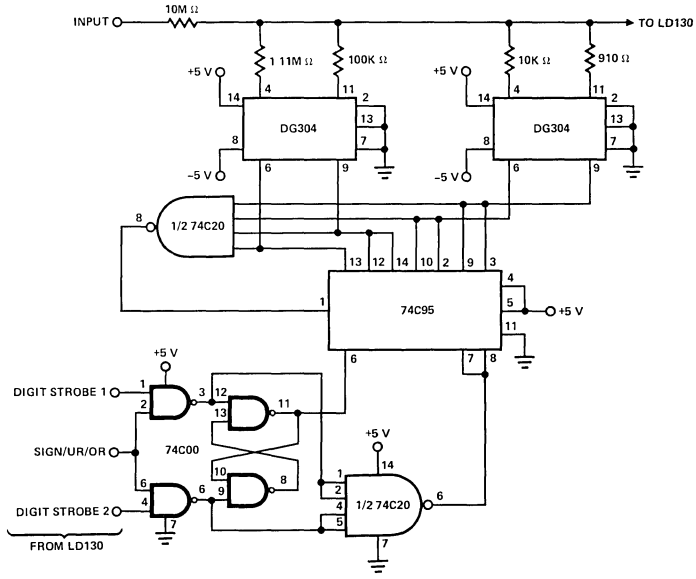
Battery or Low Power Applications

The DG300 series of switches are inherently Low Power and are ideal candidates for applications using battery supplies. Figure 15 shows the variation of device power dissipation versus the switching frequency of the switch. It can be seen that in low frequency switching the power dissipation is negligible. One application for which this switch is ideal is in autoranging circuits for battery operated Digital Volt Meters as shown in Figure 16.

A reduction of approximately 4 mA of supply current is realized when substituting two DG304s for the DG201 originally used in this autoranging circuit. Package size reduction can be obtained by using metal cans instead of Dual-in-lines.



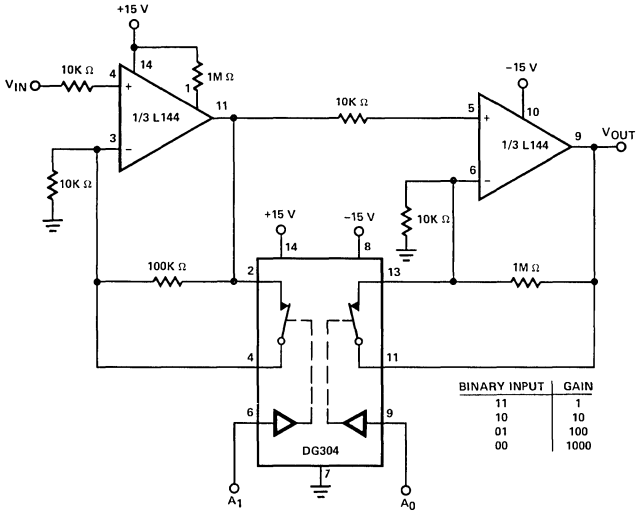
Device Power Dissipation vs Switching Frequency
Figure 15



Note: See Design Aid DA76-3 for DVM circuit detail. (Ref. 3)

Low Power Autoranging System for LD130 DVM
With ±5 V Supplies
Figure 16

Figure 17 is the schematic of a binary addressed amplifier in which the gain increases by decades as the binary input decreases from 1,1 to 0,0. Its minimum gain, as shown in the table, is 1 and its maximum gain is 1000. Since the switch is static in this type of amplifier the power dissipation of the switch will be less than a tenth of a milliwatt.



Low Power Binary to 10^n Gain Low Frequency Amplifier
Figure 17

The low power of the DG307 also makes it ideal for use with the low power programmable triple op amp, the L144, in an active filter. Figure 18 shows the use of the DG307 in a switchable center frequency active filter, allowing a decade change in center frequency. Additional information on the L144 and the active filter circuit can be found in References 6 and 7.

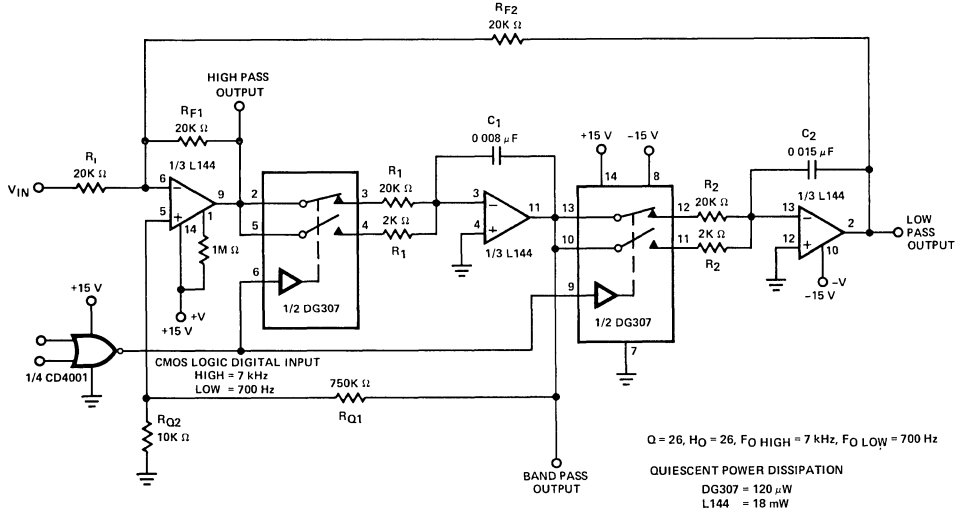
Table 1
Design Procedure for the State Variable Active Filter
Given: f_0 (Resonant Frequency), H_0 (Gain at the Resonant Frequency) and Q_0

STANDARD DESIGN
(Assumes Infinte Op-Amp Gain)

1. CHOOSE $C_1 = C_2 = C$, A CONVENIENT VALUE
2. LET $R_1 = R_2 = R$
3. THEN $R = \dfrac{1}{2\pi \times f_o \times C}$
4. CHOOSE $R_{11} = R_{12} = KR$, WHERE R_{11}, R_{12} = A CONVENIENT VALUE
   AND $K = \dfrac{H_o}{Q_o}$
   IF H_o IS UNIMPORTANT (i.e., GAIN CAN BE ADDED BEFORE AND/OR AFTER THE FILTER), CHOOSE K = 1
5. LET R_{Q1} = A CONVENIENT VALUE
6. THEN $R_{Q2} = \dfrac{R_{Q1}}{(2 + K) \times Q_o - 1}$

A (f_o) = THE NOMINAL OP AMP GAIN AT THE RESONANT FREQUENCY.

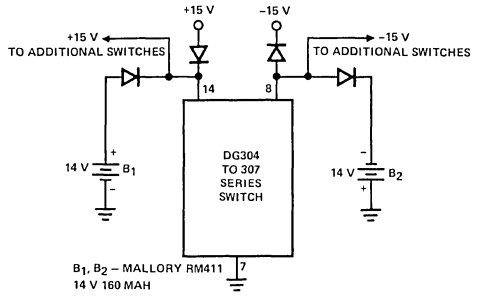
GBWP = THE NOMINAL GAIN-BANDWIDTH PRODUCT OF THE OPERATIONAL AMPLIFIER.



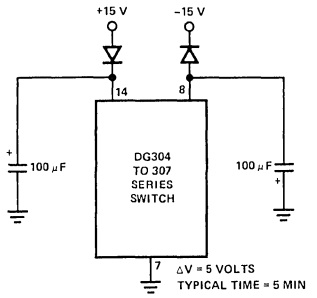
Low Power Active Filter With Digitally Selectable Center Frequency
Figure 18

An advantage of the DG304 to DG307 family of switches due to their low power consumption is the ability to use batteries or capacitors to supply standby power to the switch. In this way errors at analog output and shorting of signals can be avoided when supply power fails. This method would also prevent loading of the analog signal by the switch which could prevent the use of the signal in other portions of a system. Figures 19 and 20 show methods of implementing standby power.

Battery lifetime should be well over 1 year with continuous standby.



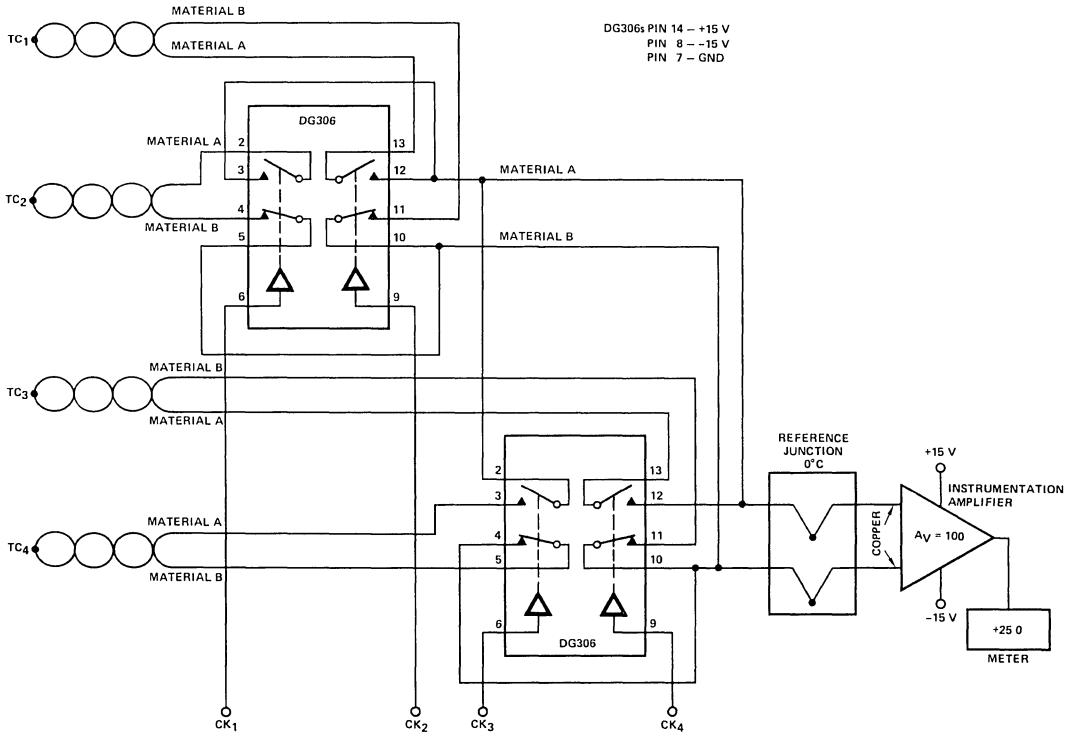
Long Term Supply Standby
Figure 19



Short Term Supply Standby
Figure 20

Thermocouple Applications

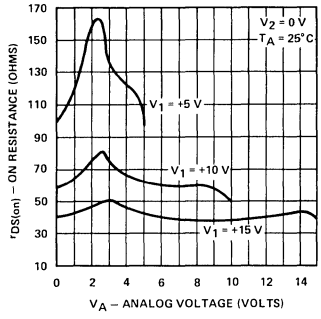
Because silicon in contact with aluminum creates a thermocouple, low power dissipation by the integrated analog switch will mean lower offset voltages added to the thermocouple voltage. Thus, lower power dissipation translates into better potential accuracy. The DG300 series of analog switches do quite well in this type of application. Figure 21 shows a typical schematic of a thermocouple switching circuit. It is necessary to switch the thermocouples differentially in order to cancel any thermal offsets due to the switch.



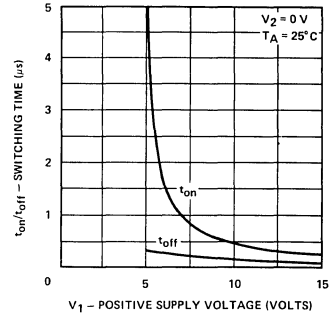
Thermocouple Multiplexing
Figure 21

Single Supply Operation

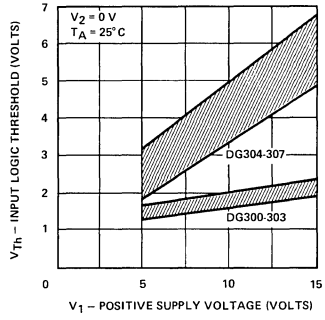
The DG300 series of analog switches will switch positive analog signals while using a single positive supply. This will allow use in many applications where only one supply is available. The trade-offs or performance given up while using single supplies are: 1) Increased $r_{DS(ON)}$; 2) slower switching speed. Typical curves for aid in designing with single supplies are supplied in Figures 22 to 24. As stated in the absolute maximum ratings section of the data sheet, the analog voltage should not go above or below the supply voltages which in single supply operation are V_1 and 0 volts.



$R_{DS(on)}$ vs Analog and Positive Supply Voltage With V_2 = 0 V
Figure 22



Switching Time vs V_1 – Positive Supply Voltage
Figure 23

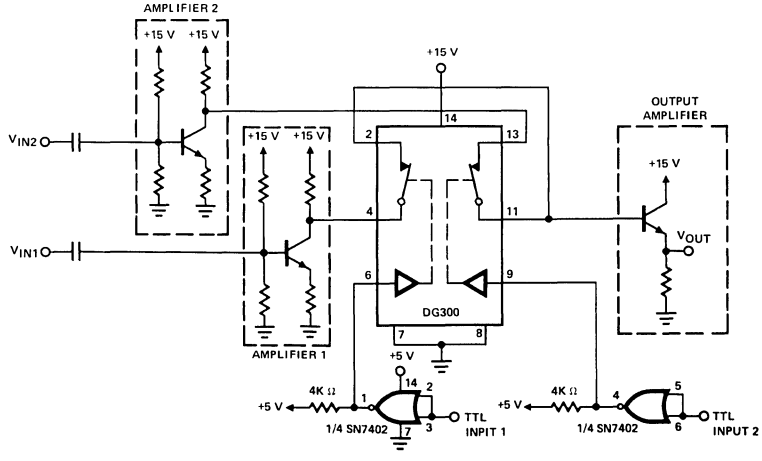


Input Threshold Voltage vs Positive Supply
Figure 24

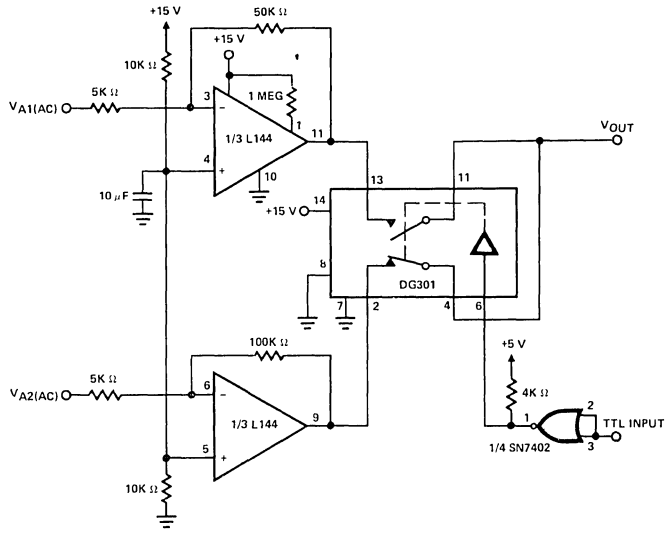
Single Supply Range:
(V_2 and GND Tied Together)
V_1: +5 V to +25 V

Analog Signal Range:
$V_2 \leq V_{ANALOG} \leq V_1$

Figures 25 and 26 demonstrate methods of interfacing analog switches to single supply DC coupled amplifiers.

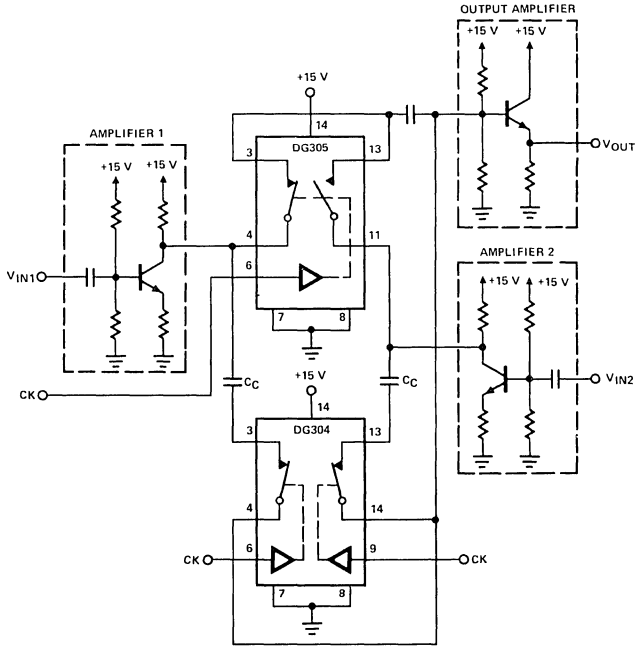


Switching Single Supply Amplifiers Using the DG300
Figure 25



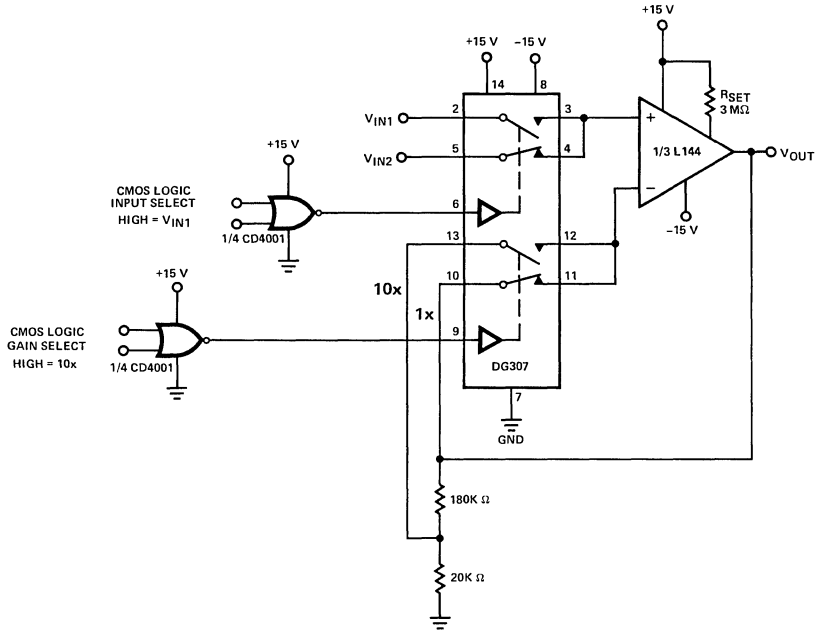
Single Supply Op Amp Switching
Figure 26

As shown in Figure 27 when switching capacitor-coupled analog signals, the coupling capacitor should appear either before or after but not on both sides of the switch. This is necessary to keep a positive bias on the switch drain and source when the switch is turned on.

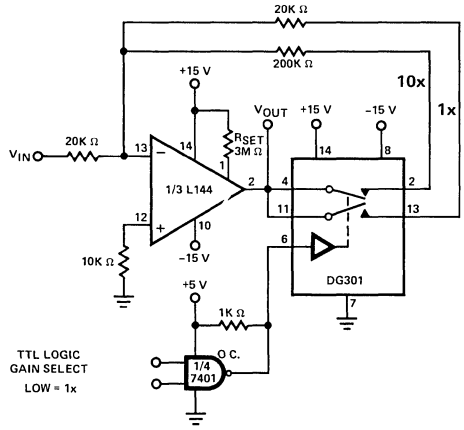


Proper Methods for Interfacing Capacitive Coupled Outputs to Analog Switches
Figure 27

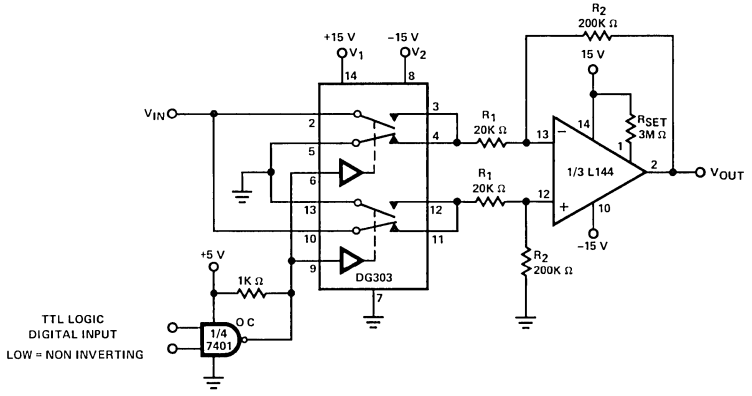
CHAPTER 7



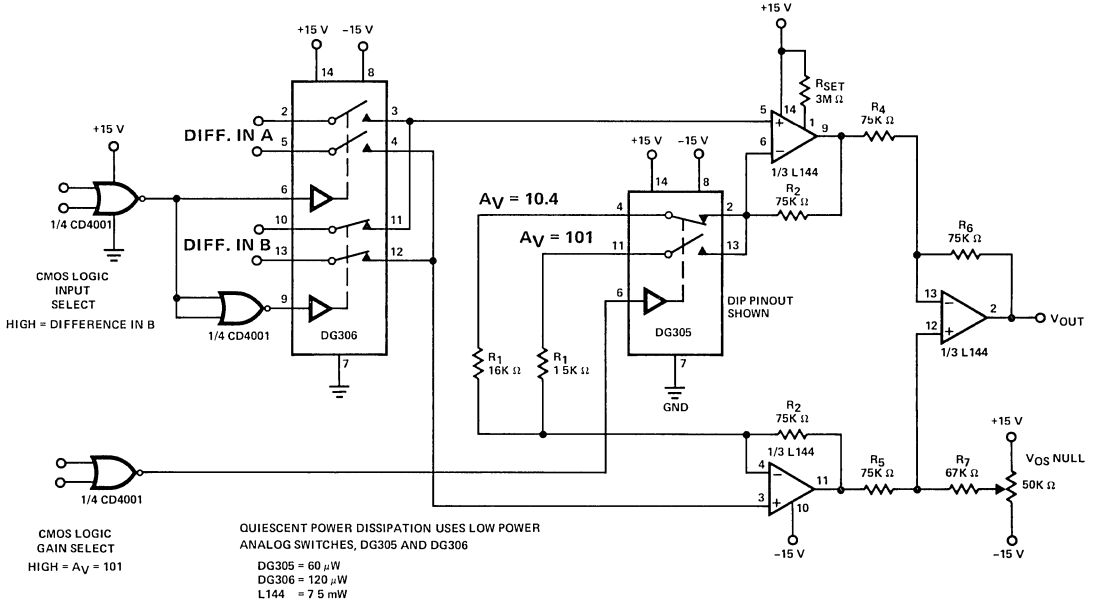
Low Power Non-Inverting Amplifier with Digitally Selectable Inputs and Gain
Figure 28



Low Power Inverting Amplifier with Digitally Selectable Gain
Figure 29



Polarity Reversing Low Power Amplifier
Figure 30



R_{SET} programs L144 power dissipation, gain-bandwidth product. Refer to AN73-6 and the L144 data sheet.

Voltage gain of the instrumentation amplifier is:

$$A_V = 1 + \frac{2R_2}{R_1} \quad \text{(In the circuit shown, } A_{V1} = 10.4, A_{V2} = 101\text{)}$$

Low Power Instrumentation Amplifier with Digitally Selectable Inputs and Gain
Figure 31

REFERENCES

1. Lee Shaeffer, "CMOS Analog Switches – A Powerful Design Tool," Siliconix Application Note AN75-1, July 1975.
2. Gary Dixon, "Analog Switches in Sample and Hold Circuits," Siliconix Application Note AN74-2, Jan. 1976.
3. Gary Grandbois, "Build an Autoranging DMM with the LD130 A/D Converter," Siliconix Design Aid DA76-3, June 1976.
4. "Siliconix Analog Switch Data·Book," pp. 1-115 to 1-124, June 1976.
5. J. Jenkins, "IC Multiplexer Increases Analog Switching Speeds," Siliconix Application Note AN73-2, April 1976.
6. Marvin K. Vander Kooi, "L144 Programmable Micro-Power Triple Op Amp," Siliconix Application Note AN73-6, Jan. 1975.
7. Lee Shaeffer, "Op Amp Active Filters – Simple to Design Once You Know the Game," EDN Magazine, April 20, 1976.

7.9 Multiplexer adds Efficiency to 32-Channel Telephone System (TA73-1)

Analog signals are time-division multiplexed by recently developed integrated circuits in a two-level switching scheme; the technique promises to add speed and efficiency to digital telephone systems

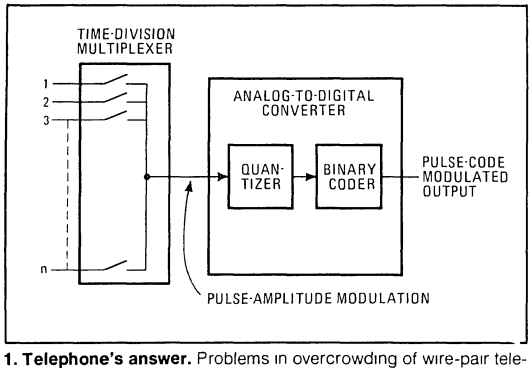
by John A. Roberts* and J.O.M. Jenkins, Siliconix Ltd., *Swansea, England*

☐ Time-division multiplexing has gained wide acceptance in recent years as a means of combining multiple telephone channels on wire-pair transmission lines that previously accommodated only one channel. Combined with pulse-code-modulation (PCM) circuitry to convert the sampled signals to a digital format, the multiplexing techniques have generally reduced size, power consumption, and costs of plant equipment.

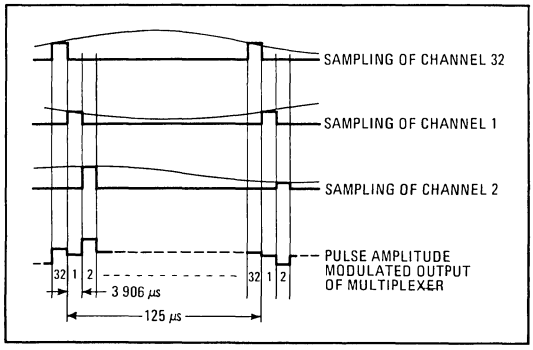
To achieve minimum signal loss and distortion in such systems, much effort has been directed toward building multiplexers that switch from channel to channel with minimum output rise and fall times. Such a multiplexer design recently built and tested provides 150-nanosecond switching time, an order of magnitude faster than presently available circuits.

This high-speed switching is achieved by applying biphase control logic to a two-level multiplexer arrangement that takes advantage of the fast rise times and the break-before-make action of newly developed integrated-circuit multiplexers.

*Now with Microsystems International Ltd., Ottawa, Canada



1. Telephone's answer. Problems in overcrowding of wire-pair telephone-transmission lines are lessened by using analog time-division multiplexers followed by a-d converters

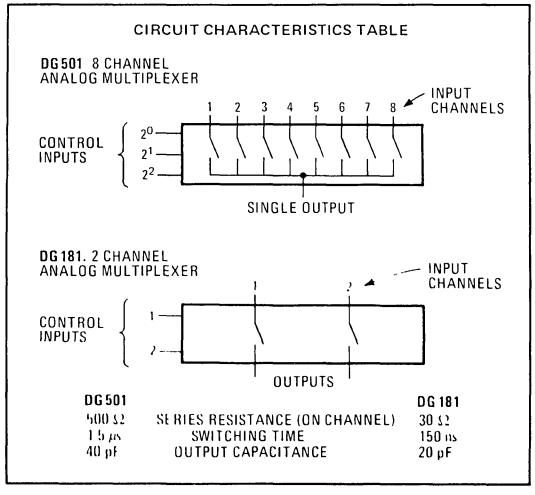


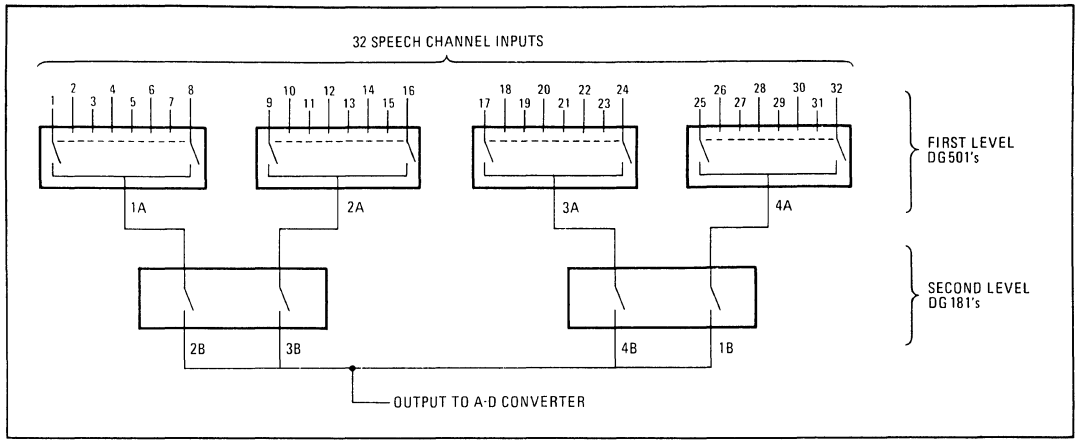
2. Tight fit. For accurate reconstruction of a 3.3-kHz telephone signal, it must be sampled at a rate of about 8 kHz, or once every 125 μs. The hierarchy of today's telephone system makes it highly desirable to multiplex 32 speech channels during this period

Telephone system requirements

A generalized system used to time-division multiplex voice signals is shown in Fig. 1. After the signals on each of analog channels have been sampled, each sample is quantized and coded into a PCM format. The new design focuses on the analog multiplexer, which feeds the analog-to-digital converter.

The sampling rate for each of the incoming channels is determined by the desired bandwidth of the voice signals being sampled, while sampling dwell time is fixed by the number of channels that must be sampled. Nyquist's sampling theory[1,2] states that any transmitted waveform that is band-limited to a maximum frequency of f_L can be accurately reconstructed from periodic sam-





3. Two-level multiplexing. Output-node capacitance is significantly reduced when a second level of multiplexers is added Interchannel switching time, however, is still determined primarily by the speed of the first-level switches

ples taken at a rate as slow as $2f_L$.

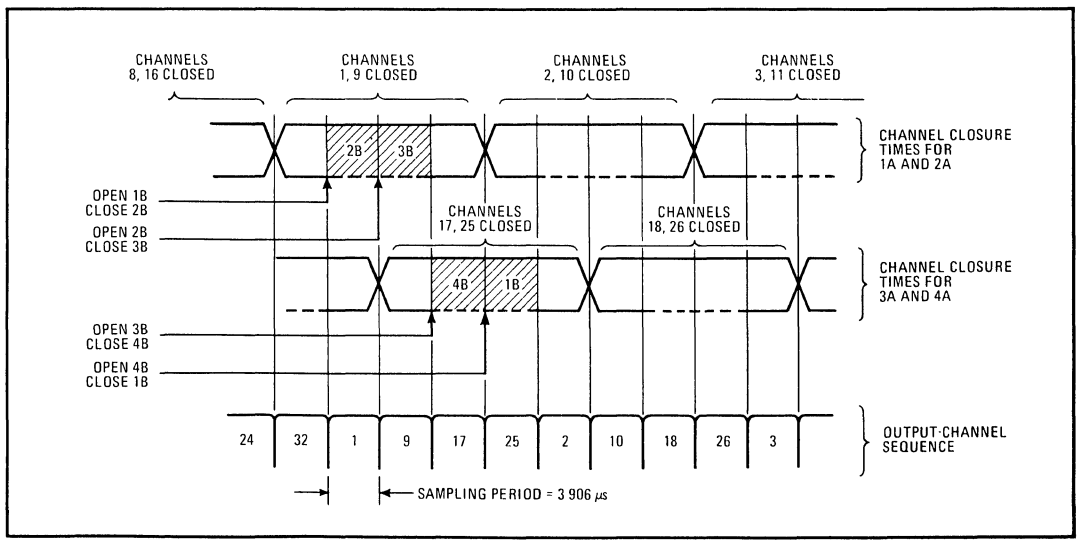
In practice, however, filters do not provide ideal cutoff at f_L, and a somewhat higher sampling rate must be tolerated. For example, to achieve less than 1% error in reconstruction accuracy, the sampling rate must be at least twice the frequency at which the unwanted signals above cutoff are reduced by 40 dB.[2,3] Thus, to relax difficult filtering requirements at the input-to-sampling circuitry, a voice bandwidth that is nominally limited to about 3.3 kHz is usually sampled at an 8-kHz rate, or once every 125 μs.

Single-level multiplexers

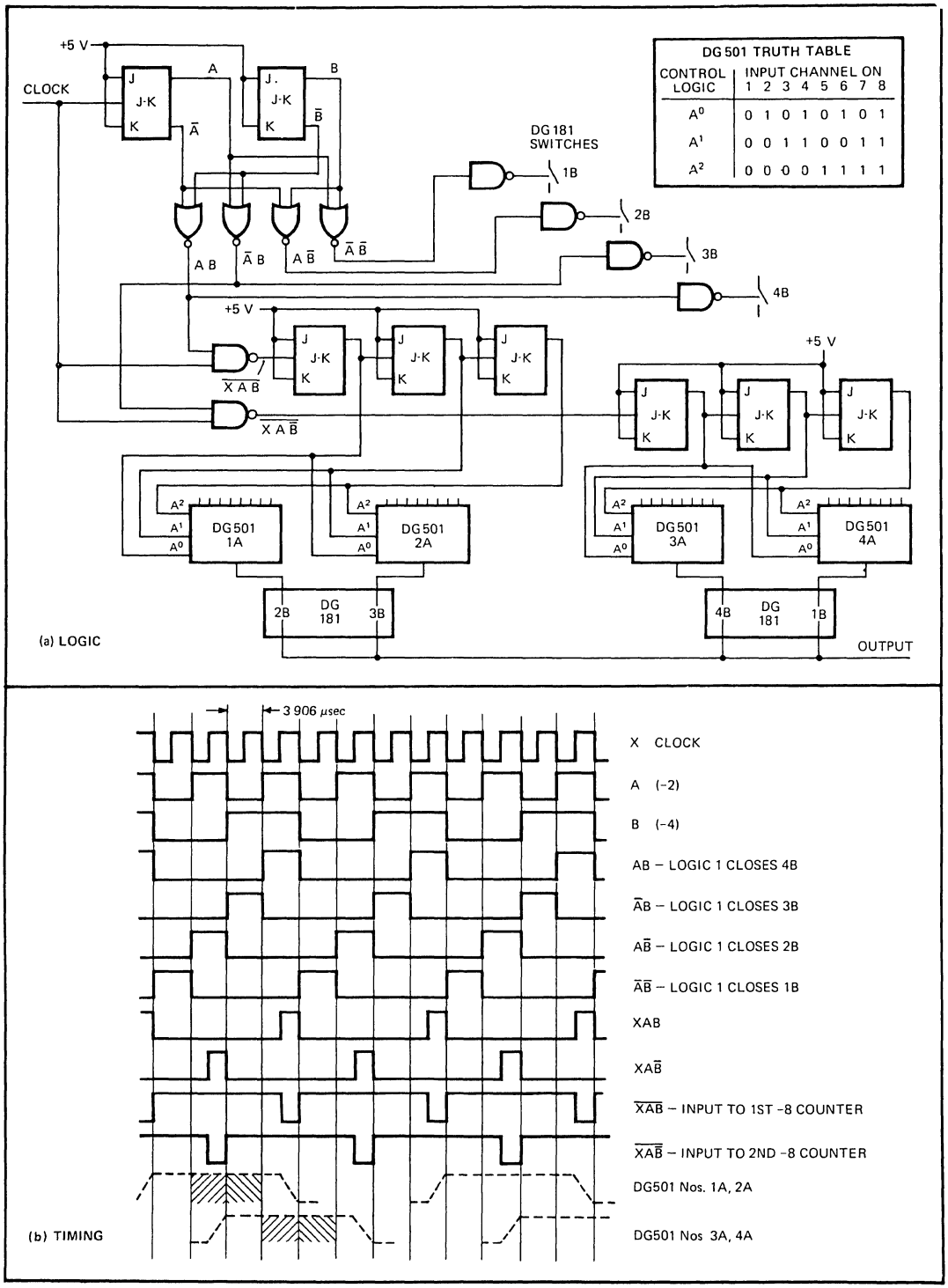
The standard configurations of today's telephone systems dictate that a fundamental group of 32 channels be multiplexed onto one line. Therefore, with a sample frame time of 125 μs, each of 32 multiplexed channels is sampled for 125/32, or 3.906 μs, as Fig. 2 indicates.

Conventional multiplexing networks can be implemented with either descrete components or integrated circuits, such as the Siliconix DG501 (see table). This circuit multiplexes eight input channels with a switching time between channels of 1 to 2 μs. A 32-channel multiplexer is constructed simply by paralleling four DG501s. Thus, in single-level switching, each of the 32 analog input channels is multiplexed through a single switching bank.

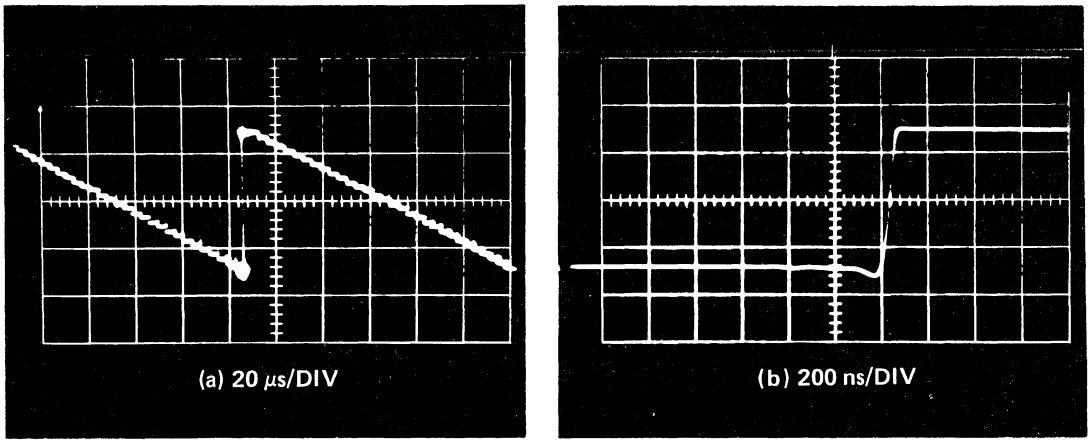
The problem with such a system stems from the relatively slow 1-2-μs switching times between channels. Depending on the design of the particular multiplexer, there can either be an overlap between sampling pulses, which leads to crosstalk between channels, or a large separation between samples, which reduces the sampling time of a particular channel. The reduced



4. Phase II timing. By adding two-phase control logic to the two-level multiplexer of Fig 3, the full advantage of the 150-ns switching speed of the DG181 circuits is realized Channel numbers correspond with those in Fig 3



5. Logic hardware. TTL control circuits (a) implement timing (b) required in two-phase, two-level multiplexing system. First-level DG501 switches are MOS circuits, and J-FET technology gives the faster switching times needed in the DG181 second-level switches.



6. Quick switch. Thirty-two dc levels are sampled in a prototype multiplexer to demonstrate switching speed of the two-level two-phase design. Largest single transition, from −3 to + 3 volts, is expanded in the lower trace. Vertical scale for both traces: 2 V per division.

sampling time results in lower multiplexer efficiency.

Added to the 1-2-μs switching time is a delay associated with the increased output-node capacitance when multiple channels are combined. For four DG501s (32 channels), the added delay is about 200 ns. These delays further reduce the effective sampling time and bring some uncertainty into the timing strobe for the a-d converter. The node-capacitance problem can be eased to some extent by a high-performance sample-and-hold circuit between the multiplexer and the a-d converter. However, the 1-2-μs switching times remain, and this problem becomes acute for signals obtained from sources with output impedances of 2 kilohms and above.

Two-level multiplexing

System-response time can be improved by reducing the output-node capacitance. This is achieved by using a two-level multiplexing system as shown in Fig. 3.[4] Here, circuits with lower output capacitance (such as the DG181, with performance shown in the table) are placed in the second multiplexing level, which feeds the a-d converter.

The DG181 circuits can switch at a speed of 150 ns. The full advantages of these speeds, however, are not realized, since interchannel sampling time is still limited by the 1-2-μs rise times of the DG501s.

A timing sequence that makes maximum use of the switching rise times of the DG181s (and therefore results in extremely high sampling efficiency) can be achieved by applying control logic to the two-level multiplexer in a manner which will give the sampling sequence shown in Fig. 4. The faster switching speed and the break-before-make action of the DG181 virtually removes the possibility of overlap.

The problems caused by the relatively slow switching time of the DG501 are eliminated by ensuring that the first channels of multiplexer switches 1A and 2A (Fig. 3) are already fully closed when 2B and 3B, respectively, are closed, and that the first channels of switches 3A and 4A are fully closed when 4B and 1B, respectively, are closed. This sequence is then repeated for each of the eight channels of the DG501s, and the complete cycle is again repeated.

Two-phase control logic

The timing requirement and logic-control layout for the complete circuit are shown in Figs. 5a and 5b. Waveforms A and B are obtained from the input clock waveform by an asynchronous divider. The A and B waveforms are combined to give AB, $A\overline{B}$, $\overline{A}B$ and $\overline{A}\,\overline{B}$ which are needed to close the DG181 gates sequentially. Functions XAB and $XA\overline{B}$ then clock two three-bit asynchronous counters. A delay of two clock periods exists between XAB and $XA\overline{B}$ so that the count sequence applied to the second and third multiplexer is suitably delayed.

A prototype multiplexer with two-phase control logic has been constructed and successfully tested. Series 7400 TTL circuitry is used to implement the timing and control logic. First-level DG501 switches are MOS circuits, while J-FET technology gives the faster switching times needed in the DG181 second-level switches.

To simulate all 32 analog inputs to the multiplexer, a voltage-divider network of series resistors is connected across a ±3-volt supply. Thus, 32 dc voltage levels are consecutively tapped off the network and applied to the multiplexer input. The multiplexer output is displayed on the oscilloscope, as shown in Fig. 6a. As can be seen, the largest transition is from −3 to +3 V. In Fig. 6b, this 6-V transition is demonstrated as being accomplished in less than 100 ns.

If low-power TTL or diode-transistor logic is used in the control circuits, synchronous counters may be necessary to eliminate cumulative flip-flop delays. Although the system shown is designed for negative-edge-triggered J-K flip-flops, the circuitry can be rearranged quite simply for almost any bistable logic element. □

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7.10 Designing with Monolithic FET Switches (TA73-2)

INTRODUCTION

Field-effect transistor switches have become increasingly common components of analog multiplex systems, sample-and-hold circuits, and even digital switching circuits. The major advantages of field-effect transistors (FETs) include an ON-to-OFF current ratio of 10^9, a relatively simple equivalent ON circuit (resistive and bilateral), inherent high-speed switching capability and, if properly used, a high degree of control-signal isolation.

MOSFETs are Simple

Among solid-state switches, the MOSFET switch is the simplest to use. The switch itself is easy to construct, and the ON/OFF drive circuitry is quite basic (Figure 1). As the PMOS gate is forced negative with respect to the source, the resultant field attracts holes or p-type carriers, forming a conductive p-channel (resistive path) between source and drain. The point where conduction begins is called the threshold voltage V_{TH}. As gate-to-source voltage V_{GS} is forced more and more negative, the conductive channel widens and the drain-to-source resistance r_{DS} decreases. V_{TH} is commonly −3 V to −4 V. However, for a useful ON resistance of 200 ohms, it is necessary to force V_{GS} to −10 V.

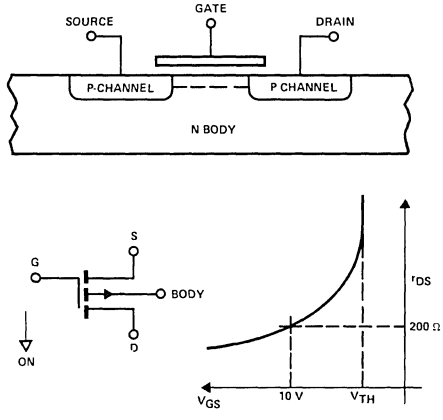

Figure 1. Cross sectional representation, schematic and threshold characteristics for a p-channel enhancement mode MOSFET.

Three basic types of PMOS driver-gates are shown in Figure 2: a basic FET and driver, a PMOS driver-gate employing both FETs and bipolar devices, and an all-PMOS unit. The

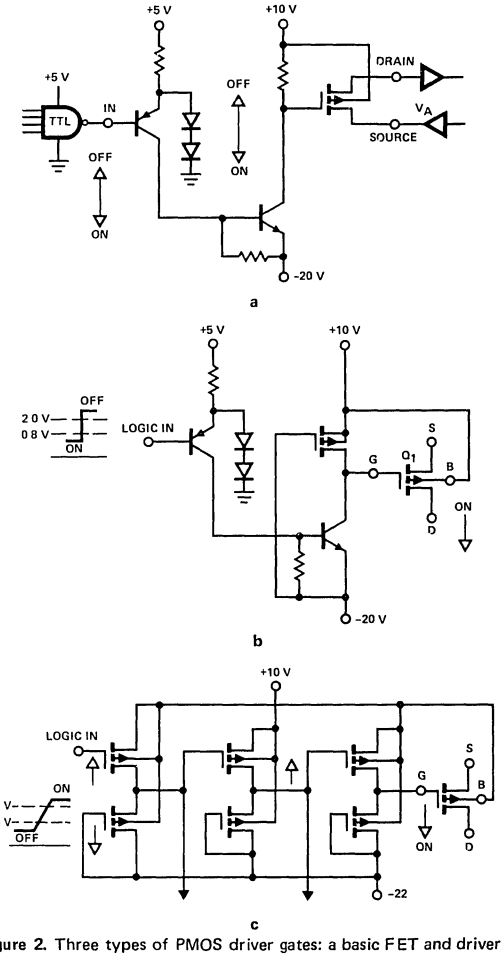

Figure 2. Three types of PMOS driver gates: a basic FET and driver (a), FETs combined with bipolars (b), and an all-PMOS unit (c).

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CHAPTER 7

gate is direct-driven by a level-shifting circuit that also serves as an amplifier, since it converts TTL logic signals (0.8 V to 2.0 V) into the −20 V to −10 V gate signals required to turn the FET ON or OFF. This range of drive-gate amplitude permits switching an analog signal of ±10 V. In these circuits, when the driver is ON, the PMOS gates are at −20 V.

Examining the main drawbacks of PMOS driver-gates, a portion of Figure 1 is modified to show the effect of analog voltage, V_A, on the gate (Figure 3). The chief disadvantage of the PMOS gate is the 3:1 ratio in $r_{DS(on)}$ for analog voltages varying between −10 V and 10 V. A second disadvantage lies in the requirement for 10 V and −20 V supplies (Figure 2), which is often a problem in analog systems built around the typical ±15 V op amp power supply.

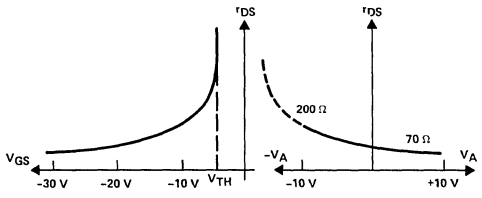


Figure 3. Threshold characteristic (Figure 1) modified to show the effect of analog voltage V_A on the gate.

An ideal means of avoiding variation of r_{DS} with analog signal voltages is to use a CMOS gate. The CMOS switch uses two enhancement-mode MOSFETs in parallel (one PMOS and one NMOS) between each source and drain terminal (Figure 4). The NMOS FET is similar to a PMOS FET, save for changed polarities. To turn the NMOS FET ON, V_{GS} is made more positive than $V_{GS(TH)}$, which is now 3 V to 4 V.

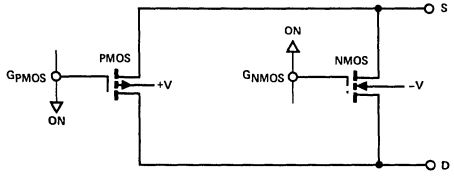


Figure 4. CMOS switch formed from PMOS and NMOS FETs connected in parallel.

The basic CMOS switch is derived by connecting the PMOS and NMOS FETs in parallel. The switch is turned ON by driving the PMOS gate negative, and the NMOS gate positive simultaneously (Figure 5a). Using "desirable" ±15 V supply voltages, assume that the analog signal voltage is $V_A = 0$. $V_{GS(P)}$ is −15 V and $V_{GS(N)}$ is 15 V. Both FETs are ON, and r_{DS} of the complementary switch is the parallel combination of $r_{DS(P)}$ and $r_{DS(N)}$ (around 70 ohms for larger switches).

In Figure 5b, for $V_A = 15$ V, $V_{GS(P)}$ is −30 V, but $V_{GS(N)} = 0$. The NMOS FET is OFF, but since the PMOS FET has twice the necessary V_{GS}, that FET is "twice as ON." R_{DS} is again about 70 ohms.

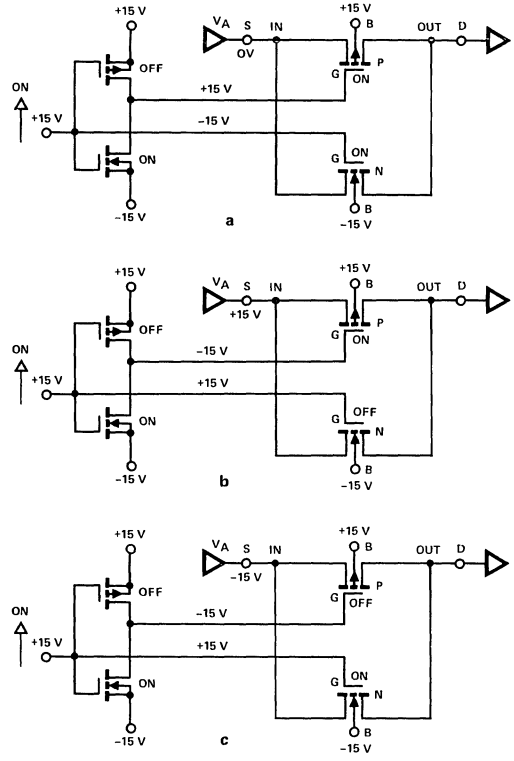


Figure 5. Resistance through the PMOS and NMOS parallel combination remains about 70 ohms for three different ON conditions.

In Figure 5c, for $V_A = -15$ V, $V_{GS(N)}$ is 0 while $V_{GS(P)}$ is 30 V. The PMOS FET is OFF while the NMOS FET has an r_{DS} of approximately 70 ohms. It is important that the relative sizes of the NMOS and PMOS FETs be balanced so that r_{DS} will be the same whether $V_A = 15$ V or −15 V. If the PMOS and NMOS FET sizes are properly matched, then one FET will compensate for the other during varying analog voltage signals, and a nearly constant $r_{DS(on)}$ (±10%) will be achieved for an analog signal range equal to the supply voltages.

Like the PMOS switch, the analog signal in a CMOS switch cannot exceed the positive supply voltage. Neither can the analog signal exceed the level of the negative supply voltage (Figure 6).

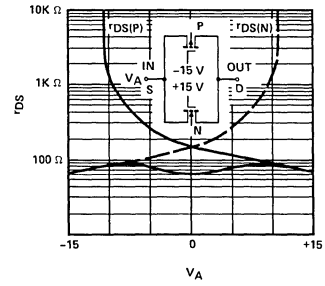


Figure 6. The CMOS switch's analog signal (V_A) range is equal to ± supply voltage.

Another advantage of the CMOS switch (shared with CMOS logic) is that driver stages, including all decode gates, have quiescent power requirements of nearly zero.

A number of CMOS switches are available today, ranging from simple dual spst devices to 16- and dual 8-channel multiplexers in a single package. CMOS construction puts both n-channel and p-channel devices on a common substrate.

The JFET Approach

CMOS technology is responsible for several new driver-gate switch combinations. One very important technique produces junction FET switching circuits. The cross-section of an idealized JFET is shown in Figure 11.

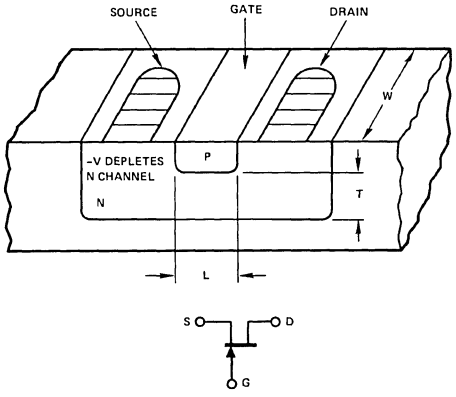


Figure 7. Cross sectional representation and schematic for a JFET.

Junction FETs are depletion-mode devices. When $V_{GS} = 0$, the FET is ON. The gate of a JFET surrounds the channel and is not separated by an insulating oxide layer, as is the case in MOSFETs. As a result, changes in channel current per change in gate-source voltage are higher in JFETs than in MOSFETs. Directly related to this characteristic is the ability of the JFETs to produce a lower r_{DS} than can be developed in a MOSFET with the same area and the same ON capacitance.

On the other hand, the JFET is harder to drive than the MOSFET. The drive problem arises in the gate to channel p-n junction. In the MOSFET, the gate may either be positive or negative relative to the source and drain (within breakdown limits), and current will not flow in the gate circuit. This MOSFET characteristic permits direct connection of the gate to a level-shifting driver circuit. Conversely, if the gate of an n-channel JFET becomes positive with respect to the source, not only does the device turn ON, but undesirable error current will flow between the gate and the source.

In a JFET driver circuit, the objective in turning the FET ON then becomes driving the gate so that $V_{GS} = 0$. The direct-coupled drive circuit shown in Figure 8 satisfies this JFET operating objective. If the npn transistor is OFF, then

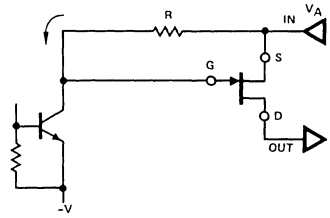


Figure 8. Direct-coupled JFET switch clamps the gate to the source through resistor r if the npn driver transistor is OFF.

a resistor clamps the gate to the source. A trade-off arising from this condition is that collector leakage in the driver transistor may draw current from the analog signal path.

A more serious problem common to direct-coupled circuits occurs when the switch is turned OFF. An n-channel JFET is turned OFF by application of a negative gate voltage, so that V_{GS} is more negative than the FET cut-off voltage. In such a circuit, the FET is turned OFF by turning ON the npn driver transistor. The negative supply must be more negative than the most negative analog voltage. When the driver is OFF in the circuit, a current flows from V_A to -V, limited only by R (Figure 8). An unreasonably long turn-ON time will result if R is too large.

A JFET driver circuit commonly used with low-cost systems that employ discrete components is shown in Figure 9. The diode permits the driver to pull the JFET negative and turn it OFF. When the driver cathode becomes positive, the diode is reverse-biased and the diode capacitor inserts sufficient charge into the FET gate to bring V_{GS} slightly above zero. The FET is thus turned ON and, if $C_{GS} + C_{GD}$ is more than C_d, the gate will stay ON, pulled along with the analog voltage being supplied to the source. This diode-coupled JFET switch produces a problem when handling a-c signals. A negative signal on the source forward-biases the gate-source junction, pulling the gate negative. When the source voltage rises, the diode capacitance C_d prevents the gate from fully following the source. Increased r_{DS} and even device cut-off may occur on the positive signal peak.

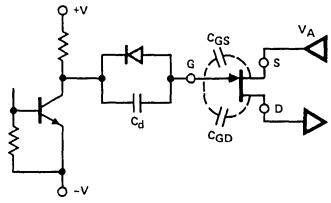


Figure 9. Diode capacitance in this low cost diode-coupled JFET switch prevents the gate from exactly following the source.

A charge-transfer driver for a JFET switch is shown in Figure 10. The circuit functions like the diode-coupled driver in Figure 9. A controlled amount of charge is inserted into the FET gate until C charges up to +V, then the transistor turns OFF. Compared to the diode-coupled driver circuit, the charge-transfer driver circuit's advantage is that its output capacitance is much lower than the 10 to 20 pF required for the diode-coupled arrangement. This charge-transfer type of driver gate is offered as an integrated circuit by several major manufacturers.

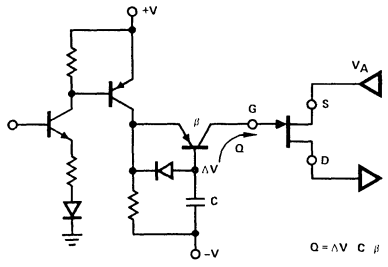


Figure 10. Charge-transfer driver has much less capacitance than the diode-coupled arrangement of Figure 9.

Earlier, it was pointed out that the best way to turn ON a JFET driver circuit is to clamp the gate to the source. An attractive way to accomplish this is suggested in Figure 11. When point A is pulled negative, the PMOS FET is turned ON, with the JFET tied to its source through a resistance of several hundred ohms. V_{GS} remains at zero, and the JFET will remain ON even at high frequencies.

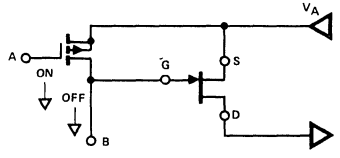


Figure 11. Using a PMOS driver for a JFET switch allows the JFET to remain ON even at high frequencies.

In Figure 12, an NMOS FET has been added to the circuit of Figure 11 to provide an excellent JFET driver. A negative input will turn the PMOS FET and the JFET ON. A positive input will turn the NMOS FET ON, the PMOS FET OFF, and since the JFET gate is also pulled to the negative state, that device also will turn OFF.

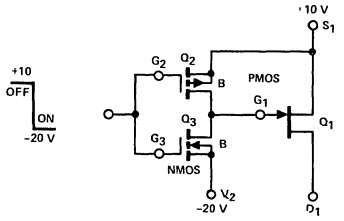


Figure 12. A negative (–20 V) input turns ON the PMOS FET and JFET. A positive (10 V) input turns ON the NMOS FET, but turns OFF the PMOS FET and the PFET (G_1 clamped to –20 V).

The circuit shown in Figure 13 also uses a PMOS FET to drive a JFET. The gate pull-down (turn-off) element is a pnp transistor. The entire drive circuit can be constructed on one monolithic chip.

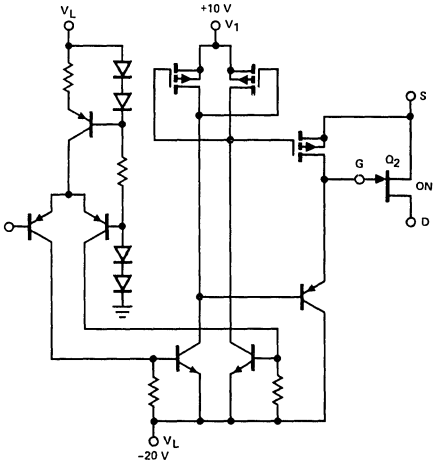


Figure 13. Monolithic JFET switch with both a push-pull driver and a level shifter.

Appendix I

Analysis of error accumulated across sampling capacitor, using JFET as analogue switch is low level sample-and-hold applications

The error developed across the sampling capacitor during the ON-to-OFF switch transition can be found by considering FET operation in 2 phases. The first phase covers switch operation between fully ON and fully OFF states, i.e. for $V_{gs} = 0$ to $V_{gs} = V_p$. The second phase covers switch operation above pinch-off.

A.4.1 **Switch operation between $V_{GS} = 0$ volts and $V_{GS} = V_p$.**

Fig. A.4.1 shows the application of a negative going ramp voltage applied to the gate of the n-channel Junction FET. For analogue voltages around zero volts, (e.g. tens of millivolts), the gate voltage for the ON state of the FET can be made zero volts and for the OFF state > Vp volts. The minimum ramp voltage excursion required at the gate will therefore be from 0 volts to Vp volts. The change in voltage at the gate will generate an error voltage across the sampling capacitor which will add to the true value of the stored analogue voltage.

Fig. A.4.1 **Negative going ramp to turn FET from ON to OFF. OFF state of switch is achieved when V_{gate} reaches a negative value equal to $-V_p$.**

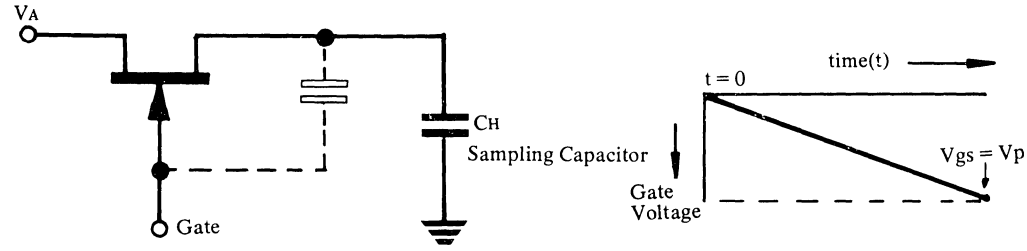
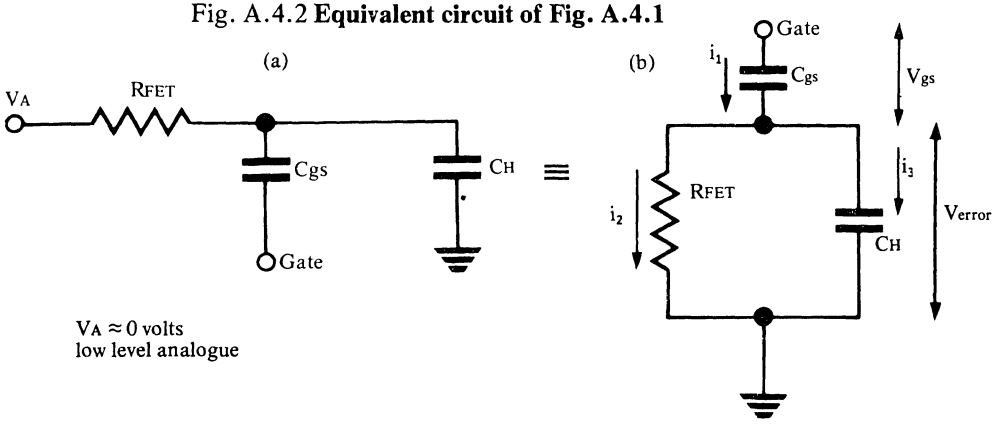


Fig. A.4.2 **Equivalent circuit of Fig. A.4.1**



VA ≈ 0 volts
low level analogue

R_{FET} = drain-to-source resistance of FET. This varies very nearly according to relationship :

$$R_{FET} = \frac{r_{DS(on)}}{1 - \frac{V_{GS}}{V_p}}$$

Reference to Fig. A.4.2b

Circuit equations are :

$$i_1 = C_{gs} \cdot \frac{dV_{GS}}{dt},\ i_2 = \frac{V_{error}}{R_{FET}}$$

$$i_3 = C_H \cdot \frac{dV_{error}}{dt},\ i_1 - i_2 = C_{gs} \cdot \frac{dV_{GS}}{dt} - \frac{V_{error}}{R_{FET}}$$

$$\frac{V_{error}}{R_{FET}} = C_{gs} \cdot \frac{dV_{GS}}{dt} - C_H \cdot \frac{dV_{error}}{dt}$$

$$\frac{V_{error}}{R_{FET}} = C_{gs} \cdot \frac{d}{dt}(V_{gate} - V_{error}) - C_H \cdot \frac{dV_{error}}{dt}$$

or $$\frac{V_{error}}{R_{FET}} = C_{gs} \cdot \frac{dV_{gate}}{dt} - (C_{gs} + C_H) \cdot \frac{dV_{error}}{dt} \qquad \text{eqn. A.4.1}$$

Substitute relationship for R_{FET} in equation A.4.1 :

$$\frac{V_{error}}{\frac{r_{DS(on)}}{1 - V_{GS}/V_p}} = C_{gs} \frac{dV_{gate}}{dt} - (C_{gs} + C_H) \cdot \frac{dV_{error}}{dt} \qquad \text{eqn. A.4.2}$$

Since V_{gate} is taken as a ramp function, the rate of change of V_{gate} with time is constant, i.e.

$$\frac{dV_{gate}}{dt} = K \text{ and } V_{GS} = V_{gate} - V_{error}$$

In any sample-and-hold application, C_H will be much greater than the device capacitance, i.e. $C_H >> C_{gs}$. In this case, therefore, V_{GS} will be practically equal to the applied gate voltage (V_{gate}), i.e. $V_{GS} = V_{gate} = Kt$

∴ equation A.4.2 becomes :

$$\frac{V_{error}}{r_{DS(on)} V_p} \cdot (V_p - Kt) = C_{gs} K - (C_{gs} + C_H) \cdot \frac{dV_{error}}{dt}$$

$$\therefore \frac{dV_{error}}{dt} + \frac{V_{error}(V_p - Kt)}{r_{DS(on)} V_p (C_{gs} + C_H)} = \frac{C_{gs} K}{C_{gs} + C_H} \qquad \text{eqn. A.4.3}$$

This equation has the standard form

$$\frac{dy}{dt} + yP = Q \qquad \text{eqn. A.4.4}$$

where P and Q can, but not necessarily, be functions of t only.
Comparing equations A.4.3 and A.4.4 :

$$P = \frac{Vp\text{-}Kt}{r_{DS(on)}\,Vp(C_{gs} + C_H)} \text{ and } Q = \frac{C_{gs}K}{C_{gs} + C_H}$$

The equation can be solved by multiplying each term by ϕ , where $\phi = \exp(\int P dt)$.

Equation A.4.4 becomes :

$$\frac{dy}{dt}\,\phi + yP = Q\phi$$

This can be rewritten as:

$$\frac{d}{dt}(\phi y) = \phi Q$$

$$\therefore \phi y = \int \phi Q dt + Z$$

$$\therefore y = \frac{\int \phi Q dt}{\phi} + \frac{Z}{\phi}$$

$$V_{error} = \frac{\int \exp(\int P dt).\, Q dt}{\exp(\int P dt)} + \frac{Z}{\exp(\int P dt)} \qquad \text{eqn. A.4.5}$$

At time t = 0, input ramp is zero and therefore V_{error} is zero. Therefore Z must be zero.
By substitution of circuit values instead of P and Q, V_{error} becomes :

$$V_{error} = \frac{\displaystyle\int_{t=a}^{t=b} \exp\left(\int \frac{(V_p\text{-}Kt)\,dt}{r_{DS(on)}\,Vp\,(C_{gs} + C_H)}\right) \frac{C_{gs}\,K}{C_{gs} + C_H} \cdot dt}{\exp\left(\int \frac{(Vp\text{-}Kt)\,dt}{r_{DS(on)}\,Vp\,(C_{gs} + C_H)}\right)}$$

Now

$$\int \frac{(V_p - Kt)\,dt}{r_{DS(on)}\,V_p\,(C_{gs} + C_H)} = \frac{t.\,Vp}{r_{DS(on)}\,Vp\,(C_{gs} + C_H)} - \frac{Kt^2}{2r_{DS(on)}\,Vp\,(C_{gs} + C_H)} + \text{Constant}$$

(=0 when integrating between limits)

$$V_{error} = \frac{C_{gs}\,K}{C_{gs} + C_H} \cdot \frac{\displaystyle\int_{t=a}^{t=b} \exp\left(\frac{t}{r_{DS(on)}\,(C_{gs} + C_H)} - \frac{Kt^2}{2r_{DS(on)}\,Vp\,(C_{gs} + C_H)}\right) \cdot dt}{\exp\left(\frac{t}{r_{DS6on)}\,(C_{gs} + C_H)} - \frac{Kt^2}{2r_{DS(on)}\,Vp\,(C_{gs} + C_H)}\right)}$$

eqn. A.4.6

The integral in the numerator of equation A.4.6 is difficult to evaluate exactly but an excellent approximation can be made by the application of Simpson's Rule.

Simpson's Rule for Integration

This states that :

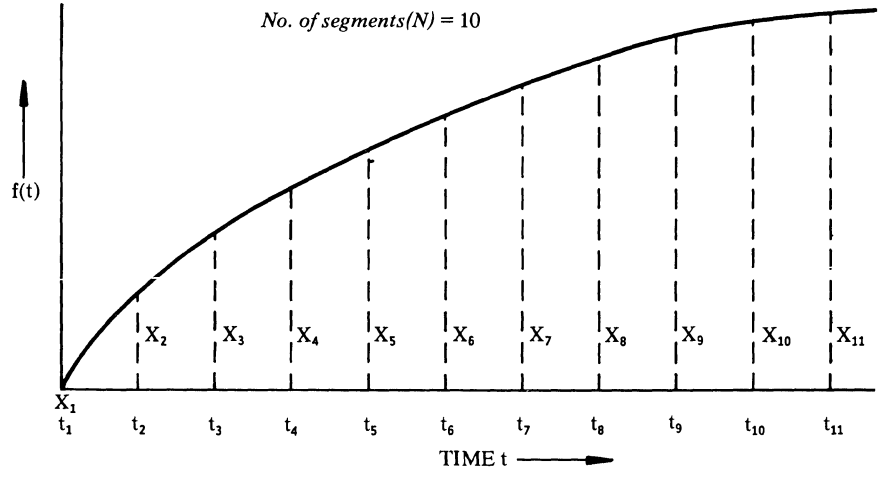
eqn. A.4.7

$$\int_{t=a}^{t=b} f(t)dt = \frac{h}{3}\left[X_1 + X_{N+1} + 4(X_2 + X_4 + ... + X_N) + 2(X_3 + X_5 + ... + X_{N-1}) \right]$$

where $h = \frac{b-a}{N}$; N = number of segments see Fig. A.4.3 below

and where X_1 ..... X_{N+1} are the ordinate values of f(t) at times t_1 .... t_{N+1} respectively.

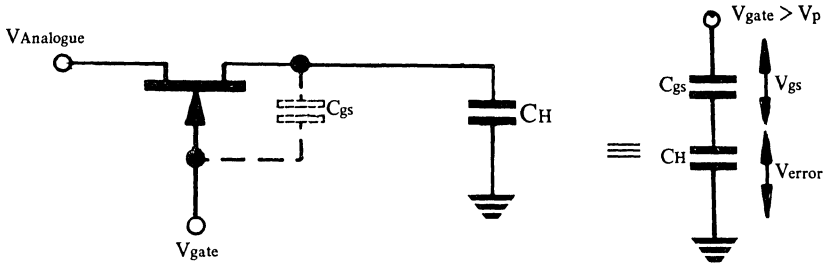
Fig. A.4.3 **Segmentation method for calculating integrals.**



A.4.2 **Switch operation if ramp goes more negative in value than the V_P of the FET.**

When the ramp continues to increase above the V_P value of the FET, an additional error voltage will be transmitted into the sampling capacitor. Calculation of this error can be easily found by considering the FET now to be an open circuit (i.e. R_{FET} is extremely large at and beyond pinch-off). The circuit at and beyond pinch-off is given in Fig. A4 below.

Fig. A.4.4 **Equivalent circuit of FET in pinched-off state.**



The circuit is now basically a capacitor potential divider system so that :

$$V_{error} = \frac{C_{gs}}{C_{gs} + C_H} (V_{gate} - V_p)$$

For an excursion at the gate which is v volts more negative than the V_p value, the error voltage transmitted will be :

$$V_{error} = \frac{C_{gs}}{C_{gs} + C_H} \cdot v \qquad \text{eqn. A.4.8}$$

INDEX

APPLICATION CIRCUITS SHOWN IN *ITALICS*

INDEX

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INDEX

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INDEX

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