FEATURES

- Drives both high-side and low-side MOSFETs in synchronous buck configuration
- Allows high switching frequencies up to 1MHz
- Transitions times & propagation delays less than 20ns
- High-side Driver - 1.65A Source / 2A Sink
- Low-side Driver - 2.0A Source / 3A Sink
- Tri-Level PWM input to disable both MOSFETs
  - within < 30ns with no hold-off time
- Adaptive Non overlap protection minimizes diode conduction time
- Input supply under voltage protection
- Available in thermally enhanced 10 pin DFN package
- Lead free RoHS compliant package, MSL level 1

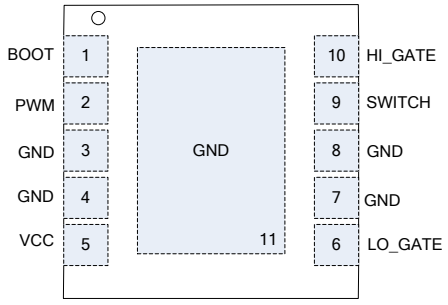

Figure 1. CHL8500 10 pin DFN Package

DESCRIPTION

The CHL8500 is a high frequency MOSFET gate driver specially designed to drive both the high-side and low-side N-channel MOSFETs in a synchronous buck power converter. This driver is designed to be used with the CHL8100 and CHL83xx Digital Controllers and MOSFETs to provide a total voltage regulator (VR) solution which meets the demands of voltage regulation for today's advanced computing applications.

The CHL8500 incorporates a unique Active Tri-level (ATL) PWM input. The CHiL ATL mode allows the controller to disable the high and low side FETS in less than 30ns without the need for a dedicated disable pin. This improves VR transient performance, especially during load release.

The CHL8500 driver can efficiently switch high and low-side MOSFETs at frequencies up to 1MHz. Each driver is capable of driving at least a 3nF load with 3A sink current. This driver features an adaptive non overlap control providing shoot through protection. This prevents cross conduction of both high-side and low-side MOSFETs and minimizes body diode conduction time to provide best in class efficiency.

APPLICATIONS

- Multiphase synchronous buck converter for desktop and server computers using Intel® VR11.x and AMD® microprocessors
- High efficiency and compact VRM
- High current DC/DC Converters

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FUNCTIONAL BLOCK DIAGRAM

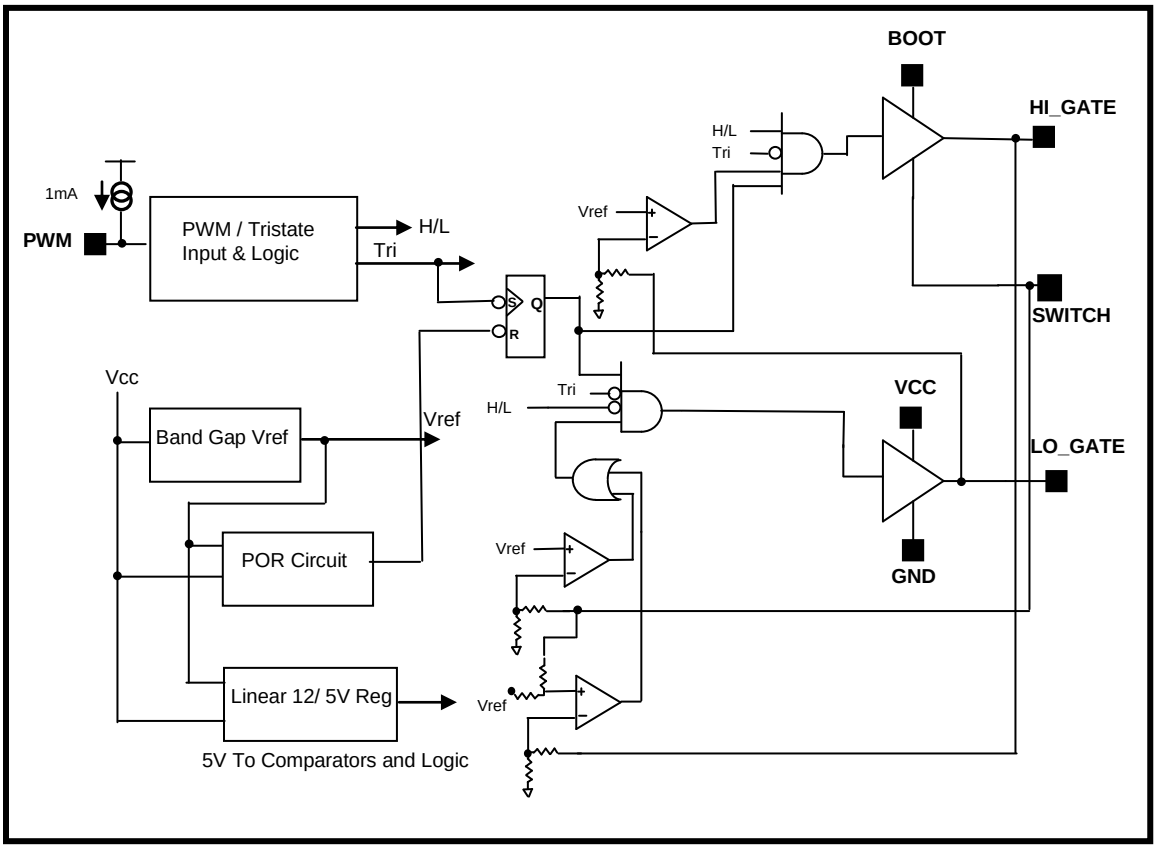

Figure 2. Simplified Block Diagram

PIN DESCRIPTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	BOOT	**Bootstrap supply.** Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and SWITCH pin to provide the charge for upper MOSFET turn on.
2	PWM	**PWM Control signal Input**. The PWM signal is the control input for the driver. It can enter three distinct states during operation. Connect this pin to the PWM output of the controller.
3,4 7,8, Pad(11)	GND	**Bias and reference ground.** All signals are referenced to this node. It is also the power ground return of the driver.
5	VCC	**Supply voltage.** Connect this pin to a +12V bias supply. Place a high quality low ESR ceramic capacitor from this pin to GND.
6	LO_GATE	**Lower gate drive output.** Connect to gate of the low-side power N-Channel MOSFET.
9	SWITCH	Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET. This pin provides a return path for the upper gate drive.
10	HI_GATE	**Upper gate drive output.** Connect to gate of high-side power N-Channel MOSFET.