HIGH EFFICIENCY VARIABLE GATE MOSFET DRIVER

FEATURES

- Ideal for Server Memory applications using +5V
- Separate HVCC and LVCC capable of drive voltages from 4.0 to 13.2V for optimal system efficiency
- Large drivers designed to drive 3nF in ≤ **10**ns with any voltage from 5V to 12V (typ) supplied to the HVCC and LVCC pins
  - Low side driver - 2A source / 4A sink
  - High side driver – 2A source / 2A sink
  - Transitions times & Propagation delays ≤ **10**ns
- Integrated bootstrap diode
- Capable of high switching frequencies from 200kHz up to greater than 1MHz
- Compatible with CHiL's patented Active Tri-Level (ATL) PWM for fastest response to transient overshoot
- Non-overlap and under voltage protection
- Thermally enhanced 10 pin DFN package
- Lead free RoHS compliant package
- Low Quiescent power to optimize efficiency

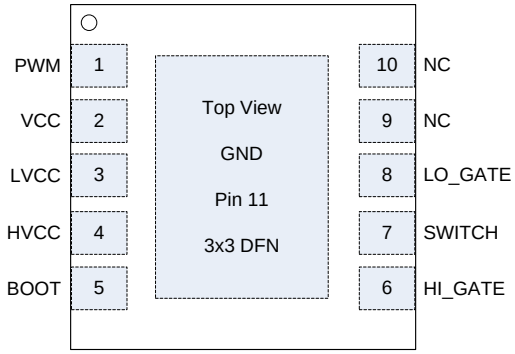


Figure 1. CHL8550 10 pin DFN Package

DESCRIPTION

The CHL8550 MOSFET is a high efficiency gate driver which can switch both high-side and low-side N-channel external MOSFETs in a synchronous buck converter. It is intended for use with CHiL Digital PWM controllers to provide a total voltage regulator (VR) solution for today's advanced computing applications.

The CHL8550 driver is capable of rapidly switching large MOSFETs with low R_{dson} and large input capacitance used in high efficiency designs. It is unquiely designed to operate from a 5V source, minimizing low load current, yet can operate from separate HVCC and LVCC drive voltages from 4.0V to 13.2V to optimize efficiency of the power train as well as to operate from a 5V standby source in sleep modes. Operating the CHL8550 in conjuction with CHiL's Variable Gate Drive controller feature.

The CHL8550 has a unique circuit which maintains drive strength to the external MOSFETs regardless of the drive voltage, insuring fast switching even at 5V as the drive voltage. The integrated boot diode reduces external component count. The CHL8550 also features an adaptive non-overlap control for shoot-through protection.

The CHL8550 is configured to drive both the high and low side switches from the patented CHiL fast Active Tri-Level (ATL) PWM signal, which will optimize the turn off time of individual phases, optimizing transient performance.

APPLICATIONS

- Multiphase synchronous buck converter for Server CPUs and DDR Memory VR solutions
- High efficiency and compact VRM
- Optimized for Sleep state S3 systems using +5VSB
- Notebook Computer and Graphics VR solutions

One Highwood Drive, Tewksbury, MA 01876
Tel: +1(978)-640-0011
www.chilsemi.com

ORDERING INFORMATION

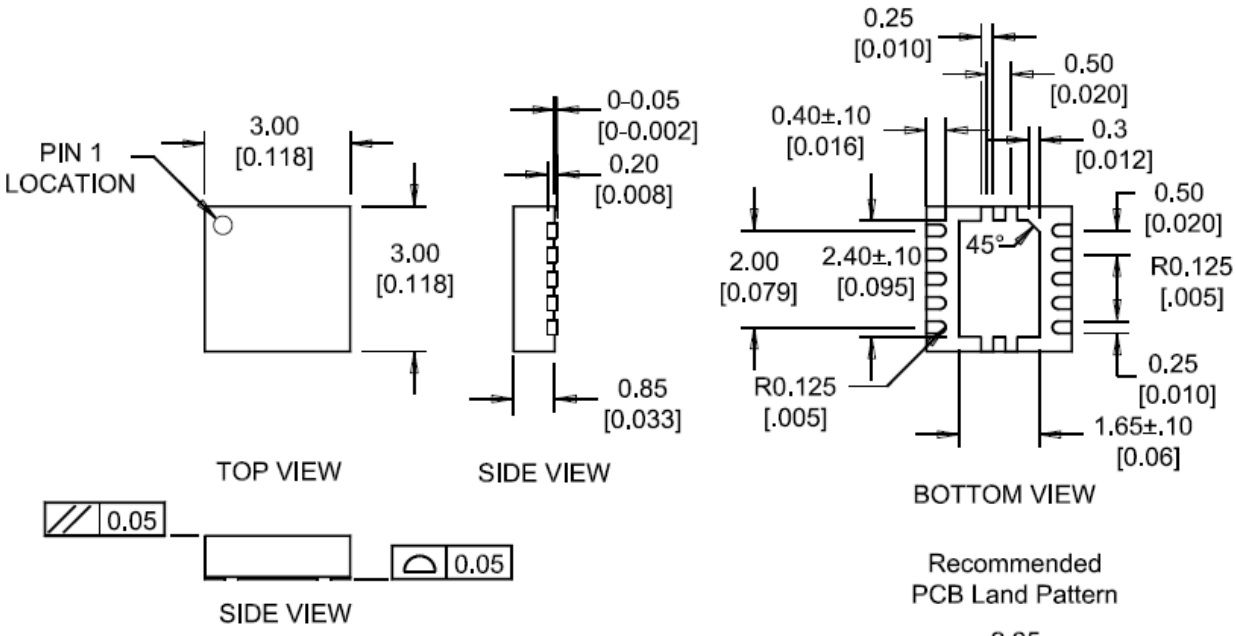
CHL8550 □ □ □

- T: Tape & Reel
- Package type
  R : DFN
- Operating Temperature
  C: Commercial Standard

Package	Tape & Reel Qty	Part Number
DFN	3000	CHL8550CRT

PACKAGE INFORMATION & LAND PATTERN

DFN 3x3mm, 10 pin



UNLESS OTHERWISE SPECIFIED
TOLERANCE ON DIMENSIONS:
.XX ±0.05
.XXX ±0.030
ALL DIMENSIONS ARE IN mm [INCH]

Recommended
PCB Land Pattern