intersil™

Dual 4-Phase + 1-Phase PWM Controller for VR12/IMVP7 Applications

ISL6364

The ISL6364 is a dual PWM controller; its 4-phase PWMs control the microprocessor core or the memory voltage regulator, while its single-phase PWM controls the peripheral voltage regulator for graphics, system agent, or processor I/O.

The ISL6364 utilizes Intersil's proprietary Enhanced Active Pulse Positioning (EAPP) modulation scheme to achieve the extremely fast transient response with fewer output capacitors.

The ISL6364 is designed to be compliant to Intel VR12/IMVP7 specifications. It accurately monitors the load current via the IMON pin and reports this information via the IOUT register to the microprocessor, which sends a PSI# signal to the controller at low power mode via SVID bus. The controller enters 1- or 2-phase operation in low power mode (PSI1); in the ultra low power mode (PSI2,3), it can further drop the number of phases and then enable the diode emulation of the operational phase. In low power modes, the magnetic core and switching losses are significantly reduced, yielding high efficiency at light load. After the PSI# signal is de-asserted, the dropped phase(s) are added back to sustain heavy load transient response and efficiency.

Today's microprocessors require a tightly regulated output voltage position versus load current (droop). The ISL6364 senses the output current continuously by measuring the voltage across the dedicated current sense resistor or the DCR of the output inductor. The sensed current flows out of the FB pin to develop the precision voltage drop across the feedback resistor for droop control. Current sensing circuits also provide the needed signals for channel-current balancing, average overcurrent protection and individual phase current limiting. The TM and TMS pins are to sense an NTC thermistor's temperature, which is internally digitized for thermal monitoring and for integrated thermal compensation of the current sense elements of the respective regulator.

The ISL6364 features remote voltage sensing and completely eliminates any potential difference between remote and local grounds. This improves regulation and protection accuracy. The threshold-sensitive enable input is available to accurately coordinate the start-up of the ISL6364 with other voltage rails.

Features

- Intel VR12/IMVP7 Compliant
  - SerialVID with Programmable IMAX, TMAX, BOOT, ADDRESS OFFSET Registers

- Intersil's Proprietary Enhanced Active Pulse Positioning (EAPP) Modulation Scheme, Patented
  - Voltage Feed-forward and Ramp Adjustable Options
  - High Frequency and PSI Compensation Options
  - Variable Frequency Control During Load Transients to Reduce Beat Frequency Oscillation
  - Linear Control with Evenly Distributed PWM Pulses for Better Phase Current Balance During Load Transients

- Dual Outputs
  - Output 1 (VR0): 1 to 4-Phase, Coupled Inductor Compatibility, for Core or Memory
  - Output 2 (VR1): Single Phase for Graphics, System Agent, or Processor I/O
  - Differential Remote Voltage Sensing
  - ±0.5% Closed-loop System Accuracy Over Load, Line and Temperature
  - Phase Doubler Compatibility (NOT Phase Dropping)

- Proprietary Active Phase Adding and Dropping with Diode Emulation Scheme For Enhanced Light Load Efficiency

- Programmable Slew Rate of Fast Dynamic VID for VR0

- Dynamic VID Compensation (DVS) for VR1 at No Droop

- Droop and Diode Emulation Options

- Programmable 1 or 2-Phase Operation in PSI1/2/3 Mode

- Programmable Standard or Coupled-Inductor Operation

- Precision Resistor or DCR Differential Current Sensing
  - Integrated Programmable Current Sense Resistors
  - Integrated Thermal Compensation
  - Accurate Load-Line (Droop) Programming
  - Accurate Channel-Current Balancing
  - Accurate Current Monitoring

- Average Overcurrent Protection and Channel Current Limit With Internal Current Comparators

- Precision Overcurrent Protection on IMON & IMONS Pins

- Independent Oscillators, up to 1MHz Per Phase, for Cost, Efficiency, and Performance Optimization

- Dual Thermal Monitoring and Thermal Compensation

- Start-up Into Pre-Charged Load

- Pb-Free (RoHS Compliant)

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6364CRZ	ISL6364 CRZ	0 to +70	48 Ld 6x6 QFN	L48.6x6B
ISL6364IRZ	ISL6364 IRZ	-40 to +85	48 Ld 6x6 QFN	L48.6x6B

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6364. For more information on MSL please see techbrief TB363.

Pin Configuration

ISL6364
(48 LD 6X6 QFN)
TOP VIEW
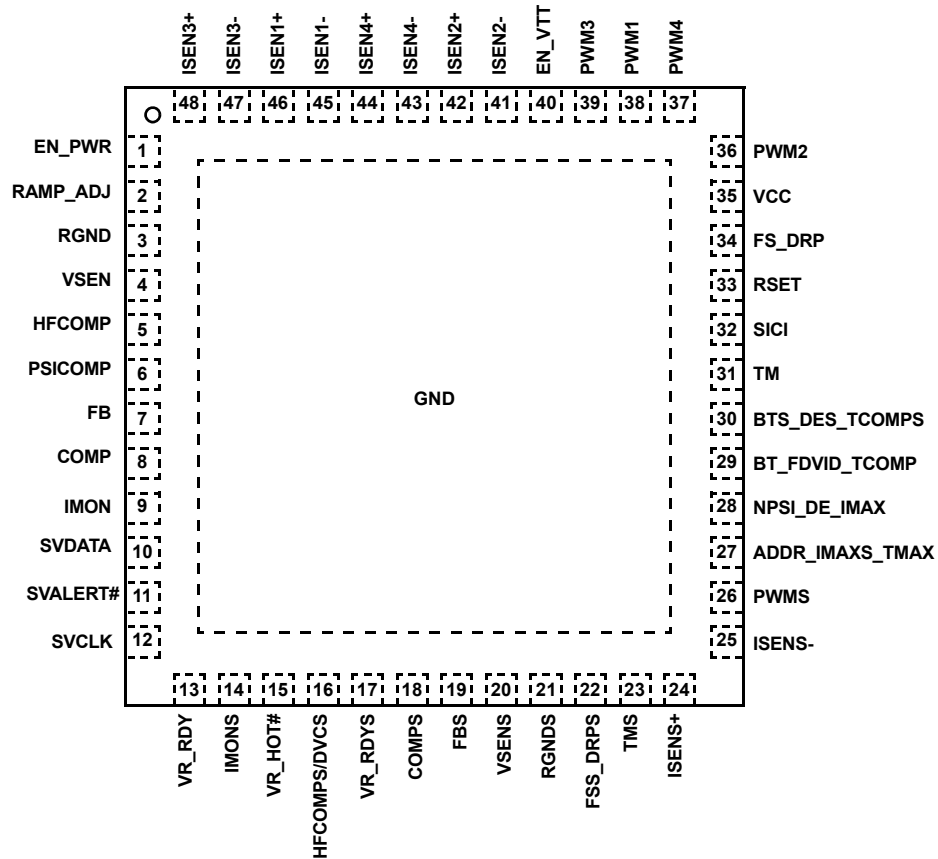
Controller and Driver Recommendation

DRIVER	QUIESCENT CURRENT (mA)	GATE DRIVE VOLTAGE	# OF DRIVERS	DIODE EMULATION (DE)	GATE DRIVE DROP (GVOT)	COMMENTS
ISL6627	1.0	5V	Single	Yes	No	For PSI# channel and its coupled channel in coupled inductor applications or all channels
ISL6620 ISL6620A	1.2	5V	Single	Yes	No	For PSI# channel and its coupled channel in coupled inductor applications or all channels. Shorter body diode conduction time when enters PSI2 mode at a fixed voltage.
ISL6596	0.19	5V	Single	No	No	For dropped phases or all channels without DE
ISL6610 ISL6610A	0.24	5V	Dual	No	No	For dropped phases or all channels without DE
ISL6611A	1.25	5V	Dual	No	No	Phase Doubler with Integrated Drivers, up to 12-Phase. For all channels with DE Disabled
ISL6617	5.0	N/A	N/A	No	No	PWM Doubler for DrMOS, up to 12 or 24-Phase. For all channels with DE Disabled
ISL6625	1.2	12V	Single	Yes	Yes	For PSI# channel and its coupled channel in coupled inductor applications or all channels
ISL6622	5.5	12V	Single	Yes	Yes	For PSI# channel and its coupled channel in coupled inductor applications or all channels. Shorter body diode conduction time when enters PSI2 mode at a fixed voltage.
ISL6622A ISL6622B	5.5	12V	Single	Yes	No	For PSI# channel and its coupled channel in coupled inductor applications or all channels. Shorter body diode conduction time when enters PSI2 mode at a fixed voltage.
ISL6625A	1.0	12V	Single	No	No	For dropped phases or all channels without DE

NOTE: Intersil 5V and 12V drivers are mostly pin-to-pin compatible and allow for dual footprint layout implementation to optimize MOSFET selection and efficiency. 5V Drivers are more suitable for high frequency and high efficiency applications.

ISL6364 Internal Block Diagram
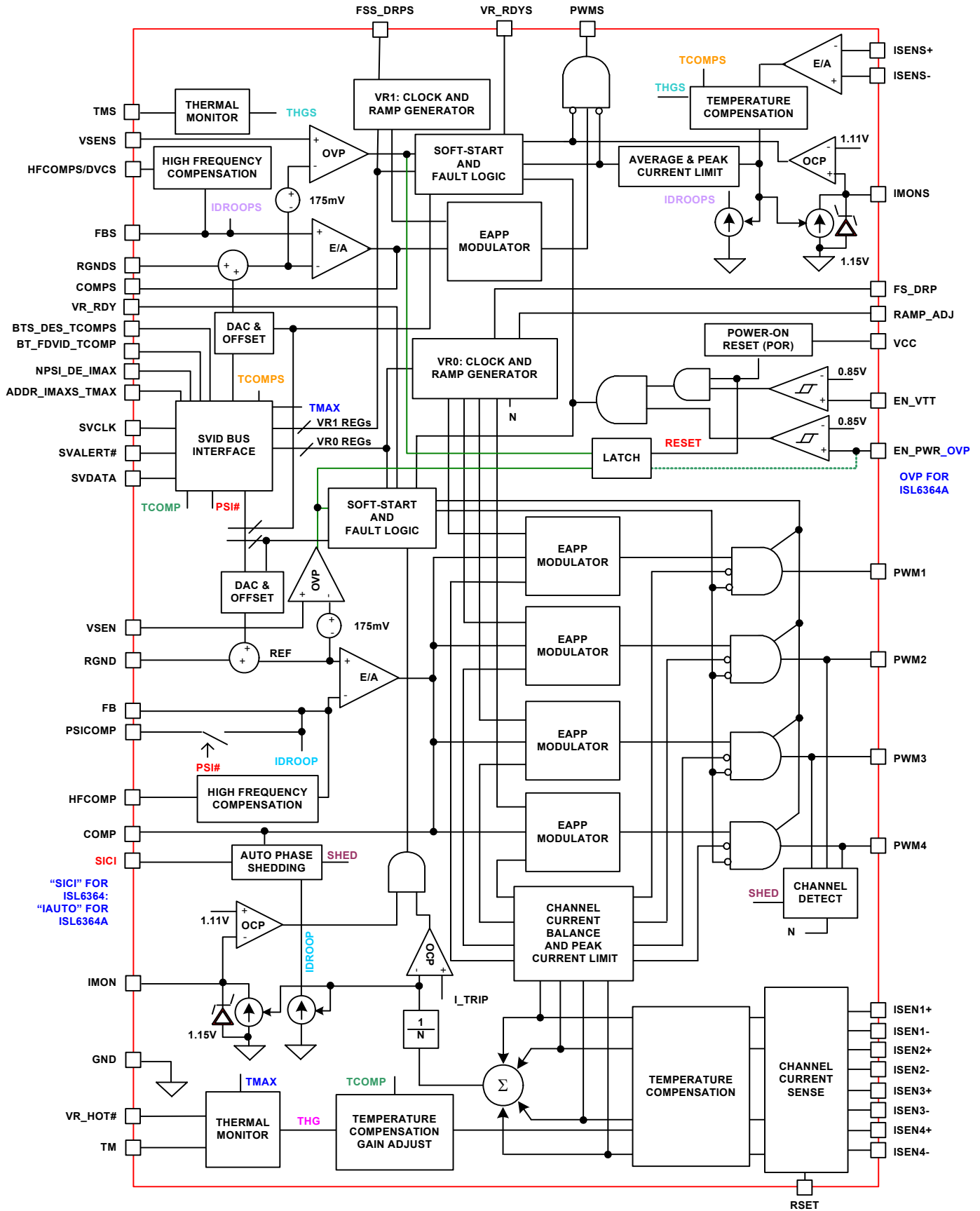
Typical Application: 4-Phase VR and 1-Phase VR WITH ISL6364

NTC: Beta = ~ 3477

Typical Application: 4-Phase Coupled-Inductor VR and 1-Phase VR
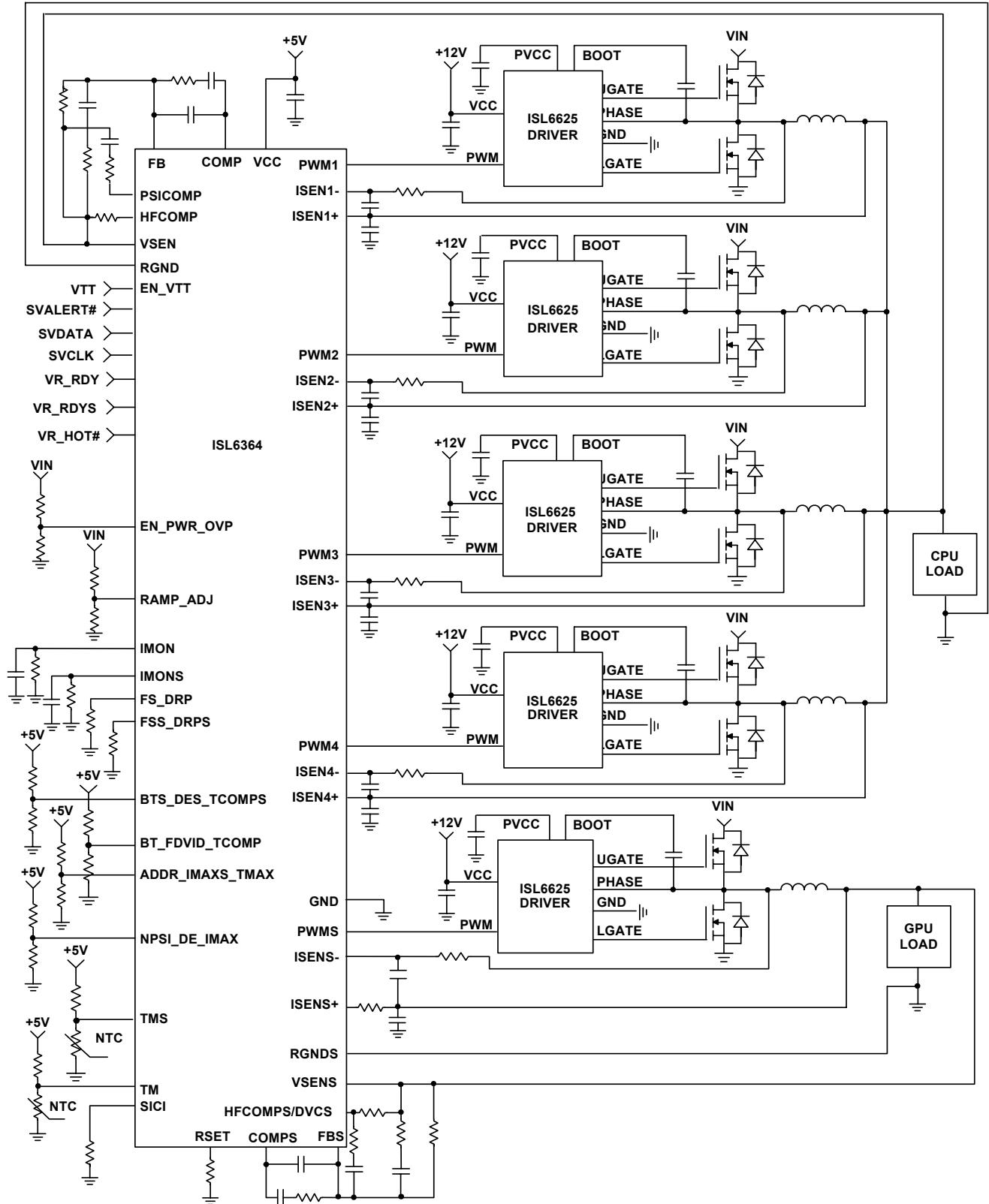
NTC: BETA = ~ 3477

Table of Contents

Absolute Maximum Ratings

VCC, VR_RDY, VR_RDYS. . . . . +6V
All Other Pins . . . . .GND -0.3V to V_{CC} + 0.3V

Recommended Operating Conditions

Supply Voltage, VCC . . . .+5V ±5%
Ambient Temperature
  ISL6364CRZ . . . . 0°C to +70°C
  ISL6364IRZ. . . . .-40°C to +85°C

Thermal Information

Thermal Resistance (Notes 4, 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
48 Ld 6x6 QFN Package	27	1.5

Maximum Junction Temperature . . . .+150°C
Maximum Storage Temperature Range . . . .-65°C to +150°C
Pb-free reflow profile . . . . see link below
  http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications
Recommended Operating Conditions, V_{CC} = 5V, Unless Other wise specified. **Boldface limits apply over the operating temperature range.**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
VOLTAGE REGULATOR (VR) ADDRESS					
Multiple-Phase Voltage Regulator (VR0) ADDRESS		**0**	EVN	**C**	
Single-Phase Voltage Regulator (VR1) ADDRESS		**1**	ODD	**7**	
VCC SUPPLY CURRENT					
Nominal Supply	VCC = 5VDC; EN_PWR = 5VDC; R_T = 125kΩ, ISEN1-4 = 80µA, ISL6364, 400kHz	**21**	28	**33.5**	mA
Shutdown Supply	VCC = 5VDC; EN_PWR = 0VDC; R_T = 125kΩ	**14**	21	**27.5**	mA
POWER-ON RESET AND ENABLE					
VCC Rising POR Threshold		**4.30**	4.40	**4.50**	V
VCC Falling POR Threshold		**3.75**	3.90	**4.00**	V
EN_PWR_FT Rising Threshold		**0.830**	0.850	**0.870**	V
EN_PWR_FT Falling Threshold		**0.730**	0.750	**0.770**	V
EN_VTT Rising Threshold		**0.830**	0.850	**0.870**	V
EN_VTT Falling Threshold		**0.730**	0.750	**0.770**	V
REFERENCE VOLTAGE AND DAC					
System Accuracy of ISL6364CRZ (VID = 1V to 2.155V, T_J = 0°C to +70°C)	(Note 6, Closed-Loop)	**-0.5**	-	**0.5**	%VID
System Accuracy of ISL6364CRZ (VID = 0.8V to 1V, T_J = 0°C to +70°C)	(Note 6, Closed-Loop)	**-5**	-	**5**	mV
System Accuracy of ISL6364CRZ (VID = 0.25V to 0.8V, T_J = 0°C to +70°C)	(Note 6, Closed-Loop)	**-8**	-	**8**	mV
System Accuracy of ISL6364IRZ (VID = 1V to 2.155V, T_J = -40°C to +85°C)	(Note 6, Closed-Loop)	**-0.6**	-	**0.6**	%VID
System Accuracy of ISL6364IRZ (VID = 0.8V to 1V, T_J = -40°C to +85°C)	(Note 6, Closed-Loop)	**-6**	-	**6**	mV
System Accuracy of ISL6364IRZ (VID = 0.25V to 0.8V, T_J = -40°C to +85°C)	(Note 6, Closed-Loop)	**-9**	-	**9**	mV

Electrical Specifications Recommended Operating Conditions, V_{CC} = 5V, Unless Other wise specified. **Boldface limits apply over the operating temperature range. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
OSCILLATORS					
Accuracy of VR0 Switching Frequency Setting	R_{FS} = 125kΩ	**360**	400	**440**	kHz
Accuracy of VR1 Switching Frequency Setting	R_{FSS} = 125kΩ	**360**	400	**440**	kHz
Maximum Switching Frequency		**1.0**	-	-	MHz
Minimum Switching Frequency		-	-	**0.08**	MHz
Soft-start Ramp Rate for VR0	FDVID = 10mV/µs	**2.5**	2.8	**3.2**	mV/µs
	FDVID = 20mV/µs	**5.0**	5.55	**6.2**	mV/µs
Soft-start Ramp Rate for VR1		**2.5**	2.8	**3.2**	mV/µs
Maximum Duty Cycle Per PWM for VR0	400kHz, V_{RAMP} <1.8V	**95**	97	**99**	%
Maximum Duty Cycle for VR1	400kHz	**69**	83	**96**	%
PWM GENERATOR (Note 7)					
Sawtooth Amplitude for VR0	R_{RAMP_ADJ} = Open, all Switching Frequency	-	1	-	V
Sawtooth Amplitude for VR0	R_{RAMP_ADJ} = 2.4 MΩ to 12V, 500kHz	-	0.5	-	V
Sawtooth Amplitude for VR0	R_{RAMP_ADJ} = 1.2 MΩ to 12V, 500kHz	-	1	-	V
Maximum Adjustable Ramp for VR0	Applicable to VR0 Only	-	3	-	V
Minimum Adjustable Ramp for VR0	Applicable to VR0 Only	-	0.3	-	V
Sawtooth Amplitude for VR1	Applicable to VR1 Only		2.0		V
ERROR AMPLIFIER					
Open-Loop Gain	R_L = 10kΩ to ground	-	96	-	dB
Open-Loop Bandwidth		-	80	-	MHz
Slew Rate		-	25	-	V/µs
Maximum Output Voltage	No Load	**4.1**	4.4	**4.6**	V
Output High Voltage @ 2mA	2mA Load	**3.8**	4.1	**4.6**	V
Output Low Voltage @ 2mA	2mA Load	**0.85**	0.96	**1.2**	V
PWM OUTPUT (PWM[4:1] and PWMS)					
Sink Impedance	PWM = Low with 1mA Load	**-**	170	**-**	Ω
Source Impedance	PWM = High, Forced to 3.7V	**-**	150	**-**	Ω
PWM PSI2/3/Decay Mid-Level	0.4mA Load	**38**	40	**44**	%VCC
CURRENT SENSE AND OVERCURRENT PROTECTION					
Sensed Current Tolerance of VR0	ISEN1-4= 40µA; CS Offset and Mirror Error Included, R_{SET} = 12.8kΩ	**36.5**	40.7	**44**	µA
	ISEN1-4 = 80µA; CS Offset and Mirror Error Included, R_{SET} = 12.8kΩ	**75.5**	80.7	**85.5**	µA
Sensed Current Tolerance of VR1	ISENS= 40µA; R_{ISENS} = 100Ω;	**33**	37	**41**	µA
	ISENS = 80µA; R_{ISENS}= 100Ω	**69.5**	75	**81**	µA
VR0 Average Overcurrent Trip Level at Normal CCM PWM Mode	CS Offset and Mirror Error Included, R_{SET} = 12.8kΩ	-	100	-	µA
VR0 Average Overcurrent Trip Level at PSI1/2/3 Mode	N = 4 Drop to 1-Phase	-	99	-	µA
VR0 Average Overcurrent Trip Level at PSI1 Mode	N = 4 Drop to 2-Phase	-	100	-	µA

ISL6364

Electrical Specifications Recommended Operating Conditions, V_{CC} = 5V, Unless Other wise specified. **Boldface limits apply over the operating temperature range. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
VR0 Peak Current Limit for Individual Channel		-	140	-	µA
VR1 Average Overcurrent Trip Level	CS Offset and Mirror Error Included, R_{ISENS} = 200Ω	-	100	-	µA
IMON, IMOS Clamped and OCP Trip Level		**1.085**	1.12	**1.14**	V
IMON, IMONS IMAX TRIP POINT (FF)	Higher than this will be "FF"	**875**	880	**887**	mV
THERMAL MONITORING					
VR_HOT# Pull-down Impedance		**8.4**	9.2	**13**	Ω
Thermal Trip (Programmable via TMAX)	TMAX = +100°C, see Table 7	-	39.12	-	%
VR_HOT# and Thermal Alert# Hysteresis		-	3	-	^{0}C
Leakage Current of VR_HOT#	With external pull-up resistor connected to VCC	-	-	**1**	µA
VR READY AND PROTECTION MONITORS					
Leakage Current of VR_RDY, VR_RDYS	With pull-up resistor externally connected to VCC	-	-	**1**	µA
VR READY Low Voltage	4mA Load	-	-	**0.3**	V
Overvoltage Protection Threshold	Prior to the End of Soft Start		2.3		V
	After the End of Soft Start, the voltage above VID	**160**	179	**200**	mV
Overvoltage Protection Reset Hysteresis		**98**	107	**117**	mV
SVID BUS					
ALERT# Pull-down Impedance		-	11	**13**	Ω
SVDATA		-	11	**13**	Ω
SVCLK Maximum Speed		-	26.5	-	MHz
SVCLK Minimum Speed		-	13.0	-	MHz

NOTES:

6. These parts are designed and adjusted for accuracy with all errors in the voltage loop included.

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Functional Pin Descriptions

Note: VR0 is the multi-phase voltage regulator. VR1 is the single-phase voltage regulator. Refer to Table 13 on page 35 and Table 14 on page 39 for Design and Layout Consideration.

VCC - Supplies the power necessary to operate the chip. The controller starts to operate when the voltage on this pin exceeds the rising POR threshold and shuts down when the voltage on this pin drops below the falling POR threshold. Connect this pin directly to a +5V supply with a high quality ceramic capacitor.

GND - The bottom metal base of ISL6364 is the GND. Bias and reference ground for the IC. It is also the return for all PWM output drivers.

EN_PWR - This pin is a threshold-sensitive enable input. Connecting the power train input supply to this through an appropriate resistor divider provides a means to synchronize the power sequencing of the controller and the MOSFET driver ICs. When EN_PWR is driven above 0.85V, the ISL6364 is actively depending on status of the EN_VTT, the internal POR, and pending fault states. Driving EN_PWR below 0.75V will clear all fault states and prepare the ISL6364 to soft-start when re-enabled.

EN_VTT - This pin is a threshold-sensitive enable input. It's typically connected to the output of the VTT voltage regulator in the computer mother board. When this pin is driven above 0.85V, the ISL6364 is actively depending on status of the EN_PWR, the internal POR, and pending fault states. Driving this below 0.75V will clear all fault states and prepare the ISL6364 to soft-start when re-enabled.

VSEN - This pin monitors the regulator VR0 output for over-voltage protection. Connect this pin to the positive rail remote sensing point of the microprocessor or load. This pin tracks with the FB pin. If a resistive divider is placed on the FB pin, a resistive divider with the same ratio should also be on the VSEN pin. Tie it to GND if not used.

RGND - This pin compensates the offset between the remote ground of the VR0 load and the local ground of this device. Connect this pin to the negative rail remote sensing point of the microprocessor or load. Tie it to GND if not used.

COMP and FB - COMP and FB are the output and inverting input of the precision error amplifier, respectively. A type III loop compensation network should be connected to these pins, while the FB's R-C network should connect to the positive rail remote sensing point of the microprocessor or load. Combined with RGND, the potential difference between remote and local rails is completely compensated and it improves regulation accuracy. A properly chosen resistor between FB and remote sensing point can set the load line (droop, if enabled), because the sensed current will flow out of FB pin. The droop scale factor is set by the ratio of the effective ISEN resistors (set by RSET) and the inductor DCR or the dedicated current sense resistor. COMP is tied back to FB through an external R-C network to compensate the regulator. An RC from the FB pin to ground will be needed if the output is lagging from the DAC, typically for applications with too many output capacitors and droop enabled.

VR_RDY - VR_RDY indicates that soft-start has completed and this VR0 output remains in normal operation. It is an open-drain logic output. When OCP or OVP occurs in VR0, VR_RDY will be pulled to low.

TM - TM is an input pin for the VR0 temperature measurement. Connect this pin through an NTC thermistor to GND and a resistor to VCC of the controller. The voltage at this pin is inversely proportional to the VR temperature. The device monitors the VR temperature based on the voltage at the TM pin. Combining with "TCOMP" setting, VR0's sensed current is thermally compensated. The VR_HOT# asserts low if the sensed temperature at this pin is higher than the maximum desired temperature, "TMAX". The NTC should be placed close to the current sensing element, the output inductor or dedicated sense resistor on Phase 1 of VR0. A decoupling capacitor (0.1µF) is typically needed to be in close proximity to the controller. If not used, connect this pin to TMS or $1M\Omega/2M\Omega$ resistor divider, but DON'T tie it to VCC or GND.

VR_HOT# - VR_HOT# is used as an indication of high VR temperature. It is an open-drain logic output. It will be open if the measured VR temperature is less than a certain level, and pulled low when the measured VR temperature reaches a certain level.

PWM[4:1] - Pulse width modulation outputs of VR0. Connect these pins to the PWM input pins of the Intersil driver IC. The number of active channels is determined by the state of PWM[4:2]. Tie PWM(N+1) to VCC to configure for N-phase operation. PWM firing order is sequential from 1 to N with N being the number of active phases. If PWM1 is tied high, the respective address is released for use, i.e, the VR0 is disabled and does not respond to the SVID commands. IMON, VSEN, FB, ISEN[4:1]-, and RGND must be grounded to remove OCP and OVP faults of VR0, while TM can be tied to TMS, or 1/2 ratio resistor divider. In addition, must connect FS_DRP to $1M\Omega$ from GND or VCC. See Table page 15 on and Table 13 on page 35 for details.

PWMS - Pulse width modulation output of VR1. Connect this pin to the PWM input pin of the Intersil driver IC. Tie this pin to VCC to disable this PWM channel, while the respective address is released for use, i.e., the VR1 is disabled and does not respond to the SVID commands. IMONS, VSENS, FBS, ISENS-, and RGNDS must be grounded to remove OCP and OVP faults of VR1, while TMS can be tied to TM, or 1/2 ratio resistor divider. In addition, must connect FSS_DRPS to $1M\Omega$ from GND or VCC for proper SVID address. See Table 13 for details.

ISEN[4:1]+, ISEN[4:1]- - The ISEN+ and ISEN- pins are current sense inputs to individual differential amplifiers of VR0. The sensed current is used for channel current balancing, overcurrent protection, and droop regulation. Inactive channels should have their respective current sense inputs, ISEN[4:#]- grounded, and ISEN[4:#]+ open. For example, ground ISEN[4:3]- and open ISEN[4:3]+ for 2-phase operation. DON'T ground ISEN[4:1]+. For DCR sensing, connect each ISEN- pin to the node between the RC sense elements. Tie the ISEN+ pin to the other end of the sense capacitor (typically output rail). The voltage across the sense capacitor is proportional to the inductor current. Therefore, the sensed current is proportional to the inductor current and scaled by the DCR of the inductor and R_{SET}. When VR0 is disabled, have ISEN[4:1]- grounded and ISEN[4:1]+ open.

RSET - A resistor connected from this pin to ground sets the current gain of the current sensing amplifier for VR0. The RSET resistor value can be from $3.84k\Omega$ to $115.2k\Omega$ and is 64x of the required R_{ISEN} resistor value. Therefore, the current sense gain

resistor value can be effectively set at 60Ω to 1.8kΩ. When VR0 is disabled (PWM1 = VCC), connect 1MΩ from this pin to GND.

ISENS+, ISENS- - The ISENS+ and ISENS- pins are current sense inputs to the differential amplifier of VR1. The sensed current is used for overcurrent protection and droop regulation. For DCR sensing, connect each ISENS- pin to the node between the RC sense elements. Tie the ISENS+ pin to the other end of the sense capacitor through a resistor, R_{ISENS}. The voltage across the sense capacitor is proportional to the inductor current. Therefore, the sense current is proportional to the inductor current and scaled by the DCR of the inductor and R_{ISENS}. When VR1 is disabled, have ISENS- grounded and ISENS+ open.

IMON - IMON is the output pin of sensed, thermally compensated (if internal thermal compensation is used) average current of VR0. The voltage at the IMON pin is proportional to the load current and the resistor value, and internally clamped to 1.12V. If the clamped voltage is triggered, it will initiate an overcurrent shutdown. By choosing the proper value for the resistor at IMON pin, the overcurrent trip level can be set to be lower than the fixed internal overcurrent threshold. During the dynamic VID, the OCP function of this pin is disabled to avoid false triggering. Tie it to GND if not used. Does not need to refer to the remote ground for VR12/IMPV7 applications.

FS_DRP - A resistor placed from this pin to GND/VCC will set the switching frequency of VR0. The relationship between the value of the resistor and the switching frequency will be approximated by Equation 4 on page 16. This pin is also used to set the droop option. The droop is disabled when the resistor is pulled to VCC and enabled when the resistor is pulled to ground. When VR0 is disabled (PWM1 = VCC), connect 1MΩ from this pin to GND.

HFCOMP - Connect a resistor with a similar value of the feedback impedance to the VR0 output to compensate the level-shifted output voltage during high-frequency load transient events. Connecting more than 2x of feedback impedance to this pin or keeping it open virtually disables this feature.

PSICOMP - Connect an RC to the type III compensation capacitor of the VR0 output voltage. This improves loop gain and load transient response in PSI1/2/3/Decay mode. An open pin will disable this feature.

SICI - When this pin is pulled to ground, it sets for standard-inductor (SI) operation; when this pin is pulled to VCC, it sets coupled-inductor (CI) operation. The phase dropping operation options for PSI1/2/3 mode are summarized in Table 3 on page 16. The ISL6364A will re-name this pin as "IAUTO" for auto phase shedding operation, while the standard and coupled-inductor programmable option is still valid on this pin.

VSENS, RGNDS, FBS, COMPS, VR_RDYS, IMONS, FSS_DRPS, HFCOMPS - These pins are for VR1 regulator and have the same function as VSEN, RGND, FB, COMP, VR_RDY, IMON, FS_DRP, and HFCOMP, respectively. However, HFCOMPS has multiplexed the DVCS function, while the FSS_DRPS does have additional programming feature as described in the following.

HFCOMPS/DVCS - Connect a resistor with a similar value of the feedback impedance to the VR1 output to compensate the level-shifted output voltage during high-frequency load transient events. Connecting more than 2x of feedback impedance to this pin or keeping it open virtually disables this feature. If the droop option of VR1 is disabled, then this pin becomes DVCS. A series resistor and capacitor can be connected from this pin to the FBS pin to compensate and smooth dynamic VID transitions for VR1 output.

FSS_DRPS - A resistor placed from this pin to ground/VCC will set the switching frequency of VR1. The relationship between the value of the resistor and the switching frequency will be approximated by Equation 4 on page 16. This pin is also used to set the droop option. The droop is disabled when the resistor is pulled to VCC and enabled when the resistor is pulled to ground. When VR1 is disabled (PWMS = VCC), connect 1MΩ from this pin to GND for ADDR: 0, 2, 4, and 6; to VCC for ADDR: 8, A, and C.

TMS - This is an input pin for the temperature monitoring. Connect this pin through an NTC thermistor to GND and a resistor to VCC of the controller. The voltage at this pin is inversely proportional to the VR temperature. The thermal information can be used for VR1 thermal compensation. If TCOMPS is set at "OFF" bit, the integrated thermal compensation is disabled; otherwise, the thermal information is used for VR1 thermal compensation with "TCOMPS" data. Combined with TM pin, the thermal information at TMS pin will also be used to trigger VR_HOT#. The NTC should be placed close to the current sensing element, the output inductor or dedicated sense resistor of VR1. A decoupling capacitor (0.1µF) is typically needed to be in close proximity to the controller. If not used, connect this pin to TM or 1MΩ/2MΩ resistor divider, but DON'T tie it to VCC or GND.

SVCLK - An input pin for a synchronous clock signal of SerialVID bus from CPU.

SVDATA - An input pin for transferring open-drain data signals between CPU and VR controller.

SVALERT# - An output pin for transferring the active low signal driven asynchronously from the VR controller to CPU.

RAMP_ADJ - An input pin to set the slope of Sawtooth for VR0. The slope of the Sawtooth is proportional to the current, sampled by the an active pull-down device, into this pin. When the resistor is connected to the input voltage of the VR0, the slope will be proportional to the input voltage, achieving voltage feed-forward compensation. For a 12V supply (V_{IN}) and 2.4MΩ pull-up (~ 5µA), it sets a nominal 0.25V/µs up-ramp slope at 500kHz switching frequency, corresponding to 0.5V peak-to-peak up ramp. The maximum peak-to-peak up ramp should be limited to 3V, corresponding a pull-down current of 30µA at 500kHz, i.e., the pull-up impedance should be higher than V_{IN}/30µA at 500kHz. See Equation 3 on page 15 for the up ramp amplitude calculation. When this pin is floating, the up ramp amplitude sets to 1V regardless of the switching frequency and the feedforward function is disabled.

ADDR_IMAXS_TMAX, BTS_DES_TCOMPS, BT_FDVID_TCOMP, NSPI_DE_IMAX - These are four register pins to program system parameters. The meaning of each is described in the following. See Table 9 on page 33 for the summary.

ADDR_IMAXS_TMAX (0C):

ADDR - An input pin to set the address offset register of VR0 (0, 2, 4, 6, 8, A, C) and VR1 (1, 3, 5, 7). E/F is an ALL call address and is not used.

IMAXS - An input pin to set the maximum current, I_{CCMAX}, register of the VR1. It can be programed to 20A, 25A, 30A, and 35A when the droop is enabled (R_{FSS_DRPS} = GND). This register represents the maximum allowed load current for VR1 and corresponds to a 900mV (typically set) at IMONS. When VR1 droop is disabled (R_{FSS_DRPS} = VCC), the I_{CCMAX} can be programed to15A, 20A, 25A, and 30A.

TMAX - An input pin to set the maximum temperature register (TMAX) of the VR0 and VR1 and the thermal trip point of VR_HOT#. It covers +90°C to +120°C with 5°C/step. The register represents the maximum allowed temperature of VR0 and VR1, and programs the over-temperature trip point at VR_HOT#. The typical application should use +100°C or lower since the NTC thermistor temperature represents the PCB, not the hottest component on the board. In addition, the NTC thermistor typically picks up a temperature lower than the PCB due to the thermal impedance between PCB and NTC.

BTS_DES_TCOMPS (0D):

BTS - An input pin to set the start-up boot voltage register of VR1. It has four levels: 0, 0.9V, 1.0, and 1.1V for graphic rails with droop enabled (R_{FSS_DRPS} = GND). When the droop is disabled (R_{FSS_DRPS} = VCC), the boot levels will be changed to 0, 0.85V, 0.925V, 1.05V for VCCIO and System Agent rails.

DES - An input pin to set the diode emulation (DE) operation register of VR1 at PSI2, PSI3, and Decay modes. At PSI1 mode, the VR1 always operates in CCM mode. When the diode emulation is disabled, the output will decay at the rate of setVID Slow; however, the SVID bus is still be acknowledged of execution of the command.

TCOMPS - An input pin to set the mis-matching temperature (+13°C to +43°C) between the actual sensed inductor and the NTC thermistor at TMS pin. The voltage sensed on the TMS pin is utilized as the temperature input to adjust the droop current and the overcurrent protection limit to effectively compensate for the temperature coefficient of the current sense element of VR1. To implement the integrated temperature compensation, select a proper temperature offset "TCOMP," other than the "OFF" value, which is to disable the integrated temperature compensation function.

BT_FDVID_TCOMP (0E):

BT - An input pin to set the start-up boot voltage register of VR0. It has four levels: 0V, 0.9V, 1.0V, and 1.1V for core applications with droop enabled (R_{FS_DRP} = GND). When the droop is disabled (R_{FS_DRP} = VCC), the boot levels will be changed to 0V, 1.2V, 1.35V, and 1.5V for memory applications.

FDVID - An input pin to set the slew rate of fast Dynamic VID. It has choices of 10mV/µs and 20mV/µs. This will only apply to VR0, not VR1.

TCOMP - An input to set the mis-matching temperature (+13°C to +43°C) between the actual sensed inductor of VR0 regulator and the NTC thermistor at the TM pin. The voltage sensed on the TM pin is utilized as the temperature input to adjust the droop current and the overcurrent protection limit to effectively compensate for the temperature coefficient of the current sense element of VR0. To implement the integrated temperature compensation, select a proper temperature offset "TCOMP," other than the "OFF" value,

which is to disable the integrated temperature compensation function.

NSPI_DE_IMAX (0F):

NPSI - An input pin to set the number of phases dropping at low power mode. See Table 3 on page 16 for more details.

DE - An input pin to set the diode emulation (DE) operation register of VR0 at PSI2, PSI3, and Decay modes. At PSI1 mode, the VR0 always operates in CCM mode. When the diode emulation is disabled, the output will decay at the rate of setVID Slow; however, the SVID bus is still be acknowledged of execution of the command.

IMAX - An input pin to set the maximum current, I_{CCMAX}, register of the VR0 voltage regulator. It has a range of 15A to 165A with 5A/step.This register represents the maximum allowed load current for VR0 and corresponds to a 900mV (typically set) at IMON.

Operation

The ISL6364 is a dual PWM controller; its 4-phase PWMs control microprocessor core or memory voltage regulator, while its single-phase PWM controls the peripheral voltage regulator such graphics rail, system agent, or processor I/O. The ISL6364 is designed to be compliant to Intel VR12/IMVP7 specifications with SerialVID Features. The system parameters and SVID required registers are programmable with four dedicated pins. It greatly simplifies the system design for various platforms and lowers inventory complexity and cost by using a single device.

In addition, this controller is compatible, except for forced phase dropping via PWM lines, with phase doublers (ISL6611A and ISL6617), which can double or quadruple the phase count. For instance, the multi-phase PWM can realize a beyond 4-phase and up to 16-phase count system, and the single-phase PWM can be scaled up to 2 or 4 phases. The higher phase count system can improve thermal distribution and power conversion efficiency at heavy load.

Multiphase Power Conversion

Microprocessor load current profiles have changed to the point that the advantages of multiphase power conversion are impossible to ignore. The technical challenges associated with producing a single-phase converter (which are both cost-effective and thermally viable), have forced a change to the cost-saving approach of multiphase. The ISL6364 controller helps reduce the complexity of implementation by integrating vital functions and requiring minimal output components. The typical application circuits diagrams on page 5 and page 6 provide the top level views of multiphase power conversion using the ISL6364 controller.

Interleaving

The switching of each channel in a multiphase converter is timed to be symmetrically out-of-phase with each of the other channels. In a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the 3-phase converter has a combined ripple frequency three times greater than the ripple frequency of any one phase,

as illustrated in Figure 1. The three channel currents (IL1, IL2, and IL3) combine to form the AC ripple current and the DC load current. The ripple component has three times the ripple frequency of each individual channel current. Each PWM pulse is terminated 1/3 of a cycle after the PWM pulse of the previous phase. The DC components of the inductor currents combine to feed the load.

To understand the reduction of ripple current amplitude in the multiphase circuit, examine Equation 1, which represents an individual channel's peak-to-peak inductor current.

$$I_{PP} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{L \cdot F_{SW} \cdot V_{IN}} \tag{EQ. 1}$$

In Equation 1, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and F_{SW} is the switching frequency.
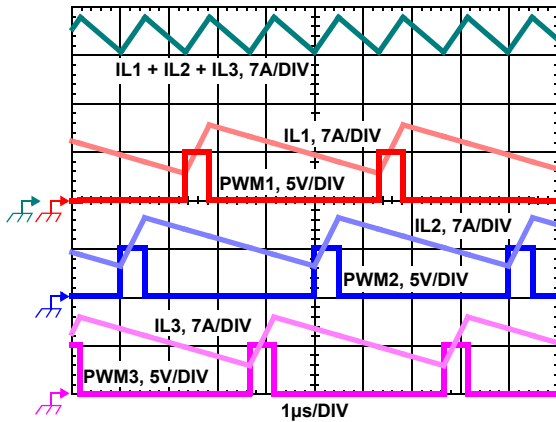

FIGURE 1. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

In the case of multiphase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 2, the peak-to-peak overall ripple current ($I_{C,PP}$) decreases with the increase in the number of channels, as shown in Figure 2.
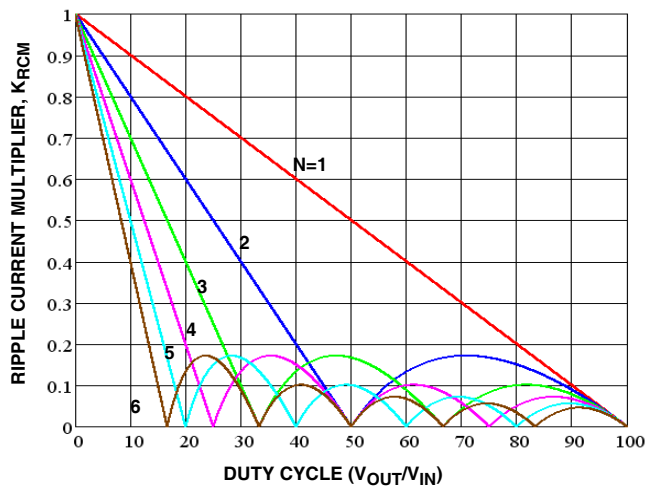

FIGURE 2. RIPPLE CURRENT MULTIPLIER vs DUTY CYCLE

Output voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and the summed inductor ripple current. Increased ripple frequency and lower ripple amplitude mean that the designer can use less per-channel inductance and few or less costly output capacitors for any performance specification.

$$I_{C, PP} = \frac{V_{OUT}}{L \cdot F_{SW}} K_{RCM} \tag{EQ. 2}$$

$$K_{RCM} = \frac{(N \cdot D - m + 1) \cdot (m - (N \cdot D))}{N \cdot D}$$

$$\text{for} \qquad m - 1 \le N \cdot D \le m$$

$$m = ROUNDUP(N \cdot D, 0)$$

Another benefit of interleaving is to reduce input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multiphase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitors. The example in Figure 3 illustrates input currents from a three-phase converter combining to reduce the total input ripple current.
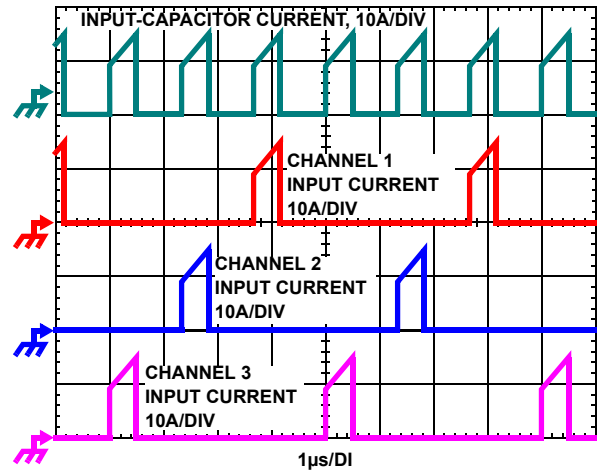
FIGURE 3. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

The converter depicted in Figure 3 delivers 36A to a 1.5V load from a 12V input. The RMS input capacitor current is 5.9A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase converter has 11.9A$_{RMS}$ input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent three-phase converter.

Figures 29, 30 and 31, as described in "Input Capacitor Selection" on page 38 , can be used to determine the input capacitor RMS current based on load current, duty cycle, and the number of channels. They are provided as aids in determining the optimal input capacitor solution. Figure 32 shows the single phase input-capacitor RMS current for comparison.

PWM Modulation Scheme

The ISL6364 adopts Intersil's proprietary Enhanced Active Pulse Positioning (EAPP) modulation scheme to improve transient performance. The EAPP is a unique dual-edge PWM modulation scheme with both PWM leading and trailing edges being

independently moved to give the best response to transient loads. The EAPP has an inherited function, similar to Intersil's proprietary Adaptive Phase Alignment (APA) technique, which turns on all phases together in order to further improve the transient response when there are sufficiently large load step currents. The EAPP is a variable frequency but linear control over the transient events such that it can evenly distribute the pulses among all phases to achieve a very good current balance and eliminate the beat frequency oscillation over wide frequency range of load transients.

To further improve the line and load transient responses, the multi-phase PWM features feedforward function to change the up ramp with the input line to maintain a constant overall loop gain over a wide range input voltage. The up ramp of the internal Sawtooth is defined in Equation 3.

$$V_{RAMP} = \frac{5 \cdot 10^{10} \cdot V_{IN}}{F_{SW} \cdot R_{RAMP\_ADJ}}$$ (EQ. 3)

With EAPP control and feedforward function, the ISL6364 can achieve excellent transient performance over wide frequency range of load step, resulting in lower demand on the output capacitors.

At DC load conditions, the PWM frequency is constant and set by the external resistor between the FS pin and GND during normal mode (PSI0) and low power mode (PSI1). However, when PSI2 or PSI3 is asserted in ultra low power conditions and if the VR is configured into diode emulation operation, the EAPP reduces the switching frequency as the load decreases. Thus, the VR can enter burst mode at extreme light load conditions and improve power conversion efficiency significantly.

Under steady state conditions, the operation of the ISL6364 PWM modulator appears to be that of a conventional trailing edge modulator. Conventional analysis and design methods can therefore be used for steady state and small signal operation.

The single-phase PWM has a fix ramp of 2V peak to peak. Its modulation gain does not change with the input line.

PWM and PSI# Operation

The timing of each channel is set by the number of active channels. The default channel setting for the ISL6364 is four. The switching cycle is defined as the time between PWM pulse termination signals of each channel. The cycle time of the pulse signal is the inverse of the switching frequency set by the resistor between the FS pin and ground. The PWM signals command the MOSFET driver to turn on/off the channel MOSFETs.

The ISL6364 can work in a 0 to 4-Phase configuration. Tie PWM(N+1) to VCC to configure for N-phase operation. PWM firing order is sequential from 1 to N with N being the number of active phases, as summarized in Table 1. For 4-phase operation, the channel firing sequence is 1-2-3-4, and they are evenly spaced 1/4 of a cycle. Connecting PWM4 to VCC configures 3-phase operation, the channel firing order is 1-2-3 and the phase spacing is 1/3 of a cycle. If PWM2 is connected to VCC, only Channel 1 operation is selected. If PWM1 is connected to VCC, the multi-phase (VR0) operation is turned off; to ensure proper operation of VR1, the VR0's respective pins should be configured as described in "Disabling Output" on page 35.

TABLE 1. PHASE NUMBER AND PWM FIRING SEQUENCE

N	PHASE SEQUENCE PSI# = PSI0	PWM# TIED TO VCC	ACTIVE PHASE PSI# = PSI1
4	1-2-3-4	-	PWM1/3
3	1-2-3	PWM4	PWM1/2
2	1-2	PWM3	PWM1/2
1	1	PWM2	PWM1
0	OFF	PWM1	OFF

The CPU can enter four distinct power states, as shown in Table 2. The ISL6364 supports all states, but it treats PSI2 and PSI3 the same. In addition, the setDecay mode will automatically enter PSI2 state while decaying the output voltage. However, prior to the end of soft-start (i.e: VR_RDY goes high), the lower power mode (PSI1/2/3/Decay) is NOT enabled.

TABLE 2. POWER STATE COMMAND FROM CPU

STATE	DESCRIPTION
PSI0	High Power Mode, All Phases are running
PSI1	Low Power Mode
PSI2	Very Low Power Mode
PSI3	Ultra Low Power Mode, treated as PSI2
Decay	Automatically entering PSI2 and Ramping down the output voltage to a target voltage in Decay Mode

When the SVID bus sends PSI1/2/3 or setVID Decay command, it indicates the low power mode operation of the processor. The controller will start phase shedding the next switching pulse. The controller allows to drop the number of active phases according to the logic on Table 3 for high light load efficiency performance. The "NPSI" register and SICI pin are to program the controller in operation of non-coupled (SI), 2-phase coupled, or (N-x)-Phase coupled inductors. Different cases yield different PWM output behaviors on both dropped phase(s) and operational phase(s) as PSI# is asserted and de-asserted. When CPU sends PSI0 command, it will pull the controller back to normal CCM PWM operation to sustain an immediate heavy transient load and high efficiency. Note that "N-x" means N-x phase coupled and x phase(s) are uncoupled.

For 2-Phase coupled inductor (CI) operation, both coupled phases should be 180° out of phase. In low power states (PSI1/2/3/Decay), the opposite phase of the operational phase will turn on its Low-side MOSFET to circulate inductor current to minimize conduction loss when Phase 1 is high.

When PSI1 is asserted, the VR0 is in single-phase CCM operation with PWM1, or 2-phase CCM operation with PWM1 and 2, or 3, as shown in Table 1. The number of operational phases is configured by "NPSI" register, shown in Table 3. In PSI2/3/Decay state, only single phase is in DCM/CCM operation, which is programmed by the "DE" register; the opposite PWM 2, or 3 (depending upon configured maximum phase number as in Table 1) of the PWM1 however will pull low at PWM1 high in CI applications.

TABLE 3. PHASE DROPPING CONFIGURATION AT PSI1 AND PSI2/3/DECAY

SICI	NPSI	CODE		PSI1 Mode	PSI2/3 & DECAY
0	0	SI1	SI, (N-1)-CI	1-Phase	1-Phase
0	1	SI2	SI, (N-2)-CI	2-Phase	1-Phase
1	0	CI1	2-Phase CI	1-Phase	1-Phase
1	1	CI2	2-Phase CI	2-Phase	1-Phase

NOTE: For 2-Phase CI option, the dropped coupled phase turns on LGATE to circulate current when PWM1 is high.

The VR1 output can be disabled by pulling PWMS to VCC while the respective address is released for use with a different VR controller. For proper operation of VR0, the VR1's respective pins should be configured as described in "Disabling Output" on page 35.

While the controller is operational (VCC above POR, EN_VTT and EN_PWR are both high, valid VID inputs), it can pull the PWM pins to ~40% of VCC (~2V for 5V VCC bias) during various stages, such as soft-start delay, phase shedding operation, or fault conditions (OC or OV events). The matching driver's internal PWM resistor divider can further raise the PWM potential, but not lower it below the level set by the controller IC. The controller's PWM outputs are directly compatible with Intersil drivers that require 5V PWM signal amplitudes. Drivers requiring 3.3V PWM signal amplitudes are generally incompatible.

Diode Emulation Operation

To improve light efficiency, the ISL6364 can enter diode emulation operation in PSI2/3 or Decay mode. Users however should select Intersil VR12/IMVP7 compatible drivers: ISL6627 or ISL6625 for PSI# channel(s). The diode emulation should be disabled if non-compatible power stages or drivers are used.

Switching Frequency

Both VR0 and VR1 can independently set switching frequency, which is determined by the selection of the frequency-setting resistor, R_T, which is connected from FS or FSS pin to GND or VCC. Equation 4 and Figure 4 are provided to assist in selecting the correct resistor value.

$$R_T = \frac{5 \cdot 10^{10}}{F_{SW}} \qquad \text{(EQ. 4)}$$

where F_{SW} is the switching frequency of each phase.

Independent frequency for VR0 and VR1 allows for cost, efficiency, and performance optimization. Proximity between the power trains of the two regulators imposed by the space-constrained layouts can lead to cross-coupling. To minimize the effect of cross-coupling between regulators, select operating frequencies at least 50kHz apart.
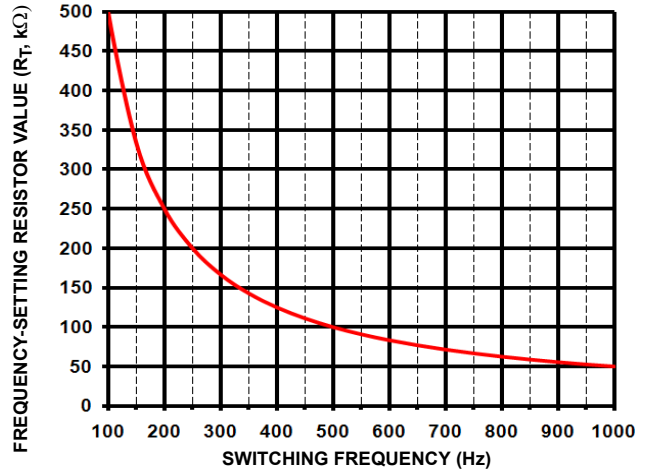
FIGURE 4. SWITCHING FREQUENCY vs RT

Current Sensing

The ISL6364 senses current continuously for fast response. The ISL6364 supports inductor DCR sensing, or resistive sensing techniques. The associated channel current sense amplifier uses the ISEN inputs to reproduce a signal proportional to the inductor current, I_L. The sense current, I_{SEN}, is proportional to the inductor current. The sensed current is used for current balance, load-line regulation, and overcurrent protection.

The internal circuitry, shown in Figures 5-6 and 9-10, represents VR1's channel or one channel of the VR0 output, respectively. For VR0 output, the ISEN± circuitry is repeated for each channel, but may not be active depending on the status of the PWM2, PWM3, and PWM4 pins, as described in "PWM and PSI# Operation" on page 15. The input bias current of the current sensing amplifier is typically 60nA; less than 8.34kΩ input impedance (0.5mV offset) is preferred to minimized the offset error, i.e., a larger C value as needed.

INDUCTOR DCR SENSING

An inductor's winding is characteristic of a distributed resistance, as measured by the DCR (Direct Current Resistance) parameter. Consider the inductor DCR as a separate lumped quantity, as shown in Figure 5. The channel current I_L, flowing through the inductor, will also pass through the DCR. Equation 5 shows the s-domain equivalent voltage across the inductor V_L.

$$V_L(s) = I_L \cdot (s \cdot L + DCR) \qquad \text{(EQ. 5)}$$

A simple R-C network across the inductor extracts the DCR voltage, as shown in Figure 5.

ISL6364
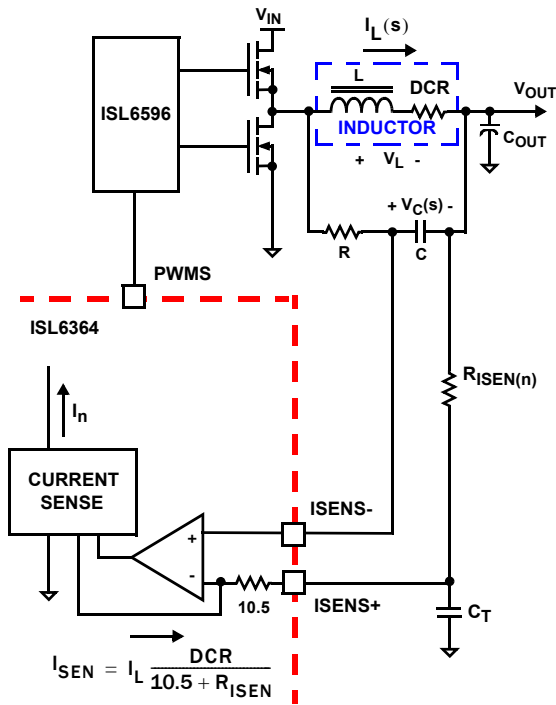
FIGURE 5. DCR SENSING CONFIGURATION FOR VR1

The voltage on the capacitor V_C, can be shown to be proportional to the channel current I_L. See Equation 6.

$$V_C(s) = \frac{\left(s \cdot \frac{L}{DCR} + 1\right) \cdot (DCR \cdot I_L)}{(s \cdot RC + 1)} \quad \text{(EQ. 6)}$$

If the R-C network components are selected such that the RC time constant matches the inductor time constant (R*C = L/DCR), the voltage across the capacitor V_C is equal to the voltage drop across the DCR, i.e., proportional to the channel current.

With the internal low-offset current amplifier, the capacitor voltage V_C is replicated across the sense resistor R_{ISEN}. Therefore, the current out of the ISENS+ pin, I_{SEN}, is proportional to the inductor current.

Because of the internal filter at the ISENS- pin, one capacitor, C_T, is needed to match the time delay between the ISENS- and ISENS+ signals. Select the proper C_T to keep the time constant of R_{ISEN} and C_T (R_{ISEN} x C_T) close to 27ns.

Equation 7 shows that the ratio of the channel current to the sensed current, I_{SEN}, is driven by the value of the sense resistor and the DCR of the inductor.

$$I_{SEN} = I_L \cdot \frac{DCR}{R_{ISEN}} \quad \text{(EQ. 7)}$$

RESISTIVE SENSING

For more accurate current sensing, a dedicated current-sense resistor R_{SENSE} in series with each output inductor can serve as the current sense element (see Figure 6). This technique however reduces overall converter efficiency due to the additional power loss on the current sense element R_{SENSE}.
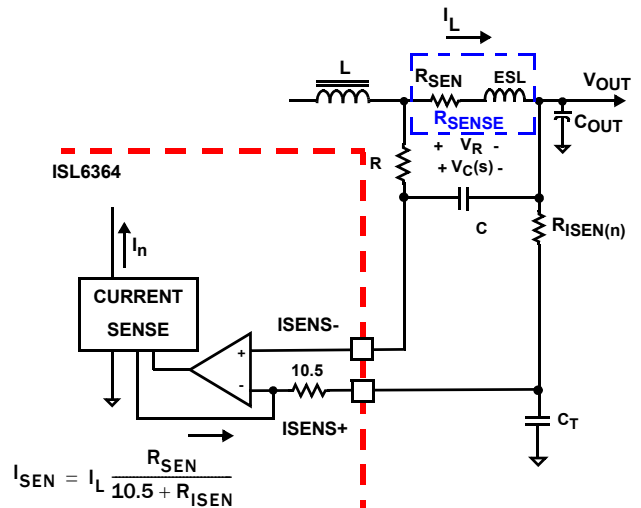
FIGURE 6. SENSE RESISTOR IN SERIES WITH INDUCTOR FOR VR1

A current sensing resistor has a distributed parasitic inductance, known as ESL (equivalent series inductance, typically less than 1nH) parameter. Consider the ESL as a separate lumped quantity, as shown in Figure 6. The channel current I_L, flowing through the inductor, will also pass through the ESL. Equation 8 shows the s-domain equivalent voltage across the resistor V_R.

$$V_R(s) = I_L \cdot (s \cdot ESL + R_{SEN}) \quad \text{(EQ. 8)}$$

A simple R-C network across the current sense resistor extracts the R_{SEN} voltage, as shown in Figure 6.

The voltage on the capacitor V_C, can be shown to be proportional to the channel current I_L. See Equation 9.

$$V_C(s) = \frac{\left(s \cdot \frac{ESL}{R_{SEN}} + 1\right) \cdot (R_{SEN} \cdot I_L)}{(s \cdot RC + 1)} \quad \text{(EQ. 9)}$$

If the R-C network components are selected such that the RC time constant matches the ESL-R_{SEN} time constant (R*C = ESL/R_{SEN}), the voltage across the capacitor V_C is equal to the voltage drop across the R_{SEN}, i.e., proportional to the channel current. As an example, a typical 1mΩ sense resistor can use R = 348 and C = 820pF for the matching. Figures 7 and 8 show the sensed waveforms without and with matching RC when using resistive sense.

Because of the internal filter at the ISENS- pin, one capacitor, C_T, is needed to match the time delay between the ISENS- and ISENS+ signals. Select the proper C_T to keep the time constant of R_{ISEN} and C_T (R_{ISEN} x C_T) close to 27ns.
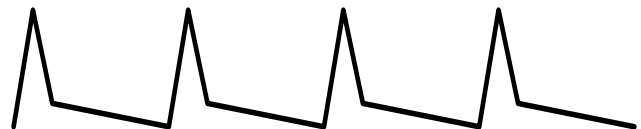
FIGURE 7. VOLTAGE ACROSS R WITHOUT RC

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December 22, 2010

FIGURE 8. VOLTAGE ACROSS C WITH MATCHING RC

Equation 10 shows that the ratio of the channel current to the sensed current, I_{SEN}, is driven by the value of the sense resistor and the R_{ISEN}.

$$I_{SEN} = I_L \cdot \frac{R_{SEN}}{R_{ISEN}} \qquad \text{(EQ. 10)}$$

Figures 5 and 7 configurations apply for VR1 output, while the R_{ISEN} should include the internal metal impedance of 10.5Ω for accurate current sense.

For VR0 output, the R_{ISEN} resistor of each channel is integrated, while its value is determined by the R_{SET} resistor. The R_{SET} resistor value can be from 3.84kΩ to 115.2kΩ and is 64x of the required ISEN resistor value. Therefore, the current sense gain resistor (Integrated R_{ISEN}) value is effectively set at 60Ω to 1.8kΩ. Figures 9 and 10 show the configurations for inductor DCR sensing and resistive sensing of VR0, respectively; their sensing current is represented by Equations 11 and 12, respectively.

$$I_{SEN} = I_L \cdot \frac{DCR \cdot 64}{R_{SET}} \qquad \text{(EQ. 11)}$$

$$I_{SEN} = I_L \cdot \frac{R_{SEN} \cdot 64}{R_{SET}} \qquad \text{(EQ. 12)}$$

The inductor DCR value will increase as the temperature increases. Therefore, the sensed current will increase as the temperature of the current sense element increases. In order to compensate the temperature effect on the sensed current signal, a Negative Temperature Coefficient (NTC) resistor can be used for thermal compensation, or the integrated temperature compensation function of ISL6364 should be utilized. The integrated temperature compensation function is described in "Temperature Compensation" on page 31.

Decoupling capacitor (C_T) on ISEN[4:1]- pins are optional and might be required for long sense traces and a poor layout.

FIGURE 9. DCR SENSING CONFIGURATION FOR VR0

FIGURE 10. SENSE RESISTOR IN SERIES WITH INDUCTORS FOR VR0

L/DCR OR ESL/R$_{SEN}$ MATCHING

Assuming the compensator design is correct, Figure 11 shows the expected load transient response waveforms if L/DCR or ESL/R$_{SEN}$ is matching the R-C time constant. When the load current I$_{OUT}$ has a square change, the output voltage V$_{OUT}$ also has a square response, except for the overshoot at load release. However, there is always some PCB contact impedance of current sensing components between the two current sensing points; it hardly accounts into the L/DCR or ESL/R$_{SEN}$ matching calculation. Fine tuning the matching is necessarily done in the board level to improve overall transient performance and system reliability.

If the R-C timing constant is too large or too small, V$_C$(s) will not accurately represent real-time I$_{OUT}$(s) and will worsen the transient response. Figure 12 shows the load transient response when the R-C timing constant is too small. V$_{OUT}$ will sag excessively upon load insertion and may create a system failure or early overcurrent trip. Figure 13 shows the transient response when the R-C timing constant is too large. V$_{OUT}$ is sluggish in drooping to its final value. There will be excessive overshoot if load insertion occurs during this time, which may potentially hurt the CPU reliability.
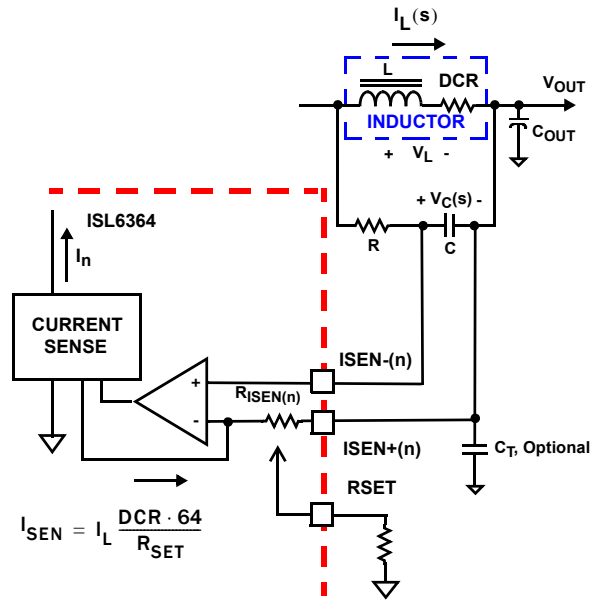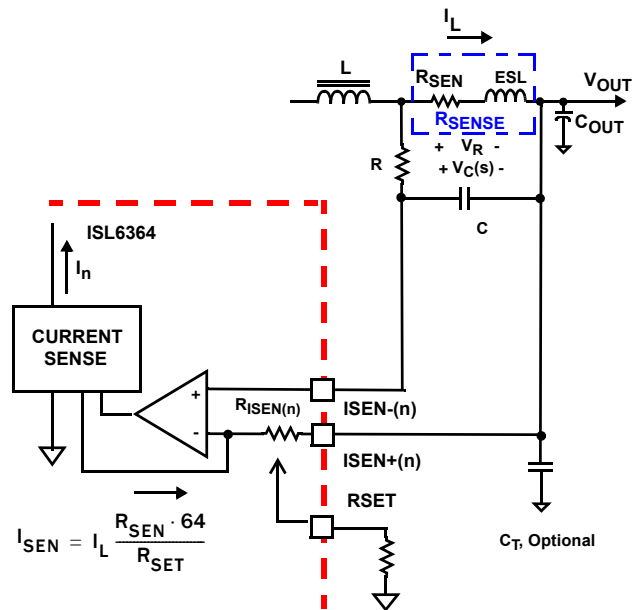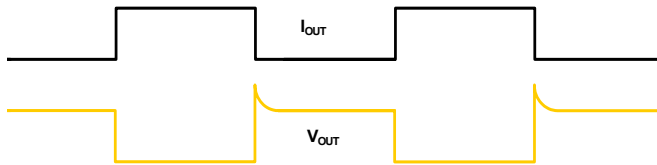

FIGURE 11. DESIRED LOAD TRANSIENT RESPONSE WAVEFORMS
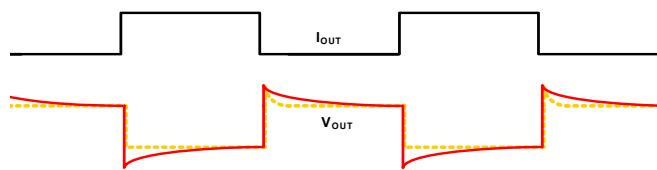
FIGURE 12. LOAD TRANSIENT RESPONSE WHEN R-C TIME CONSTANT IS TOO SMALL
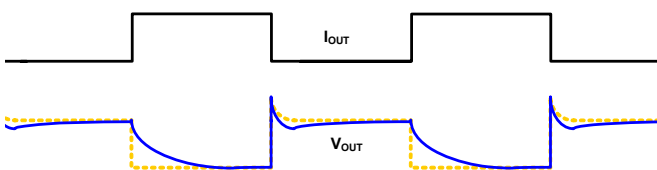
FIGURE 13. LOAD TRANSIENT RESPONSE WHEN R-C TIME CONSTANT IS TOO LARGE

Channel-Current Balance for VR0

The sensed current I$_n$ from each active channel is summed together and divided by the number of active channels. The resulting average current I$_{AVG}$ provides a measure of the total load current. Channel current balance is achieved by comparing the sensed current of each channel to the average current to

make an appropriate adjustment to the PWM duty cycle of each channel with Intersil's patented current-balance method.

Channel current balance is essential in achieving the thermal advantage of multiphase operation. With good current balance, the power loss is equally dissipated over multiple devices and a greater area.

Voltage Regulation

The compensation network shown in Figure 14 assures that the steady-state error in the output voltage is limited only to the error in the reference voltage (DAC & OFFSET) and droop current source, remote sense, and error amplifier.

The sensed average current I$_{DROOP}$ is tied to FB internally and will develop voltage drop across the resistor between FB and V$_{OUT}$ for droop control. This current can be disconnected from the FB node by tying R$_{FS\_DRP}$ high to VCC for non-droop applications.

The output of the error amplifier, V$_{COMP}$, is compared to the internal sawtooth waveforms to generate the PWM signals. The PWM signals control the timing of the Intersil MOSFET drivers and regulate the converter output to the specified reference voltage.

The ISL6364 does not have a unity gain amplifier in between the feedback path and error amplifier. For remote sensing, connect the microprocessor sensing pins to the non-inverting input, FB, via the feedback resistor (R$_{FB}$), and inverting input, RGND, of the error amplifier. This configuration effectively removes the voltage error encountered when measuring the output voltage relative to the local controller ground reference point. VSEN should connect to remote sensing's positive rail as well for over voltage protection.
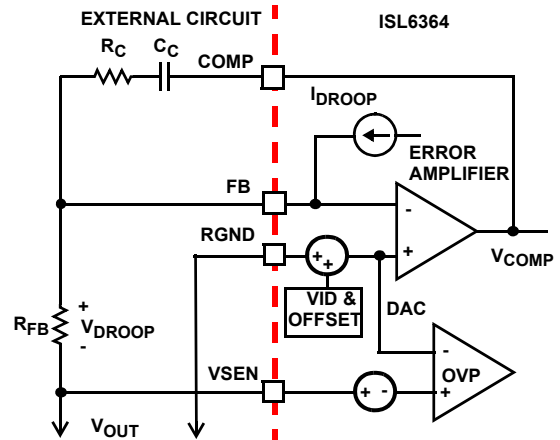
FIGURE 14. OUTPUT VOLTAGE AND LOAD-LINE REGULATION

A digital-to-analog converter (DAC) generates a reference voltage, which is programmable via SVID bus. The DAC decodes the SVID set command into one of the discrete voltages shown in Table 4 on page 20. In addition, the output voltage can be margined in ±5mV step between -640mV and 635mV, as shown in Table 5 on page 23, via SVID set OFFSET command (33h). For a finer than 5mV offset, a large ratio resistor divider can be placed on the FB pin between the output and GND for positive offset or VCC for negative offset.

VR1's VSENS, RGNDS, FBS, and COMPS pins function in the similar manner as VR0's VSEN, RGND, FB, and COMP pins.

ISL6364

TABLE 4. VR12/IMVP7 VID 8-BIT

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	VOLTAGE
0	0	0	0	0	0	0	0	00	OFF
0	0	0	0	0	0	0	1	01	0.2500
0	0	0	0	0	0	1	0	02	0.2550
0	0	0	0	0	0	1	1	03	0.2600
0	0	0	0	0	1	0	0	04	0.2650
0	0	0	0	0	1	0	1	05	0.2700
0	0	0	0	0	1	1	0	06	0.2750
0	0	0	0	0	1	1	1	07	0.2800
0	0	0	0	1	0	0	0	08	0.2850
0	0	0	0	1	0	0	1	09	0.2900
0	0	0	0	1	0	1	0	0A	0.2950
0	0	0	0	1	0	1	1	0B	0.3000
0	0	0	0	1	1	0	0	0C	0.3050
0	0	0	0	1	1	0	1	0D	0.3100
0	0	0	0	1	1	1	0	0E	0.3150
0	0	0	0	1	1	1	1	0F	0.3200
0	0	0	1	0	0	0	0	10	0.3250
0	0	0	1	0	0	0	1	11	0.3300
0	0	0	1	0	0	1	0	12	0.3350
0	0	0	1	0	0	1	1	13	0.3400
0	0	0	1	0	1	0	0	14	0.3450
0	0	0	1	0	1	0	1	15	0.3500
0	0	0	1	0	1	1	0	16	0.3550
0	0	0	1	0	1	1	1	17	0.3600
0	0	0	1	1	0	0	0	18	0.3650
0	0	0	1	1	0	0	1	19	0.3700
0	0	0	1	1	0	1	0	1A	0.3750
0	0	0	1	1	0	1	1	1B	0.3800
0	0	0	1	1	1	0	0	1C	0.3850
0	0	0	1	1	1	0	1	1D	0.3900
0	0	0	1	1	1	1	0	1E	0.3950
0	0	0	1	1	1	1	1	1F	0.4000
0	0	1	0	0	0	0	0	20	0.4050
0	0	1	0	0	0	0	1	21	0.4100
0	0	1	0	0	0	1	0	22	0.4150
0	0	1	0	0	0	1	1	23	0.4200
0	0	1	0	0	1	0	0	24	0.4250
0	0	1	0	0	1	0	1	25	0.4300
0	0	1	0	0	1	1	0	26	0.4350
0	0	1	0	0	1	1	1	27	0.4400

TABLE 4. VR12/IMVP7 VID 8-BIT (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	VOLTAGE
0	0	1	0	1	0	0	0	28	0.4450
0	0	1	0	1	0	0	1	29	0.4500
0	0	1	0	1	0	1	0	2A	0.4550
0	0	1	0	1	0	1	1	2B	0.4600
0	0	1	0	1	1	0	0	2C	0.4650
0	0	1	0	1	1	0	1	2D	0.4700
0	0	1	0	1	1	1	0	2E	0.4750
0	0	1	0	1	1	1	1	2F	0.4800
0	0	1	1	0	0	0	0	30	0.4850
0	0	1	1	0	0	0	1	31	0.4900
0	0	1	1	0	0	1	0	32	0.4950
0	0	1	1	0	0	1	1	33	0.5000
0	0	1	1	0	1	0	0	34	0.5050
0	0	1	1	0	1	0	1	35	0.5100
0	0	1	1	0	1	1	0	36	0.5150
0	0	1	1	0	1	1	1	37	0.5200
0	0	1	1	1	0	0	0	38	0.5250
0	0	1	1	1	0	0	1	39	0.5300
0	0	1	1	1	0	1	0	3A	0.5350
0	0	1	1	1	0	1	1	3B	0.5400
0	0	1	1	1	1	0	0	3C	0.5450
0	0	1	1	1	1	0	1	3D	0.5500
0	0	1	1	1	1	1	0	3E	0.5550
0	0	1	1	1	1	1	1	3F	0.5600
0	1	0	0	0	0	0	0	40	0.5650
0	1	0	0	0	0	0	1	41	0.5700
0	1	0	0	0	0	1	0	42	0.5750
0	1	0	0	0	0	1	1	43	0.5800
0	1	0	0	0	1	0	0	44	0.5850
0	1	0	0	0	1	0	1	45	0.5900
0	1	0	0	0	1	1	0	46	0.5950
0	1	0	0	0	1	1	1	47	0.6000
0	1	0	0	1	0	0	0	48	0.6050
0	1	0	0	1	0	0	1	49	0.6100
0	1	0	0	1	0	1	0	4A	0.6150
0	1	0	0	1	0	1	1	4B	0.6200
0	1	0	0	1	1	0	0	4C	0.6250
0	1	0	0	1	1	0	1	4D	0.6300
0	1	0	0	1	1	1	0	4E	0.6350
0	1	0	0	1	1	1	1	4F	0.6400

TABLE 4. VR12/IMVP7 VID 8-BIT (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	VOLTAGE
0	1	0	1	0	0	0	0	5 0	0.6450
0	1	0	1	0	0	0	1	5 1	0.6500
0	1	0	1	0	0	1	0	5 2	0.6550
0	1	0	1	0	0	1	1	5 3	0.6600
0	1	0	1	0	1	0	0	5 4	0.6650
0	1	0	1	0	1	0	1	5 5	0.6700
0	1	0	1	0	1	1	0	5 6	0.6750
0	1	0	1	0	1	1	1	5 7	0.6800
0	1	0	1	1	0	0	0	5 8	0.6850
0	1	0	1	1	0	0	1	5 9	0.6900
0	1	0	1	1	0	1	0	5 A	0.6950
0	1	0	1	1	0	1	1	5 B	0.7000
0	1	0	1	1	1	0	0	5 C	0.7050
0	1	0	1	1	1	0	1	5 D	0.7100
0	1	0	1	1	1	1	0	5 E	0.7150
0	1	0	1	1	1	1	1	5 F	0.7200
0	1	1	0	0	0	0	0	6 0	0.7250
0	1	1	0	0	0	0	1	6 1	0.7300
0	1	1	0	0	0	1	0	6 2	0.7350
0	1	1	0	0	0	1	1	6 3	0.7400
0	1	1	0	0	1	0	0	6 4	0.7450
0	1	1	0	0	1	0	1	6 5	0.7500
0	1	1	0	0	1	1	0	6 6	0.7550
0	1	1	0	0	1	1	1	6 7	0.7600
0	1	1	0	1	0	0	0	6 8	0.7650
0	1	1	0	1	0	0	1	6 9	0.7700
0	1	1	0	1	0	1	0	6 A	0.7750
0	1	1	0	1	0	1	1	6 B	0.7800
0	1	1	0	1	1	0	0	6 C	0.7850
0	1	1	0	1	1	0	1	6 D	0.7900
0	1	1	0	1	1	1	0	6 E	0.7950
0	1	1	0	1	1	1	1	6 F	0.8000
0	1	1	1	0	0	0	0	7 0	0.8050
0	1	1	1	0	0	0	1	7 1	0.8100
0	1	1	1	0	0	1	0	7 2	0.8150
0	1	1	1	0	0	1	1	7 3	0.8200
0	1	1	1	0	1	0	0	7 4	0.8250
0	1	1	1	0	1	0	1	7 5	0.8300
0	1	1	1	0	1	1	0	7 6	0.8350
0	1	1	1	0	1	1	1	7 7	0.8400

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	VOLTAGE
0	1	1	1	1	0	0	0	7 8	0.8450
0	1	1	1	1	0	0	1	7 9	0.8500
0	1	1	1	1	0	1	0	7 A	0.8550
0	1	1	1	1	0	1	1	7 B	0.8600
0	1	1	1	1	1	0	0	7 C	0.8650
0	1	1	1	1	1	0	1	7 D	0.8700
0	1	1	1	1	1	1	0	7 E	0.8750
0	1	1	1	1	1	1	1	7 F	0.8800
1	0	0	0	0	0	0	0	8 0	0.8850
1	0	0	0	0	0	0	1	8 1	0.8900
1	0	0	0	0	0	1	0	8 2	0.8950
1	0	0	0	0	0	1	1	8 3	0.9000
1	0	0	0	0	1	0	0	8 4	0.9050
1	0	0	0	0	1	0	1	8 5	0.9100
1	0	0	0	0	1	1	0	8 6	0.9150
1	0	0	0	0	1	1	1	8 7	0.9200
1	0	0	0	1	0	0	0	3 8	0.9250
1	0	0	0	1	0	0	1	8 9	0.9300
1	0	0	0	1	0	1	0	8 A	0.9350
1	0	0	0	1	0	1	1	8 B	0.9400
1	0	0	0	1	1	0	0	8 C	0.9450
1	0	0	0	1	1	0	1	8 D	0.9500
1	0	0	0	1	1	1	0	8 E	0.9550
1	0	0	0	1	1	1	1	8 F	0.9600
1	0	0	1	0	0	0	0	9 0	0.9650
1	0	0	1	0	0	0	1	9 1	0.9700
1	0	0	1	0	0	1	0	9 2	0.9750
1	0	0	1	0	0	1	1	9 3	0.9800
1	0	0	1	0	1	0	0	9 4	0.9850
1	0	0	1	0	1	0	1	9 5	0.9900
1	0	0	1	0	1	1	0	9 6	0.9950
1	0	0	1	0	1	1	1	9 7	1.0000
1	0	0	1	1	0	0	0	9 8	1.0050
1	0	0	1	1	0	0	1	9 9	1.0100
1	0	0	1	1	0	1	0	9 A	1.0150
1	0	0	1	1	0	1	1	9 B	1.0200
1	0	0	1	1	1	0	0	9 C	1.0250
1	0	0	1	1	1	0	1	9 D	1.0300
1	0	0	1	1	1	1	0	9 E	1.0350
1	0	0	1	1	1	1	1	9 F	1.0400

TABLE 4. VR12/IMVP7 VID 8-BIT (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX		VOLTAGE
1	0	1	0	0	0	0	0	A	0	1.0450
1	0	1	0	0	0	0	1	A	1	1.0500
1	0	1	0	0	0	1	0	A	2	1.0550
1	0	1	0	0	0	1	1	A	3	1.0600
1	0	1	0	0	1	0	0	A	4	1.0650
1	0	1	0	0	1	0	1	A	5	1.0700
1	0	1	0	0	1	1	0	A	6	1.0750
1	0	1	0	0	1	1	1	A	7	1.0800
1	0	1	0	1	0	0	0	A	8	1.0850
1	0	1	0	1	0	0	1	A	9	1.0900
1	0	1	0	1	0	1	0	A	A	1.0950
1	0	1	0	1	0	1	1	A	B	1.1000
1	0	1	0	1	1	0	0	A	C	1.1050
1	0	1	0	1	1	0	1	A	D	1.1100
1	0	1	0	1	1	1	0	A	E	1.1150
1	0	1	0	1	1	1	1	A	F	1.1200
1	0	1	1	0	0	0	0	B	0	1.1250
1	0	1	1	0	0	0	1	B	1	1.1300
1	0	1	1	0	0	1	0	B	2	1.1350
1	0	1	1	0	0	1	1	B	3	1.1400
1	0	1	1	0	1	0	0	B	4	1.1450
1	0	1	1	0	1	0	1	B	5	1.1500
1	0	1	1	0	1	1	0	B	6	1.1550
1	0	1	1	0	1	1	1	B	7	1.1600
1	0	1	1	1	0	0	0	B	8	1.1650
1	0	1	1	1	0	0	1	B	9	1.1700
1	0	1	1	1	0	1	0	B	A	1.1750
1	0	1	1	1	0	1	1	B	B	1.1800
1	0	1	1	1	1	0	0	B	C	1.1850
1	0	1	1	1	1	0	1	B	D	1.1900
1	0	1	1	1	1	1	0	B	E	1.1950
1	0	1	1	1	1	1	1	B	F	1.2000
1	1	0	0	0	0	0	0	C	0	1.2050
1	1	0	0	0	0	0	1	C	1	1.2100
1	1	0	0	0	0	1	0	C	2	1.2150
1	1	0	0	0	0	1	1	C	3	1.2200
1	1	0	0	0	1	0	0	C	4	1.2250
1	1	0	0	0	1	0	1	C	5	1.2300
1	1	0	0	0	1	1	0	C	6	1.2350
1	1	0	0	0	1	1	1	C	7	1.2400

TABLE 4. VR12/IMVP7 VID 8-BIT (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX		VOLTAGE
1	1	0	0	1	0	0	0	C	8	1.2450
1	1	0	0	1	0	0	1	C	9	1.2500
1	1	0	0	1	0	1	0	C	A	1.2550
1	1	0	0	1	0	1	1	C	B	1.2600
1	1	0	0	1	1	0	0	C	C	1.2650
1	1	0	0	1	1	0	1	C	D	1.2700
1	1	0	0	1	1	1	0	C	E	1.2750
1	1	0	0	1	1	1	1	C	F	1.2800
1	1	0	1	0	0	0	0	D	0	1.2850
1	1	0	1	0	0	0	1	D	1	1.2900
1	1	0	1	0	0	1	0	D	2	1.2950
1	1	0	1	0	0	1	1	D	3	1.3000
1	1	0	1	0	1	0	0	D	4	1.3050
1	1	0	1	0	1	0	1	D	5	1.3100
1	1	0	1	0	1	1	0	D	6	1.3150
1	1	0	1	0	1	1	1	D	7	1.3200
1	1	0	1	1	0	0	0	D	8	1.3250
1	1	0	1	1	0	0	1	D	9	1.3300
1	1	0	1	1	0	1	0	D	A	1.3350
1	1	0	1	1	0	1	1	D	B	1.3400
1	1	0	1	1	1	0	0	D	C	1.3450
1	1	0	1	1	1	0	1	D	D	1.3500
1	1	0	1	1	1	1	0	D	E	1.3550
1	1	0	1	1	1	1	1	D	F	1.3600
1	1	1	0	0	0	0	0	E	0	1.3650
1	1	1	0	0	0	0	1	E	1	1.3700
1	1	1	0	0	0	1	0	E	2	1.3750
1	1	1	0	0	0	1	1	E	3	1.3800
1	1	1	0	0	1	0	0	E	4	1.3850
1	1	1	0	0	1	0	1	E	5	1.3900
1	1	1	0	0	1	1	0	E	6	1.3950
1	1	1	0	0	1	1	1	E	7	1.4000
1	1	1	0	1	0	0	0	E	8	1.4050
1	1	1	0	1	0	0	1	E	9	1.4100
1	1	1	0	1	0	1	0	E	A	1.4150
1	1	1	0	1	0	1	1	E	B	1.4200
1	1	1	0	1	1	0	0	E	C	1.4250
1	1	1	0	1	1	0	1	E	D	1.4300
1	1	1	0	1	1	1	0	E	E	1.4350
1	1	1	0	1	1	1	1	E	F	1.4400

TABLE 4. VR12/IMVP7 VID 8-BIT (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX		VOLTAGE
1	1	1	1	0	0	0	0	F	0	1.4450
1	1	1	1	0	0	0	1	F	1	1.4500
1	1	1	1	0	0	1	0	F	2	1.4550
1	1	1	1	0	0	1	1	F	3	1.4600
1	1	1	1	0	1	0	0	F	4	1.4650
1	1	1	1	0	1	0	1	F	5	1.4700
1	1	1	1	0	1	1	0	F	6	1.4750
1	1	1	1	0	1	1	1	F	7	1.4800
1	1	1	1	1	0	0	0	F	8	1.4850
1	1	1	1	1	0	0	1	F	9	1.4900
1	1	1	1	1	0	1	0	F	A	1.4950
1	1	1	1	1	0	1	1	F	B	1.5000
1	1	1	1	1	1	0	0	F	C	1.5050
1	1	1	1	1	1	0	1	F	D	1.5100
1	1	1	1	1	1	1	0	F	E	1.5150
1	1	1	1	1	1	1	1	F	F	1.5200

TABLE 5. VR12/IMVP7 -640/+635mV OFFSET 8-BIT

OFS7	OFS6	OFS5	OFS4	OFS3	OFS2	OFS1	OFS0	HEX		VOLTAGE (mV)
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	1	0	0	2	10
0	0	0	0	0	0	1	1	0	3	15
0	0	0	0	0	1	0	0	0	4	20
0	0	0	0	0	1	0	1	0	5	25
0	0	0	0	0	1	1	0	0	6	30
0	0	0	0	0	1	1	1	0	7	35
0	0	0	0	1	0	0	0	0	8	40
0	0	0	0	1	0	0	1	0	9	45
0	0	0	0	1	0	1	0	0	A	50
0	0	0	0	1	0	1	1	0	B	55
0	0	0	0	1	1	0	0	0	C	60
0	0	0	0	1	1	0	1	0	D	65
0	0	0	0	1	1	1	0	0	E	70
0	0	0	0	1	1	1	1	0	F	75
0	0	0	1	0	0	0	0	1	0	80
0	0	0	1	0	0	0	1	1	1	85
0	0	0	1	0	0	1	0	1	2	90
0	0	0	1	0	0	1	1	1	3	95

TABLE 5. VR12/IMVP7 -640/+635mV OFFSET 8-BIT (Continued)

OFS7	OFS6	OFS5	OFS4	OFS3	OFS2	OFS1	OFS0	HEX		VOLTAGE (mV)
0	0	0	1	0	1	0	0	1	4	100
0	0	0	1	0	1	0	1	1	5	105
0	0	0	1	0	1	1	0	1	6	110
0	0	0	1	0	1	1	1	1	7	115
0	0	0	1	1	0	0	0	1	8	120
0	0	0	1	1	0	0	1	1	9	125
0	0	0	1	1	0	1	0	1	A	130
0	0	0	1	1	0	1	1	1	B	135
0	0	0	1	1	1	0	0	1	C	140
0	0	0	1	1	1	0	1	1	D	145
0	0	0	1	1	1	1	0	1	E	150
0	0	0	1	1	1	1	1	1	F	155
0	0	1	0	0	0	0	0	2	0	160
0	0	1	0	0	0	0	1	2	1	165
0	0	1	0	0	0	1	0	2	2	170
0	0	1	0	0	0	1	1	2	3	175
0	0	1	0	0	1	0	0	2	4	180
0	0	1	0	0	1	0	1	2	5	185
0	0	1	0	0	1	1	0	2	6	190
0	0	1	0	0	1	1	1	2	7	195
0	0	1	0	1	0	0	0	2	8	200
0	0	1	0	1	0	0	1	2	9	205
0	0	1	0	1	0	1	0	2	A	210
0	0	1	0	1	0	1	1	2	B	215
0	0	1	0	1	1	0	0	2	C	220
0	0	1	0	1	1	0	1	2	D	225
0	0	1	0	1	1	1	0	2	E	230
0	0	1	0	1	1	1	1	2	F	235
0	0	1	1	0	0	0	0	3	0	240
0	0	1	1	0	0	0	1	3	1	245
0	0	1	1	0	0	1	0	3	2	250
0	0	1	1	0	0	1	1	3	3	255
0	0	1	1	0	1	0	0	3	4	260
0	0	1	1	0	1	0	1	3	5	265
0	0	1	1	0	1	1	0	3	6	270
0	0	1	1	0	1	1	1	3	7	275
0	0	1	1	1	0	0	0	3	8	280
0	0	1	1	1	0	0	1	3	9	285
0	0	1	1	1	0	1	0	3	A	290

TABLE 5. VR12/IMVP7 -640/+635mV OFFSET 8-BIT (Continued)

OFS7	OFS6	OFS5	OFS4	OFS3	OFS2	OFS1	OFS0	HEX		VOLTAGE (mV)
0	0	1	1	1	0	1	1	3	B	295
0	0	1	1	1	1	0	0	3	C	300
0	0	1	1	1	1	0	1	3	D	305
0	0	1	1	1	1	1	0	3	E	310
0	0	1	1	1	1	1	1	3	F	315
0	1	0	0	0	0	0	0	4	0	320
0	1	0	0	0	0	0	1	4	1	325
0	1	0	0	0	0	1	0	4	2	330
0	1	0	0	0	0	1	1	4	3	335
0	1	0	0	0	1	0	0	4	4	340
0	1	0	0	0	1	0	1	4	5	345
0	1	0	0	0	1	1	0	4	6	350
0	1	0	0	0	1	1	1	4	7	355
0	1	0	0	1	0	0	0	4	8	360
0	1	0	0	1	0	0	1	4	9	365
0	1	0	0	1	0	1	0	4	A	370
0	1	0	0	1	0	1	1	4	B	375
0	1	0	0	1	1	0	0	4	C	380
0	1	0	0	1	1	0	1	4	D	385
0	1	0	0	1	1	1	0	4	E	390
0	1	0	0	1	1	1	1	4	F	395
0	1	0	1	0	0	0	0	5	0	400
0	1	0	1	0	0	0	1	5	1	405
0	1	0	1	0	0	1	0	5	2	410
0	1	0	1	0	0	1	1	5	3	415
0	1	0	1	0	1	0	0	5	4	420
0	1	0	1	0	1	0	1	5	5	425
0	1	0	1	0	1	1	0	5	6	430
0	1	0	1	0	1	1	1	5	7	435
0	1	0	1	1	0	0	0	5	8	440
0	1	0	1	1	0	0	1	5	9	445
0	1	0	1	1	0	1	0	5	A	450
0	1	0	1	1	0	1	1	5	B	455
0	1	0	1	1	1	0	0	5	C	460
0	1	0	1	1	1	0	1	5	D	465
0	1	0	1	1	1	1	0	5	E	470
0	1	0	1	1	1	1	1	5	F	475
0	1	1	0	0	0	0	0	6	0	480
0	1	1	0	0	0	0	1	6	1	485

OFS7	OFS6	OFS5	OFS4	OFS3	OFS2	OFS1	OFS0	HEX		VOLTAGE (mV)
0	1	1	0	0	0	1	0	6	2	490
0	1	1	0	0	0	1	1	6	3	495
0	1	1	0	0	1	0	0	6	4	500
0	1	1	0	0	1	0	1	6	5	505
0	1	1	0	0	1	1	0	6	6	510
0	1	1	0	0	1	1	1	6	7	515
0	1	1	0	1	0	0	0	6	8	520
0	1	1	0	1	0	0	1	6	9	525
0	1	1	0	1	0	1	0	6	A	530
0	1	1	0	1	0	1	1	6	B	535
0	1	1	0	1	1	0	0	6	C	540
0	1	1	0	1	1	0	1	6	D	545
0	1	1	0	1	1	1	0	6	E	550
0	1	1	0	1	1	1	1	6	F	555
0	1	1	1	0	0	0	0	7	0	560
0	1	1	1	0	0	0	1	7	1	565
0	1	1	1	0	0	1	0	7	2	570
0	1	1	1	0	0	1	1	7	3	575
0	1	1	1	0	1	0	0	7	4	580
0	1	1	1	0	1	0	1	7	5	585
0	1	1	1	0	1	1	0	7	6	590
0	1	1	1	0	1	1	1	7	7	595
0	1	1	1	1	0	0	0	7	8	600
0	1	1	1	1	0	0	1	7	9	605
0	1	1	1	1	0	1	0	7	A	610
0	1	1	1	1	0	1	1	7	B	615
0	1	1	1	1	1	0	0	7	C	620
0	1	1	1	1	1	0	1	7	D	625
0	1	1	1	1	1	1	0	7	E	630
0	1	1	1	1	1	1	1	7	F	635
1	0	0	0	0	0	0	0	8	0	-640
1	0	0	0	0	0	0	1	8	1	-635
1	0	0	0	0	0	1	0	8	2	-630
1	0	0	0	0	0	1	1	8	3	-625
1	0	0	0	0	1	0	0	8	4	-620
1	0	0	0	0	1	0	1	8	5	-615
1	0	0	0	0	1	1	0	8	6	-610
1	0	0	0	0	1	1	1	8	7	-605
1	0	0	0	1	0	0	0	3	8	-600

TABLE 5. VR12/IMVP7 -640/+635mV OFFSET 8-BIT (Continued)

OFS7	OFS6	OFS5	OFS4	OFS3	OFS2	OFS1	OFS0	HEX		VOLTAGE (mV)
1	0	0	0	1	0	0	1	8	9	-595
1	0	0	0	1	0	1	0	8	A	-590
1	0	0	0	1	0	1	1	8	B	-585
1	0	0	0	1	1	0	0	8	C	-580
1	0	0	0	1	1	0	1	8	D	-575
1	0	0	0	1	1	1	0	8	E	-570
1	0	0	0	1	1	1	1	8	F	-565
1	0	0	1	0	0	0	0	9	0	-560
1	0	0	1	0	0	0	1	9	1	-555
1	0	0	1	0	0	1	0	9	2	-550
1	0	0	1	0	0	1	1	9	3	-545
1	0	0	1	0	1	0	0	9	4	-540
1	0	0	1	0	1	0	1	9	5	-535
1	0	0	1	0	1	1	0	9	6	-530
1	0	0	1	0	1	1	1	9	7	-525
1	0	0	1	1	0	0	0	9	8	-520
1	0	0	1	1	0	0	1	9	9	-515
1	0	0	1	1	0	1	0	9	A	-510
1	0	0	1	1	0	1	1	9	B	-505
1	0	0	1	1	1	0	0	9	C	-500
1	0	0	1	1	1	0	1	9	D	-495
1	0	0	1	1	1	1	0	9	E	-490
1	0	0	1	1	1	1	1	9	F	-485
1	0	1	0	0	0	0	0	A	0	-480
1	0	1	0	0	0	0	1	A	1	-475
1	0	1	0	0	0	1	0	A	2	-470
1	0	1	0	0	0	1	1	A	3	-465
1	0	1	0	0	1	0	0	A	4	-460
1	0	1	0	0	1	0	1	A	5	-455
1	0	1	0	0	1	1	0	A	6	-450
1	0	1	0	0	1	1	1	A	7	-445
1	0	1	0	1	0	0	0	A	8	-440
1	0	1	0	1	0	0	1	A	9	-435
1	0	1	0	1	0	1	0	A	A	-430
1	0	1	0	1	0	1	1	A	B	-425
1	0	1	0	1	1	0	0	A	C	-420
1	0	1	0	1	1	0	1	A	D	-415
1	0	1	0	1	1	1	0	A	E	-410
1	0	1	0	1	1	1	1	A	F	-405

OFS7	OFS6	OFS5	OFS4	OFS3	OFS2	OFS1	OFS0	HEX		VOLTAGE (mV)
1	0	1	1	0	0	0	0	B	0	-400
1	0	1	1	0	0	0	1	B	1	-395
1	0	1	1	0	0	1	0	B	2	-390
1	0	1	1	0	0	1	1	B	3	-385
1	0	1	1	0	1	0	0	B	4	-380
1	0	1	1	0	1	0	1	B	5	-375
1	0	1	1	0	1	1	0	B	6	-370
1	0	1	1	0	1	1	1	B	7	-365
1	0	1	1	1	0	0	0	B	8	-360
1	0	1	1	1	0	0	1	B	9	-355
1	0	1	1	1	0	1	0	B	A	-350
1	0	1	1	1	0	1	1	B	B	-345
1	0	1	1	1	1	0	0	B	C	-340
1	0	1	1	1	1	0	1	B	D	-335
1	0	1	1	1	1	1	0	B	E	-330
1	0	1	1	1	1	1	1	B	F	-325
1	1	0	0	0	0	0	0	C	0	-320
1	1	0	0	0	0	0	1	C	1	-315
1	1	0	0	0	0	1	0	C	2	-310
1	1	0	0	0	0	1	1	C	3	-305
1	1	0	0	0	1	0	0	C	4	-300
1	1	0	0	0	1	0	1	C	5	-295
1	1	0	0	0	1	1	0	C	6	-290
1	1	0	0	0	1	1	1	C	7	-285
1	1	0	0	1	0	0	0	C	8	-280
1	1	0	0	1	0	0	1	C	9	-275
1	1	0	0	1	0	1	0	C	A	-270
1	1	0	0	1	0	1	1	C	B	-265
1	1	0	0	1	1	0	0	C	C	-260
1	1	0	0	1	1	0	1	C	D	-255
1	1	0	0	1	1	1	0	C	E	-250
1	1	0	0	1	1	1	1	C	F	-245
1	1	0	1	0	0	0	0	D	0	-240
1	1	0	1	0	0	0	1	D	1	-235
1	1	0	1	0	0	1	0	D	2	-230
1	1	0	1	0	0	1	1	D	3	-225
1	1	0	1	0	1	0	0	D	4	-220
1	1	0	1	0	1	0	1	D	5	-215
1	1	0	1	0	1	1	0	D	6	-210

TABLE 5. VR12/IMVP7 -640/+635mV OFFSET 8-BIT (Continued)

OFS7	OFS6	OFS5	OFS4	OFS3	OFS2	OFS1	OFS0	HEX		VOLTAGE (mV)
1	1	0	1	0	1	1	1	D	7	-205
1	1	0	1	1	0	0	0	D	8	-200
1	1	0	1	1	0	0	1	D	9	-195
1	1	0	1	1	0	1	0	D	A	-190
1	1	0	1	1	0	1	1	D	B	-185
1	1	0	1	1	1	0	0	D	C	-180
1	1	0	1	1	1	0	1	D	D	-175
1	1	0	1	1	1	1	0	D	E	-170
1	1	0	1	1	1	1	1	D	F	-165
1	1	1	0	0	0	0	0	E	0	-160
1	1	1	0	0	0	0	1	E	1	-155
1	1	1	0	0	0	1	0	E	2	-150
1	1	1	0	0	0	1	1	E	3	-145
1	1	1	0	0	1	0	0	E	4	-140
1	1	1	0	0	1	0	1	E	5	-135
1	1	1	0	0	1	1	0	E	6	-130
1	1	1	0	0	1	1	1	E	7	-125
1	1	1	0	1	0	0	0	E	8	-120
1	1	1	0	1	0	0	1	E	9	-115
1	1	1	0	1	0	1	0	E	A	-110
1	1	1	0	1	0	1	1	E	B	-105
1	1	1	0	1	1	0	0	E	C	-100
1	1	1	0	1	1	0	1	E	D	-95
1	1	1	0	1	1	1	0	E	E	-90
1	1	1	0	1	1	1	1	E	F	-85
1	1	1	1	0	0	0	0	F	0	-80
1	1	1	1	0	0	0	1	F	1	-75
1	1	1	1	0	0	1	0	F	2	-70
1	1	1	1	0	0	1	1	F	3	-65
1	1	1	1	0	1	0	0	F	4	-60
1	1	1	1	0	1	0	1	F	5	-55
1	1	1	1	0	1	1	0	F	6	-50
1	1	1	1	0	1	1	1	F	7	-45
1	1	1	1	1	0	0	0	F	8	-40
1	1	1	1	1	0	0	1	F	9	-35
1	1	1	1	1	0	1	0	F	A	-30
1	1	1	1	1	0	1	1	F	B	-25
1	1	1	1	1	1	0	0	F	C	-20
1	1	1	1	1	1	0	1	F	D	-15

TABLE 5. VR12/IMVP7 -640/+635mV OFFSET 8-BIT (Continued)

OFS7	OFS6	OFS5	OFS4	OFS3	OFS2	OFS1	OFS0	HEX		VOLTAGE (mV)
1	1	1	1	1	1	1	0	F	E	-10
1	1	1	1	1	1	1	1	F	F	-5

Load-Line Regulation

Some microprocessor manufacturers require a precisely controlled output resistance. This dependence of output voltage on load current is often termed "droop" or "load line" regulation. By adding a well controlled output impedance, the output voltage can effectively be level shifted in a direction, which works to achieve the load-line regulation required by these manufacturers.

In other cases, the designer may determine that a more cost-effective solution can be achieved by adding droop. Droop can help to reduce the output-voltage spike that results from fast load-current demand changes.

The magnitude of the spike is dictated by the ESR and ESL of the output capacitors selected. By positioning the no-load voltage level near the upper specification limit, a larger negative spike can be sustained without crossing the lower limit. By adding a well controlled output impedance, the output voltage under load can effectively be level shifted down so that a larger positive spike can be sustained without crossing the upper specification limit.

As shown in Figure 14, a current proportional to the average current of all active channels, I_{AVG}, flows from FB through a load-line regulation resistor R_{FB}. The resulting voltage drop across R_{FB} is proportional to the output current, effectively creating an output voltage droop with a steady-state value defined, as shown in Equation 13:

$$V_{DROOP} = I_{AVG} \cdot R_{FB} \qquad \text{(EQ. 13)}$$

The regulated output voltage is reduced by the droop voltage V_{DROOP}. The output voltage as a function of load current is derived by combining Equation 13 with the appropriate sample current expression defined by the current sense method employed, as shown in Equation 14:

$$V_{OUT} = V_{REF} - \left(\frac{I_{LOAD}}{N} \frac{R_X}{R_{ISEN}} R_{FB} \right) \qquad \text{(EQ. 14)}$$

where V_{REF} is the reference voltage (DAC), I_{LOAD} is the total output current of the converter, R_{ISEN} is the sense resistor connected to the ISEN+ pin, R_{FB} is the feedback resistor, N is the active channel number, and R_X is the DCR, or R_{SENSE} depending on the sensing method.

Therefore, the equivalent loadline impedance, i.e. Droop impedance, is equal to Equation 15:

$$R_{LL} = \frac{R_{FB}}{N} \frac{R_X}{R_{ISEN}} \qquad \text{(EQ. 15)}$$

The major regulation error comes from the current sensing elements. To improve load-line regulation accuracy, a tight DCR tolerance of inductor or a precision sensing resistor should be considered.

Output-Voltage Offset Programming

The output voltage can be margined in ±5mV steps between -640mV and 635mV, as shown in Table 5, via SVID set OFFSET command (33h). The minimum offset step is ±5mV. For a finer than 5mV offset, a large ratio resistor divider can be placed on the FB pin between the output and GND for positive offset or VCC for negative offset.

Dynamic VID

Modern voltage regulators need to make changes to their voltage as part of normal operation. They direct the voltage regulator to do this by making changes to the VID during regulator operation. The power management solution is required to monitor the DAC and respond to on-the-fly VID changes in a controlled manner. Supervising the safe output voltage transition within the DAC range of the processor or the load without discontinuity or disruption is a necessary function of the voltage regulator.

Three different slew rates can be selected during Dynamic VID (DVID) transition for VR0, but during VR0 soft-start, the setVID SLOW rate is defaulted. FDVID has no impact on VR1 rail, which can be 10mV/μs minimum rate for setVID Fast, 2.5mV/μs minimum rate for setVID Slow.

TABLE 6. SLEW RATE OPTIONS

	FDVID	SetVID FAST (Minimum Rate)	SetVID SLOW (Minimum Rate)
VR0	0	10mV/μs	2.5mV/μs
	1	20mV/μs	5.0mV/μs
VR1	DON'T CARE	10mV/μs	2.5mV/μs

During dynamic VID transition and VID step up, the overcurrent trip point increases by 140% to avoid falsely triggering OCP circuits, while the overvoltage trip point will follow the DAC+179mV level. If the dynamic VID occurs at PSI1/2/3/Decay (low power state) asserted, the system should exit to PSI0 (full power state) and complete the transition, and will not resume the low power state operation unless the low power mode command is asserted again.

In addition to ramping down the output voltage with a controlled rate as previously described, both VR0 and VR1 can be programmed into decay mode via SVID's setDecay command. Whenever the Decay command is received, the VR will enter PSI2 mode. The VR will be in single-phase operation. If the DE register is selected to be "Enable", the VR will operate in diode emulation mode and drop to the target voltage at a decay rate determined by the load impedance and output capacitive bank. The decay rate will be limited to 2.5mV/μs rate setting. If the "DE" register is selected to be "Disable", then VR will drop at 2.5mV/μs rate setting.

Operation Initialization

Prior to converter initialization, proper conditions must exist on the enable inputs and VCC. When the conditions are met, the controller begins soft-start. Once the output voltage is within the proper window of operation, VR_RDY asserts logic high.

Enable and Disable

While in shutdown mode, the PWM outputs are held in a high-impedance state (or pulled to 40% of VCC) (or pulled to 40% of VCC) to assure the drivers remain off. The following input conditions must be met before the ISL6364 is released from shutdown mode.

1. The bias voltage applied at VCC must reach the internal power-on reset (POR) rising threshold. Once this threshold is reached, proper operation of all aspects of the ISL6364 is guaranteed. Hysteresis between the rising and falling thresholds assure that once enabled, ISL6364 will not inadvertently turn off unless the bias voltage drops substantially (see "Electrical Specifications" table beginning on page 8).

2. The ISL6364 features an enable input (EN_PWR) for power sequencing between the controller bias voltage and another voltage rail. The enable comparator holds the ISL6364 in shutdown until the voltage at EN_PWR rises above 0.85V. The enable comparator has about 100mV of hysteresis to prevent bounce. It is important that the drivers reach their POR level before the ISL6364 becomes enabled. The schematic in Figure 15 demonstrates sequencing the ISL6364 with the ISL66xx family of Intersil MOSFET drivers.

3. The voltage on EN_VTT must be higher than 0.85V to enable the controller. This pin is typically connected to the output of VTT VR.
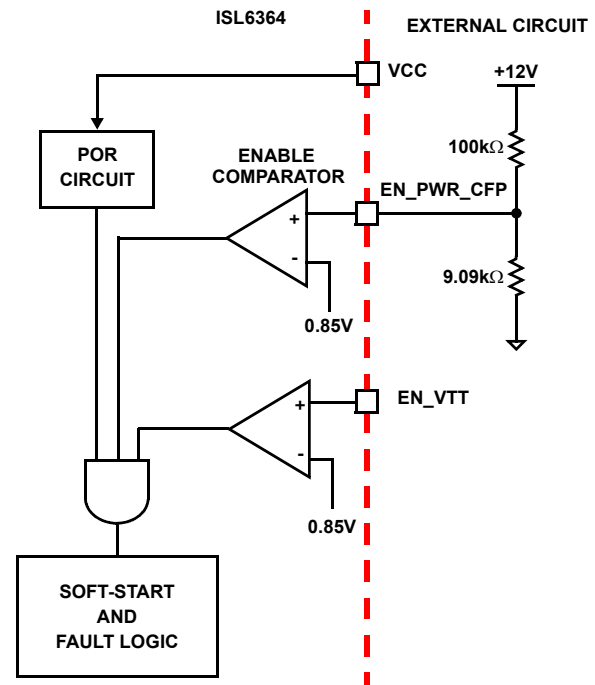
FIGURE 15. POWER SEQUENCING USING THRESHOLD-SENSITIVE ENABLE (EN) FUNCTION

When all conditions previously mentioned are satisfied, ISL6364 begins the soft-start and ramps the output voltage to the Boot Voltage set by hard-wired "BT" and "BTS" registers or first setVID command if boot voltage set to zero volts. After remaining at boot voltage for some time, ISL6364 reads the VID code via SVID bus. If the VID code is valid, ISL6364 will regulate the output to the final VID setting. If the VID code is "OFF" code, ISL6364 will remain shut down.

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Soft-Start

ISL6364 based VR has 4 periods during soft-start, as shown in Figure 16. After VCC, EN_VTT and EN_PWR reach their POR/enable thresholds, the controller will have a fixed delay period t_{D1}. After this delay period, the VR will begin first soft-start ramp until the output voltage reaches V_{BOOT} voltage at a fixed slew rate, quarter of setVID FAST rate as in Table 6. Then, the controller will regulate the VR voltage at V_{BOOT} for another period t_{D3} until SVID sends a new VID command. If the VID code is valid, ISL6364 will initiate the second soft-start ramp at a slew rate, set by setVID FAST or SLOW command in Table 6, until the voltage reaches the new VID voltage.

The soft-start time is the sum of the 4 periods, as shown in Equation 16.

$$t_{SS} = t_{D1} + t_{D2} + t_{D3} + t_{D4} \qquad \text{(EQ. 16)}$$

t_{D1} is a fixed delay with the typical value as 4.6ms. t_{D3} is determined by the time to obtain a valid new VID voltage from the SVID bus. If the VID is valid before the output reaches the boot voltage, the output will turn around to respond to the new VID code.

During t_{D2} and t_{D4}, ISL6364 digitally controls the DAC voltage change at 5mV per step. The soft-start ramp time t_{D2} and t_{D4} can be calculated based on Equations 17 and 18:

$$t_{D2} = \frac{V_{BOOT}}{\text{SetVID SLOW RATE}}(\mu s) \qquad \text{(EQ. 17)}$$

$$t_{D4} = \frac{V_{VID} - V_{BOOT}}{\text{SetVID RATE}}(\mu s) \qquad \text{(EQ. 18)}$$

For example, when the V_{BOOT} is set at 1.1V and SetVID rate is set at 10mV/μs, the first soft-start ramp time t_{D2} will be around 440μs and the second soft-start ramp time t_{D4} will be at maximum of 40μs if an setVID command for 1.5V is received after t_{D3}. However, if V_{BOOT} is set at 0V, the first setVID command is for 1.5V, then t_{D2} will be around 150μs. Note that the initial 0 to 250mV DAC is typically at a slower rate to minimize the inrush current, the response time could be dictated by the compensation network and the output filter.
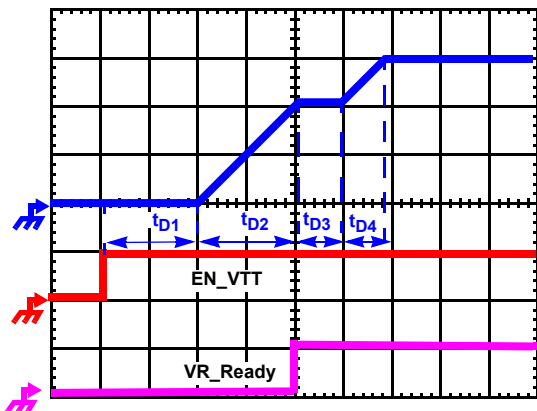
FIGURE 16. SOFT-START WAVEFORMS

Current Sense Output

The current flowing out of the IMON pin is equal to the sensed average current inside ISL6364. In typical applications, a resistor is placed from the IMON pin to GND to generate a voltage, which is proportional to the load current and the resistor value, as shown in Equation 19:

$$V_{IMON} = \frac{R_{IMON}}{N} \frac{R_X}{R_{ISEN}} I_{LOAD} \qquad \text{(EQ. 19)}$$

where V_{IMON} is the voltage at the IMON pin, R_{IMON} is the resistor between the IMON pin and GND, I_{LOAD} is the total output current of the converter, R_{ISEN} is the sense resistor connected to the ISEN+ pin, N is the active channel number, and R_X is the DC resistance of the current sense element, either the DCR of the inductor or R_{SENSE} depending on the sensing method.

The resistor from the IMON pin to GND should be chosen to ensure that the voltage at the IMON pin is typically 900mV at the maximum load current, typically corresponding to ICCMAX register. The IMON voltage is linearly digitized every 132μs and stored in the IOUT register (15h). When the IMON voltage reaches 900mV or beyond, the digitized IOUT will be FFh and the Alert pin is pulled low to alarm the CPU. If the desired maximum load current alert is not the exact ICCMAX value, the IMON resistor can be scaled accordingly to make sure that it reaches 900mV at the desired maximum output load.

$$R_{IMON} = \frac{0.9V}{R_X} R_{ISEN} \frac{N}{I_{DESIRED\_MAX}} \qquad \text{(EQ. 20)}$$

A small capacitor can be placed between the IMON pin and GND to reduce the noise impact and do the average. The typical time constant is 1ms for VR12 applications. If this pin is not used, tie it to GND.

In addition, if the IMON pin voltage is higher than 1.12V, overcurrent shutdown will be triggered, as described in "Overcurrent Protection" on page 29.

Fault Monitoring and Protection

The ISL6364 actively monitors output voltage and current to detect fault conditions. Fault monitors trigger protective measures to prevent damage to a microprocessor load. One common power-good indicator is provided for linking to external system monitors. The schematic in Figure 15 outlines the interaction between the fault monitors and the VR_RDY signal.

VR_Ready Signal

The VR_RDY pin is an open-drain logic output, which indicates that the soft-start period is complete and the output voltage is within the regulated range. VR_RDY is pulled low during shutdown and releases high after a successful soft-start. VR_RDY will be pulled low when an fault (OCP or OVP) condition is detected, or the controller is disabled by a reset from EN_PWR, EN_VTT, POR, or VID OFF-code. If the Multi_VR_config register is set to 01h, then the VR_Ready line will stay high when receiving a 00h VID code after the first soft-start. The VR_RDYS behaves the same as VR_RDY, and both are independent from each other. However, the defaulted Multi_VR_config is 00h for VR0 and 01h for VR1.

Overvoltage Protection

Regardless of the VR being enabled or not, the ISL6364 overvoltage protection (OVP) circuit will be active after its POR. The OVP thresholds are different under different operation conditions. When VR is not enabled and during the soft-start intervals t_{D1}, the

OVP threshold is 2.3V. Once the VR output voltage reaches above the DAC, fires the first PWM and completes the soft-start, the OVP trip point will change to a tacking level of DAC+179mV.

Two actions are taken by ISL6364 to protect the microprocessor load when an overvoltage condition occurs.

At the inception of an overvoltage event, all PWM outputs are commanded low instantly. This causes the Intersil drivers to turn on the lower MOSFETs and pull the output voltage below a level to avoid damaging the load. When the output voltage falls below the DAC plus 107mV, PWM signals enter a high-impedance state (or pulled to 40% of VCC). The Intersil drivers respond to the high-impedance input by turning off both upper and lower MOSFETs. If the overvoltage condition reoccurs, ISL6364 will again command the lower MOSFETs to turn on. ISL6364 will continue to protect the load in this fashion as long as the overvoltage condition occurs.

Once an overvoltage condition is detected, the respective VR# ceases the normal PWM operation and pulls its VR_Ready low until ISL6364 is reset. Cycling the voltage VCC below the POR-falling threshold will reset the controller. Cycling the EN_VTT, or EN_PWR will also reset the controller in ISL6364, but not in ISL6364A.
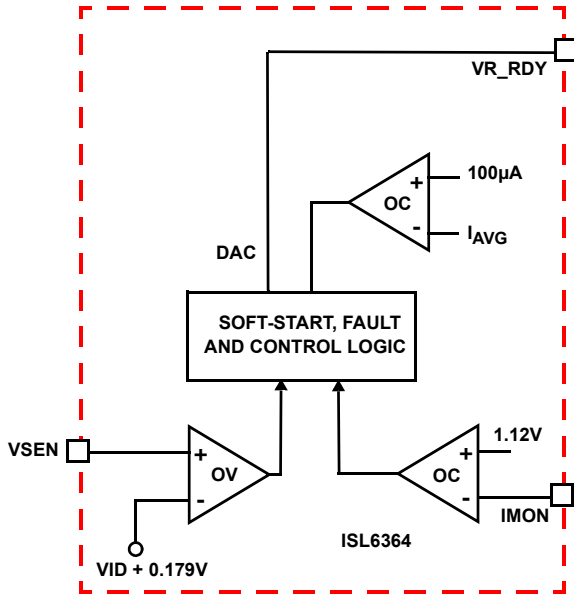
FIGURE 17. VR_RDY AND PROTECTION CIRCUITRY

Overcurrent Protection

ISL6364 has two levels of overcurrent protection. Each phase is protected from a sustained overcurrent condition by limiting its peak current, while the combined phase currents are protected on an instantaneous basis.

For the individual channel overcurrent protection, ISL6364 continuously compares the sensed peak current (~50ns filter) signal of each channel with the 140µA reference current. If one channel current exceeds the reference current, ISL6364 will pull PWM signal of this channel to low for the rest of the switching cycle. This PWM signal can be turned on next cycle if the sensed channel current is less than the 140µA reference current. The peak current limit of individual channel will only use for cycle-by-cycle current limiting and will not trigger the converter to shutdown.

In instantaneous protection mode, ISL6364 utilizes the sensed average current I_{AVG} to detect an overcurrent condition. See "Current Sensing" on page 16 for more details on how the average current is measured. The average current is continually compared with a constant 100µA reference current, as shown in Figure 17. Once the average current exceeds the reference current, a comparator triggers the converter to shutdown. In addition, the current out of the IMON pin is equal to the sensed average current I_{AVG}. With a resistor from IMON to GND, the voltage at the IMON will be proportional to the sensed average current and the resistor value. The ISL6364 continuously monitors the voltage at IMON pin. If the voltage at the IMON pin is higher than 1.12V, a precision comparator triggers the overcurrent shutdown. Since the internal current comparator has wider tolerance than the voltage comparator, the IMON voltage comparator is the preferred one for OCP trip. Hence, the resistor between IMON and GND can be scaled such that the overcurrent protection threshold is tripping lower than 100µA. For example, the overcurrent threshold for the sensed average current I_{AVG} can be set to 95µA by using a 11.8kΩ resistor from IMON to GND. Thus, the internal 100µA comparator might only be triggered at its lower corner. However, IMON OCP trip should NOT be too far away from 140µA, which is used for cycle-by-cycle protection and inductor saturation.
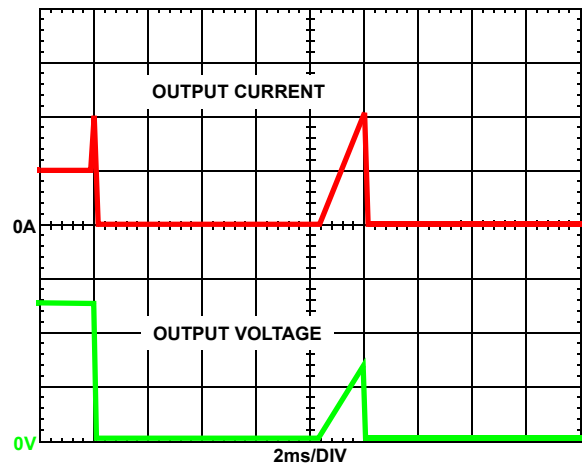
FIGURE 18. OVERCURRENT BEHAVIOR IN HICCUP MODE. F_{SW} = 500kHz

At the beginning of overcurrent shutdown, the controller places all PWM signals in a high-impedance state (or pulled to 40% of VCC), commanding the Intersil MOSFET driver ICs to turn off both upper and lower MOSFETs. The system remains in this state a period of 8ms. If the controller is still enabled at the end of this wait period, it will attempt a soft-start. If the fault remains, the trip-retry cycles will continue indefinitely (as shown in Figure 18) until either controller is disabled or the fault is cleared. Note that the energy delivered during trip-retry cycling is much less than during full-load operation, so there is no thermal hazard during this kind of operation

Thermal Monitoring (VR_HOT#)

VR_HOT# indicates the temperature status of the voltage regulator. VR_HOT# is an open-drain output, and an external pull-up resistor is required. This signal is valid only after the controller is enabled.

The VR_HOT# signal can be used to inform the system that the temperature of the voltage regulator is too high and the CPU should reduce its power consumption. The VR_HOT# signal may be tied to the CPU's PROC_HOT signal.
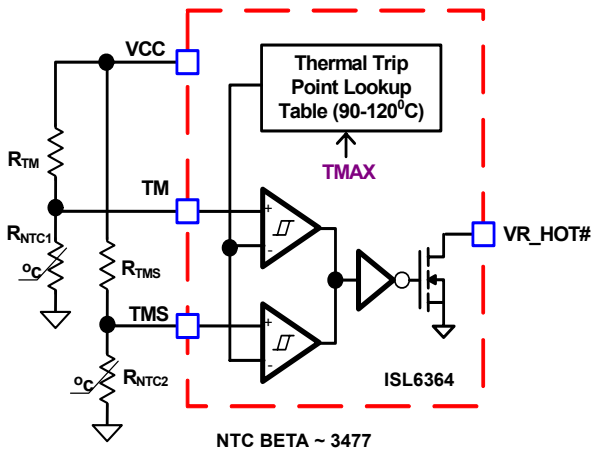
FIGURE 19. BLOCK DIAGRAM OF THERMAL MONITORING FUNCTION

The diagram of thermal monitoring function block is shown in Figure 19. One NTC resistor should be placed close to the respective power stage of the voltage regulator VR0 and VR1 to sense the operational temperature, and one pull-up resistor is needed to form the voltage divider for the TM pin. As the temperature of the power stage increases, the resistance of the NTC will reduce, resulting in the reduced voltage at the TM pin. Figure 20 shows the TM voltage over the temperature for a typical design with a recommended 6.8kΩ NTC (P/N: NTHS0805N02N6801 from Vishay, β = 3477) and 1kΩ resistor R_{TM}. It is recommended to use those resistors for the accurate temperature compensation since the internal thermal digital code is developed based upon these two components. If a different value is used, the temperature coefficient must be close to 3477 and R_{TM} must be scaled accordingly. For instance, say NTC = 10kΩ (β = 3477), then R_{TM} should be 10kΩ/6.8kΩ*1kΩ = 1.47kΩ.

There is a comparator with hysteresis to compare the TM pin voltage to the threshold set by the TMAX register for VR_HOT# signal. With TMAX set at +100°C, the VR_HOT# signal is pulled to GND when either TM or TMS voltage is lower than 39.12% of VCC voltage, and is open when both TM and TMS voltages increase to above 40.98% of VCC voltage. The comparator trip point will be programmable by TMAX values. Figure 20 shows the operation of those signals.
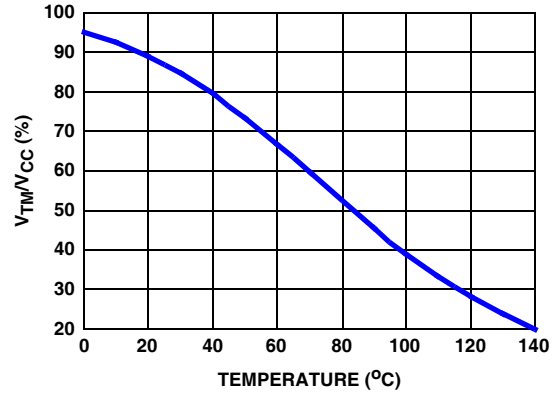
FIGURE 20. THE RATIO OF TM VOLTAGE TO NTC TEMPERATURE WITH RECOMMENDED PARTS
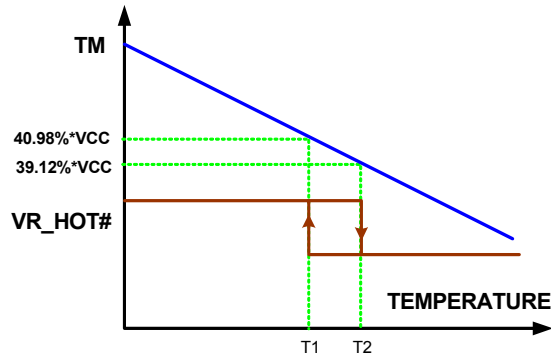
FIGURE 21. VR_HOT# SIGNAL (TMAX = +100°C) vs TM VOLTAGE

Based on the NTC temperature characteristics and the desired threshold of the VR_HOT# signal, the pull-up resistor R_{TM} of TM pin is given by Equation 21:

$$R_{TM} = 1.557 \times R_{NTC(T2)} \tag{EQ. 21}$$

$R_{NTC(T2)}$ is the NTC resistance at the VR_HOT# threshold temperature T2. The VR_HOT# is de-asserted at temperature T1, as in Table 7. Since the NTC directly senses the temperature of the PCB and not the exact temperature of the hottest component on the board due to airflow and varied thermal impedance, therefore, user should select a lower TMAX number, depending upon the mismatching between NTC and the hottest components, than such component to guarantee a safe operation.

TABLE 7. VR_HOT# TYPICAL TRIP POINT AND HYSTERESIS

TMAX (°C)	VR_HOT# LOW (°C; T2, %VCC)	VR_HOT# OPEN (°C; T1, %VCC)	HYSTERESIS (°C)
90	88.6; 45.52%	85.9; 47.56%	2.7
95	94.3; 42.26%	91.4; 44.20%	2.9
100	100.0; 39.12%	97.1; 40.98%	2.9
105	106.1; 36.14%	103.0; 37.92%	3.1
110	109.1; 33.32%	106.1; 35.00%	3.0
115	115.5; 30.68%	112.3; 32.24%	3.2
120	118.7; 28.24%	115.5; 29.7%	3.2

Temperature Compensation

The ISL6364 supports inductor DCR sensing, or resistive sensing techniques. The inductor DCR has a positive temperature coefficient, which is about +0.385%/°C. Since the voltage across the inductor is sensed for the output current information, the sensed current has the same positive temperature coefficient as the inductor DCR.

In order to obtain the correct current information, there should be a way to correct the temperature impact on the current sense component. ISL6364 provides two methods: integrated temperature compensation and external temperature compensation.

The ISL6364 utilizes the voltage at the TM pin and "TCOMP" register to compensate the temperature impact on the sensed current. The block diagram of this function is shown in Figure 22.
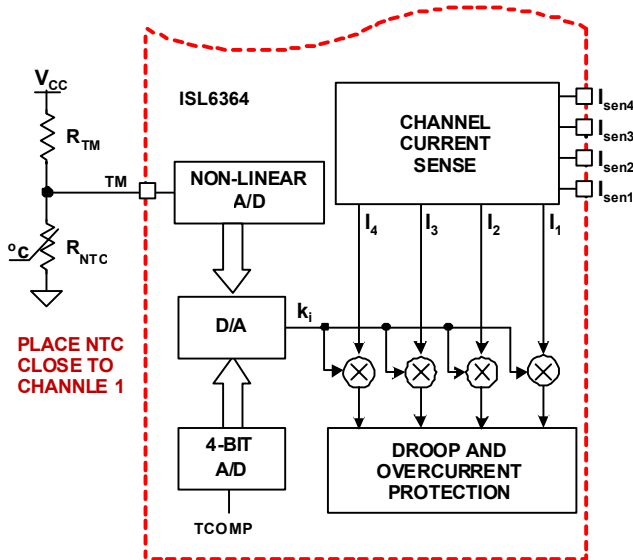
FIGURE 22. BLOCK DIAGRAM OF INTEGRATED TEMPERATURE COMPENSATION

When the NTC is placed close to the current sense component (inductor), the temperature of the NTC will track the temperature of the current sense component. Therefore, the TM voltage can be utilized to obtain the temperature of the current sense component. Since NTC could pick up noise from the phase node, a 0.1μF ceramic decoupling capacitor is recommended on the TM pin in close proximity to the controller.

Based on the VCC voltage, the ISL6364 converts the TM pin voltage to a 6-bit TM digital signal for temperature compensation. With the non-linear A/D converter of ISL6364, the TM digital signal is linearly proportional to the NTC temperature. For accurate temperature compensation, the ratio of the TM voltage to the NTC temperature of the practical design should be similar to that in Figure 20.
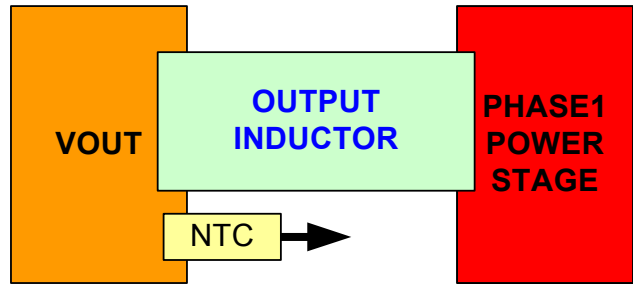
FIGURE 23. RECOMMENDED PLACEMENT OF NTC

Since the NTC attaches to the PCB, but not directly to the current sensing component, it inherits high thermal impedance between the NTC and the current sensing element. The "TCOMP" register values can be utilized to correct the temperature difference between NTC and the current sense component. As shown in Figure 23, the NTC should be placed in proximity to the PSI channel and the output rail; DON'T place it close to the MOSFET side, which generates much more heat.

ISL6364 multiplexes the "TCOMP" value with the TM digital signal to obtain the adjustment gain to compensate the temperature impact on the sensed channel current. The compensated channel current signal is used for droop and overcurrent protection functions.

TABLE 8. "TCOMP" AND "TCOMPS" VALUES

TCOMP/TCOMPS (°C)	TCOMP/TCOMPS (°C)
13	29.7
16	32.4
18.9	35.1
21.6	37.8
24.3	40.5
27	43.2
	OFF

When a different NTC type or different voltage divider is used for the TM function, the TCOMP voltage can also be used to compensate for the difference between the recommended TM voltage curve in Figure 20 and that of the actual design. If the same type NTC (β = 3477) but different value is used, the pull-up resistor needs to be scaled as shown in Equation 22:

$$R_{TM} = \frac{1k\Omega \cdot R_{NTC\_NEW}}{6.8k\Omega} \qquad \text{(EQ. 22)}$$

Design Procedure

1. Properly choose the voltage divider for the TM pin to match the TM voltage vs temperature curve with the recommended curve in Figure 20.

2. Run the actual board under the full load and the desired cooling condition.

3. After the board reaches the thermal steady state, record the temperature (T_{CSC}) of the current sense component (inductor or MOSFET) and the voltage at TM and VCC pins.

4. Use Equation 23 to calculate the resistance of the NTC, and find out the corresponding NTC temperature T_{NTC} from the NTC datasheet or using Equation 24, where β is equal to 3477 for recommended NTC.

$$R_{NTC}(T_{NTC}) = \frac{V_{TM} \times R_{TM}}{V_{CC} - V_{TM}}$$ (EQ. 23)

$$T_{NTC} = \frac{\beta}{\ln\left(\frac{RTM}{R_{NTC}(T_{NTC})}\right) + \frac{\beta}{298.15}} - 273.15$$ (EQ. 24)

5. In Intersil designed worksheet, choose a number close to the result as in Equation 25 in the "TCOMP" cell to calculate the needed resistor network for the register "TCOMP" pin. (Note: for worksheet, please contact Intersil Application support at www.intersil.com/design/).

$$T_{COMP} = T_{CSC} - T_{NTC}$$ (EQ. 25)

6. Run the actual board under full load again with the proper resistors connected to the "TCOMP" pin.

7. Record the output voltage as V1 immediately after the output voltage is stable with the full load. Record the output voltage as V2 after the VR reaches the thermal steady state.

8. If the output voltage increases over 2mV as the temperature increases, i.e. V2 - V1 > 2mV, reduce "TCOMP" value; if the output voltage decreases over 2mV as the temperature increases, i.e. V1 - V2 > 2mV, increase "TCOMP" values.

External Temperature Compensation

When the "OFF" code of TCOMP is selected, then the internal current source is not thermally compensated, i.e, the integrated temperature compensation function is disabled. However, one external temperature compensation network, shown in Figure 24, can be used to cancel the temperature impact on the droop (i.e., load line).
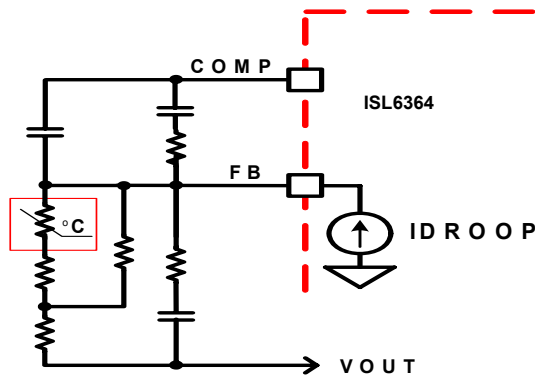
FIGURE 24. EXTERNAL TEMPERATURE COMPENSATION FOR LOAD LINE

The sensed current will flow out of the FB pin and develop a droop voltage across the resistor equivalent (R_{FB}) between the FB pin and VOUT sensing node. If R_{FB} resistance reduces as the temperature increases, the temperature impact on the droop can be compensated. An NTC resistor can be placed close to the power stage and used to form R_{FB}. Due to the nonlinear temperature characteristics of the NTC, a resistor network is needed to make

the equivalent resistance between the FB pin and VOUT sensing node inversely proportional to the temperature.

This external temperature compensation network can only compensate the temperature impact on the droop, while it has no impact to the sensed current inside ISL6364. Therefore, this network cannot compensate for the temperature impact on the overcurrent protection function. In addition, NTC could pick up phase switching noise and easily inject into the loop. This method is typically not recommended.
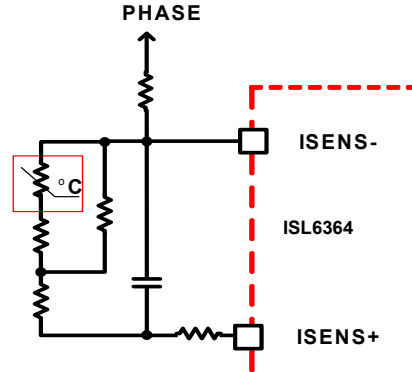
FIGURE 25. NTC WITH L/DCR MATCHING NETWORK FOR THERMAL COMPESNATION

Furthermore, the NTC can be placed with L/DCR matching network to thermally compensate the sensed current, or with IMON network to thermally compensate the IMON voltage (typically need to set internal overcurrent trip higher than IMON OCP trip), as shown in Figures 25 and 26, respectively. These methods are typically applicable to both VR0 and VR1 for non-droop applications.
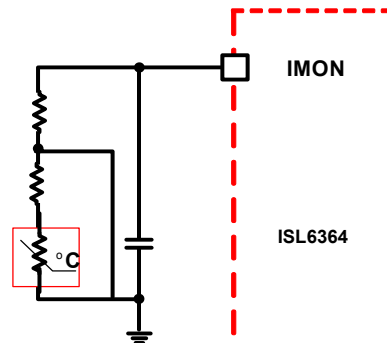
FIGURE 26. NTC WITH IMON NETWORK FOR THERMAL COMPESNATION

Hard-wired Registers (Patent Pending)

To set registers for VR12/IMVP7 applications using lowest pin-count package and with lowest overall cost, Intersil has developed a high resolution ADC using a patented technique with simple 1%, 100ppm/k or better temperature coefficient resistor divider, as shown in Figure 27. The same type of resistors are preferred so that it has similar change over temperature. In addition, the divider is comparing to the internal divider off VCC and GND nodes and therefore must refer to VCC and GND pins, not through any RC decoupling network.
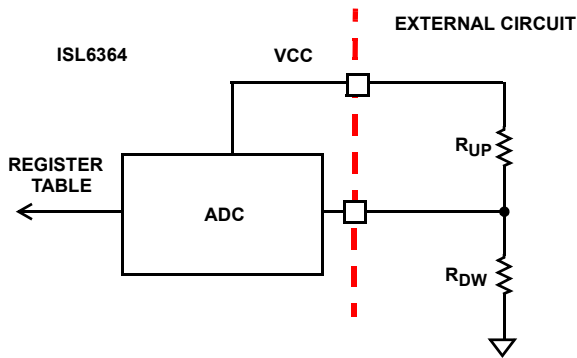
FIGURE 27. SIMPLIFIED RESISTOR DIVIDER ADC

There are total of four register pins to program the system parameters: Address OFFSET, setVID fast slew rate, boot voltage, ICCMAX, diode emulation option, number of phase operation at low power mode, and temperature compensation, as summarized in Table 9. Prior to the soft-start, the system parameters are stored in the SVID data registers of 0C, 0D, 0E, and 0F, respectively, as shown in Table 10. They are reset by Enable or VCC POR. In addition, data is available to verify that the system setting is over a high volume production. A design worksheet to select these pairs of resistors is available for use. Please contact Intersil Application support at www.intersil.com/design/.

As an example, Table 11 shows the R_{UP} and R_{DW} values of each pin for a specific system design; DATA for corresponding registers can be read out via SVID's Get(reg) command. In addition, as shown in Table 12, some tie-high and tie-low options are for easy programming and can also be used to validate the VR operation during In-Circuit Test (ICT). For instance, when the system boot voltage is required at zero Volts, the BT_XX or BTS_XX pin can be tied to GND or VCC, prior to Enable, to get a known boot voltage to check VR operation with ICT.

TABLE 9. SYSTEM PARAMETER DESCRIPTION

CODE NAME	DESCRIPTION	RANGE
ADDR	VR0/1 Address offset (VR0 and VR1 Are In Operation)	0/1, 2/3 to 6/7
	VR0 Address offset (PWMS = VCC, FSS_DRPS = 1 MΩ to GND)	0, 2, 4, 6
	VR0 Address offset (PWMS = VCC, FSS_DRPS = 1 MΩ to VCC)	8,A,C
	VR1 Address offset (PWM1 = VCC)	1, 3, 5, 7
BT	VR0 Boot Voltages (R_FS_DRP TIED GND)	0, 0.9, 1.0, 1.1V
	VR0 Boot Voltages (R_FS_DRP TIED VCC)	0,1.2, 1.35, 1.5V
BTS	VR1 Boot Voltages (R_FSS_DRPS TIED GND)	0, 0.9, 1.0, 1.1V
	VR1 Boot Voltages (R_FSS_DRPS TIED VCC)	0, 0.85, 0.925, 1.05V
FDVID	setVID Fast Slew Rate for VR0	10mV/µs, 20mV/µs

TABLE 9. SYSTEM PARAMETER DESCRIPTION (Continued)

CODE NAME	DESCRIPTION	RANGE
DE	Diode Emulation Option of VR0	Enable, or Disable
DES	Diode Emulation Option of VR1	Enable, or Disable
TMAX	Maximum Operating Temperature	+90°C to +120°C (+5°C/Step)
IMAX	Iccmax of VR0	15-165A (5/step)
IMAXS	Iccmax of VR1 (R_FSS_DRPS TIED GND)	20A, 25A, 30A, 35A
	Iccmax of VR1 (R_FSS_DRPS TIED VCC)	15A, 20A, 25A, 30A
NPSI	Number of Operational Phases in PSI1/2/3/Decay States	1 or 2-Phase
TCOMP	Mismatching Temperature Compensation between sensing element and NTC for VR0	OFF, +13°C to +43.2°C
TCOMPS	Mismatching Temperature Compensation between sensing element and NTC for VR1	OFF, +13°C to +43.2°C

TABLE 10. SYSTEM DATA REGISTER LOCATION

REGISTER PIN NAME	DATA REGISTER CODE
ADDR_IMAXS_TMAX	0C
BTS_DES_TCOMPS	0D
BT_FDVID_TCOMP	0E
NPSI_DE_IMAX	0F

TABLE 11. DESIGN EXAMPLE

REG				R_{UP}	R_{DW}	DATA
0C	ADDR	IMAXS	TMAX			
	0/1	25A	100°C	29.4kΩ	15kΩ	08h
0D	BTS	DES	TCOMPS			
	0.85V	ENABLED	29.7°C	255kΩ	140kΩ	C0h
0E	BT	FDVID	TCOMP			
	1.1V	20mV/µs	29.7°C	10kΩ	OPEN	DFh
0F	NPSI	DE	IMAX			
	SI1	ENABLED	100A	OPEN	10kΩ	00h

TABLE 12. TIE-HIGH AND TIE-LOW OPTIONS

REG				R_{UP}	R_{DW}	DATA
0C	ADDR	IMAXS (R_FSS_DRPS: GND/VCC)	TMAX			
	0/1	35A/30A	100°C	10kΩ	OPEN	0h
	0/1	20A/15A	95°C	OPEN	10kΩ	1Fh
	6/7	35A/30A	100°C	499kΩ	OPEN	C0h

TABLE 12. TIE-HIGH AND TIE-LOW OPTIONS (Continued)

REG				R$_{UP}$	R$_{DW}$	DATA
0C	ADDR	IMAXS (R$_{FSS\_DRPS}$: GND/VCC)	TMAX			
	6/7	20A/15A	95°C	OPEN	499kΩ	DFh
0D	BTS (R$_{FSS\_DRPS}$: GND/VCC)	DES	TCOMPS			
	1.1V/1.5V	DISABLED	+29.7°C	OPEN	10kΩ	00h
	1.1V/1.5V	ENABLED	+29.7°C	10kΩ	OPEN	1Fh
	0	DISABLED	+29.7°C	OPEN	499kΩ	C0h
	0	ENABLED	+29.7°C	499kΩ	OPEN	DFh
0E	BT (R$_{FS\_DRP}$: GND/VCC)	FDVID	TCOMP			
	1.1V/1.05V	10mV/µs	+29.7°C	OPEN	10kΩ	00h
	1.1V/1.05V	20mV/µs	+29.7°C	10kΩ	OPEN	1Fh
	0	10mV/µs	+29.7°C	OPEN	499kΩ	C0h
	0	20mV/µs	+29.7°C	499kΩ	OPEN	DFh
0F	NPSI	DE	IMAX			
	SI1/CI1	ENABLED	100A	OPEN	10kΩ	00h
	SI1/CI1	ENABLED	165A	10kΩ	OPEN	1Fh
	SI2/CI2	DISABLED	100A	OPEN	499kΩ	C0h
	SI2/CI2	DISABLED	165A	499kΩ	OPEN	DFh

NOTE: Whenever 10kΩ is tie-high or tie-low, 0Ω can be used.

Dynamic VID Compensation (DVC)

During a VID transition, the resulting change in voltage on the FBS pin and the COMPS pin causes an AC current to flow through the error amplifier compensation components from the FBS to the COMPS pin. This current then flows through the feedback resistor, R$_{FBS}$, and can cause the output voltage to overshoot or undershoot at the end of the VID transition. In order to ensure the smooth transition of the output voltage during a VID change, a VID-on-the-fly compensation network is required. This network is composed of a resistor and capacitor in series, R$_{DVC}$ and C$_{DVC}$, between the DVCS and the FBS pin.

This VID-on-the-fly compensation network works by sourcing AC current into the FBS node to offset the effects of the AC current flowing from the FBS to the COMPS pin during a VID transition. To create this compensation current, the controllers set the voltage on the DVCS pin to be 4/3 of the voltage on the DAC. Since the error amplifier forces the voltage on the FBS pin and the DAC to be equal, the resulting voltage across the series RC between DVCS and FBS is equal to the DAC voltage. The RC compensation components, R$_{DVC}$ and C$_{DVC}$, can then be selected to create the desired amount of compensation current.
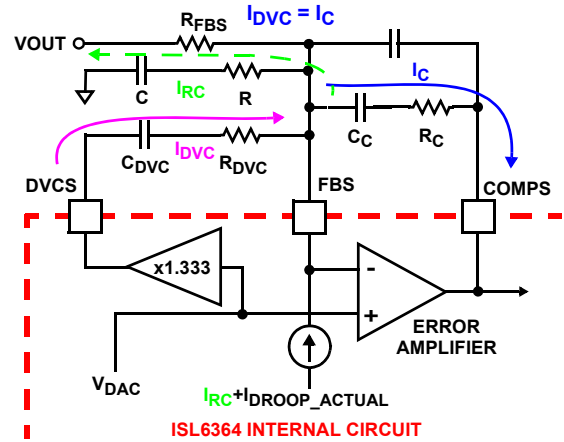
FIGURE 28. DYNAMIC VID COMPENSATION NETWORK

The amount of compensation current required is dependant on the modulator gain of the system, K1, and the error amplifier R-C components, R$_C$ and C$_C$, that are in series between the FBS and COMPS pins. Use Equations 26, 27, and 28 to calculate the RC component values, R$_{DVC}$ and C$_{DVC}$, for the VID-on-the-fly compensation network. For these equations: V$_{IN}$ is the input voltage for the power train; V$_{RAMP}$ is the oscillator ramp amplitude as in Equation 3; and R$_C$ and C$_C$ are the error amplifier R-C components between the FBS and COMPS pins.

$$K1 = \frac{V_{IN}}{V_{RAMP}} \tag{EQ. 26}$$

$$R_{DVC} = A \cdot R_C \qquad A = \frac{K1}{3 \cdot (K1-1)} \tag{EQ. 27}$$

$$C_{DVC} = \frac{C_C}{A} \tag{EQ. 28}$$

During DVID transitions, extra current builds up in the output capacitors due to the C*dv/dt. The current is sensed by the controller and fed across the feedback resistor creating extra droop (if Enabled) and causing the output voltage not properly tracking the DAC voltage. Placing a series R-C to ground from the FB pin can sink this extra DVID induced current.

$$C = \frac{C_{OUT} \cdot R_{LL}}{R_{FBS}} \tag{EQ. 29}$$

$$R = \frac{C_{OUT} \cdot R_{LL}}{C} = R_{FBS} \tag{EQ. 30}$$

When the output voltage overshoots during DVID, the RDVC-CDVC network can be used to compensate the movement of the error-amplifier compensation network. When the output voltage is lagging from DAC (or SVALERT#) or having a rough-off prior to the final settling of DVID, the R-C network can be used to compensate for the extra droop current generated by the C*dv/dt. Sometimes, both networks can work together to achieve the best result. In such case, both networks need to be fine tuned in the board level for optimized performance.

Only VR1 is available for DVC compensation when the droop is disabled, while the R-C network to compensate the lagging of VOUT from DAC is applicable for both VR1 and VR0 when needed.

Disabling Output

When disabling any output, its respective pins should be tied accordingly as in Table 13. However, when both outputs are fully populated, pulling the respective PWM line to VCC should be sufficient.

TABLE 13. DISABLE OUTPUT CONFIGURATION

DISABLE VR1 OUTPUT	
PIN NAME	**PIN CONFIGURATION**
PWMS	VCC
RNGDS; VSENS; FBS; IMONS; ISENS-; VR_RDYS	GND
HFCOMPS/DVCS; ISENS+	OPEN
FSS_DRPS	1MΩto GND (for 0,2,4,6 ADDR) or 1MΩ to VCC for 8,A,C ADDR)
TMS	Connect To TM pin or a 1/2 ratio Resistor Divider (1MΩ/2MΩ) to avoid tripping VR_HOT#; or Use it as a second thermal sensing for VR_HOT#. DON'T tie it to VCC or GND.
DISABLE VR0 OUTPUT	
PIN NAME	**PIN CONFIGURATION**
PWM1	VCC
RNGD; VSEN; FB; IMON; ISEN[1:4]-; VR_RDY	GND
HFCOMP; ISEN[1:6]+	OPEN
FS_DRP, RSET	1MΩ to GND
TM	Connect To TMS pin or a 1/2 ratio Resistor Divider (1MΩ/2MΩ) to avoid tripping VR_HOT#; or Use it as a second thermal sensing for VR_HOT#. DON'T tie it to VCC or GND.

SVID Operation

The device is fully compliant with Intel VR12/IMVP7 SVID protocol Rev 1.5, document# of 456098. To ensure proper CPU operation, refer to this document for SVID bus design and layout guidelines; each platform requires different pull-up impedance on the SVID bus, while impedance matching and spacing among DATA, CLK, and ALERT# signals must be followed. Common mistakes are insufficient spacing among signals and improper pull-up impedance. A simple operational instruction of SVID bus with Intel VTT Tool is documented in **"VR12 Design and Validation"** in Table 15.

General Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a multiphase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following. In addition to this guide, Intersil provides complete reference designs, which include schematics, bills of materials, and example board layouts for common microprocessor applications.

Power Stages

The first step in designing a multiphase converter is to determine the number of phases. This determination depends heavily upon the cost analysis, which in turn depends on system constraints that differ from one design to the next. Principally, the designer will be concerned with whether components can be mounted on both sides of the circuit board; whether through-hole components are permitted; and the total board space available for power supply circuitry. Generally speaking, the most economical solutions are those in which each phase handles between 15A and 25A. All surface-mount designs will tend toward the lower end of this current range. If through-hole MOSFETs and inductors can be used, higher per-phase currents are possible. In cases where board space is the limiting constraint, current can be pushed as high as 40A per phase, but these designs require heat sinks and forced air to cool the MOSFETs, inductors and heat-dissipating surfaces.

MOSFETs

The choice of MOSFETs depends on the current each MOSFET will be required to conduct; the switching frequency; the capability of the MOSFETs to dissipate heat; and the availability and nature of heat sinking and air flow.

Lower MOSFET Power Calculation

The calculation for heat dissipated in the lower MOSFET is simple, since virtually all of the heat loss in the lower MOSFET is due to current conducted through the channel resistance ($r_{DS(ON)}$). In Equation 31, I_M is the maximum continuous output current; I_{PP} is the peak-to-peak inductor current (see Equation 1 on page 14); d is the duty cycle (V_{OUT}/V_{IN}); and L is the per-channel inductance.

$$P_{LOW,1} = r_{DS(ON)} \left[\left(\frac{I_M}{N} \right)^2 + \frac{I_{PP}^2}{12} \right] \cdot (1-d) \qquad \text{(EQ. 31)}$$

An additional term can be added to the lower-MOSFET loss equation to account for additional loss accrued during the dead time when inductor current is flowing through the lower-MOSFET body diode. This term is dependent on the diode forward voltage at I_M, $V_{D(ON)}$; the switching frequency, F_{SW}; and the length of dead times, t_{d1} and t_{d2}, at the beginning and the end of the lower-MOSFET conduction interval respectively.

$$P_{LOW,2} = V_{D(ON)}F_{SW} \left[\left(\frac{I_M}{N} + \frac{I_{PP}}{2} \right) t_{d1} + \left(\frac{I_M}{N} - \frac{I_{PP}}{2} \right) t_{d2} \right] \qquad \text{(EQ. 32)}$$

Finally, the power loss of output capacitance of the lower MOSFET is approximated in Equation 33:

$$P_{LOW,3} \approx \frac{2}{3} \cdot V_{IN}^{1.5} \cdot C_{OSS\_LOW} \cdot \sqrt{V_{DS\_LOW}} \cdot F_{SW} \qquad \text{(EQ. 33)}$$

where C_{OSS_LOW} is the output capacitance of the lower MOSFET at the test voltage of V_{DS_LOW}. Depending on the amount of ringing, the actual power dissipation will be slightly higher than this.

Thus the total maximum power dissipated in each lower MOSFET is approximated by the summation of $P_{LOW,1}$, $P_{LOW,2}$ and $P_{LOW,3}$.

Upper MOSFET Power Calculation

In addition to $r_{DS(ON)}$ losses, a large portion of the upper-MOSFET losses are due to currents conducted across the input voltage (V_{IN}) during switching. Since a substantially higher portion of the

upper-MOSFET losses are dependent on switching frequency, the power calculation is more complex. Upper MOSFET losses can be divided into separate components involving the upper-MOSFET switching times; the lower-MOSFET body-diode reverse-recovery charge, Q_{rr}; and the upper MOSFET $r_{DS(ON)}$ conduction loss.

When the upper MOSFET turns off, the lower MOSFET does not conduct any portion of the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting, the current in the upper MOSFET falls to zero as the current in the lower MOSFET ramps up to assume the full inductor current. In Equation 34, the required time for this commutation is t_1 and the approximated associated power loss is $P_{UP,1}$.

$$P_{UP,1} \approx V_{IN}\left(\frac{I_M}{N} + \frac{I_{PP}}{2}\right)\left(\frac{t_1}{2}\right)F_{SW} \qquad \text{(EQ. 34)}$$

At turn on, the upper MOSFET begins to conduct and this transition occurs over a time t_2. In Equation 35, the approximate power loss is $P_{UP,2}$.

$$P_{UP,2} \approx V_{IN}\left(\frac{I_M}{N} - \frac{I_{PP}}{2}\right)\left(\frac{t_2}{2}\right)F_{SW} \qquad \text{(EQ. 35)}$$

A third component involves the lower MOSFET's reverse-recovery charge, Q_{rr}. Since the inductor current has fully commutated to the upper MOSFET before the lower-MOSFET's body diode can draw all of Q_{rr}, it is conducted through the upper MOSFET across VIN. The power dissipated as a result is $P_{UP,3}$ and is approximated in Equation 36:

$$P_{UP,3} = V_{IN}Q_{rr}F_{SW} \qquad \text{(EQ. 36)}$$

The resistive part of the upper MOSFET's is given in Equation 37 as $P_{UP,4}$.

$$P_{UP,4} \approx r_{DS(ON)}\left[\left(\frac{I_M}{N}\right)^2 + \frac{I_{PP}^2}{12}\right] \cdot d \qquad \text{(EQ. 37)}$$

Equation 38 accounts for some power loss due to the drain-source parasitic inductance (L_{DS}, including PCB parasitic inductance) of the upper MOSFETs, although it is not the exact:

$$P_{UP,5} \approx L_{DS}\left(\frac{I_M}{N} + \frac{I_{PP}}{2}\right)^2 \qquad \text{(EQ. 38)}$$

Finally, the power loss of output capacitance of the upper MOSFET is approximated in Equation 39:

$$P_{UP,6} \approx \frac{2}{3} \cdot V_{IN}^{1.5} \cdot C_{OSS\_UP} \cdot \sqrt{V_{DS\_UP}} \cdot F_{SW} \qquad \text{(EQ. 39)}$$

where C_{OSS_UP} is the output capacitance of lower MOSFET at test voltage of V_{DS_UP}. Depending on the amount of ringing, the actual power dissipation will be slightly higher than this.

The total power dissipated by the upper MOSFET at full load can now be approximated as the summation of the results from Equations 34 to 39. Since the power equations depend on MOSFET parameters, choosing the correct MOSFETs can be an iterative process involving repetitive solutions to the loss equations for different MOSFETs and different switching frequencies.

Current Sensing Resistor

The resistors connected to the ISEN+ pins determine the gains in the load-line regulation loop and the channel-current balance loop as well as setting the overcurrent trip point. Select values for these resistors by using Equation 40:

$$R_{ISEN} = \frac{R_X}{100 \times 10^{-6}}\frac{I_{OCP}}{N} \qquad \text{(EQ. 40)}$$

where R_{ISEN} is the sense resistor connected to the ISEN+ pin, N is the active channel number, R_X is the resistance of the current sense element, either the DCR of the inductor or R_{SENSE} depending on the sensing method, and I_{OCP} is the desired overcurrent trip point. Typically, I_{OCP} can be chosen to be 1.2 times the maximum load current of the specific application.

With integrated temperature compensation, the sensed current signal is independent of the operational temperature of the power stage, i.e. the temperature effect on the current sense element R_X is cancelled by the integrated temperature compensation function. R_X in Equation 40 should be the resistance of the current sense element at the room temperature.

When the integrated temperature compensation function is disabled by selecting "OFF" TCOMP code, the sensed current will be dependent on the operational temperature of the power stage, since the DC resistance of the current sense element may be changed according to the operational temperature. R_X in Equation 40 should be the maximum DC resistance of the current sense element at the all operational temperature.

In certain circumstances, especially for a design with an unsymmetrical layout, it may be necessary to adjust the value of one or more ISEN resistors for VR0. When the components of one or more channels are inhibited from effectively dissipating their heat so that the affected channels run cooler than the average, choose new, larger values of R_{ISEN} for the affected phases (see the section entitled "Current Sensing" on page 16). Choose $R_{ISEN,2}$ in proportion to the desired increase in temperature rise in order to cause proportionally more current to flow in the cooler phase, as shown in Equation 41:

$$R_{ISEN,2} = R_{ISEN}\frac{\Delta T_2}{\Delta T_1}$$
$$\Delta R_{ISEN} = R_{ISEN,2} - R_{ISEN} \qquad \text{(EQ. 41)}$$

In Equation 41, make sure that ΔT_2 is the desired temperature rise above the ambient temperature, and ΔT_1 is the measured temperature rise above the ambient temperature. Since all channels' R_{ISEN} are integrated and set by one RSET, a resistor (ΔR_{ISEN}) should be in series with the cooler channel's ISEN+ pin to raise this phase current. While a single adjustment according to Equation 41 is usually sufficient, it may occasionally be necessary to adjust R_{ISEN} two or more times to achieve optimal thermal balance between all channels.

Load-Line Regulation Resistor

The load-line regulation resistor is labelled R_{FB} in Figure 14. Its value depends on the desired loadline requirement of the application.

The desired loadline can be calculated using Equation 42:

$$R_{LL} = \frac{V_{DROOP}}{I_{FL}}$$
(EQ. 42)

where I_{FL} is the full load current of the specific application, and VR_{DROOP} is the desired voltage droop under the full load condition.

Based on the desired loadline R_{LL}, the loadline regulation resistor can be calculated using Equation 43:

$$R_{FB} = \frac{N \cdot R_{ISEN} \cdot R_{LL}}{R_X}$$
(EQ. 43)

where N is the active channel number, R_{ISEN} is the sense resistor connected to the ISEN+ pin, and R_X is the resistance of the current sense element, either the DCR of the inductor or R_{SEN} depending on the sensing method.

If one or more of the current sense resistors are adjusted for thermal balance (as in Equation 41), the load-line regulation resistor should be selected based on the average value of the current sensing resistors, as given in Equation 44:

$$R_{FB} = \frac{R_{LL}}{R_X} \sum_n R_{ISEN(n)}$$
(EQ. 44)

where $R_{ISEN(n)}$ is the current sensing resistor connected to the nth ISEN+ pin.

Output Filter Design

The output inductors and the output capacitor bank together to form a low-pass filter responsible for smoothing the pulsating voltage at the phase nodes. The output filter also must provide the transient energy until the regulator can respond. Because it has a low bandwidth compared to the switching frequency, the output filter necessarily limits the system transient response. The output capacitor must supply or sink load current while the current in the output inductors increases or decreases to meet the demand.

In high-speed converters, the output capacitor bank is usually the most costly (and often the largest) part of the circuit. Output filter design begins with minimizing the cost of this part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, ΔI; the load-current slew rate, di/dt; and the maximum allowable output-voltage deviation under transient loading, ΔV_{MAX}. Capacitors are characterized according to their capacitance, ESR, and ESL (equivalent series inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output-voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount, as shown in Equation 45:

$$\Delta V \approx (ESL)\frac{di}{dt} + (ESR)\Delta I$$
(EQ. 45)

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

Most capacitor solutions rely on a mixture of high-frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but limited high-frequency performance. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

The ESR of the bulk capacitors also creates the majority of the output-voltage ripple. As the bulk capacitors sink and source the inductor AC ripple current (see "Interleaving" on page 13 and Equation 2), a voltage develops across the bulk-capacitor ESR equal to $I_{C,PP}$ (ESR). Thus, once the output capacitors are selected, the maximum allowable ripple voltage, $V_{PP(MAX)}$, determines the lower limit on the inductance, as shown in Equation 46.

$$L \geq ESR \cdot \frac{V_{OUT} \cdot K_{RCM}}{F_{SW} \cdot V_{IN} \cdot V_{PP(MAX)}}$$
(EQ. 46)

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

Equation 47 gives the upper limit on L for the cases when the trailing edge of the current transient causes a greater output-voltage deviation than the leading edge. Equation 48 addresses the leading edge. Normally, the trailing edge dictates the selection of L because duty cycles are usually less than 50%. Nevertheless, both inequalities should be evaluated, and L should be selected based on the lower of the two results. In each equation, L is the per-channel inductance, C is the total output capacitance, and N is the number of active channels.

$$L \leq \frac{2 \cdot N \cdot C \cdot V_{OUT}}{(\Delta I)^2}\left[\Delta V_{MAX} - \Delta I \cdot ESR\right]$$
(EQ. 47)

$$L \leq \frac{1.25 \cdot N \cdot C}{(\Delta I)^2}\left[\Delta V_{MAX} - \Delta I \cdot ESR\right]\left(V_{IN} - V_{OUT}\right)$$
(EQ. 48)

Switching Frequency Selection

There are a number of variables to consider when choosing the switching frequency, as there are considerable effects on the upper-MOSFET loss calculation. These effects are outlined in "MOSFETs" on page 35, and they establish the upper limit for the switching frequency. The lower limit is established by the requirement for fast transient response and small output-voltage ripple as outlined in "Output Filter Design" on page 37. Choose the lowest switching frequency that allows the regulator to meet the transient-response and output-voltage ripple requirements. To minimize the effect of cross coupling between regulators, select operating frequencies of VR0 and VR1 at least 50kHz apart.

Input Capacitor Selection

The input capacitors are responsible for sourcing the AC component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the AC component of the current drawn by the upper MOSFETs which is related to duty cycle and the number of active phases. The input RMS current can be calculated with Equation 49.

$$I_{IN, RMS} = \sqrt{K_{IN, CM}^2 \bullet Io^2 + K_{RAMP, CM}^2 \bullet I_{Lo, PP}^2} \qquad \text{(EQ. 49)}$$

$$K_{IN, CM} = \sqrt{\frac{(N \bullet D - m + 1) \bullet (m - N \bullet D)}{N^2}} \qquad \text{(EQ. 50)}$$

$$K_{RAMP, CM} = \sqrt{\frac{m^2(N \bullet D - m + 1)^3 + (m - 1)^2(m - N \bullet D)^3}{12N^2D^2}}$$
$$\text{(EQ. 51)}$$
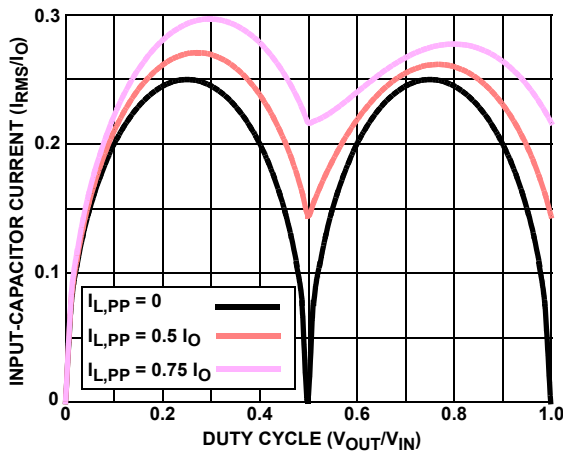
FIGURE 29. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 2-PHASE CONVERTER

FIGURE 30. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 3-PHASE CONVERTER
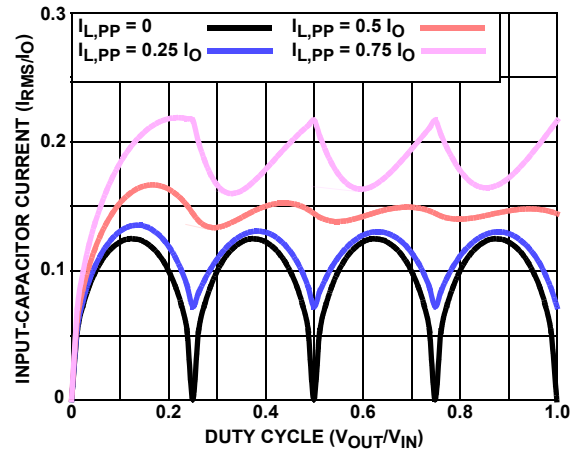
FIGURE 31. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 4-PHASE CONVERTER

For a 2-phase design, use Figure 29 to determine the input capacitor RMS current requirement given the duty cycle, maximum sustained output current (I_O), and the ratio of the per-phase peak-to-peak inductor current ($I_{L,PP}$) to I_O. Select a bulk capacitor with a ripple current rating which will minimize the total number of input capacitors required to support the RMS current calculated. The voltage rating of the capacitors should also be at least 1.25 times greater than the maximum input voltage.

Figures 27 and 28 provide the same input RMS current information for 3 and 4-phase designs respectively. Use the same approach to selecting the bulk capacitor type and number as previously described.

Low capacitance, high-frequency ceramic capacitors are needed in addition to the bulk capacitors to suppress leading and falling edge voltage spikes. The result from the high current slew rates produced by the upper MOSFETs turn on and off. Select low ESL ceramic capacitors and place one as close as possible to each upper MOSFET drain to minimize board parasitic impedances and maximize noise suppression.
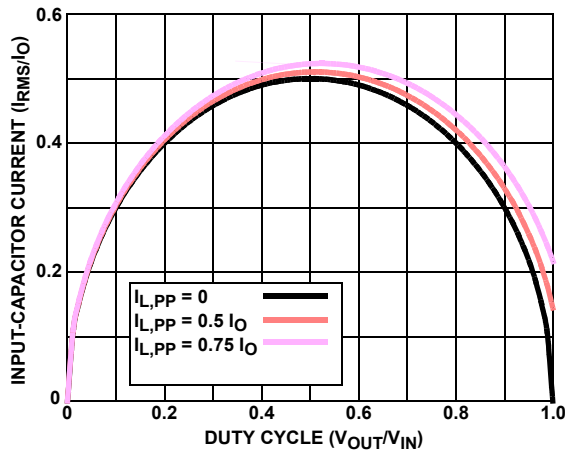
FIGURE 32. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR SINGLE-PHASE CONVERTER

MULTIPHASE RMS IMPROVEMENT

Figure 32 is provided as a reference to demonstrate the dramatic reductions in input-capacitor RMS current upon the implementation of the multiphase topology. For example, compare the input RMS current requirements of a 2-phase converter versus that of a single phase. Assume both converters have a duty cycle of 0.25, maximum sustained output current of 40A, and a ratio of $I_{L,PP}$ to I_O of 0.5. The single phase converter would require 17.3A_{RMS} current capacity while the 2-phase converter would only require 10.9A_{RMS}. The advantages become even more pronounced when output current is increased and additional phases are added to keep the component cost down relative to the single phase approach.

Layout and Design Considerations

The following layout and design strategies are intended to minimize the noise coupling, the impact of board parasitic impedances on converter performance and to optimize the heat-dissipating capabilities of the printed-circuit board. These sections highlight some important practices which should follow during the layout process. A layout check list in excel format is available for use.

Pin Noise Sensitivity, Design and Layout Consideration

Table 14 below shows the noise sensitivity of each pin and their design and layout consideration. All pins and external components should not be across switching nodes and placed in general proximity to the controller.

TABLE 14. PIN DESIGN AND/OR LAYOUT CONSIDERATION

PIN NAME	NOISE SENSITIVITY	DESCRIPTION
EN_PWR	No	There is an internal 1µs filter. Decoupling capacitor is NOT needed, but if needed, use a low time constant one to avoid too much of shut-down delay. It will also be the output of OVP function in ISL6364A: 34Ω strong pull-up. 25 mils spacing from other traces.

TABLE 14. PIN DESIGN AND/OR LAYOUT CONSIDERATION (Continued)

PIN NAME	NOISE SENSITIVITY	DESCRIPTION
RAMP_ADJ	Yes	NO decoupling capacitor allowed on this pin, but decoupling its resistor pull-up RAIL with a high quality ceramic capacitor (0.1µF or higher) or with very small RC filter (<2.2µs).
RGND	Yes	Pairing up with the positive rail remote sensing line that connected to FB resistor, and routing them to the load sensing points.
VSEN	No	Used for Overvoltage protection sensing only, and it has 1µs internal filter. Decoupling is NOT needed. Add a ZERO Ohm series impedance to be compatible with ISL6364A.
FB	Yes	Pairing up with the negative rail of remote sensing line that connected to RGND, and routing them to the load sensing points. Reserve an RC from FB to GND to compensate the output lagging from DAC during DVID transitions.
HFCOMP	Yes	Connect an R to the VR0 output. The R value is typically equal or slightly higher than the feedback resistor (droop resistor), fine tuned according to the high frequency transient performance. Placing the compensation network in close proximity to the controller.
PSICOMP	Yes	The series impedance typically should be 2x-3x the impedance in type III compensation to reduce noise coupling. Placing the compensation network in close proximity to the controller.
COMP	Yes	Placing the compensation network in close proximity to the controller. Typically use a 68pF or higher across FB to COMP depending upon the noise coupling of the layout.
IMON	Yes	Referring to GND, not RGND. Place R and C in general proximity to the controller. The time constant of RC should be sufficient, typically 1ms, as an average function for the digital IOUT of VR0.
SVDATA; SVCLK	Yes	13 to 26MHz signals when the SVID bus is sending commands, pairing up with SVALERT# and routing carefully back to CPU socket. 20 mils spacing within SVDATA, SVALERT#, and SVCLK; and more than 30 mils to all other signals. Refer to the Intel individual platform design guidelines and place proper terminated (pull-up) resistance for impedance matching. Local decoupling capacitor is needed for the pull-up rail.
SVALERT#	No	Open drain and high dv/dt pin during transitions. Routing it in the middle of SVDATA and SVCLK. Also see above.

TABLE 14. PIN DESIGN AND/OR LAYOUT CONSIDERATION (Continued)

PIN NAME	NOISE SENSITIVITY	DESCRIPTION
VR_RDY	No	Open drain and high dv/dt pin. Avoid its pull-up higher than VCC. Tie it to ground when not used.
IMONS	Yes	Referring to GND, not RGNDS. Place R and C in general proximity to the controller. The time constant of RC should be sufficient, typically 1ms, as an average function for the digital IOUT of VR1.
VR_HOT#	No	Open drain and high dv/dt pin during transitions. Avoid its pull-up rail higher than VCC. 30 mils spacing from other traces.
HFCOMPS/DVCS	Yes	Connect an R in similar value (equal or slight higher) of the feedback resistor. If programmed to be used as DVCS, Connect an RC to FBS from this pin. Placing the compensation network in close proximity to the controller.
VR_RDYS	No	Open drain and high dv/dt pin. Avoid its pull-up higher than VCC. Tie it to GND when not used.
COMPS	Yes	Placing the compensation network in close proximity to the controller. Typically use a 68pF or higher across FBS to COMPS depending upon the noise coupling of the layout.
FBS	Yes	Pairing up with the negative rail of remote sensing line that connected to RGNDS, and routing them to the load sensing points. Reserve an RC from FBS to GND to compensate the output lagging from DAC during DVID transitions.
VSENS	No	Used for Overvoltage protection sensing only, and it has 1µs internal filter. Decoupling is NOT needed. Add a series impedance to be compatible with ISL6364A.
RGNDS		Pairing up with the positive rail remote sensing line that connected to FB resistor, and routing them to the load sensing points.
FSS_DDRS	Yes	Placing the R in close proximity to the controller. Avoid using decoupling capacitor on this pin. Must tie GND or VCC via 1MΩ depending upon the desired ADDRESS offset when VR1 is not in use. Don't use decoupling capacitor on this pin. To minimize the effect of cross coupling between regulators, select operating frequencies of VR0 and VR1 at least 50kHz apart.

TABLE 14. PIN DESIGN AND/OR LAYOUT CONSIDERATION (Continued)

PIN NAME	NOISE SENSITIVITY	DESCRIPTION
TMS		Placing NTC in close proximity to the output inductor of VR1 and to the output rail, not close to MOSFET side (see Figure 23); the return trace should be 25 mils away from other traces. Place 1k pull-up and decoupling capacitor (typically 0.1µF) in close proximity to the controller. The pull-up resistor should be exactly tied to the same point as VCC pin, not through an RC filter. If not used, connect this pin to TM or 1MΩ/2MΩ resistor divider, but DON'T tie it to VCC or GND. Place the NTC in proximity to the output rail, not close to MOSFET side.
ISENS+	Yes	Connect to the output rail side of the output inductor or current sensing resistor pin with Isen resistor and decoupling capacitor (27ns) placed in close proximity to the controller.
ISENS-	Yes	Connect to the phase node side of the output inductor or resistor pin with L/DCR or ESL/R_{SEN} matching network in close proximity to the ISENS±- pins of the controller. Differential pair with ISENS+ routing back to the controller.
PWMS	No	Avoid the routing across or under other phase's power trains and DCR sensing network. Don't make them across or under external components of the controller. At least 30mils away from any other traces.
ADDR_XX; NPSI_XX; BT_XX; BTS_XX	No	Register setting is locked prior to soft start. Since the external resistor-divider ratio compares with the internal resistor ratio of the VCC, their rail should be exactly tied to the same point as VCC pin, not through an RC filter. DON'T use decoupling capacitors on these pins.
TM		Placing NTC in close proximity to the output inductor of VR0's Channel 1 and to the output rail, not close to MOSFET side (see Figure 23); the return trace should be 25 mils away from other traces. Place 1k pull-up and decoupling capacitor (typically 0.1µF) in close proximity to the controller. The pull-up resistor should be exactly tied to the same point as VCC pin, not through an RC filter. If not used, connect this pin to TMS or 1M Ω/2M Ω resistor divider, but DON'T tie it to VCC or GND.
SICI	No	Program SI (standard-inductor, tied to GND) and CI (coupled inductor, tied to VCC). It is reserved for IAUTO in ISL6364A and will be noise sensitive; SI and CI are still programmable with this pin.
RSET	Yes	Placing the R in close proximity to the controller. DON'T use decoupling capacitor on this pin.

TABLE 14. PIN DESIGN AND/OR LAYOUT CONSIDERATION (Continued)

PIN NAME	NOISE SENSITIVITY	DESCRIPTION
FS_DRP	Yes	Placing the R in close proximity to the controller. Must tie GND or VCC via 1MΩ when VR0 is not in use. Don't use decoupling capacitor on this pin.
VCC	Yes	Place the decoupling capacitor in close proximity to the controller.
PWM1-4	NO	Avoid the respective PWM routing across or under other phase's power trains/planes and current sensing network. Don't make them across or under external components of the controller. At least 20mils away from any other traces.
EN_VTT	No	There is an internal 1μs filter. Decoupling capacitor is not needed, but if needed, use a low timing constant one to avoid too much shut-down delay.
ISEN[4:1]+	Yes	Connect to the output rail side of the respective channel's output inductor or resistor pin. Decoupling is optional and might be required for long sense traces and a poor layout.
ISEN[4:1]-	Yes	Connect to the phase node side of the respective channel's output inductor or resistor pin with L/DCR or ESL/R_{SEN} matching network in close proximity to the ISEN± pins of VR0. Differentially routing back to the controller by paring with respective ISEN+; at least 20 mils spacing between pairs and away from other traces. Each pair should not across or under the other channel's switching nodes [Phase, UGATE, LGATE] and power planes even though they are not in the same layer.
GND	Yes	This EPAD is the return of PWM output drivers and SVID bus. Use 4 or more vias to directly connect the EPAD to the power ground plane. Avoid using only single via or 0Ω resistor connection to the power ground plane.
General Comments		The layer next to the Top or Bottom layer is preferred to be ground players, while the signal layers can be sandwiched in the ground layers if possible.

Component Placement

Within the allotted implementation area, orient the switching components first. The switching components are the most critical because they carry large amounts of energy and tend to generate high levels of noise. Switching component placement should take into account power dissipation. Align the output inductors and MOSFETs such that space between the components is minimized while creating the PHASE plane. Place the Intersil MOSFET driver IC as close as possible to the MOSFETs they control to reduce the parasitic impedances due to trace length between critical driver input and output signals. If possible, duplicate the same placement of these components for each phase.

Next, place the input and output capacitors. Position the high-frequency ceramic input capacitors next to each upper MOSFET drain. Place the bulk input capacitors as close to the upper MOSFET drains as dictated by the component size and dimensions. Long distances between input capacitors and MOSFET drains result in too much trace inductance and a reduction in capacitor performance. Locate the output capacitors between the inductors and the load, while keeping them in close proximity to the microprocessor socket.

To improve the chance of first pass success, it is very important to take time to follow the above outlined design guidelines and Intersil generated layout check list, see more details in "Voltage-Regulator (VR) Design Materials" on page 42. Proper planning for the layout is as important as designing the circuits. Running things in a hurry, you could be end up spending weeks and months to debug a poorly-designed and improper-layout board.

Powering Up And Open-Loop Test

The ISL6364 features very easy debugging and powering up. For the first-time powering up, an open-loop test can be done by applying sufficient voltage (current limiting to 0.25A) to VCC, proper pull-up to SVID bus, and signal high to EN_VTT and EN_PWR pins with the input voltage (VIN) disconnected.

1. Each PWM output should operate at maximum duty cycle (typically VR0 at 98% and VR1 at 83%) and correct switching frequency.
2. The 0C, 0D, 0E, and 0F registers can be read via SVID bus to check its proper setting if an VTT tool is installed and operating.
3. If 5V drivers are used and share the same rail as VCC, the proper switching on UGATEs and LGATEs should be seen.
4. If 12V drivers are used and can be disconnected from VIN and sourced by an external 12V supply, the proper switching on UGATEs and LGATEs should be observed.
5. If the above is not properly operating, you should check soldering joint, resistor register setting, Power Train connection or damage, i.e, shorted gates, drain and source. Sometimes the gate might be measured short due to residual gate charge. Therefore, a measured short gate with ohmmeter cannot validate if the MOSFET is damaged unless the Drain to Source is also measured short.
6. When the re-work is needed for the L/DCR matching network, use an ohmmeter across the C to see if the correct R value is measured before powering the VR up; otherwise, the current imbalance due to improper re-work could damage the power trains.
7. After everything is checked, apply low input voltage (1-5V) with appropriate current limiting (~0.5A). All phases should be switching evenly.
8. Remove the pull-up from EN_PWR pin, using bench power supplies, power up VCC with current limiting (typically ~ 0.25A if 5V drivers included) and slowly increase Input Voltage with current limiting. For typical application, VCC limited to 0.25A, VIN limited to 0.5A should be safe for powering up without no load. High core-loss inductors likely need to increase the input current limiting. All phases should be switching evenly.

Voltage-Regulator (VR) Design Materials

The tolerance band calculation (TOB) worksheets for VR output regulation and IMON have been developed using the Root-Sum-Squared (RSS) method with 3 sigma distribution point of the related components and parameters. Note that the "Electrical Specifications" table beginning on page 8 specifies no less than 6 sigma distribution point, not suitable for RSS TOB calculation. To support VR design and layout, Intersil also developed a set of worksheets and evaluation boards, as listed in Tables 15 and 16, respectively. Contact Intersil's local office or field support for the latest available information.

TABLE 15. AVAILABLE DESIGN ASSISTANCE MATERIALS

Item	Description
0	**VR12 Design and Validation**
1	VR12 Design Worksheet for Compensation and Component Selection
2	Transient Response Optimization Guidelines
3	VOUT and IMON TOB Calculator
4	SVID and PMBus Communication Tool
5	Resistor Register Calculator
6	Dynamic VID Compensation Calculator
7	VR12 Layout Design Guidelines
8	TCOMP and TM Selection Worksheet
9	Fine Tune OCP and Droop Worksheet
10	Evaluation Board Schematics in OrCAD Format and Layout in Allegro Format

NOTE: For worksheets, please contact Intersil Application support at www.intersil.com/design/.

TABLE 16. AVAILABLE VR12 EVALUATION BOARDS

EVALUATION BOARDS	# OF PHASES	# OF INTEGRATED DRIVERS	PACKAGE	TARGETED APPLICATIONS	I^{2}C/PMBUS	PEAK EFFICIENCY	PEAK CURRENT
ISL6366/67EVAL1	6+1	-	7x7 60 Ld	High-End Desktop and Server with Discrete Drivers and MOSFETs	Yes	93%, 1.2V@50A	190A +25A
ISL6366/67EVAL2	6+1	-	7x7 60 Ld	High-End Desktop and Server with DrMOS	Yes	93.5%, 1.2V@50A	190A +25A
ISL6364EVAL1	4+1	-	6x6 48 Ld	Desktop/Memory		88%, 1.2V@50A	120A +35A
ISL6363EVAL1	4+1	2+1	7x7 60 Ld	Desktop		88%, 1.2V@50A	120A +35A
ISL6353EVAL1	3+0	2	5x5 40 Ld	Memory		94%, 1.5V@25A	100A

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
12/22/10	FN6861.0	Initial Release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL6364

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: http://rel.intersil.com/reports/sear

intersil™

Package Outline Drawing

L48.6x6B
48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 9/09

TOP VIEW

BOTTOM VIEW

TYPICAL RECOMMENDED LAND PATTERN

SIDE VIEW

DETAIL "X"
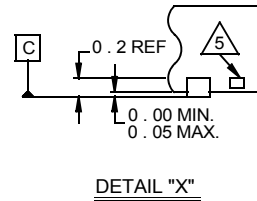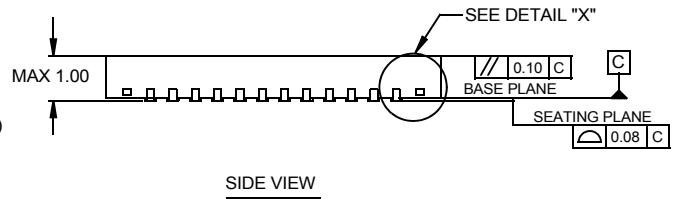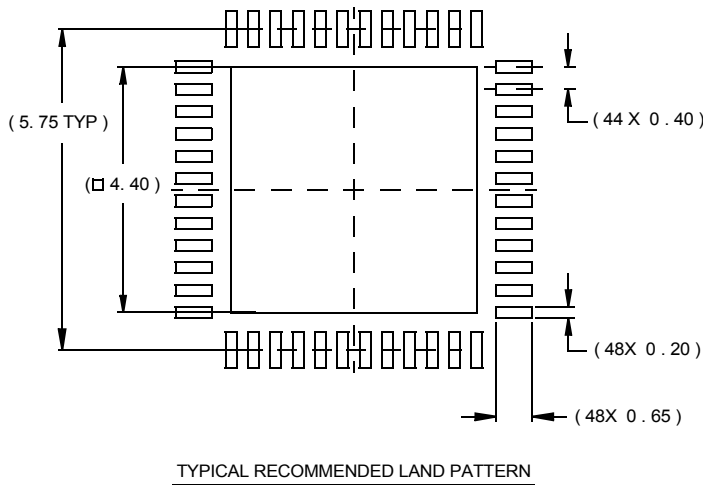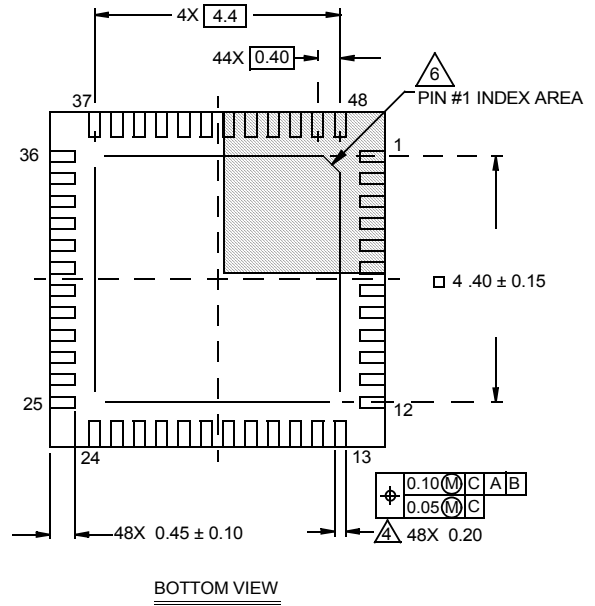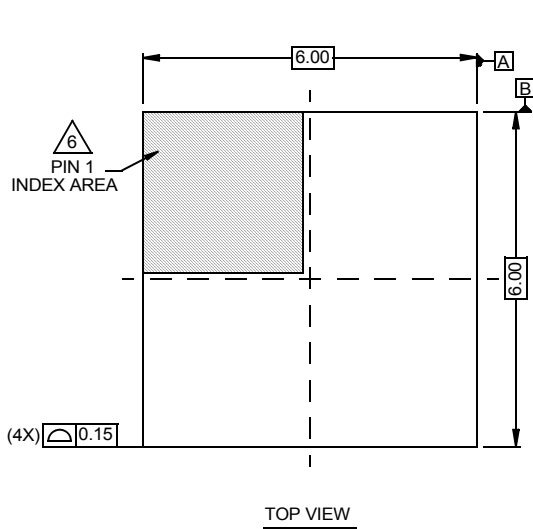
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.

2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.

3. Unless otherwise specified, tolerance : Decimal ± 0.05

4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.

5. Tiebar shown (if present) is a non-functional feature.

6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.