HIGH FREQUENCY & HIGH DRIVE SYNCHRONOUS PWM CONTROLLER

PRELIMINARY DATA SHEET

DESCRIPTION

The NX2210/2211 family of controller ICs are synchronous Buck controller IC designed for step down DC to DC converter applications. They are optimized to convert bus voltages from 2V to 25V to outputs as low as 0.8V voltage. Both devices offer an Enable pin that can be used to program the converter's start voltage using an external divider from bus voltage. The NX2211 operates at fixed 600kHz while 2210 has ability to program switching frequency from 200kHz to 1MHz, making it ideal for applications requiring ceramic output capacitor. The NX2211 has an added Power Good function. Both devices have less than 50 nS of dead band which increases efficiency at higher frequencies.

Other features of the device are:Internal digital soft start; Vcc undervoltage lock out; Output undervoltage protection with digital filter and shutdown capability via the enable pin.

FEATURES

- <1ohm Driver keeps High Capacitance Synchronous MOSFET off during SW node transition
- Bus voltage operation from 2V to 25V
- Power Good indicator available for NX2211
- Fixed 600kHz for NX2211 and adjustable frequency up to 1MHz for NX2210
- Internal Digital Soft Start Function
- Less than 50 nS adaptive deadband
- Enable pin allows BUS voltage UVLO programmability
- Short protection with feedback UVLO

APPLICATIONS

- Graphic Card on board converters
- Memory Vddq Supply
- On board DC to DC such as 12V to 3.3V, 2.5V or 1.8V
- ADSL Modem

TYPICAL APPLICATION

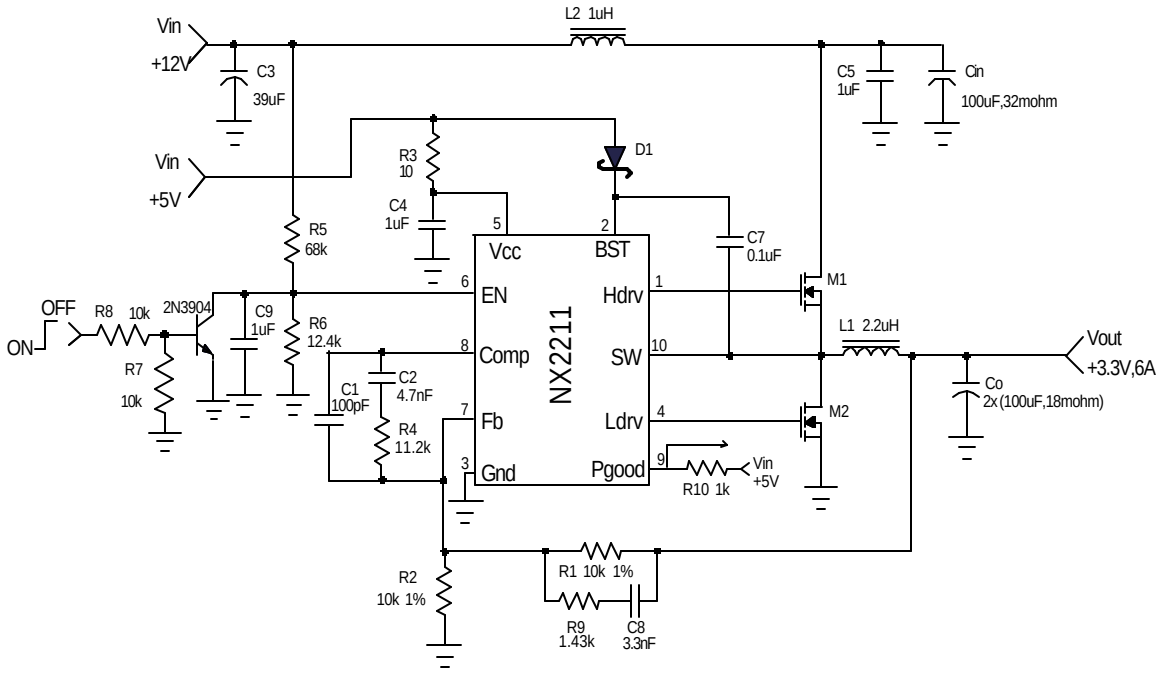


Figure1 - Typical application of 2211

ORDERING INFORMATION

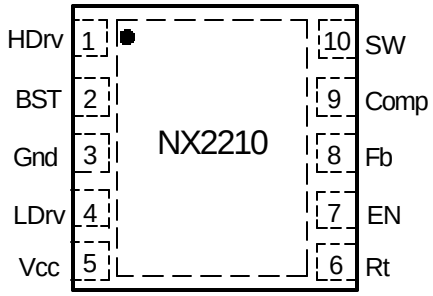
Device	Temperature	Package	Frequency
NX2210CMTR	0 to 70°C	MLPD-10L	200kHz to 1MHz
NX2211CMTR	0 to 70° C	MLPD-10L	600kHz

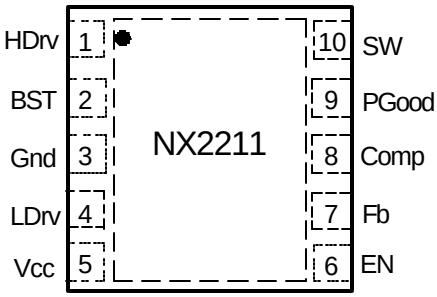
ABSOLUTE MAXIMUM RATINGS(NOTE1)

Vcc to GND & BST to SW voltage 6.5V
BST to GND Voltage 35V
Storage Temperature Range ..... -65°C to 150°C
Operating Junction Temperature Range ..... -40°C to 125°C

PACKAGE INFORMATION

10-LEAD PLASTIC MLPD(NX2210)	10-LEAD PLASTIC MLPD(NX2211)
$\theta_{JA} \approx 52°C/W$ (NOTE2)	$\theta_{JA} \approx 52°C/W$ (NOTE3)





ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc = 5V, and T_A= 0 to 70°C. Typical values refer to Ta = 25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Feedback Voltage						
FB Voltage	V_{REF}	4.5 < Vcc < 5.5		0.800		V
FB Voltage Line Regulation				0.2		%
Vcc supply voltage						
UVLO Threshold - Vcc	V_{CC}	Supply Ramping Up		4.1		V
UVLO Hysteresis - Vcc	$V_{CC—Hyst}$			0.22		V
UVLO Threshold - BST	V_{BST}	Supply Ramping Up		2.4		V
UVLO Threshold - FB		FB Ramping Down		0.4		V
Supply Current						
Vcc Dynamic Supply Current	I_{CC_DYN}	Freq =300KHz, Cl = 3300pF		5		mA
BST Dynamic Supply Current	I_{BST_DYN}	Freq = 300KHz, Cl = 3300pF		5		mA
Vcc Static Supply Current	I_{CC_STA}			3		mA
BST Static Supply Current	I_{BST_STA}			0.1		mA
Soft Start Section						
Soft start time	T_{ss}	Fsw=300Khz, 2211 Fsw=1Mhz, 2210		3.4 1.02		mS mS
Error Amp						
Transconductance	g_m			2500		umho

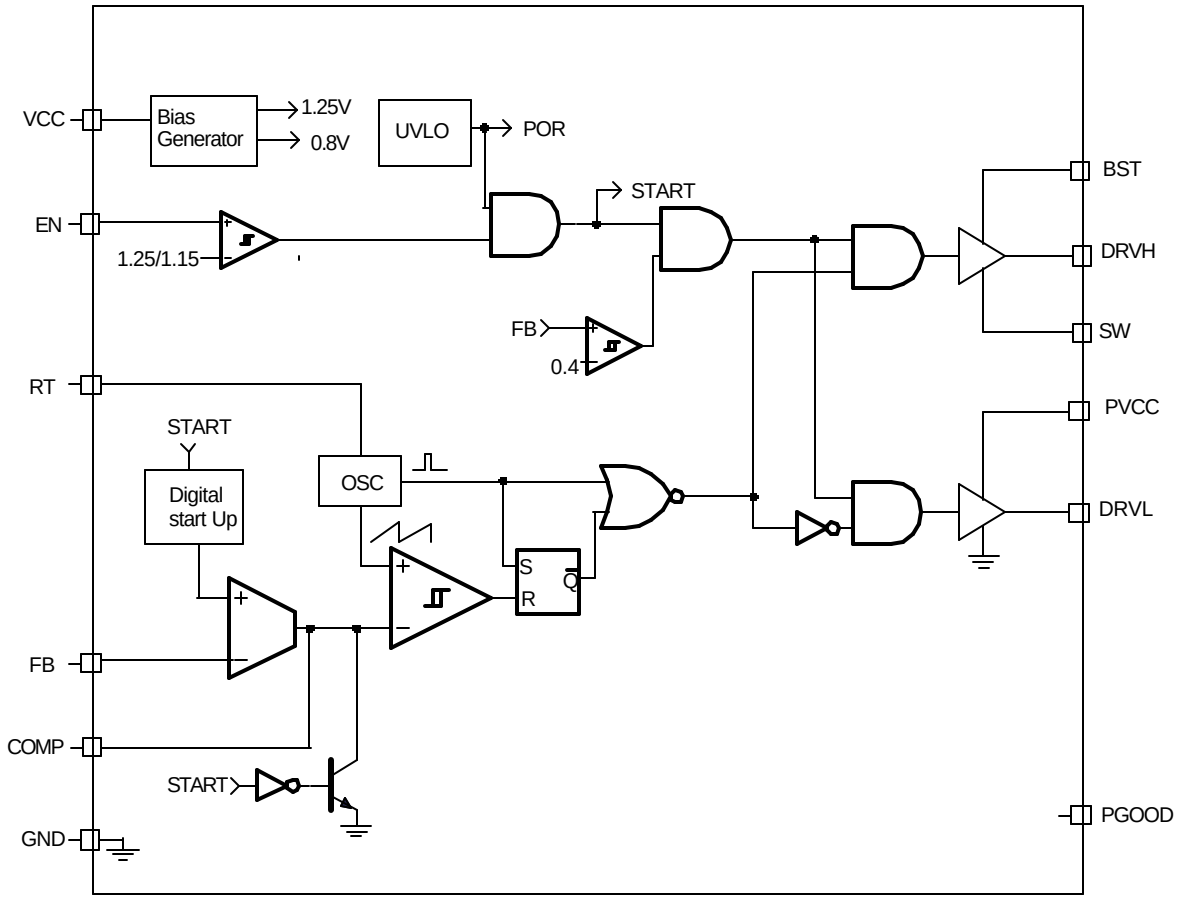
PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Oscillator						
Frequency	F_S	NX2211		600		KHz
		NX2210		1000		KHz
Ramp Amplitude	V_{RAMP}			2		Vpp
Output Drivers						
HDRV source impedance		I=200mA		0.9		ohm
HDRV sink impedance		I=200mA		0.65		ohm
LDRV source impedance		I=200mA		0.9		ohm
LDRV sink impedance		I=200mA		0.5		ohm
Rise Time	T_{RISE}	Cload = 1500pF		50		nS
Fall Time	T_{FALL}	Cload = 1500pF		50		nS
Dead Band Time	T_{dead}			30		nS
Max Duty Cycle	D_{max}	FB = 0.6V		95		%
Min Duty Cycle	D_{min}	FB = 1V			0	%
EN						
Enable Threshold Voltage		Enable ramp up		1.6		V
Enable Hysterises				0.1		V
Power Good(2211 only)						
Threshold				$0.9V_{REF}$		V
Hysteresis				$0.05V_{REF}$		V
PGood Voltage Low				0.2		V

NOTE1: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
NOTE2: PAD is NC.
NOTE3: PAD is NC.

PIN DESCRIPTIONS

PIN #		PIN SYMBOL	PIN DESCRIPTION
2210	2211		
1	1	HDRV	High side MOSFET gate driver.
2	2	BST	This pin supplies voltage to the high side driver. A high frequency ceramic capacitor of 0.1 to 1 uF must be connected from this pin to SW pin.
3	3	Gnd	Power and analog ground pin. Connect this pin directly to ground plane using a via.
4	4	LDRV	Low side MOSFET gate driver.
5	5	Vcc	Voltage supply for the internal circuit as well as the low side MOSFET gate driver. A 1uF high frequency ceramic capacitor must be connected from this pin to ground plane using a via.
6		Rt	Add resistor to this pin for adjustable frequency which is from 20kHz to 1MHz
7	6	EN	Pull up this pin to Vcc for normal operation. Pulling this pin down below 1.25V shuts down the controller and resets the soft start. This pin can also be used as a UVLO detector for the bus voltage via a resistor divider.
8	7	FB	FB pin is the error amplifier inverting input. This pin is also connected to the output UVLO comparator. When this pin falls below 0.4V, both HDRV and LDRV outputs are latched off.
9	8	COMP	This pin is the output of the error amplifier and together with FB pin is used to compensate the voltage control feedback loop. This pin is also used as a shut down pin.
10	10	SW	This pin is connected to the source of the high side MOSFET and provides return path for the high side driver.
	9	PGood	This is an open drain output and it is pulled low if the output voltage is not within the above specification. If not used it may be left floating.

BLOCK DIAGRAM



Demo Board Schematic

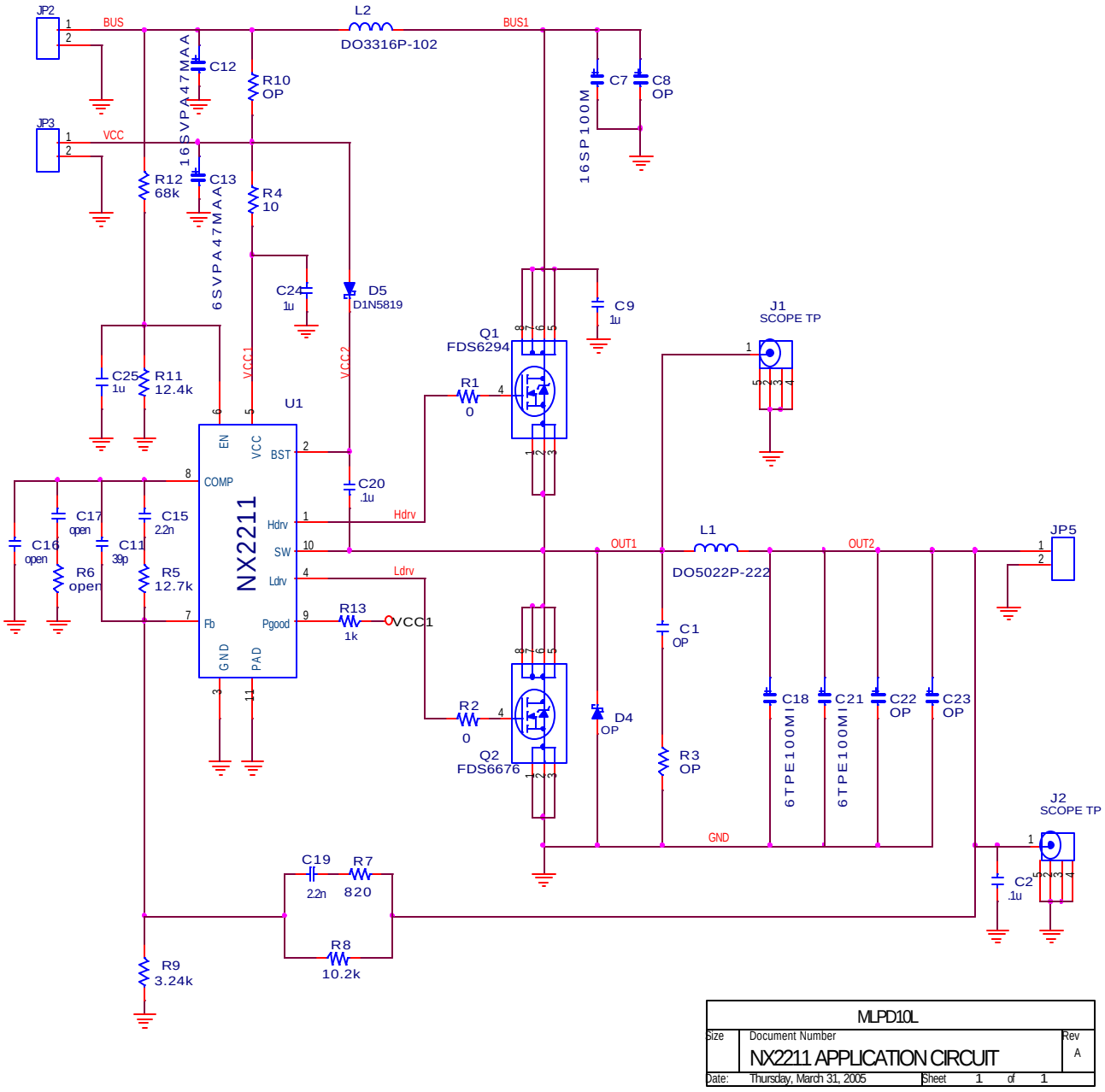


Figure 2 - Demoboard design on NX2211

Bill of Materials

Item	Quantity	Reference	Part	Manufacture
1	8	C1,R3,D4,C8,R10,C22,C23,	OPEN	
		C25		
2	2	C2,C20	.1u	
3	1	C7	16SP100M	SANYO
4	2	C9,C24	1u	
5	1	C11	39p	
6	1	C12	16SVPA47MAA	SANYO
7	1	C13	6SVPA47MAA	SANYO
8	2	C15,C19	2.2n	
9	3	R6,C16,C17	open	
10	2	C18,C21	6TPE100MI	SANYO
11	1	D5	D1N5819	
12	3	JP2,JP3,JP5	CON2	
13	2	J1,J2	SCOPE TP	
14	1	L1	DO5022P-222	Coilcraft
15	1	L2	DO3316P-102	Coilcraft
16	1	Q1	FDS6294	Fairchild
17	1	Q2	FDS6676	Fairchild
18	2	R1,R2	0	
19	1	R4	10	
20	1	R5	12.7k	
21	1	R7	820	
22	1	R8	10.2k	
23	1	R9	3.24k	
24	3	R11	12.4k	
24	3	R12	68k	
24	3	R13	1k	
25	1	U1	NX2211	NEXSEM INC.

DEMO BOARD WAVEFORM

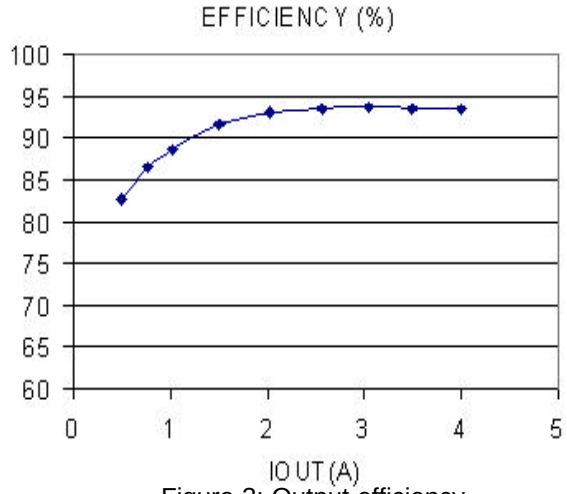


Figure 3: Output efficiency

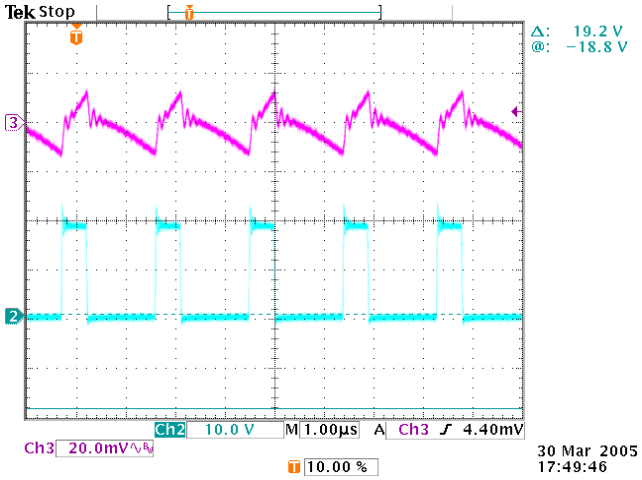


Figure 4: Voltage ripple @1.6 V output voltage. (Ch3-ripple, Ch2-Hdrv)

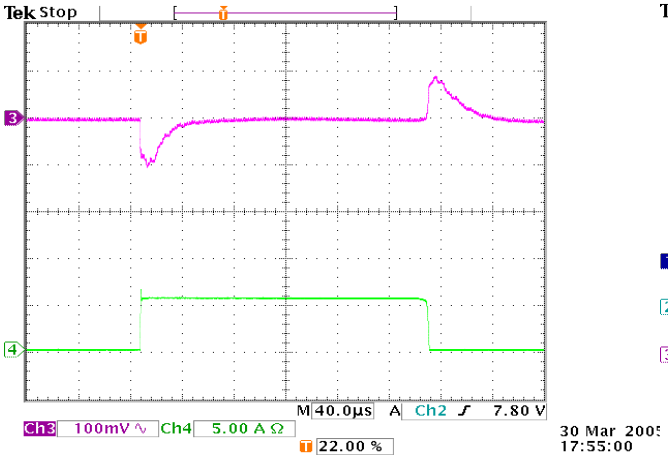


Figure 5: Output voltage transient response for load curent 0A-10A

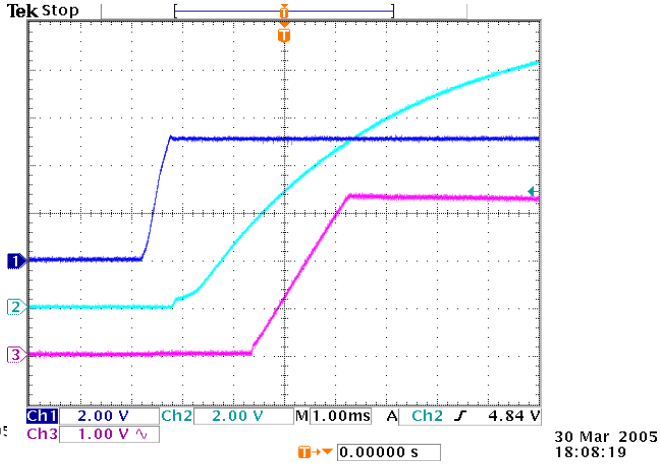


Figure 6: Start up time(Ch1-VCC, Ch2-Bus voltage, Ch3-output volatge)

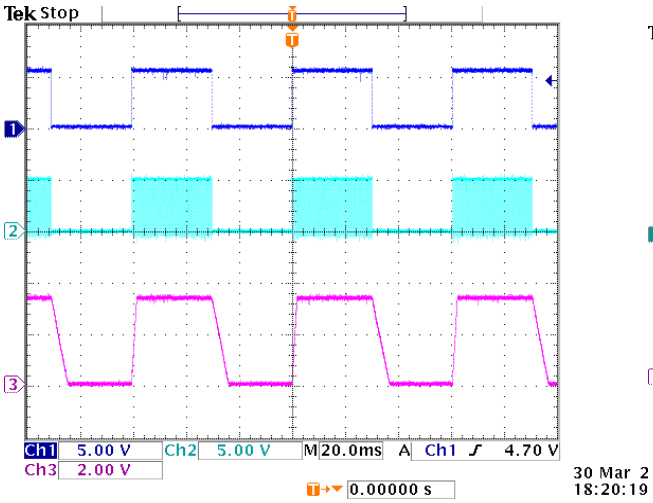


Figure 7: ENABLE function.(Ch1-enable, Ch2-Ldrv, Ch3-output voltage)

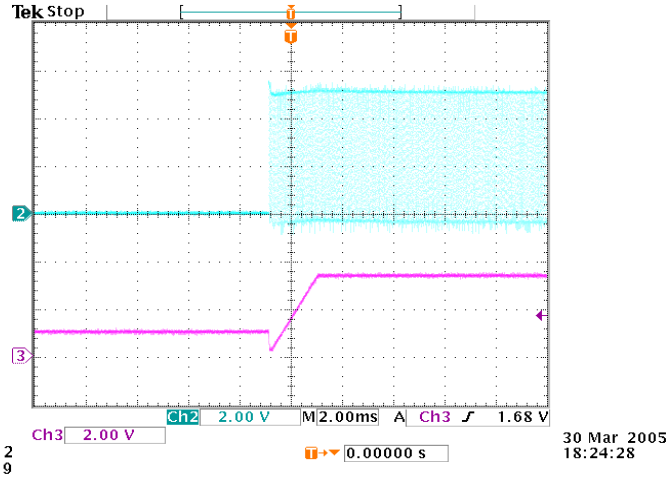


Figure 8: Startup operation waveform

APPLICATION INFORMATION

Symbol Used In Application Information:

V_{IN} - Input voltage
V_{OUT} - Output voltage
I_{OUT} - Output current
ΔV_{RIPPLE} - Output voltage ripple
F_S - Working frequency
ΔI_{RIPPLE} - Inductor current ripple

Design Example

The following is typical application for NX2211, the schematic is figure 2.

V_{IN} = 12V
V_{OUT}=3.3V
F_S=600kHz
I_{OUT}=6A
ΔV_{RIPPLE} <=30mV
ΔV_{DROOP}<=100mV @ 6A step

Output Inductor Selection

The selection of inductor value is based on inductor ripple current, power rating, working frequency and efficiency. Larger inductor value normally means smaller ripple current. However if the inductance is chosen too large, it brings slow response and lower efficiency. Usually the ripple current ranges from 20% to 40% of the output current. This is a design freedom which can be decided by design engineer according to various application requirements. The inductor value can be calculated by using the following equations:

$$L_{OUT}=\frac{V_{IN}-V_{OUT}}{\Delta I_{RIPPLE}}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{F_S} \quad ...(1)$$

$$I_{RIPPLE}=k\times I_{OUTPUT}$$

where k is between 0.2 to 0.4.

Select k=0.3, then

$$L_{OUT}=\frac{12V-3.3V}{0.3\times 6A}\times\frac{3.3V}{12V}\times\frac{1}{600kHz}$$

L_{OUT}=2.2uH

Choose inductor from COILCRAFT DO5022P-222 with L=2.2uH is a good choice.

Current Ripple is recalculated as

$$\Delta I_{RIPPLE}=\frac{V_{IN}-V_{OUT}}{L_{OUT}}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{F_S}$$
$$=\frac{12V-3.3V}{2.2uH}\times\frac{3.3v}{12v}\times\frac{1}{600kHz}=1.8A \quad ...(2)$$

Output Capacitor Selection

Output capacitor is basically decided by the amount of the output voltage ripple allowed during steady state(DC) load condition as well as specification for the load transient. The optimum design may require a couple of iterations to satisfy both condition.

Based on DC Load Condition

The amount of voltage ripple during the DC load condition is determined by equation(3).

$$\Delta V_{RIPPLE}=ESR\times\Delta I_{RIPPLE}+\frac{\Delta I_{RIPPLE}}{8\times F_S\times C_{OUT}} \quad ...(3)$$

Where ESR is the output capacitors' equivalent series resistance,C_{OUT} is the value of output capacitors.

Typically when large value capacitors are selected such as Aluminum Electrolytic,POSCAP and OSCON types are used, the amount of the output voltage ripple is dominated by the first term in equation(3) and the second term can be neglected.

For this example, POSCAP are chosen as output capacitors, the ESR and inductor current typically determines the output voltage ripple.

$$ESR_{desire}=\frac{\Delta V_{RIPPLE}}{\Delta I_{RIPPLE}}=\frac{30mV}{1.8A}=16.7m\Omega \quad ...(4)$$

If low ESR is required, for most applications, multiple capacitors in parallel are better than a big capacitor. For example, for 30mV output ripple, POSCAP 6TPE100MI with 18mΩ are chosen.

$$N=\frac{ESR_E\times\Delta I_{RIPPLE}}{\Delta V_{RIPPLE}} \quad ...(5)$$

Number of Capacitor is calculated as

$$N=\frac{18m\Omega\times 1.8A}{30mV}$$

N =1.08

The number of capacitor has to be round up to a integer. Choose N =2.

If ceramic capacitors are chosen as output ca

pacitors, both terms in equation (3) need to be evaluated to determine the overall ripple. Usually when this type of capacitors are selected, the amount of capacitance per single unit is not sufficient to meet the transient specification, which results in parallel configuration of multiple capacitors .

For example, one 100uF, X5R ceramic capacitor with 2mΩ ESR is used. The amount of output ripple is

$$\Delta V_{RIPPLE} = 2m\Omega \times 1.8A + \frac{1.8A}{8 \times 600kHz \times 100uF}$$
$$= 3.6mV + 3.8mV = 7.4mV$$

Although this meets DC ripple spec, however it needs to be studied for transient requirement.

Based On Transient Requirement

Typically, the output voltage droop during transient is specified as:

$\Delta V_{DROOP} < \Delta V_{TRAN}$ @ step load ΔI_{STEP}

During the transient, the voltage droop during the transient is composed of two sections. One Section is dependent on the ESR of capacitor, the other section is a function of the inductor, output capacitance as well as input, output voltage. For example, for the overshoot, when load from high load to light load with a ΔI_{STEP} transient load, if assuming the bandwidth of system is high enough, the overshoot can be estimated as the following equation.

$$\Delta V_{overshoot} = ESR \times \Delta I_{step} + \frac{V_{OUT}}{2 \times L \times C_{OUT}} \times \tau^2 \quad ...(6)$$

where t is the a function of capacitor, etc.

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \dfrac{L \times \Delta I_{step}}{V_{OUT}} - ESR \times C_{OUT} & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(7)$$

where

$$L_{crit} = \frac{ESR \times C_{OUT} \times V_{OUT}}{\Delta I_{step}} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} \quad ...(8)$$

where ESR_E and C_E represents ESR and capacitance of each capacitor if multiple capacitors are used in parallel.

The above equation shows that if the selected output inductor is smaller than the critical inductance, the voltage droop or overshoot is only dependent on the ESR of output capacitor. For low frequency capacitor such as electrolytic capacitor, the product of ESR and capacitance is high and $L \le L_{crit}$ is true. In that case, the transient spec is dependent on the ESR of capacitor.

In most cases, the output capacitors are multiple capacitors in parallel. The number of capacitors can be calculated by the following

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2 \quad ...(9)$$

where

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \dfrac{L \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(10)$$

For example, assume voltage droop during transient is 100mV for 6A load step.

If the POSCAP 6TPE100MI(100uF, 18mΩ) is used, the critical inductance is given as

$$L_{crit} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} =$$
$$\frac{18m\Omega \times 100\mu F \times 3.3V}{6A} = 0.99\mu H$$

The selected inductor is 2.2uH which is bigger than critical inductance. In that case, the output voltage transient not only dependent on the ESR, but also capacitance.

number of capacitors is

$$\tau = \frac{L \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E$$
$$= \frac{2.2\mu H \times 6A}{3.3V} - 18m\Omega \times 100\mu F = 2.2us$$

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2$$
$$= \frac{18m\Omega \times 6A}{100mV} +$$
$$\frac{3.3V}{2 \times 2.2\mu H \times 100\mu F \times 100mV} \times (2.2us)^2$$
$$= 1.4$$

The number of capacitors has to satisfied both ripple and transient requirement. Overall, we can choose N=2.

It should be considered that the proposed equation is based on ideal case, in reality, the droop or overshoot is typically more than the calculation. The equation gives a good start. For more margin, more capacitors have to be chosen after the test. Typically, for high frequency capacitor such as high quality POSCAP especially ceramic capacitor, 20% to 100% (for ceramic) more capacitors have to be chosen since the ESR of capacitors is so low that the PCB parasitic can affect the results tremendously. More capacitors have to be selected to compensate these parasitic parameters.

Compensator Design

Due to the double pole generated by LC filter of the power stage, the power system has 180° phase shift , and therefore, is unstable by itself. In order to achieve accurate output voltage and fast transient response,compensator is employed to provide highest possible bandwidth and enough phase margin.Ideally,the Bode plot of the closed loop system has crossover frequency between1/10 and 1/5 of the switching frequency, phase margin greater than 50° and the gain crossing 0dB with -20dB/decade. Power stage output capacitors usually decide the compensator type. If electrolytic capacitors are chosen as output capacitors, type II compensator can be used to compensate the system, because the zero caused by output capacitor ESR is lower than crossover frequency. Otherwise type III compensator should be chosen.

A. Type III compensator design

For low ESR output capacitors, typically such as Sanyo oscap and poscap, the frequency of ESR zero caused by output capacitors is higher than the crossover frequency. In this case, it is necessary to compensate the system with type III compensator. The following figures and equations show how to realize the type III compensator by transconductance amplifier.

$$F_{Z1} = \frac{1}{2\times p \times R_4 \times C_2} \quad ...(11)$$

$$F_{Z2} = \frac{1}{2\times p \times (R_2 + R_3)\times C_3} \quad ...(12)$$

$$F_{P1} = \frac{1}{2\times p \times R_3 \times C_3} \quad ...(13)$$

$$F_{P2} = \frac{1}{2\times p \times R_4 \times \frac{C_1 \times C_2}{C_1 + C_2}} \quad ...(14)$$

where F_{Z1},F_{Z2},F_{P1} and F_{P2} are poles and zeros in the compensator. Their locations are shown in figure 10.

The transfer function of type III compensator for transconductance amplifier is given by:

$$\frac{V_e}{V_{OUT}} = \frac{1 - g_m \times Z_f}{1 + g_m \times Z_{in} + Z_{in}/R_1}$$

For the voltage amplifier, the transfer function of compensator is

$$\frac{V_e}{V_{OUT}} = \frac{-Z_f}{Z_{in}}$$

To achieve the same effect as voltage amplifier, the compensator of transconductance amplifier must satisfy this condition: R4>>2/gm.R1||R2||R3>>1/gm is desirable.

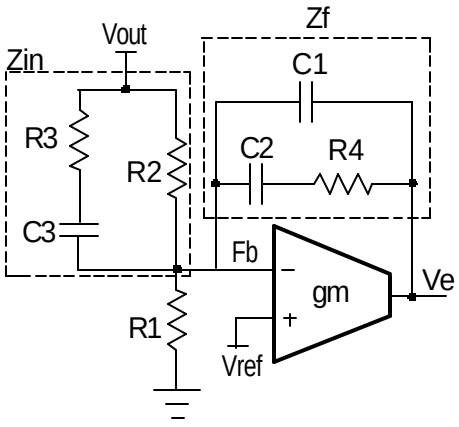


Figure 9 - Type III compensator using transconductance amplifier

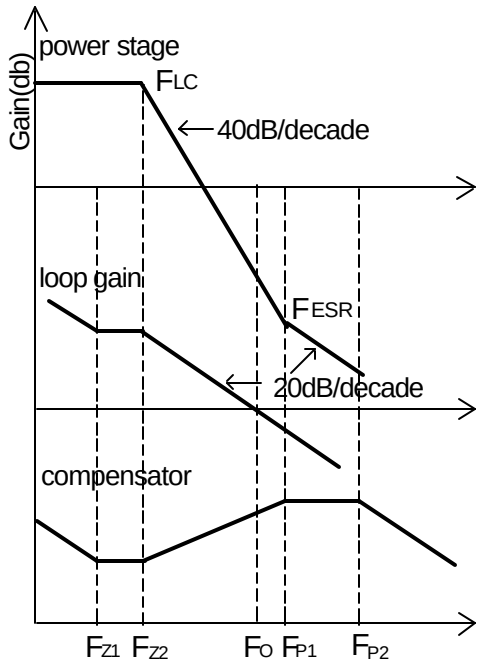


Figure 10 - Bode plot of Type III compensator

Design example for type III compensator are in order. The crossover frequency has to be selected as $F_{LC}<F_O<F_{ESR,}$ and $F_O<=1/10~1/5F_{s.}$

1.Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC}=\frac{1}{2\times p\times\sqrt{L_{OUT}\times C_{OUT}}}=\frac{1}{2\times p\times\sqrt{2.2uH\times 200uF}}=7.59kHz$$

$$F_{ESR}=\frac{1}{2\times p\times ESR\times C_{OUT}}=\frac{1}{2\times p\times 9m\Omega\times 200uF}=88.42kHz$$

2.Set R_2 equal to10.2kΩ,

$$R_1=\frac{R_2\times V_{REF}}{V_{OUT}-V_{REF}}=\frac{10.2k\Omega\times 0.8V}{3.3V-0.8V}=3.26k\Omega$$

Choose R_1= 3.24kΩ.

3. Set zero $F_{Z2}=F_{LC}$ and $F_{p1}=F_{ESR}$.

4. Calculate R_4 and C_3 with the crossover frequency smaller than 1/10~ 1/5 of the swithing frequency. Set F_O=60kHz.

$$C_3=\frac{1}{2\times p\times R_2}\times\left(\frac{1}{F_{z2}}-\frac{1}{F_{p1}}\right)=\frac{1}{2\times p\times 10k\Omega}\times\left(\frac{1}{7.59kHz}-\frac{1}{88.42kHz}\right)=1.9nF$$

Choose C3=2.2nF.

$$R_4=\frac{V_{OSC}}{V_{in}}\times\frac{2\times p\times F_O\times L}{C_3}\times C_{out}=\frac{2V}{12V}\times\frac{2\times p\times 60kHz\times 2.2uH}{2.2nF}\times 200uF=12.6k\Omega$$

Choose R4=12.7k

5. Calculate C_2 with zero F_{z1} at 75% of the LC double pole by equation (11).

$$C_2=\frac{1}{2\times p\times F_{Z1}\times R_4}=\frac{1}{2\times p\times 0.75\times 7.59kHz\times 12.7k\Omega}=2.22nF$$

Choose C2=2.2nF

6. Calculate C_1 by equation (14) with pole F_{p2} at half the swithing frequency.

$$C_1=\frac{1}{2\times p\times R_4\times F_{P2}}=\frac{1}{2\times p\times 12.7k\Omega\times 150kHz}=42pF$$

Choose C1=39pF

7. Calculate R_3 by equation (13).

$$R_3=\frac{1}{2\times p\times F_{P1}\times C_3}=\frac{1}{2\times p\times 88.42kHz\times 2.2nF}=818\Omega$$

Choose R_3= 820Ω.

B. Type II compensator design

If the electrolytic capacitors are chosen as power stage output capacitors, usually the Type II compensator can be used to compensate the system.

Type II compensator can be realized by simple RC circuit without feedback as shown in figure 11. R3 and C1 introduce a zero to cancel the double pole effect. C2 introduces a pole to suppress the switching noise. The following equations show the compensator pole zero location and constant gain.

$$Gain = g_m \times \frac{R_1}{R_1 + R_2} \times R_3 \quad \text{... (15)}$$

$$F_z = \frac{1}{2 \times p \times R_3 \times C_1} \quad \text{... (16)}$$

$$F_p \approx \frac{1}{2 \times p \times R_3 \times C_2} \quad \text{... (17)}$$

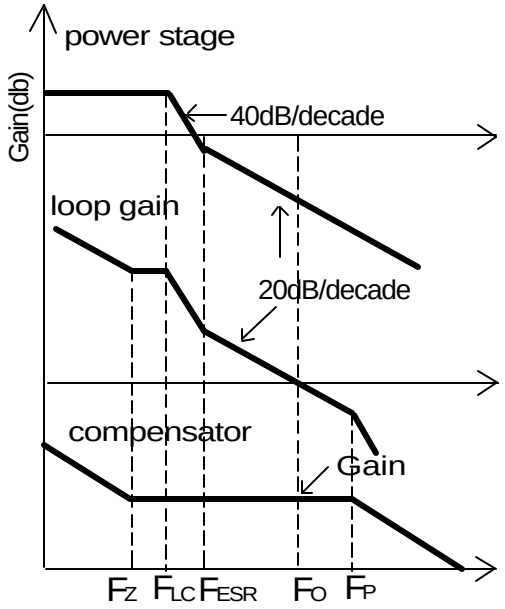


figure 12 - Bode plot of Type II compensator

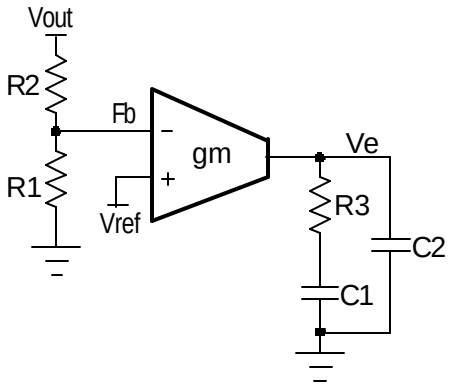


Figure 11 - Type II compensator with transconductance amplifier

For this type of compensator, F_O has to satisfy $F_{LC} < F_{ESR} << F_O <= 1/10 \sim 1/5 F_s$.

The following uses the same power stage parameters as demoboard design in figure 2 as an example for type II compensator design, except for output capacitor is one POSCAP 220uF with 12mΩ instead.

1.Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC} = \frac{1}{2 \times p \times \sqrt{L_{OUT} \times C_{OUT}}} = \frac{1}{2 \times p \times \sqrt{2.2uH \times 220uF}} = 7.2kHz$$

$$F_{ESR} = \frac{1}{2 \times p \times ESR \times C_{OUT}} = \frac{1}{2 \times p \times 15m\Omega \times 220uF} = 48kHz$$

2.Set R_2 equal to10kΩ. Using equation 18,

$$R_1 = \frac{10k\Omega \times 0.8V}{3.3V\text{-}0.8V} = 3.2k\Omega$$

3. Set crossover frequency at 1/10~ 1/5 of the swithing frequency, here F_O=65kHz.

4.Calculate R_3 value by the following equation.

$$R_3 = \frac{V_{OSC}}{V_{in}} \times \frac{2 \times p \times F_O \times L}{R_{ESR}} \times \frac{1}{g_m} \times \frac{R_1 + R_2}{R_1}$$
$$= \frac{2V}{12} \times \frac{2 \times p \times 65kHz \times 2.2uH}{15m\Omega} \times \frac{1}{2.5mA/V} \times \frac{3.2k\Omega + 10k\Omega}{3.2k\Omega}$$
$$= 16.5k\Omega$$

Choose R_3 =16.2kΩ.

5. Calculate C_1 by setting compensator zero F_Z at 75% of the LC double pole.

$$C_1 = \frac{1}{2 \times p \times R_3 \times F_z}$$
$$= \frac{1}{2 \times p \times 16.2k\Omega \times 0.75 \times 7.2kHz}$$
$$= 1.8nF$$

Choose C_1=1.8nF.

6. Calculate C_2 by setting compensator pole F_p at half the swithing frequency.

$$C_2 = \frac{1}{p \times R_3 \times F_s}$$
$$= \frac{1}{p \times 16.2k\Omega \times 600kHz}$$
$$= 33pF$$

Choose C_1=33pF.

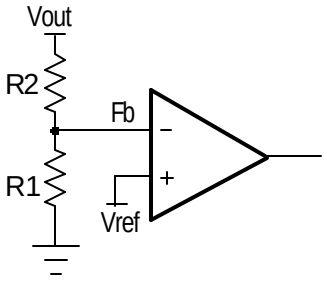
Output Voltage Calculation

Output voltage is set by reference voltage and external voltage divider. The reference voltage is fixed at 0.8V. The divider consists of two ratioed resistors so that the output voltage applied at the Fb pin is 0.8V when the output voltage is at the desired value. The following equation and picture show the relationship between V_{OUT} , V_{REF} and voltage divider.

$$R_1 = \frac{R_2 \times V_{REF}}{V_{OUT} - V_{REF}} \quad ...(18)$$

where R_2 is part of the compensator, and the value of R_1 value can be set by voltage divider.

Choose R_2=10kΩ, to set the output voltage at 1.6V, the result of R_1 is 10kΩ.



Voltage divider

Figure 13 - Voltage divider

In general, the minimum output load impedance including the resistor divider should be less than 5kΩ to prevent overcharge the output voltage by leakage current (e.g. Error Amplifier feedback pin bias current). A minimum load for 5kΩ less (<1/16w for most of application) is recommended to put at the output. For example, in this application,

Vout=1.6V

The power loss is 1/16W less

$R_{LOAD} = 1.6V \times 1.6V/(1/16W) = 40\Omega$

Select minimum load is 1kΩ should be good enough.

Input Capacitor Selection

Input capacitors are usually a mix of high frequency ceramic capacitors and bulk capacitors. Ceramic capacitors bypass the high frequency noise, and bulk capacitors supply current to the MOSFETs. Usually 1uF ceramic capacitor is chosen to decouple the high frequency noise. The bulk input capacitors are decided by voltage rating and RMS current rating. The RMS current in the input capacitors can be calculated as:

$$I_{RMS} = I_{OUT} \times \sqrt{D} \times \sqrt{1 - D}$$
$$D = \frac{V_{OUT}}{V_{IN}} \quad ...(19)$$

V_{IN} = 12V, V_{OUT}=3.3V, I_{OUT}=6A, using equation (19), the result of input RMS current is 2.68A.

For higher efficiency, low ESR capacitors are recommended. One Sanyo OSCON SP series 16SP100M 16V 100uF with 2.89A is chosen as input bulk capacitor.

Power MOSFETs Selection

The NX2211 requires two N-Channel power MOSFETs. The selection of MOSFETs is based on maximum drain source voltage, gate source voltage, maximum current rating, MOSFET on resistance and power dissipation. The main consideration is the power loss contribution of MOSFETs to the overall converter efficiency. In this design example,one Fairchild FDS6294($V_{DS=}$30V, I_D =13A,R_{DSON} =14.4mΩ,Q_{GATE}=10nC) and one Fairchild FDS6676($V_{DS=}$30V, I_D =14.5A,R_{DSON} =8mΩ,Q_{GATE}=45nC) are used.

There are three factors causing the MOSFET power loss:conduction loss, switching loss and gate driver loss.

Gate driver loss is the loss generated by discharging the gate capacitor and is dissipated in driver circuits. It is proportional to frequency and is defined as:

$$P_{gate} = (Q_{HGATE} \times V_{HGS} + Q_{LGATE} \times V_{LGS}) \times F_S \quad ...(20)$$

where Q_{HGATE} is the high side MOSFETs gate charge, Q_{LGATE} is the low side MOSFETs gate charge, V_{HGS} is the high side gate source voltage, and V_{LGS} is the low side gate source voltage.

According to equation (20), P_{GATE} =0.17W. This power dissipation should not exceed maximum power dissipation of the driver device.

Conduction loss is simply defined as:

$$P_{HCON} = I_{OUT}^2 \times D \times R_{DS(ON)} \times K$$
$$P_{LCON} = I_{OUT}^2 \times (1 - D) \times R_{DS(ON)} \times K$$
$$P_{TOTAL} = P_{HCON} + P_{LCON} \quad ...(21)$$

where the $R_{DS(ON)}$ will increases as MOSFET junction temperature increases, K is $R_{DS(ON)}$ temperature dependency. As a result, $R_{DS(ON)}$ should be selected for the worst case, in which K approximately equals to 1.43 at 125°C according to datasheet. Using equation (21), the result of P_{TOTAL} is 0.5W. Conduction loss should not exceed package rating or overall system thermal budget.

Switching loss is mainly caused by crossover conduction at the switching transition. The total switching loss can be approximated.

$$P_{SW} = \frac{1}{2} \times V_{IN} \times I_{OUT} \times T_{SW} \times F_S \quad ...(22)$$

where I_{OUT} is output current, T_{SW} is the sum of T_R and T_F which can be found in mosfet datasheet, and F_S is switching frequency. Swithing loss P_{SW} is frequency dependent.

Soft Start, Enable and shut Down

The NX2211 has a digital start up. It is based on digital counter with 1024 cycles. For NX2211 with 600kHz operation, the start up time is about 1.75ms. For NX2210 with 1MHz operation, the start up time is about 1mS.

The start up of NX2211/2210 can be programmed through resistor divider at Enable pin. For example, if the input bus voltage is 12V and we want NX2211 starts when Vbus is above 8V. We can select

R2=1.24k

$$R_1 = \frac{(8V - 1.25V) \times R_2}{1.25V} = 6.8k\Omega$$

The NX2211/NX2210 can be turned off by pulling down the ENable pin by extra signal MOSFET or NPN transistor such as 2N3904 as shown in the above Figure. When Enable pin is below 1.15V, the digital soft start is reset to zero. In addition, all the high side is off and output voltage is turned off.

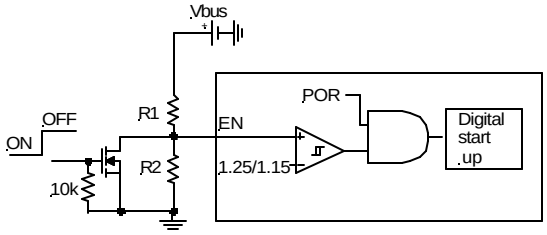


Figure 14 - Enable and Shut down NX2211/NX2210 by pulling down EN pin.

Feedback Under Voltage Shut Down

NX2211/NX2210 relies on the Feedback Under Voltage Lock Out (FB UVLO) to provide short circuit protection. Basically, NX2211/NX2210 has a comparator compares the feedback voltage with the FB UVLO threshold 0.4V.

During the normal operation, if the output is short, the feedback voltage will be lower than 0.4V and

comparator will change the state. After certain internal delay, both high side and low side driver will be turned off. The output will be latched. The normal operation should be achieved by removing the short and recycle the VCC.

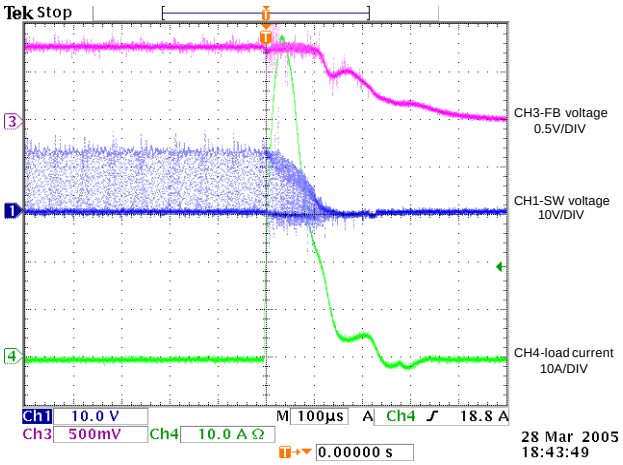


Figure 15 - Operation waveform during short

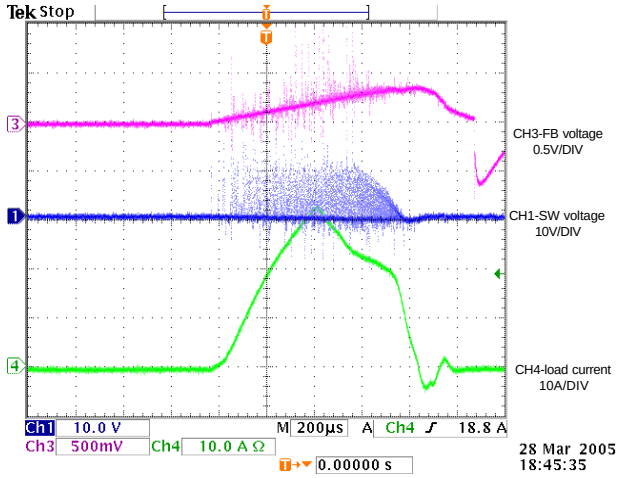


Figure 16 - Operation waveform with start up at short.

During the start up, the output voltage is discharged to zero by the synchronous FET. FB voltage starts increase from zero when digital start block operates. Before half of the start up time, the Feedback Under Voltage Lock Out comparator is disabled. After half of start up time, the Feedback UVLO comparator is enabled. The FB UVLO threshold is set to be half of voltage at the positive input of error amplifier. With this set up, if the output is short before soft start, the Feedback UVLO comparator can catch it and turn off the driver. The short circuit operation waveform during normal operation and during the soft start are shown as follows.

The Feedback UVLO can provide certain short circuit protection. However, since feedback does not have accurate information of current, this protection only provides certain level of over current protection. MOSFET should design such that it can survive with high pulse current for a short period of time. A 0.1uF or 1uF capacitor should be added on enable pin to keep enable pin high during short.

Layout Considerations

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components, make all the connection in the top layer with wide, copper filled areas. The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET, to reduce the ESR replace the single input capacitor with two parallel units. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC. In multilayer PCB use one layer as power ground plane and have a control circuit ground (analog ground), to which all signals are referenced.

The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.