

# NEXSEM

## NX2601

### DUAL SYNCHRONOUS PWM CONTROLLER WITH NMOS LDO CONTROLLER

PRELIMINARY DATA SHEET

#### DESCRIPTION

The NX2601 controller IC is a dual channel synchronous Buck controller IC designed for step down DC to DC converter applications. It provides two channel PWM controller with 180 degree out of phase as well as a LDO controller. NX2601 has programmable frequency from 200kHz to 1MHz. The NX2601 offers three enable pin which are ideal for different power sequence requirement. Adaptive driver provides optimized efficiency while maintain sufficient deadband. Other features of the device are; Internal digital soft start; external VCC Bias regulator which is ideal for high voltage application; Vcc undervoltage lock out; Enable pin available; Three individual digital soft start; Hiccup current limit, etc.

#### FEATURES

- Two channel PWM with out of phase operation
- Individual digital soft start for two PWM output and LDO controller
- Bus voltage operation from 4V to 25V
- Hiccup Current limit by sensing Rdson of MOSFET
- Adjustable frequency
- Adaptive deadband time
- Three enable pin available
- 32 leads MLPQ package

#### APPLICATIONS

- Graphic Card on board converters
- Vddq Supply in mother board applications
- On board DC to DC such as 12V to 3.3V, 2.5V or 1.8V
- Hard Disk Drive

#### TYPICAL APPLICATION

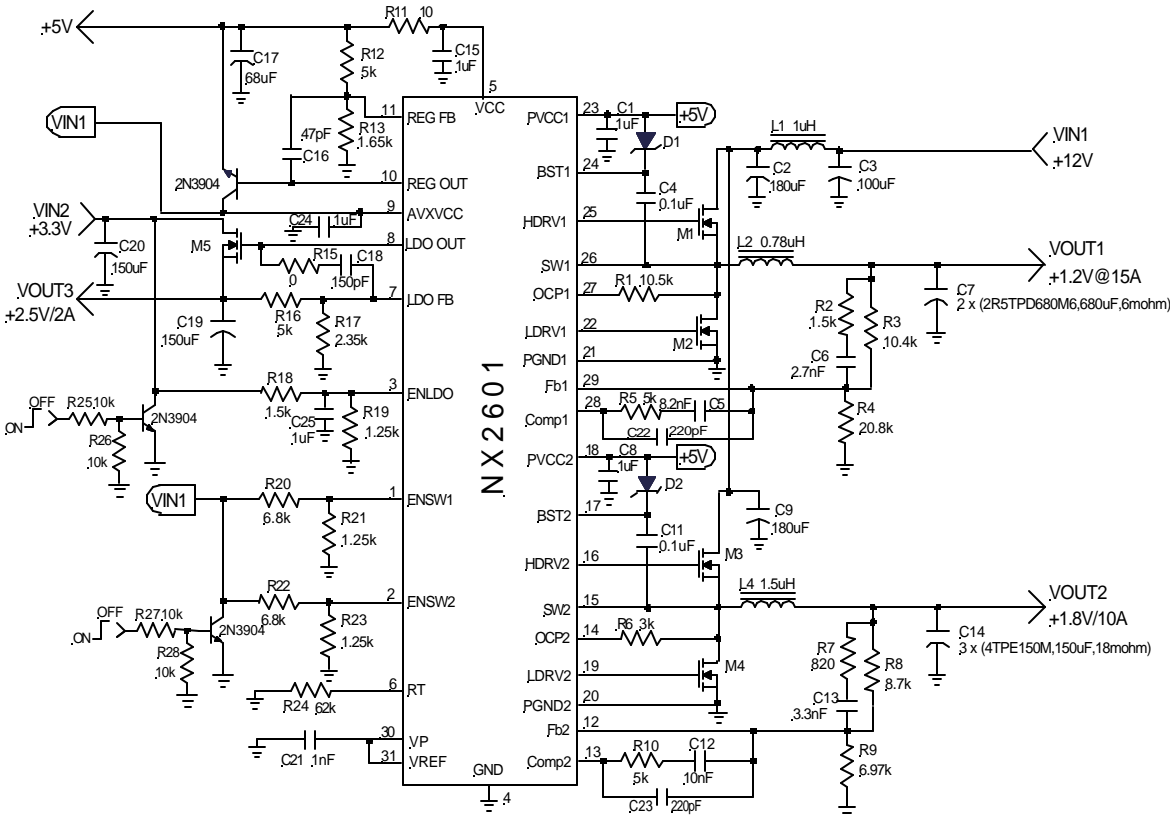


Figure1 - Typical application of 2601

PATENT PENDING

#### ORDERING INFORMATION

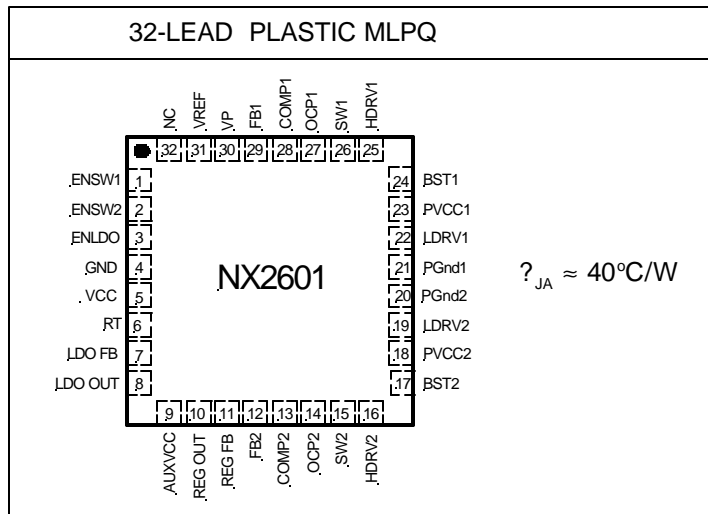
Device	Temperature	Package	Frequency
NX2601CSTR	0 to 70°C	MLPQ-32L	200kHz to 1MHz

## ABSOLUTE MAXIMUM RATINGS

Vcc,PVcc & BST to SW voltage .....	6.5V
BST Voltage .....	35V
SW .....	-5V(Note1) to 35V
AUXVCC .....	35V
All other pins .....	GND to Vcc+0.3V
Storage Temperature Range .....	-65°C To 150°C
Operating Junction Temperature Range .....	-40°C To 125°C

CAUTION: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## PACKAGE INFORMATION



## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc = 5V, V<sub>BST</sub>-V<sub>SW</sub>=5V, ENSW1=HIGH, ENSW2=HIGH, ENLDO=HIGH, and T<sub>A</sub> = 0 to 70°C. Typical values refer to T<sub>A</sub> = 25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
<b>Reference Voltage</b>						
FB Voltage	V <sub>REF</sub>	4.5 < Vcc < 5.5		0.800		v
FB Voltage Line Regulation				0.2		%
<b>Vcc Supply Voltage</b>						
Vcc Voltage Range	V <sub>CC</sub>		4.5	5.0	5.5	v
Vcc Static Supply Current	I <sub>CC_STA</sub>	Outputs not switching		2.0		mA
Vcc Dynamic Supply Current	I <sub>CC_DYN</sub>	Freq=600kHz, C <sub>LOAD</sub> = 3300pF		TBD		mA
V <sub>BST</sub> Voltage Range	V <sub>BST</sub>		4.5	5.0	5.5	v
V <sub>BST</sub> Static Supply Current	I <sub>BST_STA</sub>	Outputs not switching		2.0		mA
V <sub>BST</sub> Dynamic Supply Current	I <sub>BST_DYN</sub>	Freq = 600KHz, C <sub>LOAD</sub> = 3300pF		TBD		mA

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
<b>Under Voltage Lockout</b>						
UVLO Threshold - V <sub>CC</sub>	V <sub>CC_UVLO</sub>	Supply Ramping Up		4		V
UVLO Hysteresis - V <sub>CC</sub>	V <sub>CC_HYST</sub>	Supply Ramping Down		0.2		V
UVLO Threshold - V <sub>AUXVCC</sub>	V <sub>AUX_UVLO</sub>	Supply Ramping Up		9.6		V
UVLO Hysteresis - V <sub>AUXVCC</sub>	V <sub>AUX_HYST</sub>	Supply Ramping Down		1		V
<b>Error Amplifiers</b>						
Open Loop Gain				65		dB
Input Bias Current				TBD		nA
Input Offset Voltage				TBD		mV
Gain-Bandwidth Product	GBWP	GBNT(Note 1)		TBD		MHz
Slew Rate	SR	GBNT(Note 1)		TBD		V/μs
<b>Oscillator</b>						
Frequency	F <sub>S</sub>	Rt=TBD,measured at the output drive		600		KHz
Ramp Amplitude	V <sub>RAMP</sub>			1		V
<b>Output Drivers</b>						
Rise Time	T <sub>RISE</sub>	Cl <sub>oad</sub> = 1500pF		50		nS
Fall Time	T <sub>FALL</sub>	Cl <sub>oad</sub> = 1500pF		50		nS
Dead Band Time	T <sub>dead</sub>			250		nS
Max Duty Cycle	D <sub>max</sub>	FB = 0.6V		95		%
Min Duty Cycle	D <sub>min</sub>	FB = 1V				%
<b>EN &amp; SS</b>						
Soft Start Time	T <sub>SS</sub>	Fs=600KHz		3.41		mS
Enable Threshold Voltage				1.2		V
Enable Hysterises		Enable ramp up		100		mV
<b>LDO Controller</b>						
FB Pin Bias Current			-0.2	0	0.2	μA
Reg <sub>out</sub> Output Voltage High		AUXVCC=12V	9.5	10.3		V
Reg <sub>out</sub> Output Voltage Low				0.1	1	V
High Output Source Current			0.7	1.4		mA
Low Output Sink Current			0.9	1.4		mA
Open Loop Gain		GBNT(Note2)	50			dB

Note 1: 500ns transient. This pin can withstand -1V DC.

Note 2: This parameter is guaranteed by design but not tested in production(GBNT).

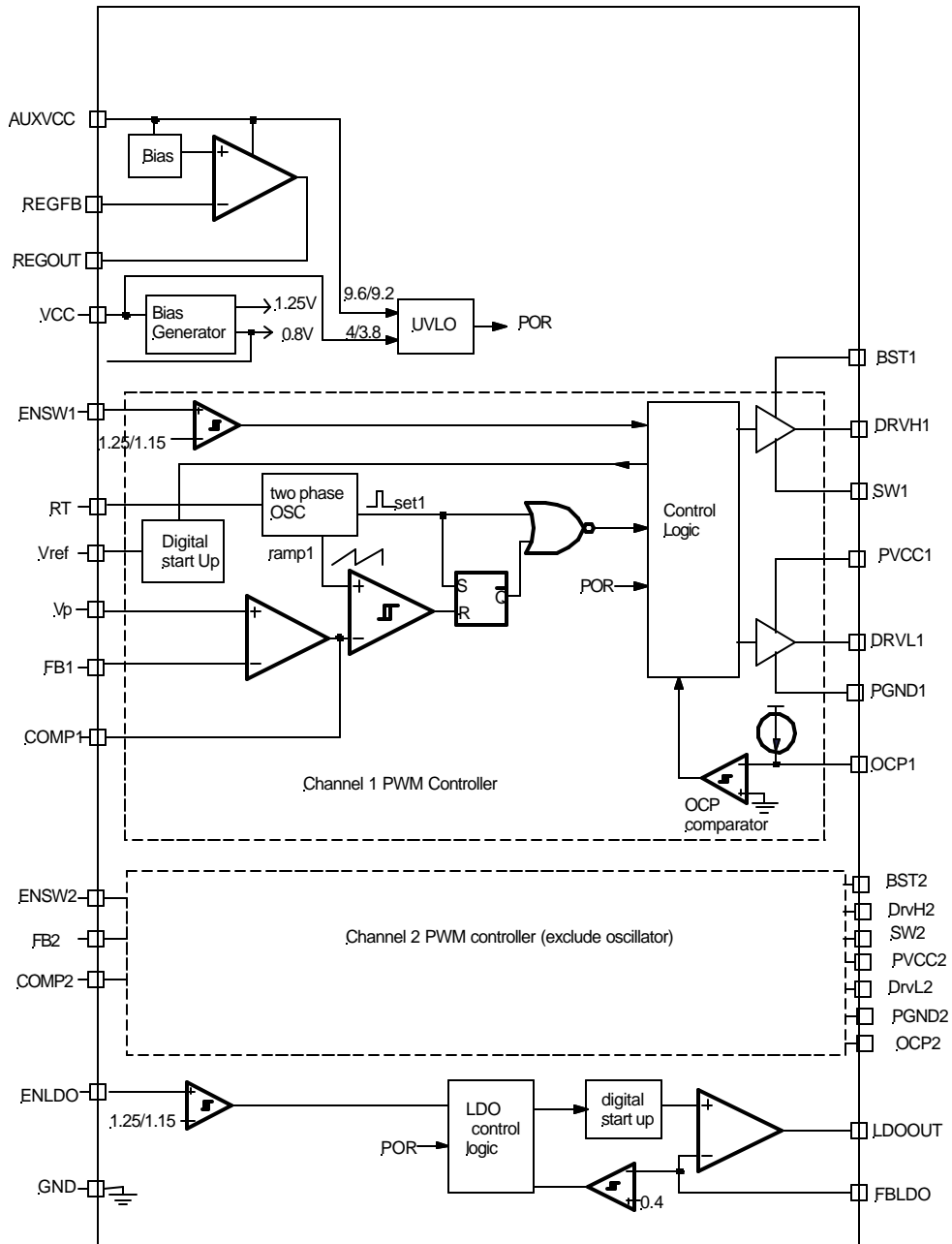
## PIN DESCRIPTIONS

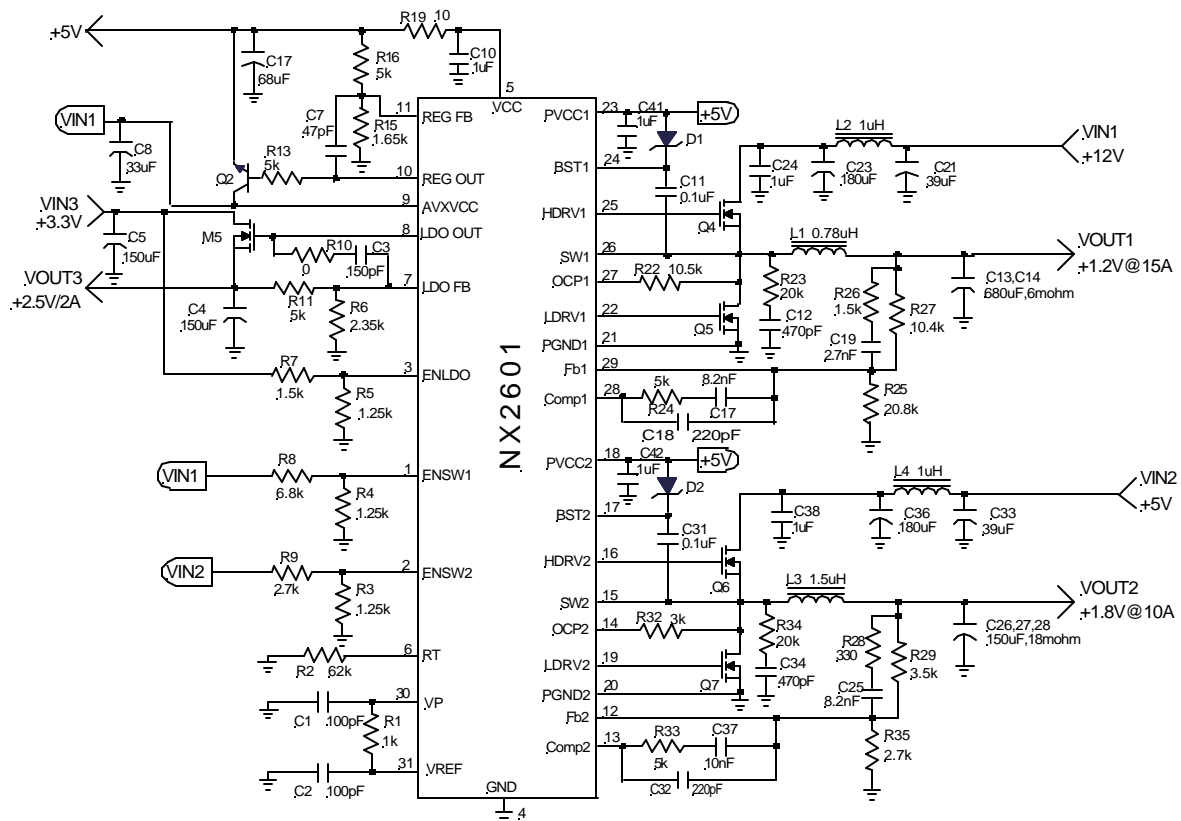
PIN #	PIN SYMBOL	PIN DESCRIPTION
1	ENSW1	A resistor divider is connected from the respective switcher BUS voltages to these pins that holds off the controllers soft start until this threshold is reached. An external low cost MOSFET or NPN transistor can be connected to this pin for external enable control.
2	ENSW2	
3	ENLDO	A resistor divider is connected from the LDO bus voltage to this pin that holds off the LDO soft start until this threshold is reached. An external low cost MOSFET can be connected to this pin for external enable control.
4	GND	Analog ground.
5	VCC	IC's supply voltage. This pin biases the internal logic circuits. A high freq 1uF ceramic capacitor is placed as close as possible to and connected to this pin and ground pin.
6	RT	Oscillator's frequency can be set by using an external resistor from this pin to GND. This frequency is the master clock frequency which is internally divided by two to set each controller frequency.
7	LDO FB	LDO controller feedback input. If the LDOFB pin is pulled below $0.5 \cdot V_{ref}$ , an internal comparator after certain delay and pulls down LDOOUT pin and initiates the HICCUP circuitry. During the startup this latch is not activated, allowing the LDOFB pin to come up and follow the Soft started $V_{ref}$ voltage.
8	LDO OUT	LDO controller output. This pin is controlling the gate of an external NCH MOSFET. The maximum rating of this pin is 16V.
9	AVXVCC	This pin is the supply voltage for the LDO controller as well as the 5V regulator controller that regulates the voltage at $V_{cc}$ derived from the BUS voltage. The maximum voltage applied to this pin is 24V.
10	REGOUT	The output of the 5V regulator controller that drives a low current low cost external BIPOLAR transistor or an external MOSFET to regulate the voltage at $V_{cc}$ pin derived from BUS voltage. This eliminates an otherwise external regulator needed in applications where 5V is not available.
11	REGFB	Feedback pin of the 5V regulator controller. A resistor divider is connected from the output of the 5V regulator to this pin to complete the loop.
12	FB2	This pin is the error amplifiers inverting input. These pins are connected via resistor dividers to the output of the switching regulators to set the output DC voltage.
29	FB1	
13	COMP2	These pins are the outputs of error amplifiers and are used to compensate the respective voltage control feedback loops.
28	COMP1	

## PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
14	OCP2	This pin is connected to the drain of the external low side MOSFET and is the input of the over current protection(OCP) comparator. An internal current source which equals 1.25V divided by Rt resistor is flow to the external resistor which sets the OCP voltage across the Rds-on of the low side MOSFET. Current limit point is this voltage divided by the Rds-on. Once this threshold is reached the Hdrv and Ldrv pins are switched low and an internal hiccup circuit is set that recycles the soft start circuit after 2048 switching cycles.
27	OCP1	
15	SW2	These pins are connected to source of high side FETs and provide return path for the high side drivers. They are also used to hold the low side drivers low until this pin is brought low by the action of high side turning off. LDRVs can only go high if SW is below 1V threshold .
26	SW1	
16	HDRV2	High side gate driver outputs.
25	HDRV1	
17	BST2	This pin supplies voltage to high side FET driver. A high freq 1uF ceramic capacitor is placed as close as possible to and connected to these pins and respected SW pins.
24	BST1	
18	PVCC2	Supply voltage for the low side fet drivers. A high frequency 1uF ceramic cap must be connected from this pin to the PGND1 and PGND2 pin as close as possible to the pins.
23	PVCC1	
19	LDRV2	Low side gate driver outputs.
22	LDRV1	
20	PGND2	Power ground pin for low side drivers.
21	PGND1	
30	VP	This pin is the second error amplifier non-inverting input. This pin should be connected either to an external reference voltage (tracking application) or to the internal reference voltage provided by this device.
31	VREF	Reference voltage available. A 100pF capacitor can be connected from this pin to GND. This pin is held low until internal Vcc UVLO and the ENSW1 pin are good, allowing it to soft start.
32	NC	

## BLOCK DIAGRAM





Simplified Demo board schematic

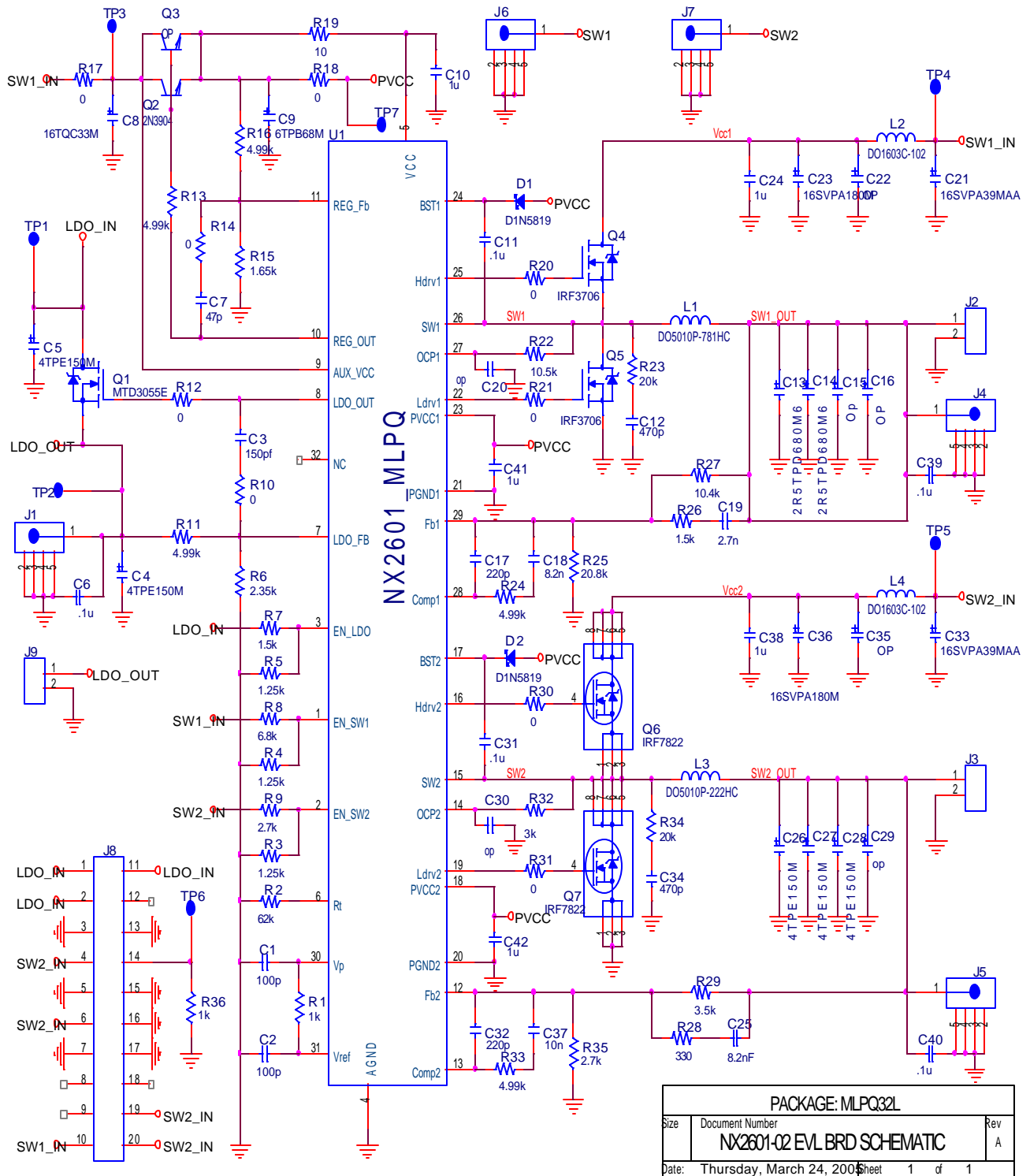


Figure 2 - Demo board schematic based on ORCAD



### Bill of Materials

Item numb	Quantity		Value	Manufacture
1	2	C2,C1	100p	
2	1	C3	150pf	
3	5	C4,C5,C26,C27,C28	4TPE150M	SANYO
4	5	C6,C11,C31,C39,C40	.1u	
5	1	C7	47p	
6	1	C8	16TQC33M	SANYO
7	1	C9	6TPB68M	SANYO
8	5	C10,C24,C38,C41,C42	1u	
9	2	C12,C34	470p	
10	2	C14,C13	2R5TPD680M6	SANYO
11	9	Q3,R14,C15,C16,C20,C22, C29,C30,C35	OP	
12	2	C17,C32	220p	
13	1	C18	8.2n	
14	1	C19	2.7n	
15	2	C21,C33	16SVPA39MAA	SANYO
16	2	C36,C23	16SVPA180M	SANYO
17	1	C25	8.2nF	
18	1	C37	10n	
19	2	D1,D2	D1N5819	
20	5	J1,J4,J5,J6,J7	SCOPE TP	Tektronics
21	3	J2,J3,J9	CON2	
22	1	J8	CON20B	
23	1	L1	DO5010P-781HC	Coilcraft
24	2	L2,L4	DO1603C-102	
25	1	L3	DO5010P-222HC	
26	1	Q1	MTD3055E	
27	1	Q2	2N3904	
28	2	Q4,Q5	IRF3706	International Rectifier
29	2	Q7,Q6	IRF7822	International Rectifier
30	1	R1	1k	
31	1	R2	62k	
32	3	R3,R4,R5	1.25k	
33	1	R6	2.35k	
34	2	R7,R26	1.5k	
35	1	R8	6.8k	
36	2	R35,R9	2.7k	
37	8	R10,R12,R17,R18,R20,R21, R30,R31	0	
38	5	R11,R13,R16,R24,R33	4.99k	
39	1	R15	1.65k	
40	1	R19	10	
41	1	R22	10.5k	
42	2	R34,R23	20k	
43	1	R25	20.8k	
44	1	R27	10.4k	
45	1	R28	330	
46	1	R29	3.5k	
47	1	R32	3k	
48	1	R36	10k	
49	7	TP1,TP2,TP3,TP4,TP5,TP6, TP7	TP	
50	1	U1	NX2601_MLPQ	NEXSEM INC.

## Demoboard waveforms

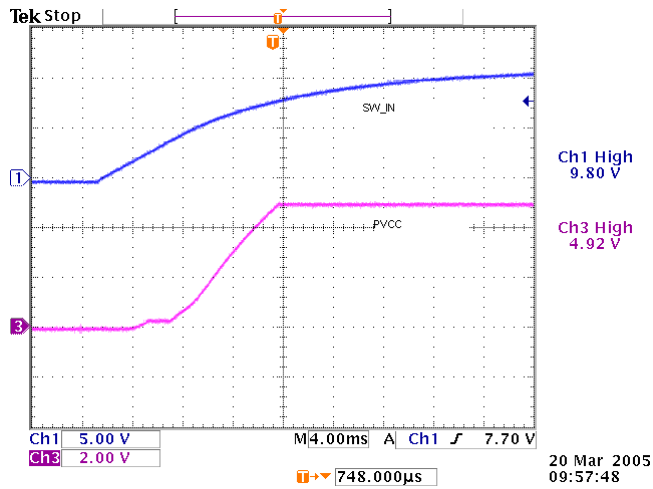


Figure 3 - Start up waveform of VCC by internal regulator. Ch1(AUXVCC), Ch3( VCC&PVCC)

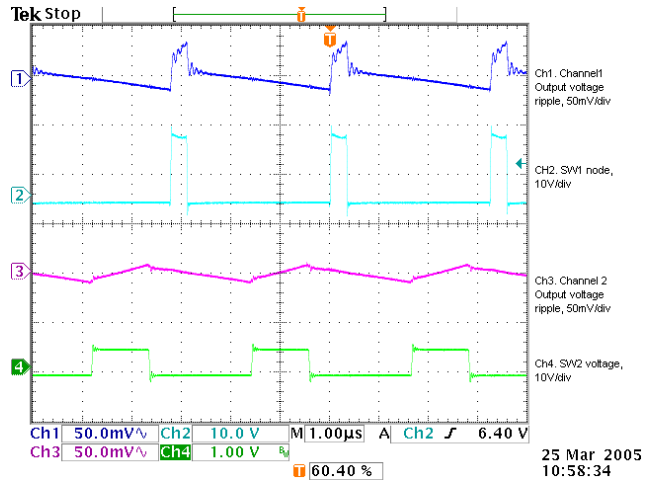


Figure 6 - Output ripple for power output CH1 and CH2

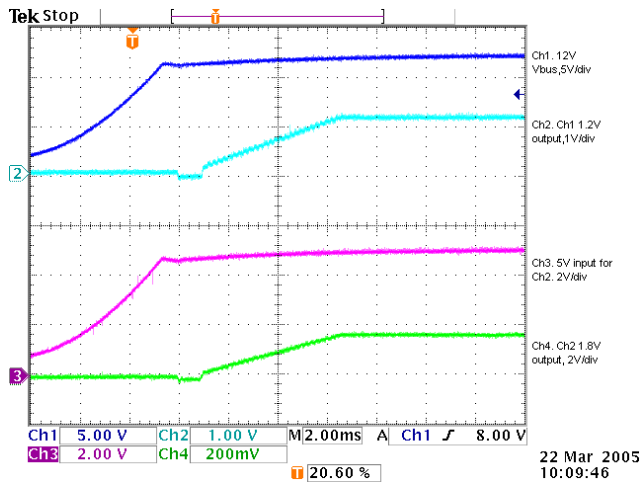


Figure 4 - Soft start for Channel 1 1.2V and channel 2 1.8V output

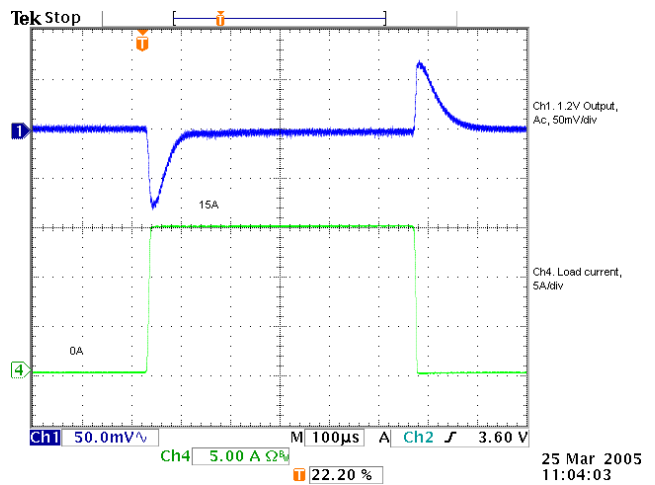


Figure 7-Transient response for first channel 1.2V output

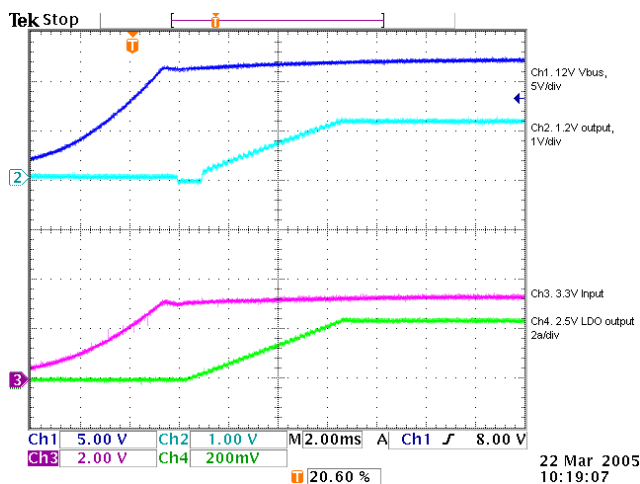


Figure 5 - Soft start for Channel 1 1.2V and LDO output

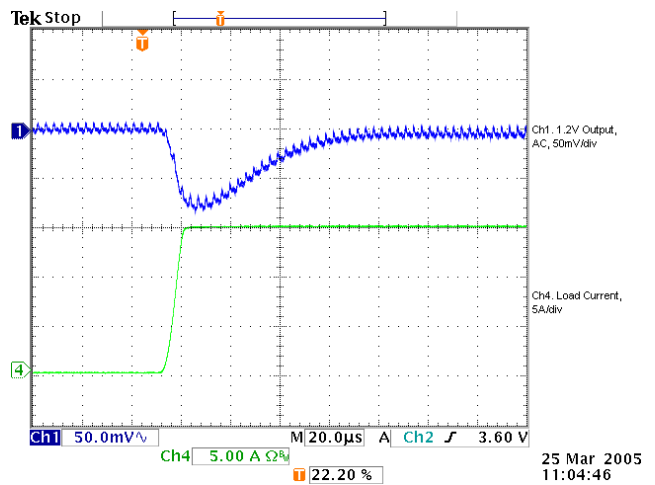


Figure 8 - transient response for Channel 1. (zoomed)

## Demo Board Waveforms (Cont')

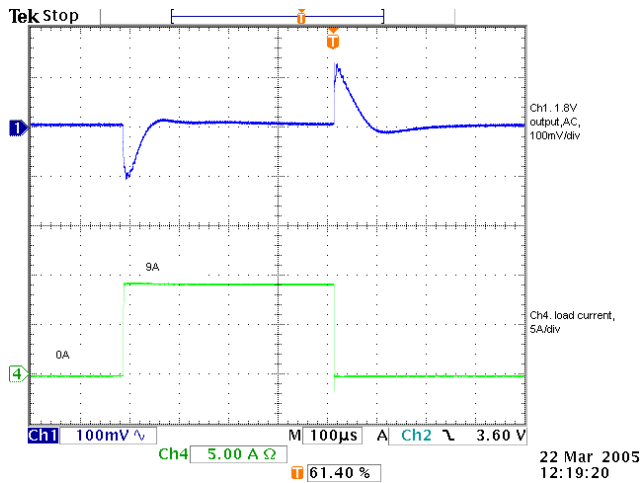


Figure 9 - Ch2 1.8V output transient 0 to 9A.

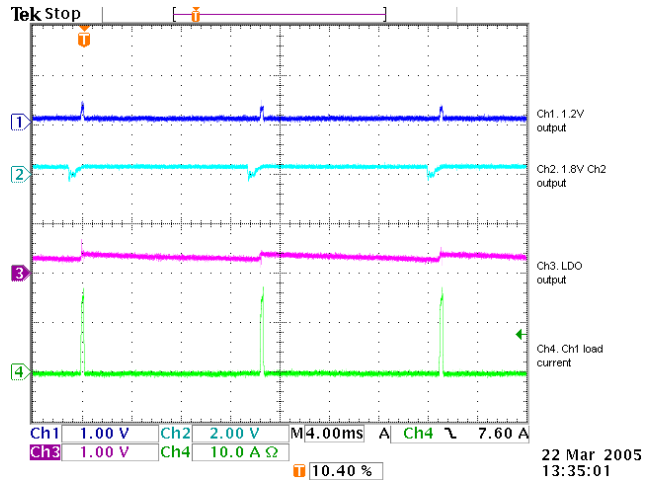


Figure 12 - Ch1 is short. All channels go into hiccup.

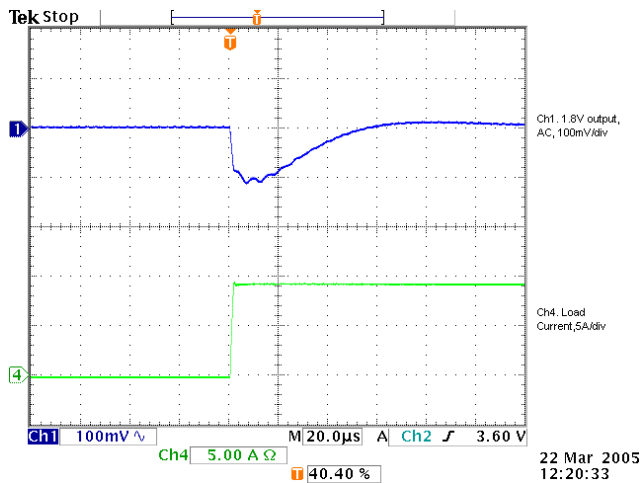


Figure 10 - Ch2 1.8V transient (zoomed)

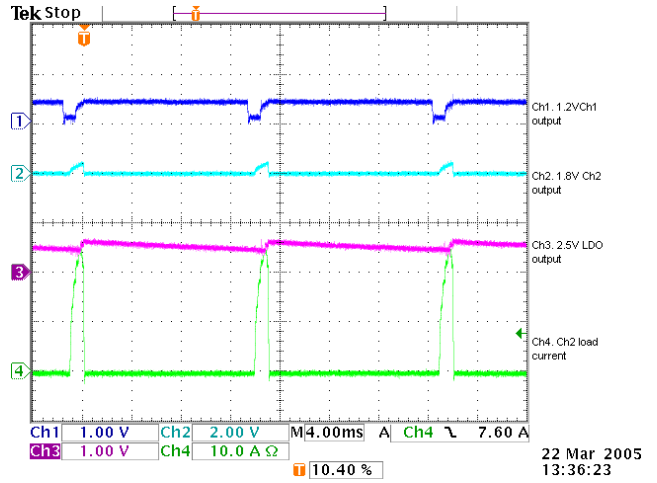


Figure 13 - Ch2 is in short. All channels are in hiccup.

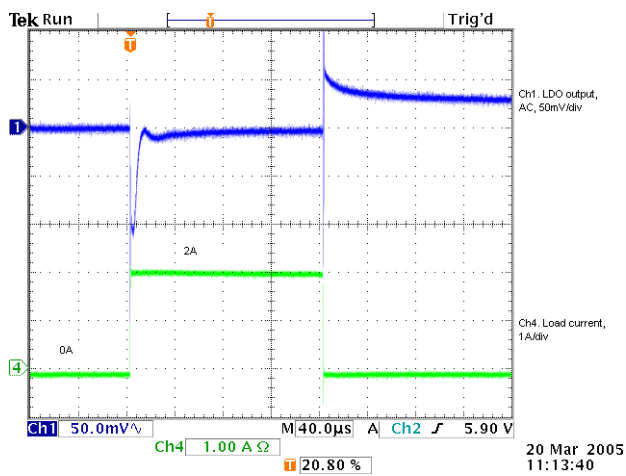


Figure 11 - Transient response for 2.5V LDO output

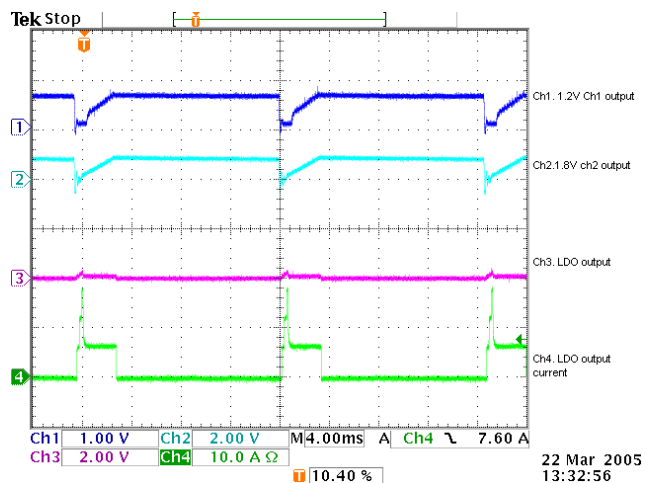


Figure 14 - LDO in short. All channels go into hiccup.

## APPLICATION INFORMATION

### Symbol Used In Application Information:

- $V_{IN}$  - Input voltage
- $V_{OUT}$  - Output voltage
- $I_{OUT}$  - Output current
- ?  $V_{RIPPLE}$  - Output voltage ripple
- $F_S$  - Switching frequency
- ?  $I_{RIPPLE}$  - Inductor current ripple

### Design Example

Power stage design requirements:

$$V_{IN}=12V$$

$$V_{OUT}=1.2V$$

$$I_{OUT}=15A$$

$$? V_{RIPPLE} \leq 20mV$$

$$? V_{TRAN} \leq 100mV @ 15A \text{ step}$$

$$F_S=300kHz$$

### Output Inductor Selection

The selection of inductor value is based on inductor ripple current, power rating, working frequency and efficiency. Larger inductor value normally means smaller ripple current. However if the inductance is chosen too large, it brings slow response and higher cost. Usually the ripple current ranges from 20% to 40% of the output current. This is a design freedom which can be decided by design engineer according to various application requirements. The inductor value can be calculated by using the following equations:

$$L_{OUT} = \frac{V_{IN} - V_{OUT}}{\Delta I_{RIPPLE}} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_S} \quad \dots(1)$$

$$I_{RIPPLE} = k \times I_{OUTPUT}$$

where k is between 0.2 to 0.4.

Select k=0.3, then

$$L_{OUT} = \frac{12V - 1.2V}{0.3 \times 15A} \times \frac{1.2V}{12V} \times \frac{1}{300kHz}$$

$$L_{OUT} = 0.8\mu H$$

Choose  $L_{OUT}=0.78\mu H$ , then coilcraft inductor DO5010P-781HC is a good choice.

Current Ripple is calculated as

$$\begin{aligned} \Delta I_{RIPPLE} &= \frac{V_{IN} - V_{OUT}}{L_{OUT}} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_S} \\ &= \frac{12V - 1.2V}{0.78\mu H} \times \frac{1.2V}{12V} \times \frac{1}{300kHz} = 4.6A \quad \dots(2) \end{aligned}$$

### Output Capacitor Selection

Output capacitor value is basically decided by the output voltage ripple, capacitor RMS current rating and load transient.

#### Based on Voltage Ripple

For electrolytic, POSCAP bulk capacitor, the ESR (equivalent series resistance) and inductor current ripple typically determines the output voltage ripple.

$$ESR_{\text{desire}} = \frac{\Delta V_{RIPPLE}}{\Delta I_{RIPPLE}} = \frac{20mV}{4.6A} = 4.3m\Omega \quad \dots(3)$$

If low ESR is required, for most of application, multiplase capacitor in parraller is better than a big capacitor. For example, for 20mV output ripple, POSCAP 2R5TPD680M6 with 6mΩ are chosen.

$$N = \frac{ESR_E \times \Delta I_{RIPPLE}}{\Delta V_{RIPPLE}} \quad \dots(4)$$

Number of Capacitor is calculated as

$$N = \frac{6m\Omega \times 4.6A}{20mV}$$

$$N = 1.38$$

The number of capacitor has to be round up to a integer. Choose N = 2.

For ceramic capacitor, the current ripple is determined by the number of capacitor instead of ESR

$$C_{OUT} = \frac{\Delta I_{RIPPLE}}{8 \times F_S \times \Delta V_{RIPPLE}} \quad \dots(5)$$

Typically, the calculated capacitance is so small that the output voltage droop during the transient can not meet the spec although ripple is small.

#### Based On Transient Requirement

Typically, the output voltage droop during tranisent is specified as

$$\Delta V_{\text{droop}} < \Delta V_{\text{tran}} @ \text{step load } \Delta I_{\text{STEP}}$$

During the tranisent, the voltage droop during the tranisent is composed of two sections. one Section is dependent on the ESR of capacitor, the other section is

a function of the inductor, output capacitance as well as input, output voltage. For example, for the overshoot when load from high load to light load with a  $\Delta I_{step}$  transient load, if assuming the bandwidth of system is high enough, the overshoot can be estimated as the following equation.

$$\Delta V_{overshoot} = ESR \times \Delta I_{step} + \frac{V_{OUT}}{2 \times L \times C_{OUT}} \times \tau^2 \quad \dots(6)$$

where  $\tau$  is the a function of capacitor, etc.

$$\tau = \begin{cases} 0 & \text{if } L \leq L_{crit} \\ \frac{L \times \Delta I_{step} - ESR \times C_{OUT}}{V_{OUT}} & \text{if } L \geq L_{crit} \end{cases} \quad \dots(7)$$

where

$$L_{crit} = \frac{ESR \times C_{OUT} \times V_{OUT}}{\Delta I_{step}} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} \quad \dots(8)$$

where  $ESR_E$  and  $C_E$  represents ESR and capacitance of each capacitor if multiple capacitors are used in parallel.

The above equation shows that if the selected output inductor is smaller than the critical inductance, the voltage droop or overshoot is only dependent on the ESR of output capacitor. For low frequency capacitor such as electrolytic capacitor, the product of ESR and capacitance is high and  $L \leq L_{crit}$  is true. In that case, the the transient spec is likely to dependent on the ESR of capacitor.

For most cases, the output capacitors are multiple capacitor in parallel. The number of capacitors can be calculated by the following

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2 \quad \dots(9)$$

where

$$\tau = \begin{cases} 0 & \text{if } L \leq L_{crit} \\ \frac{L \times \Delta I_{step} - ESR_E \times C_E}{V_{OUT}} & \text{if } L \geq L_{crit} \end{cases} \quad \dots(10)$$

For example, assume voltage droop during transient is 100mV for 15A load step.

If the POSCAP 2R5TPD680M6 (680uF, 6mohm

ESR) is used, the critical inductance is given as

$$L_{crit} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} = \frac{6m\Omega \times 680\mu F \times 1.2V}{15A} = 0.33\mu H$$

The selected inductor is 0.78uH which is bigger than critical inductance. In that case, the output voltage transient not only dependent on the ESR, but also capacitance.

number of capacitors is

$$\tau = \frac{L \times \Delta I_{step} - ESR_E \times C_E}{V_{OUT}} = \frac{0.78\mu H \times 15A}{1.2V} - 6m\Omega \times 680\mu F = 5.67\mu s$$

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2 = \frac{6m\Omega \times 15A}{100mV} + \frac{1.2V}{2 \times 0.78\mu H \times 680\mu F \times 100mV} \times (5.67\mu s)^2 = 1.3$$

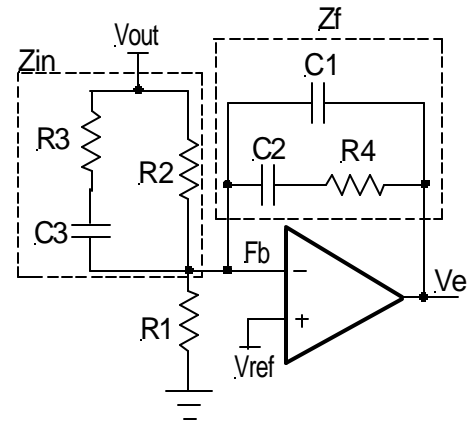
The number of capacitors has to satisfied both ripple and transient requirement. Overall, we can choose  $N=2$ .

It should be considered that the proposed equation is based on ideal case, in reality, the droop or overshoot is typically more than the calculation. The equation gives a good start. For more margin, more capacitors have to choose after the test. Typically, for high frequency capacitor such as high quality POSCAP especially ceramic capacitor, 20% up 100% (for ceramic) more capacitors have to be chosen since the ESR of capacitors is so low that the PCB parasitics can affect the results tremendously. More capacitors have to be selected to compensate these parasitic parameters.

## Compensator Design

Due to the double pole generated by LC filter of the power stage, the power system has 180° phase shift, and therefore, is unstable by itself. In order to achieve accurate output voltage and fast transient response,

compensator is employed to provide highest possible bandwidth and enough phase margin. Ideally, the Bode plot of the closed loop system has crossover frequency between 1/10 and 1/5 of the switching frequency, phase margin greater than 50° and the gain crossing 0db with -20db/decade. Power stage output capacitors usually decide the compensator type. If electrolytic capacitors are chosen as output capacitors, type II compensator can be used to compensate the system, because the zero caused by output capacitor ESR is lower than crossover frequency. Otherwise type III compensator should be chosen.



### A. Type III compensator design

For low ESR output capacitors, typically such as Sanyo OSCON and POSCAP, the frequency of ESR zero caused by output capacitors is higher than the crossover frequency. In this case, it is necessary to compensate the system with type III compensator. The following figures and equations show how to realize the type III compensator by voltage mode amplifier.

$$F_{Z1} = \frac{1}{2 \times p \times R_4 \times C_2} \quad \dots(11)$$

$$F_{Z2} = \frac{1}{2 \times p \times (R_2 + R_3) \times C_3} \quad \dots(12)$$

$$F_{P1} = \frac{1}{2 \times p \times R_3 \times C_3} \quad \dots(13)$$

$$F_{P2} = \frac{1}{2 \times p \times R_4 \times \frac{C_1 \times C_2}{C_1 + C_2}} \quad \dots(14)$$

where  $F_{Z1}, F_{Z2}, F_{P1}$  and  $F_{P2}$  are poles and zeros in the compensator. Their locations are shown in figure 15.

The transfer function of type III compensator is given by:

$$\frac{V_e}{V_{OUT}} = \frac{1}{sR_2 \times (C_2 + C_1)} \times \frac{(1 + sR_4 \times C_2) \times [1 + s(R_2 + R_3) \times C_3]}{(1 + sR_4 \times \frac{C_2 \times C_1}{C_2 + C_1}) \times (1 + sR_3 \times C_3)}$$

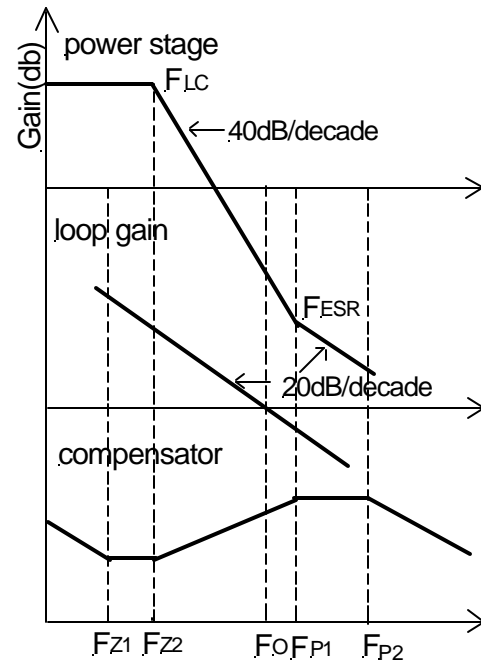


Figure 15. Type III compensator and its bode plot

The crossover frequency has to be selected as  $F_{LC} < F_O < F_{ESR}$ , and  $F_O \leq 1/10 \sim 1/5 F_s$  for type III compensator .

1. Calculate the location of LC double pole  $F_{LC}$  and ESR zero  $F_{ESR}$  .

$$F_{LC} = \frac{1}{2 \times p \times \sqrt{L_{OUT} \times C_{OUT}}}$$

$$= \frac{1}{2 \times p \times \sqrt{0.78\mu H \times 1320\mu F}}$$

$$= 4.89\text{kHz}$$

$$F_{ESR} = \frac{1}{2 \times p \times ESR \times C_{OUT}}$$

$$= \frac{1}{2 \times p \times 3\text{m}\Omega \times 1360\mu F}$$

$$= 39\text{kHz}$$

2. Set  $F_o = 25\text{kHz} < F_{ESR}$

3. Set  $F_{z1} = 0.75 \times F_{LC}$ ,  $F_{z2} = F_{LC}$ ,  $F_{p1} = F_{ESR}$  and  $F_{p2} = 0.5 \times F_s$ .

4. Set  $R_4$  equal to  $5\text{k}\Omega$ .

5. Calculate  $C_1$  and  $C_2$ .

$$C_2 = \frac{1}{2 \times p \times F_{z1} \times R_4}$$

$$= \frac{1}{2 \times p \times 0.75 \times 4.89\text{kHz} \times 5\text{k}\Omega}$$

$$= 8.7\text{nF}$$

Choose  $C_2 = 8.2\text{nF}$ .

$$C_1 = \frac{1}{2 \times p \times R_4 \times F_{p2}}$$

$$= \frac{1}{2 \times p \times 5\text{k}\Omega \times 150\text{kHz}}$$

$$= 212\text{pF}$$

Choose  $C_1 = 220\text{pF}$ .

6. Calculate  $C_3$  with the crossover frequency

$F_o = 25\text{kHz}$ .

$$C_3 = \frac{2 \times p \times V_{osc} \times F_o \times L \times C}{V_{IN} \times R_4}$$

$$= \frac{2 \times p \times 1\text{V} \times 25\text{kHz} \times 0.78\mu H \times 1360\mu F}{12\text{V} \times 10\text{k}}$$

$$= 2.78\text{nF}$$

Choose  $C_3 = 2.7\text{nF}$ .

7. Calculate  $R_2, R_3$ .

$$R_3 = \frac{1}{2 \times p \times F_{p1} \times C_3}$$

$$= \frac{1}{2 \times p \times 39\text{kHz} \times 2.7\text{nF}}$$

$$= 1.5\text{k}\Omega$$

Choose  $R_3 = 1.5\text{k}\Omega$ .

$$R_2 = \frac{1}{2 \times p \times F_{z2} \times C_3} - R_3$$

$$= \frac{1}{2 \times p \times 3.9\text{kHz} \times 2.7\text{nF}} - 1.5\text{k}\Omega$$

$$= 10.5\text{k}\Omega$$

Choose  $R_2 = 10.4\text{k}\Omega$ .

8. Calculate  $R_1$ .

$$R_1 = \frac{R_2 \times V_{REF}}{V_{OUT} - V_{REF}} = \frac{10.4\text{k}\Omega \times 0.8\text{V}}{1.2\text{V} - 0.8\text{V}} = 20.8\text{k}\Omega$$

Choose  $R_1 = 20.8\text{k}\Omega$ .

## B. Type II compensator design

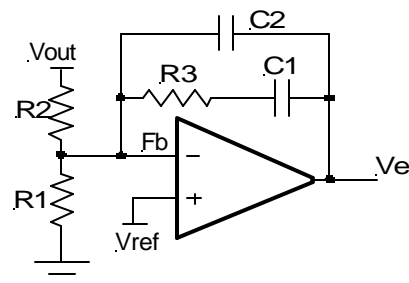
If the electrolytic capacitors are chosen as power stage output capacitors, usually the Type II compensator can be used to compensate the system.

Type II compensator can be realized by simple RC circuit as shown in figure 16.  $R_3$  and  $C_1$  introduce a zero to cancel the double pole effect.  $C_2$  introduces a pole to suppress the switching noise. The following equations show the compensator pole zero location and constant gain.

$$\text{Gain} = \frac{R_3}{R_2} \quad \dots (15)$$

$$F_z = \frac{1}{2 \times p \times R_3 \times C_1} \quad \dots (16)$$

$$F_p = \frac{1}{2 \times p \times R_3 \times C_2} \quad \dots (17)$$



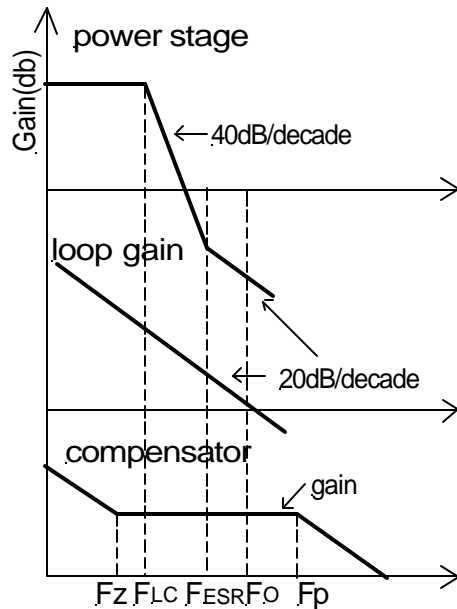


Figure 16 - Type II compensator and its bode plot

For type II compensator,  $F_o$  has to satisfy

$$F_{LC} < F_{ESR} \ll F_o \leq 1/10 \sim 1/5 F_s$$

The following parameters are used as an example for type II compensator design, three 1500uF with 19mohm Sanyo electrolytic CAP 6MV1500WGL are used as output capacitors. Coilcraft DO5010P-152HC 1.5uH is used as output inductor. The other power stage information is that:

$V_{IN}=12V$ ,  $V_{OUT}=1.2V$ ,  $I_{OUT}=15A$ ,  $F_s=200kHz$ .

1. Calculate the location of LC double pole  $F_{LC}$  and ESR zero  $F_{ESR}$ .

$$\begin{aligned} F_{LC} &= \frac{1}{2 \times p \times \sqrt{L_{OUT} \times C_{OUT}}} \\ &= \frac{1}{2 \times p \times \sqrt{1.5\mu H \times 4500\mu F}} \\ &= 1.94kHz \end{aligned}$$

$$\begin{aligned} F_{ESR} &= \frac{1}{2 \times p \times ESR \times C_{OUT}} \\ &= \frac{1}{2 \times p \times 6.33m\Omega \times 4500\mu F} \\ &= 5.6kHz \end{aligned}$$

2. Set crossover frequency  $F_o=20kHz \gg F_{ESR}$ .

3. Set  $R_2$  equal to  $10k\Omega$ . Based on output voltage, using equation 18, the final selection of  $R_1$  is  $20k\Omega$ .

4. Calculate  $R_3$  value by the following equation.

$$\begin{aligned} R_3 &= \frac{V_{OSC}}{V_{in}} \times \frac{2 \times p \times F_o \times L}{ESR} \times R_2 \\ &= \frac{1V}{12V} \times \frac{2 \times p \times 20kHz \times 1.5\mu H}{6.33m\Omega} \times 10k\Omega \\ &= 24.8k\Omega \end{aligned}$$

Choose  $R_3=24.8k\Omega$ .

5. Calculate  $C_1$  by setting compensator zero  $F_z$  at 75% of the LC double pole.

$$\begin{aligned} C_1 &= \frac{1}{2 \times p \times R_3 \times F_z} \\ &= \frac{1}{2 \times p \times 24.8k\Omega \times 0.75 \times 1.94kHz} \\ &= 4.4nF \end{aligned}$$

Choose  $C_1=4.7nF$ .

6. Calculate  $C_2$  by setting compensator pole  $F_p$  at half the switching frequency.

$$\begin{aligned} C_2 &= \frac{1}{p \times R_3 \times F_s} \\ &= \frac{1}{p \times 24.8k\Omega \times 300kHz} \\ &= 64pF \end{aligned}$$

Choose  $C_2=68pF$

## Output Voltage Calculation

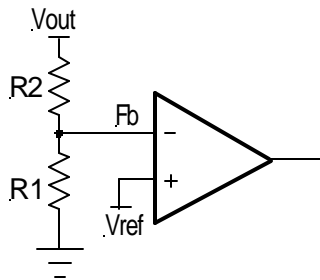
Output voltage is set by reference voltage and external voltage divider. The reference voltage is fixed at 0.8V. The divider consists of two ratioed resistors so that the output voltage applied at the Fb pin is 0.8V when the output voltage is at the desired value. The following equation and picture show the relationship between  $V_{OUT}$ ,  $V_{REF}$  and voltage divider.

$$R_1 = \frac{R_2 \times V_{REF}}{V_{OUT} - V_{REF}} \quad \dots(18)$$

where  $R_2$  is part of the compensator, and the value of  $R_1$  value can be set by voltage divider.



Choose  $R_2=10k\Omega$ , to set the output voltage at 1.8V, the result of  $R_1$  is  $8k\Omega$ .



Voltage divider

Figure 17 - Voltage divider

## Input Capacitor Selection

Input capacitors are usually a mix of high frequency ceramic capacitors and bulk capacitors. Ceramic capacitors bypass the high frequency noise, and bulk capacitors supply current to the MOSFETs. Usually 1uF ceramic capacitor is chosen to decouple the high frequency noise. The bulk input capacitors are decided by voltage rating and RMS current rating. The RMS current in the input capacitor can be calculated

$$I_{RMS} = I_{OUT} \times \sqrt{D} \times \sqrt{1-D}$$

$$D = \frac{V_{OUT}}{V_{IN}} \quad \dots(19)$$

$V_{IN} = 12V$ ,  $V_{OUT}=1.2V$ ,  $I_{OUT}=15A$ , using equation (19), the result of input RMS current is 4.5A.

For higher efficiency, low ESR capacitors are recommended.

Two Sanyon OS-CON SVPA180M 16V 180uF 29mO with 3.4A RMS rating are chosen as input bulk capacitors.

## Power MOSFETs Selection

The NX2601 requires two N-Channel power MOSFETs. The selection of MOSFETs is based on maximum drain source voltage, gate source voltage, maximum current rating, MOSFET on resistance and power dissipation. The main consideration is the power loss contribution of MOSFETs to the overall converter

efficiency. In this design example, two IRFR3706 are used. They have the following parameters:  $V_{DS}=30V$ ,  $I_D=75A$ ,  $R_{DS(ON)}=9m\Omega$ ,  $Q_{GATE}=23nC$ .

There are three factors causing the MOSFET power loss: conduction loss, switching loss and gate driver loss.

Gate driver loss is the loss generated by discharging the gate capacitor and is dissipated in driver circuits. It is proportional to frequency and is defined as:

$$P_{gate} = (Q_{HGATE} \times V_{HGS} + Q_{LGATE} \times V_{LGS}) \times F_s \quad \dots(20)$$

where  $Q_{HGATE}$  is the high side MOSFETs gate charge,  $Q_{LGATE}$  is the low side MOSFETs gate charge,  $V_{HGS}$  is the high side gate source voltage, and  $V_{LGS}$  is the low side gate source voltage.

According to equation (3),  $P_{GATE}=0.07W$ . This power dissipation should not exceed maximum power dissipation of the driver device.

Conduction loss is simply defined as:

$$P_{HCON} = I_{OUT}^2 \times D \times R_{DS(ON)} \times K$$

$$P_{LCON} = I_{OUT}^2 \times (1-D) \times R_{DS(ON)} \times K \quad \dots(21)$$

$$P_{TOTAL} = P_{HCON} + P_{LCON}$$

where the  $R_{DS(ON)}$  will increase as MOSFET junction temperature increases,  $K$  is  $R_{DS(ON)}$  temperature dependency. As a result,  $R_{DS(ON)}$  should be selected for the worst case, in which  $K$  equals to 1.4 at 125°C according to IRFR3706 datasheet. Using equation (4), the result of  $P_{TOTAL}$  is 0.54W. Conduction loss should not exceed package rating or overall system thermal budget.

Switching loss is mainly caused by crossover conduction at the switching transition. The total switching loss can be approximated.

$$P_{SW} = \frac{1}{2} \times V_{IN} \times I_{OUT} \times T_{SW} \times F_s \quad \dots(22)$$

where  $I_{OUT}$  is output current,  $T_{SW}$  is the sum of  $T_R$  and  $T_F$  which can be found in mosfet datasheet, and  $F_s$  is switching frequency. The result of  $P_{SW}$  is 1.5W. Switching loss  $P_{SW}$  is frequency dependent.

## Soft Start and Enable

NX2601 has two switching controller and one LDO controller. Each of them has individual digital soft start. Each channel has one enable pin for start up. When the Power Ready (POR) signal is high and the voltage at enable pin is above 1.25V, the internal digital counter starts to operate and the voltage at positive input of Error amplifier starts to increase, the feedback network will force the output voltage follows the reference and starts the output slowly. After 2048 cycles, the soft start is complete and the output voltage is regulated to the desired voltage decided by the feedback resistor divider

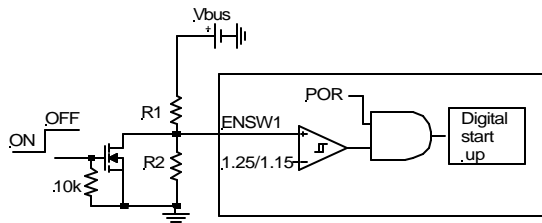


Figure 18 - Enable and Shut down the NX2601 with Enable pin.

The start up of NX2601 can be programmed through resistor divider at Enable pin. For example, for channel 1, if the input bus voltage is 12V and we want NX2601 starts when Vbus is above 8V. We can select

$$R_2 = 1.24k$$

$$R_1 = \frac{(8V - 1.25V) \times R_2}{1.25V} = 6.8k\Omega$$

The NX2601 can be turned off by pulling down the Enable pin by extra signal MOSFET as shown in the above Figure. When Enable pin (ENSW1) is below 1.15V, the digital soft start is reset to zero. In addition, all the high side is off and output voltage is turned off.

The frequency can be set by external Rt resistor. The relationship between frequency and RT pin is shown as follows.

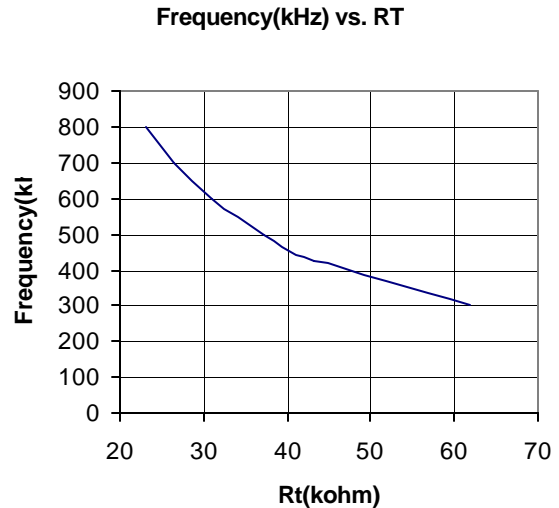


Figure 19 - Frequency versus Rt resistor

For example, for 300khz operation, Rt is about 62kohm.

## Over Current Limit Protection

Over current limit for step down converter is achieved by sensing current through the low side MOSFET. Inside NX2601, the current through Rt pin is mirrored and injecting to the pin OCP. Since the current through Rt pin is decided as

$$I_{RT} = \frac{1.25}{R_t}$$

This current is very accurate and does not change with silicon process and temperature, the over current limit tripping point can be set more accurate than traditional current source. This scheme is the property of Nexsem. When synchronous FET is on, the voltage at node SW is given as

$$V_{SW} = I_L \times R_{DSON}$$

The voltage at pin OCP is given as

$$I_{OC} \times R_{OC} + V_{SW}$$

When the voltage is below zero, the over current occurs. The over current limit can be set by the following equation

$$I_{SET} = I_{RT} \times R_{OC} / R_{DSON}$$

For example, For 20A current limit and 9mohm Rds on for IRFR3706, the OCP set resistor is calculated as

$$I_{RT} = \frac{1.25V}{62k} = 20\mu A$$

$$R_{OC} = \frac{I_{SET}}{I_{RT}} \times R_{DSON} = \frac{20A}{20\mu A} \times 9mohm = 9kohm$$

Select OCP set resistor R=10.5k.

For NX2601, if one channel goes to hiccup current limit, the other channels include LDO will go to hiccup too.

## LDO Selection Guide

NX2601 offers a LDO controller. The selection of MOSFET to meet LDO is more straight forward. The selection is that the Rds on of MOSFET should meet the dropout requirement. For example.

$$V_{LDOIN} = 3.3V$$

$$V_{LDOOUT} = 2.5V$$

$$I_{Load} = 2A$$

The maximum Rds on of MOSFET should be

$$R_{RDSON} = (V_{LDOIN} - V_{LDOOUT}) \times I_{LOAD} \\ = (3.3V - 2.5V) / 2A = 0.4\Omega$$

Most of MOSFETs can meet the requirement. More important is that MOSFET has to be selected right package to handle the thermal capability. For LDO, maximum power dissipation is given as

$$P_{LOSS} = (V_{LDOIN} - V_{LDOOUT}) \times I_{LOAD} \\ = (3.3V - 2.5V) \times 2A = 1.6W$$

Select IR MOSFET IRFR376 with 9mW R<sub>DSON</sub> is sufficient.

## LDO Compensation

The diagram of LDO controller including VCC regulator is shown in above figure. For low frequency capacitor such as electrolytic, POSCAP, OSCON, etc, The compensation parameter can be calculated as follows

$$C_c = \frac{1}{2 \times \pi \times F_o \times R_{f1}} \times \frac{g_m \times ESR}{1 + g_m \times ESR}$$

where F<sub>o</sub> is the desired loop gain.

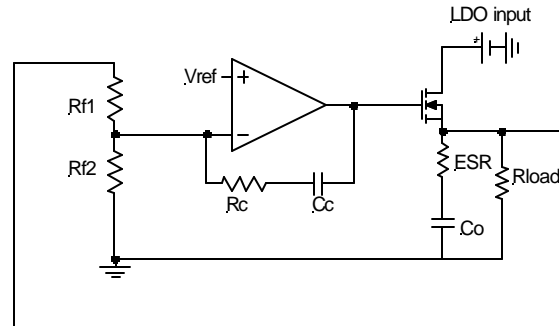


Figure 20 - NX2601 LDO controller.

Typically, F<sub>o</sub> has to be higher than zero caused by ESR. F<sub>o</sub> is typically around several tens kHz to a few hundred kHz. For this example, we select Fo=100KHz. g<sub>m</sub> is the forward trans-conductance of MOSFET.

For IRFR3706, g<sub>m</sub>=53.

Select Rf1=5kohm.

Output capacitor is Sanyo POSCAP 4TPE150MI with 150uF, ESR=18mohm.

$$C_c = \frac{1}{2 \times \pi \times 100kHz \times 5k\Omega} \times \frac{53 \times 18m\Omega}{1 + 53 \times 18m\Omega} = 155pF$$

Choose C<sub>c</sub>=150pF.

For electrolytic or POSCAP, R<sub>c</sub> is typically selected to be zero.

R<sub>f2</sub> is determined by the desired output voltage

$$R_{f2} = R_{f1} \times V_{REF} / (V_{LDOOUT} - V_{REF}) \\ = 5k\Omega \times 0.8V / (2.5V - 0.8) = 2.35k\Omega$$

Choose R<sub>f2</sub>=2.34kΩ.

## Current Limit for LDO

Current limit of LDO is achieved by sensing the LDO feedback voltage. When LDO\_FB pin is below 0.4V, the IC goes into hiccup mode. The IC will turn off all the channel (Channel 1 and Channel 2) for 2096 cycles and start to restart system again.

## Layout Considerations

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components, make all the connection in the top layer with wide, copper filled areas. The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET, to reduce the ESR replace the single input capacitor with two parallel units. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC. In multilayer PCB use one layer as power ground plane and have a control circuit ground (analog ground), to which all signals are referenced.

The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

## TYPICAL APPLICATIONS

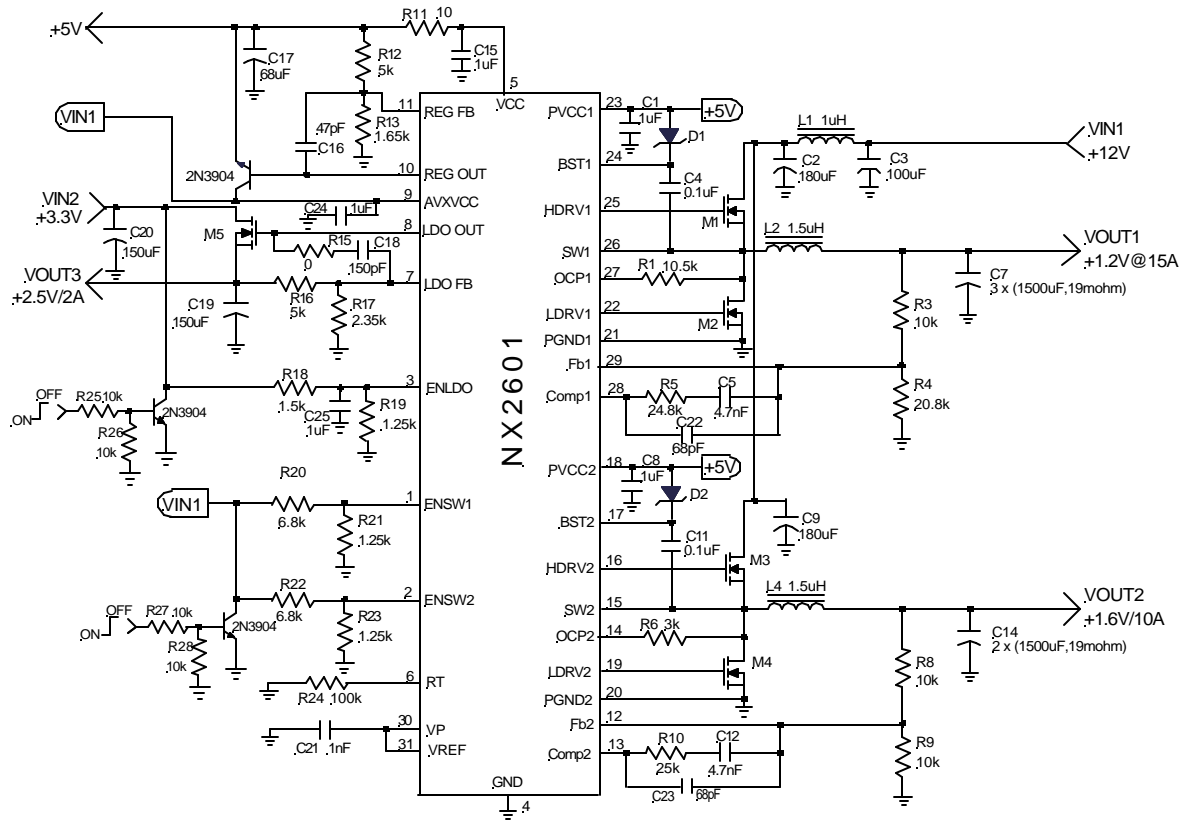


Figure 21 - NX2601 application with electrolytic capacitors as output capacitors

## TYPICAL APPLICATIONS(cont')

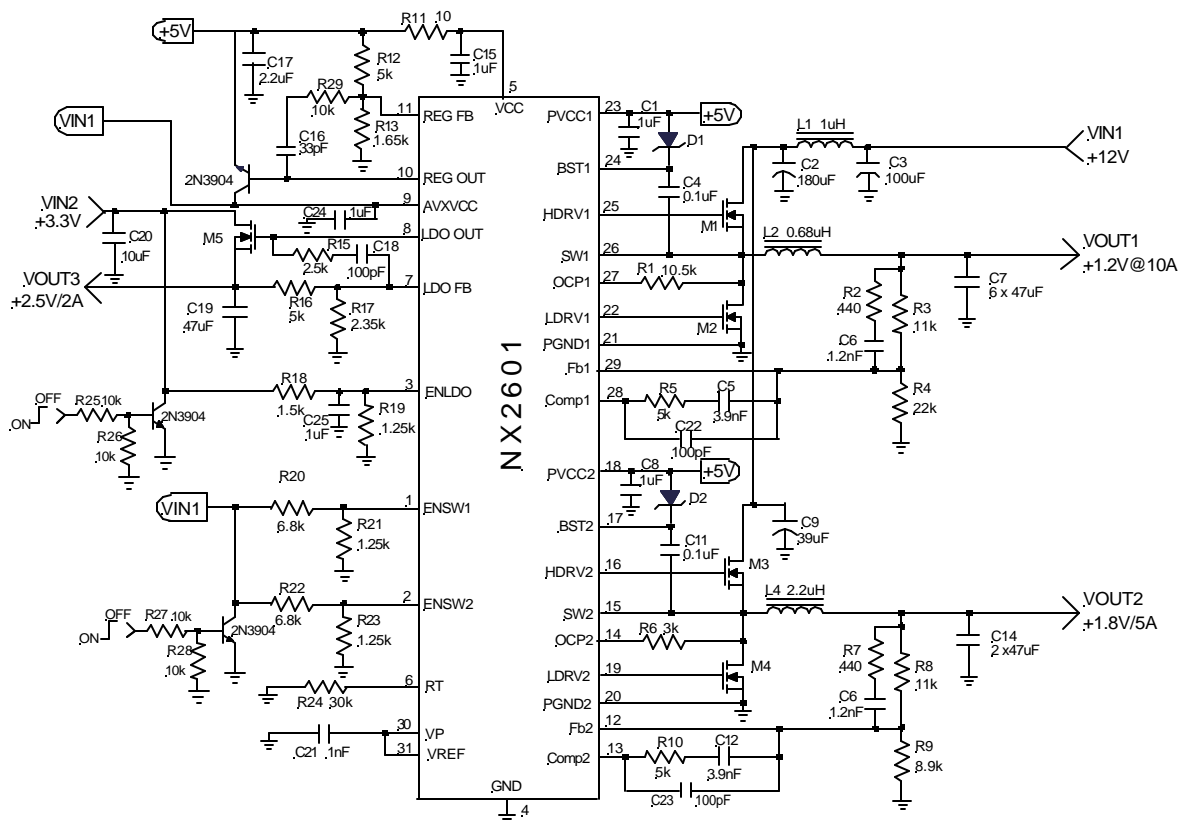


Figure 22 - NX2601 application with ceramic capacitors as output capacitors

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