General Purpose 2/3-Phase PWM Controller for High-Density Power Supply

General Description

The RT8800/B are general purpose multi-phase synchronous buck controllers dedicating for high density power supply regulation. The parts implement 2, and 3 buck switching stages operating in interleaved phase set automatically. The output voltage is regulated and controlled following the input voltage of FB pin. With such a single analog control, the RT8800/B provide a simple, flexible, wide-range and extreme cost-effective high-density voltage regulation solutions for various high-density power supply application. The RT8800/B multi-phase architecture provide high output current while maintaining low power dissipation on power devices and low stress on input and output capacitors. The high equivalent operating frequency also reduces the component dimension and the output voltage ripple in load transient.

RT8800/B implement both voltage and current loops to achieve good regulation, response and power stage thermal balance. The RT8800/B apply the time sharing DCR current sensing technology newly as well; with such a topology, the RT8800/B extract the DCR of output inductor as sense component to deliver a more precise load line regulation and better thermal balance capability. Moreover, the parts monitor the output voltage for over-current and over-voltage protection; Soft-start and programmable under-voltage lockout are also provided to assure the safety of power system.

Applications

- Desktop CPU core power
- Low Output Voltage, High power density DC-DC Converters
- Voltage Regulator Modules

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area, otherwise visit our website for detail.

Features

- **5V Power Supply Voltage**
- **2/3-Phase Power Conversion with Automatic Phase Selection (RT8800 : 2/3-Phase, RT8800B : 2-Phase)**
- **Output Voltage Controlled by External Reference Voltage**
- **Precise Core Voltage Regulation**
- **Power Stage Thermal Balance by DCR Current Sensing**
- **Extreme Low-Cost, Lossless Time Sharing Current Sensing**
- **Internal Soft-start**
- **Hiccup Mode Over-Current Protection**
- **Over-Voltage Protection**
- **Adjustable Operating Frequency and Typical at 300kHz Per Phase**
- **Power Good indication**
- **Small 16-Lead VQFN Package (For RT8800 only)**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Ordering Information

RT8800/B □ □

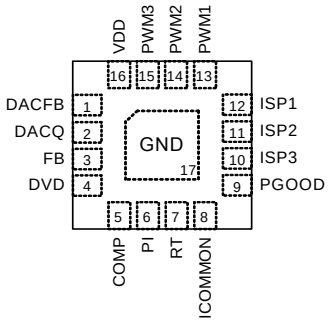
- Package Type
  - QV : VQFN-16L 3x3 (V-Type)
  - S : SOP-16
- Operating Temperature Range
  - P : Pb Free with Commercial Standard
  - G : Green (Halogen Free with Commercial Standard)
- 2-Phase
- 2/3-Phase

Note :

- Richtek Pb-free and Green products are :
  - RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
  - Suitable for use in SnPb or Pb-free soldering processes.
  - 100% matte tin (Sn) plating.

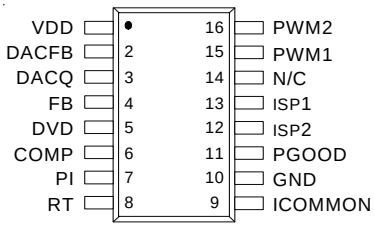
Pin Configurations

(TOP VIEW)



VQFN-16L 3x3

RT8800



SOP-16

RT8800B

Functional Pin Description

DACFB

Negative input of internal buffer amplifier for reference voltage regulation. The pin voltage is locked at internal V_{REF} = 0.8V by properly close the buffer amplifier feedback loop.

DACQ

The pin is defined as the output of internal buffer amplifier for reference voltage regulation.

FB

The pin is defined as the inverting input of internal error amplifier.

DVD

The pin is defined as a programmable power UVLO detection input. Trip threshold = 0.8V at V_{DVD} rising.

COMP

The pin is defined as the output of the error amplifier and the input of all PWM comparators.

PI

The pin is defined as the positive input of the error amplifier.

RT

Switching frequency setting. Connect this pin to GND with a resistor to set the frequency.

ICOMMON

Common negative input of current sense amplifiers for all three channels.

PGOOD

Output power-good indication. The signal is implemented as an output signal with open-drain type.

ISP1 , ISP2 , ISP3

Current sense positive inputs for individual converter channel current sense.

PWM1 , PWM2 , PWM3

PWM outputs for each phase switching drive.

VDD

Chip power supply. Connect this pin to a 5V supply.

GND

Chip power ground.

Exposed Pad (17) (RT8800)

The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Typical Application Circuit

(Note : The inductor' s DCR value must be large than 0.3mΩ

: X7R/R-type capacitor is required for all time constant setting capacitor of DCR sensing.)

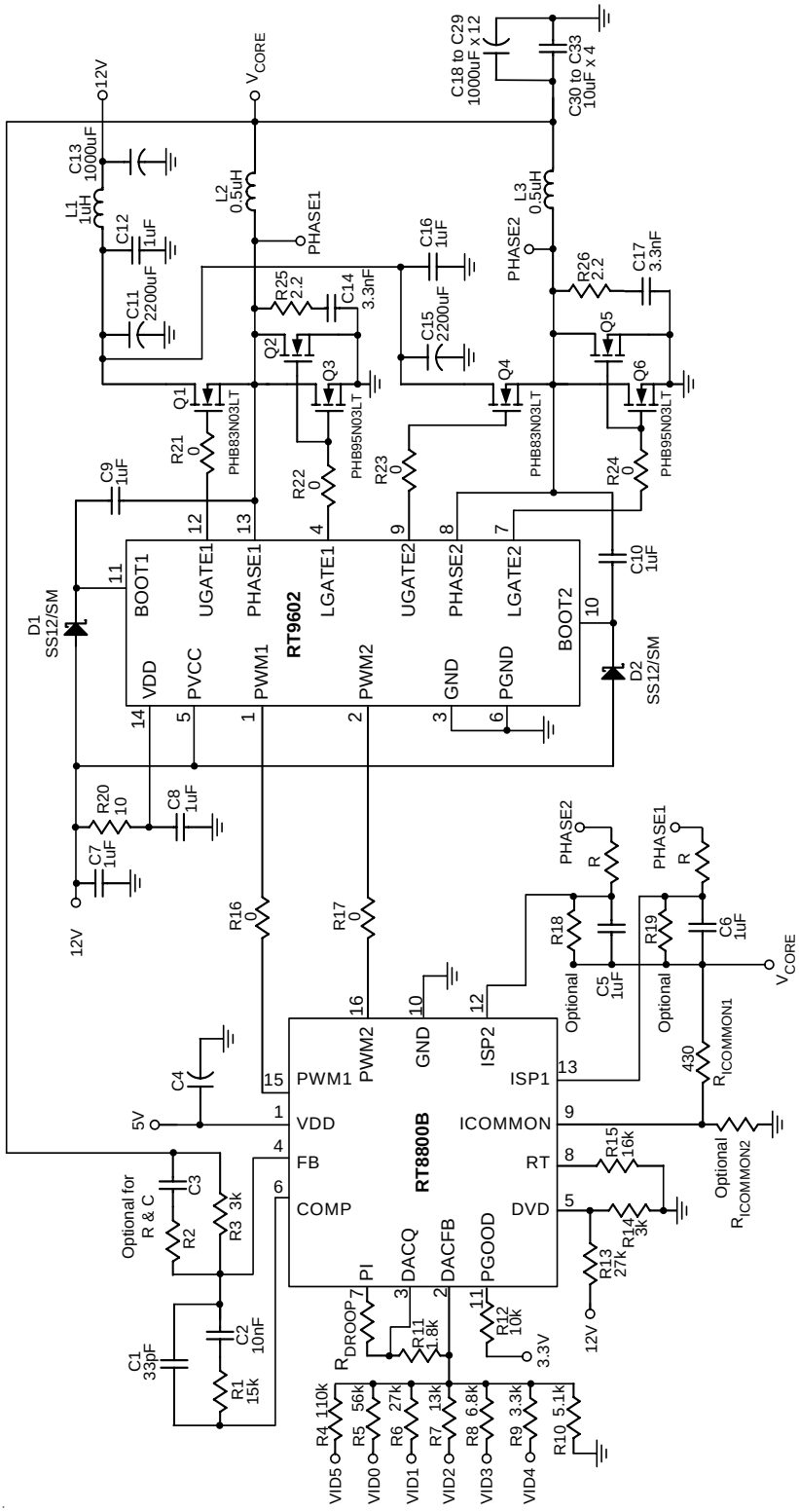


Figure A. 2-phase with resistive DAC

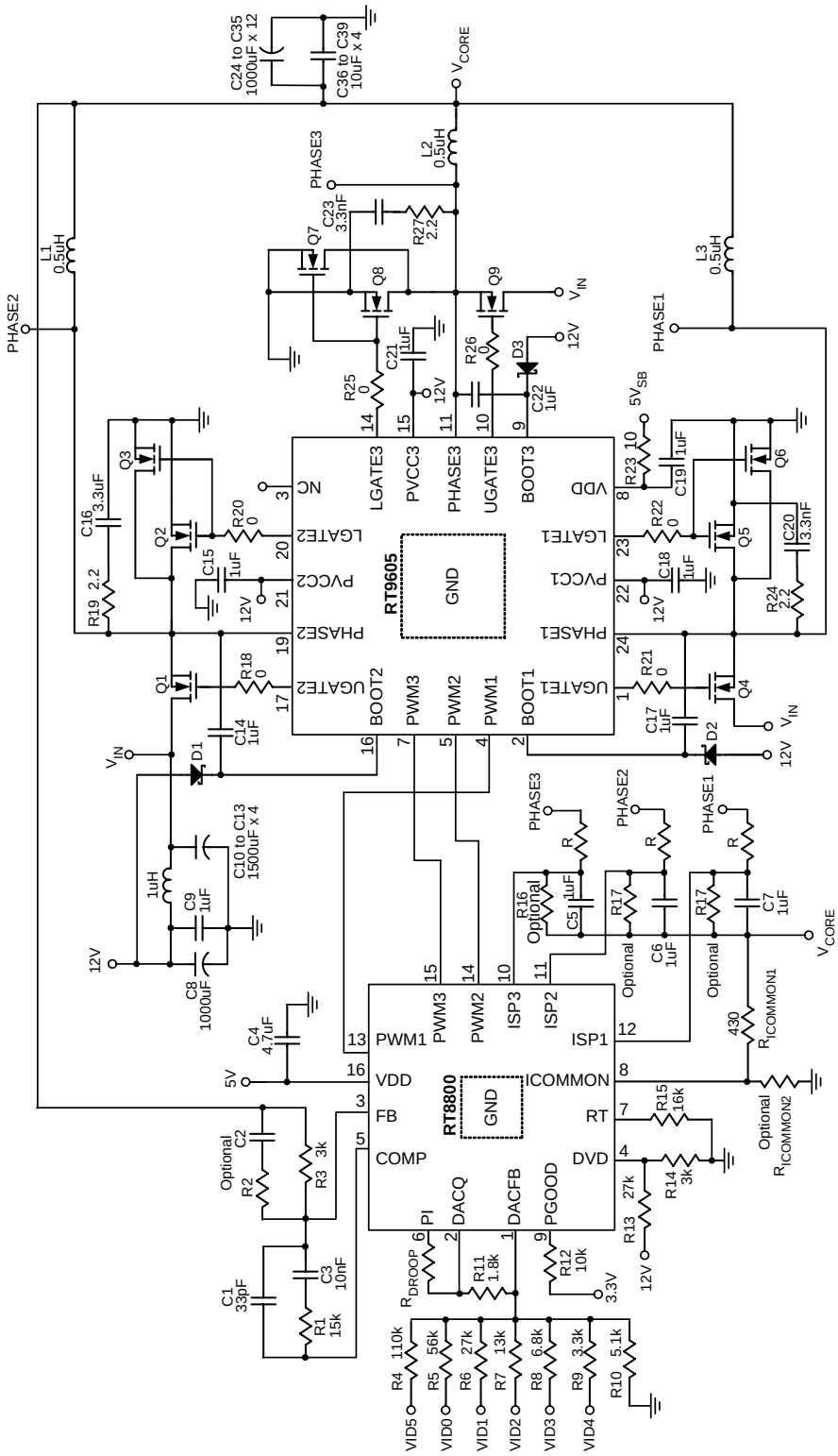


Figure B. 3-phase with resistive DAC

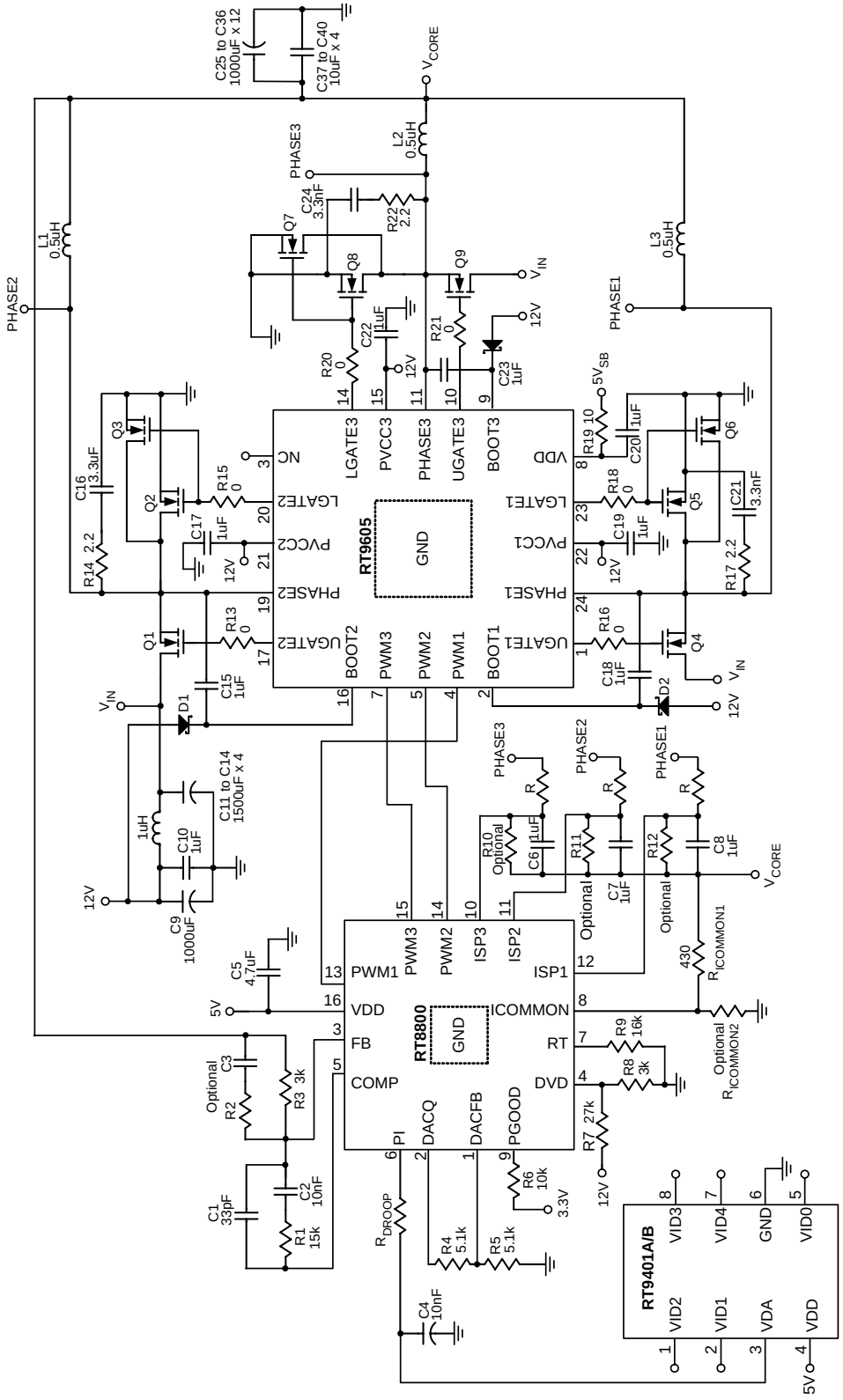


Figure C. 3-phase with RT9401A/B DAC generator

Function Block Diagram

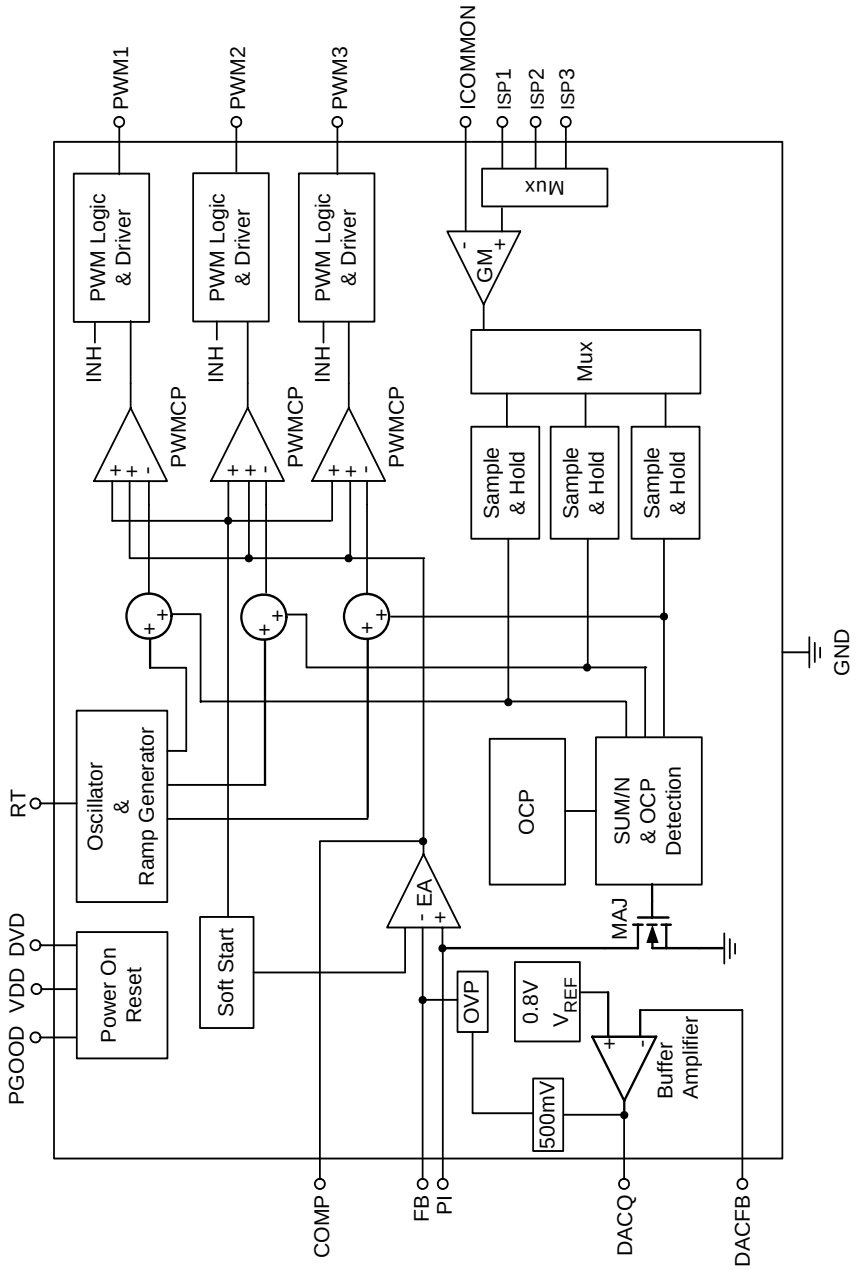


Table. Output Voltage Program

VID5	VID4	VID3	VID2	VID1	VID0	Nominal Output Voltage (V)
1	1	1	1	1	1	1.0800
1	1	1	1	1	0	1.1000
0	1	1	1	1	0	1.1125
1	1	1	1	0	1	1.1250
0	1	1	1	0	1	1.1375
1	1	1	1	0	0	1.1500
0	1	1	1	0	0	1.1625
1	1	1	0	1	1	1.1750
0	1	1	0	1	1	1.1875
1	1	1	0	1	0	1.2000
0	1	1	0	1	0	1.2125
1	1	1	0	0	1	1.2250
0	1	1	0	0	1	1.2375
1	1	1	0	0	0	1.2500
0	1	1	0	0	0	1.2625
1	1	0	1	1	1	1.2750
0	1	0	1	1	1	1.2875
1	1	0	1	1	0	1.3000
0	1	0	1	1	0	1.3125
1	1	0	1	0	1	1.3250
0	1	0	1	0	1	1.3375
1	1	0	1	0	0	1.3500
0	1	0	1	0	0	1.3625
1	1	0	0	1	1	1.3750
0	1	0	0	1	1	1.3875
1	1	0	0	1	0	1.4000
0	1	0	0	1	0	1.4125
1	1	0	0	0	1	1.4250
0	1	0	0	0	1	1.4375
1	1	0	0	0	0	1.4500
0	1	0	0	0	0	1.4625
1	0	1	1	1	1	1.4750
0	0	1	1	1	1	1.4875
1	0	1	1	1	0	1.5000
0	0	1	1	1	0	1.5125
1	0	1	1	0	1	1.5250
0	0	1	1	0	1	1.5375
1	0	1	1	0	0	1.5500

To be continued

Table. Output Voltage Program

VID5	VID4	VID3	VID2	VID1	VID0	Nominal Output Voltage (V)
0	0	1	1	0	0	1.5625
1	0	1	0	1	1	1.5750
0	0	1	0	1	1	1.5875
1	0	1	0	1	0	1.6000
1	0	1	0	0	1	1.6250
1	0	1	0	0	0	1.6500
1	0	0	1	1	1	1.6750
1	0	0	1	1	0	1.7000
1	0	0	1	0	1	1.7250
1	0	0	1	0	0	1.7500
1	0	0	0	1	1	1.7750
1	0	0	0	1	0	1.8000
1	0	0	0	0	1	1.8250
1	0	0	0	0	0	1.8500

Note: 1 : Open

0 : V_{SS} or GND

Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{DD} ---------- 7V
- Input, Output or I/O Voltage ---------- GND – 0.3V to V_{DD} + 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  VQFN-16L 3X3 ---------- 1.47W
  SOP-16 ---------- 1W
- Package Thermal Resistance (Note 4)
  VQFN-16L 3X3, θ_{JA} ---------- 68°C/W
  SOP-16, θ_{JA} ---------- 100°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Supply Voltage, V_{DD} ---------- 5V ± 10%
- Ambient Temperature Range ---------- 0°C to 70°C
- Junction Temperature Range ---------- 0°C to 125°C

Electrical Characteristics

(V_{DD} = 5V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
V_{DD} Supply Current							
Nominal Supply Current		I_{DD}	PWM 1,2,3 Open	--	5	--	mA
Power-On Reset							
V_{DD} Threshold	Rising			4.0	4.2	4.5	V
	Hysteresis			0.2	0.5	--	V
DVD Rising Threshold				0.75	0.8	0.85	V
DVD Hysteresis				--	65	--	mV
Oscillator							
Free Running Frequency		f_{OSC}	R_{RT} = 16kΩ	170	200	230	kHz
Frequency Adjustable Range		f_{OSC_ADJ}		50	--	400	kHz
Ramp Amplitude		ΔV_{OSC}	R_{RT} = 16kΩ	--	1.7	--	V
Ramp Valley		V_{RV}		--	1.0	--	V
Maximum On-Time of Each Channel				62	66	75	%
Minimum On-Time of Each Channel				--	120	--	ns
RT Pin Voltage		V_{RT}	R_{RT} = 16kΩ	0.77	0.82	0.87	V

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reference Voltage						
Reference Voltage	V_{DACFB}		0.79	0.8	0.81	V
DACFB Sourcing Capability			--	--	10	mA
Error Amplifier						
DC Gain			--	65	--	dB
Gain-Bandwidth Product	GBW	C_L = 10pF	--	10	--	MHz
Slew Rate	SR	C_L = 10pF	--	8	--	V/μs
Current Sense GM Amplifier						
Recommended Full Scale Source Current			--	100	--	μA
OCP trip level	I_{OCP}		160	190	220	μA
Protection						
Over-Voltage Trip (V_{FB} - V_{DACQ})			--	500	--	mV
Power Good						
PGOOD Output Low Voltage	V_{PGOOD}	I_{PGOOD} = 4mA	--	--	0.2	V
PGOOD Delay	T_{PGOOD_Delay}	90% * V_{OUT} to PGOOD_H	4	--	8	ms

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

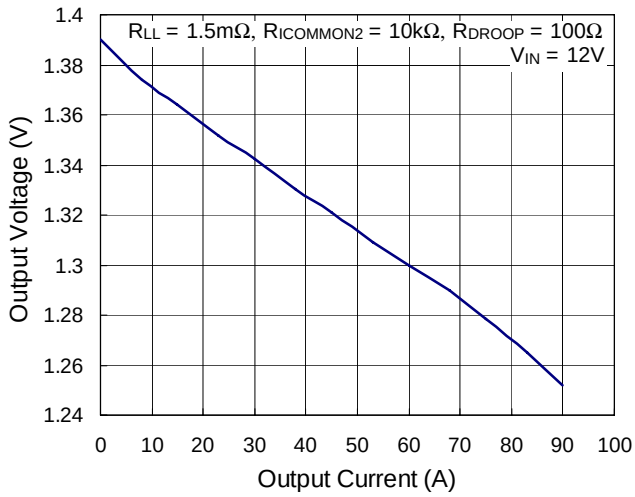
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

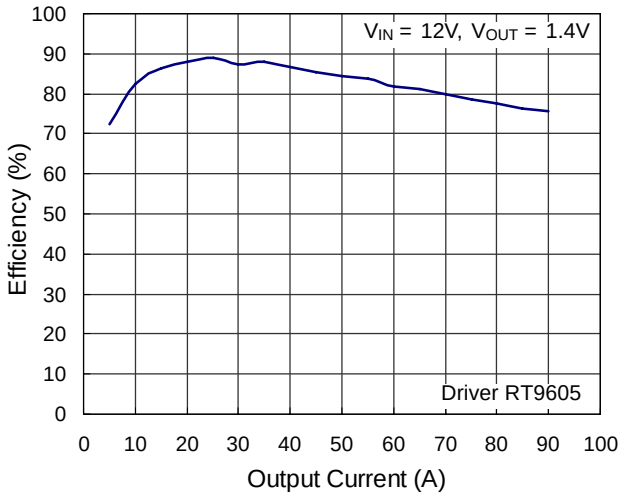
Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Typical Operating Characteristics

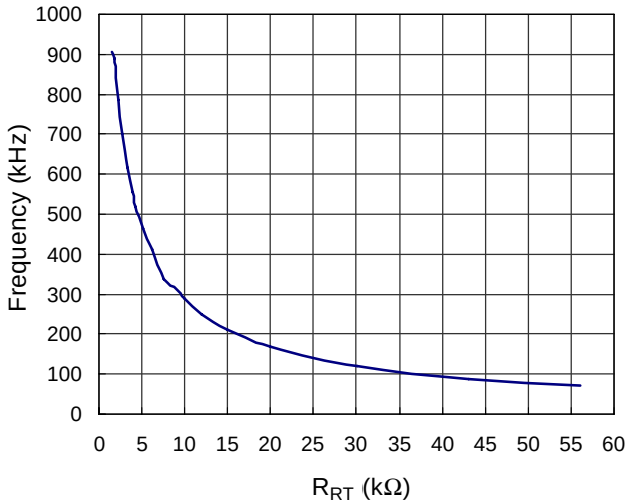
Load Line



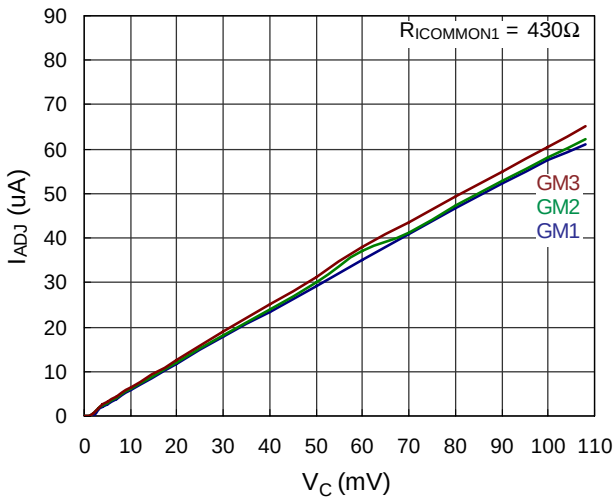
Efficiency vs. Output Current



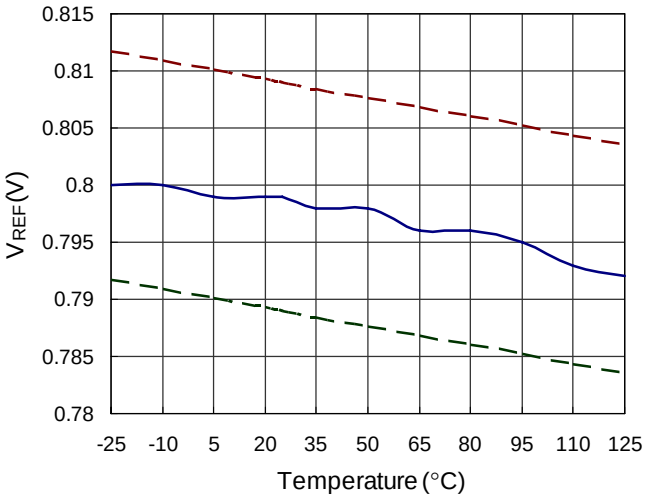
Frequency vs. R_{RT}



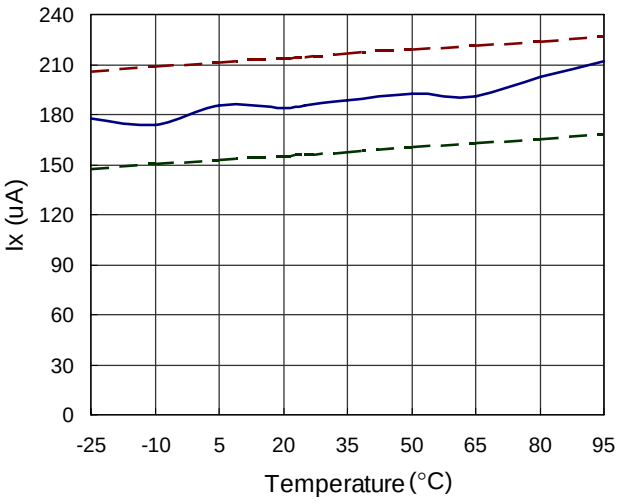
GM



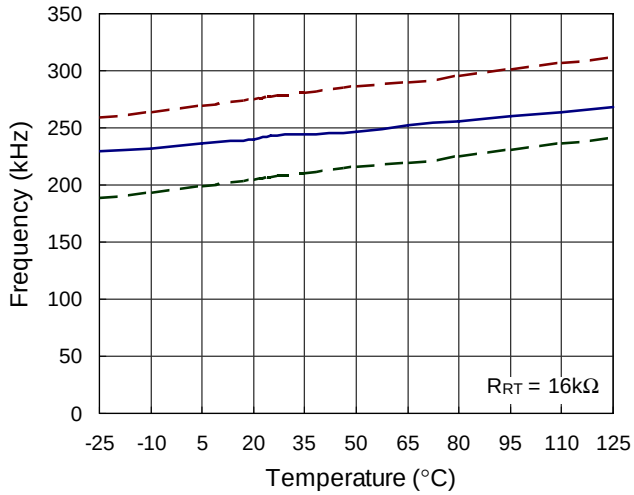
V_{REF} vs. Temperature



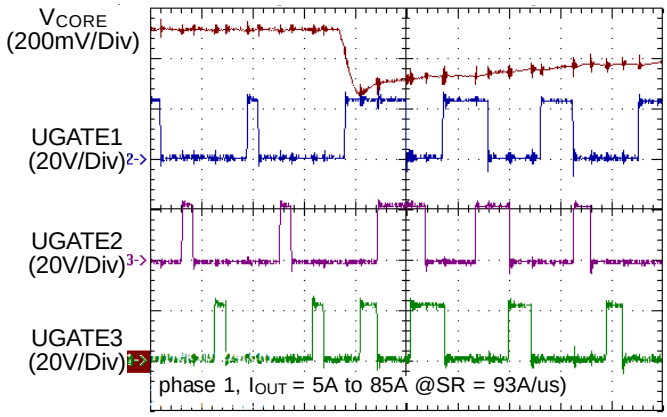
OCP Trip Point vs. Temperature



Frequency vs. Temperature

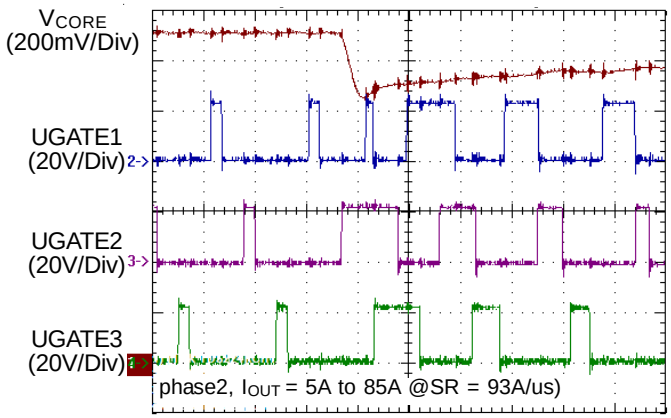


Load Transient Response



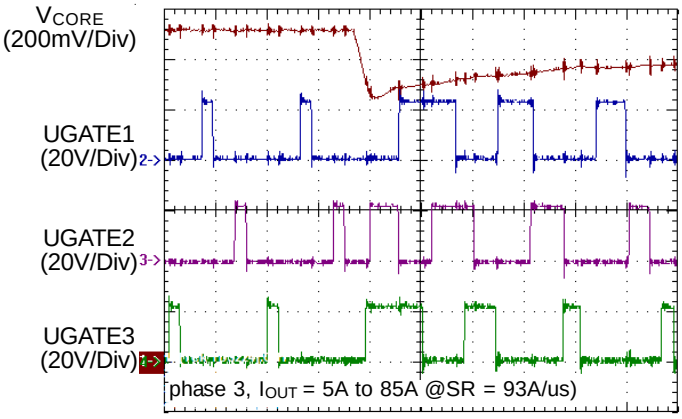
Time (2.5µs/Div)

Load Transient Response



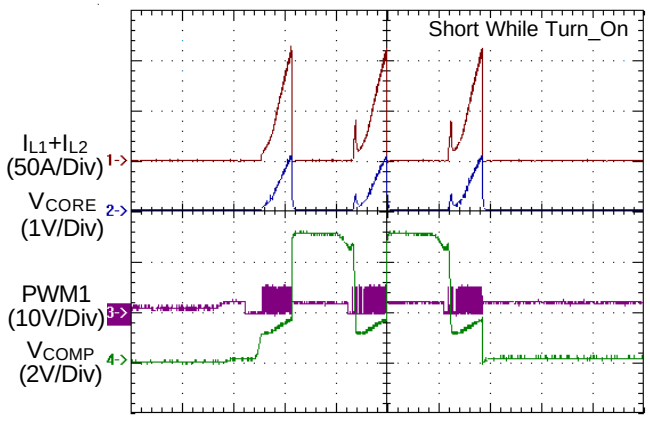
Time (2.5µs/Div)

Load Transient Response



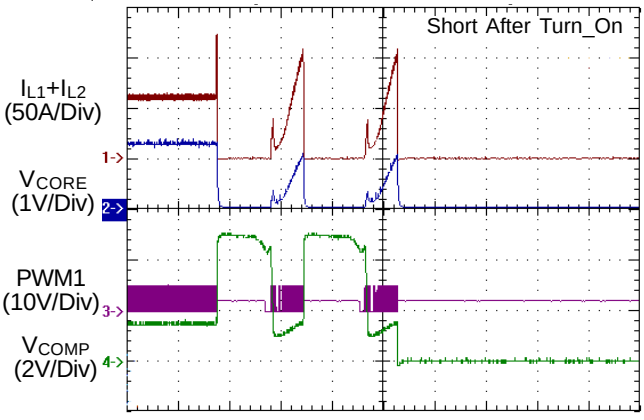
Time (2.5µs/Div)

Over Current Protection



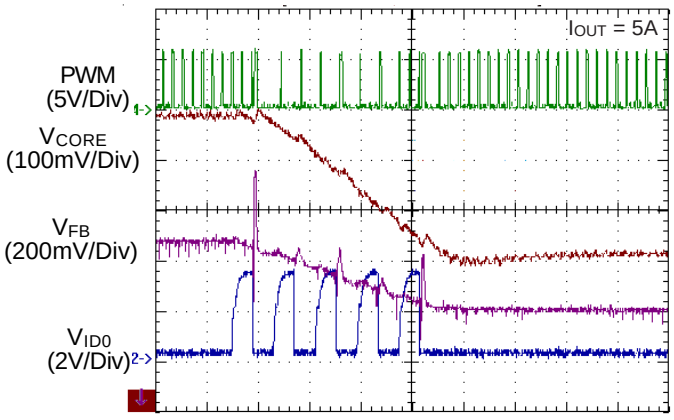
Time (10ms/Div)

Over Current Protection

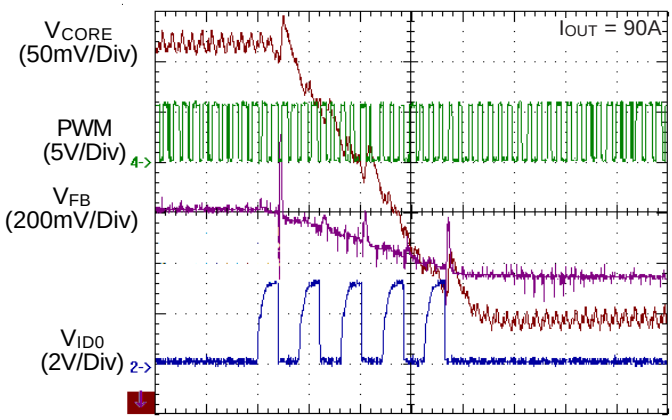


Time (10ms/Div)

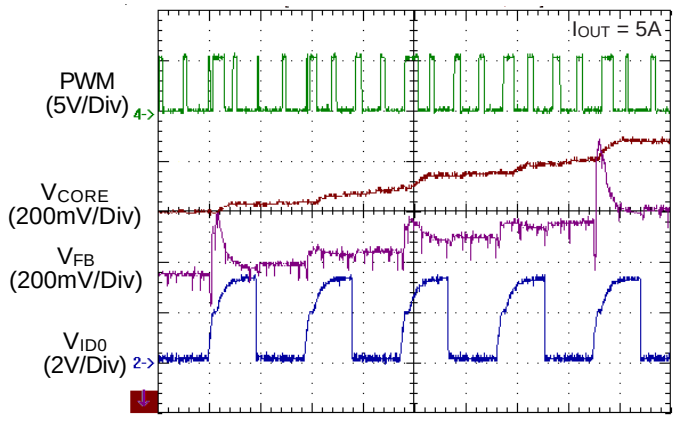
V_{ID} On the Fly Falling



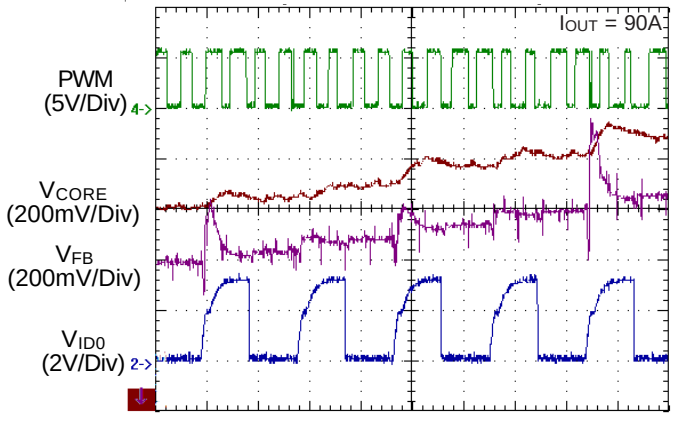
V_{ID} On the Fly Falling



V_{ID} On the Fly Rising



V_{ID} On the Fly Rising



Application Information

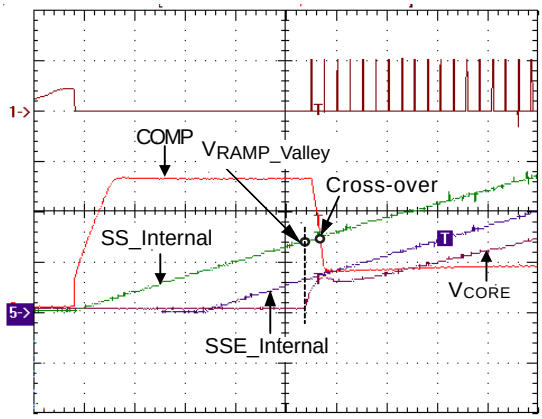
RT8800/B are multiphase DC/DC controllers for extreme low cost applications that precisely regulate CPU core voltage and balance the current of different power channels using time sharing current sensing method. The converter consisting of RT8800/B and its companion MOSFET driver RT96xx series provide high quality CPU power and all protection functions to meet the requirement of modern VRM.

Phase Setting and Converter Start Up

RT8800/B interface with companion MOSFET drivers (like RT9602, RT9603, and RT9605) for correct converter initialization. RT8800/B will sense the voltage on PWM pins at the instant of POR rising. If the voltage is smaller than (V_{DD} – 1.2V) the related channel is activated. Tie the PWM to V_{DD} and the corresponding current sense pins to GND or left float if the channel is unused. For example, for 2-Channel application, tie PWM3 to V_{DD} and ISP3 to GND (or let ISP3 open).

PGOOD Function and Soft Start

To indicate the condition of multiphase converter, RT8800/B provide PGOOD signal through an open drain connection. The output becomes high impedance after internal SS ramp > 3.5V.



1) Mode 1 (SS< Vramp_valley)

Initially the COMP stays in the positive saturation. When SS< V_{RAMP_Valley}, there is no non-inverting input available to produce duty width. So there is no PWM signal and V_{OUT} is zero.

2) Mode 2 (V_{RAMP_Valley}< SS< Cross-over)

When SS>V_{RAMP_Valley}, SS takes over the non-inverting input and produce the PWM signal and the increasing duty width according to its magnitude above the ramp signal. The output follows the ramp signal, SS. However while V_{OUT} increases, the difference between V_{OUT} and SSE(SS – V_{GS}) is reduced and COMP leaves the saturation and declines. The takeover of SS lasts until it meets the COMP. During this interval, since the feedback path is broken, the converter is operated in the open loop.

3) Mode3 (Cross-over< SS < V_{GS} + V_{REF})

When the Comp takes over the non-inverting input for PWM Amplifier and when SSE (SS – V_{GS}) < V_{REF}, the output of the converter follows the ramp input, SSE (SS – V_{GS}). Before the crossover, the output follows SS signal. And when Comp takes over SS, the output is expected to follow SSE (SS – V_{GS}). Therefore the deviation of V_{GS} is represented as the falling of V_{OUT} for a short while. The COMP is observed to keep its decline when it passes the cross-over, which shortens the duty width and hence the falling of V_{OUT} happens.

Since there is a feedback loop for the error amplifier, the output' s response to the ramp input, SSE (SS – V_{GS}) is lower than that in Mode 2.

4) Mode 4 (SS > V_{GS} + V_{REF})

When SS > V_{GS} + V_{REF}, the output of the converter follows the desired V_{REF} signal and the soft start is completed now.

Voltage Control

The voltage control loop consists of error amplifier, multiphase pulse width modulator, driver and power components. As conventional voltage mode PWM controller, the output voltage is locked at the positive input of error amplifier and the error signal is used as the control signal of pulse width modulator. The PWM signals of different channels are generated by comparison of EA output and split-phase sawtooth wave. Power stage transforms V_{IN} to output by PWM signal on-time ratio.

Output Voltage Program

The output voltage of a RT8800/B converter is programmed to discrete levels between 1.08V and 1.85V. The voltage identification (V_{ID}) pins program an external voltage reference (DACQ) with a 6-bit digital-to-analog converter (DAC). The level of DACQ also sets the OVP threshold. The output voltage should not be adjusted while the converter is delivering power. Remove input power before

changing the output voltage. Adjusting the output voltage during operation may trigger the over-voltage protection. The DAC function is a precision non-inverting summation amplifier shown in Figure 1. The resistor values shown are only approximations of the actual precision values used. Grounding any combination of the V_{ID} pins increases the DACQ voltage. The "open" circuit voltage on the V_{ID} pins is the band gap reference voltage (V_{REF} = 0.8V).

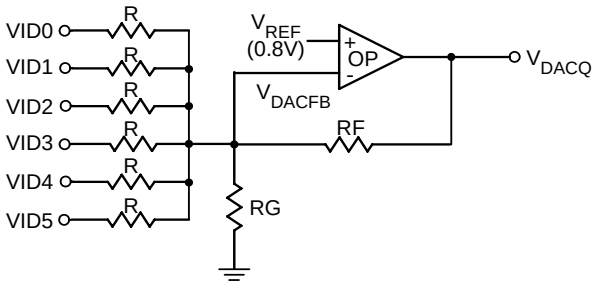


Figure 1. The Structure of Discrete DAC Generator

DAC Design Guideline

In high temperature environment, V_{CORE} becomes unstable for the leakage current in VID pins is increasing. The leakage will increase current consumption of CPU, and then raise RT8800's V_{DACQ} reference output, so does V_{CORE} voltage. Below are four comparison charts for different CPUs.

Note: In Below Figure 2 to Figure 5, The Original R means the resister values shown in typical application circuit. R=1/3 and R=1/9 mean that The Original R is divided by 3 or 9.

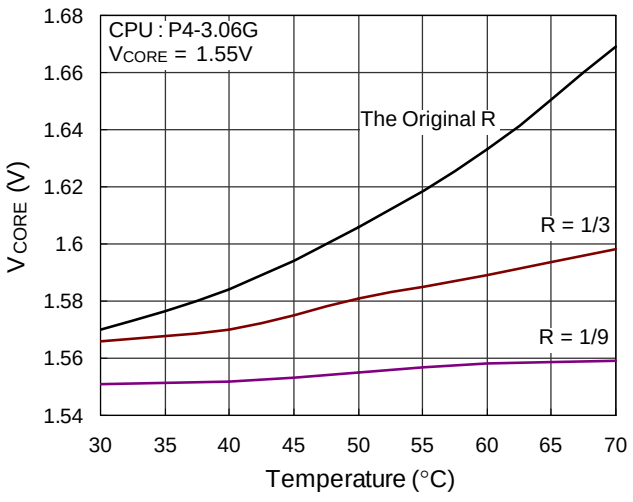


Figure 2

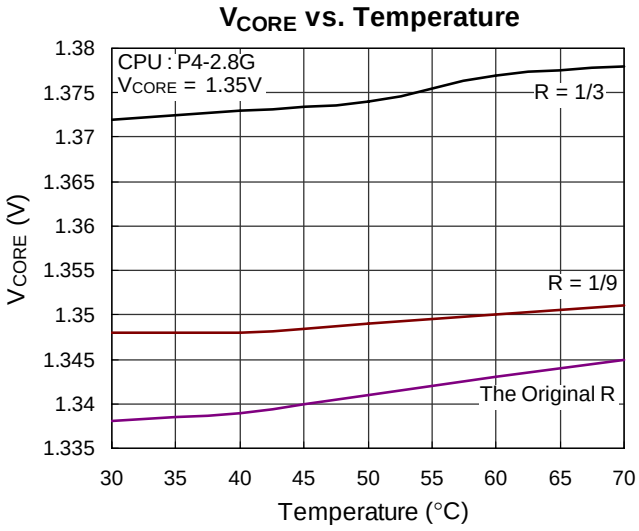


Figure 3

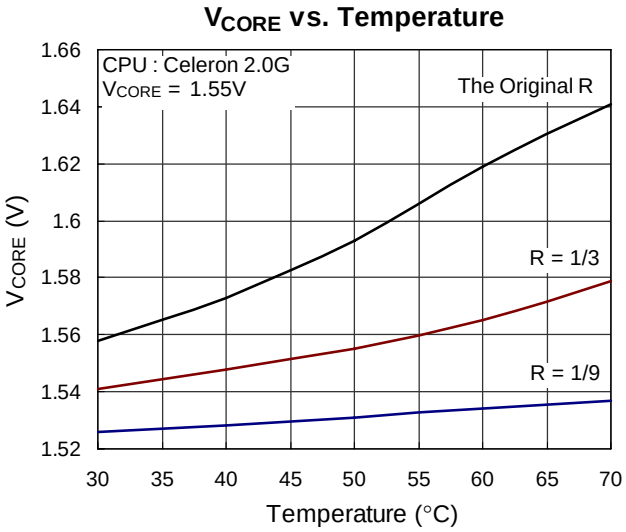


Figure 4

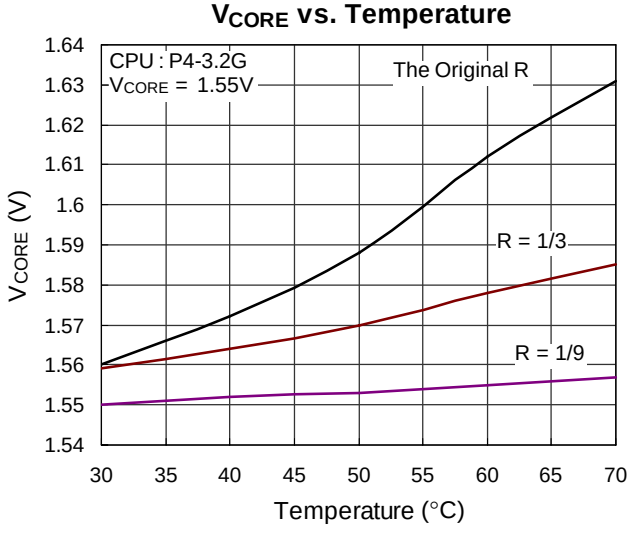


Figure 5

In order to maintain the V_{DACQ} within 1% tolerance in the worst case, the total driver current of the DAC regulator should support up to 40mA. As the design of RT8800/B, the maximum driving current of the internal OP is 10mA. As shown in Figure 6, we suggest to add an external transistor 2N3904 for higher current for V_{DAC} regulation.

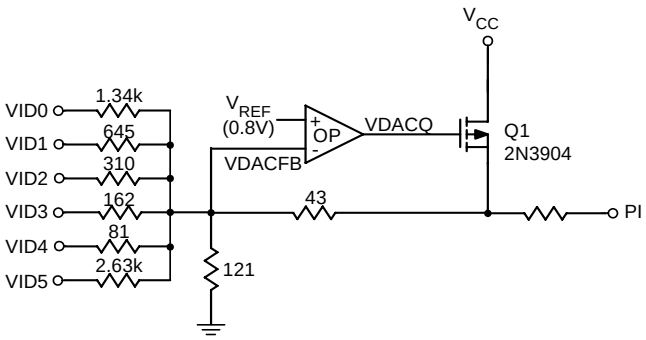


Figure 6. Immune circuit against CPU Leakage Current

Current Sensing Setting

RT8800/B senses the current flowing through inductor via its DCR for channel current balance and droop tuning. The differential sensing GM amplifier converts the voltage on the sense component (can be a sense resistor or the DCR of the inductor) to current signal into internal circuit (see Figure 7).

$$\frac{L}{DCR} = R \times C \quad V_C = DCR \times I_L \quad I_X = \frac{V_C}{R_{ICOMMON1}}$$

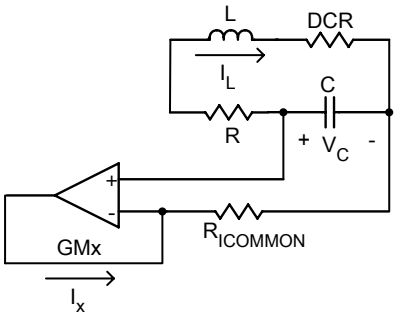


Figure 7. Current Sense Circuit

The sensing circuit gets $I_X = \frac{I_L \times DCR}{R_{ICOMMON1}}$ by local feedback.

I_X is sampled and held just before low side MOSFET turns off (Figure 8).

$$I_{X(S/H)} = \frac{I_{L(S/H)} \times DCR}{R_{ICOMMON1}} ; I_{L(S/H)} = I_{L(AVG)} - \frac{V_O}{L} \times \frac{T_{OFF}}{2}$$

$$T_{OFF} = \left(\frac{V_{IN} - V_O}{V_{IN}}\right) \times T_S$$

for switching, period = T_S

$$I_{X(S/H)} = \left[I_{L(AVG)} - \frac{V_O - \left(\frac{V_{IN} - V_O}{V_{IN}}\right) \times T_S}{2L} \right] \times \frac{DCR}{R_{ICOMMON1}}$$

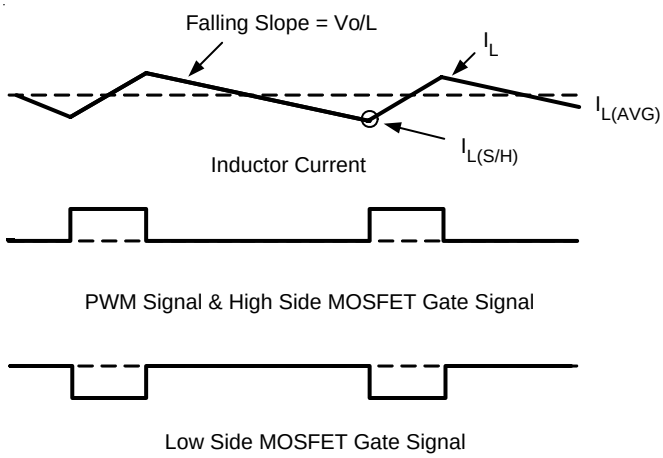


Figure 8. Inductor current and PWM signal

Figure 9 is the test circuit for GM. We apply test signal at GM inputs and observe its signal process output by PI pin sinking current. Figure 10 shows the variation of signal processing of all channels. We observe zero offsets and good linearity between phases.

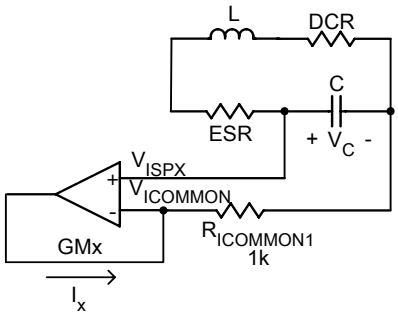


Figure 9. The Test Circuit of GM

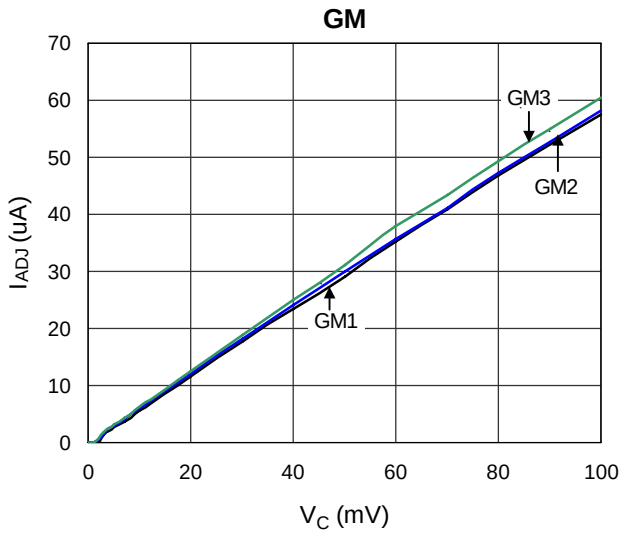


Figure 10. The Linearity of GMx

Figure 11 shows the time sharing technique of GM amplifier. We apply test signal at phase 3 and observe the waveforms at both pins of GM amplifier. The waveforms show time sharing mechanism and the perfomance of GM to hold both input pins equal when the shared time is on.

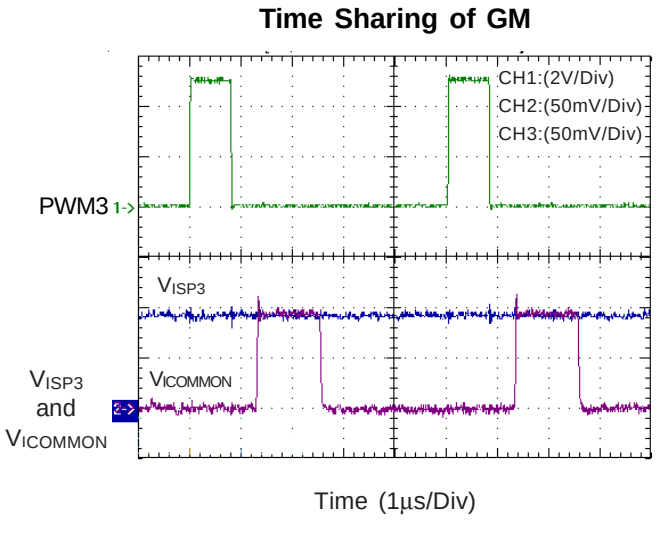


Figure 11

Current Ratio Setting

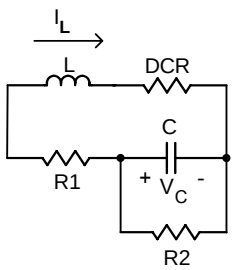


Figure 12. Application circuit for current ratio setting

For some case with preferable current ratio instead of current balance, the corresponding technique is provided. Due to different physical environment of each channel, it is necessary to slightly adjust current loading between channels. Figure 12. shows the application circuit of GM for current ratio requirement. Applying KVL along L+DCR branch and R1+C//R2 branch:

$$L\frac{dI_L}{dt} + DCR \times I_L = R1\left(\frac{V_C}{R2} + C\frac{dV_C}{dt}\right) + V_C$$

$$= R1 \times C\frac{dV_C}{dt} + \frac{R1+R2}{R2}V_C$$

$$\text{For } V_C = \frac{R2}{R1+R2} DCR \times I_L$$

Look for its corresponding conditions:

$$L\frac{dI_L}{dt} + DCR \times I_L = (R1//R2) \times C \times DCR \times \frac{dI_L}{dt} + DCR \times I_L$$

$$\text{Let } \frac{L}{DCR} = (R1//R2) \times C$$

$$\text{Thus if } \frac{L}{DCR} = (R1//R2) \times C$$

$$\text{Then } V_C = \frac{R2}{R1+R2} \times DCR \times I_L$$

With internal current balance function, this phase would share $(R_1+R_2)/R_2$ times current than other phases. Figure 13 &14 show different settings for the power stages.

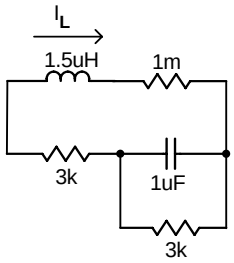


Figure 13. GM3 Setting for current ratio function

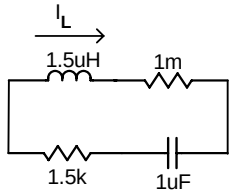


Figure 14. GM1,2 Setting for current ratio function

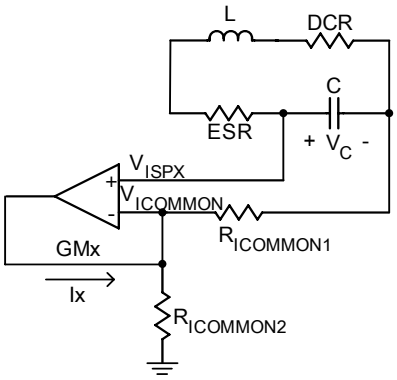


Figure 15. Application circuit of GM

For load line design, with application circuit in Figure 15, it can eliminate the dead zone of load line at light loads.

$$V_{ISPX} = V_{OUT} + I_L \times DCR$$

if GM holds input voltages equal, then

$$V_{ISPX} = V_{ICOMMON}$$

$$I_X = \frac{V_{ICOMMON}}{R_{ICOMMON2}} + \frac{I_L \times DCR}{R_{ICOMMON1}}$$

$$= \frac{V_{OUT} + I_L \times DCR}{R_{ICOMMON2}} + \frac{I_L \times DCR}{R_{ICOMMON1}}$$

$$= \frac{V_{OUT}}{R_{ICOMMON2}} + \frac{I_L \times DCR}{R_{ICOMMON2}} + \frac{I_L \times DCR}{R_{ICOMMON1}}$$

For the lack of sinking capability of GM, $R_{ICOMMON2}$ should be small enough to compensate the negative inductor valley current especially at light loads.

$$\frac{V_{ICOMMON}}{R_{ICOMMON2}} \geq \left| \frac{I_L \times DCR}{R_{ICOMMON1}} \right|$$

Assume the negative inductor valley current is –5A at no load, then for

$R_{ICOMMON1} = 330\Omega$, $R_{ADJ} = 160\Omega$, $V_{OUT} = 1.300$

$$\frac{1.3V}{R_{ICOMMON2}} \geq \left| \frac{-5A \times 1m\Omega}{330\Omega} \right|$$

$R_{ICOMMON2} \leq 85.8k\Omega$

Choose $R_{ICOMMON2}$ = 82kΩ

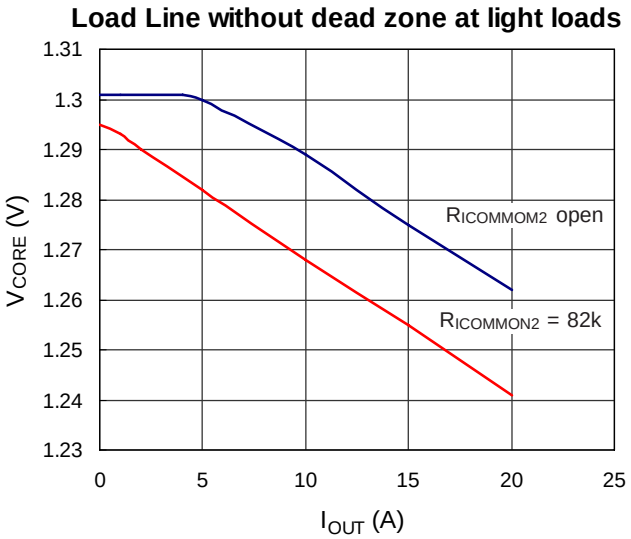


Figure 16

Current Balance

RT8800/B senses the inductor current via inductor' s DCR for channel current balance and droop tuning. The differential sensing GM amplifier converts the voltage on the sense component (can be a sense resistor or the DCR of the inductor) to current signal into internal balance circuit.

The current balance circuit sums and averages the current signals and then produces the balancing signals injected to pulse width modulator. If the current of some power channel is larger than average, the balancing signal reduces that channels pulse width to keep current balance.

The use of single GM amplifier via time sharing technique to sense all inductor currents can reduce the offset errors and linearity variation between GMs. Thus it can greatly improve signal processing especially when dealing with such small signal as voltage drop across DCR.

Voltage Reference for Converter Output & Load Droop

The positive input of error amplifier is PI pin that sinks current proportional to the sum of converter output current. $V_{DRP} = 2I_{SINK} \times R_{DRP}$. The load droop proportional to load current can be set by the resistor between PI pin & external V_{DACQ} produced by either buffer amplifier or other voltage source. The PI pin voltage should be larger than 0.8V for good droop circuit performance.

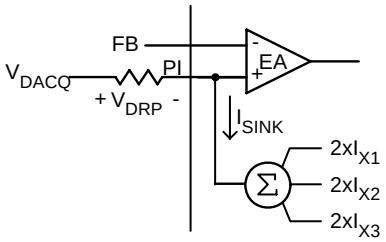


Figure 17. Load Droop Circuit

DAC Offset Voltage Tuning

The Intel specification requires that at no load the nominal output voltage of the regulator be offset to a value lower than the nominal voltage corresponding to the V_{ID} code. The offset is tuning from RG in the DAC generator as Figure 18.

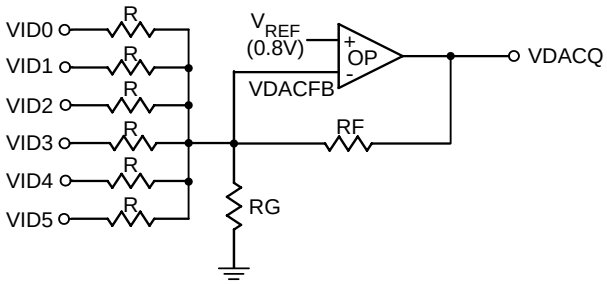


Figure 18. The Structure of Discrete DAC Generator

If VID0~6 is set at VSS (Ground), and to suppose that shunt resistance is Rs.

From below equation, we can tune the value of RG to increase or decrease the base voltage of V_{DACQ}.

$$V_{DACQ} = (1 + \frac{R_F}{R_G}) \times V_{REF} + \frac{R_F}{R_S} \times V_{REF}$$

Over Current Protection

OCP comparator co\mpares each inductor current sensed & sample/hold by current sense circuit with this reference current(150uA). RT8800/B uses hiccup mode to eliminate fault detection of OCP or reduce output current when output is shorted to ground.

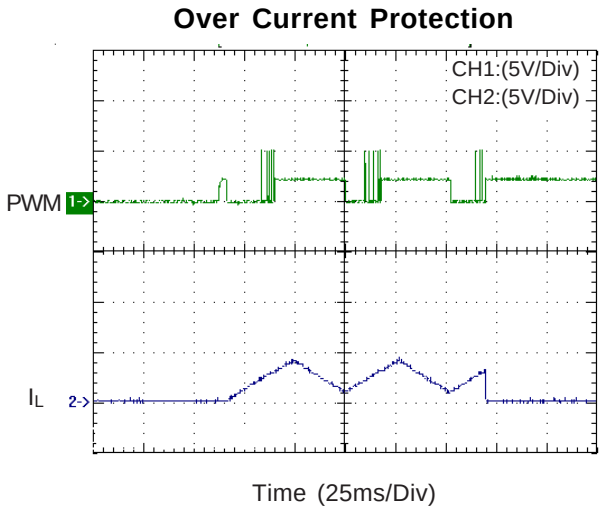


Figure 19. The Over Current Protection in the interval

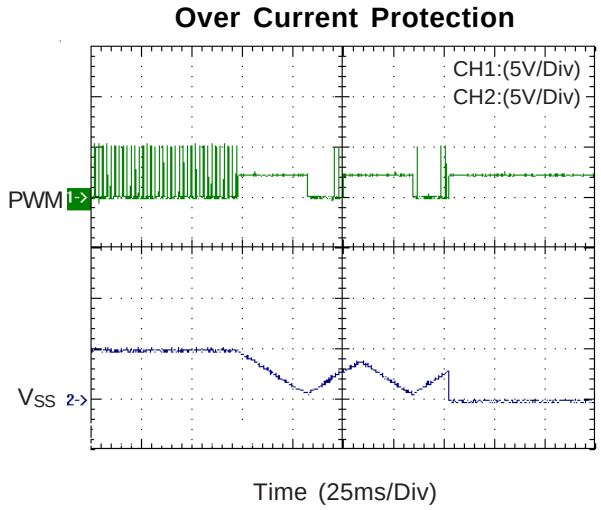


Figure 20. Over Current Protection at steady state

Fault Detection

The “hiccup mode” operation of over current protection is adopted to reduce the short circuit current. The in-rush current at the start up is suppressed by the soft start circuit through clamping the pulse width and output voltage by an internal slow rising ramp.

Design Procedure Suggestion

a. Output filter pole and zero (Inductor, output capacitor value & ESR).

b. Error amplifier compensation & sawtooth wave amplitude (compensation network).

Current Loop Setting

a. GM amplifier S/H current (current sense component DCR, ICOMMON pin external resistor value).

b. Over-current protection trip point ($R_{ICOMMON1}$ resistor).

VRM Load Line Setting

a. Droop amplitude (PI pin resistor).

b. No load offset ($R_{ICOMMON2}$)

Power Sequence & SS

DVD pin external resistor and SS pin capacitor.

PCB Layout

a. Sense for current sense GM amplifier input.

b. Refer to layout guide for other items.

Voltage Loop Setting

Design Example

Given:

Apply for four phase converter

V_{IN} = 12V

V_{CORE} = 1.5V

$I_{LOAD(MAX)}$ = 100A

V_{DROOP} = 100mV at full load (1mΩ Load Line)

OCP trip point set at 35A for each channel (S/H)

DCR = 1mΩ of inductor at 25°C

L = 1.5µH

C_{OUT} = 8000µF with 5mΩ equivalent ESR.

1. Compensation Setting

a. Modulator Gain, Pole and Zero:

From the following formula:

Modulator Gain =V_{IN}/V_{RAMP} =12/2.4=5 (i.e 14dB)

where V_{RAMP} : ramp amplitude of saw-tooth wave

LC Filter Pole = 1.45kHz and

ESR Zero =3.98kHz

b. EA Compensation Network:

Select R1 = 4.7k, R2 = 15k, C1 = 12nF, C2 = 68pF and use the Type 2 compensation scheme shown in Figure 21. By calculation, the F_Z = 0.88kHz, F_P = 322kHz and Middle Band Gain is 3.19 (i.e 10.07dB).

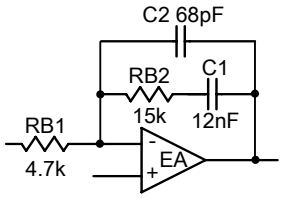


Figure 21. Type 2 compensation network of EA

2. Over-Current Protection Setting

Consider the temperature coefficient of copper 3900ppm/°C,

$$\frac{I_L \times DCR}{R_{ICOMMON1}} = 150\mu A$$

$$\frac{I_L \times 1.39m\Omega}{330\Omega} = 150\mu A$$

$$I_L = 35.6A$$

Layout Guide

Place the high-power switching components first, and separate them from sensitive nodes.

1. Most critical path:

   The current sense circuit is the most sensitive part of the converter. The current sense resistors tied to ISP1,2,3 and ICOMMON should be located not more than 0.5 inch from the IC and away from the noise switching nodes. The PCB trace of sense nodes should be parallel and as short as possible. R&C filter of choke should place close to PWM and the R & C connect directly to the pin of each output choke, use 10 mil differencial pair, and 20 mil gap to other phase pair. Less via as possible.

2. Switching ripple current path:

   a. Input capacitor to high side MOSFET.

   b. Low side MOSFET to output capacitor.

   c. The return path of input and output capacitor.

   d. Separate the power and signal GND.

   e. The switching nodes (the connection node of high/low side MOSFET and inductor) is the most noisy points.Keep them away from sensitive small-signal node.

   f . Reduce parasitic R, L by minimum length, enough copper thickness and avoiding of via.

3. MOSFET driver should be closed to MOSFET.

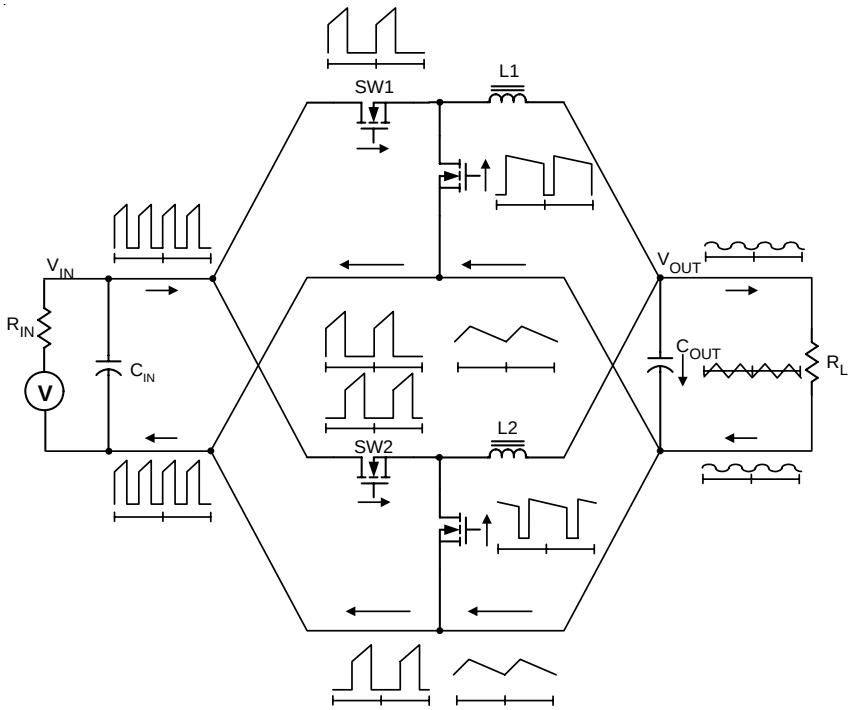


Figure 22. Power Stage Ripple Current Path

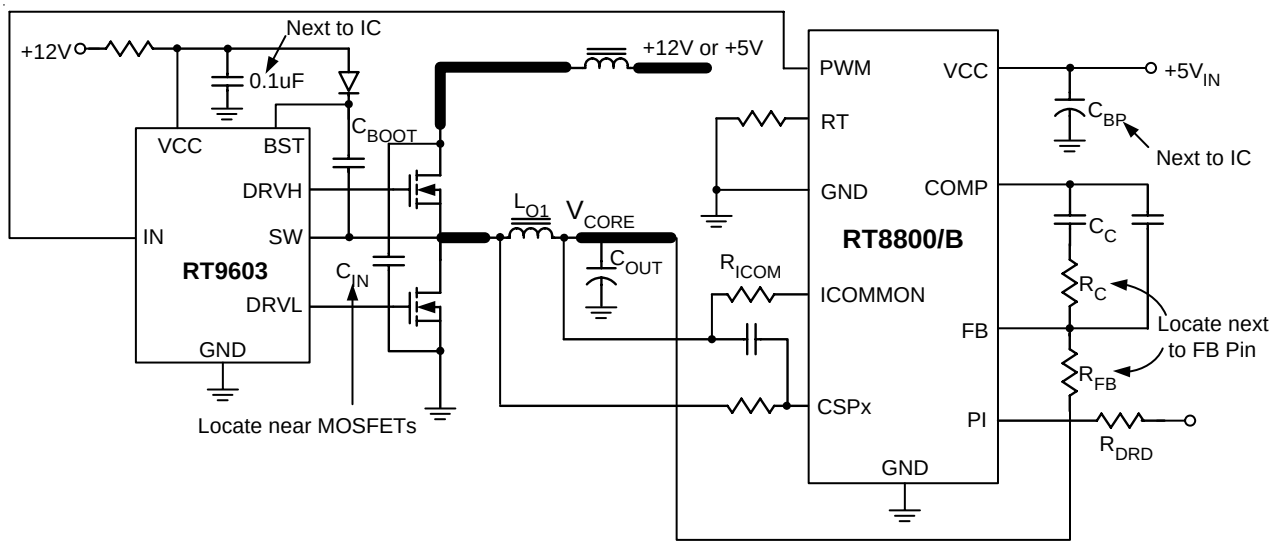


Figure 23. Layout Consideration

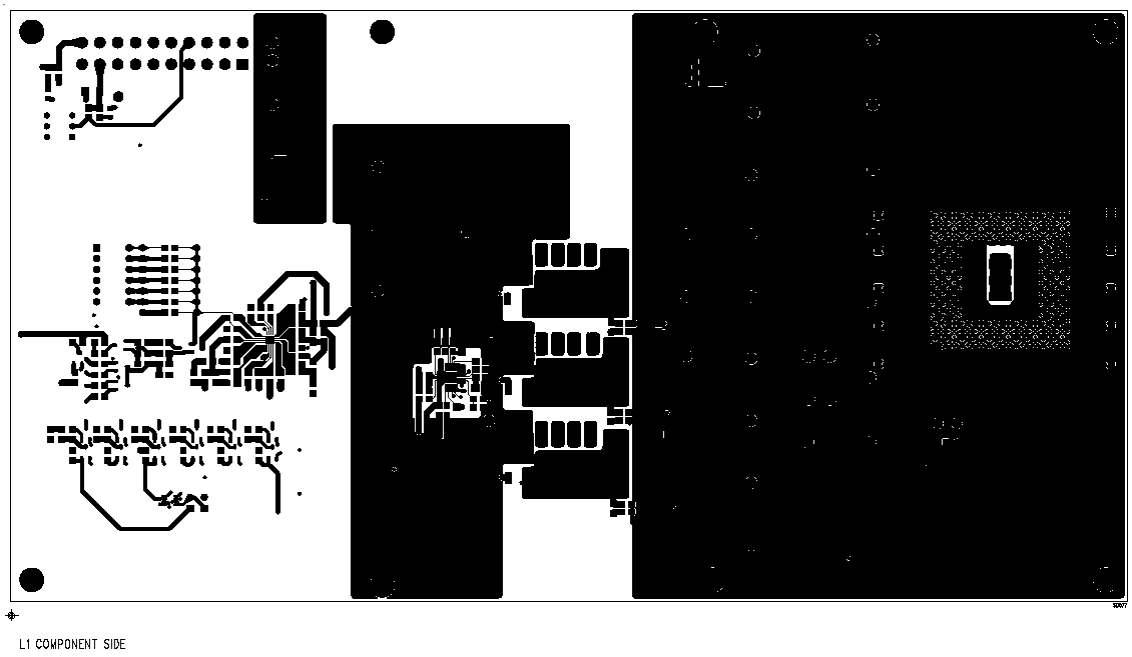


Figure 24

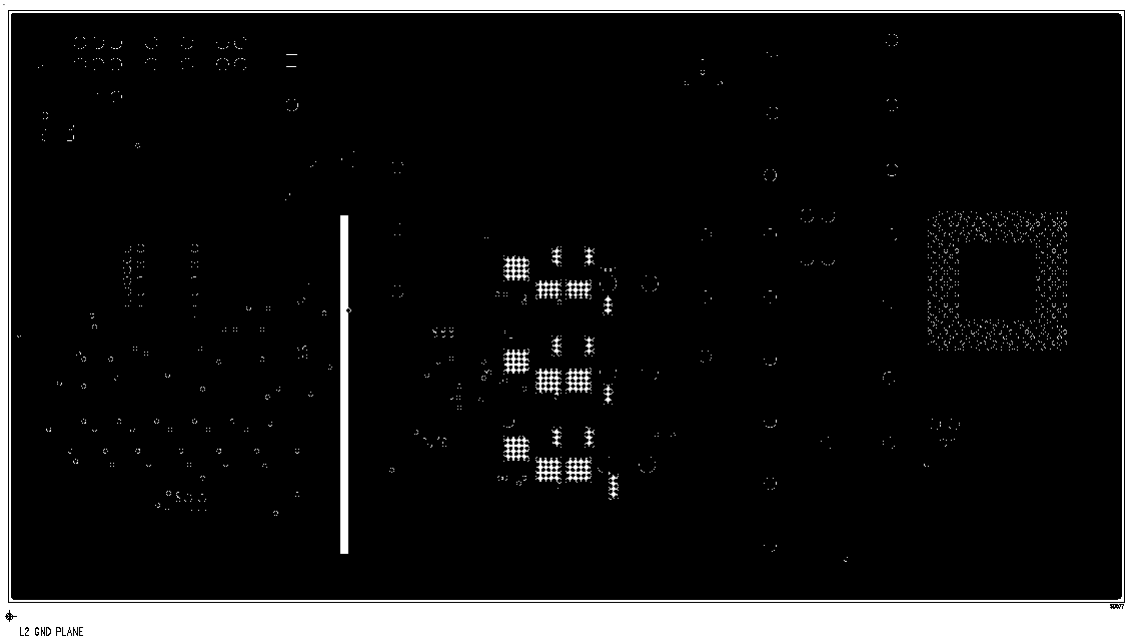


Figure 25

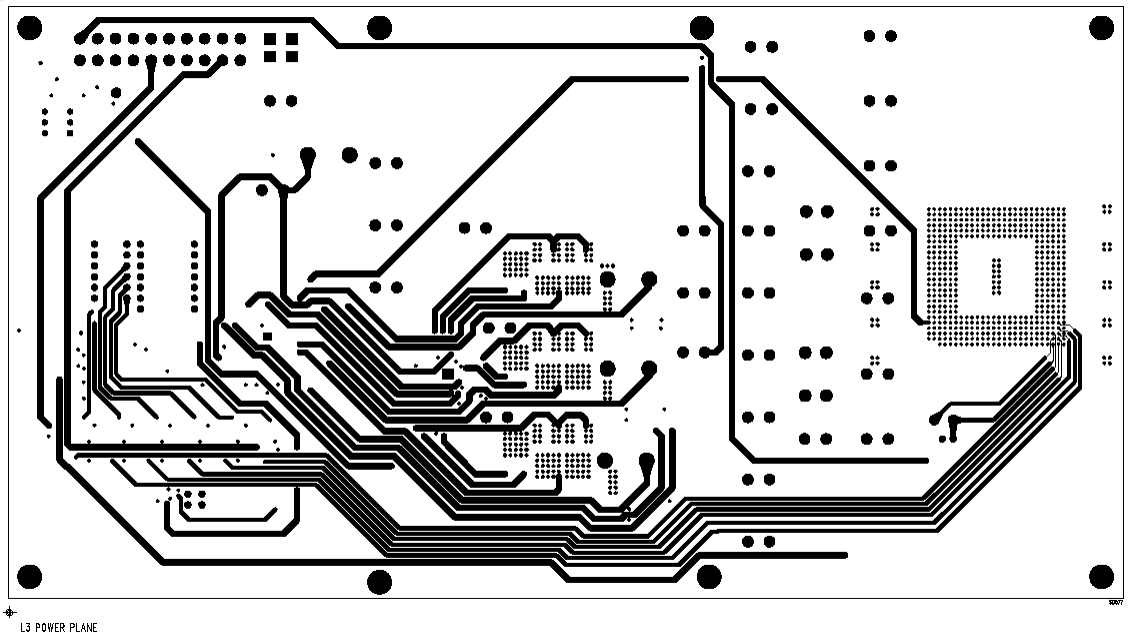


Figure 26

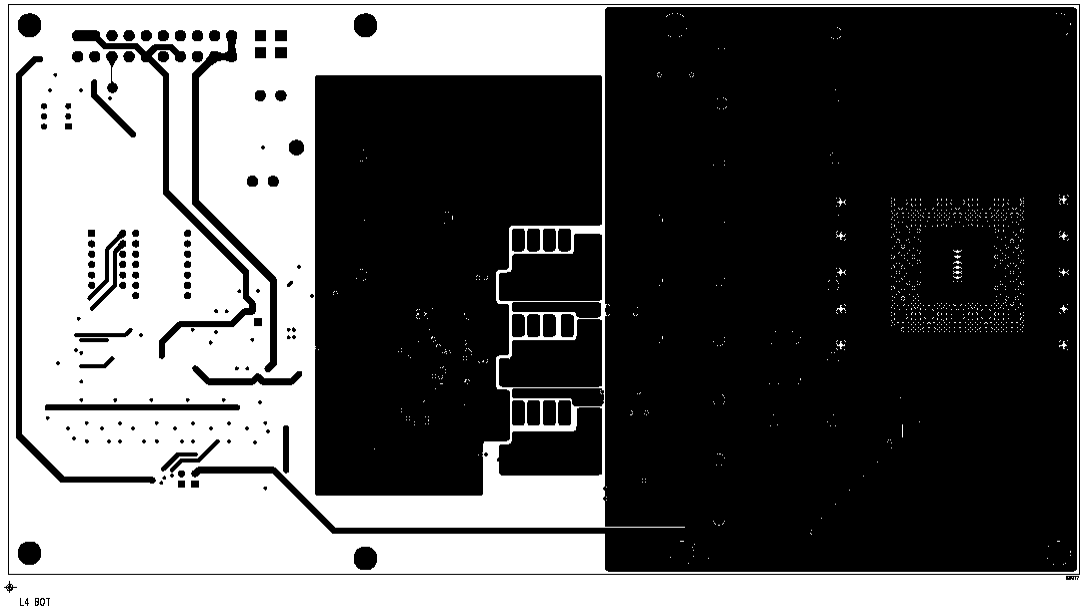
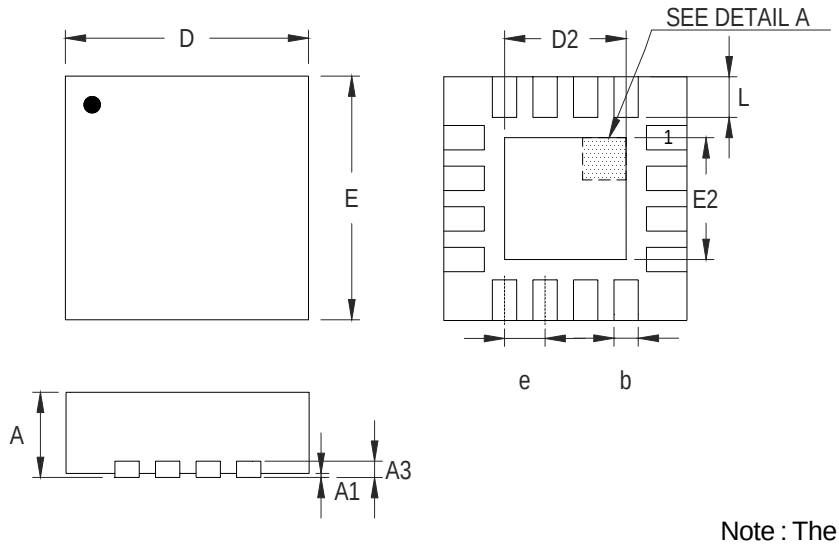
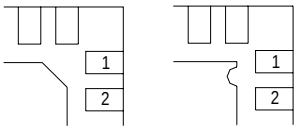


Figure 27

Outline Dimension





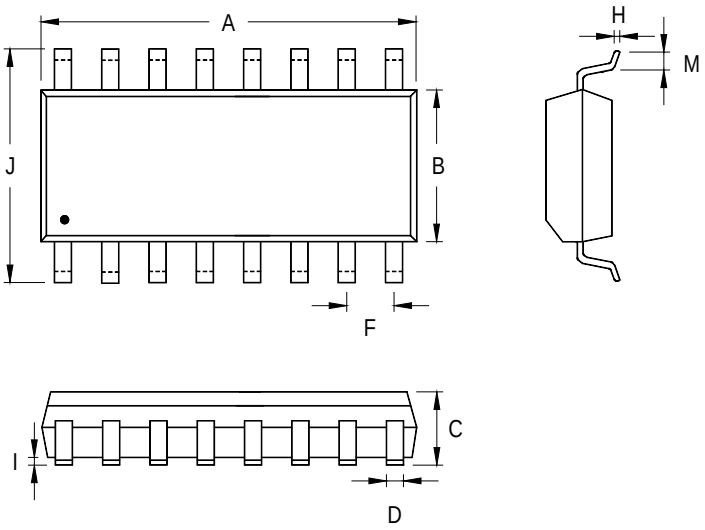
DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 16L QFN 3x3 Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	9.804	10.008	0.386	0.394
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050

16-Lead SOP Plastic Package

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