design ideas

Edited by Bill Travis

DPP adds versatility to VFC

Chuck Wojslaw, Catalyst Semiconductor, Sunnyvale, CA

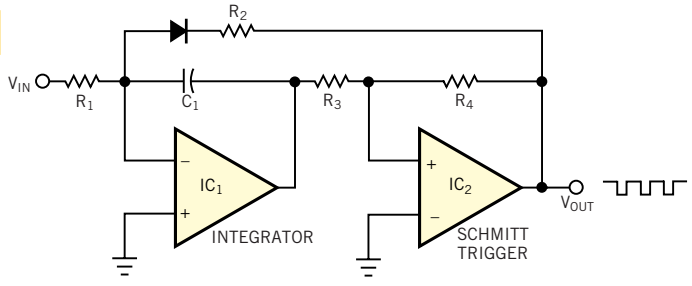
THE BASIC VFC (voltage-to-frequency converter) in **Figure 1** comprises an integrator (IC_1) and a Schmitt-trigger circuit (IC_2). The integrator converts the dc input voltage, V_{IN}, to a linear voltage ramp, and the Schmitt trigger sets the limits of the integrator's output voltage. Feedback around both circuits provides the condition for oscillation. The DPP (digitally programmable potentiometer) in **Figure 2** adds programmable limits to the Schmitt trigger and adds two powerful features to the VFC. First, the scale or conversion factor is programmable, and, second, for a fixed dc-input voltage, the converter is a programmable oscillator. The frequency, f_0, of the single-supply converter in **Figure 2** is:

$$f_o = f_{BASE}\frac{(1-p)}{p}\frac{(V_{IN}-2.5V)}{5V};$$

$$0<p<0.5, \text{ and } 2.5V<V_{IN}<5V,$$

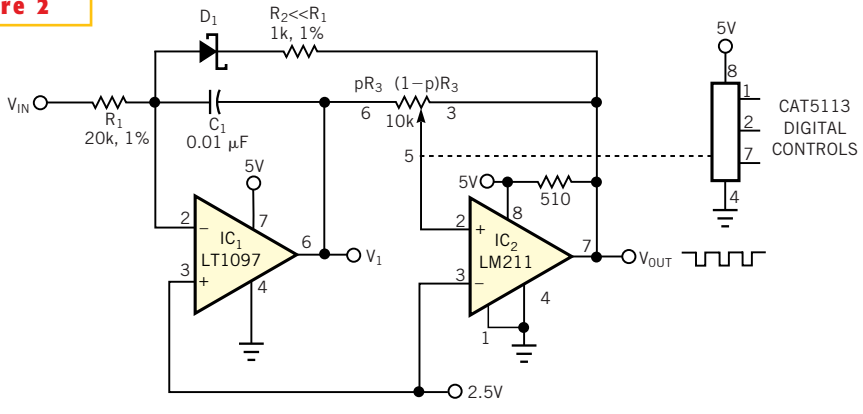
where $f_{BASE}=1/2\pi R_1C_1$, and p is the relative position of the wiper from one end (0) of the DPP to the other end (1). For the100-tap Catalyst (www.catsemi.com)

Figure 1



This schematic depicts a basic voltage-to-frequency converter.

Figure 2



Using a digitally programmable potentiometer, you can vary the scale factor of this voltage-to-frequency converter.

5113 potentiometer, the range of the scale-factor term (1-p)/p is 1 to 99 with a resolution and accuracy of approximately 1%. For the values shown in **Figure 2**, the practical range of frequencies is 500 Hz to 25 kHz. Higher bandwidth, rail-to-rail CMOS versions of IC_1 and IC_2, and a greater R_1/R_2 ratio can extend the accuracy and range of the circuit. The automated, accurate setting of the scale factor saves manufacturing test time and eliminates the need for expensive, accurate resistors and capacitors. The scale factor relates to the ratiometric temperature coefficient of the DPP and hence is minimally temperature-dependent. You can use the circuit as a programmable oscillator when V_{IN} is fixed and the potentiometer's wiper setting changes the limits of the Schmitt trigger.

Is this the best Design Idea in this issue? Select at www.edn.com.

Publish your Design Idea in *EDN*. See the What's Up section at www.edn.com.

Power circuit terminates DDR DRAMs

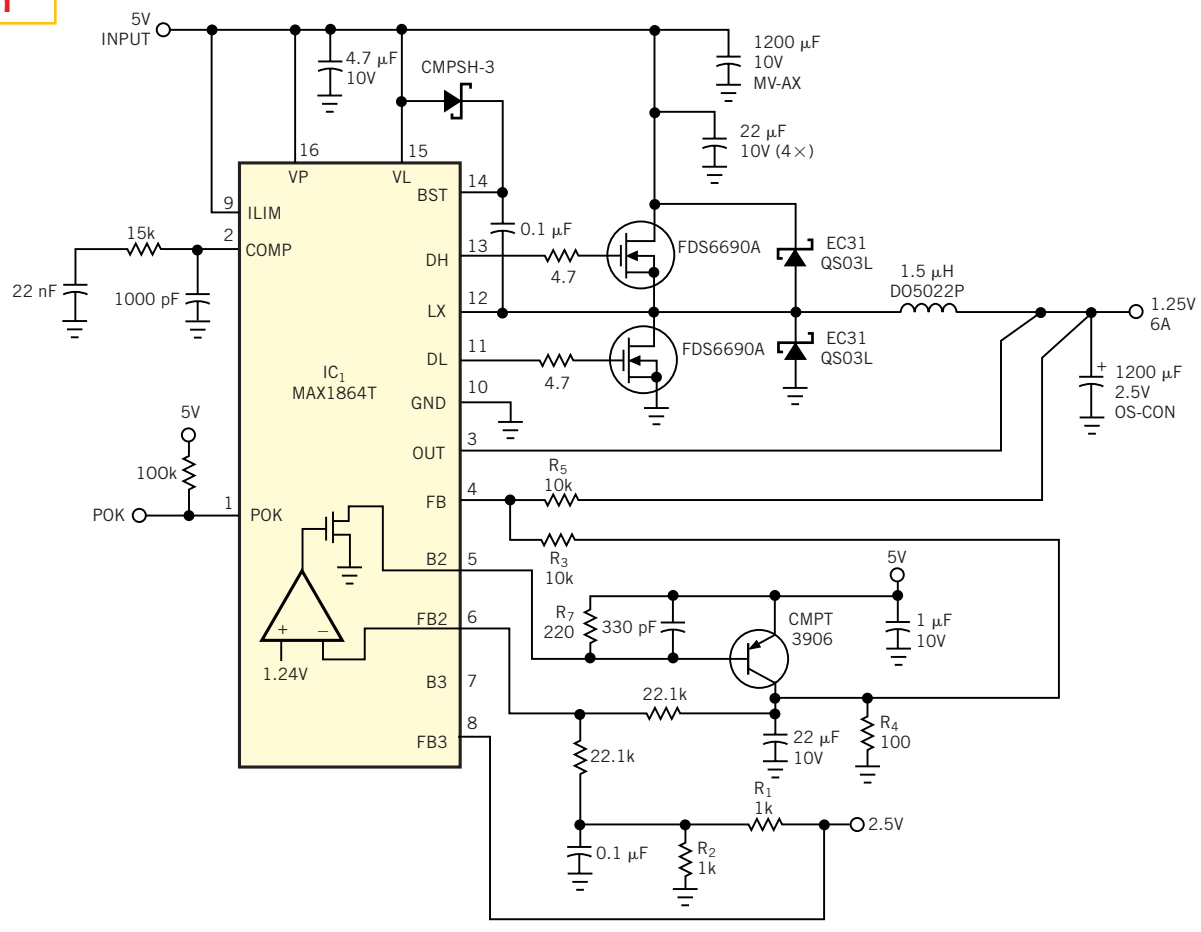
Ron Young, Maxim Integrated Products, Sunnyvale, CA

DDR (DOUBLE-DATA-RATE) SDRAMs find use in high-speed memory systems in workstations and servers. The memory ICs operate with 1.8 or 2.5V supply voltages and require a reference voltage equal to half the supply voltage ($V_{REF}=V_{DD}/2$). In addition, the logic outputs terminate with a resistor to the termination voltage, V_{TT}, which equals and tracks V_{REF}. V_{TT} must source or sink current while maintaining $V_{TT}=V_{REF}\pm 0.04V$. The circuit of **Figure 1** provides the termination voltage for both 1.8 and 2.5V memory systems and delivers output current as high as 6A. IC_1 includes a step-down controller and two linear-regulator controllers and operates with input voltages of 4.5 to 28V.

IC_1's fixed-frequency, 200-kHz PWM controller maintains the output voltage by sourcing and sinking current. Maximum sink current equals the maximum source current, though the sink current has no current limiting. When sinking current, the device returns some current to the input supply. To implement the tracking function, one of IC_1's extra linear-regulator controllers is configured as an inverting amplifier. This amplifier compares $V_{DD}/2$ (created by R_1 and R_2) with V_{REF} from IC_1 and generates an error signal that connects via R_3 to IC_1's FB pin, thereby forcing V_{OUT} to track $V_{DD}/2$. A 10-mA load, R_4, is necessary to bias the inverting amplifier for accurate tracking. V_{OUT} can track $V_{DD}/2$ for V_{DD} in the range 1 to 4V.

Is this the best Design Idea in this issue? Select at www.edn.com.

Figure 1

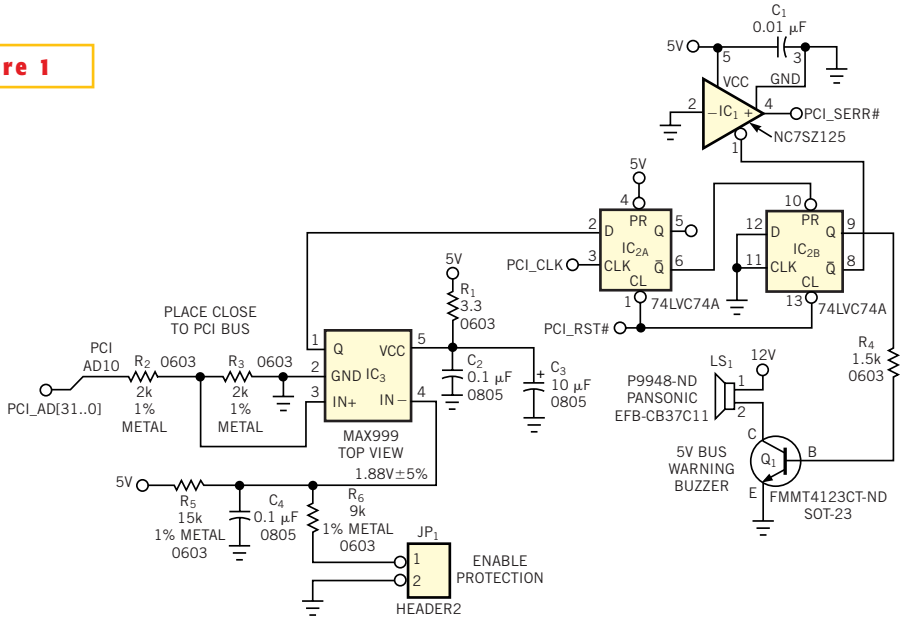


This circuit generates the termination voltage for DDR synchronous DRAMs.

Circuit protects bus from 5V swings

Said Jackson, Equator Technologies Inc, Campbell, CA

Figure 1



This circuit provides both an audible alarm and an error flag when an overvoltage condition exists.

THE CIRCUIT IN **Figure 1** automatically detects voltage and protects a bus, such as a 3.3V-limited PCI bus, from 5V signal-level swings. You can also use the circuit to determine bus-voltage swings within one bus-cycle for setting appropriate termination voltages of protection diodes or termination resistors. Today's deep-submicron VLSI-manufacturing techniques sometimes require circuits to limit I/O voltages to 3.3V signal swings. Connecting such circuits to a bus with 5V level-swing cards could damage the circuitry. The circuit in **Figure 1** can accurately and—within one bus cycle—detect a level swing larger than 3.3V on any bus and, upon a fault situation, generate a reset signal and an alarm output to notify the user and the system of this fault. Some of the novel circuit features include a highly accurate synchronous-detection capability to avoid false alarms arising from large signal overshoots, high impedance and low capacitive loading of the bus, automatic system shutdown during fault conditions, and a single-cycle response time.

This circuit successfully operates in products using the high-performance 3.3V MAP-CA processor family from Equator Technologies (www.equator.com), but you can use it in other high-speed 3.3V or even lower voltage systems. Equator's latest generation chips are 5V-tolerant, but you can adjust the circuit to protect other 1.8 and 2.5V chips. The circuit uses IC_3, an ultrahigh-speed Maxim (www.maxim-ic.com) MAX999 comparator with 4.5-nsec propagation delay, T_{PD}, to constantly compare a signal line, PCI_AD10 in case of a PCI bus, to a reference level of 3.8V. This reference voltage is an optimal compromise between 5V signals clamped by 3.3V protection diodes and the normal-operation 3.3V signals. Once the voltage exceeds this reference level for an entire bus clock period, the system turns on an alarm buzzer connected to Q_1.

The circuit generates a signal that can reset the system, or it can generate a system-error signal. Because the alarm-register memory, IC_{2B}, serves as an asynchronous register, you can switch the alarm off only by removing power from the system or by asserting the reset signal. To avoid false triggering by signal overshoot and undershoot, a flip-flop-based register, IC_{2A}, samples the comparator output only during the rising edges of the bus clock. This method allows for a generous 33-nsec period at 33 MHz for the bus signal to settle down before being sampled. Lowpass filtering by sensor resistors R_2, R_3 and the 3- to 5-pF parasitic capacitance on Pin 3 of IC_3 limit the maximum clock speed of this circuit. The traces connecting to Pin 3 of IC_3, R_2, and R_3 thus must be as short as possible and may limit the bus speed to approximately 40 to 50 MHz. Symmetrically lowering the resistance of R_2 and R_3 increases the maximum bus speed to a theoretical 7-nsec cycle time (greater than 140 MHz) at the expense of a higher signal-loading current on the bus.

In the case of monitoring a PCI bus, Pin 3 of comparator IC_3 monitors signal PCI_AD10. Every PCI device asserts this signal at least once during PCI enumeration, but you can monitor other signals if necessary. This method guarantees recognition of a 5V PCI device shortly after the BIOS starts enumerating the PCI bus during system boot. IC_{2A} then latches the comparator's, IC_3, Q-output Pin 1 during the rising edge of the PCI clock. This action asserts flip-flop IC_{2B}, which in turn enables buzzer LS_1 and generates an open-collector, low-active, system-error signal through IC_1. You could use this error signal to automatically remedy the fault condition by disabling the offending circuit on the bus. The sense and reference resistors R_2, R_3, R_5, and R_6 should be metal-film 1% types. The 5V reference voltage connected to R_5 determines the accuracy of the trip voltage, and today's power regulators have sufficient accuracy so that you can use a 5V system-power line as the reference voltage, obviating the need for a special 5V-reference generator. Removing jumper JP_1 disables the circuit.

Is this the best Design Idea in this issue? Select at www.edn.com.

Use a 555 timer as a switch-mode power supply

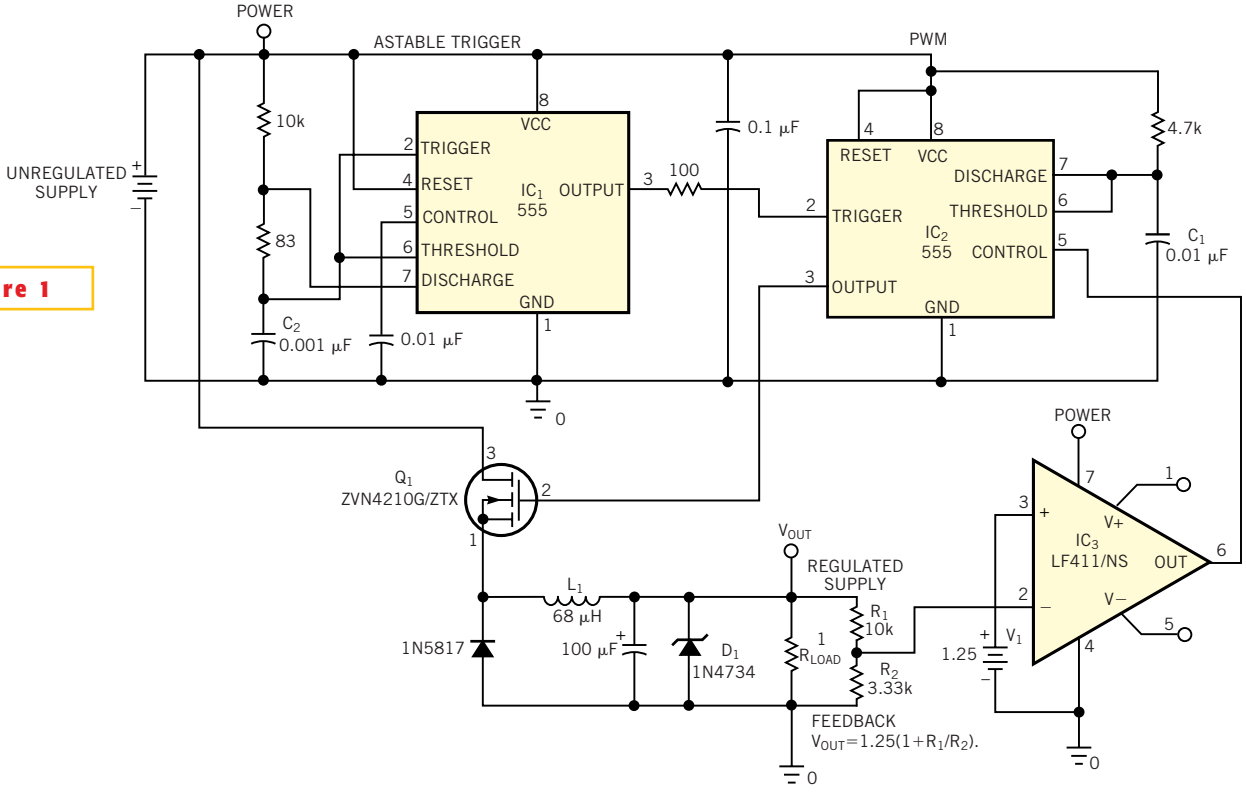
Aaron Lager, Masterwork Electronics, Rohnert Park, CA

Most switch-mode power supplies rely on a PWM (pulse-width-modulated) output that is controlled via voltage feedback. A 555-timer IC can inexpensively perform PWM. The circuit in **Figure 1** shows how to turn a 555 PWM circuit into an switch-mode power supply with only one simple equation. The design uses two 555s. IC_1, in astable mode, triggers IC_2 in PWM mode. IC_1 is set to oscillate at approximately 60 kHz at a high duty cycle. The output is low for only approximately 2.5 µsec to trigger the PWM circuit and then goes high for the rest of the period. The PWM circuit has a maximum pulse width of approximately 85 µsec, and it becomes shorter, depending on the control voltage from the feedback circuit. You can reduce the chip count by using a 556 or another continuous-trigger source. The input must be ($1.5V_{OUT}$+Margin), so for 5V output you need 9V minimum input. If you use CMOS chips and small timing capacitors C_1 and C_2, you can keep the operating current low. Thus, you can use a simple zener-diode regulator for the 555 and increase the input voltage to more than 30V. The input-voltage limit is a function of how much power the zener supply can handle while delivering 5 to 10 mA to the 555s.

Q_1 has low $R_{DS(ON)}$ and low V_{GS} and can handle more than 40V. D_1 clamps any voltage spikes, such as those that occur when a large current flow ceases, causing a large magnetic field to be left in the inductor. You should select D_1 according to the output voltage you need. For 5V output, use a 5.6V zener diode, for example. IC_3, R_1, R_2, and V_1 form the feedback circuit to set the output voltage. The output-voltage equation is $V_{OUT}=V_1(R_1/R_2+1)$. The TL431 is a popular part for setting a voltage reference and can easily create the 1.25V shown for V_1. You can supply 5V at 1.5A with an input of 9 to 40V. At voltages higher than 12V, you can add a 10V zener-diode supply for the chips. The zener supply only slightly reduces the efficiency. With 12V input, 5V, 1.5A output efficiency is approximately 70%, and it drops to 65% with a 40V input and a zener circuit. The zener diode's influence is more noticeable at lower current levels; at a 50-mA load the efficiency drops to approximately 50%.

Is this the best Design Idea in this issue? Select at www.edn.com.

Figure 1



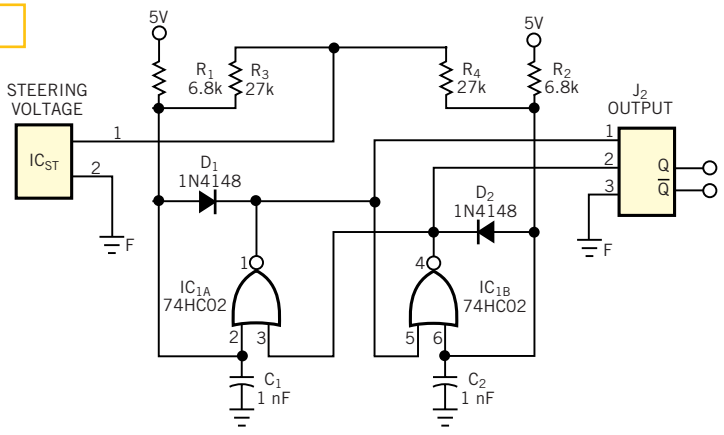
Here's one more use for the ubiquitous 555 timer: a switch-mode power supply.

VCO uses programmable logic

Susanne Nell, Breitenfurt, Austria

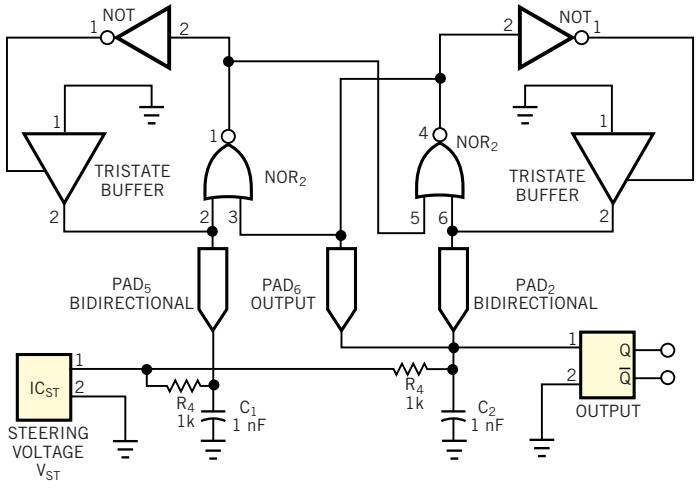
A VCO (voltage-controlled oscillator) is an analog circuit, so you cannot find it in the libraries for the design of digital programmable chips. When you need such a circuit for synchronization or clock multiplication, you need to find a circuit that works with the standard digital functions, such as AND and NAND. Several possibilities exist for building variable-frequency oscillators. For example, you can change the frequency using a varactor diode. Unfortunately, these diodes have a small change of frequency per volt. So, the standard Pierce oscillator with one inverter and capacitors is not useful for these applications. Another idea is to use a Schmitt-trigger inverter and to vary the charging resistor. This method can work, but the hysteresis of the IC usually has a wide tolerance, so the selected inverter chip has a large influence on the frequency.

Figure 1



This unique VCO, implemented with discrete logic, has a wide tuning range.

Figure 2



This VCO uses an EPLD and has high gain, expressed in kilohertz per volt.

For these reasons, this design modifies a two-NOR-gate RC oscillator (**Figure 1**) to function as a VCO. For almost all pure-CMOS circuits, the switching point between high and low states is approximately $V_{CC}/2$. This point does not depend on the device. Using this circuit, you can obtain a wide frequency-tuning range. The output is a square wave with a 50% duty cycle. At power-on, both capacitors C_1 and C_2 are uncharged, and IC_{1A} has a low output. Thus, the output of IC_{1B} is high, and C_2 charges with the time constant R_2C_2. The additional charging current from IC_{ST} and R_4 also influences this charging time. When the voltage on C_2 reaches $V_{CC}/2$, IC_{1B} switches to a low state. Now, the output of IC_{1A} switches high, and C_1 charges with time constant R_1C_1, influenced by IC_{ST} and R_3. The low signal at the output of IC_{1B} forward-biases D_2 and quickly discharges C_2.

This circuit produces a 50% duty cycle if $C_1=C_2$, $R_1=R_2$, and $R_3=R_4$. The values of R_4 and R_3 and the steering voltage, V_{ST}, determine the VCO's gain in kilohertz per volt. The circuit in **Figure 2** yields the highest possible value for the VCO's gain. The circuit uses an Altera (www.altera.com) EPLD (erasable programmable-logic device), the EPM3032. Tristate buffers replace the diodes in **Figure 1**, and the charging resistors connect directly to the steering voltage. This configuration produces the highest possible VCO gain: approximately 700 kHz/V for the component values shown. You can switch off the VCO by using a steering voltage lower then $V_{CC}/2$. You can implement this circuit using almost all programmable-logic devices with CMOS inputs. You can also use steering voltages much higher then the supply voltage of the programmable chip, because the voltage on the input of the chip never goes higher then $V_{CC}/2$. This fact makes the circuit suitable as a voltage-to-frequency converter with a high input-voltage range.

Is this the best Design Idea in this issue? Select at www.edn.com.

Controlling slew times tames EMI in offline supplies

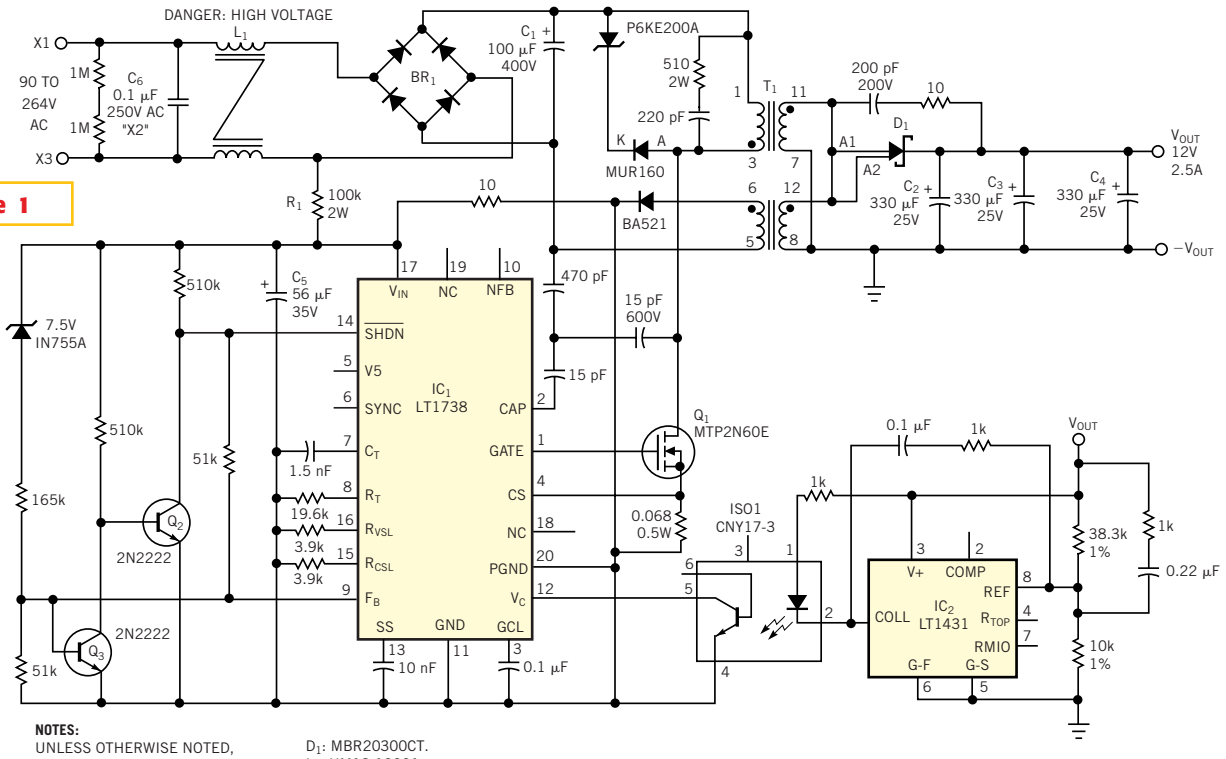
David Canny, Linear Technology Corp, Milpitas, CA

EMI from offline switching power supplies typically causes all sorts of problems for power-supply designers. You may need a large EMI filter to meet FCC emission requirements. Switchers for high efficiency produce high-frequency switching noise that can propagate through the rest of the system and cause problems. Board layout is critical, requiring considerable experimentation, even for experienced designers. The low-noise circuit in **Figure 1** significantly reduces the complexity of these issues by continuous, closed-loop control of the voltage and current slew rates. High-frequency noise suppression is particularly important for medical devices because they don't require the ac-line-to-earth ground capacitors ("Y" capacitors) that typically suppress this noise. The absence of these capacitors allows medical devices to easily comply with the more stringent low-leakage-current healthcare specifications of UL544, UL2601, and CSA22.2.

Figure 1 shows a 30W (12V output at 2.5A) offline power supply. IC_1, an LT1738 low-noise switching regulator in a flyback topology, drives Q_1 and continuously controls the current slew using the resistor at the R_{CSL} pin. The IC controls the voltage slew using the resistor at the R_{VSL} pin and the capacitance at the CAP pin. IC_2, an LT1431 programmable reference, and the optocoupler close the isolated loop back to the LT1738. The circuit achieves current limit by sensing the current through a 68-mΩ resistor at the CS pin. Q_2, Q_3 and their associated circuitry provide undervoltage lockout with hysteresis. During start-up, the $\overline{SHDN}$ pin stays low until C_5 charges to 12V via R_1. The LT1738 then turns on and subsequently obtains most of its operating power from T_1's auxiliary winding. The feedback goes directly to the LT1738's V_C pin rather than to the F_B pin because the optocoupler provides the feedback gain that the LT1738's internal feedback amplifier typically provides. C_6 and L_1 attenuate the low-frequency harmonics of the LT1738 switching frequency.

You can see the benefits of the circuit by measuring its ac-line-conducted EMI and then comparing these measured results with those for basically the same circuit with the LT1738 replaced with a

Figure 1



NOTES:
UNLESS OTHERWISE NOTED,
ALL RESISTORS: 1206,5%.
BR_1: GENERAL INSTRUMENTS WO6G.
C_2, C_3, AND C_4: SANYO MV-GX.
D_1: MBR20300CT.
L_1: HM18-10001.
T_1: PREMIER MAGNETICS POL-15033.

A 30W offline power supply passes FCC Class B emission requirements without line-to-earth-ground capacitors.

generic switcher. The only circuit-parameter difference is that, unlike the LT1738, the generic switcher doesn't actively control the switching current and voltage slew rates. **Figure 2** shows the frequency spectra for both circuits. You can see by the respective frequency spectra that the LT1738-based circuit generates emissions well within FCC Class B requirements, whereas the circuit with the generic part results in emissions that exceeds FCC Class B allowable emissions by a significant margin.

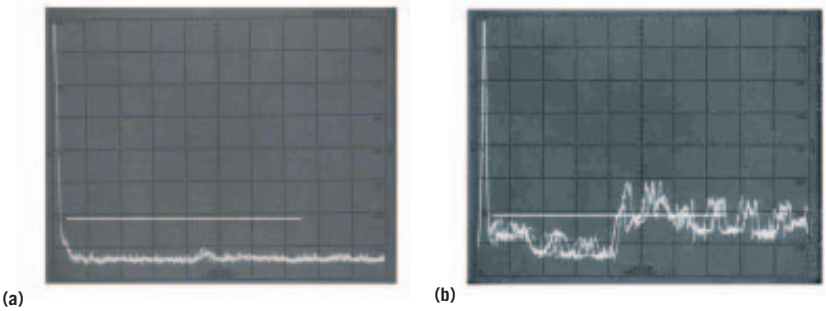


Figure 2 In these 50-MHz-wide spectral plots, areas under horizontal lines indicate acceptable FCC Class B emission requirements. The spectral plot for the LT1738-based circuit (a) shows emissions well within FCC Class B requirements, unlike the plot for the generic switcher (b).

Another benefit of the circuit in **Figure 1** is that the output voltage noise comprises the fundamental ripple with practically no high-frequency components. You can attenuate this ripple voltage if desired to less than 300 μV using a 100-μH, 100-μF LC filter on the output. The generic switcher, on the other hand, produces more output noise because the high-frequency noise passes to the output with little attenuation through the parasitic capacitance of the output filter's inductor. The circuit in **Figure 1** minimizes noise and EMI by controlling the voltage and current slew rates of the external n-channel MOSFET. This circuit is well-suited for offline power supplies in medical devices because the absence of Y capacitors results in low leakage current to earth ground in compliance with health-care specifications.

Is this the best Design Idea in this issue? Select at www.edn.com.