



Edited by Bill Travis

Circuit controls microneedle etching

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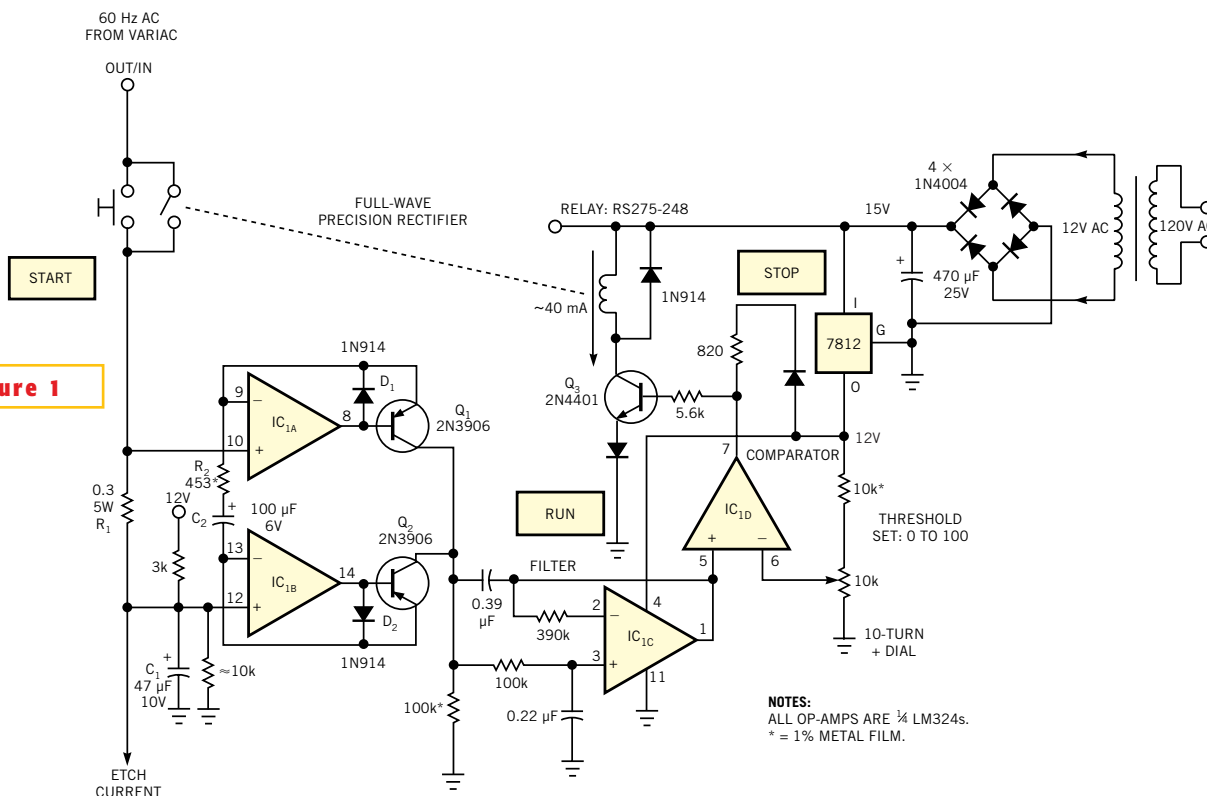
AT ITS INVENTION roughly two decades ago, STM (scanning tunneling microscopy) created a sensation because it was the first technology to make atomic-scale-resolution imaging a routine procedure. An essential requirement for the practical application of STM is some means for the reproducible fabrication of supersharp, atomic-scale needle tips. One way to make the tips is to etch them from short pieces of platinum wire in a calcium-chloride electrolyte bath. Applying an ac voltage between the electrolyte and the wire generates a chemical reaction accompanied by vigorous fizzing at the surface of the liquid. This reaction etches the platinum, causing the wire to neck down and eventually break into two

pieces. If the etching current turns off within milliseconds of the wire's breaking, then the point of separation remains supersharp. This sharp point is suitable for use as a high-quality STM tip. Swift interruption of the current, however, is essential to tip sharpness, because only a few milliseconds of overetch suffice to dull and ruin the tip. The circuit in **Figure 1** achieves precision etch-termination by using relay-actuated etch turn-off based on the sudden drop in etch current that occurs when the wire parts. Precision sensing and full-wave rectification of the etch current is critical to circuit operation; the circuit achieves this precision by using an unusual differential-input rectifier.

Precision, full-wave rectification of low-level ac signals to a dc format is a common signal-processing function; many classic rectifier topologies accom-

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Figure 1



This etch-control circuit produces supersharp microneedles by terminating the etching process at precisely the right time.

plish this function. But the accuracy of typical precision rectifiers depends on the precise matching of resistor ratios. Moreover, op-amp input-offset voltages limit the accuracy of these standard circuits. The offset error generally limits sensitivity to input spans no smaller than some hundreds of millivolts. The converter in this design avoids these faults and adds a number of new and useful features. The differential ac signal to be rectified goes to the noninverting inputs of op amps IC_{1A} and IC_{1B} (Figure 1). Rectification proceeds as follows: Consider a signal excursion, V_{IN}, that drives IC_{1A}'s input more positive than IC_{1B}'s. Amplifier IC_{1A} responds by driving diode D₁ into conduction, thereby forcing R₂ to track the in-

put. Amplifier IC_{1B} responds with a negative output excursion, forcing transistor Q₂ to conduct sufficiently to cause the inverting input of IC_{1A} and the bottom end of R₁ to track. Q₂'s emitter current, and therefore, collector current is then $I = V_{IN} / R_2 = V_{R1} / R_2$; Q₂ is a high-alpha transistor.

The respective roles of the amplifiers reverse for input excursions of the opposite polarity, with D₂ and Q₂ conducting. The match of Q₁ and Q₂ alpha values, which is typically 0.3% or better, is the only limit on rectification symmetry. This precision rectifier is therefore unique in that neither rectification symmetry nor common-mode rejection, which exceeds 60 dB, depends on resistor

matching. Meanwhile, C₂ affords ac coupling, which eliminates offset-voltage-related errors. Operation of the rest of the etch controller is straightforward. IC_{1C} implements a unity-gain, two-pole Butterworth lowpass filter for good ripple attenuation without excessive time delay. Etching begins when you push the Start pushbutton. The etch-current comparator, IC_{1D}, then drives Q₃ to keep the relay energized until the etch current drops below the level set by the Threshold Set potentiometer. IC_{1D}'s output then drops low, turning Q₃ off, opening the relay, and terminating the etch. The result is a serviceable, atomically sharp scan tip almost every time. □

Circuit removes relay-contact bounce

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ADVANCES IN SEMICONDUCTOR technology have allowed ICs to replace many mechanical relays, but relays still dominate in high-current circuits that must stand off high voltages of arbitrary polarity. Contact bounce in those

drives the relay closed, and that relay closure connects the input of the hot-swap controller to the power supply: 28V, in this case. The hot-swap controller, IC₁, keeps the p-channel MOSFET, Q₁, off for a minimum of 150 msec after the input supply reaches a valid level. That delay allows ample time for contact bounce in the relay to subside. After the 150-msec delay, IC₁ drives the MOSFET gate such that the output voltage slews at 9V/msec. This controlled ramp rate minimizes the inrush current, thereby reducing stress on the power supply, the relay, and capacitors downstream from the hot-swap controller.

An example of relay contact bounce shows three bounces with an inrush-current peak of almost 30A (Figure 2). The top trace is output voltage at 10V/division, the lower trace is input current at 5A/division, and the output load is 54Ω in parallel with 100 μF. Use of the Figure 1 circuit under these conditions yields a better picture (Figure 3). The delayed rise in output voltage is clearly visible, with no hiccups arising from contact bounce. The input

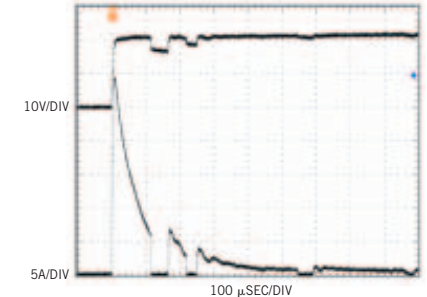


Figure 2 The mechanical relay, K₁, by itself exhibits contact bounce on closure as shown.

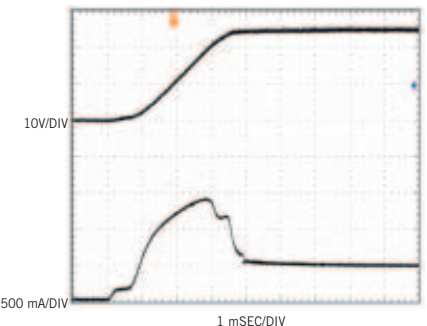


Figure 3 The Figure 1 circuit removes relay-contact bounce and reduces inrush current.

current shows much less variation, peaking under 1.5A before settling to a steady-state value of 500 mA. □

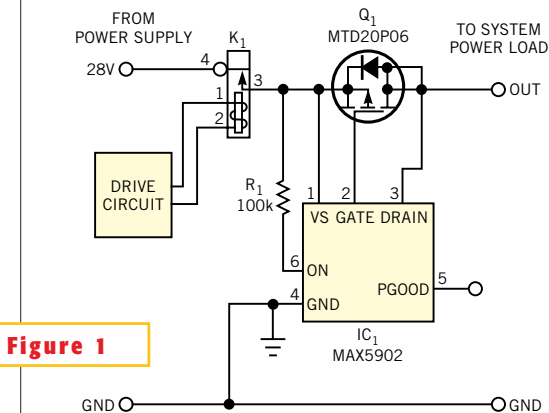


Figure 1

A hot-swap controller IC and external MOSFET removes contact bounce from relay K₁.

relays, however, can prove troublesome to downstream circuitry. One approach to contact bounce combines a relay with a hot-swap controller. Such controllers are increasingly popular as the means for switching system components without shutting down the system power. In Figure 1, a relay contact replaces the pin of a mechanical connector. The drive circuit

Log-ratio amplifier has six-decade dynamic range

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YOU NEED OPTICAL-POWER monitoring to guarantee overall system performance in fiber-optic communication systems. Logarithmic-signal processing can maintain precise measurements over a wide dynamic range. The wide-dynamic-range signal undergoes compression, and the use of a lower resolution measurement system then saves cost. As an example of this technique, consider a photodiode with responsivity of 0.5A/W that converts light energy to a current of 100 nA to 1 mA. With a four-decade dynamic range and 1% error, the required measurement resolution is 0.01×10^{-4} , or 1 ppm. This measurement requires a 20-bit ADC. Instead, you can compress this input to a 0 to 4V range using a log-ratio amplifier and then use a 10-bit ADC, substantially reducing the system cost. Programming the reference current allows shifting the output voltage to the desired level. You can customize and use the circuit in **Figure 1** in applications involving unusual combinations of dynamic range; input signal, such as

voltage or current; polarity; and scaling; or operations such as log products and ratios. Log-ratio amplifiers find applications in wide-dynamic-range ratiometric measurements, which measure an unknown signal against a variable-current reference. The transfer function of the circuit in **Figure 1** is:

$$V_{OUT} = K \times \log_{10} \left(\frac{I_{IN}}{I_{REF}} \right);$$

$$K = -2.303 \frac{(R_T + R_2) \times V_T}{R_{(T)}}$$

where K is the output scale factor, I_{IN} is the current that the photodiode generates, V_T is a temperature-dependent term (typically, 26 mV at 25°C and proportional to absolute temperature), and I_{REF} is the reference current. $V_{OUT} = 0$ when $I_{IN} = I_{REF}$. For proper operation, I_{IN}/I_{REF} should always be greater than 0. The output of the log-ratio circuit can be positive, negative, or bipolar, depending on the ratio of I_{IN}/I_{REF} . The 4V full-scale in-

put range of the ADC sets the 4-mA full-scale input-current range. Programming I_{REF} to a value of 40 to 600 μ A places the output in the middle of the measurement range.

The components give an output-scale factor of -1 . This circuit has an output defined over a range of 4.5 decades of signal current, I_{IN} , and 1.5 decades of reference current, I_{REF} (limited by the load-driving capability of the reference for a total six-decade range. For most applications, you would use only a portion of the entire six-decade range. By determining the range of the expected input signals and computing their ratios, you can use the equations to predict the expected output-voltage range. You can assign I_{REF} and I_{IN} to match device performance to the current range, but you should observe polarity.

A log amplifier generally depends on the nonlinear transfer function of a transistor. The general transfer function of a log amplifier is related to I_S and V_T , which both depend on temperature. I_S is the

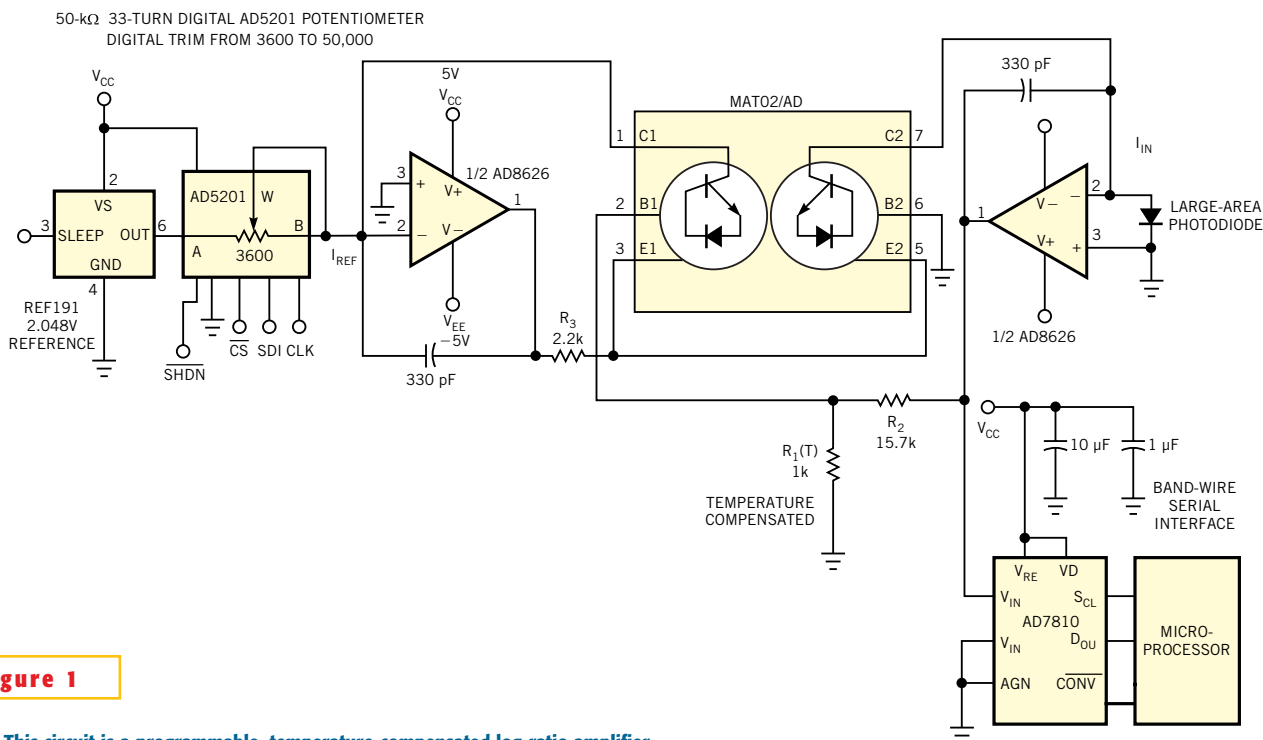
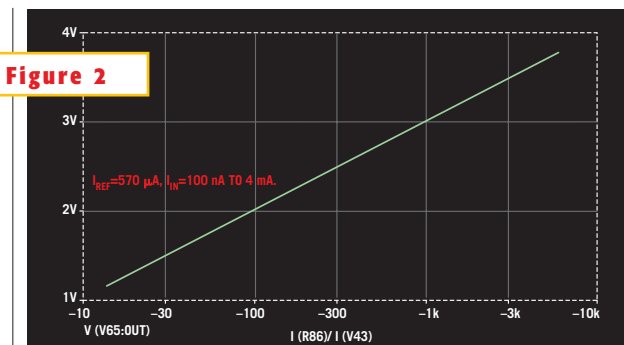
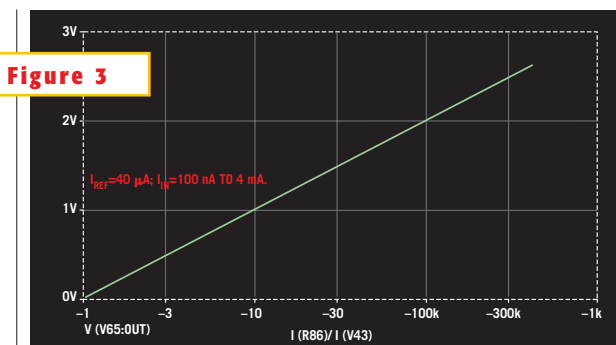


Figure 1

This circuit is a programmable, temperature-compensated log-ratio amplifier.



V_{OUT} has I_{REF} programmed to full scale of 570 μ A.



V_{OUT} has I_{REF} programmed to zero scale of 40 μ A.

transistor's collector saturation current, and V_T is the transistor's "thermal voltage." To overcome this temperature dependency, this design uses a matched pair of MAT02 transistors to cancel the I_S temperature drift and a temperature-sensitive resistive voltage divider to compensate for the temperature coefficient of V_T . The heart of the I_{REF} generator is a REF191. You adjust its output with an AD5201 digital potentiometer. This modification allows you to program the

reference current in 33 steps, from 40 to 600 μ A.

The combination of the REF191 and the AD5201 provides a current source that is stable with respect to time and temperature. For higher resolution, you can use the 1024-position AD5231. The AD8626 is a dual precision-JFET-input amplifier with true single-supply operation to 26V, low power consumption, and rail-to-rail output swing, allowing a wide dynamic range. Its output is stable with

capacitive loads in excess of 500 pF. **Figures 2 and 3** show the transfer function of the log-ratio amplifier at the input of the ADC. The output is limited to 0 to 4V to match the unipolar input-voltage range of the AD7810 ADC. □

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VCXO makes inexpensive dual-clock reference

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THIS DESIGN IDEA describes an inexpensive circuit to generate two extremely high-quality, crystal-clock-reference-signals, one of which is a PWM-controlled VCXO (voltage-controlled crystal oscillator) clock signal (**Figure 1**). The design also includes circuitry to statically switch and hold the VCXO at its nominal fixed frequency of operation (equivalent to 50% PWM) without requiring any external PWM stimulus. Most digital audio/video microprocessor-based systems today require several independent clocks with low jitter and the potential adjustability a VCXO provides. The described circuit replaces two expensive monolithic VCXO and crystal oscillators at a fraction of their cost and provides much higher quality output signals than the monolithic solutions can generate, especially at the control limits of the VCXO ($\pm 100\%$ deviation). The circuit generates signals with higher stability, much lower jitter, lower operating voltage (3.3 versus 5V)

and a wider VCXO pull range than comparable monolithic approaches at less than one-third of their cost.

You can use the circuit in a wide variety of applications; the indicated component values make it a perfect fit for a digital audio/video system, such as a digital video recorder, digital camera, or set-top box. The circuit is well-suited to single-chip, media-processing applications that require adjustability, low cost, and low-jitter performance, such as systems based on Equator's (www.equator.com) broadband-signal processors. These types of systems generally require a fixed frequency, such as 25 or 33 MHz, for the processor subsystem (Ethernet, PCI bus, for example) and an adjustable 27-MHz reference clock for the audio/video reference subsystem. A PLL system generally controls the 27-MHz reference clock. (This PLL is usually implemented in software with PWM outputs from the microprocessor controlling the 27-MHz clock's deviation.) This approach guar-

antees a correct synchronization of the audio and the video data streams to each other and the broadcast source. The clock requires ± 50 -ppm adjustability, and the circuit in **Figure 1** provides more than ± 70 ppm. The circuit suits high-volume manufacturing, the highest quality signal (lowest jitter), and the lowest production cost.

The design incorporates several novel circuit features, such as both overtone- and harmonic-crystal operation, use of inexpensive voltage-controlled capacitors (varactor diodes), a single 3.3V power-supply operating voltage, and a selectable 50%-duty-cycle, 27-MHz-operation, fixed-frequency mode. The fixed-frequency mode allows operation at 27 MHz without the PLL-PWM circuit's having to provide a 50% duty cycle, potentially freeing up hardware and software resources in the microprocessor that usually generates the PWM signal. This mode is usually invoked when the audio/video signals are generated internal-

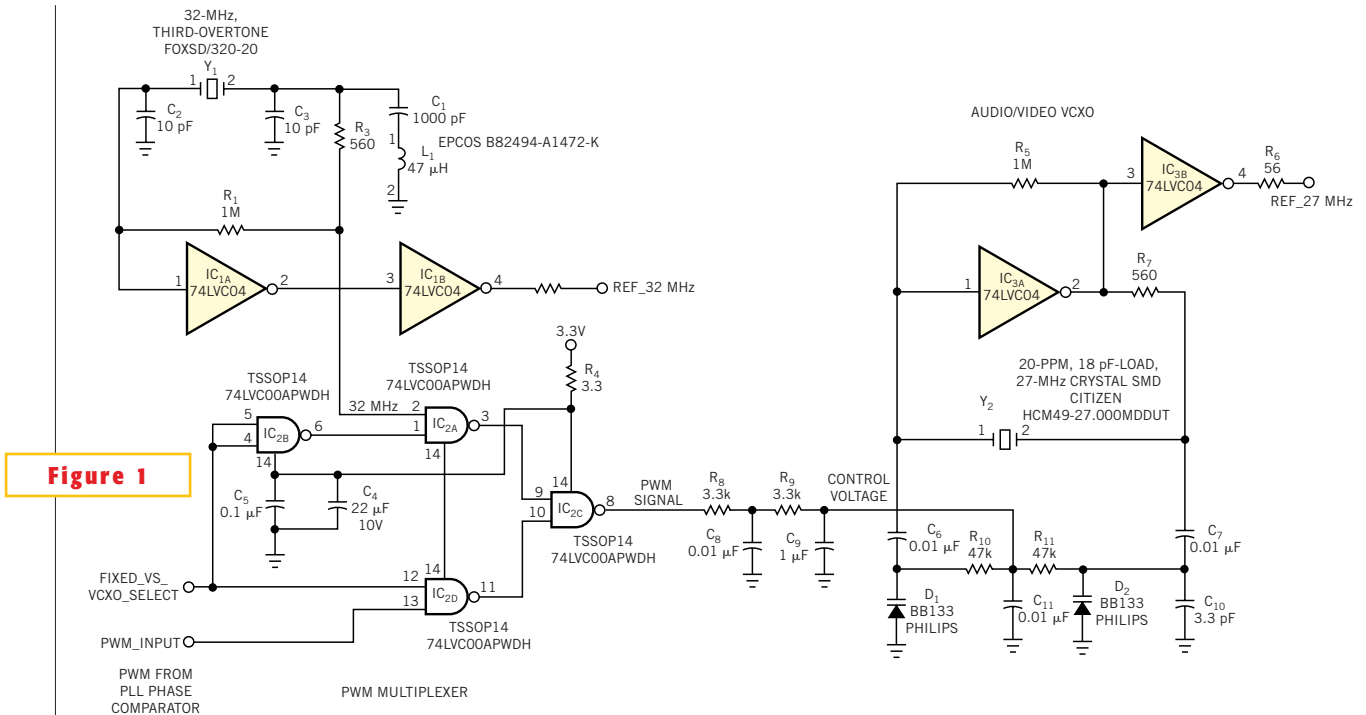


Figure 1

This circuit, ideal for A/V applications, generates two high-quality clock-reference signals.

ly to the system, such as when playing back from a hard drive, and audio/video synchronization to an external source is unnecessary.

The circuit includes IC_{1A}, a 32-MHz, PCI-based fixed-frequency reference clock; IC₂, a PWM multiplexer; and IC₃, a 27-MHz VCXO clock. A Fox (www.foxonline.com) 32-MHz, third-overtone crystal serves to generate both the PCI reference clock and the 50%-duty-cycle reference for the fixed-frequency mode. A third-overtone, 32-MHz part is less expensive and more mechanically robust than a 33-MHz, fundamental-mode crystal at the expense of running the PCI clock slightly slower. The tank circuit around inductor L₁ and capacitors C₁ and C₃ prevent the crystal from oscillating at its fundamental mode of approximately 11 MHz. This tank circuit works by creating an LC series-resonant circuit between L₁ and C₃ that has natural resonance at approximately 24 MHz, which is approximately 75% of the desired 32-MHz frequency. Note that C₁ is large enough to have no effect on this tank circuit's resonance frequency; it merely acts as a dc blocker for inductor L₁. One thing to avoid is to connect this tank circuit to

the input side of inverter IC_{1A}. Connecting it to the input side of IC_{1A} could potentially create a resonant RC circuit with resistor R₁ and capacitor C₁ acting as the RC components. This circuit could oscillate at less than 1 kHz, a frequency at which L₁ would effectively be a short circuit, and crystal Y₁ would be an open circuit. Placing C₁ and L₁ on the output side of IC_{1A} prevents this spurious-oscillation mode.

By tuning L₁ and C₃, you can adjust the circuit to oscillate at a frequency higher than the third overtone. Oscillation at the fifth, seventh, or even ninth overtone is possible and is limited only by the performance of IC_{1A} and the parasitic capacitance. The 32-MHz PCI reference-clock output also serves as a 50%-duty-cycle reference for the VCXO when the VCXO is operating in its fixed-frequency, 27-MHz mode. Multiplexer IC₂ selects either this 32-MHz, 50% PWM clock signal or the PWM clock signal from a PLL phase comparator (usually implemented in the microprocessor and not shown in the schematic) to set the VCXO to its fixed-frequency mode. The advantage of using the PCI clock for this feature is that traditional circuits would

have to generate an analog one-half-V_{DD} voltage and use an analog multiplexer to set the VCXO at its nominal frequency. Thus, this design avoids the necessity of using accurate and expensive analog circuitry and also generates a reference signal with much higher immunity to temperature, for example, than analog approaches could provide.

Digital multiplexer IC₂ forwards one of two PWM signals to the VCXO based on the state of the fixed-versus-VCXO selected input signal. The PWM-input signal serves as the PWM reference input to the VCXO if the select pin is high, and the design uses the 50%-duty-cycle PWM signal from the PCI clock circuit if the select pin is low. The design uses a 74LVCO04 chip as a multiplexer because of its ready availability and low cost. IC_{2C} buffers the PWM signal, and the cascaded RC filter comprising R₈, R₉, C₈, and C₉ then low-pass-filters the signal. The analog-voltage stability of the VCXO control voltage at the output of this RC filter depends on the quality of the V_{DD} supply to IC_{2C}. IC₂ receives its 3.3V power through an RC filter: R₄ with C₄ and C₅, IC₂ with R₈, R₉, C₈, and C₉ thus form a highly accurate D/A converter.

The VCXO's lowpass filter uses a cascaded design, because stray 32-MHz noise could pass across the small parasitic capacitance inherent in R_8 into the analog VCXO-control voltage. Cascading also has the advantage of filtering noise with 12 dB of attenuation per octave for frequencies greater than 5 kHz, thus creating a noise-free VCXO control voltage. The 27-MHz audio/video VCXO circuit uses a fundamental-mode crystal that varactor diodes D_1 and D_2 load with adjustable capacitance. These back-biased diodes' junction capacitance depends highly on the bias voltage. Larger bias voltages lower their capacitance, thus lowering the load across the crystal and increasing its oscillation frequency. Diodes D_1 and D_2 find use in many tuners and are widely available. Capacitors C_6 and C_7 again function as dc blockers.

The adjustment range of the VCXO is

approximately $27 \text{ MHz} \pm 2 \text{ kHz}$, which calculates to approximately $\pm 74 \text{ ppm}$. The circuit is stable with very low jitter throughout its entire 0 to 100% VCXO-adjustment range. You can use the VCXO subcircuit by itself to generate a spread-spectrum clock for EMI compliance. You drive the VCXO voltage or PWM duty cycle from 0V (0%) to 3.3V (100%) with a triangular-shaped drive signal. The frequency of the triangular wave must be below the PWM RC filter's cutoff frequency of 24 Hz to be effective. The oscillator circuit's jitter depends on the power-supply quality of IC_1 , IC_2 , and IC_3 and on the noise inside these chips. To avoid crosstalk between 32 MHz and 27 MHz, the design uses two chips. Implementing buffers IC_{1B} and IC_{3B} with separate chips, thus separating the power-supply loading from the sensitive buffers, IC_{1A} and IC_{3A} , could further reduce jitter. With independent clock buffers and a

low-noise power supply, this circuit has exhibited a maximum cycle-to-cycle jitter of less than the 60-psec limitation of the HP54720D oscilloscope that measures it. This figure better the jitter characteristics of popular crystal oscillators and VCXO chips available for consumer applications. It also does not suffer from unstable operation at its adjustment margins (operating at $\pm 100\%$ deviation), as designers commonly encounter with monolithic components. Another added benefit is that it achieves its ± 74 -ppm adjustment range with only a single 3.3V power supply, whereas monolithic approaches usually require a 5V power supply and control voltage. Finally, it offers all this performance at a total price of less than \$1.40 in large quantities by using only commonly available, off-the-shelf components. This figure compares to \$3 to \$6 parts cost with monolithic approaches. □