design ideas

Edited by Bill Travis

DPPs program key parameters of bandpass filter

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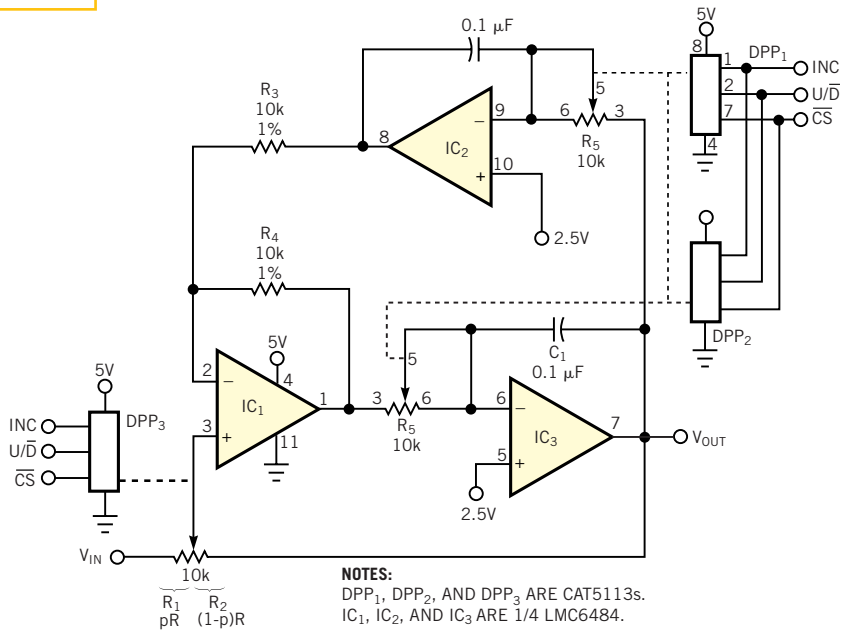
THE THREE-AMPLIFIER implementation of the state-variable filter in **Figure 1** provides for second-order bandpass, highpass, and lowpass responses. The strength of the circuit, however, is in the bandpass response (V_{OUT}/V_{IN}), in which it's easy to achieve high gain (G) and high Q. These two characteristics are important in applications in which selectivity is a key parameter in the filter. The application value of the circuit becomes even greater when DPPs (digitally programmable potentiometers) control and vary the bandpass filter's center frequency, f_0, and passband gain, G. The independent control of a bandpass filter's parameters is a rarity among traditional filter-circuit techniques.

For the filter, IC_1 functions as a summing amplifier, and IC_2 and IC_3 function as integrators. Three potentiometers, DPP_1, DPP_2, and DPP_3, program the center frequency and passband gain of the filter. The 100-tap Catalyst potentiometers, DPP_1 and DPP_2, are electronically ganged to program the frequency, f_0, and DPP_3 programs the gain, G. The center frequency is $f_0=1/(2\pi R_5C_1)=1/(2\pi pRC_1)$, and the gain is $G=R_2/R_1=(1-p)/p$, where p represents the relative position of the wiper from one end (0) of the potentiometer to the other end (1). R represents the DPP's end-to-end resistance. The gain and Q are related by $Q=(1+G)/2$. The increment/decrement interface of the CAT5113 DPP allows for real-time, closed-loop applications, in which you can continuously vary the center frequency of the filter to track an input signal or to accommodate a system-level requirement. For the values shown, the center frequency varies from less than 200 Hz to more than 6 kHz with gain values as high as 25.

Figure 1



Using digitally programmable potentiometers, you can control a passband filter's center frequency and gain.

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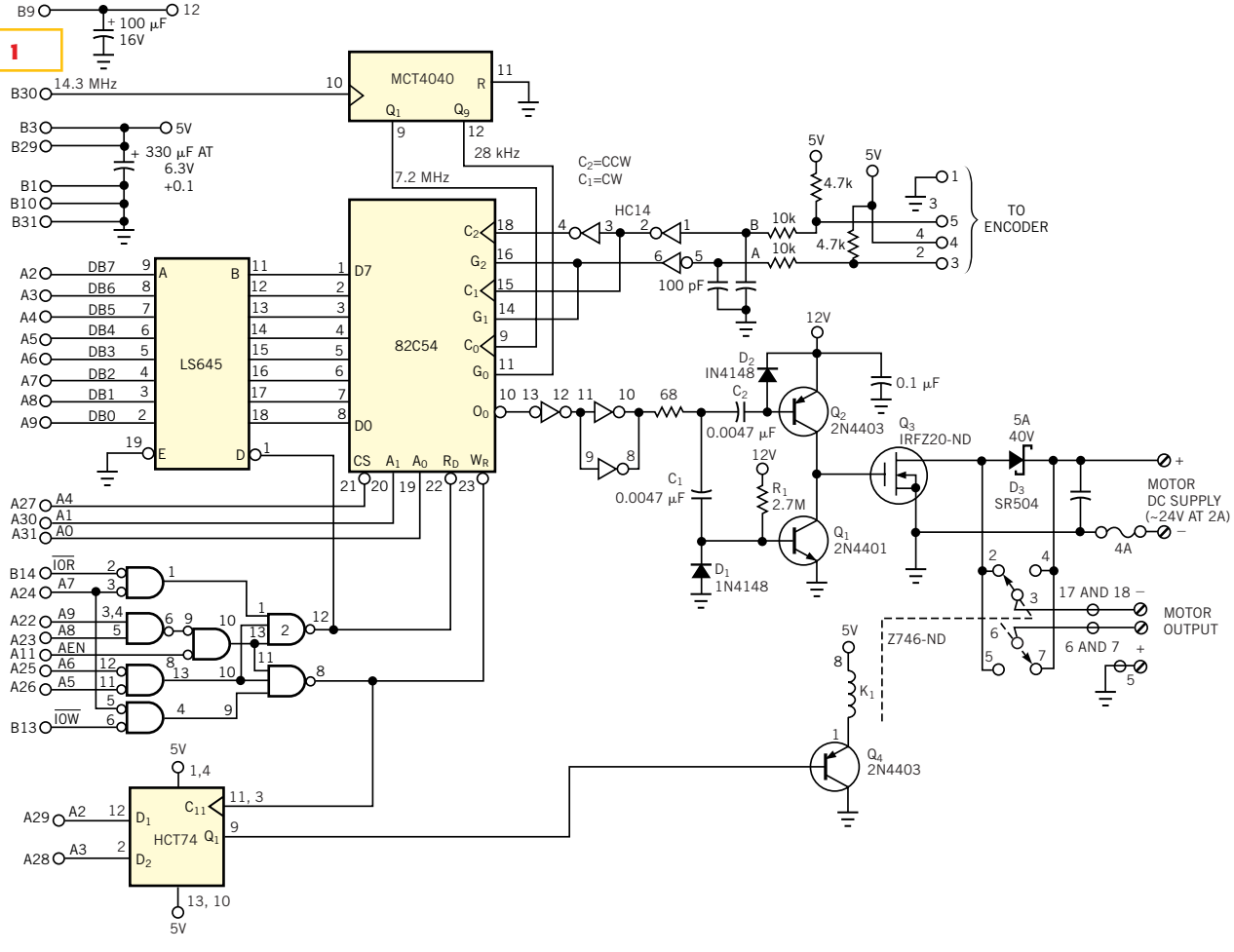
Encoder and PC make complete motor-control system

Steve Woodward, University of North Carolina, Chapel Hill, NC

THIS DESIGN IDEA COMBINES a simple ISA-bus-resident interface circuit; a garden-variety PC; a high-resolution optical shaft encoder; and a PWM-controlled, 0.05-hp, brushed, permanent-magnet dc motor to make a high-precision and high-power motion-control system. The system sequences the precise rotation of an evacuated steel bell jar several feet in diameter, such as those used in molecular-beam spectroscopy (**Figure 1**). Although the speed of the intermittent rotation of the jar isn't fast, the system needs large torques to overcome the friction of a large O-ring seal that is subjected to tens of tons of atmospheric pressure. Moving against this drag requires a heavy-duty drive that energizes a 48W (24V, 2A) motor. A different choice of MOSFET in **Figure 1** would allow the system to handle even heavier loads.

The quadrature-output, incremental optical shaft encoder that this Design Idea uses is popular in high-performance, bidirectional, rotation-sensing applications. Incremental encoders provide an inexpensive and reliable means for digital readout of bidirectional mechanical motion. They're usable to 10,000 rpm and higher. However, the interface logic they need can sometimes be problematic. Such logic typically includes at least one 16-bit or longer bidirectional counter. Several handy peripheral chips, such as the 8253, 8254, and 9511, are available that implement *unidirectional* counting, but *bidirectional* counter chips are comparatively scarce. ASICs can provide the

Figure 1



This block of bidirectional logic and a PC comprise a complete motion-control system.

needed functions, and hard-wired or programmable logic is a viable, though component-count-intensive, option.

Unfortunately, none of these options is ideal from either a cost or a pc-board-area standpoint. This alternative combines the industry-standard 82C54 unidirectional counter-timer peripheral chip with simple software to create a convenient interface between quadrature encoders and the ISA PC I/O bus. Thus, you can easily digitize bidirectional motion. The trick is to use two of the three unidirectional counters in the 82C54—one for each encoder-rotation direction. **Reference 1** describes the logic involved in detail. This Design Idea expands upon the material in **Reference 1** by closing the motion-control loop with an 8-bit-resolution, digital PWM motor-speed-control circuit. The PWM modulator consists of counter-timer 0 (CT0) of the 82C54, operating in retriggerable-one-shot mode and controlling the Q_1-Q_2 drivers for the MOSFET, Q_3.

The HC4040 provides a 7.2-MHz clock to CT0 and triggers CT0 at 28 kHz (7.2 MHz/256). The result is a variable-duty-factor PWM waveform at CT0's output (O_0). Q_1 and Q_2 buffer and boost the waveform to 12V p-p and apply the boosted waveform to the gate of MOSFET Q_3. The MOSFET then modulates the 24V-dc motor-supply rail and thus generates a more-than-95%-efficient, programmable motor-speed control. The motor's armature inductance combines with flyback diode D_3 to filter the high-frequency components of the 28-kHz PWM waveform and to extract the dc component. Minimizing the time the MOSFET spends between full-off and -on states is critical to the efficiency of this PWM circuit, as in all power-handling topologies.

The Q_1-Q_2 driver circuit achieves fast MOSFET on/off transition times of approximately 10 nsec, as well as minimal 12V supply-power consumption. The driver circuit achieves these two goals by avoiding saturation-induced cross-conduction of Q_1 and Q_2. The circuit avoids the cross-conduction by taking advantage of the fact that Q_3's gate presents an almost entirely capacitive load to the Q_1-Q_2 pair. Therefore, although currents of approximately 100 mA into Q_3's gate are necessary during on/off transitions to ensure efficiency-promoting speed, the drive requirement drops to zero between transitions. The circuit takes advantage of the situation by using capacitive drive to Q_1 and Q_2. Coupling capacitors C_1 and C_2 deliver robust base drive during rise and fall edges but virtually no drive after the transitions. Hence, the circuit avoids cross-conduction of the bipolar transistors. Meanwhile, R_1 provides just a trickle of dc bias to Q_1, so that Q_3 and, therefore, the motor stays off before the programming of the 82C54, regardless of whatever arbitrary state the IC may assume after power-up. Q_4 is a pnp transistor that controls the direction-reversing relay, K_1. **Listing 1** is an MBasic demo program for the motion-control system. You can download the software from the Web version of this Design Idea at www.ednmag.com.

LISTING 1—MBASIC DEMO PROGRAM FOR MOTION CONTROL

```
DEFINT I
IOADD = &H300: ' BASE ADDRESS FOR MOCONT CARD
IC0 = IOADD: IC1 = IC0 + 1: IC2 = IC0 + 2: ICS = IC0 + 3: ' 8254 COUNTER
ADDRESSES
IREV = 4: ' MOTOR-REVERSE BIT

OUT ICS, &H12: ' PROGRAM PULSE-WIDTH GENERATOR IN C0
OUT ICS, &H70: OUT ICS, &HB0: ' SETUP CW/CCW COUNTERS IN C1 AND C2

OUT IC0, 5: 'START PULSE-WIDTH GENERATOR
OUT ICS, &HDC: 'LATCH CW/CCW
I1L = INP(IC1): ICW = INP(IC1)
I2L = INP(IC2): ICCW = INP(IC2)
OUT IC1, I1L: OUT IC1, ICW: '...INITIALIZE CW/CCW COUNTERS
OUT IC2, I2L: OUT IC2, ICCW
OFFSET = I1L - I2L + 256! * (ICW - ICCW)

CLS : PRINT TAB(20); "MOTION-CONTROL-ADAPTER DEMO"
PRINT TAB(18); "W. S. Woodward...March 16, 1990"
PRINT "POSITION=": PRINT : PRINT : PRINT
PRINT "HIT '1' TO SLOW BY 4 STEPS OUT OF 256"
PRINT "     '2' TO SLOW BY 3"
PRINT "     '3' TO SLOW BY 2"
PRINT "     '4' TO SLOW BY 1"
PRINT "     '5' TO SPEED UP BY 1 STEP"
PRINT "     '6' TO SPEED BY 2"
PRINT "     '7' TO SPEED BY 3"
PRINT "     '8' TO SPEED BY 4"
PRINT
PRINT "     'R' TO STOP AND REVERSE"
PRINT
PRINT "     'T' TO INVERT SPEED SETTING"


AROUND:

OUT ICS, &HDC: 'LATCH CW/CCW
I1L = INP(IC1): I1M = INP(IC1): IF I1M > ICW THEN OFFSET = OFFSET + 65536
ICW = I1M
I2L = INP(IC2): I2M = INP(IC2): IF I2M > ICCW THEN OFFSET = OFFSET - 65536
ICCW = I2M
LOCATE 3, 10: PRINT I1L - I2L + 256! * (I1M - I2M) - OFFSET

IKEY = INSTR(" 1234-5678RT", UCASE$(INKEY$)) - 6: IF IKEY <= -5 THEN GOTO AROUND
IF IKEY = 5 THEN IKEY = -ISPEED + 1: IC1 = IC1 XOR IREV: IC2 = IC2 XOR IREV: IC0
= IC0 XOR IREV: ICS = ICS XOR IREV
IF IKEY = 6 THEN IKEY = (ISPEED XOR 255) - ISPEED
ISPEED = ISPEED + IKEY: IF ISPEED > 0 AND ISPEED < 256 THEN OUT IC0, ISPEED ELSE
ISPEED = ISPEED - IKEY
GOTO AROUND
```


Reference

1. Woodward, Steve, "Unidirectional counters accumulate bidirectional pulses," *EDN*, April 11, 2002, pg 72.

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Use PSpice for behavioral modeling of VCOs

Dobromir Dobrev, Jet Electronics, Sofia, Bulgaria

PSpice, a member of the Spice family for PC users, is becoming a standard tool for analog and mixed analog-digital simulation. Many analog designers are familiar with the software of Design Center, Design Lab, and OrCad (www.orcad.com) PSpice and use the software in their everyday lives. This Design Idea should be helpful to those who design and simulate PLL systems at a behavioral level. A basic PLL system comprises a phase detector, a loop filter, and a VCO (voltage-controlled oscillator), connected in a negative-feedback loop. The phase detector produces a voltage that, after low-pass-filtering by the loop filter, becomes an error voltage, V_E, applied to the control input of the VCO to set the angular frequency, (ω). When $V_E=0$, the VCO oscillates at some initial frequency, ω_0, called the frequency offset or free-running frequency. The output frequency of the VCO is:

$$\omega(t)=\omega_0+G_{VCO}V_E(t). \quad (1)$$

Here,

$$G_{VCO}=\frac{d\omega}{dV_E}=2\pi\frac{df}{dV_E}=2\pi g_{VCO}, \quad (2)$$

where G_{VCO} is the VCO's voltage-to-radian frequency gain in radians per second per volt and g_{VCO} is the VCO's voltage-to-frequency gain in hertz per volt. Consider a sinusoidal voltage with amplitude V_{AMPL}, argument $\theta(t)$, and dc offset V_{OFF}:

$$V(t)=V_{AMPL}\sin(\theta(t))+V_{OFF}. \quad (3)$$

The argument $\theta(t)$ is the time integral of the angular frequency:

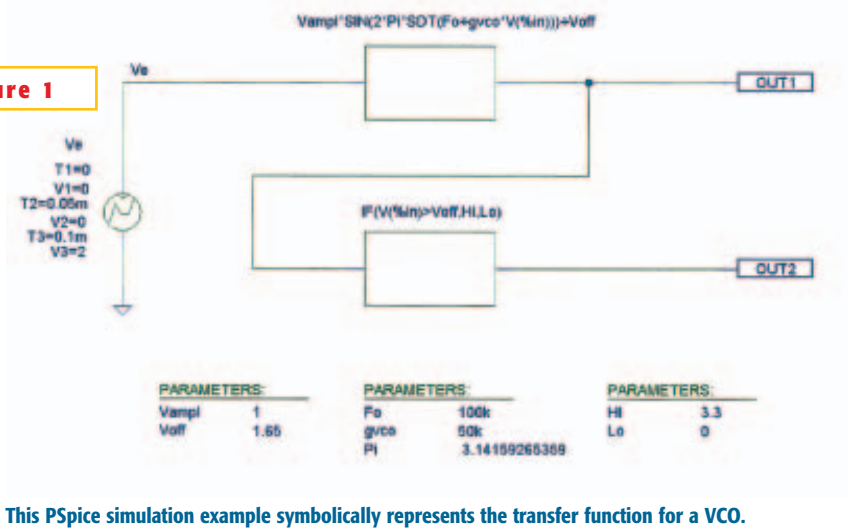
$$\theta(t)=\int\omega(t)dt+\theta(0). \quad (4)$$

Assuming ω is constant and substituting $\theta(t)$ in $V(t)$ yields the popular form:

$$V(t)=V_{AMPL}\sin(\omega t+\theta(0))+V_{OFF}. \quad (5)$$

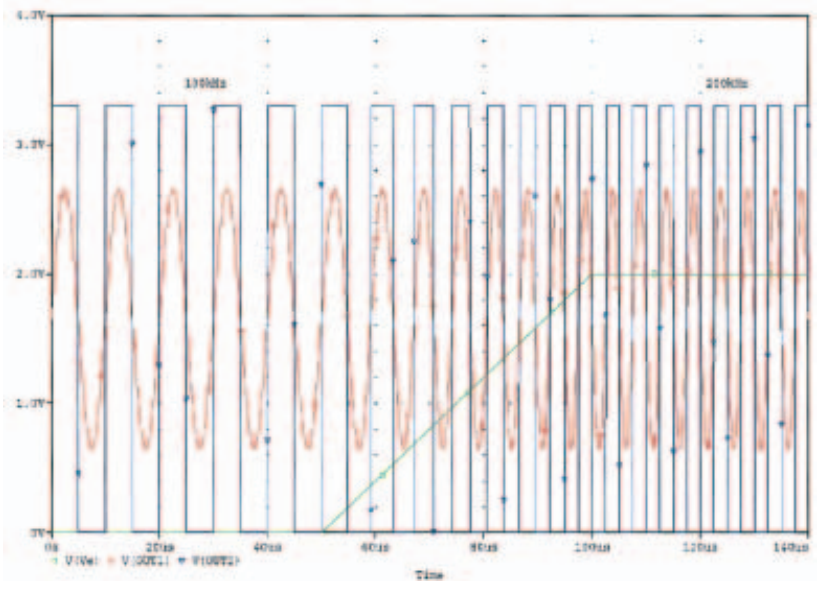
If ω is not constant, the general form is:

Figure 1



This PSpice simulation example symbolically represents the transfer function for a VCO.

Figure 2



A simulation example shows the results for the behavioral model of a VCO.

$$V(t)=V_{AMPL}\sin\left(\int(\omega(t)dt+\theta(0))\right)+V_{OFF}. \quad (6)$$

Replacing $\omega(t)$ with **Equation 1** and considering $\theta(0)=0$, you obtain the VCO's transfer function:

$$V_{VCO}(t)=V_{AMPL}\sin\left(\int(\omega_0+G_{VCO}V_E(t))dt\right)+V_{OFF}=V_{AMPL}\sin\left(\omega_0t+G_{VCO}\int V_E(t)dt\right)+V_{OFF}. \quad (7)$$

Equation 7 is the heart of the VCO's time-analysis modeling. Thus, you can easily perform VCO behavioral modeling, using the ABM1 part from the Analog Behavioral Modeling Symbol Library abm.slb (abm.olb in OrCad Capture). You can simply write the formula for the transfer function, adapted for PSpice. **Figure 1** shows the PSpice representation of the process. **Figure 2** shows a simulation example, in which V_E is the VCO's input voltage, and $V_{(OUT1)}$ is the output voltage. Because most phase detectors (types I, II, and III) use a digital input signal, you can easily obtain a digital VCO-output waveform using the conditional expression above the lower box in **Figure 1**. The simulated curve is $V_{(OUT2)}$, also shown in **Figure 2**. Finally, for loop-gain evaluation in ac analysis, you simply model the VCO in the frequency domain in an ideal integrating unit, using the Laplace form $T_{VCO}(s)=G_{VCO}/s$. Most obvious behavioral VCO models are based on a real circuit concept. Thus, they comprise many elements—for example, controllable sources, capacitors, and others. Hence, the models are complicated. This modeling is simple without involving superfluous computation resources.

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Circuit delivers high voltage swing from lower supplies

Bruce Carter and Ron Shakery, Texas Instruments, Dallas, TX

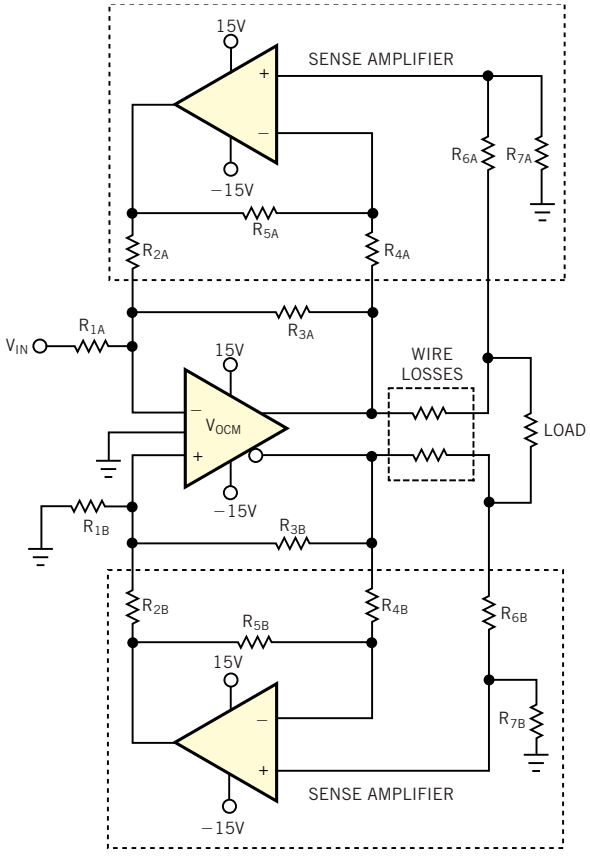
The need for higher voltage swings in applications such as test-and-measurement instruments is constantly increasing, but the power supplies impose limitations on the operational amplifier rails make the high-voltage need a challenge for designers. How do you deliver high-voltage swings to a load without increasing the voltage levels of the power supplies of the operational amplifier? In other words, for example, how can you produce a ±16V or greater signal swing across the load using only ±15V power supplies? The circuit in **Figure 1** uses a fully differential amplifier to offer an answer to this problem. Fully differential amplifiers enable you to deliver an output-voltage swing beyond the rails into the load. One of the common problems in working with operational amplifiers is the limit that the power-supply rails impose. The standard since the days of analog computers has been ±15V. Analog computers are gone, but their legacy remains in the power-supply voltages. These voltages find widespread use in transducer interfaces and applications in which voltage swing and dynamic range are of primary importance.

This ±15V supply voltage notwithstanding, applications exist that require a higher swing range beyond the power-supply limits. Typical ±15V operational amplifiers are seldom optimized for rail-to-rail operation, and their useful output-voltage range may be only 24 to 26V. Many audio consoles use older technology 741 op amps with ±18, ±20, and even ±22V power supplies to obtain more voltage swing and, therefore, more dynamic range from their systems in light of this limitation. The op amps in these systems often run hot and have heat sinks. The advent of fully differential op amps has given designers a better way to extend the output-swing range. Fully differential operational amplifiers 40 to 50 years ago were tube or discrete-transistor units. They have recently re-emerged as a way to interface to fully differential A/D converters and applications in which the load needs differential drive for better swing range or to reduce the noise effects in the systems.

The outputs of fully differential op amps have a characteristic that makes them useful for doubling the swing. The two outputs are 180° out of phase: When one output swings positive, the other swings negative and vice versa. The net effect is similar to what happens in a bridged amplifier: The effective output-voltage range doubles. The price of doubling this output-voltage swing is that you can no longer connect the output load to ground. Designers of automotive audio amplifiers are familiar with this concept: Audio-power bridged amplifiers have a fully differential output. Many installers have learned the hard way that the minus speaker connection cannot connect to ground. When the output voltage doubles, power quadruples. This feature is useful for audio power amplifiers in a limited-power-supply-voltage application.

To illustrate the advantage of fully differential outputs, assume that a fully differential op amp has a voltage-rail limitation of ±13V when operated from ±15V supplies. The absolute- maximum output range of each output is ±13V. But when the top output is at 13V, the bottom output is −13V: (13V)−(−13V)=26V. When the top output is −13V, the bottom output is 13V. As a result, the output voltage is (−13V)−(13V)=−26V. Therefore, the output-voltage range is

Figure 1



Similar to a bridged audio amplifier, this op-amp circuit delivers output-voltage swings to the load beyond the span of the power supplies.

±26V, which enables the output to swing from −26V to +26V, resulting in a doubled voltage-swing range. Fully differential op-amp designs require that the two feedback loops be symmetrical; the components in the top and the bottom sections must be the same. In **Figure 1**'s schematic, the components in the top feedback path are labeled "A," and those in the bottom are labeled "B." When this design references a designator, the comment applies to both paths A and B.

The gain of the overall circuit is $V_{OUT}/V_{IN}=R_3/R_1$. The location of the load is often at the end of a balanced line. You cannot discount the effect of the wire; it affects the amplitude across the load, reducing the expected gain of the system. The sense lines help compensate for the voltage drop across the lines, resulting in the delivery of the targeted voltage to the load. The two sense amplifiers in the schematic are each composed of an op amp and resistors R_4 through R_7. R_2 acts as a summing component, adding small-signal amplitude equal to the voltage drop of the wire back into the input, boosting the op amp's output such that the expected gain appears at the load. If you make R_4 though R_7 equal in value to R_1, then it is easy to calculate R_2: It takes the same value as R_3. If R_4 through R_7 cannot be equal to R_1, then R_3 should be proportional to R_2. You should be aware that the resistors in the sense amplifiers change the load characteristics. For 600Ω audio-distribution systems, this fact is less of a problem than it is in 50Ω systems. You should be aware, however, of the output-drive characteristics of your operational amplifiers, if you wish to deliver the exact desired voltage swing to the load.

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