Edited by Bill Travis

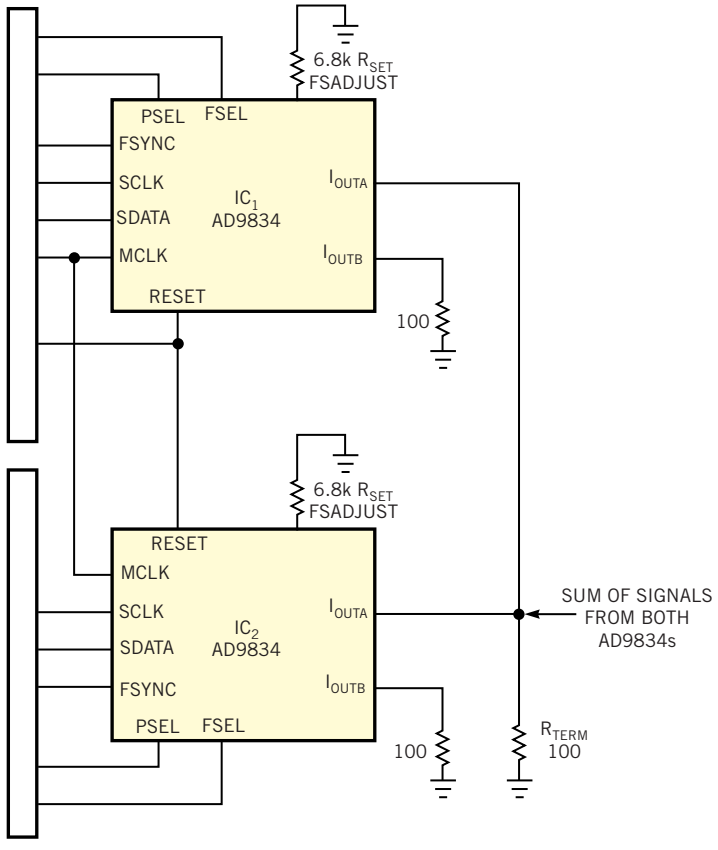
Two DDS ICs implement amplitude-shift keying

Noel McNamara, Analog Devices, Limerick, Ireland

Many communications systems, including RFID systems and cable modems, use AM (amplitude modulation). This Design Idea shows how two DDS (direct-digital-synthesis) devices can implement AM and ASK (amplitude-shift keying) over a range of frequencies. The AD9834 complete 50-MHz DDS IC (**Figure 1**) has a current output, so you can easily sum the outputs of two or more of them by connecting them to a common termination resistor. Each AD9834 has two internal phase registers, P_0 and P_1, and two internal frequency registers, F_0 and F_1 (not shown). With each AD9834 generating a sine wave at the same frequency, the amplitude of the summed signal depends on the phase of each signal. You can achieve four preset amplitude levels—or any on-the-fly level—by summing the outputs of two AD9834s.

Table 1 shows two AD9834s, IC_1 and IC_2, configured to give four output levels. P_{0A} is phase register 0 for IC_1, P_{1A} is phase register 1 for IC_1, and so on. You can select the desired output level with either the PSEL pins or with the PSEL bits in the control register. **Figure 2** shows the waveforms at the R_{TERM} summing junction for the phases used in **Table 1**. You can achieve any signal level from 0V to a full-scale voltage of approximately 600 mV by programming the phase registers with the appropriate values. Both devices use the same MCLK (master clock), and you need to synchronize them to get the correct signal levels at the R_{TERM} output. You achieve synchronization by simultaneously applying a Reset signal to both parts after programming both parts with the correct phase and frequency. You can accomplish the synchronization by applying a positive pulse to the Reset pins, or you can implement a software synchronization by setting the reset bit in the control register to one, stopping MCLK, setting the reset bit in the control register to zero, and then starting MCLK. Either method ensures that both parts simultaneously exit the reset state.

Figure 1



You can use two DDS chips to implement amplitude modulation and amplitude-shift keying.

You can easily implement 100% AM with a single AD9834 by toggling the Reset pin or the reset bit in the control register. When the part is in reset, the DAC's output is at midscale. The predetermined sine wave is available at I_{OUT} when the DDS exits reset. To calculate the magnitude of the sum of the two signals from the AD9834s, represent each signal as a rotating vector (**Figure 3**). You can easily calculate the magnitude and phase of the resulting summed vector as follows: If the length of each vector is 1, then:

Publish your Design Idea in *EDN*. See the What's Up section at www.edn.com.

TABLE 1—THE PHASE-REGISTER CONTENTS YIELD FOUR OUTPUT LEVELS FROM THE CIRCUIT IN FIGURE 1

	Device number	Phase-register values (°)		Normalized level of summed signal	Output level with R_{TERM} = 100Ω and R_{SET}=6.8 kΩ (mV)
P_0	A	45	$P_{0A}+P_{0B}(45+180)°$	0.765	223
P_1	A	95	$P_{0A}+P_{1B}(45+210)°$	0.426	128
P_0	B	180	$P_{1A}+P_{0B}(95+180)°$	1.47	435
P_1	B	210	$P_{1A}+P_{1B}(95+210)°$	1.191	350

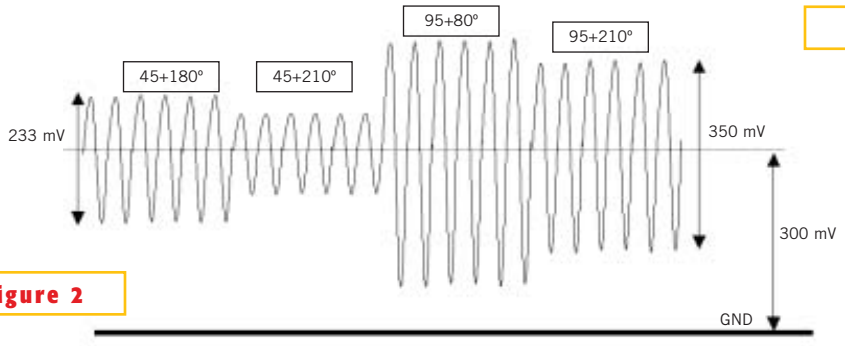
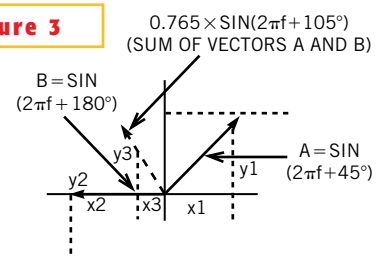


Figure 2

The waveforms at the R_{TERM} summing junction use the phases in Table 1.

Figure 3



You can calculate the magnitude of the summed signals from the DDS chips by representing each signal as a rotating vector.

- x1 = Cos(45°)=0.707: y1=Sin(45°)=0.707;
- x2=Cos(180°)=−1.00: y2=Sin(180°)=0;
- x3=x1+x2=−0.293: y3=y1+y2=0.707;
- Magnitude of resulting vector: $\sqrt{(x3)^2+(y3)^2}$=0.765;
- Phase of summed vector: 112.5° (180°−Tan^{-1}(y3/x3)).

The maximum output-voltage level that any one AD9834 can develop across the 100Ω termination resistor with R_{SET}=6.8 kΩ is 320 mV p-p. Therefore, the voltage level this example achieves is 320 mV×0.765=244.8 mV. This example shows that the phase of the resulting summed vector depends on the phase of two input vectors and may result in a phase discontinuity as the phases of the input vector change. To avoid phase discontinuity at the transition, you can set the resultant phase, P3, to a fixed angle, say 180°≥p2=360°−p1.

Sin(2πf+p1)+Sin(2πf+p2)=2Cos(0.5(p1−p2))×Sin(2πf+(p1+p2)/2).

Desired amplitude: A=2Cos[0.5(p1−p2)]; p1−p2 = 2Cos^{-1}(A/2).

Resultant phase: P3=(p2+p2)/2.

Therefore, p1=180°+Cos^{-1}(A/2), and p2=180°−Cos^{-1}(A/2) gives amplitude A with no phase shift at the transition.□

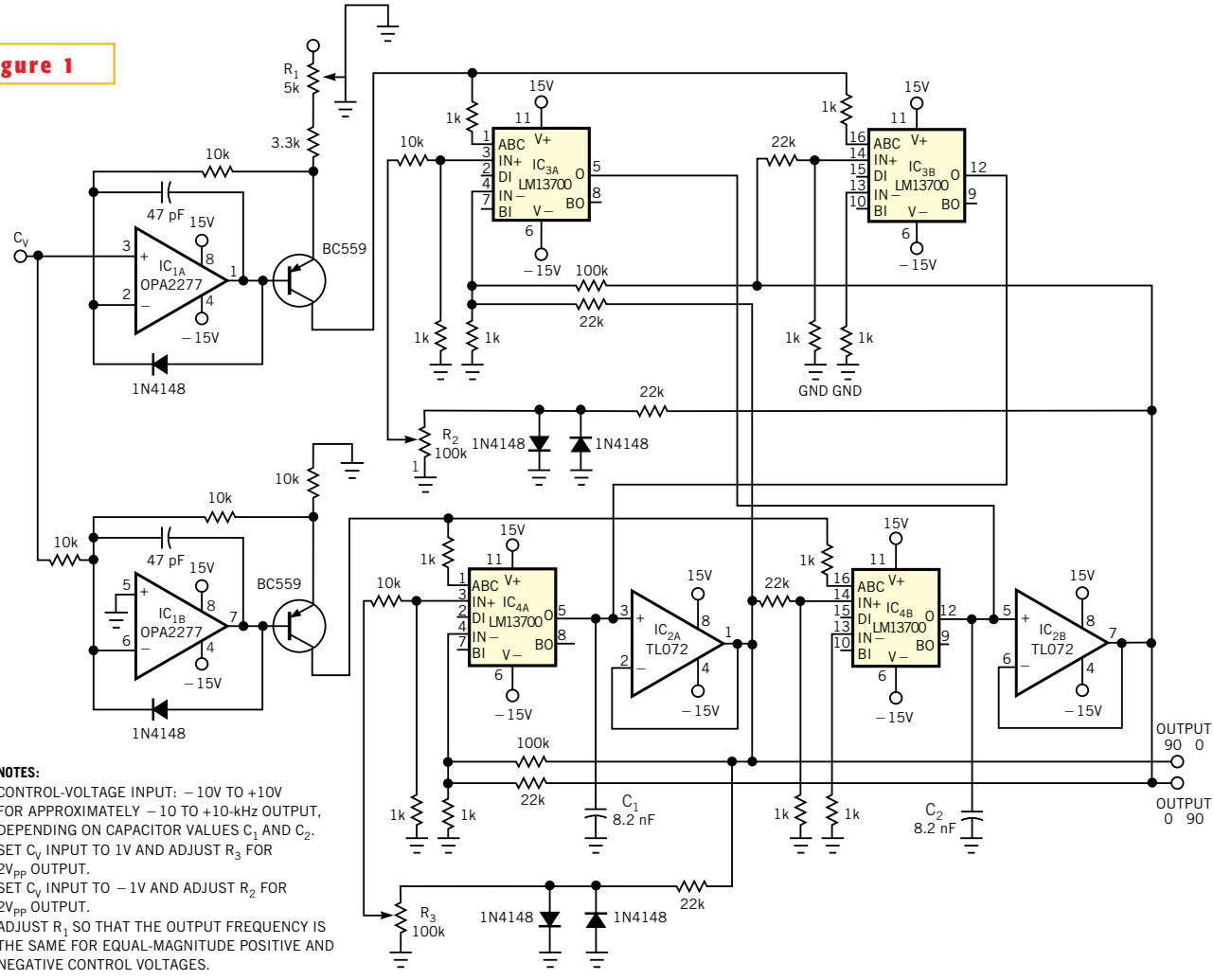
VCO produces positive and negative output frequencies

Henry Walmsley, Farnborough, UK

THE CIRCUIT IN **Figure 1** is a quadrature-output VCO that provides both positive and negative output frequencies, depending on the polarity of the control-voltage input. The circuit provides a function that designers traditionally implement in analog music-effects units, such as Bode/Moog frequency shifters. Bode/Moog shifters use fixed-beat-frequency oscillators at 20 kHz and variable sine oscillators that go higher and lower than 20 kHz. Both oscillators feed into mixers. The circuit in this design reduces the number of oscillators to one and uses no mixers (**Figure 1**). As a result, the output has fewer spurious harmonics and unharmonically related frequency products, resulting in a cleaner output overall.

The two lower transconductance amplifiers, IC_{4A} and IC_{4B}, form a standard, double-integrator bandpass/lowpass filter. The lower amplifiers are active for positive control voltages, and the upper amplifiers, IC_{3A} and IC_{3B}, are effectively turned off for lack of bias current. The upper amplifiers thus play no part in the circuit when the control voltage is positive. The TL072 op amps, IC_{2A} and IC_{2B}, are merely buffers to enable an easier choice of resistor values for IC_{4B}'s input and to avoid excessive loading of the integrator capacitors. The resistor values set the Q (quality factor) to exceed unity. Positive feedback from the bandpass output to the noninverting input makes the filter oscillate. Adjusting the R_3 trimmer allows you to adjust the output amplitude and lets you set the drive to the diodes at a level that ensures oscillation but minimizes distortion. This fairly standard configuration yields quadrature outputs

Figure 1



NOTES:
CONTROL-VOLTAGE INPUT: −10V TO +10V
FOR APPROXIMATELY −10 TO +10-kHz OUTPUT, DEPENDING ON CAPACITOR VALUES C_1 AND C_2.
SET C_V INPUT TO 1V AND ADJUST R_3 FOR $2V_{PP}$ OUTPUT.
SET C_V INPUT TO −1V AND ADJUST R_2 FOR $2V_{PP}$ OUTPUT.
ADJUST R_1 SO THAT THE OUTPUT FREQUENCY IS THE SAME FOR EQUAL-MAGNITUDE POSITIVE AND NEGATIVE CONTROL VOLTAGES.

This quadrature-output VCO produces both positive and negative output frequencies.

from the two buffers with the highest distortion product approximately 40 dB down from the fundamental.

For negative control voltages, the upper transconductance amplifiers, IC_{3A} and IC_{3B}, receive bias current, and the lower amplifiers shut off. The upper amplifiers work in exactly the same way as the lower ones, but they cross-connect to the inputs and integrator capacitors. In this way, the in-phase and quadrature outputs are reversed for negative control voltages, thus creating a smooth transition to what you can consider a "negative frequency." In operation, when viewing the outputs on an X-Y trace, the circular rotation of the dot becomes slower as you adjust the control voltage near zero and then perfectly reverses direction as the control voltage goes negative. This transition occurs without any unwanted crossing of the circle or drifting off beyond the circle.

The two current sources, IC_{1A} and IC_{1B}, are fairly self-explanatory; the upper source operates for negative control voltages and vice versa. The R_1 gain trimmer on the upper source allows you to adjust the oscillator such that a given negative control voltage yields the same frequency as does the equal-magnitude positive control voltage. This trim compensates for differences in transconductance of the two separate dual-amplifier packages. The diodes across the current-source op amps avoid heavy saturation when the respective source turns off. You trim the R_2 potentiometer to obtain equal amplitudes from the upper and the lower sections. The circuit in **Figure 1** uses standard, inexpensive, multiple-sourced components. It requires only minimal (and easy) trimming, with no interacting trims. A 0V control input results in a guaranteed 0-Hz output, dependent only on well-controlled op-amp offsets. With the Bode/Moog system, you must make a front-panel adjustment to zero-beat two oscillators running at 20 kHz.□

16-bit adjustable reference uses 8-bit digital potentiometers

Bonnie Baker, Tucson, AZ

IT MAY BE EASY to find a precision voltage reference for your application; however, a programmable precision reference is another matter. The circuit in **Figure 1** yields a precision reference with an LSB of 62.5 µV. The circuit is a 16-bit DAC using three 8-bit digital potentiometers and three CMOS op amps. Each digital potentiometer operates as an 8-bit multiplying DAC. On the left side of **Figure 1**, two digital potentiometers, IC_{3A} and IC_{3B}, span across V_{REF} to ground, and the wiper outputs are connected to the noninverting inputs of two amplifiers, IC_{4A} and IC_{4B}. In this configuration, the inputs to the amplifiers have high impedance levels, thus isolating the digital potentiometers from the rest of the circuit. The microcontroller, IC_1, programs digital potentiometers IC_{3A} and IC_{3B} through its SPI port. If V_{REF} is equal to 4.096V, the LSB at the outputs of IC_{4A} and IC_{4B} is 16 mV.

To make this circuit perform as a 16-bit DAC, a third digital potentiometer, IC_{2A}, spans across the outputs of the two amplifiers, IC_{4A} and IC_{4B}. The programmed setting of IC_{3A} and IC_{3B} sets the voltage across this third digital potentiometer. If V_{REF} is 4.096V, you can program IC_{3A} and IC_{3B} such that the output difference of op amps IC_{4A} and IC_{4B} is 16 mV. You can achieve high accuracy with this circuit by using a dual digital potentiometer for IC_{3A} and IC_{3B}. With the dual structure, the resistances of these two devices match typically within 0.2%. Given the size of the voltage across the third digital potentiometer, the LSB of the complete circuit from left to right is 62.5 µV ($V_{REF}/2^{16}$). **Table 1** shows the critical device specifications to obtain optimum performance with this circuit.□

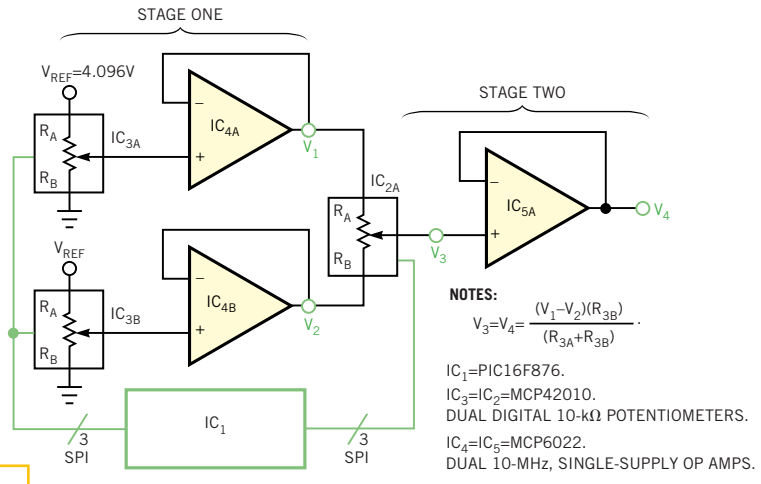


Figure 1

You can design a precision 16-bit DAC by using three digital potentiometers and three op amps.

TABLE 1–DEVICE SPECIFICATIONS FOR OPTIMUM PERFORMANCE

Device	Specification		Purpose
Digital potentiometers (IC_2, IC_3) (MCP42010)	Number of bits	8 bits	Determines the overall LSB and resolution of the circuit.
	Nominal resistance (potentiometer element)	10 kΩ (typical)	Achieve better noise performance by using lower resistance potentiometers. The trade-off for low-noise potentiometers is higher current consumption.
	Differential nonlinearity	±1 LSB (maximum)	Good differential linearity ensures that the circuit exhibits no missing codes.
	Voltage-noise density (for half the resistive element)	9 nV/√Hz at 1 kHz (typical)	If the noise contribution of these devices is too high, it reduces the possibility of achieving 16-bit, noise-free performance. Selecting lower resistance elements can reduce the potentiometer noise.
Operational amplifiers (IC_4, IC_5) (MCP6022)	Input bias current (IB)	1 pA at 25°C (maximum)	Higher input bias current causes a dc error across the potentiometer. CMOS amplifiers are, therefore, good choices.
	Input offset voltage	500 µV (maximum)	A difference in amplifier offset error between IC_{4A} and IC_{4B} could compromise the differential linearity to the overall system; 50 µV is considerably lower than 1 LSB in Stage 1 of the circuit.
	Voltage-noise density	8.7 nV/√Hz at 10 kHz (typical)	If the noise contribution of these devices is too high, it reduces the possibility of achieving 16-bit, noise-free performance. Selecting lower noise amplifiers can reduce overall system noise.