design ideas

Edited by Bill Travis

Motor-control scheme yields four positions with two outputs

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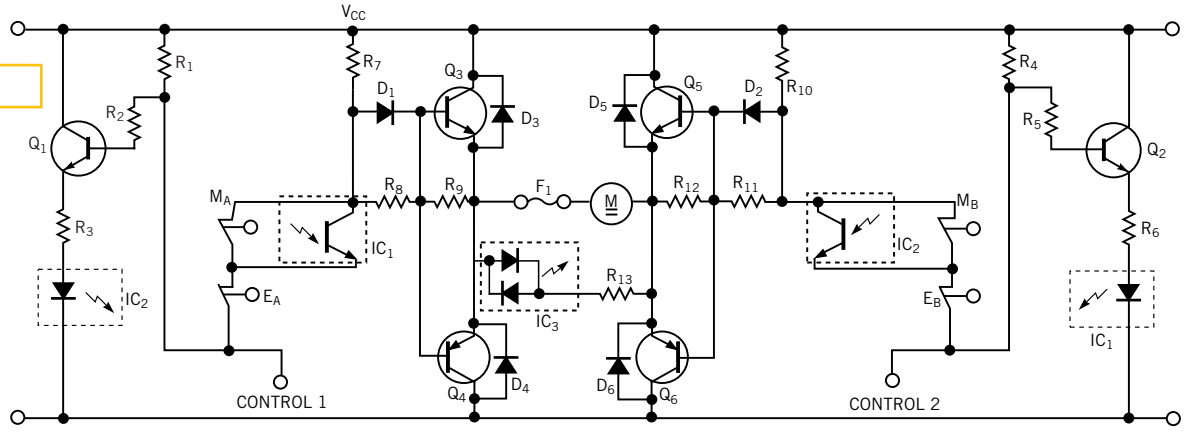
FIGURE 1 shows how to position a mechanical device into four discrete positions but with only two free outputs and one free input from the control system. The position depends on a set of cams and four corresponding limit switches. The 24V-dc motor comes with a worm gear. Darlington transistors Q_3 to Q_6 and resistors R_7 to R_{12} form an H-bridge that drives the dc motor, M. Diodes D_3 to D_6 protect these transistors from inductive spikes. The outputs of the controller (not shown), connected to the Control 1 and Control 2 inputs, have open-collector structures that connect Control 1, Control 2, or both to ground upon activation. If you activate neither Control 1 nor Control 2, Q_3 and Q_5 conduct, receiving base current through R_7 and D_1 and R_{10} and D_2, respectively. This action short-circuits (brakes) the motor. In this case, Q_4 and Q_6 are turned off. Optocouplers IC_1 and IC_2 are on, thereby short-circuiting the limit switches, M_A and M_B.

Activating only one control input (for example, Control 1), if the cam does not push open the corresponding limit switch, E_A, causes Q_3 to switch off and Q_4 to switch on with R_8 limiting the base current. Thus, the motor rotates until the cam pushes open limit switch E_A (Position 1 in **Figure 2**). The limit switch, M_A, has no influence because optocoupler IC_1 short-circuits M_A when Control 2 is in a high state. A similar, symmetrical operation occurs if you activate (ground) Control 2. In this case, the motor rotates to push open limit switch E_B (Position 4). To bring the motor to one of the middle positions—say, Position 2—you use the following procedure:

1. With Control 2 high (not connected), activate (ground) Control 1. The motor rotates until it pushes open limit switch E_A. The bases of Q_3

Figure 1



NOTES:

D_1, D_2: 1N4148
D_3 TO D_6: 1N4937
R_1, R_2, R_4, R_5, R_9, R_{12}: 10 kΩ, 0.25W
R_7, R_8, R_{10}, R_{11}: 3.3 kΩ , 0.25W
R_3, R_6, R_{13}: 1.5 kΩ, 0.6W

Q_1, Q_2: 2N2222, 2N3904...
Q_3, Q_5: BDX33C
Q_4, Q_6: BDX34C
IC_1 TO IC_3: PC814, H11AA1, SFH6206-2...

This simple circuit provides four-position motor control with two inputs.

through Q_6 are all high.

2. Activate (ground) Control 2. The bases of Q_5 and Q_6 switch low. (M_B and E_B are closed.) The motor rotates in reverse until M_A closes. At this time, all bases are low. Q_4 and Q_6 short-circuit the motor to ground, thereby braking it to a stop.

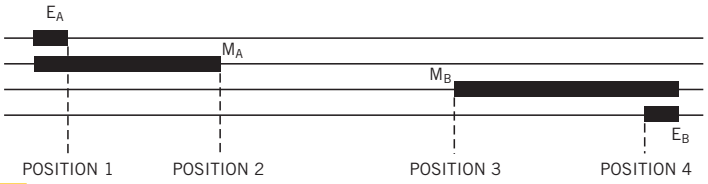


Figure 2

Cams operate the limit switches in Figure 1, producing four discrete positions.

First activating Control 2 and then Control 1 brings the motor to Position 3, the edge of cam M_B. Otocoupler IC_3 remains on as long as the motor receives voltage. The output of IC_3 connects to a feedback input of the controller. Thus, you can control whether the motor is rotating or stopped through this input. F_1, a polymer-based resettable fuse, protects the motor and the circuit against overcurrent conditions, such as a stalled motor. You can mount the circuit in **Figure 1** on small machine tools, such as a workpiece changer. The values of the components are not critical. The transistors are preferably Darlington types and, like the diodes, should have adequate ratings to accommodate the power-supply voltage and the motor current. (Don't forget the high inductance of the motor.) The components in **Figure 1** accommodate a 24V-dc, 2.5A motor.

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Single switch controls digital potentiometer

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The control of electronic potentiometers in most today's applications comes from controller-generated signals. However, a significant number of applications exist that require adjustments using manual, front-panel controls. The circuit in **Figure 1** uses one IC, one switch, and 10 discrete components. It implements the interface of a single DPDT, momentary-contact rocker switch to a DPP (digitally programmable potentiometer). The Catalyst DPP has a three-wire increment/decrement interface. The traditional way to implement the front-panel controls for potentiometers with this type of interface is to use two single-pole, single-throw switches. Switch S_1 reduces the front-panel hardware by half. The action of the switch is natural for the control of increment-up/increment-down potentiometers.

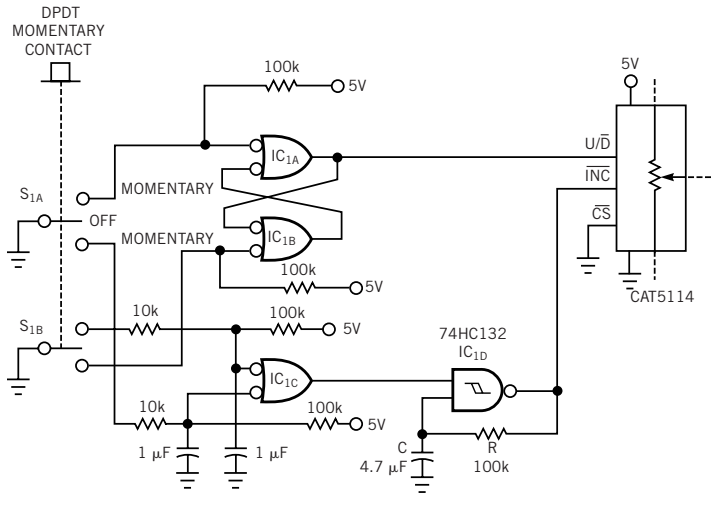

Figure 1

A single switch is all you need to control a digitally programmable potentiometer.

IC_{1A} and IC_{1B}, which implement an R-S flip-flop, control the potentiometer's wiper direction—up or down. The output of the flip-flop reflects the up/down position of S_1. The potentiometer's wiper advances on the falling edge of the signal driving the $\overline{INC}$ input of the DPP. The clock output of IC_{1D} drives $\overline{INC}$. The clock becomes enabled when you depress the rocker switch either up or down. The RC networks at the inputs of IC_{1C} debounce the switches. If you momentarily depress the rocker switch, the clock generates one pulse. If you continuously depress the rocker switch, the clock free-runs at a frequency of approximately $1/R_1C_1$.

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Versatile power-supply load uses light bulbs

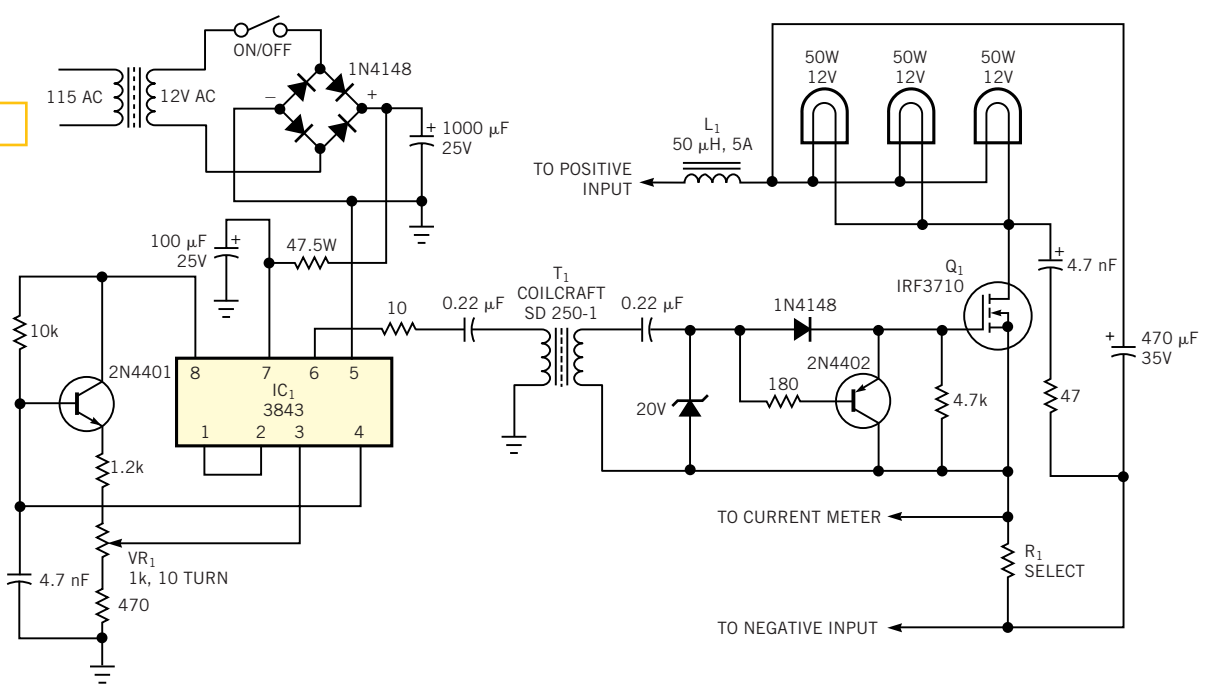
William Sloot, Computron Display Systems, Mount Prospect, IL

Improvising loads for bench-testing and designing power supplies is often a frustrating and sometimes hazardous experience. When you push large power resistors to their limit, they tend to burn benches and melt solder connections. Many electronic loads are on the market but are usually expensive and of laboratory-type precision and often represent overkill for the average designer. Incandescent light bulbs make excellent loads, able to handle large amounts of power. Moreover, they come in small packages and require no heat sinks. Furthermore, because they light up, you obtain instant feedback, rather like an analog versus a digital meter. The drawback is that the resistance of an incandescent lamp changes dramatically with the power input. The power into the load must therefore be controllable over a broad range, if the bulb is to be a useful current sink. A simple approach to this control problem is to pulse-width-modulate a power MOSFET in series with the load. This design uses a four-rail, 100W supply with outputs of 5, 12, and ±15V. For these voltage and power levels, 50W, 12V bulbs provide a suitable load. This application required three bulbs connected in parallel (**Figure 1**). Many automotive-supply dealers offer 50W, 12V bulbs.

Because these bulbs screw into an ordinary 115V light socket, you can create a virtually unlimited combination of loads. The use of old-fashioned porcelain-type sockets wired in parallel allows you connect any number of bulbs in the load circuit. The circuit in **Figure 1** addresses supplies of 1 to 24V output levels, of positive or negative polarity, with power levels as high as 150W. You can use the same basic approach to load higher voltage supplies by using 115V light bulbs and appropriately sizing the power MOSFET and other components. The circuit uses a standard PWM 3843 IC, IC_1, in open-loop mode. Potentiometer VR_1 controls the duty cycle over its full range. The frequency is not critical and is approximately 37 kHz with the values shown in **Figure 1**. A small, modular plug-in transformer provides power, but you can use any source of approximately 18V dc at 50 mA.

T_1 provides isolated drive to the power MOSFET, Q_1. The transformer allows you to load negative as well as positive sources. The various components in the gate circuit provide efficient drive to Q_1 over a broad range of duty cycles. The L_1 choke isolates the input from the switching pulses in Q_1. You could use either an analog or a digital current readout. This design uses an LED readout salvaged

Figure 1



Incandescent light bulbs provide convenient loads for testing power supplies.

from an old power supply. You must size the current resistor, R_1, for the power dissipation and the requirements of the current meter. In this application, three metal-oxide, 0.1Ω, 2W resistors connected in series met the requirements (maximum current of 4A). You must fasten Q_1 to a heat sink adequate for the application. The circuit in **Figure 1** uses an Aavid (www.aavid.com) 530101B00100. This heat sink is a U-shaped radiator measuring approximately 1.75×175 in. on each side. Applications requiring higher currents could use two MOSFETs in parallel. The gate-drive scheme shown has enough power to drive two MOSFETs.

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Two-transistor circuit replaces IC

Jim Hagerman, Hagerman Technology, Honolulu, HI

Linear Technology's recently introduced LTC4300 chip buffers I²C clock and data lines to and from a hot-swappable card. This task is difficult because the IC must work bidirectionally, meaning that you can simultaneously and actively drive both sides. However, as is sometimes the case, you can replace a complicated circuit by a simple one without much loss of performance. For example, transistors and resistors replace the entire IC (**Figure 1**). The circuit handles only the clock signal or only the data signal. Two npn transistors, connected head-to-head, form the heart of the circuit. I²C signals come from open-collector or open-drain outputs, so can only pull down (sink current). When Enable is high, a low-going SCL signal drives the emitter of one of the transistors as a common-base amplifier. The 10-kΩ resistor in the base circuit provides enough current to saturate the transistor and drop the V_{CE} voltage to approximately 0.1V, thereby pulling the other side low.

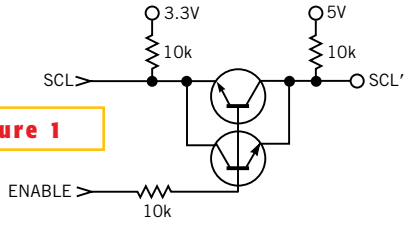

Figure 1

This circuit is an I²C-compatible, hot-swappable translator/buffer.

The circuit acts like an efficient diode. With Enable low, the hot-swappable side has no effect on the signal, with or without power applied. The two-transistor circuit offers the additional benefit of acting as a level translator between two logic levels. This example shows a buffer-translation between a 3.3V system and a 5V card. For proper operation, the Enable line must not go higher than the lower of the two supply voltages. **Figures 2a** and **b** show operation at 100 kHz. Some edge glitches and overshoot, stemming from transistor-junction capacitance, are evident in the 3.3V signal, but these slight defects should be tolerable in many low-cost applications. **References 1** and **2** treat similar level-translation circuits.

References

1. Hagerman, Jim, "Two transistors form bidirectional level translator," *EDN*, Nov 7, 1996, pg 114.

2. Poon, CC, and Edward Chui, "Low-voltage interface circuits translate 1.8V to 5V," *EDN*, Nov 5, 1998, pg 119.

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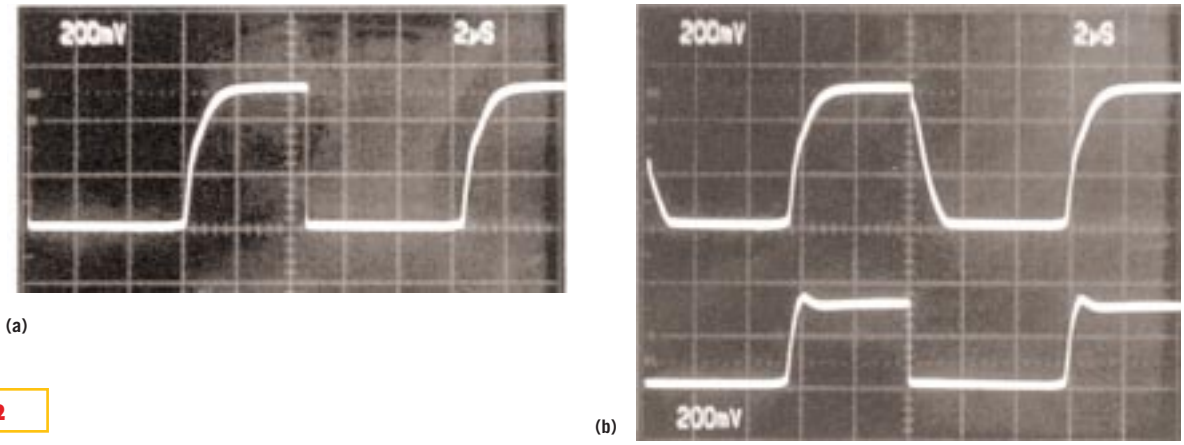


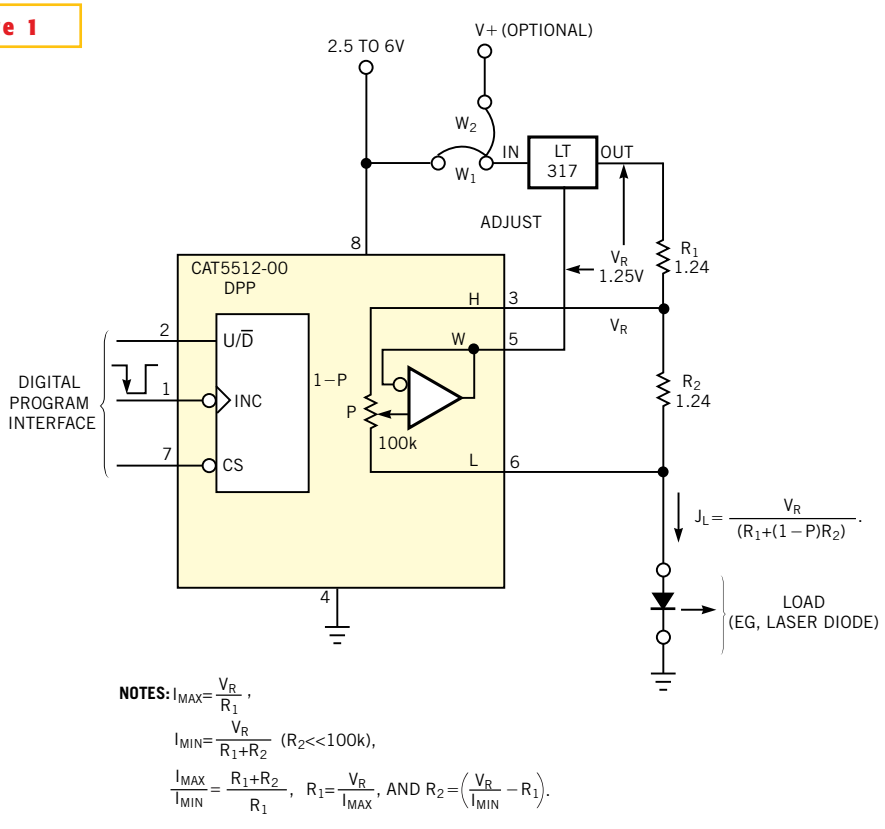
Figure 2

The 5V side (a) and the 3.3V side (b) drive operation with the circuit.

Digital current source is nonvolatile

Stephen Woodward, University of North Carolina, Chapel Hill

Figure 1



This digitally programmable current source is suitable for driving VCSELs in communications equipment.

Digitally programmable current sources that feature automatic trimming and retain the setting despite power-down cycles are useful in applications such as RF- and laser-communications drivers. The circuit in **Figure 1**, for example, is particularly suited for setting the drive current for the optical pump in widely tunable VCSELs (vertical-cavity surface-emitting lasers). These lasers are suitable in systems using wavelength-agile DWDM fiber-optic communication links. The circuit in **Figure 1** delivers a stable drive current that derives its control from DPP (digitally programmed potentiometer), a Catalyst Semiconductor (www.catsemi.com) CAT5512. For the circuit values shown, you can set the output current to 500 mA to 1A; however, you can alter this span over a wide range by the judicious selection of sense resistors R_1 and R_2.

The unique features of the CAT5512 make possible the low component count (two chips and two resistors). The device combines a 5-bit-resolution, 100-kΩ DPP, a nonvolatile EEPROM for long-term storage of the DPP setting, and a unity-gain analog-wiper-buffer amplifier. The DPP provides a complete digital interface of the LT317 precision regulator chip to the R_1, R_2 split current-sense-resistor network. The result is a robust, precision programmable current source with 5-bit resolution over a flexible I_{MIN} to I_{MAX} range. The basis of circuit operation is the fact that the LT317 regulator generates the current necessary to maintain a constant 1.25V across the effective sense resistance: $R_1+(1-p)R_2$, where p is the DPP setting: 0, 0.032, 0.064, 0.097, ..., 0.98, 1. In this way, $I_1=1.25V/(R_1+(1-p)R_2)$ over the range of $I_{MIN}=1.25V/(R_1+R_2)$ for p=0 to $I_{MAX}=1.25V/R_1$ for p=1. The pertinent design equations are $R_1=1.25V/I_{MAX}$, and $R_2=1.25V/I_{MIN}-R_1$.

Note that the R_2 equation is an approximation, based on the assumption that R_2 is much lower than 100 kΩ, the parallel DPP resistance. The full expression for R2 is:

$R_2=1/(1/((1.25V/I_{MIN})-R_1)-1/100\,k\Omega)$.

You exert control of the DPP setting "p"—and storage of the setting in nonvolatile EEPROM—via the three-wire digital interface, as described in the CAT5512 data sheet. The load-voltage-compliance limit is a function of the W_1 and W_2 V+ supply jumpers, connected to the LT317. The maximum output voltage is the difference between the LT317's input voltage and the sum of the LT317's dropout voltage (approximately 2V) and the voltage drop across the R_1+R_2 series resistance: $V_{MAX}=V+ - 2V-I_{MAX}(R_1+R_2)$. In the circuit in **Figure 1**, this voltage is V+ − 4.5V. This arithmetic leads to a V_{MAX} of only 500 mV if you use the W_1 option and V+ = 5V. This compliance figure may be insufficient for some applications. If, by contrast, you choose the W_2 option and V+ is greater than 7.5V (not necessarily regulated), V_{MAX} increases to a much more adequate 2.5V.

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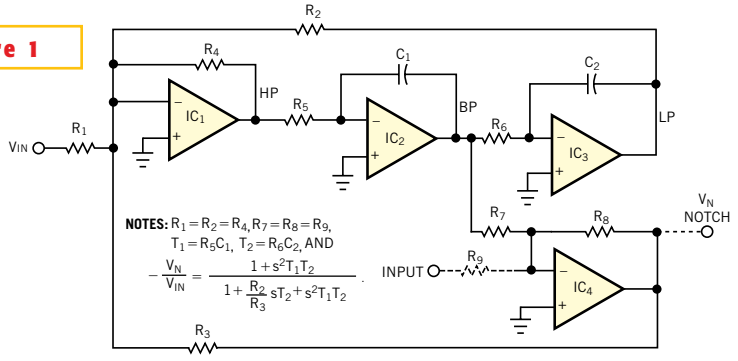
Closing the loop deepens notches

Tom Napier, North Wales, PA

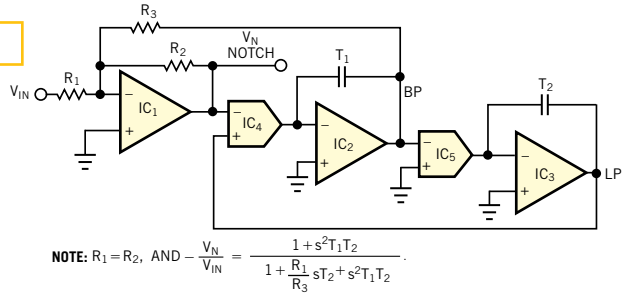
Notch filters remove a single unwanted frequency from an input signal. They are also a vital component of pulse-shaping networks, such as time-averaging filters. You can tune a state-variable filter over a wide range by changing the time constants of its integrating amplifiers (**references 1**, **2**, and **3**). Textbooks focus on its high-pass, bandpass, and low-pass outputs, but they sometimes fail to note that subtracting the bandpass output from the input signal creates a notch filter. The attenuation of such an open-loop notch filter is limited by how well the components match; typically, it's approximately 40 dB. **Figure 1** shows a standard state-variable filter with an amplifier, IC_4, added to invert the bandpass output. You can implement a notch filter by adding a further amplifier to sum the input signal and the output of IC_4.

Figure 1



Changing connections makes the depth of the notch depend only on the gain of the integrating amplifiers.

Figure 2



Replacing two resistors by multiplier ICs results in a tunable notch filter.

An alternative is to move the input to R_9 and to take the notch output from the output of IC_4. Closing the loop around the notch filter makes the depth of the notch depend only on the gain of the integrating amplifiers. Replacing R_5 and R_6 by differential-input, current-output multipliers (for example, the Harris HA2547) creates the tunable notch filter in **Figure 2**. The time constants T_1 and T_2 are the products of the values of the integrating capacitors and the multipliers' transimpedances. In **Figures 1** and **2**, R_3 controls the width of the notch.

References

1. Napier, Tom, "Multipliers implement tunable filters," *EDN*, March 16, 1992, pg 131.
2. Siu, Chris, "Design innovations provide for voltage-tunable, state-variable active filters for megahertz ranges," *EDN*, Sept 28, 1995, pg 117.
3. Napier, Tom, "Take tunable lowpass filters to new heights," *EDN*, Jan 15, 1998, pg 145.

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Hints and kinks for USB decoding

Bert Erickson, Fayetteville, NY

The USB is a serial data-transmission system that uses cables to connect peripheral equipment to PCs. All new computers have two or more USB receptacles, and the predictions are that they will replace most of the legacy receptacles on older PCs. The 1.0 and 1.1 standards for USB were for 1.5 and 12 Mbps at low- and full-speed rates, respectively. These standards targeted low- and medium-speed peripherals. The latest 2.0 standard is for a 480-Mbps rate that will accommodate many high-speed devices along with the previous low- and full-speed rates. At the PC-accessible USB receptacle and at the peripheral, if it has a receptacle, the signal has the format of differen-

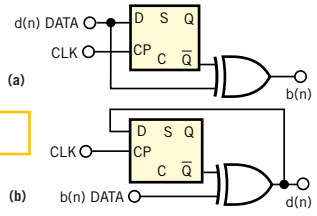
TABLE 1–BINARY VERSUS DIFFERENTIAL-NRZI CODE

Binary		Differential NRZI				
b(n − 1)	b(n)	d(n − 1)	d(n)	or	d(n − 1)	d(n)
0	0	1	0		0	1
0	1	0	0		1	1
1	0	0	1		1	0
1	1	1	1		0	0

tial-NRZI (nonreturn-to-zero-inverted) code. After conversion (with a simple circuit or test probes) of this differential to single-ended signal, the signal becomes a waveform that assumes the voltage levels used to recognize ones and zeros in computer code.

In this NRZI waveform, a transition between the d(n−1) and d(n) bits decodes to a binary b(n)=0 data bit. No transition decodes to a binary b(n)=1 bit. However, when you display the d(n) waveform on an oscilloscope of a logic analyzer, it is difficult for an observer to decode it back to the originating binary waveform, or vice versa. In this situation, you may doubt your judgment and turn to dedicated test equipment to make the conversion. Much of the human problem occurs because NRZI decoding depends on knowledge of the previous and current input bits to determine a value for the current output bit. In the encoding descriptions in most textbooks and technical articles, the transitions receive passing mention, and the material presents a pair of waveforms with little or no elaboration. The following suggestions involve some computer statements and logic circuits that provide a different way to effect the conversion.

Figure 1



Simple circuits perform NRZI-to-binary (a) and binary-to-NRZI (b) conversion.

Table 1 shows all the combinations that can exist in NRZI encoding. For the differential-NRZI-d(n)-to-binary-b(n) code conversion, the following observations apply:

- The conversion is independent of b(n−1).
- If d(n−1)≠d(n), then b(n)=0.
- If d(n−1)=d(n), then b(n)=1.
- Or, simply, b(n)=d(n) XOR NOT d(n−1).

You can perform the conversion by using an XOR gate and a 74LS74 D-type, positive-edge-triggered flip-flop (**Figure 1a**). The flip-flop's Set and Clear terminals connect to V_{CC}, and you do not need to reset either one. For the binary b(n) to differential NRZI d(n) conversion, we offer the following observations:

- The conversion is not independent of d(n−1).

d(n)=d(n−1) *unless*

- b(n−1)=0 AND b(n)=0, then d(n)=NOT d(n−1), or
- b(n−1)=1 AND b(n)=0, then d(n)=NOT d(n−1).

You can perform the conversion by using an XOR gate and a 74LS74 D-type positive-edge-triggered flip-flop (**Figure 1b**). The flip-flop's Set and Clear terminals connect to V_{CC} *after* you use them to set d(n) to its proper initial value. For all input-data sequences that keep repeating, you must select the last and first bits to produce the first output bit. You can download a computer program that confirms the decoding from the Web version of this article at www.ednmag.com.

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