design ideas

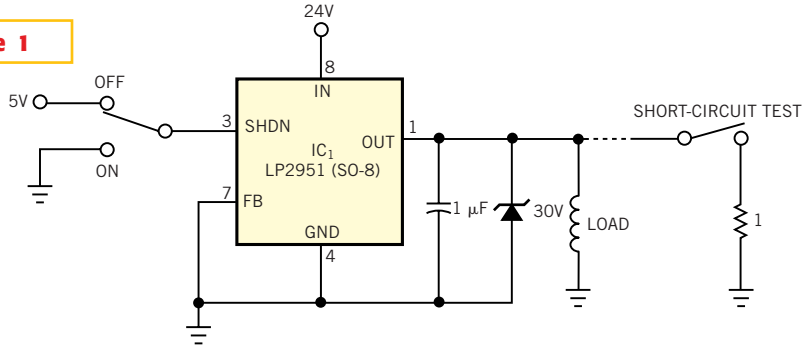
Edited by Bill Travis

High-side driver has fault protection

Carl Spearow, Tokyo Electron, Gilbert, AZ

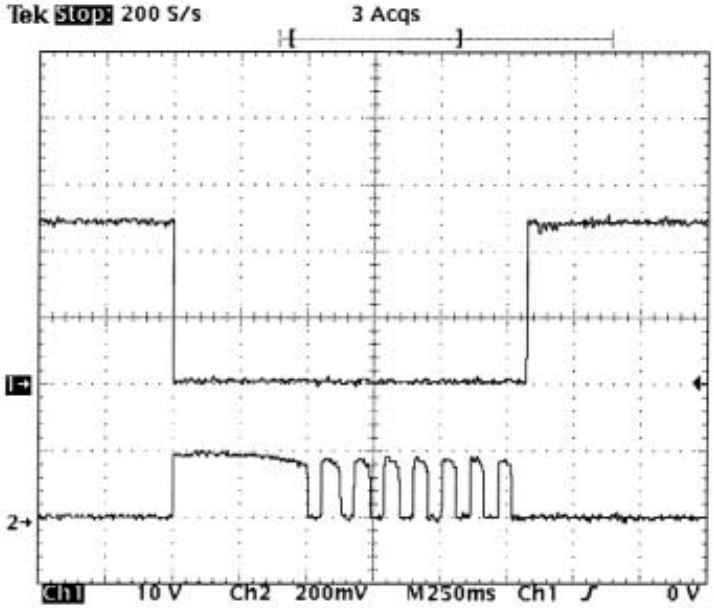
High-side drivers find common use in driving grounded solenoid coils and other loads. Short-circuit protection for such drivers is essential for avoiding damage from wiring faults and other causes. Polymer fuses are generally too slow, and discrete current-limiting circuits are large and cumbersome. The circuit in **Figure 1** uses a small, low-dropout linear regulator as a high-side switch and provides inherent current limiting and thermal shutdown. The regulator comes in an SO-8 package. The zener diode provides transient protection, and the output capacitor ensures stability of the circuit. The circuit can drive a 24V load at 100 mA. These are adequate specs for many solenoid valves, relay coils, and other moderate loads. During a short circuit, the regulator limits the current to 160 mA. This current causes the die to overheat and enter a thermal-shutdown state. Upon removal of the short circuit, the device cools down and resumes normal operation. The top trace in **Figure 2** is the output voltage during a 1.3-sec short circuit. The bottom trace is the short-circuit current, which limits itself at less than 200 mA. Note that the regulator goes into thermal shutdown after 500 msec, and the IC then toggles on and off until removal of the short circuit.

Figure 1



This simple high-side driver provides current limiting as well as transient protection.

Figure 2



In the bottom trace, the output current limits itself to 160 mA during a short circuit.

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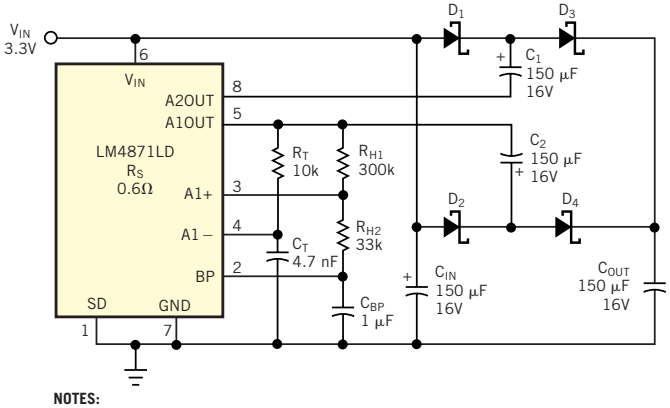
Boost 3.3V to 5V with tiny audio amplifier

Wayne Rewinkel, National Semiconductor, Santa Clara, CA

THIS CHARGE-PUMP CIRCUIT quietly converts a 3.3V source to 5V at 500 mA (**figures 1** and **2**). National's (www.national.com) LM4871LD power amplifier makes this design idea both possible and practical, thanks to its low output resistance, low cost, compact size, and high dissipation capability. Its output resistance has an average value of 0.6Ω: 0.5Ω to ground and 0.7Ω to V_{IN}. Because it is a CMOS IC, each output can swing to its rail, limited only by the resistance of the output transistor. The leadless lead-frame package has a footprint smaller than an SO-8 but provides a θ_{JA} of 56°C/W when soldered to a board with 1 sq in. of 1-oz copper exposed. This high thermal conductivity couples with low output resistance to allow the 4871 to continuously deliver nearly 1A from each of its two outputs while operating at its full rated ambient temperature of 85°C. Internal thermal shutdown protects the device from overloads, and a shutdown pin allows you to power down the device to less than 1 µA.

Figure 1



NOTES:
1. D_1 AND D_2: MBRS120T3.
2. C_1 AND C_2 ESR<11Ω.

You can use a tiny audio amplifier to boost 3.3V to 5V with respectable current capability.

Figure 2 shows the full circuit schematic, including the equivalent internal components. Amplifier IC_1 is configured as an RC oscillator similar to a 555 timer. R_T charges C_T to the voltage set by the resistor divider R_{H1} and R_{H2}, causing the amplifier to switch states, aided by the positive feedback from the R_H resistors. The remaining internal feedback and biasing resistors connected to IC_2 configure it as a simple inverter with bias at mid-supply. The amplifier outputs switch rail-to-rail out of phase with a 50% duty cycle at a frequency approximated by the following equation:

$$\frac{1}{f} = 4\ \mu SEC + \frac{4R_TC_T}{\left(\frac{R_{H1}+R_{H2}}{R_{H2}}\right)},$$

$$f = 44 \text{ TO } 53 \text{ kHz}.$$

You can calculate the output voltage across C_{OUT} from the following equation:

$$V_{OUT} = 2\left(V_{IN} - V_{DIODE} - I_{OUT}R_S - I_{OUT}(ESR) - I_{OUT}/Cf\right)$$
$$= 2(3.3 - 0.35 - 0.3 - 0.05 - 0.062) = 5.08V,$$

where I_{OUT} is the average output current, V_{DIODE} is the diode voltage drop at I_{OUT}, R_S is the source resistance of IC_1 and IC_2, ESR is that of C_1 and C_2, and C is the value of $C_1 = C_2$.

The following equation approximates the effective output resistance at the load:

$$R_{OUT} = 2\left(R_S + R_{DIODE} + ESR + 1/Cf\right) =$$
$$2(0.6 + 0.15 + 0.11 + 0.07) = 1.9\Omega.$$

Component values as shown in **Figure 1** provide a circuit that can produce 5V at 0.5A from a 3.3V source at a conversion efficiency of 78%. If necessary, you can obtain tighter regulation figures at slightly lower output current by adding a low-dropout linear regulator, such as the LP3961. At a 500-mA load it introduces a drop of only 150 mV. Its addition provides good line and load regulation over the range I_{OUT}=0 to 500 mA (**Figure 3**). You can also use the circuits of **figures 1** and **3** to provide 3.3V at 500 mA from a 2.5V source.

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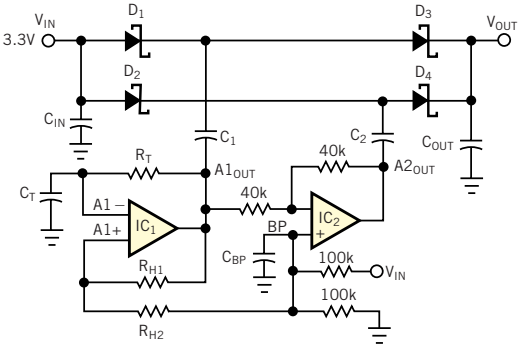
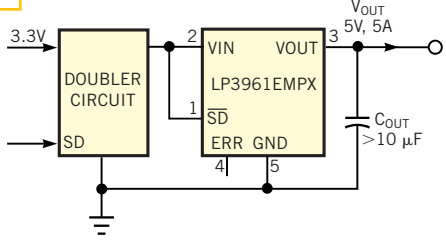
Figure 2



This equivalent circuit shows the innards of the LM4871LD audio amplifier.

Figure 3



You can tighten voltage-regulation specs in Figure 1's circuit by adding a linear regulator.

Add a signal-strength display to an FM-receiver IC

José Miguel-López, RF Center Ltd, Barcelona, Spain

The Philips (www.semiconductors.philips.com) TDA7000 integrates a monaural FM-radio receiver from the antenna connection to the audio output. External components include one tunable LC circuit for the local oscillator, a few capacitors, two resistors, and a potentiometer to control the variable-capacitance-diode tuning. The IC has an FLL (frequency-locked-loop) structure. The filtered output of the FM discriminator frequency-modulates the local oscillator to provide negative-feedback modulation. The result is compression of the signal at the output of the mixer. Thus, the IF bandpass filter and the FM discriminator deal with narrowband FM signals. For a compression factor of K=3, the original FM bandwidth reduces to 180/3=60 kHz. So, you need neither ceramic filters nor complex LC tank circuits to realize the IF filter. A simple active filter using op amps can fulfill the task. The IC incorporates a correlation muting system that suppresses interstation noise and spurious responses arising from detuning. The muting circuit uses a second mixer. Its output is available at Pin 1; you can use it to drive a detuning indicator. You can add a signal-strength display to the TDA7000 using the circuit in **Figure 1**.

You can obtain the information related to the intensity of the received signal at the output of the IF filter (IC_1, Pin 12). You can easily process this voltage with common op amps, because the IF signal is centered on 70 kHz. The voltage at Pin 12 is dc-coupled to an amplifier, IC_2. Next, an envelope detector, IC_3, yields a dc voltage proportional to the received-signal strength. The Siemens (www.siemens.com) TCA965 window discriminator, IC_4, compares this envelope voltage with a voltage derived from R_1, R_2, and R_3 for the window's center (and R_4 and R_5 for the window's half-width). Three LEDs show the result of the comparison (Low, OK, Good), but the display is valid only if the tuning is correct. If it's correct, the voltage at IC_1, Pin 1 reaches its maximum value, and the LM311 comparator, IC_5, enables the TCA965.

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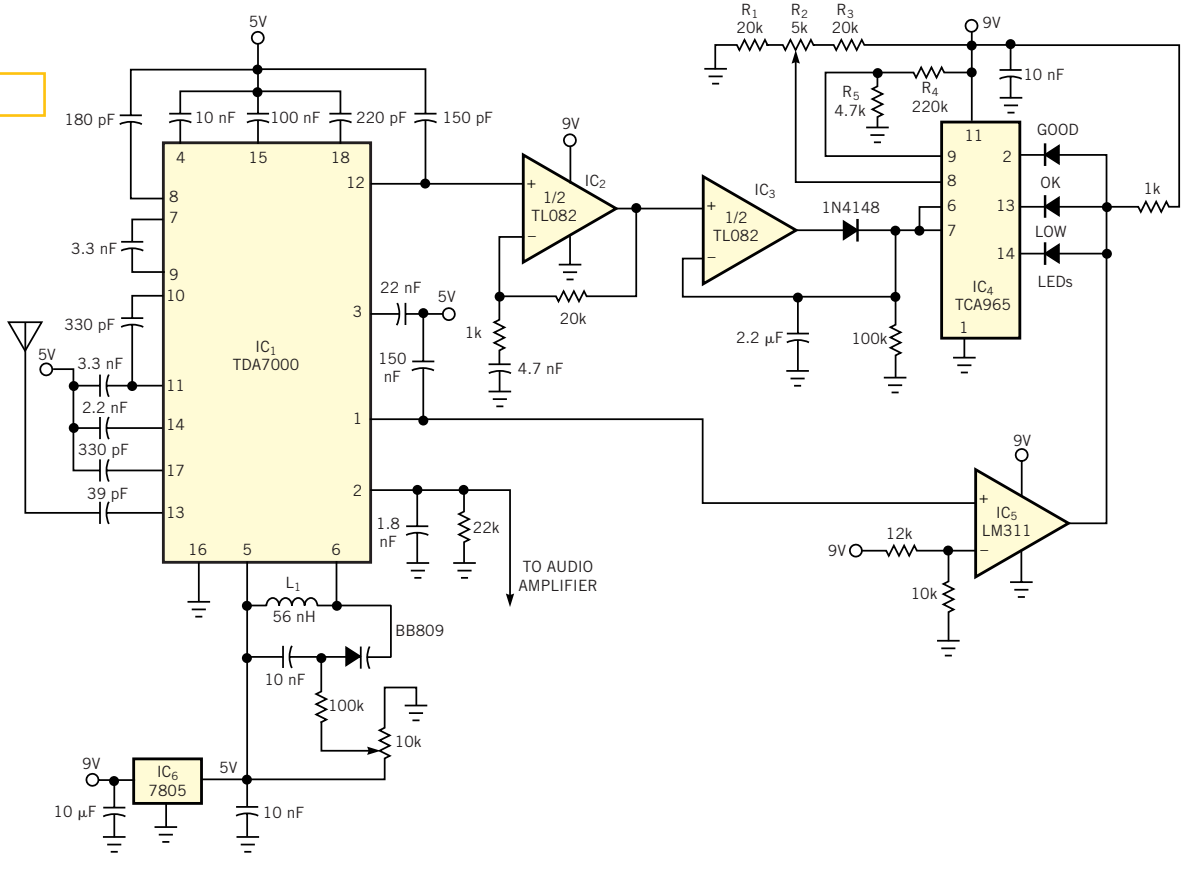
Figure 1



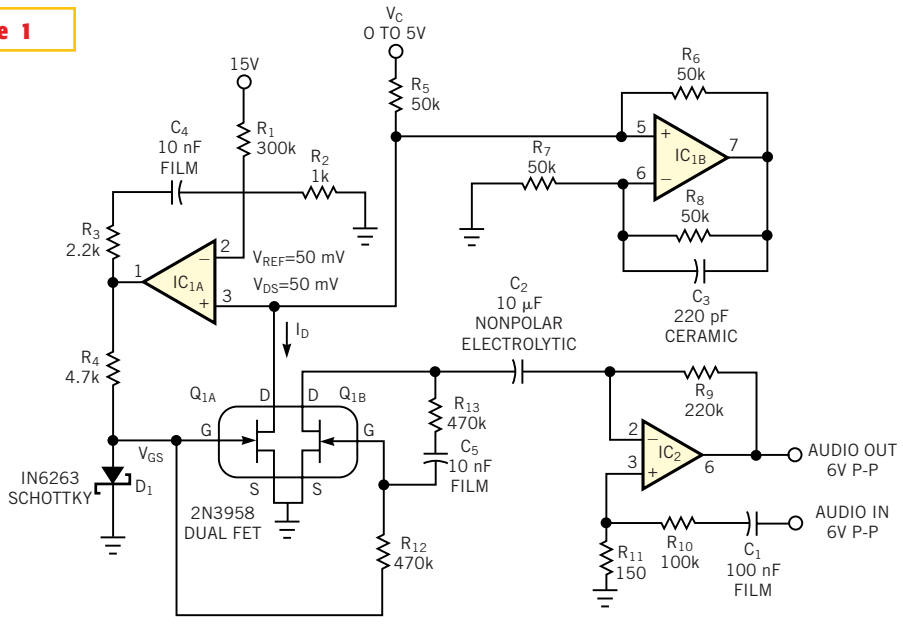
You can easily add a signal-strength indicator to the Philips TDA7000 FM-receiver IC.

Op amp linearizes response of FET VCA

Mike Irwin, Shawville, PQ, Canada

FETs find common use in VCAs (voltage-controlled amplifiers) and attenuators, in which the FET serves as a variable resistance. A control voltage applied to the gate sets the channel resistance and overall circuit gain. You frequently need to select individual FETs because of wide spreads in FET characteristics. The circuit in **Figure 1** uses a master-slave servo technique with a matched-FET pair to implement voltage-controlled variable gain. This gain is a linear function of the applied control voltage, V_C. In contrast with variable-gain circuits using a single FET as the gain-control element, the circuit in **Figure 1** exhibits minimum gain for V_C=0V and features a linear increase in gain with increasing V_C. The self-biasing operation of the circuit also compensates for unit-to-unit variations in the FET characteristics, thereby making device selection less critical.

Figure 1



This voltage-controlled amplifier has a dynamic range of −55 to 0 dB.

The circuit maintains the drain voltage, V_{DS}, of Q_{1A} at a low value (V_{REF}=50 mV) to ensure that the FET operates in the resistive region of its I_D versus V_{DS} characteristic curve. Op amp IC_{1A} servos the V_{GS} of Q_{1A} to maintain V_{DS} at V_{REF}, while Q_{1A} sinks the current from the Howland current source IC_{1B}. The sourced current is $I_D(mA)=V_C/R_5(k\Omega)$, where V_C is the control voltage. The channel resistance, R_D, in kilohms is then $R_D=V_{REF}/I_D=0.05/I_D=0.05\times R_5/V_C$. The same V_{GS} applies to Q_{1B} through R_{12}. Because Q_1 is a well-matched monolithic dual FET, Q_{1A} and Q_{1B} have identical channel resistance, R_D. V_{GS} varies from approximately 370 mV (which D_1 limits to prevent gate-source conduction) to V_P (approximately −1.7V for the 2N3958) as V_C varies from 0 to 5V. IC_2 is a variable-gain, noninverting amplifier, in which the controlled R_D of Q_{1B} sets the gain: $\text{Gain}=1+R_9/R_D=1+R_9/(V_{REF}\times R_5/V_C)$.

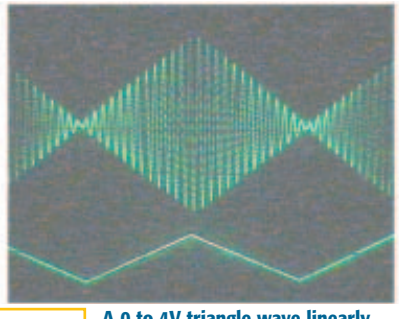


Figure 2 A 0 to 4V triangle wave linearly modulates the 500-Hz audio input.

The maximum gain is $1+R_9/R_0$. R_0 is the minimum channel resistance for V_{GS}=0V, approximately 450Ω for the 2N3958. The minimum gain is unity, when the FET does not conduct ($V_{GS}=V_{PINCHOFF}$). The circuit attenuates the audio-input signal level to lower than 10 mV p-p. This attenuation minimizes distortion in the FET and also sets the clipping level at the output of IC_2. R_{13} and C_5, in combination with R_{12}, reduce distortion at higher signal levels. With the values shown, the gain increases linearly from −55 to 0 dB as V_C varies from 0 to 5V. The circuit accepts a 6V p-p input signal. **Figure 2** shows the result of modulating a 500-Hz sine wave with a 0 to 4V triangle wave.

For best performance, IC_1 should be a low-offset, low-input-current unit, such as the OP-290. IC_2 should be a high-gain-bandwidth-product, low-noise amplifier, such as the NE5534. You can successfully use inexpensive units, such as the LF353 and LF351, at reduced gains. You can also operate the circuit from ±5V supplies (with R_1 changed to 100 kΩ), using an OP-290 for IC_1 and a TL031 for IC_2. The maximum supply current for ±5V operation is 0.33 mA, showing that low-power operation is possible.

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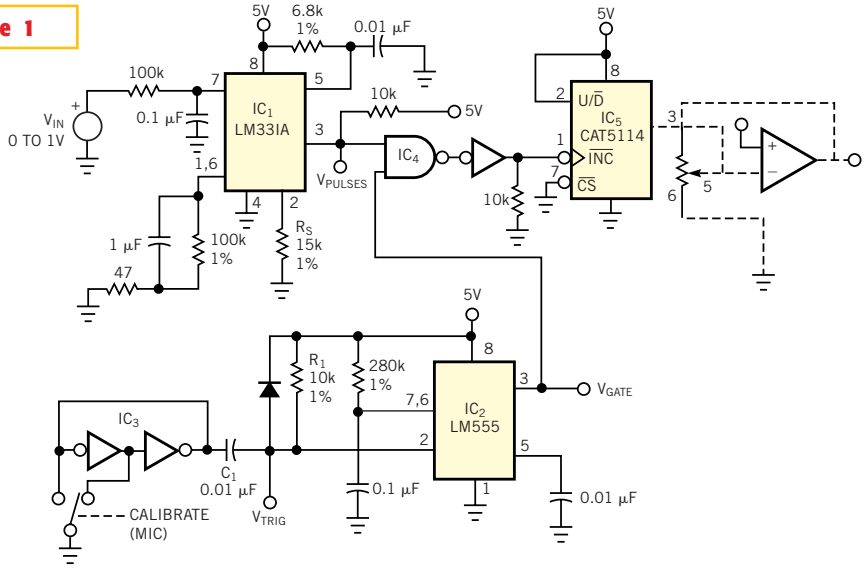
Convert voltage to potentiometer-wiper setting

Chuck Wojslaw, Catalyst Semiconductor, Sunnyvale, CA, and Chris Wojslaw, Conexant Systems, Newport Beach, CA

THE CIRCUIT IN **Figure 1** converts an analog input voltage, V_{IN}, to a proportional wiper setting of a DPP (digitally programmable potentiometer). The potentiometer's wiper setting, which varies from position 0 through 31, corresponds to the input voltage, which varies from 0 to 1V dc. The CAT5114, IC_5, is a 32-tap potentiometer with an increment/decrement interface. V_{IN} typically models the output voltage of a sensor whose value sets a parameter of an analog circuit in the signal-processing portion of a system. The basic principle of the circuit is to convert the input voltage to a number of pulses and let each pulse advance the potentiometer's wiper within a certain period of time. IC_1 is a voltage-to-frequency converter. This circuit converts the 0 to 1V dc input voltage to an output frequency, V_{PULSES}, that varies from 0 to 1 kHz.

Figure 1



You can convert an analog voltage to a wiper setting in a digitally programmable potentiometer.

This free-running oscillator advances the wiper of the potentiometer for only 31 msec, established by V_{GATE} and the AND function of IC_4. V_{GATE} is the output of the one-shot multivibrator, IC_2. The one-shot receives its trigger from a calibrate switch or an external signal. The hex inverters of IC_3 debounce the calibrate switch. R_1C_1 differentiate the voltage-level shift generated by the switch to provide a nominal 100-µsec trigger, V_{TRIG}, to IC_2. V_{TRIG} could also be a processor-generated logic signal. The 31-msec gating signal is chosen to correspond to the highest tap position of the potentiometer at the highest frequency of the voltage-to-frequency converter. For a 100-tap potentiometer, the gating signal measures 99 msec for the same sensitivity of the voltage-to-frequency converter. You can trim the 15-kΩ resistor, R_S, to match the timing of the 331 converter to the pulse width of the 555.

Tap position 00 of the digitally controlled potentiometer is stored in the DPP's nonvolatile memory and the potentiometer's up/down control is set to up. When the DPP powers up, the IC recalls wiper setting 00 from nonvolatile memory. When you depress the calibrate switch, the wiper increments from 00 to a setting corresponding to the input voltage, V_{IN}. You can use the three-terminal resistive network of the potentiometer to control the gain of an amplifier (shown in broken lines in **Figure 1**), a parameter of a filter, or the coefficient of a mathematical operator.

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Make a DAC with a microcontroller's PWM timer

Mike Mitchell, Texas Instruments Inc

MANY EMBEDDED-microcontroller applications require generation of analog signals. An integrated or stand-alone DAC fills the role. However, you can often use PWM signals for generating the required analog signals. You can use PWM signals to create both dc and ac analog signals. This Design Idea shows how to use a PWM timer to simultaneously create a sinusoid, a ramp, and a dc voltage. A PWM signal is a digital signal with fixed frequency but varying duty cycle. If the duty cycle of the PWM signal varies with time and you filter the PWM signal, the output of the fil-

ter is an analog signal (**Figure 1**). If you build a PWM DAC in this manner, its resolution is equivalent to the resolution of the PWM signal you use to create the DAC. The PWM output signal requires a frequency that is equivalent to the update rate of the DAC, because each change in PWM duty cycle is the equivalent of one DAC sample. The frequency the PWM timer requires depends on the required PWM signal frequency and the desired resolution. The required frequency is $F_{CLOCK}=F_{PWM}\times 2^n$, where F_{CLOCK} is the required PWM-timer frequency, F_{PWM} is the PWM-signal frequency, and n is the desired DAC resolution in bits.

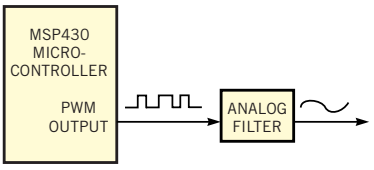


Figure 1

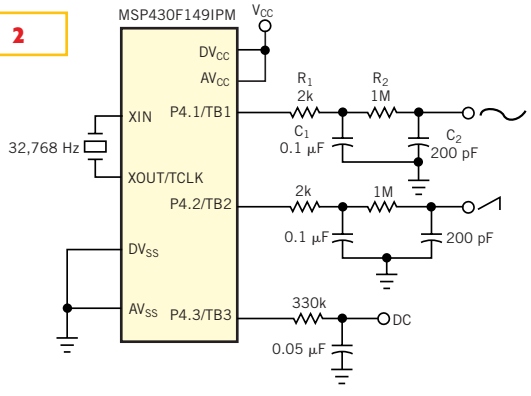
A PWM signal passing through a filter yields and analog signal.

Figure 2 depicts a circuit that delivers a 250-Hz sine wave, a 125-Hz ramp, and a dc signal. The desired sampling rate is 8 kHz (32 samples for each sine-wave cycle (16× oversampled), and 64 samples for each ramp cycle (32× oversampled)). These figures result in a required PWM-signal frequency of 8 kHz and a required PWM clock frequency of 2.048 MHz. It is usually best for the PWM signal frequency to be much higher than the desired bandwidth of the signals to be produced. Generally, the higher the PWM frequency, the lower the order of filter required and the easier it is to build a suitable filter. This design uses Timer B of the MSP430 in 16-bit mode and in "up" mode, in which the counter counts up to the contents of capture/compare register 0 (CCR0) and then restarts at zero. CCR0 is loaded with 255, thereby giving the counter an effective 8-bit length. You can find this register and others in a DAC demonstration program for the MSP430 microcontroller. You can download the program from the Web version of this Design Idea at www.edn.com.

CCR1 and output TB1 produce the sine wave. CCR2 and TB2 generate the ramp, and CCR3 and TB3 yield the dc value. For each output, the output mode is the reset/set mode. In this mode, each output resets when the counter reaches the respective CCRx value and sets when the counter reaches the CCR0 value. This scheme provides positive pulses equivalent to the value in CCRx on each respective output. If you use the timer in 8-bit mode, the reset/set output mode is unavailable for the PWM outputs because the reset/set mode requires CCR0. The timer's clock rate is 2.048 MHz. **Figure 3** shows the sine and ramp waveforms. The sine wave in this example uses 32 samples per cycle. The sample values are in a table at the beginning of the program. A pointer points to the next value in the sine table, so that, at the end of each PWM cycle, the new value of the sine wave is written to the capture/compare register of the PWM timer.

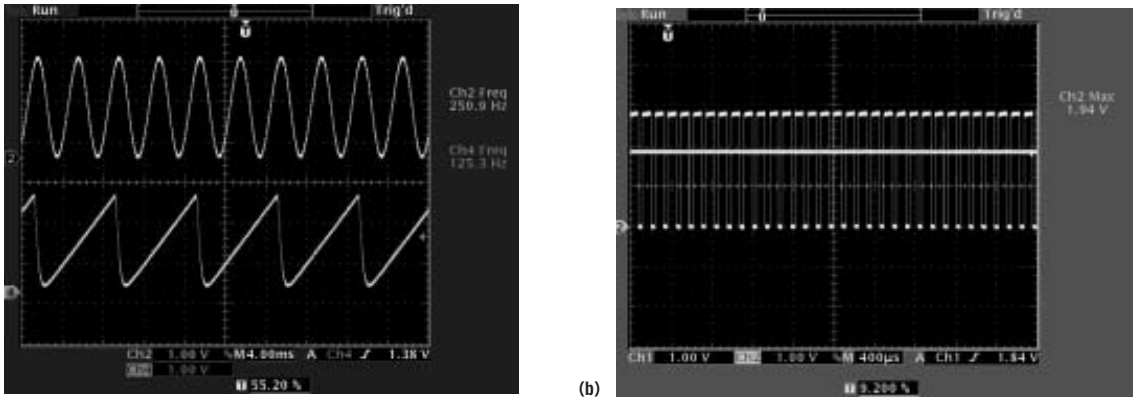
The ramp in this example does not require a table of data values. Rather, the ramp simply increments the duty cycle for each cycle of the PWM signal until it reaches the maximum and then starts over at the minimum duty cycle. This gradual increase in PWM-signal duty cycle results in a ramp voltage when the signal passes through a filter. You control the dc level by simply setting and not changing the value of the PWM-signal duty cycle. The dc level is directly proportional to the duty cycle of the PWM signal. **Figure 2** shows the reconstruction filters used for each signal in this example. The filter for the ac signals is a simple two-pole, stacked-RC filter, which is simple and has no active components. This type of filter necessitates a higher sampling rate than would be re-

Figure 2



A microcontroller and some passive filters produce a sine wave, a ramp, and a dc signal.

Figure 3



The microcontroller's PWM timer produces an ac signal (a) and a dc signal (b) of a sine wave and a ramp with 8-bit resolution.

quired if the filter had a higher order. With the type of filter shown in **Figure 2**, you should use at least a 16× oversampling rate.

The filter yields its best response when $R_2 >> R_1$. Also, setting the cutoff frequency too close to the bandwidth edge causes a fair amount of attenuation. To reduce the amount of attenuation in the filter, set the cutoff frequency above the bandwidth edge but much lower than the frequency of the PWM signal. The filter for the dc value serves for charge storage rather than ac-signal filtering. Therefore, it uses a simple, single-pole RC filter. **Figure 4** shows the software flow for the DAC. After a reset, the routine stops the watchdog timer, configures the output ports, and sets up the clock system. Next, the software calls a delay to allow the 32,768-Hz crystal to stabilize to calibrate the DCO (digitally controlled oscillator).

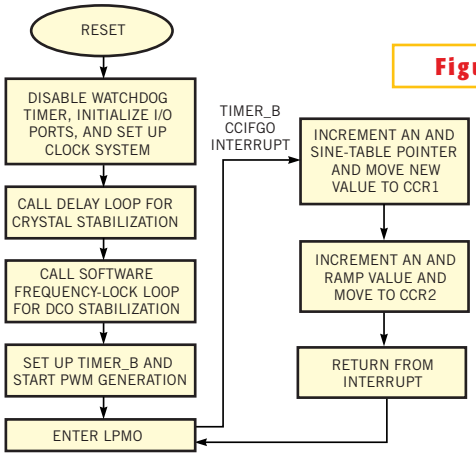


Figure 4

This software flow diagram shows how the PWM timer generates the sine and ramp signals.

Next, the routine calls the calibration routine to set the operating frequency to 2.048 MHz. After the DCO calibration, the program sets up Timer_B, CCR1 and CCR2 for PWM generation and then starts the timer. Finally, the MSP430 goes into low-power mode 0 (LPM0) to conserve power. The CPU wakes up to handle each CCIFG0 interrupt from the PWM timer and then re-enters LPM0. (See **references 1**, **2**, and **3** for more information on the DCO and the MSP430 family.)

References

1. MSP430x13x/14x data sheet, Texas Instruments document SLAS-272.

2. MSP430x1xx Family User's Guide, Texas Instruments document SLAU049.

3. "Controlling "the DCO of the MSP430x11x," Texas Instruments document SLAA074.

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