design ideas

Edited by Bill Travis

Passive circuit limits inrush current

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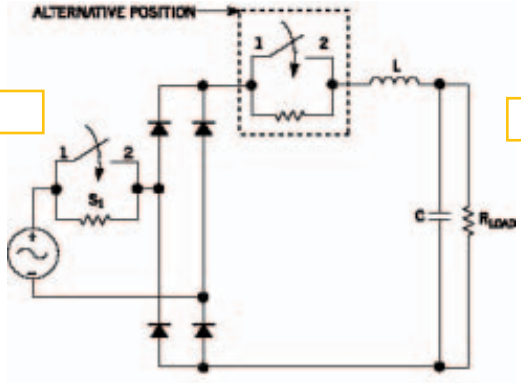
You would normally limit the inrush current during start-up of a rectifier circuit with a capacitor output filter by using the circuit in **Figure 1**. You insert a high resistance in series with the ac input or the dc output of the rectifier and then short-circuit the resistance with a switch once the filter capacitor is sufficiently charged. In this scheme, you need an additional timer relay or sensing circuit to control the closure or opening of the switch. Moreover, the switch carries the full load current during normal operation. As an alternative, the simple, passive circuit in **Figure 2** for inrush-current limiting uses commercially available components and presents advantages in size and cost. The resistance-switch arrangement inserted in series with the filter capacitor, instead of in the main power line, limits inrush current in this circuit. The current rating of the switch can therefore be much lower. A switch, S_1, short-circuits the charging resistor, R_1. This switch represents the contact of a commercially available dc relay. The relay senses the voltage on capacitor C; thus, the switch operates automatically.

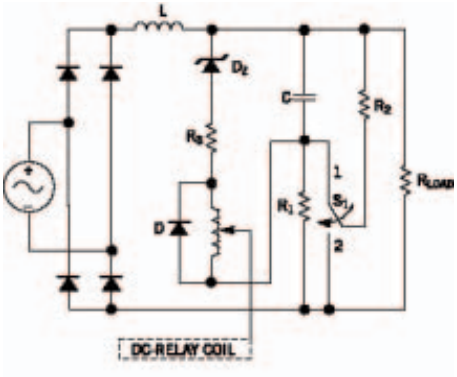
R_1 limits the peak inrush current and also determines the start-up delay. The

Figure 1



In this classic inrush-limiting circuit, the switch carries the full load current during normal operation.

Figure 2



In this inrush-limiting circuit, the current rating of the switch is considerably reduced.

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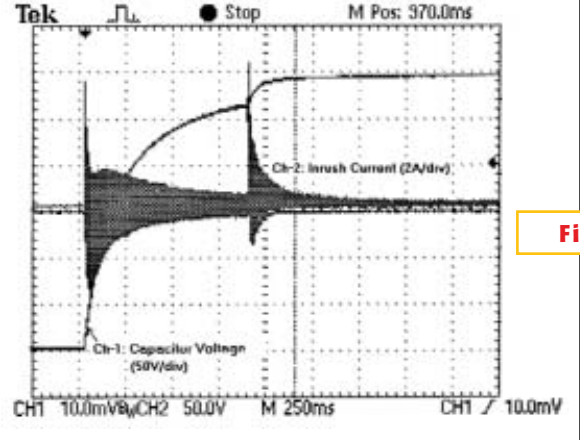

Figure 3

The circuit in Figure 2 limits the inrush current to a safe value of approximately 6A.

relay's changeover contact either short-circuits R_1 when the capacitor is sufficiently charged or connects R_2 across the capacitor to speed its discharge in the off condition. For jitter-free operation of the relay, you need suitable hysteresis between closure and opening. Too little hysteresis results in malfunction of the circuit in the presence of momentary dips. Too much hysteresis leaves the circuit unprotected against heavy inrush currents upon reclosure of the relay. You can incorporate suitable hysteresis by adding zener diode D_Z and resistor R_3 in series with the relay coil. The following equations describe the operation of the circuit in **Figure 2**:

Dc pickup voltage:

$$V_{DCP} = V_{CP}\frac{(R_C + R_3)}{R_C} + V_Z;$$

Dc dropout voltage:

$$V_D = I_Z(R_C + R_3) + V_Z;$$

and hysteresis:

$$V_{DCP} - V_D = V_{CP}\frac{(R_C + R_3)}{R_C} - I_Z(R_C + R_3),$$

where V_{CP} is the relay-coil pickup voltage, R_C is the relay-coil resistance, V_Z is the zener-diode breakdown voltage, and I_Z is the zener-diode knee current.

Commercial-grade components have variations in their parameters. These variations can affect the dc pickup and dropout voltages. For minimum sensitivity to variations in V_{CP}, R_C, and I_Z, you should make R_3 as low as possible. Tolerances in V_Z and R_3 have an insignificant effect on the circuit; however, I_Z is temperature-dependent, and its effect on dropout voltage is significant. **Figure 3** shows the experimental results. The prototype uses the following component values: C=2000 µF (nonpolar), R_1=36Ω, R_2=4.7 kΩ, R_3=12 kΩ, V_Z=110V, I_Z=3 mA, V_{CP}=65V, and R_C=10 kΩ.

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Transmitter senses triple relative-humidity figures

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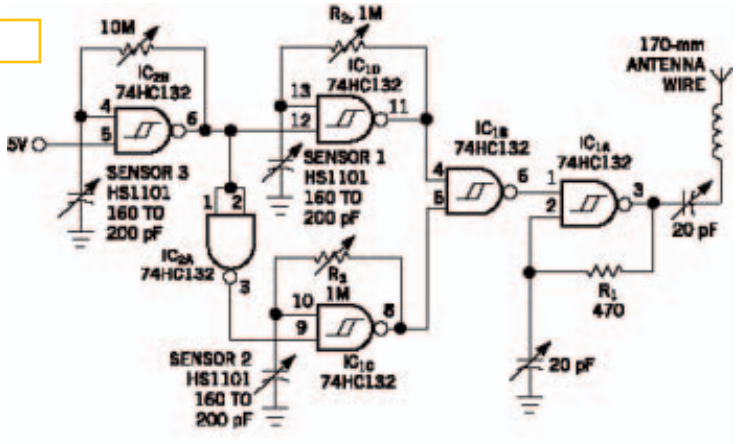
THE CIRCUIT IN **Figure 1** is a triple, relative-humidity sensor and radio transmitter. Sensors 1 and 2 form two gated oscillators with natural frequencies of 10 and 5 kHz, respectively, at relative humidity of 50%. The gated oscillators use variable resistances R_2 and R_3, respectively. Together, these two oscillators generate FSK-modulated outputs at output of IC_{1B}, Pin 6. The oscillator for Sensor 3 causes switching of the FSK signal at IC_{2B}. IC_{2B}'s natural frequency is 1 kHz at relative humidity of 50%. As the HS1101's capacitance changes from 160 to 200 pF (180 pF at relative humidity of 50%), the oscillator frequencies change by approximately ±20% for relative humidity of 0 to 100%). You can tune the RF generator, IC_{1A}, to the desired frequency of 27 to100 MHz for FM transmission. The following represents various ways to monitor the signals at the receiver end (not included in the design):

- Sensor 3 signal is the FSK-modulated signal at the receiver: 1 kHz±20% for relative humidity of 0 to 100%.
- Sensor 1 signal is the top FSK frequency, 10 kHz, on the carrier wave. It measures 10 kHz±20% for relative humidity of 0 to 100%.

Figure 1



Using FSK modulation, you can generate three independent relative-humidity measurements with one circuit.

- Sensor 2 signal is the bottom FSK frequency, 5 kHz, on the carrier wave. It measures 5 Khz±20% for relative humidity of 0 to 100%.
- The difference between the top and the bottom FSK modulating frequencies provides the difference in the relative-humidity signals.

You can replace the Sensor 3 circuit with any TTL oscillator circuit with a range of 100 Hz to 1 kHz. You can then generate the frequency from any other type of sensor. This frequency then becomes available at the receiver without affecting the relative-humidity signals from sensors 1 and 2. You can even use a TTL-based ASCII output to replace the Sensor 3 circuit to pass the ASCII data along with relative-humidity signals.

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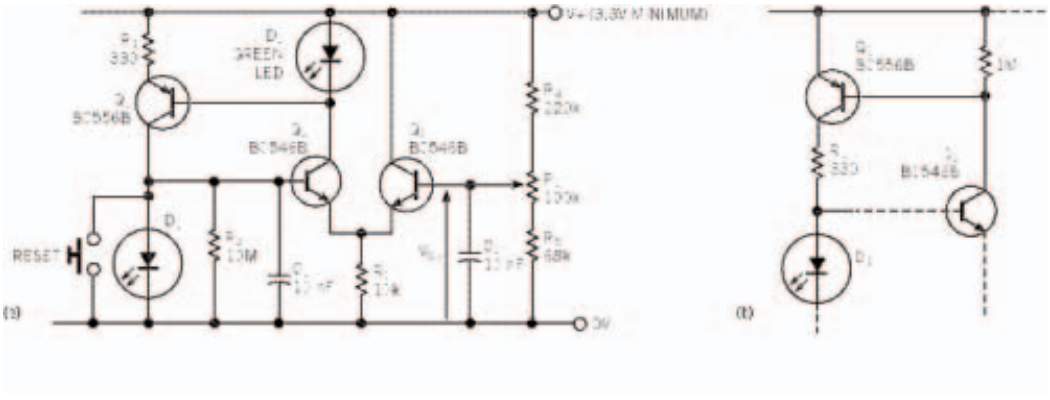
Latching light detector is frugal with power and parts

Anthony Smith, Scitech, Biddenham, Bedfordshire, UK

THIS IDEA DEMONSTRATES three uses for the humble LED. The circuit in **Figure 1a** forms a simple light detector that latches and turns on an LED when the ambient light exceeds a preset limit determined by potentiometer P_1. LED D_1 is both the indicator and the light detector. All junction diodes exhibit some degree of photosensitivity. Light-emitting diodes are photovoltaic in that they generate a small voltage in response to light with suitable spectral content. Provided that they have light loads, some LEDs can generate more than 1V in adequate light conditions. The Q_2-Q_3 differential pair acts as a comparator. At low light levels, the photovoltage that D_1 generates is lower than Q_3's base voltage, V_{B3}, and Q_1 and Q_2 are both off. When the light falling on D_1 exceeds the threshold that P_1 sets, Q_2 begins to conduct, thereby biasing the second LED, D_2, which acts as a voltage reference (the third function of an LED). Q_1 now turns on, sourcing current to D_1, which illuminates.

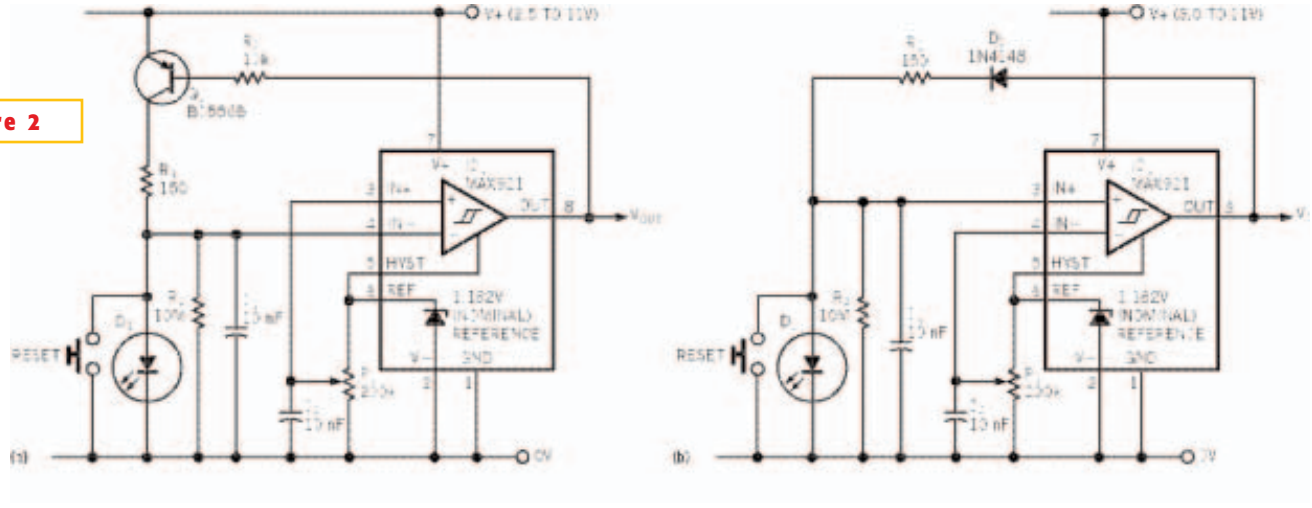
Regenerative action around Q_1 and Q_2 ensures that the circuit makes a rapid transition into the latched state. The circuit stays latched, and D_1 remains illuminated even if the light level falls below

Figure 1



This circuit uses LEDs as both light-detecting and -indicating devices (a). A modification replaces the voltage-reference LED, D_2, by a resistor (b).

Figure 2



This circuit avoids trip-point changes as a function of supply voltage (a). A modification works from slightly higher supply voltages (b).

the trip point. You can reset the circuit by short-circuiting D_1. Because Q_1 is off in the unlatched state, D_1's only load is R_2 and Q_2's base current. Provided that Q_2 has adequate beta and R_3 is fairly large, the loading is negligible. You can use R_2 and C_1 to reduce D_1's sensitivity and provide a degree of filtering. You may need such filtering in noisy environments, such as monitoring the light from fluorescent tubes. With adequate forward current, most green LEDs drop approximately 1.7V, so, in the latched state, approximately 1V appears across R_1. A value of approximately 330Ω sources 3 mA into D_1, providing adequate brightness. For obvious reasons, you should not expose the voltage-reference LED, D_2, to light. If necessary, you can omit D_2 by modifying the circuit (**Figure 1b**). For battery-powered applications, the values of R_4, R_5, and P_1 should be fairly large to ensure minimal current drain in the unlatched condition. If you need a broad threshold range, you should select the values to provide a range of V_{B3} from approximately 0.6 to 1.4V.

You need to experiment to find the optimum LED to act as photodetector. Tests on more than 50 LED color samples produced a range of unloaded output voltage varying from a low of 135 mV to more than 1V in overcast sunshine. A green LED with a clear lens produces almost 1.5V on a dull afternoon. The circuit can work from supply voltages as low as 3.3V, guaranteeing operation from three cells. In the off state, current drain is minimal. The circuit in **Figure 1a** consumed just 88 µA in the unlatched state. Although simple and effective, the circuit suffers the disadvantage that its trip point varies with changes in supply voltage. Also, the trip point's lower limit cannot be less than the 600 mV or so to bias Q_1 and Q_2. The circuit in **Figure 2a** remedies these problems. The circuit uses IC_1's internal bandgap reference to generate a stable threshold. Because the MAX921 (www.maxim-ic.com) comparator's input-voltage range includes the negative rail, you can set the trip point at 0 to 1.18V (the value of the internal reference), thus allowing D_1 to work over a wider range of light levels.

Power requirements are minuscule. The circuit operates from supplies as low as 2.5V (the MAX921's minimum supply voltage), and, in the off state, the only current drain comes from P_1 and IC_1's quiescent supply current. The prototype's total off-state current was just 7.8 µA. You can use the comparator's rail-to-rail output voltage at V_{OUT} as a digital signal and feed it to other systems to indicate light conditions. The comparator output can source more than 10 mA with little reduction in high-level voltage, thus allowing you to slightly simplify the circuit (**Figure 2b**). However, in this version, you must accommodate the voltage drop across D_2, so the minimum supply voltage becomes approximately 3V. Alternative devices you can consider for IC_1 include the Linear Technology (www.linear-tech.com) LTC1440 and the Telcom (www.telcom-semi.com) TC1031.

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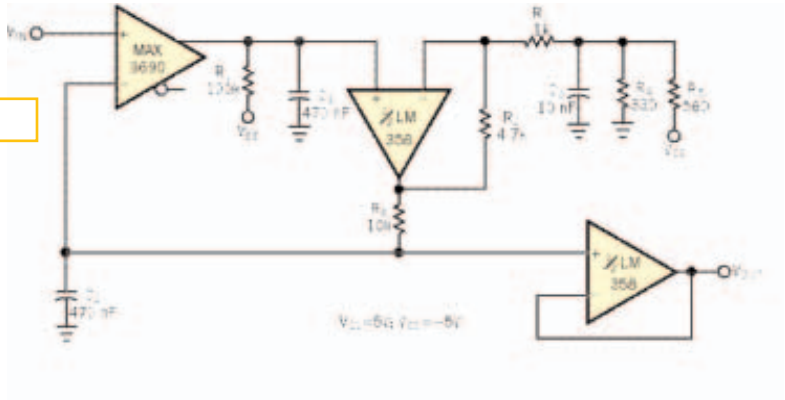
High-speed peak detector uses ECL comparator

Przemyslaw Krehlik and Lukasz Sliwczynski, Institute of Electronics, Krakow, Poland

PROFESSIONAL ELECTRONICS designers often use peak-detector circuit sin such applications as amplitude measurement, automatic gain control, and data regeneration. You can build a simple and fast peak detector from a serial diode and a shunt capacitor, but it suffers from serious inaccuracy that stems from the diode's forward-voltage drop. On the other hand, precise detectors based on op amps are rather slow. They are therefore not well-suited for measuring pulses of a few nanoseconds' duration. The circuit in **Figure 1** offers both good accuracy and good dynamic performance. The main

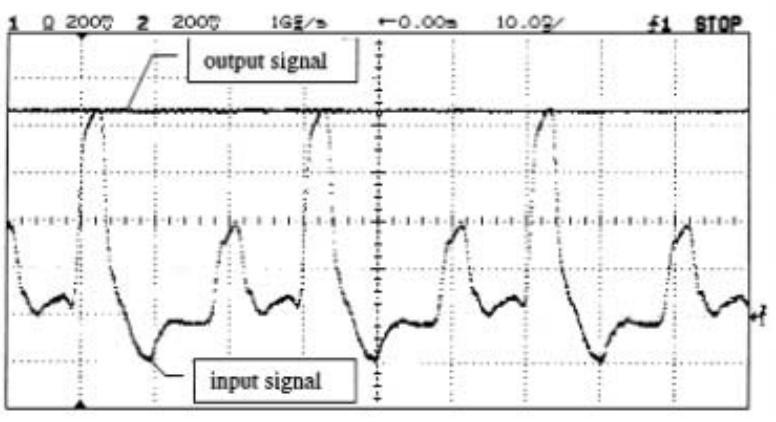
Figure 1



This circuit uses an ultrafast ECL-output comparator to measure the peak value of input signals.

part of the detector is the ultrafast MAX9690 (www.maxim-ic.com), ECL-output comparator. Because the circuit does not internally pull down the output emitter follower, you can use the circuit as a rectifier that charges capacitor C_1. The circuit amplifies and level-shifts the voltage from the capacitor and feeds it back to the negative input of the comparator. When the signal appears at the peak detector's input, capacitor C_1 charges until the feedback voltage at the comparator's negative input becomes equal to the peak value of the signal under measurement; thus, the peak detection occurs. The second op amp forms an output buffer.

Figure 2



The circuit in Figure 1 yields a dc value equal to the positive peak of the input signal.

In this design, the measured peak voltage should be 0 to 2.5V. The detector's accuracy depends on the pulse duration and duty cycle. For example, 1V rectangular pulses having 3-nsec duration and 5% duty cycle produce 5%-low readings. Similar inaccuracy occurs for 10-nsec pulses having 0.1% duty cycle. The accuracy is much better for longer pulse durations, greater duty cycles, or both. The circuit measures pulses lasting for some tens of nanoseconds and having repetition frequency of approximately 1 MHz. To deal with pulses having a lower repetition rate, you should increase the values of C_1 and C_2. That increase would, however, result in longer settling time. Another important element is the discharging resistor, R_1. A value of 100 kΩ for R_1 is appropriate for operation with low-duty-cycle pulses, but you may need lower values for fast tracking with varying input-signal amplitudes. You can also configure a minimum-value peak detector. In this case, you should use the inverting output of the comparator and also reconfigure the amplifier/shifter for inverting operation. **Figure 2** shows an example of the circuit's operation. The circuit correctly measures the peak value of the applied input signal, although the input pulses are quite short and have nearly triangular tips.

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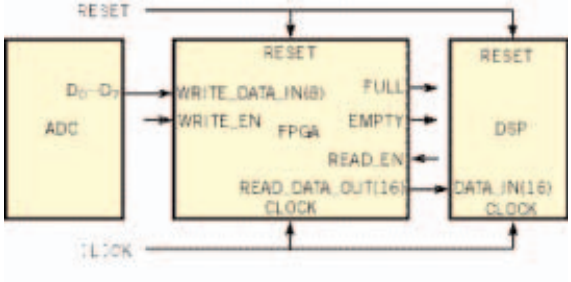
Simple FIFO provides data-width conversion

David Lou, Ghent University, Ghent, Belgium

Many designs require FIFO elastic buffers to form a bridge between subsystems with different clock rates and access requirements. However, in some applications, you need FIFO buffers for data conversion. One example is the case in which you need to connect an 8-bit ADC to a 16-bit data-bus microprocessor through a FIFO buffer (**Figure 1**). Unfortunately, most currently available FIFO buffers are unsuitable for this application. This Design Idea describes how to implement a common clock (synchronous version) for an FPGA-based FIFO for data-width conversion with different-width read and write data ports. You can implement this FIFO using a Xilinx (www.xilinx.com) Spartan II Series FPGA. The method uses an on-chip DLL (delay-locked-loop) macro, distributed memories, and simple counter logic (**Figure 2**).

Figure 1



This block diagram is an example of a system using a FIFO between an ADC and a microprocessor chip.

The width of the input data of the FIFO is 8 bits; however, the width of the output data is 16 bits. You use only one common clock for both read and write actions. The trick is to use a clocked DLL, which not only minimizes clock skews, but also offers a double-frequency output clock. So, you can implement a double data rate for the input data, write_data_in. By monitoring a sample of the DLL output clock, the DLL can compensate for the delay on the routing network, efficiently eliminating the delay from the external input port to the individual clock loads within the device. Instead of using block memory, this design employs distributed memory to hold the data in FIFO. In fact, choosing block memory or distributed memory depends on how important this FIFO is in your system. If it is not critical, you may want to consider using distributed memory.

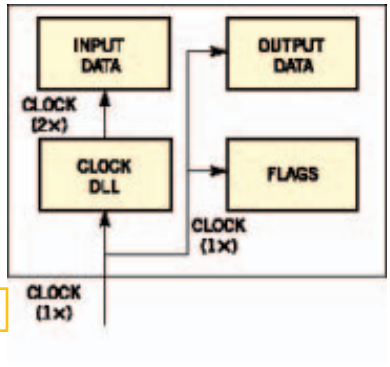


Figure 2

This FPGA uses an on-chip DLL, distributed memory, and simple counter logic.

You can put the memory anywhere you like within the FPGA. If you insist on using block memory, you can easily modify the VHDL code. You can just use some RAM macros to replace distributed memories. You can download the VHDL code for the FIFO from the Web version of this Design Idea at www.ednmag.com. FIFOs commonly use Gray-code counters or linear-feedback shift registers as read or write counters. To minimize the logic size, this design uses only two integers ranging from 0 to 7 together with a carry for the counters. When the read and write counters are equal and the carry is zero, the FIFO is empty. When the write counter plus one is equal to the read counter and the carry is one, the FIFO is full.

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Measure open-circuited cables using a multimeter

Ron Duffy, Agilent Technology, Colorado Springs, CO

You can use a multimeter with capacitance-measurement capability to measure the length of wire or cable to an open circuit. The capacitance of a pair of wires (or a wire to a shield) is directly proportional to the length of the wire. If you know the capacitance per foot of wire, then you can calculate how far it is to the open circuit. To determine the capacitance per foot, take a trip to the hardware store, use a known length of wire, and measure the capacitance with the multimeter. You must zero the multimeter's capacitance function before making any measurements. To zero the meter, select the capacitance function and separate the leads. Then, make the measurement and simply divide the total capacitance of the wire or cable by the total length to determine the capacitance per foot. Once you have this figure, and you're sure that the suspect wire or cable carries no power or signals, you can measure the capacitance, C. The wire length in feet to the open circuit is C divided by the capacitance per foot.

TABLE 1–CAPACITANCE CHARACTERISTICS OF COMMON WIRES AND CABLES

Type	Total capacitance (nF)	Total length (ft)	Capacitance per ft (pF)	Resolution (in.)	Range (ft)
Twisted pair, 18 gauge	41	1100	37.3	32.2	2682.9
16-3 SJ	0.1	5	20	6	500
Category 3 phone, PVC	21.6	1000	21.6	55.56	4629.6
Category 3 phone, plenum	22.1	1000	22.1	54.3	4524.9
14-2 NMB	5.26	250	21	5.7	475.3
16-gauge speaker	0.98	30	32.7	3.67	306.1
18-gauge speaker	0.91	30	30.3	3.96	329.7
24-gauge speaker	1.69	75	22.5	5.33	443.8
20-gauge twin lead	0.68	100	6.8	17.65	1470.6
RG-6	0.47	25	18.8	6.38	531.9
RG-8			29.5	4.07	339
RG-25			50	2.4	200
RG-59			21	5.71	476.2

The resolution depends on the range and resolution of the multimeter. The lowest range of a multimeter is usually 10 nF. The resolution in that range is 10 pF. The multimeter steps up by a factor of 10 each time it changes range. The higher ranges allow you to measure longer wires, but, as **Table 1** shows, the resolution decreases by a factor of 10 for each higher range. (Note the measurements on wires longer than 1000 ft.) All but the last three entries in **Table 1** measure the lengths of wire or cable and then calculate. The last three entries are from a coaxial-cable chart.

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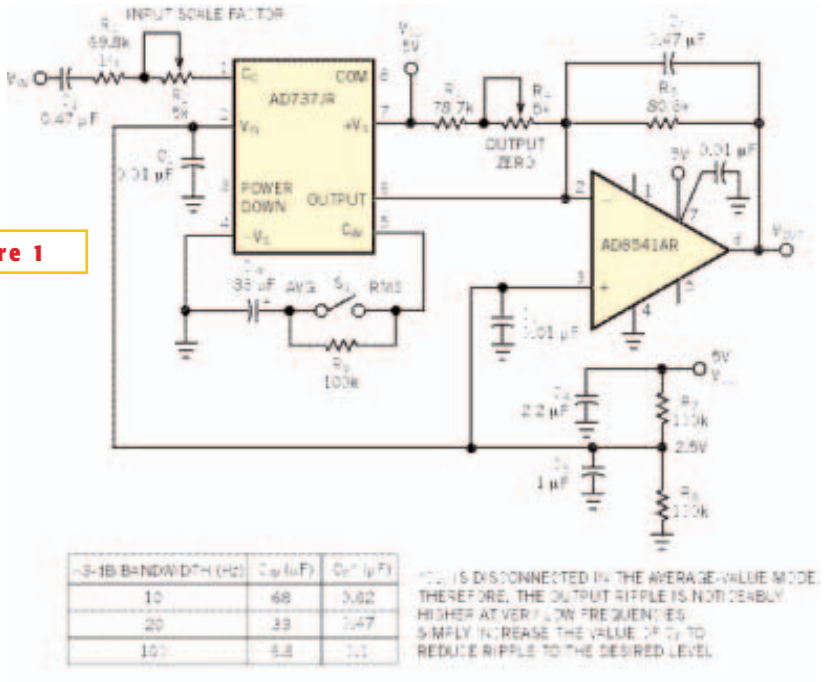
Circuit measures true-rms and average value

Charles Kitchin and Lew Counts, Analog Devices, Wilmington, MA

THE CIRCUIT IN **Figure 1** measures both the true-rms value and the rectified average value of an ac signal. This design uses two low-cost ICs in SOIC packages and consumes only 180 µA of quiescent current. Operating from a single 5V supply, the circuit has an input dynamic range of less than 30 mV to greater than 3V rms. Sine-wave accuracy is good (**Table 1**), and bandwidth is approximately 100 kHz, depending on input level. The circuit can also measure a 1V rms, crest-factor-of-five pulse train with lower than 1%-of-reading error. Most ac measurements use rectified-average-value circuits. Although these can be accurate if you calibrate their scale factor to read the rms value of one waveform, such as a sine wave, they exhibit large errors if you use them for other waveform types. In contrast, the rms value of an ac signal is the amount of dc required to produce an equivalent amount of heat in the same load. Therefore, the rms value is independent of waveform shape or duty cycle; it's often useful for measuring the power of a complex ac waveform.

Figure 1



You can measure both true-rms and average-rectified values with this circuit.

Average-responding and rms measurements have traditionally used different circuits. However, in some cases it may be useful to know both the rms and the rectified average value of an ac waveform. The ratio of rms to rectified average value is one way to determine the characteristics of a waveform without actually seeing it on an oscilloscope. For example, the rms/average-value ratio is 0.707V/0.636V or 1.11 for a 1V peak undistorted sine wave, 1.0 for a symmetrical square wave, 1.155 for a triangular wave, and 1.253 for Gaussian noise. An AD737 rms-converter IC drives an AD8541AR micropower op amp (**Figure 1**). Resistors R_7 and R_8 form a voltage divider to allow operation from a single supply voltage or battery. Capacitors C_4 and C_5 bypass any signal currents on V_{CC} or $V_{CC}/2$ to ground. The rms-converter IC has two inputs: a high-impedance ($10^{12}\Omega$) input (at Pin 2) and an 8-kΩ, wide-dynamic-range input via Pin 1. The rms converter's full-scale input range is normally 200 mV. You can greatly increase this range by adding an external resistance—in this case, resistor R_1 and trimming potentiometer R_2—between the signal input and Pin 1. This addition has the added advantage of increasing the circuit's input impedance.

TABLE 1—1-kHz SINE-WAVE ACCURACY

V_{IN}	V_{OUT} rms	V_{OUT} (rectified average value)
3	2.9999	2.6762
1	1.0027	0.8947
0.3	0.30201	0.2698
0.1	0.10082	0.09947
0.03	0.0296	0.02956

Note: V_{IN} is in ac volts rms as monitored by Keithley 191 in ac mode. Supply=5V dc.

The AD737JR measures the true-rms value when switch S_1 connects its averaging capacitor, C_{AV}, to Pin 5. The averaging capacitor performs the "mean" portion of the rms function. Removing C_{AV} by opening S_1 converts the circuit to rectified-average-value operation. Resistor R_6 allows a small leakage current to flow past the switch, keeping the capacitor charged and preventing any large surge currents from flowing into or out of C_{AV} when the switch is closed. The AD737JR drives the AD8541AR op amp with a negative-flowing output current. The op amp operates as a current-to-voltage converter and also inverts the signal, providing an output voltage that swings more positive with increasing input levels. Resistor R_5's value of 80.6 kΩ matches the effective input resistance of the AD737 ($R1+R_2+8$ kΩ), so that input/output scaling is 1-to-1. Resistor R_3 and trimming potentiometer R_4 cause a current to flow from the supply to the op amp's summing junction. This action offsets the op amp's output, such that the circuit's output is approximately 0V with no voltage applied. Note that this circuit has a maximum supply-voltage limit of 5.5V; you can extend operation to 12V by substituting an OP-196GS op amp for the AD8541AR. Circuit calibration is easy:

Adjust trimming potentiometer R_4 to mid-scale and set S_1 for rms.

1. Apply a 2.000V rms, 1-kHz sine-

wave input signal.

2. Adjust R_2 until the circuit's output voltage is 2.000V dc.
3. Reduce the input to 100 mV rms and adjust offset trimming potentiometer R_4 for a reading of 100 mV dc.
4. Repeat Step 2.

Because the dc-offset circuitry is ratiometric, it remains calibrated with modest variations in supply voltage. The measured power-supply-rejection ratio of this circuit over a 4.5 to 5.5V supply range is approximately 61 dB. The measured errors versus crest factor for a 5V supply and a 1V rms, 100-µsec pulse are: crest factor=3, error=0.67%; crest factor=5, error=0.98%; and crest factor=10, error=4.7%. Some additional points to consider: The peak rms value of a sine wave is 0.707V peak, and the peak rectified-average value is 0.636V. This ratio of 0.707V-to-0.636V is equivalent to an 11% scale-factor difference between the two measurement methods. If you want this circuit to accurately read the rms value for sine waves in the rectified-average-value mode, S_1 can be a two-pole switch. The second pole can connect a 523-kΩ, 1% resistor in parallel with R_1 to increase the scale factor in the average-value mode. However, the true rectified-average value is more useful in most cases.

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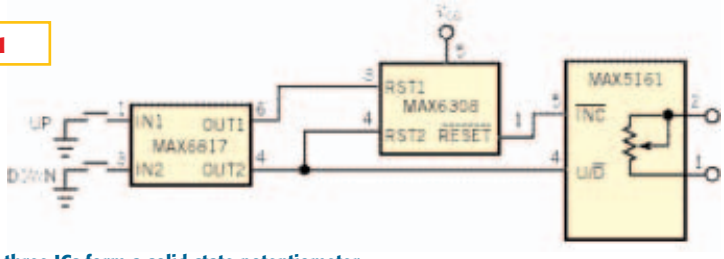
Electronic-potentiometer system has pushbutton interface

Gene Warzecha and Roger Griswold, Maxim Integrated Products, Sunnyvale, CA

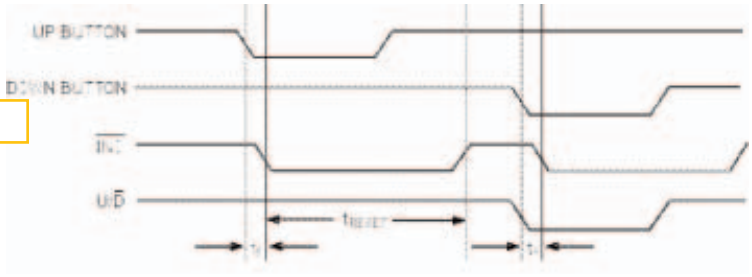
As systems grow smaller, it becomes increasingly attractive to replace mechanical potentiometers with electronic potentiometers, which are smaller and less expensive silicon equivalents. A common interface for such devices comprises a Chip-Select, Increment and, Up/$\overline{\text{Down}}$ line. CS activates the device and, on a rising edge of $\overline{\text{INC}}$ steps the wiper in a direction that the U/$\overline{\text{D}}$ pin indicates. The simple circuit of **Figure 1** uses two pushbuttons—one for up and one for down—and a few tiny silicon devices to implement a debounced, ESD-protected electronic-potentiometer system. The normally open pushbutton switches feed into the MAX6817, an ESD-protected switch debouncer in an SOT-23 package. It has internal pullup resistors on the inputs and buffered, noninverting CMOS outputs. In the absence of a switch closure, the normally open switches hold the MAX6817 outputs high. In turn, that condition ensures a low state for the active-low, push-pull output of the MAX6308, an SC70 reset device with two reset inputs that are independent of the V_{CC} pin.

Figure 1



These three ICs form a solid-state potentiometer.

Figure 2



Closing either pushbutton in Figure 1 increments the potentiometer's output in a direction that the MAX5161's U/$\overline{\text{D}}$ input indicates.

The reset device must have extra reset inputs rather than a manual-reset input, because the glitch-immunity protection of manual-reset inputs is not adequate to guarantee proper operation. The MAX-5161 is a 32-tap, linear-taper electronic potentiometer in an SOT-23 package with the standard $\overline{\text{INC}}$-U/$\overline{\text{D}}$ interface. (The electronic potentiometer pulls the CS input high internally.) Its setup requirement is 50 nsec, meaning that the U/$\overline{\text{D}}$ signal must be stable for 50 nsec preceding a rising edge at the $\overline{\text{INC}}$ pin. The transient-filtering circuitry internal to the MAX6308 introduces a delay that satisfies the setup requirement. The delay, t_r, is typically 10 to 30 µsec (**Figure 2**). $\overline{\text{INC}}$ goes high again only after the reset time-out interval expires. For the MAX6308, that interval (t_{RESET}) is factory-preset with a value as short as 1 msec.

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