Volume 40, Number 3, 2006

Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

In This Issue

40 years of Analog Dialogue 1967 2006

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ANALOG DEVICES

Editors' Notes

SPINNING THE WEB ARCHIVES

You may have noticed that the time span of our Web archive has been growing. As these words are being penned (all right, *keyed*!) the list of complete back issues in PDF goes back to Volume 11 (1977). By the end of the current year (2006), our 40th consecutive year in print, the roll call will be complete, starting with Volume 1, Number 1 (1967), and our weary scanner (and its wearier operator) can rest.

What does it all mean? First of all, the world will have available a journalistic history of products, technologies, and applications Analog Devices has been involved in, including our many successes—and yes, the few egregious failures otherwise lost in the mists of history.

Second, you will meet many of the (by now, several generations of) engineers who were part of this stream, including (perhaps too much of) ourselves—and so will get a flavor of the times.

A few cautions are necessary: These pages are reproduced without further editing, and may contain inaccuracies, especially in light of the passage of time. Since many (perhaps *most*) of the products mentioned, especially in the earliest days, are obsolete and perhaps long forgotten, even by us, the words you read in our pages may be the only surviving record of their existence. Your expectations of obtaining further information from us should properly be low.

Looking back at sampled pages, we're again impressed at their readability, but we also note that, even with the high-resolution scanning, the detail in some of the illustrations is inevitably lost. The interested reader may have to tap one's own creativity to guess at the details. Finally, because the scanning technique does not recognize characters, sufficient information has not been available to conveniently assemble a helpful index the easy way.

So with these caveats, we invite the historically interested reader to plunge into this literary stream and sample our global flow of signal processing products, technologies, and applications, as viewed from Norwood, Massachusetts.

NEW FELLOW NAMED

Frederic Boutaud, an ADI Senior Engineer, has been named to the distinguished position of Fellow during the Company's 2006 General Technical Conference (GTC), which attracted more than 1500 engineers from our design sites worldwide.

The Fellows honor is bestowed on a select group of engineers whose innovation, leadership, entrepreneurialism, and consultative skills have contributed significantly to ADI's business success. In addition, "an ADI Fellow must be a Company ambassador, bridging across organizations and demonstrating an unparalleled ability to teach and mentor others within the Company," noted Sam Fuller, Vice President of Research and Development.

With his induction, Boutaud, who has amassed an impressive 46 patents in the CPU and wireless processing fields, brings to 31 the number of Fellows at the top of the technical ladder among the Company's 3000 or so engineers worldwide.

A 25-year veteran in the field of digital IC design and architecture, Boutaud joined ADI in 1996 and assumed project lead responsibility for the digital baseband IC team, which designed the SoftFone® architecture for GSM baseband processors, "one of ADI's largest and most complex system-on-a-chip designs at the time," said Fuller. "Frederic was the IC leader, as part of the core team—from system engineering, algorithm engineering, and IC engineering disciplines—who drove architecture- and product innovation to realize this highly innovative, scalable wireless architecture."

"Frederic has been a key leader of the RF and Wireless business unit's system-on-a-chip efforts and champion for SOC design at ADI. His technical leadership and design innovations in digital ICs have contributed to ADI's accomplishments in wireless; and our analog design teams received a greater exposure to system IC techniques through his work."

Prior to joining ADI, Boutaud was an IC design engineer at Texas Instruments, where he worked with a wide range of technologies, including CPU design, oversampling converters, graphic and video processing, and low-power DSP core design. Born in Meudon (France), he graduated from École Centrale de Lyon in 1978 with an MSEE degree. He lives in Waltham, Massachusetts, and his spare-time activities include music, yoga, and biking.

Dan Sheingold [dan.sheingold@analog.com]

FEEDBACK

We love hearing from you, our faithful readers, and invite your comments on anything from the quality of our articles to the layout of our publications to the content of these editorials. Those of you who read *Analog Dialogue* online may already have noticed the new feedback box at the end of each recent article. In each box, you will find a link to Analog Diablog (http://analogdiablog.blogspot.com), where we encourage you to open a dialogue with the authors and your fellow readers. Or, as always, please feel free to send email directly to the authors, or to us, your attentive editors. As a token of our appreciation, we'll send a limited-edition 40th-anniversary pint glass to those readers who send the best suggestions for improving the *Dialogue*.

RFID

While reading about Blackfin processors in RFID readers, many of you may have realized that this is the same technology that you use every day to open doors with your company ID badge, buy groceries with your MasterCard PayPass, or pay at the pump with your Mobil Speedpass. In the age of identity theft, many of you may be concerned about the confidentiality of your personal information. Smart cards contain the same information that is encoded on the magnetic strip of a conventional credit card, but they are much more secure. Unlike magnetic strips, which can be cloned with a $20 reader—following easy-to-find instructions—smart cards allow different pieces of data to be kept distinct, where they can only be accessed by relevant applications. They use various levels of encryption and authentication, and can be combined with biometrics or keypads for additional security. The card never leaves your possession, providing additional safety and speed. More information on contactless smart-card technology, payment options, and privacy concerns can be found at http://www.ieprox.com/epayment_white_papers_payment.asp.

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Analog Dialogue

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Analog Dialogue is the free technical magazine of Analog Devices, Inc., published continuously for 40 years—starting in 1967. It discusses products, applications, technology, and techniques for analog, digital, and mixed-signal processing. It is currently published in two editions—*online*, monthly at the above URL, and quarterly *in print*, as periodic retrospective collections of articles that have appeared online. In addition to technical articles, the online edition has timely announcements, linking to data sheets of newly released and pre-release products, and "Potpourri"—a universe of links to important and rapidly proliferating sources of relevant information and activity on the Analog Devices website and elsewhere. The *Analog Dialogue* site is, in effect, a "high-pass-filtered" point of entry to the **www.analog.com** site—the virtual world of *Analog Devices*. In addition to all its current information, the *Analog Dialogue* site has archives with all recent editions, starting from Volume 11, Number 1 (1977), plus three special anniversary issues, containing useful articles extracted from earlier editions, going all the way back to Volume 1, Number 1.

If you wish to subscribe to—or receive copies of—the print edition, please go to **www.analog.com/analogdialogue** and click on **<subscribe>**. Your comments are always welcome; please send messages to **dialogue.editor@analog.com** or to these individuals: *Dan Sheingold*, Editor **[dan.sheingold@analog.com]** or *Scott Wayne*, Managing Editor and Publisher **[scott.wayne@analog.com].**

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D-Day
[The Wit and Wisdom of Dr. Leif—4]

By Barrie Gilbert [barrie.gilbert@analog.com]

For Niku Yeng, August 29, 2025 came far too quickly; but for Dr. Leif, it was just another of his Daedalus Day events. He had started this series—always convened on the last Friday of each month, with the objective of providing a forum for the youngest Originators to present their unique perspectives—shortly after the founding, in 2018, of this Analog Devices campus, in Solna, a suburb of Stockholm. Why Solna? Some believe it was ADI's decision, being quite close to customers in northern Europe and Russia. Others think it was simply Leif's hometown, and if he wished to establish a new design center there, that was good enough for the Company. It wasn't the first time.

Presentations such as D-Days are instantly available at all ADI sites worldwide and are automatically archived. It is understood that information contained in every technical presentation and review (like the ruthlessly probing Design Scrutiny) represents the lifeblood of any company at the fringes of nanotronics. To allow it to be quickly forgotten would be as irresponsible as the old practice of incinerating 'waste' materials or burying them in landfills. Recycling philosophy today is radically different from the short-minded practices pervasive at the turn of the century. Nowadays, a subscriber to the Global Used Materials Registry can readily locate over 85% of the world's recycled materials.

Usually convened in the Michael Faraday auditorium, D-Days are always well attended by the local audience; but this morning many late arrivals had to stand at the back, or on the side steps. Curiosity to watch how a 'new guy' might fare always ran high. Today it was a 'new gal,' so an extra dash of excitement stirred among the male contingent, roughly two-thirds of the total. All these auditoriums were equipped with imaginative technology for enabling and enhancing effective presentations. In planning the campus, Leif proposed that their neuromorphic simulators, impressive and inspiring showpieces as well as active partners, be located in full view at the front of the largest auditoriums.

This choice was partly dictated by their size: a *General Electro-optical Emulator* (GE°E) was bulky, due to the space required for the dense 3D webs of opto-connection fibers for the concurrent information paths. Unlike the old digital machines, a GE°E is not a mindless number cruncher. Rather, the *processes* active within it are an *inseparable*, *organic* aspect of its structure. Each *is* a GE°E, having a unique personality and its own repertoire of individually learned problem-solving tricks and philosophies. However, these are unobtrusive—users see a uniform I/O image, at least on most days ... So it is appropriate that the little ID plate, discreetly attached to the fascia by Neuromorphix Inc. shows the simulator's *personal name*, not that of the manufacturer. Here, it is the MF-GE°E, informally Michaday, more cozily Micha: one of the smaller GE°Es on campus, having some 3 million hacks. Few today can remember how this term arose. It is a *hybrid analog computing kernel*, a neuromorphic emulator ASIC, with 8192 intraconnected analog array processors, comparable to a 1-mm^2 patch of human cortex but quite incapable of autonomous 'thought' (as is the patch of cortex—although that begs the question). In circuit-simulation studies, each hack assumes the behavioral characteristics of an individual element, such as a transistor, in the user's circuit.

The GE°E designers weren't lacking a sense of humor, some of which leaked into each unique—and playful—platform, as well as into the Manual. On p. 72 we read: "Hacks are organized into groups, each representing a user's network to be simulated, by a *Matrix Attach Designator and Description Organizer*, $MAD^{D}o_{G}$, while the actual interconnections are set up by St.VITZ, the *State Variable Intertwining Zoner.* Details of the IC processes, stimuli, and all other essential data are loaded into the job-specific hacks by *Feed Units for Parameters* (FedUPS). The fast analog results are optionally delivered to a *Pre-Output Unit Processor* (POP^{UP}) for numerical purification and sanitization, using conventional matrix methods." (Purification? Sanitization!?)

"The GE°E dynamically selects heuristics and accelerators from its personally-acquired repertoire. Every job can access over 250 HURRYUPs (*Handler Unit for Redeploying Unused Paths*) which minimize solution time; 32 *Tactical Units For Technical Explication* (TUFTE) optimize how each type of simulation result is presented to maximize insight content; its *Multilingual Speech Engine*, MUSE, can accept verbal inputs from users and generate a same-language or translated response (or requested data), using its *Ubiquitous Text Transformer* (UTTER) ..." and so on.

At the bottom of a GE°E cabinet, with the comms agents, fiber-optic ports, silent power-management modules, and other riffraff, is a dusty nest of totally unimaginative binary CPUs. While tiny, fabricated in 16 nm, their lust for line power, so much more than all the rest of a GE°E combined, and so hugely out of proportion to their contribution to its function, can only be called distasteful.

Dr. Leif's breezy preamble began right on time. "Good morning, fellow travelers! Today, it's my distinct pleasure to introduce Dr. Niku Yeng, who will be describing her work concerning how an RF oscillator starts up from cold. You may perhaps be thinking this is a very simple topic, but Niku will remind us how complex the behavior of a small analog circuit can be when it is examined closely, and more thoroughly than found in most textbooks. As you know, at ADI we place a strong emphasis on the *learning experience*. It's as much a 'product' as the silicon we sell.

"I must also tell you that Niku undertook this work without any prompting. Great advances have never come from one who must be *asked*. More than a century ago, in his book *The Art of Living*, Wilfred A. Peterson said *'[A] Decision is the courageous facing of issues knowing that if they are not faced problems will remain forever unanswered. [It] is the spark that ignites Action. Until it is made, nothing happens.'* Today, our best products, and those going right back to our novel ICs of the 1970s, have come from those who *independently* selected some challenge and immersed themselves in it. They know no other way to pursue their craft than by *tracking trends* and *anticipating the future*. Then, ignoring all naysayers and using whatever subterfuges may be required, they *bring into existence* a product providing a *new function*, perhaps years ahead of any market demand. It is *this*, not mere Invention (which is invariably a fleeting *moment*) that alone may be called Innovation, the arduous *process* of turning thinking into things.

"I recall how reluctant were our valiant marketing folks to accept such a *fait accompli*! But those Pied Piper products often created whole *new families*, even *new businesses*. Many of mine are *still* alive, after decades of profitability. So please—don't hold back! Have the courage of your deepest convictions! You may make a few mistakes at first, but you must *always follow your instincts*—and seek ways to convert your clever ideas into tangible realities. Alright, well, that's quite enough from me! I'm sure you'll enjoy this talk, and benefit from Niku's exemplary work ethic and her unusual way of thinking. So now, young Yeng, it's your turn!"

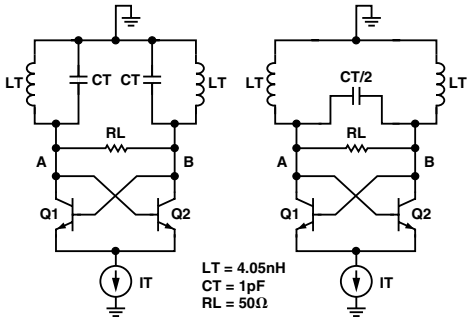
Feeling more poised than she had expected, perhaps because her faithful companion Micha was right behind her, ready to assist with the presentation, Niku began with an icebreaker.

"Thank you, Dr. Leif, and good morning, everyone! First, in case you are wondering about my mixed-up name, let me explain. My Chinese father was on business in Bangalore the day I was born in Oulu, Finland, and my Iranian mother chose my Persian name. We moved to Solna when I was about six. I must have spent my childhood in a perpetual state of perplexity because, ever since, I have always been attracted to anything enigmatic or anomalous.

"Although I'm a relative newcomer to ADI, I already consider myself fortunate in being able to tap into the wisdom of Dr. Leif, who taught me about the *Four Dees*. Let's see: Analog circuits are Durable, Diverse, and ... oh yes, Dimensional. However, he left me to find out for myself that this domain of design is at times deceptively Difficult, and demands Determination, Drive, and Dedication to deal with dozens of dastardly devious and daunting Details!"

The smiles of acknowledgement rustling around the audience assured her that she'd overcome the first barrier to acceptance.

"Oscar, as I call my oscillator, is a basic LC-tuned, differential topology using a simple BJT negative-impedance cell—an NIC. The small-signal behavior of the CMOS version will be similar; but differences appear as the oscillator approaches its eventual cyclostationary end-state, particularly for large overdrives. The fundamentals of the BJT make analysis far easier for this state.



Slide 1. Two forms of the basic Oscar.

"Micha, first slide, please. Thank you. As you see, there are two forms of the basic Oscar. Both are innocent looking, aren't they? Almost all basic analog cells have deceptively simple topologies. But, as you know, their behavior is complex and the explanations found in textbooks are frequently incorrect or, at best, superficial and inadequate for any serious design work. I must admit that, at the start of my studies, I had no idea of how many winding lanes and back alleys Oscar would lead me down. But, in the process, I have gained many rewarding and unexpected personal insights.

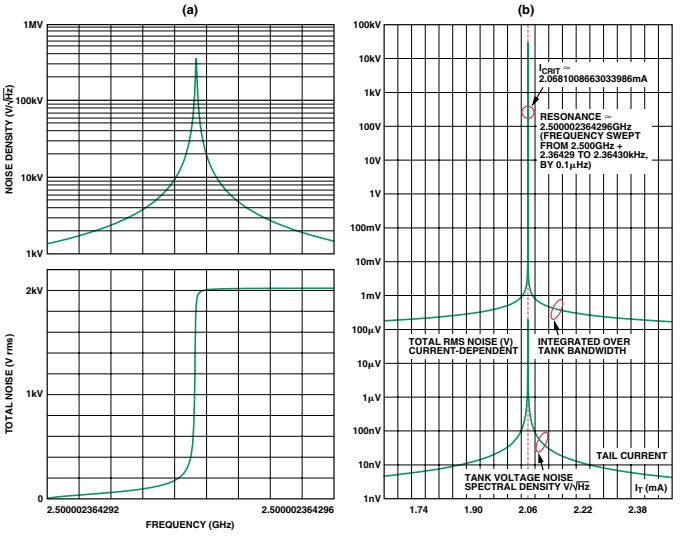
"Initially, the question was simply this: does Oscar start because of an *external disturbance*—a 'supply glitch'? Or rather, is this process driven by *internal noise*? Any oscillator that's expected to provide a spectrally clean output can't afford to be susceptible to supply hash; this is the first reason for using *fully symmetrical* circuits. The second reason is to minimize even-order harmonics. In an ideal, perfectly balanced cell, the start-up process can only be driven by *noise amplification*. But all practical circuits have mismatches so bias sensitivities are inevitable; even a minuscule mismatch could be the dominant destabilizing factor. Therefore, both noise *and* circuit mismatches can drive this process. So the question becomes: How do these two influences compare in their power to shake Oscar from his slumbers?

"Noise is analytic and can readily be quantified, with or without the help of Micha;" (Niku thought she detected a tolerant sigh behind her) "whereas the impact of device mismatches can only be assessed by making *assumptions*, about their types and their magnitudes, for a small subset of possibilities. So my objective took another turn: Could I demonstrate that noise is *invariably the dominant* driving force behind startup, even in the presence of significant mismatches? That is clearly the desired outcome, because it provides a reasonable assurance that, if nothing else, our choice of *circuit topology* is probably as good as it gets.

"In these cells, the only power source is the tail current, I_T, thus avoiding questions of supply sequencing. We can experiment in a number of ways: I_T can appear abruptly, that is, in a time much less than the tank's period—400 ps with the values shown—or slightly to much longer, and with or without mismatches added.

"Putting aside the 'glitch postulate' for the moment, let's try to understand whether noise alone could be the culprit, by ramping I_T very slowly. It makes only a little difference which form of Oscar we use—and even, in moderation, whether we include any mismatches. We must examine the *voltage noise spectral density* and *total integrated noise* at the output A, B *right at the resonant frequency*, since it has a hyperfine width of only microhertz, as this current reaches its critical value. So, Micha, please run some examples of this for us, up to and beyond I_{CRIT}. By the way, what *is* I_{CRIT}, and the resonant frequency, at this current?"

"Roughly stated, the resonance at 300 K, with R_L = 50 Ω, is at 2.500002364296 GHz for an I_{CRIT} of 2.0681008663033986 mA," piped up Micha, "and I've also found that the line width at 50% power level is about 19.22157 μHz, and that numerically the VSND and rms cross over at roughly 11 (V/Hz or V rms)."



Micha 1. VNSD and rms noise (a) vs. frequency, at $I_T = I_{CRIT}$ and (b) vs. I_T for values just above and below I_{CRIT}.

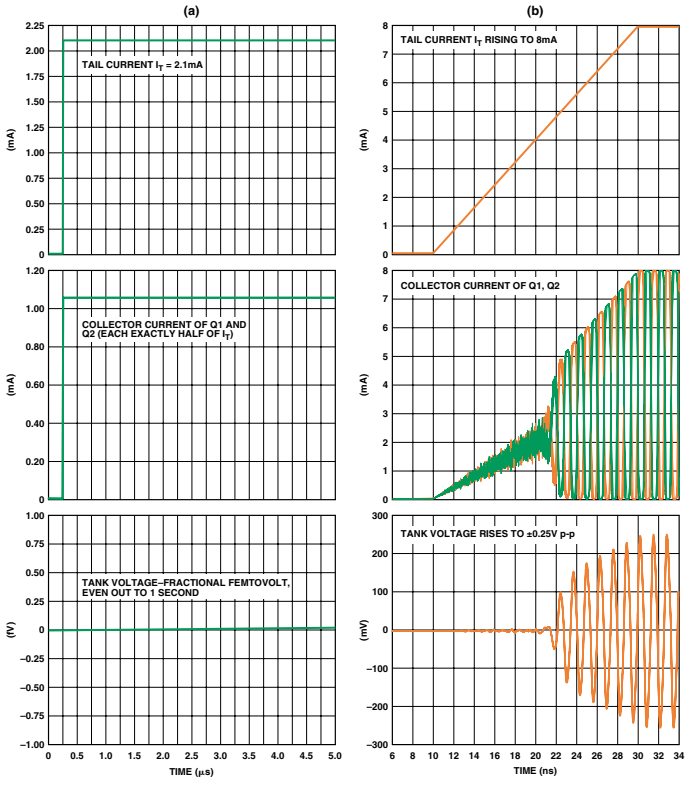
"Well, thank you, Micha, for those, um ... observations. What we should especially note here is that the basic noise sources in this circuit, which I will later identify and quantify, are amplified to extremely high values of *voltage noise spectral density*, across the nodes A-B; likewise, the total rms noise, integrated over the actual, very narrow resonance bandwidth, attains an improbably high value. But this is simply the inevitable consequence of the *closed-loop* gain briefly reaching infinity. The plot on the right shows how the VSND and rms noise vary, as the tail current is varied slightly below or above I_{CRIT}—where they again decline."

"The apparently high noise levels just indicate that the negative-impedance converter comprising Q1, Q2, and their current tail, in conjunction with the resistive component of its load, R_L = 50 Ω, exhibits an *open-loop gain* that rises to *unity* at I_{CRIT}. Thus, the *closed-loop gain* briefly becomes *infinite*. But, even at this value, an oscillation can't build up in amplitude, since if it tried to, the *nonlinearity* of the incremental r_e of each transistor, $kT/q(I_T/2)$ at balance, quickly *raises their sum*, $kT/qI_{C1} + kT/qI_{C2}$, to above the permissible maximum, $4kT/qI_{CRIT}$, during each cycle.

"Perhaps now it's apparent why the critical current is 2.086 mA. Do you see? It's because the total incremental emitter resistance is 4 × 25.85 mV/2.086 mA, which is 50 Ω, the load resistance at 300 K, while at resonance the parallel-tuned tank behaves like an open circuit. So now, Micha, show us the tank voltage in the *time domain* at precisely I_{CRIT}, following its appearance with an onset time of, say, 1 ns. First, switch off your stochastic noise sources, and then repeat the experiment with them active."

Micha demurred. "Well, there'll be nothing much to show either way because, with no noise, the fully balanced circuit will never start; and even with my stochonoise sources switched on, it will take over 14 hours to show significant signs of life, because the resonance bandwidth is only ~19 μHz. Do you have that long?"

"Ah, Micha! You're good at many things, but not talented when it comes to thinking things through! That hyperfine resonance is present *only* when the tail current is *exactly* I_{CRIT}. In rising from zero, the loop gain gradually increases; but, as it passes through lower currents, the resonance bandwidth is much higher and the loop response is proportionally faster. Alright? So now Micha, please run my time-domain experiment, but let's take the tail current just a little bit past I_{CRIT}, say, to 2.1 mA."



Micha 2. The time-domain response of the full-balanced Oscar, (a) with stochastic noise processes excluded and (b) included.

"As you see, a huge 'glitch'—in fact, the full onset of the tail current—fails to wake up a perfectly balanced Oscar, while the internal noise, amounting to rms values that readily reach many volts, and included here by Micha's complete modeling of noise *as a process in time*, evidently cause a very rapid startup. But we've a lot more to study, before reaching our final position."

A voice was raised from the back of the hall, "Why do you rely so much on simulation, when a more satisfying answer ought to come from an algebraic analysis?" asked the speaker.

"That's a fair question, although I'm not sure what constitutes a *satisfying* answer. I've learned from Dr. Leif to *simulate first*, then address the *analytical* issues later. This is not indicative of laziness, or weak-headedness, as was once so widely believed—vehemently—by a few analog diehards decades ago. In my own experience, and everyone's I expect, much precious time can be saved in trying to develop a *general* theory, by first spending a few minutes studying a number of *special cases* by simulation. This time helps us to realize both the *scope of possibilities* and the circuit's *limitations*; and we are led forward, not always to the analytical solution we may have been seeking, but to *deeper insights* than typically come out of many tedious pages of error-prone algebra. Further, the mathematics is frequently intractable in highly nonlinear circuits, even though very simple, like Oscar.

"On the other hand, in pursuing this approach (which some still adamantly call 'tinkering') it's inadmissible to accept Micha's answers without verification," (another sigh from behind) "and without any *personal understanding* of what the answers *mean*, that is, without asking *Why?*, or without *extending* one's special case to the more general case. Bursts of insight can transport you into *wild new realms of invention*; but you must *assimilate* these insights, and organize them, if you wish to become their master!"

Dr. Leif was beaming, not at all surprised that Niku's intensity was so unashamedly visible. But the audience wasn't sure what to make of this impassioned outpouring; she was "preaching to the choir." The auditorium clock had no doubts: flashing orange at the fingertip of its minute hand, it informed Niku that she had spent fifteen minutes saying little of substance. Then, standing four-square in front of her coworker, Michaday, Leif's zealous young protégé did something that amazed even him.

"I knew that I was going to have a hard time including in a one-hour talk even a small selection of all the issues comprising my recent studies, so I have asked Micha to pick up my presentation here. He will talk at normalratetimestwo, so pay close attention!"

Clever kid! thought Leif. *What a liberty*! thought the audience.

"Thank you, Nicky," began Michaday, speaking in single-time. (*Oh-ho! so it's 'Nicky' now*, gasped the stunned audience, some thinking: *He never calls me by my nickname!*). "In picking up this presentation, I will repeat it just as Dr. Yeng delivered it to me, last night, except for the time-compression factor." Then, switching to zeropitchshiftnormalratetimestwo, Michaday said, "Let's now examine the effect of element mismatches."

Absorbing technical material in double-time was no novelty to the audience; many were quite used to *triple-time*. But Niku's artful subversion had left several people feeling that this was cheating. They had come to watch the Niku girl coping with her first D-Day presentation, not listen to a clever box of wires. As the smoldering dissent spread, it grew exponentially, like Oscar's noise, and soon became palpable enough to cut with a knife.

"This next study will show some re-re-re-re-re-re ..."

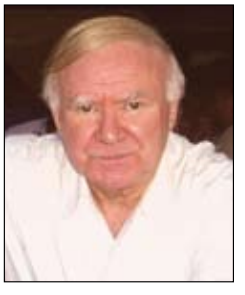
Leif had sensed the audience's unease and, using his privileged veto over "*improper use of facilities*," he interrupted Michaday's gleeful takeover with one transponder click. Before standing, he thought for a moment how best to handle this delicate impasse, not wishing to sound critical, or undermine Niku's clever ruse.

"Dr. Yeng, I'm confident that Michaday will be faithful to your material, and won't pull a HAL on you." Those aware of the old movie grinned broadly at so delightful a prospect. "But we came to hear you, and I suggest we can afford the time, this morning, to take in your material at Niku_in_single_time."

Everyone laughed, relieved to see that the respected guru was still fully in charge. Blushing like an Arizona sunset, Niku said, "I'm really very sorry, Dr. Leif. To tell the truth, I was hoping to capitalize on my discovery of how extraordinarily accomplished our GE°Es are, and to allow my good companion Micha to be in the limelight for a while. But I see that this was presumptuous of me, and I apologize to you—and everyone."

With that, she picked up where Micha was left in mid-sentence.

[*For the conclusion of Niku's talk about Oscar, and all of Micha's slides, please visit* http://www.analog.com/library/analogdialogue/leif1.html].



Barrie Gilbert, the first-appointed ADI Fellow, has "spent a lifetime in pursuit of analog excellence." Barrie was born in Bournemouth, England, in 1937. Before joining ADI, he worked with first-generation transistors at SRDE in 1954. At Mullard, Ltd., in the late '50s, he pioneered transistorized sampling oscilloscopes, and in 1964 became a leading 'scope designer at Tektronix. He spent two years as a group leader at Plessey Research Labs before joining Analog Devices in 1972, where he is now director of the Northwest Labs in Beaverton, Oregon. Barrie is a Life Fellow of the IEEE and has received numerous service awards. He has about 70 issued patents, has authored some 50 papers, is a reviewer for several professional journals, and is a co-author or co-editor of five books. In 1997, he was awarded an honorary doctorate of engineering from Oregon State University.

Fast, Versatile Blackfin® Processors Handle Advanced RFID Reader Applications

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We increasingly encounter *radio-frequency identification* (RFID) systems in our lives and work. From inventory control to fast checkouts at the supermarket, the technology is transforming many existing applications and enabling new ones. At the front end, the "signal chain" starts with small *tags* attached to the units of interest; the tags convey information in the form of a bit stream to an RFID reader that detects when tags are present in a specific area, and reads the information they carry. At the back end, a server-based system maintains and updates the tag database, generating alerts or initiating other information-based processes within the enterprise.

Most RFID readers currently employ more than one processor to satisfy application requirements. Typically, a *signal* processor is interfaced to an analog-to-digital converter (ADC) and a digital-to-analog converter (DAC). Then a *network* processor communicates with a local or remote server for information storage and retrieval. This article describes how these seemingly disparate functions—signal conversion and network connectivity—can be managed by a single processor from the Analog Devices Blackfin processor family.

We start with a brief overview of RFID technology, and discuss the present and future applications it enables. Then, focusing on RFID reader functionality, we explore the basic software components that need to run on the RFID reader—as well as the server connections. Finally, some block diagrams offer a few suggestions for system configurations.

Today's Applications and Emerging Applications

RFID technology enables many new types of applications by allowing concurrent monitoring of multiple items, without requiring a person to "touch" each one (with a hand-held barcode scanner, for example). The kinds of applications that can take advantage of this automated identification include diverse areas such as inventory control, logistics management, surveillance, and toll collection.

Today, the ubiquitous merchandise-oriented *universal product code* (UPC), a one-dimensional (1D) barcode, graces nearly everything available for public purchase. The barcode contains relevant information about the item to which it is attached, perhaps including the item's suggested retail price and/or the place and date of manufacture. 1D and 2D barcodes can also be used to track shipment details for an item.

Barcodes work well for individual items, but the workflow becomes less efficient when there are many things to scan. For example, it's impractical to open and individually scan every item on a pallet that contains hundreds or thousands of end products. But even when there are relatively few items to scan, such as groceries at the supermarket checkout, proper alignment must be established between the scanner and the label being scanned. What's more, manipulating a large item to find the barcode can be challenging.

RFID technology replaces the UPC with an EPC (Electronic Product Code), in the form of a stream of bits. At a minimum, an EPC allows the same type of information contained in a barcode to be collected automatically and accessed remotely, with minimal human intervention. In addition, an EPC can include much more information relating to unique identifying characteristics of the tagged item, even if there are many identical items. Moreover, unlike a conventional barcode, it doesn't matter in which direction the items are facing, or what the ambient lighting conditions are—the items can be still be detected and tracked. Fog, darkness, and even warehouse grime no longer matter.

Here are some more ways in which RFID systems are used today:

- In supermarket food pallets and cases, they can track the assets and allow better management of the asset pool. With the ability to write to the tag, additional information (e.g., sell-by date) can be included. In addition, automatic reordering can be implemented to keep shelves properly stocked.
- In libraries they can be used to automate the issuance and return of materials that, in earlier times, were identified by reading labels individually with a barcode scanner.
- In clothing labels they can identify the true item source. By using the tag's identification number, the item can be certified as authentic or singled out for investigation as counterfeit.
- In the pharmaceutical industry they can be used to safeguard against counterfeit supplies.
- In sports competitions they can accurately track a runner's progress during a long race.

RFID System Overview

RFID uses radio-frequency (RF) transmissions of bit streams to communicate with, identify, classify, and/or track objects. Each object has its own RFID *tag* (also known as a *transponder*). The overall system employs a *tag reader*, a subsystem that receives RF energy from each tag. The reader has embedded software that manages the interrogation, decoding, and processing of the received tag information; and it communicates with a storage system that houses a tag database and other relevant information. Figure 1 shows a conceptual diagram of an RFID system.

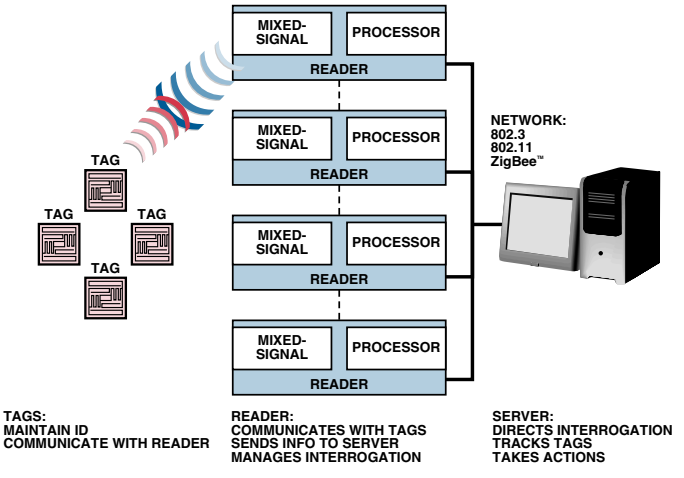

Figure 1. Simplified representation of an RFID system.

RFID Readers

The RFID *reader* provides the connectivity between individual tags and the tracking/management system. Available in a variety of form factors, it is typically small enough to be mounted on a counter, tripod, or wall. Depending on the application and operating conditions, there may be a multiplicity of readers to fully service a specific area. In a warehouse, for example, a network of readers can ensure that 100% of all pallets are queried and logged as they pass from point A to point B.

Overall, the reader provides three main functions: bidirectional communication with the tags to isolate individual ones; initial processing of received information; and connection to the server that links the information into the enterprise.

The RFID reader must deal with multiple tags within the field of interest—a very important consideration in applications with many tags within a confined spatial area (for example, multiple tagged products residing on numerous factory pallets).

The primary challenge in a multiple reader/tag scenario is that collisions will occur when many readers send out queries and multiple tags respond at the same time. The most common way to avoid this problem is to use some form of time-division multiplexing algorithm. Readers can be set to interrogate at different times, while tags can be configured to respond after a random time interval. It is clear that having the ability to implement this function in embedded software provides additional flexibility.

RFID Transponders ("Tags")

An RFID tag consists of an *integrated-circuit* (IC) chip holding unique information (such as EPC data) about the object to which the tag is affixed, an *antenna* (usually a printed circuit pattern) for receiving RF energy from the reader and for transmitting information, and some kind of *housing* that envelops the tag's components. It's worth remembering that the above term "object" can apply to any number of different things, from factory goods to animals, to people. The distance from the tag to the reader, an important system variable, is directly influenced by the tag technology. Tags can be *passive*, *active*, or *semi-active*.

Passive Tags

Passive tags are the simplest type. Powered exclusively by RF energy sent from the reader, they don't have an integrated battery, so they can be inexpensive, mechanically robust, and quite small (e.g., about the size of a thumbnail). Passive tags have a limited reader-to-tag range, however, because the received power depends on their physical proximity to the RFID reader.

The range of the link is also affected by the RF frequency chosen. Low-frequency (LF) tags commonly utilize the 125-kHz-to-135-kHz portion of the spectrum; since their range is constricted, they are mainly used for access control and animal tagging. High-frequency (HF) tags, mostly operating in the 13.56-MHz band, allow a range of a couple of feet. They are typically used for simple one-on-one object reads, such as access control, toll collection, and tracking of portable items, such as library books.

UHF tags, on the other hand, operate at frequencies from 850 MHz to 950 MHz and have a considerably longer range—10 feet or more. Moreover, because of the potentially wider bandwidth available, a reader can interrogate many of these tags at a time, as opposed to the one-on-one tag-reading process at lower frequencies. This trait helps minimize the need for multiple readers in a given zone, making UHF tags very popular in industrial applications for inventory tracking and control. However, UHF tags are unable to penetrate liquids efficiently, a major disadvantage, making them less useful for liquid-filled objects such as beverages and humans. For tracking these items, HF tags are often used instead.

In a 2004 survey[1] of passive tag suppliers, the price of UHF tags was predicted to reach 16 cents per tag in 2008, down from 57 cents in 2003—thus continuing to make tagging items a cost-effective approach to asset and inventory tracking.

Semi-Active Tags

Like passive tags, semi-active tags reflect (rather than transmit) RF energy back to the tag reader to send identification information. However, these tags also contain a battery that powers their ICs. This allows for some interesting applications, such as when a sensor is included in the tag. In addition to static identification data, each transponder can transmit real-time attributes, such as temperature, humidity, and timestamp. By using the battery only to power a simple IC and sensor—and not including a transmitter—the semi-active tag achieves a compromise between cost, size, and range.

Active Tags

Active tags go one step further, by powering both the tag IC (along with any sensors) *and* the RF transmitter, using an integrated battery. Being self-powered, they can operate over a much larger reader-to-tag range (up to 100+ meters), which also translates into allowing goods to move past the reader much faster than in the case of passive or semi-active tag systems. In addition, active tags can carry much more product information than just an EPC code.

On the downside, the battery shortens the life of an active tag and drives up both its cost and size. Active tags commonly operate in the 433-MHz and 2.4-GHz industrial-, scientific-, and medical (ISM) bands, which are available throughout most parts of the world. Consequently, as more wireless consumer products appear with 2.4-GHz-based 802.11 and Bluetooth® modules, co-existence between active tags and these devices becomes an important issue.

Software Architecture of the RFID Reader

Having described the basic functionality of an RFID reader, we now consider how to implement the reader with Blackfin-type convergent processors. The three elements of the RFID reader software architecture are: the *back-end server interface*, the *middleware*, and the *front-end tag reader algorithms*. Though distinct, all these elements of the software architecture can run concurrently on a single Blackfin processor.

Back-End Server and Connectivity

Often, the RFID reader contains a networking element—wired Ethernet (IEEE 802.3), wireless Ethernet (IEEE 802.11 a/b/g), or ZigBee™ (IEEE 802.15.4), for example—that connects single RFID-read events to a central server. The central server runs a database application, with functions that include matching, tracking, and storage. In many applications, an "alert" function is also present (the re-order trigger, for supply chain and inventory management systems, or an alert to a guard, for security applications).

Incidentally, a reader built around a high-performance embedded processor that runs μClinux (also *uClinux*) has a substantial advantage over one that doesn't when communicating with a back-end server. The presence of a robust TCP/IP stack and the availability of SQL database engines greatly reduce an otherwise major integration burden in the development process.

Middleware

The term *middleware*, as employed in RFID, has a somewhat different definition from its use in other embedded systems. In RFID terms, middleware is the software translation layer between the front-end RFID reader and the back-end enterprise system. The middleware filters the data from the reader and ensures that it is free of multiple reads or bad data. In early RFID systems, the middleware ran on the server, but the filtering of RFID data is now often performed on the reader before sending it through the enterprise's network. This degree of increased functionality is another advantage embedded processors bring to this application space.

Front End of the Reader

The system's filter- and transform-intensive signal processing, occurring in the front end of the reader, requires a device with the kind of strong signal-processing performance typically associated with Blackfin processors.

A/D and D/A Converters

Now that we have a general sense of an RFID system's components, let's focus on connectivity from the RFID reader's viewpoint. For communicating with a tag, the *mixed-signal front-end* (MxFE®) IC forms the interface of interest.

MxFE devices are general-purpose, intermediate-frequency subsystems that include A/D and D/A converters, low-noise amplifiers, mixers, AGC circuitry, and programmable filters. Output streams of I&Q data connect directly to processor parallel ports. Analog Devices MxFE IC family[2] members constitute the highest performance narrow-band receivers available, well-suited to RFID—and other—applications.

Figure 2 shows a block diagram of a typical MxFE device.

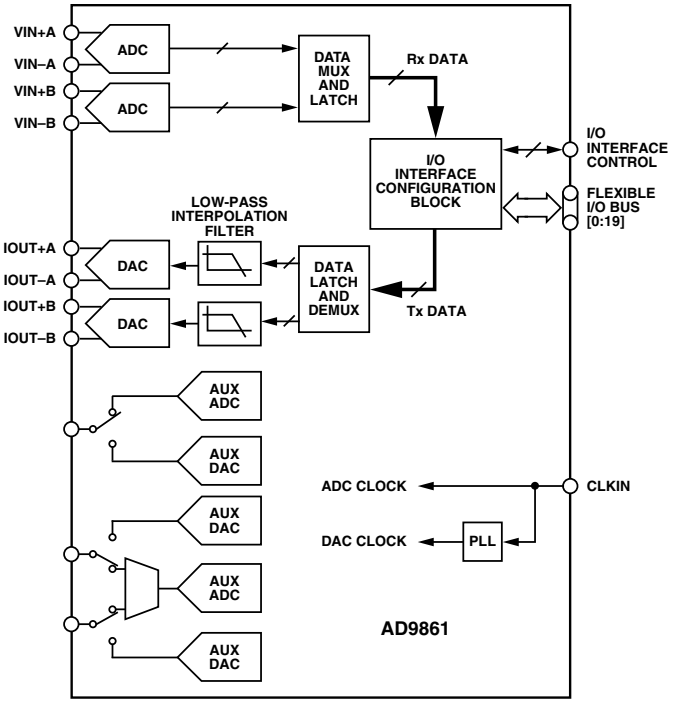

Figure 2. Block diagram of a representative MxFE IC, the AD9861.

Blackfin Processors for RFID Applications

Blackfin processors provide connectivity to both wired and wireless networks. Some processors, such as the ADSP-BF536[3] and ADSP-BF537,[4] have a 10-Base-T/100-Base-T Ethernet MAC on chip. On the wireless side, all Blackfin processors can connect directly to both 802.15.4 ZigBee and IEEE 802.11 chipsets via the SPI® and SPORT peripherals. Line-speed transfers can be obtained without consuming the entire processor bandwidth.

In addition, Blackfin processors include a *parallel peripheral interface* (PPI), which can connect directly to ADCs and DACs such as those mentioned above. Some Blackfin processors include two PPIs, which can expand system functionality even further—allowing a camera to be connected to an RFID reader, for instance. Besides RFID applications, these Blackfin features are also especially attractive for 1D and 2D barcode applications, because of Blackfin's ability to perform system control, networking, and image processing on the same device.

For RFID applications, a single PPI is often sufficient because of the way the RFID reader interrogates tags. First, the PPI is configured in *transmit* mode, and the processor sends a digital sequence to a DAC. The transmitted sequence is converted to an analog signal, which is then upconverted and sent out to excite/wake up local RFID tags, which then respond. Simultaneously, the PPI is reconfigured as a receiver in a small number of processor system clock pulses (see EE-Note 236),[5] as shown in Figure 3. In this way, a downconverted RF signal can be sampled by an ADC and brought into the Blackfin directly. In the figure, the time between each *receive* (Rx) and *transmit* (Tx) interval is measured in system clock cycles. The elapsed time allows for the transmitted signal to reach the tag and for the tag to transmit a response.

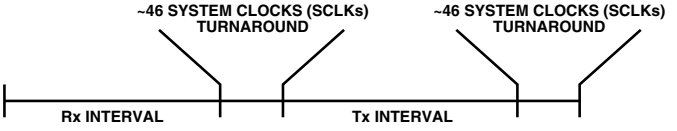

Figure 3. Illustration of Tx/Rx sequence for RFID reader with a single ADC/DAC interface.

In some RFID applications, a Blackfin processor alone can act as the server—for example, when large data stores and database manipulations are not necessary. For instance, imagine an elderly parent wearing a bracelet with a tag that could be monitored within the house. If no signs of activity were noted within a specified time interval, the monitoring agency could alert registered friends or relatives.

The software components that make up the infrastructure of a Blackfin RFID reader are available on the Blackfin.uClinux.org website. This offering includes the drivers necessary to interface to the mixed-signal, front-end IC, as well as a DMA driver that is very useful in moving data through a system. The μClinux-based network stack and SQL database engines are also available. From a system perspective, additional features, such as 802.11 Wi-Fi cards, USB thumb drives, and CompactFlash card interfaces, can very quickly be integrated with Blackfin devices. For more information, refer to http://blackfin.uclinux.org.[6]

RFID SYSTEM EXAMPLES

Wired RFID Systems

The most common application of RFID is asset management, which benefits by reduction of lost inventory, elimination of incorrect deliveries, improvement in distribution logistics, and lessening of stock-outs—as the result of being able to track a pallet's movement through the warehouse. An RFID system in a large warehouse can track a container-laden pallet's movement from the time the pallet enters the warehouse to the time it leaves. Such a system relies on fixed RFID readers placed throughout the warehouse and at points of inbound/outbound shipping.

As a means of simplifying wired infrastructure, *Power-over-Ethernet* networks (PoE) are ideal for these types of applications. IEEE 802.3a/f PoE deals with networked systems in low-power applications. A PoE system, like the one shown in Figure 4, consists of *power-sourcing equipment* (PSE) and a *powered device* (PD). The PSE provides power down the Ethernet line, while the PD (for the purpose of this discussion) constitutes the convergent networked processor and its surrounding components. PoE has a recommended maximum cable length of 100 meters, which is suitable for many embedded RFID applications, due to its relative mobility and elimination of the cost associated with installing conventional ac wiring and outlets.

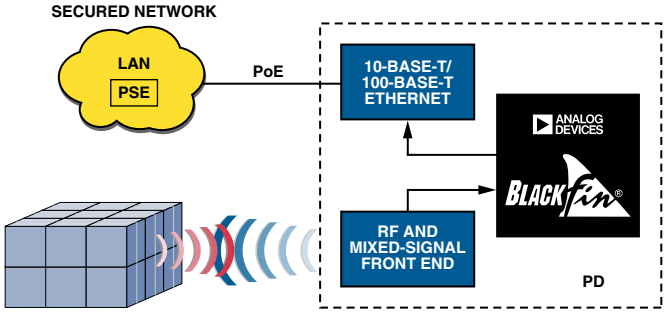

Figure 4. Example of a PoE-based RFID asset-tracking system.

A network processor supporting embedded RFID applications requires sufficient performance and integration to handle a sophisticated multilayer IP stack, in addition to the RFID acquisition software. The ADSP-BF537 Blackfin processor—which includes a 10-Base-T/100-Base-T Ethernet MAC—is a good example of such integration. For example, many Ethernet PHY devices provide a status pin with the capability to interrupt upon a status change. This feature is seamlessly integrated with Blackfin interrupt functionality to yield a robust, power-efficient system.

Wireless RFID at Low Cost

For applications such as a forklift-mounted scanner or a portable hand-held scanner, where wired or PoE operation is not possible, wireless protocols like IEEE 802.11b/g allow RFID readers to connect to a wireless *access point*, as shown in Figure 5. Blackfin processors can connect to 802.11 chipsets via either serial or parallel interfaces. In addition, because of their computational horsepower, these processors support both split-MAC and full-MAC 802.11a/b/g implementations. For example, a full-MAC might be needed for system integration of a CompactFlash 802.11b card, which interfaces through Blackfin's asynchronous memory port. A split-MAC implementation typically interfaces through a SPORT or SPI interface—the *lower MAC* resides on the wireless chipset, while the *upper MAC* is executed in Blackfin software.

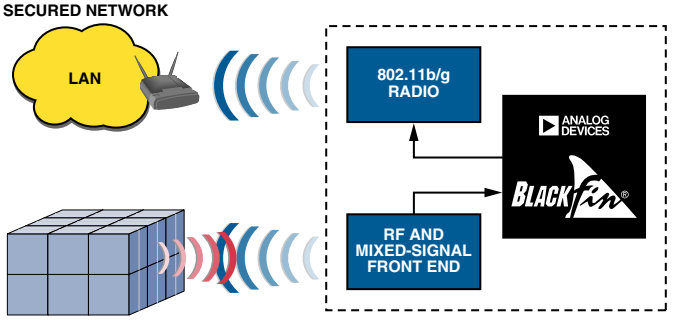

Figure 5. Example of a wireless RFID asset-tracking system.

While their stack and processing requirements can be easily handled on a single-core processor, wireless applications are testing the boundaries of performance vs. power consumption. *Managed power consumption*, offering scalable performance based on application requirements, is achievable using the dynamic power management capabilities of low-cost convergent processors such as the ADSP-BF531.[7] These dynamic power modes are designed to enable flexible performance and power arrangements for just about any networked system.

High-Performance Systems

In emerging applications, RFID technology is pairing up with additional devices such as biometric sensors or CMOS image sensors. As Figure 6 shows, in advanced applications of security authorization and personnel access control, RFID combines with image analysis to ensure that, in a secure environment, not only are there exactly *N* people in the room, but they are all "authorized personnel."

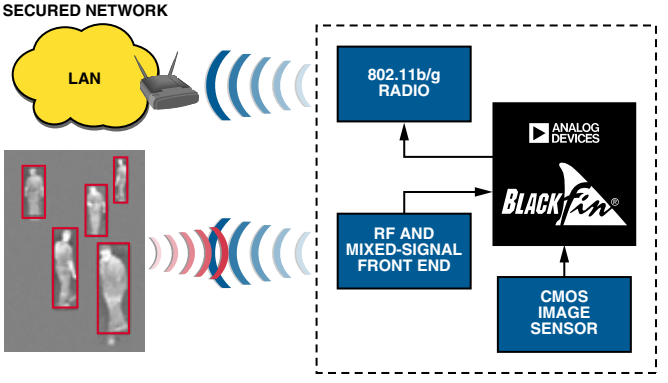

Figure 6. Example of an RFID security classification system.

The computational demands of applications of this sort are ideally suited for handling by *dual-core* convergent processors such as the ADSP-BF561.[8] An additional processor core not only effectively doubles the computational load that the device can handle; it also provides some surprising structural benefits that aren't immediately obvious.

Traditionally, a dual-core processor employs discrete, and often different, tasks running on each core. For example, one core might perform all control-related tasks—such as networking, interfacing to bulk storage, RFID acquisition, and overall flow control. This core is also where the operating system or kernel will likely reside. Meanwhile, the second core can be dedicated to the high-intensity processing functions of the application. For example, the video-processing piece of the human-recognition algorithm might run on the second core, and the resulting data packets might be passed to the first core for transmission over a network interface.

The dual-core ADSP-BF561 contains both dual high-speed L1 instruction and data memories (local to each core), and a shared L2 memory between the two cores. Each core has equal access to a wide range of peripherals—video ports, serial ports, timers, and the like. As outlined above, one core of an ADSP-BF561 can manage the RFID acquisition and networking components, while the other core can be dedicated to image classification systems that can detect, classify, and track objects in real time.

µClinux

The µClinux operating system is a popular choice for facilitating both network connectivity—which is the largest software component of the reader—and the critical requirements of

robustness and standards compliance. When reading RFID tags, it is essential to ensure that real-time requirements are met. Since the μClinux scheduler is not strictly real-time, it can be replaced with the ADEOS real-time scheduler, which safely holds off μClinux interrupts until the real-time critical processing is finished. This means that the front-end reader software can execute from the ADEOS domain in real time, while the middleware and back-end server interface can run in the traditional μClinux environment. This division gives the user hard real-time control of the application, while at the same time allowing access to all the benefits of open-source software. For more information about μClinux or ADEOS, see the Blackfin μClinux Wiki.[9]

Figure 7 shows an Analog Devices MxFE evaluation board connected to a Blackfin ADSP-BF537 STAMP development platform, which runs the MxFE driver code, μClinux operating system, and TCP/IP network stack.

CONCLUSION

As we have shown, RFID applications no longer require both a dedicated signal processor for ADC/DAC interfacing and a microcontroller for networking. A convergent processor from the Blackfin family can handle the networking and control, with plenty of performance to spare for converter interfacing and pattern matching algorithms. This, in turn, leads to lower-cost bills of material and faster time-to-market for the next wave of RFID applications.

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[3]ADI website: www.analog.com (Search) ADSP-BF536 (Go)
[4]ADI website: www.analog.com (Search) ADSP-BF537 (Go)
[5]ADI website: www.analog.com (Search) EE-236 (Go)
[6]http://blackfin.uclinux.org
[7]ADI website: www.analog.com (Search) ADSP-BF531 (Go)
[8]ADI website: www.analog.com (Search) ADSP-BF561 (Go)
[9]http://docs.blackfin.uclinux.org/doku.php

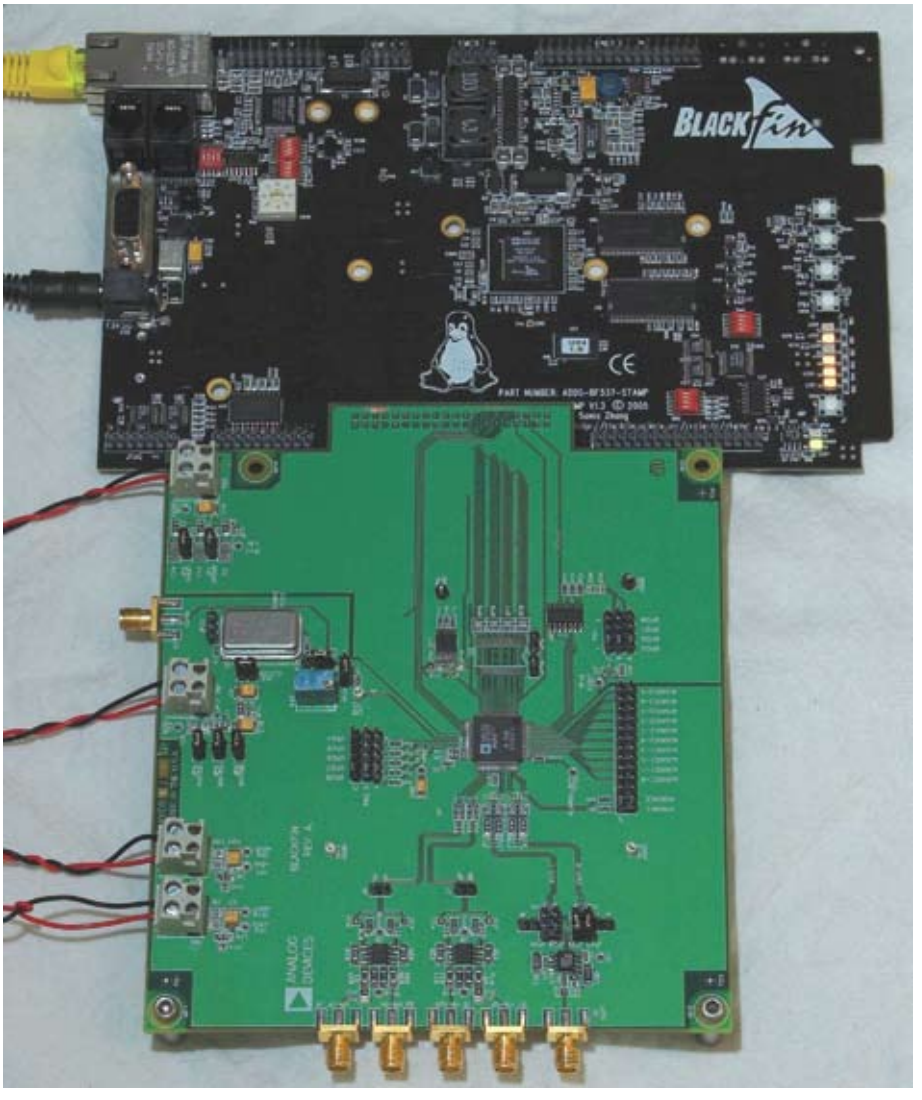

Figure 7. A Blackfin-based evaluation system for RFID reader applications.

Precision Signal-Processing and Data-Conversion ICs for PLCs Now Have More Performance at Less Power, Size, and Cost

By Albert O'Grady [albert.ogrady@analog.com]

A *programmable-logic controller* (PLC) is a compact computer-based electronic system that uses digital or analog input/output modules to control machines, processes, and other control modules. A PLC is able to receive (input) and transmit (output) various types of electrical and electronic signals and use them to control and monitor practically any kind of mechanical and/or electrical system. PLCs are classified by the number of I/O functions provided. For example, a *nano* PLC incorporates fewer than 32 I/Os, a *micro* PLC has between 32 and 128 I/Os, a *small* PLC has between 128 and 256 I/Os, and so on. A typical PLC system is outlined in Figure 1.

PLC systems comprise input modules, output modules, and input/output modules. Since many of the inputs and outputs involve real-world analog variables—while the controller is digital—PLC system hardware-design tasks focus on the requirements for digital-to-analog converters (DACs) and analog-to-digital converters (ADCs), input- and output signal-conditioning, and isolation of the electrical wiring of the input- and output modules from the controller and each other.

Resolutions of I/O modules typically range from 12 bits to 16 bits, with 0.1% accuracy over the industrial temperature range. Analog *output* voltage and current ranges include ±5 V, ±10 V, or 0 V to 5 V, 0 V to 10 V, and 4 to 20 mA or 0 to 20 mA. Settling-time requirements for DACs vary from 10 µs to 100 ms, depending on the application. Analog *input* ranges can be as small as ±10 mV, from bridge transducers, as large as ±10 V, from actuator controllers, or 4-to-20 mA currents, in industrial process-control systems. Conversion times, depending on the required accuracy and choice of ADC architecture, vary from 10 samples per second to hundreds of kilosamples per second.

Digital isolators—optocouplers or electromagnetic isolators—are used to isolate the ADCs, DACs, and signal-conditioning circuitry on the field side of the system from the controller on the digital side. If the system must also be fully isolated on the analog side, a converter would be necessary on each channel of the input or output to maximize the isolation between channels—and isolated power would be necessary, via transformers or Analog Devices *iso*Power™ technology.[1]

The *i*CMOS® Process

Many Analog Devices products used in both the input- and output sections of PLC designs benefit from *i*CMOS,[2] a new high-performance fabrication process that combines high-voltage silicon with submicron CMOS and complementary bipolar technologies.

This powerful combination allows a single chip design to mix-and-match 5-V CMOS circuits with higher-voltage 16-, 24-, or 30-V CMOS circuitry—with multiple voltage supplies feeding the same chip. With this flexibility of combining components and operating voltages, submicron *i*CMOS devices can have higher performance, a more integrated feature set, and lower power consumption—and require significantly smaller board area than previous generations of high-voltage products. The *bipolar* technology provides accurate references, excellent matching, and high stability for ADCs, DACs, and low-offset amplifiers.

Thin-film resistors, with their 12-bit initial matching, 16-bit trimmed matching, and temperature- and voltage coefficients up to 20 times better than conventional polysilicon resistors, are ideal for high-precision, high-accuracy digital-to-analog converters. On-chip thin-film fuses allow digital techniques to be used for calibration of integral nonlinearity, offset, and gain in high-precision converters.

PLC Output Module

PLC-system analog outputs—commonly used to control actuators, valves, and motors in industrial environments—employ standard analog output ranges such as ±5 V, ±10 V, 0 V to 5 V, 0 V to 10 V, 4 to 20 mA, or 0 to 20 mA. The analog output signal-chain often includes digital isolation—to isolate the controller's digital outputs from the DAC and analog signal conditioning. Converters in digitally isolated systems predominantly use 3-wire or 4-wire serial interfaces to minimize the required number of digital isolators or optocouplers.

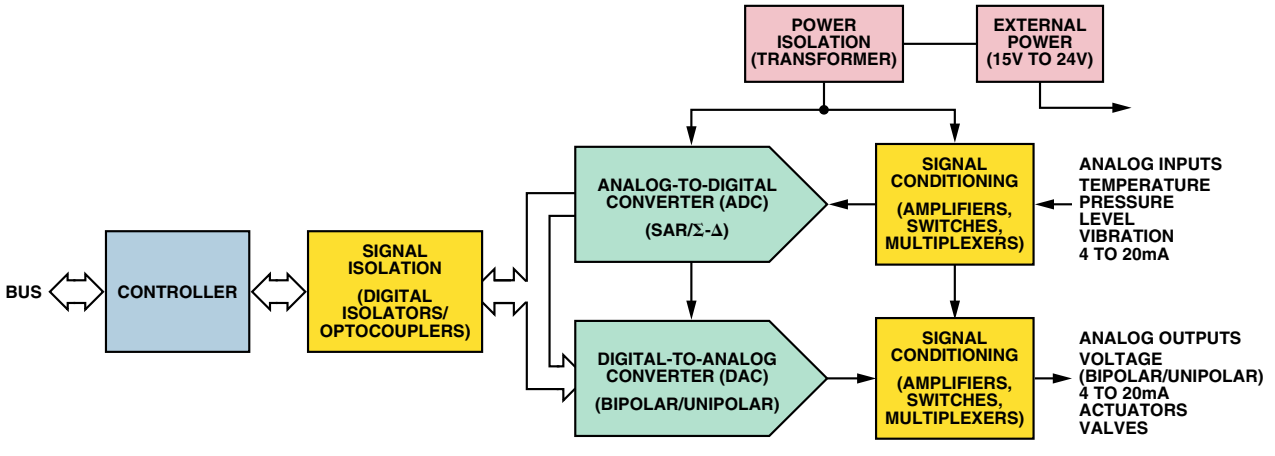

Figure 1. PLC system architecture, showing various I/O-module functions.

Two architectures are commonly used in PLC-system analog output modules: *DAC per channel* and *sample-hold per channel*. The first uses a dedicated DAC in each channel to generate its analog control voltage or current. A variety of available multiple DACs provide economy of space at low per-channel cost—but channels requiring interchannel isolation usually employ single-channel DACs. Figure 2 shows a typical DAC-per-channel configuration. The simplest DACs are low-voltage single-supply types, operating from a 2.5-V to 5.5-V supply with an output range of 0 V to V_{REF}. Their output signal may be conditioned to generate any required voltage- or current range. Bipolar-output converters, which require dual supplies, are available for use in output modules that must supply bipolar output voltage ranges.

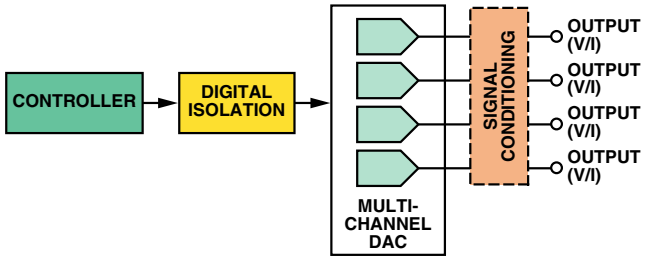

Figure 2. DAC-per-channel architecture.

Table 1, in the Appendix (page 17), shows a selection of 16-bit multichannel D/A converters suitable for implementing PLC output modules. These products offer either bipolar or unipolar output ranges, with settling times of 10 µs. Other members of these families, available with 12-bit and 14-bit resolution, are pin-compatible with the 16-bit versions—allowing a direct upgrade path from 12 bits to 16 bits with no hardware changes and minimal software changes. Most of these devices include an on-chip reference, thus offering a fully integrated output solution.

Quad D/A converters are ideally suited to nonisolated multichannel output designs where up to four different output configurations can be implemented using external signal-conditioning circuitry. For example, Figure 3 shows how the AD5664R,[3] a 16-bit quad voltage-output DAC, can deliver its specified 0-V to 5-V output range—or be connected for a variety of standard output voltage ranges, or for current-sink output, using an external quad op amp. In the bipolar-output configurations, the external output of its internal reference provides the necessary tracking offset voltage. The AD5664R operates from a single 5-V power supply, includes an internal 2.5-V, 5 ppm/°C reference, and is available in a tiny 3 mm × 3 mm LFCSP package.

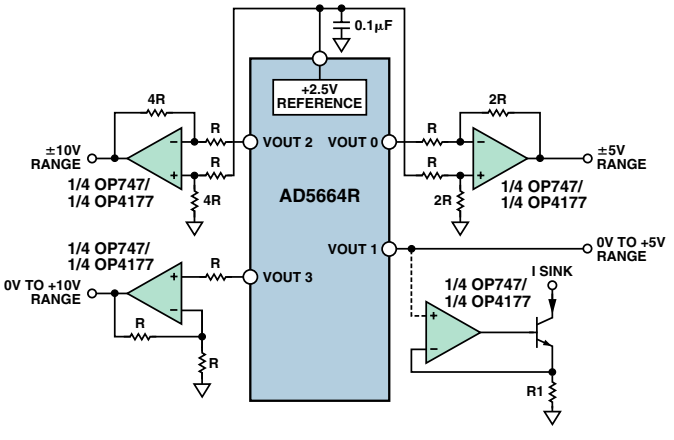

Figure 3. Implementing ±5-V, ±10-V, 0-V-to-10-V, 0-V-to-5-V, and current-sink outputs using a multichannel D/A converter.

Figure 4 shows a single-channel converter in an isolated 4-to-20-mA current-loop control circuit. The AD5662,[4] available in an SOT-23 package, is ideally suited to applications where full isolation between the analog output channels is required.

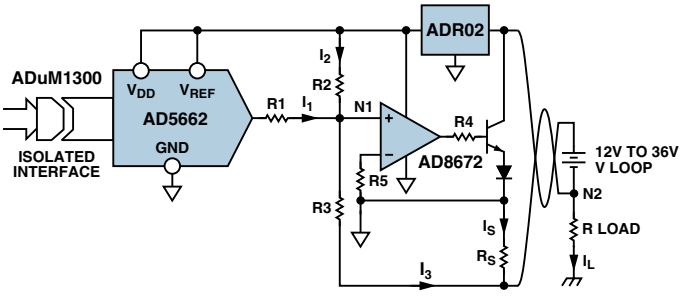

Figure 4. A 4-to-20-mA current-control circuit.

The AD5662 has a maximum output voltage span of 5 V, provided by the ADR02 voltage reference,[5] which derives a precise, regulated supply from the variable loop voltage. The 5-V DAC-output span is converted to a 4-to-20-mA current output using an operational amplifier and transistor circuit. Since the noninverting input of the op amp (N1) is a virtual ground, the op amp regulates the current, I_S, to maintain equal voltage drops across R_S and R_3, hence

$$R_S I_S = R_3 I_3$$

Current summation at N2 provides the loop current,

$$I_L = I_S + I_3 = I_3\left(\frac{R_3}{R_S} + 1\right)$$

Summing the currents at N1:

$$I_3 = I_1 + I_2 = V_{DAC}\frac{1}{R_1} + V_{REF}\frac{1}{R_2}$$

$$I_L = V_{DAC}\frac{R_3 + R_S}{R_1 R_S} + V_{REF}\frac{R_3 + R_S}{R_2 R_S}$$

The 4-mA offset component of the loop current is provided by the reference:

$$\frac{R_3 + R_S}{R_1 R_S} V_{REF}$$

The programmable 0-to-16-mA component of the loop current is provided by the DAC:

$$\frac{R_3 + R_S}{R_2 R_S} V_{DAC}$$

Sample-hold per channel

An alternative architecture uses switched capacitors and buffers as *sample-and-hold amplifiers* (SHAs) to store selected output samples from a single high-performance DAC, as shown in Figure 5. The samples are switched among the various capacitors, using an analog multiplexer. Since the *hold* accuracy of the system is determined by the droop rate of the capacitor, the channels are refreshed frequently to maintain the desired accuracy. Depending on the output requirements, the DAC can be either a low-voltage single-supply converter or a bipolar-output converter. The buffer, which may provide signal conditioning, presents high input impedance to the capacitor and offers low output impedance for driving the output load.

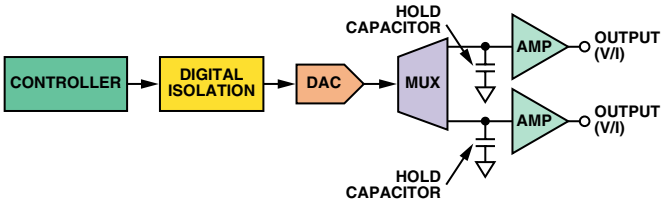

Figure 5. Single-DAC architecture.

Table 2 shows a selection of single-channel, 16-bit D/A converters, with full-scale settling times from 4 μs to 10 μs. Well-suited to sample-and-hold output architectures, they are provided in small-form-factor surface-mount packages.

Switches and Multiplexers

For sample-and-hold and other data-acquisition applications, where low-capacitance switching with low glitch and low charge injection are called for, the ADG12xx/ADG13xx family of ±15-V switches and multiplexers, designed on *i*CMOS, are useful.

For other applications, where very low on resistance is necessary, the ADG1408 and ADG1409 ±15-V multiplexers offer a maximum of 9 Ω over the full signal range. Besides having low R_{ON}, their excellent on-resistance *flatness* (with voltage level) makes them an ideal solution in applications where low distortion is essential for reliable, predictable circuit performance.

Table 3 tabulates capacitance, charge injection, and R_{ON} for a selection of *i*CMOS switches and multiplexers. They are compared with a popular earlier type, the ADG508/ADG509.

Galvanic Isolation for Power and Digital Signals

In PLCs, process control, data acquisition, and control systems, digital signals are transmitted from a variety of sensors to a central controller for processing and analysis. To maintain safe voltages at the user interface, and to prevent transients from being transmitted from the sources, galvanic isolation is required. The most commonly used isolation devices are optocouplers, transformer-based isolators, and capacitively coupled isolators.

The popular *optocouplers* contain light-emitting diodes (LEDs)—to convert electrical signals to corresponding light intensities—and photodetectors to convert the light back to electrical signals. In general, their LEDs are characterized by low conversion efficiencies—and the photodetectors by slow response; overall, optocouplers tend to have limited life, as well as excessive performance variation over temperature, speed, and power consumption. They are generally limited to 1- or 2-channel configurations and require external components to configure complete functions.

A new approach to isolation has been developed at Analog Devices, combining chip-scale transformer technology with integrated CMOS inputs and outputs. These *i*Coupler® devices are easy to use—with smaller size, lower cost, and lower power requirements than optocouplers. Available in a wide variety of channel configurations and performance levels, with standard CMOS interfaces, *i*Couplers require no external components—and provide high performance and stability over temperature, supply voltage, and life. A typical *i*Coupler isolation IC, the ADuM2400 quad isolator,[6] with its interfaces and coupling transformers, is shown in Figure 6.

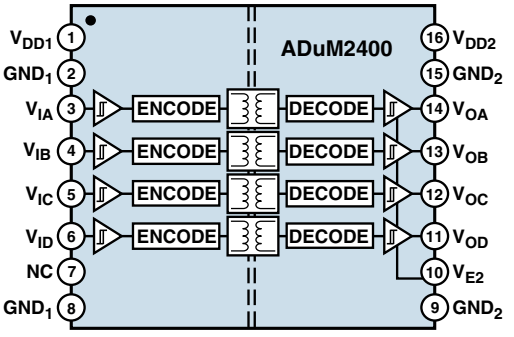

Figure 6. Block diagram of ADuM2400 quad isolator.

*i*Couplers have two- to four-times faster data rates and timing specifications than commonly used high-speed optocouplers—and they operate with as little as 1/50 the power of optocouplers, with correspondingly less heat dissipation, improved reliability, and reduced cost. Table 4 shows available channel configuration options.

Providing isolated power from the system side to the field side in fully isolated systems is another challenge that has an emerging solution. Traditional techniques employed in transferring power across an isolation barrier include either a separate, relatively large, expensive dc-to-dc converter, or a difficult-to-design-and-interface discrete assembly. A newer and better approach, currently available to supply up to 50 mW, is to use a complete, fully integrated isolation solution involving signal- and power transfer across an isolation barrier using microtransformers. The ADuM524x *iso*Power family of products provides isolation up to 5 kV, for both signal and power, within a single component—eliminating the need for a separate, isolated power supply and significantly reducing the total isolation system cost, board area requirements, and design time. A typical device is shown in Figure 7. All products have achieved UL, CSA, and VDE safety approval.

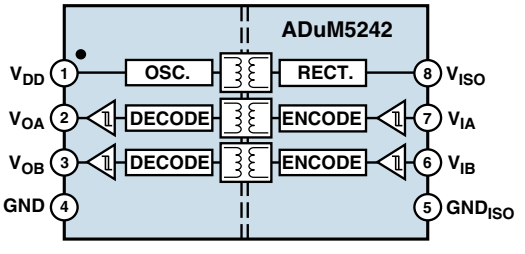

Figure 7. Block diagram of ADuM5242[7] dual-channel isolator with integrated dc-to-dc converter (0-/2-channel directionality).

PLC Input Module

The choice of architecture and input-module products for PLC systems depends upon the input signal levels that need to be monitored. The signals, from various types of sensors and process-control variables to be monitored, can involve input signal ranges from to ±10 mV to ±10 V. The table below indicates some of the sources and their typical input-range requirements.

A variety of A/D converter types can be used for industrial and PLC applications—including successive-approximation (SAR), flash/parallel, integrating (including sigma-delta), and ramp/counting. The selection of an ADC for a particular application is primarily dictated by the input-signal range required by the input transducer—as well as the required accuracy, signal-frequency content, maximum signal level, and dynamic range. The most widely used architectures are successive-approximation and sigma-delta.

Successive-approximation ADCs provide resolutions from 12 bits to 18 bits with high throughput rates; they are ideally suited to multichannel multiplexed applications, where a number of input channels need to be monitored at reasonably high sample rates.

Sigma-delta architectures provide resolutions from 16 bits to 24 bits. They employ high oversampling rates and digital filtering to achieve their high resolution and accuracy—but at lower throughput rates than are achieved by SAR types. Sigma-delta architectures generally incorporate programmable-gain amplifiers (PGAs) on the front end; in converter-per-channel applications, this allows a direct interface—without signal conditioning—between the sensor and the ADC.

A key requirement when measuring low-level signals from thermocouples, strain gages, and bridge-type pressure sensors is the ability to perform a differential measurement to reject common-mode interference and provide a more stable reading in the presence of noise. In industrial applications, for example, differential inputs are used to cancel common-mode noise or interference from motors, ac power lines, or noise sources that inject noise into the analog inputs of the A/D converter.

Single-ended inputs, which are lower in cost, provide twice the number of input channels for the same number of input pins, since they require only one analog input per channel and are all referenced to the same ground point. They are mainly used in applications with high signal levels, low noise, and a stable common ground.

Figure 8 shows many of the elements that could be included in a discrete implementation of an isolated PLC input module—including excitation, input signal conditioning, a fault-protected multiplexer to handle a number of input signals, a programmable-gain amplifier, and an A/D converter. Many of these functions, formerly assembled with discrete collections of ICs and passive elements, are now available—fully integrated and characterized—in A/D-converter and analog front-end ICs.

Analog Input-Module Low-Level Signal Ranges

Input	±10 mV	±25 mV	±50 mV	±80 mV	±0.25 V	±0.5 V	±1 V	±1.25 V	±2.5 V	±5 V	±10 V
Strain Gage	✔										
Thermocouple											
K				✔							
T		✔									
J				✔							
N			✔								
E				✔							
R		✔									
S		✔									
B		✔									
U			✔								
L				✔							
Resistor											
48 Ω				✔							
150 Ω					✔						
300 Ω						✔					
600 Ω							✔				
6 kΩ											✔
RTD											
Cu10 Std			✔								
Ni St/Kl						Ni100	Ni120/200		Ni500	Ni1000	
Pt Std							Pt100		Pt200	Pt500	Pt1000
Air Conditioning					Pt100	Pt200		Pt500	Pt1000		

For example, the AD761x (16-bit) and AD763x (18-bit) families of *i*CMOS PulSAR® ADCs with internal references provide programmable input voltage ranges (0 V to 5 V, 0 V to 10 V, ±5 V, and ±10 V) that allow the designer to change inputs on-the-fly. For these devices, all switching is done via internal registers, eliminating data latency and providing improved channel switching speeds. Table 5 shows a selection of 16-bit/18-bit PulSAR ADCs ideally suited to PLC applications.

Another, more highly integrated example is the AD7792/AD7793/AD7794/AD7795/AD7798/AD7799 family of sigma-delta ADCs. Besides their ultralow noise (40 nV) and low power requirement (400 μA), the family also provides features such as an on-chip PGA (gains from 1 to 128), voltage reference, sensor-excitation current sources, and clock—in a small TSSOP package. The combination of very low noise and low power makes these devices ideal for applications requiring high-accuracy measurements.

These ADCs can be connected directly to the sensor interface in many applications, including PLCs, temperature measurement, weigh scales, pressure- and flow measurement, and general measurement equipment. Their update rate is programmable from 4 Hz to 500 Hz, and they offer simultaneous rejection of both 50-Hz and 60-Hz signals at selected update rates. Table 6 shows features and functions offered by the AD779x family of converters.

Figure 9 shows a typical configuration using the AD7794/AD7795 to measure input signals from bridge transducers and resistance-based temperature sensors.

When high-precision fault-protected analog measurement with voltage-input capability up to ±10 V is needed in PLCs and industrial I/O, and where high throughput for multiple channels is important, the AD7732 (two fully differential input channels), AD7734 (four single-ended input channels), and AD7738 (four fully differential or eight single-ended input channels) are ideal.

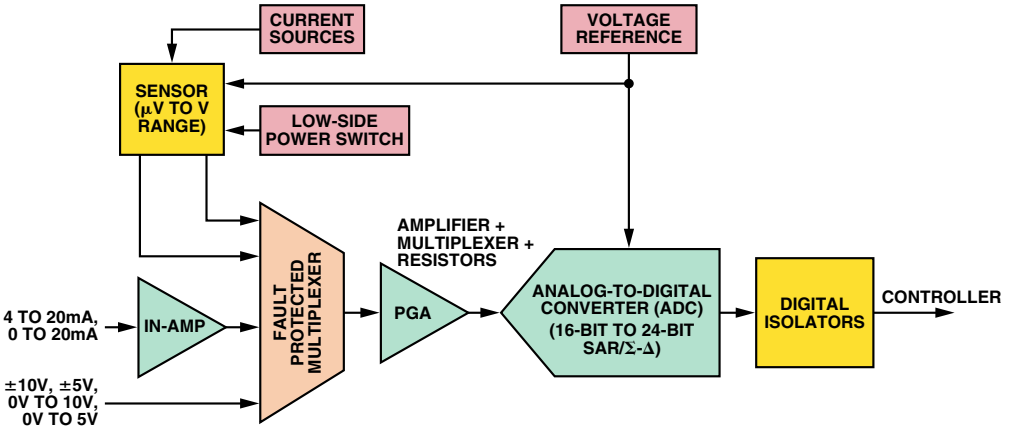

Figure 8. Functions embodied in a typical discrete PLC input module.

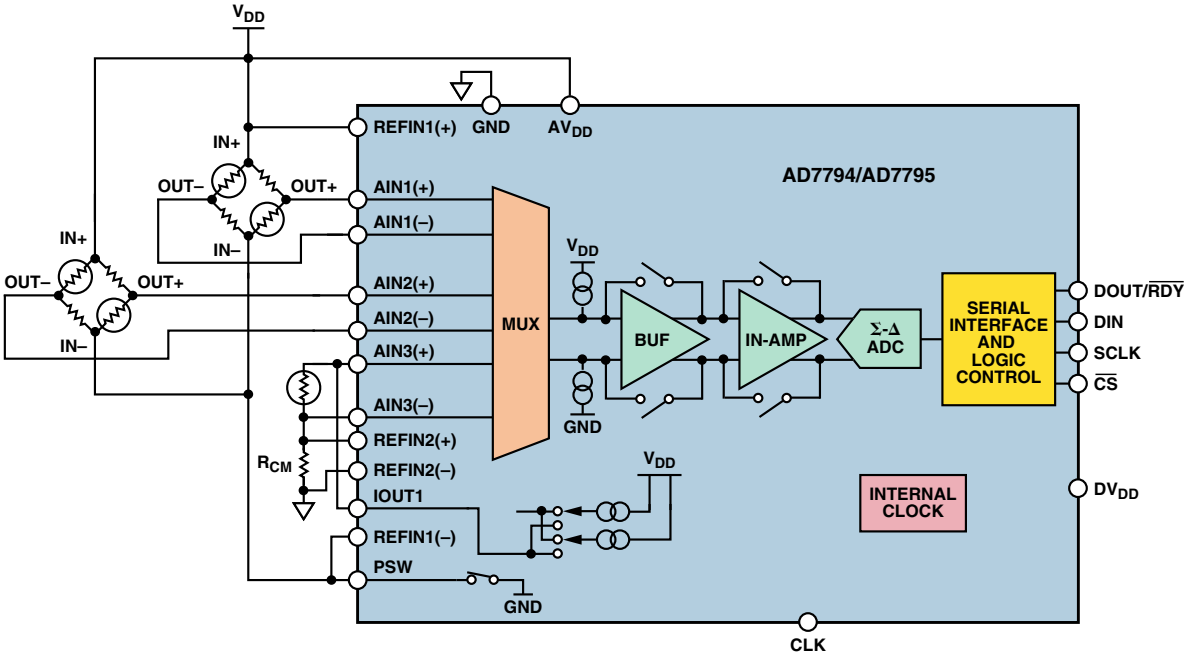

Figure 9. Low-level measurement using AD7794/AD7795.

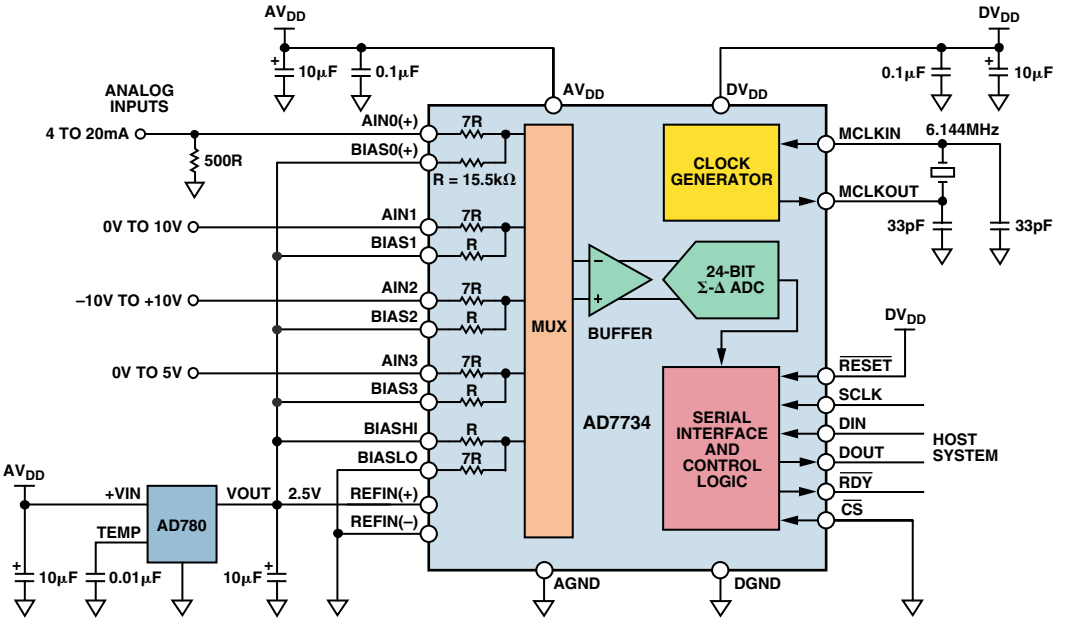

Figure 10. High-voltage signal acquisition using the AD7734.

Figure 10 shows a typical configuration using the AD7734 to measure high level signals typically seen in PLC- and process-control applications. The analog front-end features four single-ended input channels with unipolar or true-bipolar input ranges to ±10 V, while operating from a single 5-V analog supply. Analog input overvoltage of ±16.5 V can be accepted without degrading the performance of adjacent channels, and the device can signal over-range and under-range voltages.

Voltage References

Stable, accurate, low-noise standalone references are important in some PLC applications. Table 7 outlines a wide selection of high-performance voltage references, ranging from high-accuracy, low-noise ICs for high-end industrial applications to general-purpose, low-power devices for hand-held battery-powered applications.

Amplifiers (Instrumentation and Operational)

Instrumentation amplifiers (in-amps) measure the difference between two input voltages (while rejecting any signals that are common to both inputs), apply a fixed or programmable gain, and provide a single-ended output, biased by the voltage applied at a *reference* terminal. Since inadequate *common-mode rejection* (CMR) can cause large, time-varying errors that are difficult to remove at the output, modern in-amps provide from 80 dB to 120 dB of dc- and low-frequency CMR. In-amps provide an important function in extracting small signals from transducers and other signal sources in data-acquisition, PLC, and industrial process-control applications. As with all dc amplifiers, an in-amp must have low dc offset voltage and drift.

The AD8220[8] is an example of a highly versatile instrumentation amplifier that can be used in a variety of applications, such as signal conditioning between sensors—such as strain gages—and ADCs, in medical applications, programmable logic controllers, data-acquisition cards, and analog I/O cards. It offers resistor-programmable gains from 1 to 1000, with 80-dB CMR, 1-mV offset, and 10-µV/°C drift.

Operational amplifiers are the "workhorses" of analog circuitry, and Analog Devices offers one of the largest op-amp stables available in the marketplace today. Innovative design, combined with recent IC process developments, such as the high-voltage *i*CMOS and high-performance *i*Polar™, have made possible the introduction of devices for the industrial marketplace with dramatically improved performance and far greater functionality—in one-quarter the board space of older process geometries. Table 8 and Table 9, respectively, outline single- and multichannel amplifier products that are frequently used in PLC applications. They easily handle the high supply voltages generally required to support a ±10-V output range, and they feature low offset voltage and low supply current—and are housed in a small package.

CONCLUSION

Industrial system designers of PLCs continue to push for higher performance and functionality on a shrinking budget with ever shrinking board area. To provide integrated circuits capable of meeting these stringent requirements and compete for *all* significant sockets in the signal chain, Analog Devices has developed important new manufacturing processes. The *i*CMOS process technology combines high-voltage silicon with submicron CMOS and complementary bipolar technologies to make possible analog ICs capable of 30-V operation (required for many industrial applications) in a smaller footprint with higher performance at lower cost. *i*Coupler isolation technology, based on chip-scale transformers—rather than the LEDs and photodiodes—can be integrated with CMOS semiconductor functions for low-cost isolation. The *i*Polar trench-isolation process permits supply voltages of up to ±18 V and offers a dramatic improvement in performance over conventional bipolar amplifiers, while reducing power consumption by half—and package size by as much as 75%. These technologies meet present needs well—and face a brilliant future.

REFERENCES—VALID AS OF NOVEMBER 2006

[1] http://www.analog.com/Analog_Root/static/pdf/isolators/techDocs/isoPower.pdf
[2] ADI website: www.analog.com (Search) *i*CMOS (Go)
[3] ADI website: www.analog.com (Search) AD5664R (Go)
[4] ADI website: www.analog.com (Search) AD5662 (Go)
[5] ADI website: www.analog.com (Search) ADR02 (Go)
[6] ADI website: www.analog.com (Search) ADuM2400 (Go)
[7] ADI website: www.analog.com (Search) ADuM5242 (Go)
[8] ADI website: www.analog.com (Search) AD8220 (Go)

APPENDIX: SELECTION TABLES

Updated versions of these tables can be found at *www.analog.com*.
Click on the appropriate product listings.

Table 1. 16-Bit Multichannel D/A Converters Targeted at DAC-Per-Channel Applications

Part Number	Number of Channels	Output Range	INL (LSB)	Reference	Settling Time (µs)	Package
AD5668	8	Unipolar	8	Int/ext	6	TSSOP
AD5678	4 × 12-bit 4 × 16-bit	Unipolar	8	Int/ext	6	TSSOP
AD5544	4	Unipolar/bipolar	4	Ext	2	TSSOP
AD5664	4	Unipolar	6	Ext	4	LFCSP, MSOP
AD5664R	4	Unipolar	8	Int/ext	4	LFCSP, MSOP
AD5666	4	Unipolar	32	Int/ext	6	TSSOP
AD5764	4	Bipolar	—	Int/ext	8	TQFP
AD5663	2	Unipolar	6	Ext	4	LFCSP, MSOP
AD5663R	2	Unipolar	8	Int/ext	4	LFCSP, MSOP

Table 2. Single-Channel 16-Bit D/A Converters

Part Number	Output Range	INL (LSB)	Reference	Settling Time (µs)	Package
AD5570	Bipolar	0.4	Ext	12	SSOP
AD5660	Unipolar	16	Int	8	MSOP, SOT-23
AD5662	Unipolar	8	Ext	8	MSOP, SOT-23
AD5062	Unipolar	0.5	Ext	4	SOT-23
AD5063	Unipolar/bipolar	1	Ext	4	MSOP
AD5060	Unipolar	1	Ext	4	SOT-23
AD5061	Unipolar	0.5	Ext	4	SOT-23

Table 3. *i*CMOS Switches and Multiplexers

Part Number	Function	Capacitance/ Channel (pF)	Q_{INJ} (pC)	R_{ON} (Ω)
ADG1211	Quad SPST switch	1.2	–0.3	260
ADG1212	Quad SPST switch	1.2	–0.3	260
ADG1213	Quad SPST switch	1.2	–0.3	260
ADG1236	Dual SPST switch	1.6	–1	260
ADG1204	4:1 mux	4.2	–0.7	260
ADG1208	8:1 mux	7	0.4	270
ADG1209	Dual 4:1 mux	4.5	0.4	270
ADG1308	8:1 mux	15	2	300
ADG1309	Dual 4:1 mux	10	2	300
ADG1408	8:1 mux	90	20	9
ADG1409	Dual 4:1 mux	45	20	9
ADG508F	8:1 mux	50	4	400
ADG509F	Dual 4:1 mux	25	4	400

Table 4. Digital Isolators

Part Number	Number of Channels	Channel Configuration (Forward/Reverse Channels)	Isolation Rating (kV rms)
ADuM1100	1	1/0	2.5
ADuM1200	2	2/0	2.5
ADuM1201	2	1/1	2.5
ADuM1300	3	3/0	2.5
ADuM1301	3	2/1	2.5
ADuM1400	4	4/0	2.5
ADuM1401	4	3/1	2.5
ADuM1402	4	2/2	2.5
ADuM2400	4	4/0	5
ADuM2401	4	3/1	5
ADuM2402	4	2/2	5

Table 5. Programmable-Input-Range 16-Bit/18-Bit PulSAR ADCs

Part Number	Resolution (Bits)	Data Bus Interface	Sample Rate (kSPS)	Supply Range (V)	Maximum Operating Power (mW)	Reference (V)	Analog Input Range Reference (Int/Ext)	Pin Count and Package
AD7610	16	Serial/ parallel	250	±16.5	38	5	0 V to +10 V, ±5 V, ±10 V	48-lead LQFP, LFCSP
AD7612	16	Serial/ parallel	750	±16.5	100	5	0 V to +10 V, ±5 V, ±10 V	48-lead LQFP, LFCSP
AD7631	18	Serial/ parallel	250	±16.5	100	5	0 V to +10 V, ±5 V, ±10 V	48-lead LQFP, LFCSP
AD7634	18	Serial/ parallel	670	±16.5	100	5	±10 V uni, ±20 V bi, diff	48-lead LQFP, LFCSP

Table 6. Functionality Offered by the AD779x Σ-Δ ADC Family

Part Number	Resolution	Channels	PGA	Reference	Current Sources	Temperature Sensor	Reference Detect	Sensor Detect
AD7792	16	3	Yes	Yes	Yes	Yes	No	Yes
AD7793	24	3	Yes	Yes	Yes	Yes	No	Yes
AD7794	24	6	Yes	Yes	Yes	Yes	Yes	Yes
AD7795	16	6	Yes	Yes	Yes	Yes	Yes	Yes
AD7798	16	3	Yes	No	No	No	Yes	Yes
AD7799	24	3	Yes	No	No	No	Yes	Yes

Table 7. Voltage References

Reference Family	Characteristics	Voltage Output Options (V)	Key Specifications
ADR43x	XFET® series reference	2.048, 2.5, 3.0, 4.096, 4.5, 5	±0.04% accuracy 3.5 mV p-p (0.1 Hz to 10 Hz)
ADR0x	Ultracompact, high precision	2.5, 3.0, 5, 10	±0.1% accuracy low drift: SOIC: 3 ppm/°C TSOT-23 and SC70: 9 ppm/°C
ADR39x	High precision, micropower series reference	2.048, 2.5, 4.096, 5	±6 mV accuracy low power: 120 µA max 5 mV p-p (0.1 Hz to 10 Hz)
ADR5xx	High performance shunt references	1.0, 1.2, 2.048, 2.5, 3.0, 4.096, 5	±0.2% accuracy tempco: 40 ppm/°C
ADR36x	High precision, low power series reference	2.048, 2.5, 3.0, 3.3, 4.096, 5	±3 mV initial accuracy quiescent current: ≤ 190 µA 8.25 mV p-p (0.1 Hz to 10 Hz)
ADR44x	Ultralow noise, LDO XFET series reference	2.048, 2.5, 3.0, 4.096, 5	±0.04% accuracy 1.0 mV p-p (0.1 Hz to 10 Hz) tempco: B-Grade: 3 ppm/°C

Table 8. Single-Channel Amplifiers Frequently Used in PLC and Analog Signal-Conditioning Applications

Product	Power Supply (V)	Offset (mV)	Slew Rate (V/µs)	I_{SUPPLY} (mA/Amplifier)	Package
AD8671	36	0.075	4	3	MSOP
AD8675	36	0.050	1	3	MSOP
AD8677	36	0.075	0.6	1.2	TSOT
OP1177	36	0.060	0.7	0.4	MSOP
OP07D	36	0.15	0.2	0.4	SOT-23
AD820	36	1	3	0.8	MSOP
AD8641	36	0.5	5	0.7	SC70
OP07	36	0.075	0.2	0.2	SOIC

Table 9. Multichannel High-Supply-Voltage Amplifiers Frequently Used in PLC and Analog Signal-Conditioning Applications

Product	Power Supply (V)	Offset (mV)	Slew Rate (V/µs)	I_{SUPPLY} (mA/Amplifier)	Package
ADA4004-4	36	0.100	2.7	1.7	LFCSP
AD8674	36	0.060	0.7	0.4	TSSOP
AD8513	36	0.4	3	0.8	TSSOP
AD8625	26	0.5	5	0.7	TSSOP
OP482	36	3	8.5	0.25	SOIC
OP4177	36	0.06	0.7	0.4	TSSOP
AD824	36	0.4	3	0.8	SOIC
AD8643	26	0.5	5	0.7	TSSOP
OP747	36	0.1	0.2	0.3	TSSOP

Wideband A/D Converter Front-End Design Considerations

When to Use a Double Transformer Configuration

By Rob Reeder [rob.reeder@analog.com]
Ramya Ramachandran

BACKGROUND

Transformers are used for isolation and to convert signals from single-ended to differential. A factor often overlooked when using transformers in the front-end circuitry of high-speed A/D converters is that they are never ideal. With sinusoidal input signals, any imbalance introduced by the transformer delivers an imperfect sinusoidal wave to the input of the ADC, and results in overall data-conversion performance worse than the ADC could otherwise provide. We consider here the effects of input imbalances on ADC performance and provide examples of circuitry to achieve improved results.

About Transformers

The wide variety of available models from many manufacturers can make transformer selection a confusing process. The challenge is compounded by the differing approaches taken by suppliers in specifying performance; they often differ in the choice and definitions of the parameters they specify.

Some key parameters to consider when selecting a transformer to drive a particular ADC are insertion loss, return loss, magnitude imbalance, and phase imbalance. *Insertion loss* is a guide to the bandwidth capability of the transformer. *Return loss*, also useful, allows the user to design the termination to match the transformer's response at a particular frequency or band of frequencies—especially important when using transformers with greater than unity turns ratios. We will focus here on *magnitude-* and *phase imbalance*, and how they affect the ADC's performance in high-bandwidth applications.

Theoretical Analysis

Even with a wide bandwidth rating, the coupling between the transformer's single-ended primary and differential secondary, though linear, introduces magnitude- and phase imbalances. When applied to a converter (or other differential-input device), these imbalances worsen even-order distortion of the converted (or processed) signal. While usually negligible at low frequencies, this added distortion in high-speed converters becomes significant at roughly 100 MHz. Let us first examine how the magnitude- and phase imbalance of a differential-input signal, particularly the second-harmonic distortion, affect the performance of an ADC.

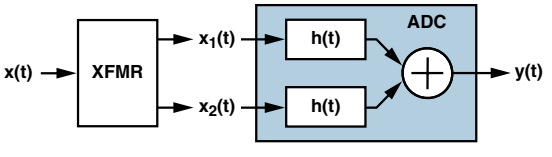

Figure 1. Simplified block diagram of the ADC front end using a transformer.

Consider the input, $x(t)$, to the transformer. It is converted into a pair of signals, $x_1(t)$ and $x_2(t)$. If $x(t)$ is sinusoidal, the differential output signals, x_1(t) and $x_2(t)$, are of the form

$$x_1(t) = k_1 \sin(\omega t)$$
$$x_2(t) = k_2 \sin(\omega t - 180° + \varphi) = -k_2 \sin(\omega t + \varphi) \quad (1)$$

The ADC is modeled as a symmetrical third-order transfer function:

$$h(t) = a_0 + a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) \quad (2)$$

Then

$$y(t) = h(x_1(t)) - h(x_2(t))$$
$$y(t) = a_1\left[x_1(t) - x_2(t)\right] + a_2\left[x_1^2(t) - x_2^2(t)\right] + a_3\left[x_1^3(t) - x_2^3(t)\right] \quad (3)$$

Ideal Case—No Imbalance

When $x_1(t)$ and $x_2(t)$ are perfectly balanced, they have the same magnitude ($k_1 = k_2 = k$) and are exactly 180° out of phase ($\varphi = 0°$). Since

$$x_1(t) = k \sin(\omega t)$$
$$x_2(t) = -k \sin(\omega t) \quad (4)$$

$$y(t) = 2a_1 k \sin(\omega t) + 2a_3 k^3 \sin^3(\omega t) \quad (5)$$

Applying the trigonometric identity for powers and gathering terms of like frequency,

$$y(t) = 2\left(a_1 k + \frac{3a_3 k^3}{4}\right)\sin(\omega t) - \left(\frac{a_3 k^3}{4}\right)\sin(3\omega t) \quad (6)$$

This is the familiar result for a differential circuit: even harmonics cancel for ideal signals, while odd harmonics do not.

Magnitude Imbalance

Now suppose the two input signals have a magnitude imbalance, but no phase imbalance. In this case, $k_1 \neq k_2$, and $\varphi = 0$.

$$x_1(t) = k_1 \sin(\omega t)$$
$$x_2(t) = -k_2 \sin(\omega t) \quad (7)$$

Substituting Equation 7 in Equation 3 and again applying the trigonometric power identities,

$$y(t) = \frac{a_2}{2}\left(k_1^2 - k_2^2\right) + \left(a_1(k_1 + k_2) + \frac{3a_3}{4}\left(k_1^3 + k_2^3\right)\right)\sin \omega t$$
$$- \left(\frac{a_2}{2}\left(k_1^2 - k_2^2\right)\right)\cos 2\omega t - \left(\frac{a_3}{4}\left(k_1^3 + k_2^3\right)\right)\sin 3\omega t \quad (8)$$

We see from Equation 8 that the second harmonic in this case is proportional to the difference of the squares of the magnitude terms, k_1 and k_2, viz.,

$$2^{nd}\ harmonic \propto k_1^2 - k_2^2 \quad (9)$$

Phase Imbalance

Assume now that the two input signals have a phase imbalance between them, with no magnitude imbalance. Then, $k_1 = k_2$, and $\varphi \neq 0$.

$$x_1(t) = k_1 \sin(\omega t)$$
$$x_2(t) = -k_1 \sin(\omega t + \varphi) \quad (10)$$

Substituting Equation 10 in Equation 3 and simplifying,

$$y(t) = \left(a_1 k_1 + \frac{3a_3 k_1^3}{4}\right)\left(\sin\omega t + \sin\omega t \cos\varphi + \cos\omega t \sin\varphi\right)$$
$$-\left(\frac{a_2 k_1^2}{2}\right)\left(\cos 2\omega t - \cos 2\omega t \cos 2\varphi + \sin 2\omega t \sin 2\varphi\right) \quad (11)$$
$$-\left(\frac{a_3 k_1^3}{4}\right)\left(\sin 3\omega t - \sin 3\omega t \cos 3\varphi + \cos 3\omega t \sin 3\varphi\right)$$

From Equation 11, we see that the second-harmonic amplitude is proportional to the square of the magnitude term, k.

$$2^{nd}\ harmonic \propto k_1^2 \quad (12)$$

Observations

A comparison of Equation 9 and Equation 12 shows that the second-harmonic amplitude is more severely affected by phase imbalance than by magnitude imbalance. For phase imbalance, the second harmonic is proportional to the square of k_1, while for magnitude imbalance, the second harmonic is proportional to the difference of the squares of k_1 and k_2. Since k_1 and k_2 are approximately equal, this difference is small.

As a test of the validity of these calculations, MATLAB code was written for the model described above to quantify and illustrate the impact of magnitude- and phase imbalances on harmonic distortion of a high-performance ADC with a transformer input (Appendix A). The model includes additive white Gaussian noise.

The coefficients, a_i, used in the MATLAB model are for the AD9445, a high-performance 16-bit, 125-MSPS ADC. The AD9445, in the front-end configuration shown in Figure 2, was used to generate the FFT shown in Figure 3, from which the coefficients were derived.

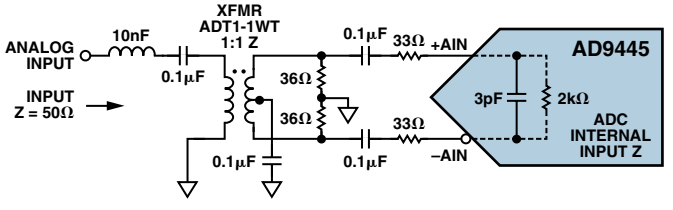

Figure 2. Front-end configuration of the AD9445 with transformer.

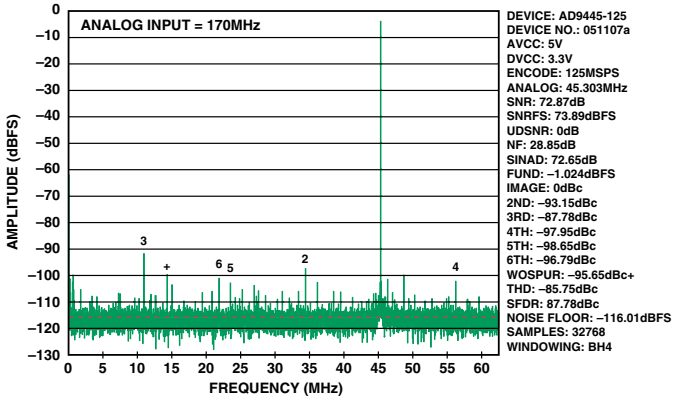

Figure 3. Typical FFT of AD9445, 125 MSPS, IF = 170 MHz.

The noise floor, second harmonic, and third harmonic here reflect the composite performance of the converter and front-end circuitry. The converter distortion coefficients (a_2 and a_3) and noise were computed using these measured results, combined with the 0.0607 dB of magnitude imbalance and 14° of phase imbalance at 170 MHz, specified for a standard 1:1 impedance ratio transformer.

These coefficients are used in Equation 8 and Equation 11 to compute $y(t)$, while the magnitude- and phase imbalances are varied in the ranges 0 V to 1 V and 0 degrees to 50 degrees, respectively (the imbalance ranges of a typical transformer in the 1-MHz-to-1000-MHz range), and observe the effect on the second harmonic. The results of the simulations are shown in Figure 4 and Figure 5.

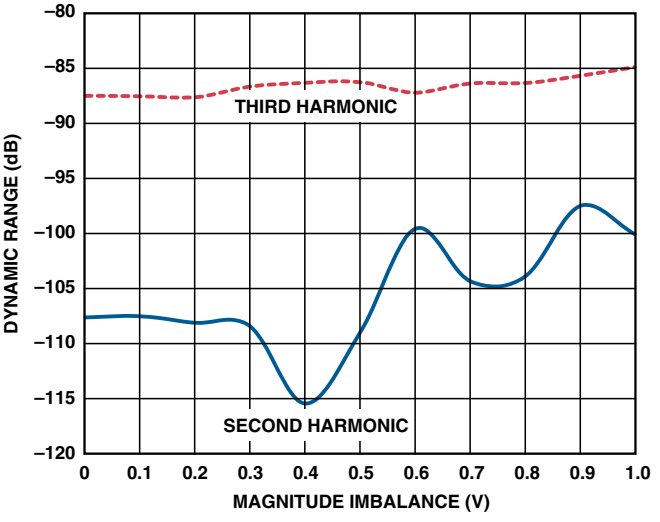

Figure 4. Harmonics plotted vs. *magnitude* imbalance only.

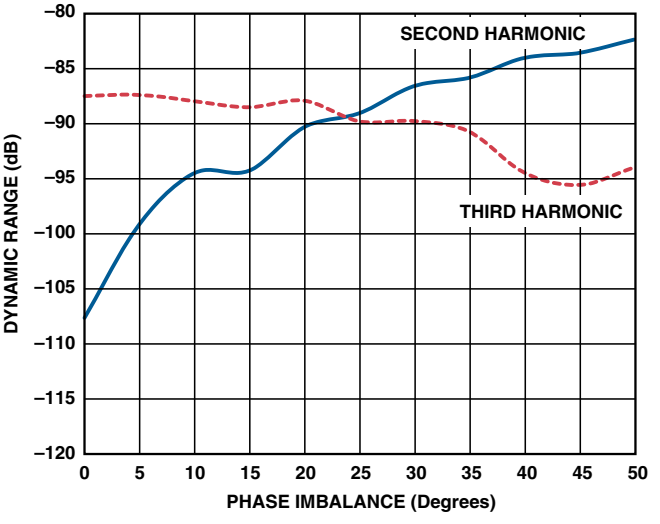

Figure 5. Harmonics plotted vs. *phase* imbalance only.

Figure 4 and Figure 5 show that (a) the third harmonic is relatively insensitive to both magnitude- and phase imbalance, and (b) that the second harmonic deteriorates more rapidly with phase imbalance than with magnitude imbalance. Thus, to achieve better performance from the ADC, a transformer configuration with improved phase imbalance is needed. Two feasible configurations, the first involving a double balun, and the second a double transformer, are shown in Figure 6 and Figure 7.

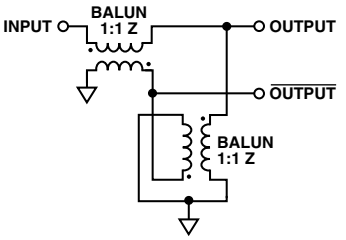

Figure 6. Double balun configuration.

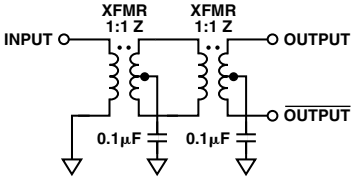

Figure 7. Double transformer configuration.

The imbalances from these configurations were compared using a vector network analyzer on specially designed characterization boards. Figure 8 and Figure 9 compare the magnitude- and phase imbalance of these configurations with that of a single transformer.

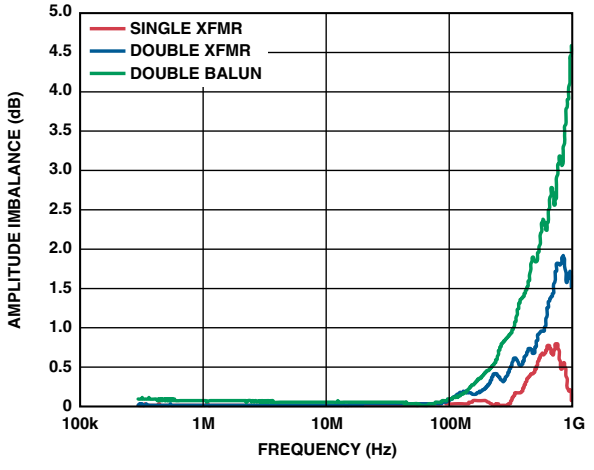

Figure 8. Magnitude imbalance from 1 MHz to 1000 MHz.

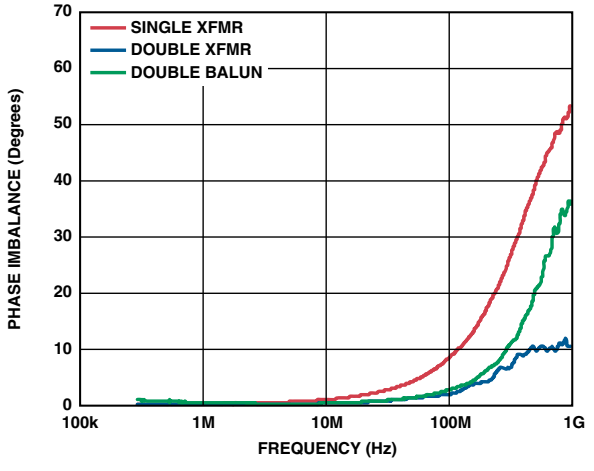

Figure 9. Phase imbalance from 1 MHz to 1000 MHz.

The above figures clearly show that the double configurations have better phase imbalance at the cost of slightly degraded magnitude imbalance. Therefore, using the results of the above analysis, it appears that the double-transformer configurations can be used to achieve better performance. FFT plots of AD9445 using a single transformer input (Figure 10) and a double balun input (Figure 11) show that this is indeed the case; a +10-dB improvement in SFDR is seen with a 300-MHz IF signal.

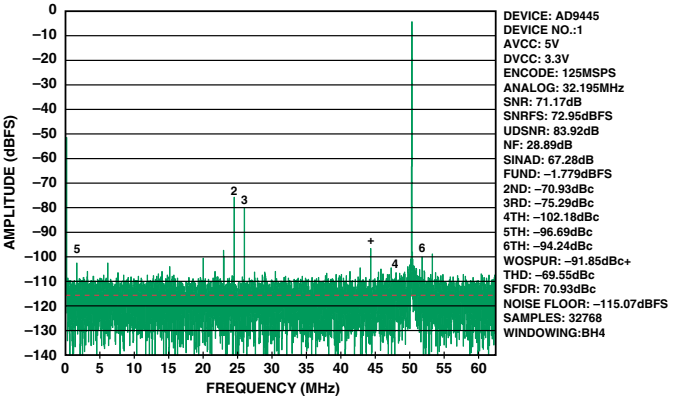

Figure 10. FFT of AD9445, single transformer input, 125 MSPS, IF = 300 MHz.

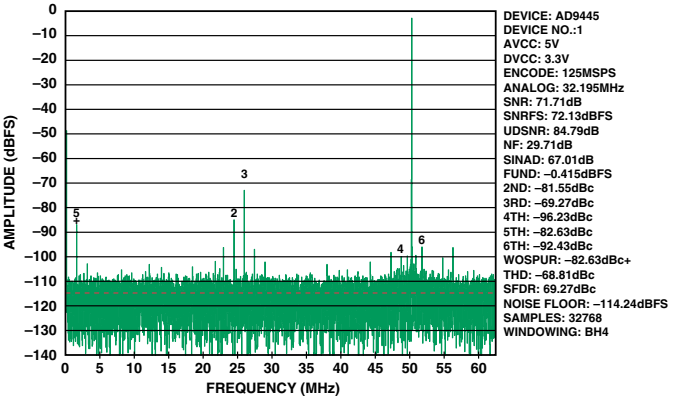

Figure 11. FFT of AD9445, double balun input, 125 MSPS, IF = 300 MHz.

Does this mean that to achieve good performance one must couple two transformers or two baluns onto the ADC's front end? Not necessarily. The analysis shows that it is essential to use a transformer that has very little phase imbalance. In the following examples (Figure 12 and Figure 13), two different single transformers were used to drive the AD9238 with a 170-MHz IF signal. These examples show that there is 29-dB improvement in second harmonic when the ADC is driven by a transformer that has improved phase imbalance at high frequencies.

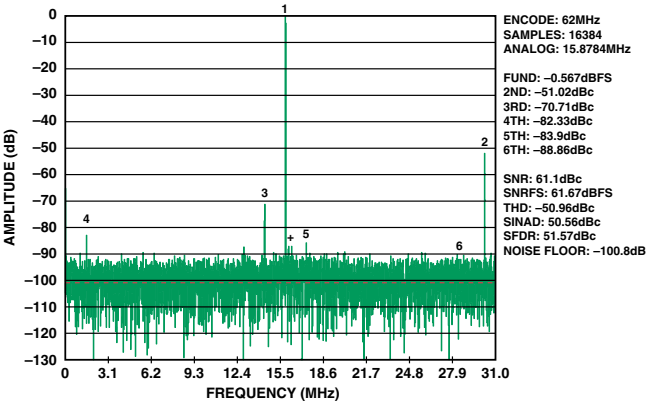

Figure 12. FFT of AD9238, single transformer input, 62 MSPS, IF = 170 MHz @ –0.5 dBFS, second harmonic = –51.02 dBc.

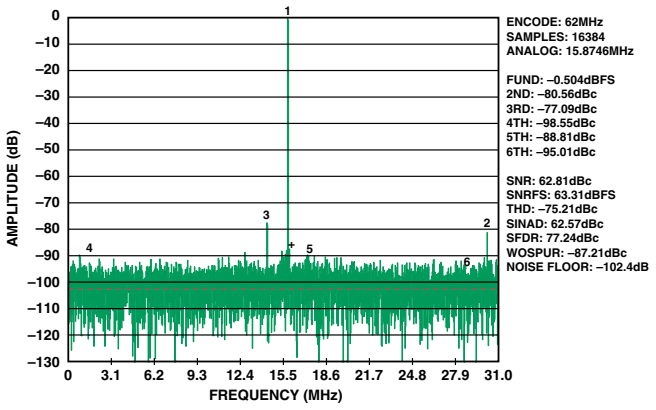

Figure 13. FFT of AD9238, single transformer input, 62 MSPS, IF = 170 MHz @ –0.5 dBFS, second harmonic = –80.56 dBc.

CONCLUSION

The phase imbalance of a transformer can worsen the second-harmonic distortion when the transformer is used as a front end for processes (such as A/D conversion, D/A conversion, and amplification) with high-IF inputs (>100 MHz). However, by employing a pair of transformers or baluns, significant improvements can be readily achieved, at the cost of an additional transformer and extra PC board space.

Single-transformer designs can achieve adequate performance if the design bandwidth is small and a suitable transformer is chosen. However, they do require a limited matching of bandwidth, and they can be expensive or physically large.

In either case, choosing the best transformer for any given application requires detailed knowledge of the transformer's specifications. Phase imbalance is of particular importance for high-IF inputs (>100 MHz). Even if it is not specified in the data sheet, most transformer manufacturers will provide phase-imbalance information upon request. A network analyzer can be used to measure the transformer's imbalances as a check, or if the information is not readily available.

ACKNOWLEDGEMENTS

The authors wish to thank Ravi Kummaraguntla, Andy Morgan, and Chad Shelton for their help in the theoretical analysis and for their lab support.

FURTHER READING

1. Reeder, Rob, "Transformer-Coupled Front End for Wideband A/D Converters," *Analog Dialogue*, Vol. 39, No. 2, pp. 3-6, 2005.
2. Mini-Circuits Data Sheet ADT1-1WT.
3. Pulse Data Sheet CX2039L.
4. Mini-Circuits Application Note: "How Transformers Work."
5. The Mathworks *Matlab* program.
6. Analog Devices Data Sheet AD9445.
7. Analog Devices Data Sheet AD9238.
8. M/A-COM Data Sheet TP101.
9. Sprague-Goodman Data Sheet GLSB4R5M102.

APPENDIX A

MATLAB code used in this experiment:

```
% Matlab code to study the effect of magnitude
and phase imbalance of input
% signals on the output
% Oct 19, 2005
clear all; close all;

% Error terms that can be set by the user
magnErrdB = 0; %in dB
phaseErr = 50; %in degrees
sd_noise = 100e-6; %std dev of noise

% Convert dB magnErr to voltage level
magnErr = 10^(magnErrdB/20);

% Coefficients
a0=0; %dc offset
a1=0.89; a2=0.00038; a3=0.0007; %coefficients
of 1st,2nd,3rd harmonics
                          %to match AD9445
typical FFT

fin = 100; %input freq - does not affect
calculations
t = 0:1:2047;
%Input signals
x1 = 0.5*sin((t/2048)*2*pi*fin);
x2 = 0.5*(magnErr)*sin(((t/2048)*2*pi*fin)-pi-
(phaseErr*pi/180));
%Each differential signal multiplied by the
transfer function
y1 = a0 + a1*x1 + a2*x1.^2 + a3*x1.^3;
y2 = a0 + a1*x2 + a2*x2.^2 + a3*x2.^3;
%Output
y = y1 - y2;
noise = sd_noise*randn(1,length(y));
y = y + noise;

% figure; plot(1000*t(1:80),x1(1:80),1000*t(1:8
0),x2(1:80),1000*t(1:80),y(1:80));

%Take the FFT
fft_y = fft(y/1024, 2048);
Pyy = 10*log10(fft_y.*conj(fft_y));
freq_axis = 0:1:1023;
% figure; plot(freq_axis, Pyy(1:1024), '-d');
% title('Frequency content of the output');
% xlabel('Frequency (Hz)');
% axis tight;

%Print fundamental and 2nd, 3rd harmonics
f = Pyy(101)
h2 = Pyy(201)
h3 = Pyy(301)
```

PRODUCT INTRODUCTIONS: VOLUME 40, NUMBER 3

Data sheets for all ADI products can be found by entering the model number in the Search box at www.analog.com

July

ADC, Sigma-Delta, 6-channel, 16-bit, includes in-amp and reference ... **AD7795**
ADC, Successive-Approximation, 16-bit, 2-MSPS, ±1.5-LSB INL ... **AD7622**
ADCs, Successive-Approximation, 6-channel, 14-/12-bit, 250-kSPS ... **AD7657/AD7658**
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Synthesizer, Direct Digital, 500-MSPS, 10-bit ... **AD9911**

August

ADC, Pipelined, quad, 14-bit, 50-MSPS, LVDS outputs ... **AD9259**
ADC, Pipelined, quad, 8-bit, 100-MSPS, LVDS outputs ... **AD9287**
Codec, Audio, 24-bit, 192-kHz includes PLL, 4 ADCs, 8 DACs ... **AD1939**
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Multiplier, Analog, symmetric, dc-to-2-GHz ... **ADL5391**
References, Voltage, LDO, precision, micropower, TSOT-23 package ... **ADR121/ADR125/ADR127**

September

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Amplifier, Current-Sense, high-side ... **ADM4073**
Amplifier, Instrumentation, precision, dual ... **AD8222**
Amplifier, Operational, quad, precision, low-noise, rail-to-rail outputs ... **AD8664**
Amplifier, Video, dual, low-power, 100 nA shutdown current ... **ADA4853-2**
Controller, Hot-Swap, 1.6-V to 16.5-V supply rails, soft-start ... **ADM1170**
Controller, Hot-Swap, 6-lead TSOT package ... **ADM4210**
Controllers, Hot-Swap, 2.7-V to 16.5-V supply rails ... **ADM1171/ADM1172**
Controller, Synchronous Buck, multiphase, 8-bit VID code ... **ADP3192**
Converter, DC-to-DC, step-up, lossless current sensing ... **ADP1621**
Converters, DC-to-DC, step-down, 97% efficiency ... **ADP2105/ADP2106/ADP2107**
DACs, Current-Output, 8-/10-/12-/14-bit, 175-MSPS, TxDAC ... **AD9704/AD9705/AD9706/AD9707**
Driver, Power Amplifier, 700-MHz to 1000-MHz, 50-Ω matching ... **ADL5322**
Driver, Power Amplifier, 1700-MHz to 2400-MHz, 50-Ω matching ... **ADL5323**
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Printed in the U.S.A. M02000403-xx-11/06

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