Volume 41, Number 1

Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

In This Issue

Analog Dialogue Since 1967

www.analog.com/analogdialogue

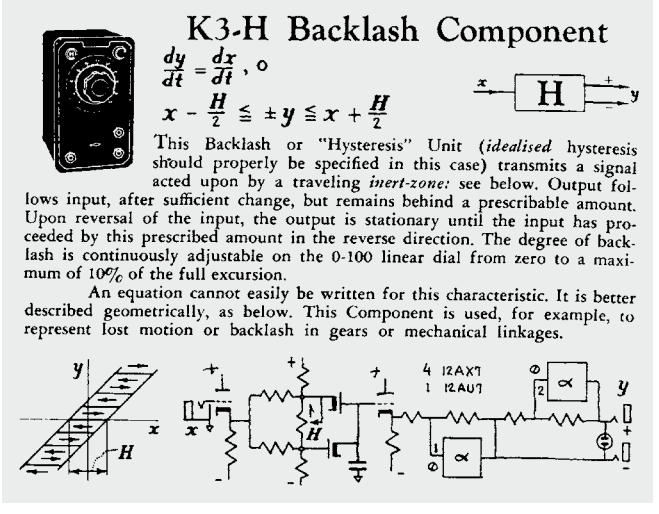
ANALOG DEVICES

Editors' Notes

HYSTERESIS AND HISTORY

In the heyday of analog computing, more than half a century ago, special circuits were needed to model nonlinear relationships; such as squaring, rooting, and bounds. Today, many such functions can be purchased or assembled rather easily. But a few were really awkward unless their nature could be clearly understood. This little essay is about the tricks used to model *linear hysteresis*, a function used to simulate such phenomena as backlash in gears or mechanical linkages. In words: Starting from a neutral position, x moves forward; after a short distance, say $\Delta x/2$, y starts to follow x and follows linearly. Whenever x reverses, y stays put until x has reversed by Δx, then it follows linearly until x again reverses direction; then y holds until x has again moved forward by Δx.

The figure shows how this was accomplished in the Philbrick K3-H Backlash Component, as described in the Philbrick *Catalog and Manual* ... (1951). The input, via a cathode follower, is split into an adjustable pair of biased voltages that are then compared with the voltage stored on a capacitor by a pair of diodes. The capacitor voltage can change only when the input either continues its existing course or reverses by more than H. The capacitor voltage is isolated by another follower, then made available at the outputs in ± polarities by a pair of op amps (α). (This description assumes that all elements are ideal-unity-gain followers, zero-drop diode conduction, $H<<E$, etc., and that if x stops for long periods, the charge on C holds.)



K3-H Backlash Component

$$\frac{dy}{dt} = \frac{dx}{dt}, \circ$$

$$x - \frac{H}{2} \leqq \pm y \leqq x + \frac{H}{2}$$

This Backlash or "Hysteresis" Unit (*idealised* hysteresis should properly be specified in this case) transmits a signal acted upon by a traveling *inert-zone:* see below. Output follows input, after sufficient change, but remains behind a prescribable amount. Upon reversal of the input, the output is stationary until the input has proceeded by this prescribed amount in the reverse direction. The degree of backlash is continuously adjustable on the 0-100 linear dial from zero to a maximum of 10% of the full excursion.

An equation cannot easily be written for this characteristic. It is better described geometrically, as below. This Component is used, for example, to represent lost motion or backlash in gears or mechanical linkages.

Another way to characterize this function is as a *dead-zone* in an integrating loop. The integrating capacitor is holding charge while the input is in the dead zone; otherwise the output voltage is tracking the input. A scheme for accomplishing this can be found in the Philbrick *Applications Manual* ... (1966), on page 60: http://www.analog.com/library/analogDialogue/archives/philbrick/056-062.pdf.

It's a not-often-thought-about function, but if you ever need it, you can find it in that venerable analog designer's bag of tricks.

Dan Sheingold [dan.sheingold@analog.com]

IN THIS ISSUE

This issue, Volume 41, Number 1, marks the first time that *Analog Dialogue* has gone to print in Chinese and Japanese, so we would like to take this opportunity to extend a special welcome to our new readers of those versions.

The rapid expansion of the electric power industry has created a worldwide need to reinforce existing transmission and distribution networks and to construct new substations. Advances in microprocessor technology and the increasing cost of support staff are key drivers for power companies to design new automated high-voltage substations using high-accuracy integrated automation systems (page 3).

The circuitry ahead of a high-performance ADC is critical to achieving desired system performance. The optimal design depends on many factors, including the application, system partition, and ADC architecture. Amplifiers consume power and add noise, whereas transformers consume no power and add negligible noise. On the other hand, amplifiers maintain dc levels, provide easily adjustable gain, and have flatter response (page 6).

Making accurate high-speed time-domain measurements can be challenging, but a few tips and tricks, coupled with some good old-fashioned common-sense engineering, can help yield quick and accurate results. When choosing a scope and probe for high-speed measurement, first consider: *signal amplitude, source impedance, rise time,* and *bandwidth*. The *type of probe* and *length of the ground lead* are also important (page 13).

2007 also marks the introduction of the *Back Burner*, an online column that features design ideas, measurement tips and tricks, tutorials, and teasers. This quarter's articles, currently available only on the Web, include tips on measuring ambient and PCB temperatures, designs for a pulse oximeter and programmable waveform generator using the ADuC7024, and an algorithm that can enhance performance in an accelerometer-based pedometer. We hope that you enjoy this new column.

As always, your comments are welcome.

Scott Wayne [scott.wayne@analog.com]

Analog Dialogue

www.analog.com/analogdialogue **dialogue.editor@analog.com**

Analog Dialogue is the free technical magazine of Analog Devices, Inc., published continuously for 41 years—starting in 1967. It discusses products, applications, technology, and techniques for analog, digital, and mixed-signal processing. It is currently published in two editions—*online*, monthly at the above URL, and quarterly *in print*, as periodic retrospective collections of articles that have appeared online. In addition to technical articles, the online edition has timely announcements, linking to data sheets of newly released and pre-release products, and "Potpourri"—a universe of links to important and rapidly proliferating sources of relevant information and activity on the Analog Devices website and elsewhere. The *Analog Dialogue* site is, in effect, a "high-pass-filtered" point of entry to the **www.analog.com** site—the virtual world of *Analog Devices*. For history buffs, the *Analog Dialogue* archives include all regular editions, starting with Volume 1, Number 1 (1967), plus three special anniversary issues.

If you wish to subscribe to the print edition, please go to **www.analog.com/analogdialogue** and click on **<subscribe>**. Your comments are always welcome; please send messages to **dialogue.editor@analog.com** or to these individuals: *Dan Sheingold*, Editor **[dan.sheingold@analog.com]** or *Scott Wayne*, Managing Editor and Publisher **[scott.wayne@analog.com].**

ISSN 0161-3626

High-Performance Multichannel Power-Line Monitoring with Simultaneous-Sampling ADCs

By Colm Slattery [colm.slattery@analog.com]

INTRODUCTION

The rapid expansion of the electric power industry has created a worldwide need to reinforce existing transmission and distribution networks and to construct new substations. Advances in microprocessor technology and the increasing cost of support staff are key drivers for power companies to design new automated high-voltage substations using high-accuracy integrated automation systems.

Substations can be classified into two categories, according to voltage level: *high-voltage* includes 500-kV, 330-kV, and some 220-kV substations, while 220-kV *terminal* substations, 110-kV, and 35-kV substations are considered *medium-* or *low-voltage*. High-voltage (*transmission*) substations are large outdoor sites. Low-voltage (*distribution*) substations are indoor systems located in urban areas to handle high load density.

Improved signal processing technologies make it possible to achieve better than 0.1% accuracy in next-generation systems, as compared to present systems' typical 0.5% accuracy levels—an improvement mainly achieved with the use of high-performance simultaneous-sampling ADCs (analog-to-digital converters); they provide the resolution and performance that will be needed for future systems.

System Architecture

Figure 1 shows waveforms in a typical 3-phase measurement system. Each power phase is represented by a *current transformer* (CT) and a *voltage transformer* (PT). The complete system comprises three such pairs. The average power in the system at any instant is calculated by rapidly taking a number of samples of the output of each transformer, performing a discrete Fourier transform (DFT) on the sampled data, and performing the necessary multiplications and summations.

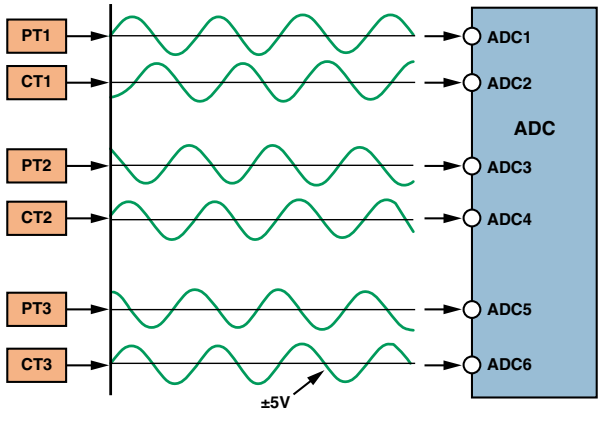


Figure 1. Waveforms in a typical 3-phase system.

The ADC takes 32 sets of simultaneous samples of three CT and three PT outputs and stores the results in RAM. The system then calculates a DFT on all six outputs, and presents the results in real- and imaginary format, $(A + jB)$. Magnitude and phase information for each transformer can be calculated as follows:

With $A + jB$ and $C + jD$ as the real and imaginary terms for CT1 and PT1, the magnitudes (M_i) and phases (P_i) are:

$$M_1(\mathrm{CT1}) = \sqrt{A^2 + B^2}, \quad P_1(\mathrm{CT1}) = \tan^{-1}(B/A) = \psi$$

$$M_2(\mathrm{PT1}) = \sqrt{C^2 + D^2}, \quad P_2(\mathrm{PT1}) = \tan^{-1}(D/C) = \theta$$

The power through the PT1/CT1 pair is:

$$\ddot{U}_1 = M_1 \times M_2 \cos(\psi - \theta)$$

Similar calculations for the power through PT2/CT2 and PT3/CT3 give $\ddot{U}_2$ and $\ddot{U}_3$. The total average power in the system is calculated by summing the three power terms:

$$Total\ Power = \ddot{U}_1 + \ddot{U}_2 + \ddot{U}_3$$

This method uses a DFT and the above calculations to determine the system power at a single frequency. Performing a fast Fourier transform (FFT) instead of a DFT provides data on harmonics and other higher frequency components; this can allow calculation of additional information, such as system losses or the effects of unwanted noise.

System Requirement

A substation may contain hundreds of transformers. The measured voltages and currents are scaled such that the ±5-V or ±10-V full-scale output range of the transformers represents a range much greater than the full-scale power output capability of the power line. Generally, the power line (especially the current measurements) will run at less than 5% of this range, and typical transformer outputs will lie in a ±20-mV range. Larger signals occur rarely; when they do they usually imply a system fault.

Accurate measurement of these small signals requires a high-resolution ADC with excellent signal-to-noise (S/N). The multichannel ADCs that are used must also be capable of simultaneous sampling. Currently available systems have 14-bit capability—the 4-channel AD7865[1] 14-bit quad ADC, for example, accepts true bipolar signals and provides 80-dB SNR. However, there is an increasing need for higher-performance multichannel ADCs, with 16-bit resolution at sampling rates of 10 kSPS. To make accurate 3-phase current- and voltage measurements, the ADC should be capable of sampling six channels simultaneously, and it must have excellent SNR to measure small signals. Where many ADCs are used in one system, low power dissipation is also important.

An example of a device that meets all of these requirements is the AD7656,[2] which includes six low-power, 16-bit, 250-kSPS successive-approximation ADCs in a single package. Shown in Figure 2, the AD7656 is fabricated in the *industrial CMOS* (*i*CMOS®)[3] process, which combines high-voltage devices with submicron CMOS and complementary bipolar technologies. *i*CMOS makes possible a wide range of high-performance analog ICs that are capable of high-voltage operation. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can readily accept bipolar input signals, providing increased performance and dramatically reducing power consumption and package size.

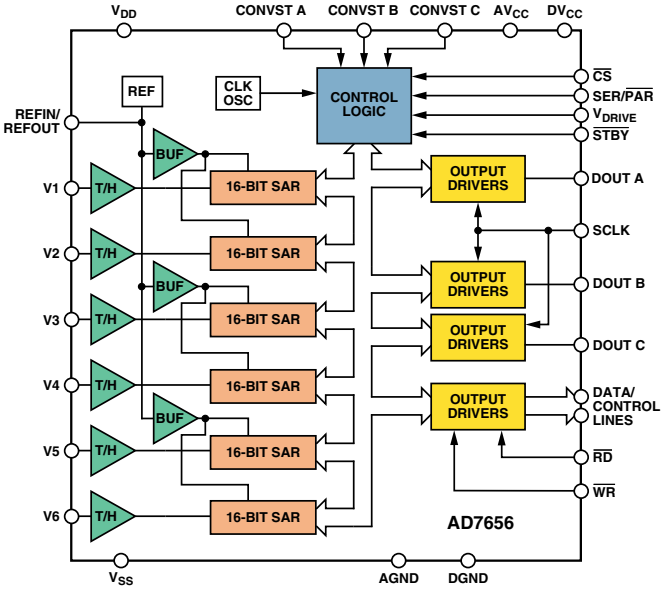


Figure 2. The AD7656 has six simultaneous-sampling ADCs, a voltage reference, three reference buffers, and an oscillator.

With 86.6-dB SNR, as shown in Figure 3, the AD7656 provides the performance needed to measure small ac outputs from transformers. Its 250-kSPS update rate is helpful in simplifying designs that need fast data acquisition in order to do real-time FFT post-processing. It is capable of directly accepting ±5-V and ±10-V outputs from the transformer without gain- or level shifting—and consumes a maximum of only 150 mW per device. This is an important consideration when a board must house many ADC channels. Because some systems require as many as 128 channels (as many as 22 six-channel ADCs) on one board, power dissipation can be a critical specification.

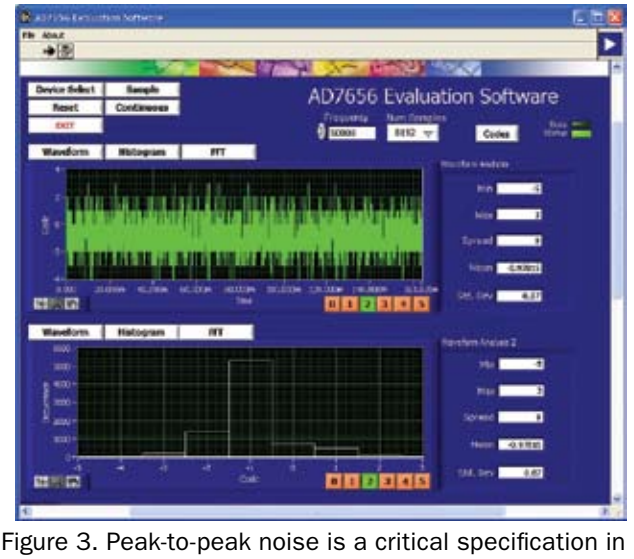


Figure 3. Peak-to-peak noise is a critical specification in power-line monitoring applications. The AD7656 here has only 6-code peak-to-peak noise over 8192 samples.

Beyond the ADC

A complete power-line measurement system is shown in Figure 4. While the ADC is the heart of the system, many other factors must be considered when designing a high-performance system. The voltage reference and input amplifiers are also critical to system performance, and isolation may be required for remote communications.

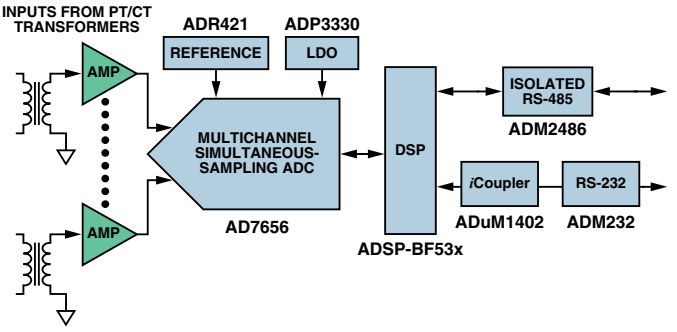


Figure 4. Power-line monitoring system.

ADC Reference Consideration

Whether to use the ADC's built-in reference (for devices that have an internal reference) or an external reference depends on the system requirements. When multiple ADCs are used on a single board, an external reference works best, as a common reference can eliminate part-to-part reference variations, thus taking advantage of ratiometric behavior.

Generally, a low-drift reference is also important for reducing reference sensitivity to temperature. A simple calculation can help in understanding the importance of drift and in deciding whether to go with the internal reference. A 16-bit ADC with 10-V full-scale input has a resolution of 152 μV. The drift specification of the AD7656's internal reference is 25 ppm/°C maximum (6 ppm/°C typical). Over a 50°C temperature range, the reference could drift as much as 1250 ppm; or about 12.5 mV. In applications where drift is important, an external low-drift reference, such as the ADR421[4] (1 ppm/°C), would be a better choice. A 1 ppm/°C reference will drift by only 0.5 mV over a 50°C temperature range.

Amplifier Choice

The key requirements to consider when choosing an amplifier for power-line monitoring applications are low noise and low offset.

The noise generated by the driver amplifier must be kept as low as possible to preserve the SNR and transition noise performance of the ADC. A low-noise amplifier is also useful for measuring small ac signals. The amplifier's total offset error, including drift, over the full temperature range should be less than the required resolution. The OP1177[5]/OP2177[6]/OP4177[7] family of amplifiers combines excellent noise performance (8.5 nV/√Hz) with low offset drift. For example, the OP1177 op amp specifies 60-μV maximum offset and 0.7-μV/°C maximum offset drift. Over a 50°C operating range, the maximum offset drift is 35 μV, so the total error due to offset and offset drift will be less than 95 μV, or 0.0625 LSB.

For power-line monitoring applications, power considerations can be important, especially when up to 128 channels may be measured on one board. The OP1177 family typically consumes a supply current of less than 400 μA per amplifier.

The following table compares some recommended amplifiers for power-line monitoring applications.

Part Number	Noise (nV/√Hz)	Offset Voltage, Typical (mV)	Offset Voltage, Maximum (mV)	Supply Current (mA)	Package
OP4177	8.0	15	75	0.4	TSSOP, SOIC
ADA4004[8]	1.8	40	125	1.7	LFCSP, SOIC
OP747[9]	15	30	100	0.3	SOIC

ADC Power Supply Generation

Both analog and digital power supplies are required for ADCs. Most systems have a 5-V digital supply, but many do not have a 5-V analog supply. Since using the same supply for both analog and digital circuitry could couple unwanted noise into the system, it is generally a practice to be avoided. For designs that have bipolar ±12-V supplies available, a low-cost, *low-dropout* regulator (LDO), such as the ADP3330,[10] could be used to generate a good quality 3-V or 5-V supply with 1.4% accuracy over variations in temperature, load, and line.

Communications

The many systems in a single substation require communication with a remote main system controller, typically with electrical isolation. Optocoupler solutions, with their LEDs and photodiodes, are now being supplanted by *i*Coupler® digital isolators,[11] which use chip-scale microtransformers. *i*Coupler devices have two- to four-times faster data rates than commonly used high-speed optocouplers—and they operate with as little as 1/50 the power—with correspondingly lower heat dissipation, improved reliability, and reduced cost. In addition to these benefits, the integrated solution also reduces board space and simplifies layout. The ADuM1402[12] 4-channel digital isolator handles data rates up to 100 MSPS with isolation up to 2.5 kV.

RS-232 is often used to connect multiple systems, so isolation between each system and the bus is critical. Digital isolators do not support the RS-232 standard, so they cannot be used between the transceiver and the cable; instead they are used between the transceiver and the local system. Combining an ADuM1402 *i*Coupler digital isolator, an ADM232L[13] RS-232 transceiver, and an isolated power supply eliminates ground loops and provides effective protection against surge damage.

For systems using the RS-485 protocol, the ADM2486[14] single-chip isolated RS-485 transceiver is available (Figure 5). It can support data rates up to 20 Mbps and has a 2.5-kV isolation rating.

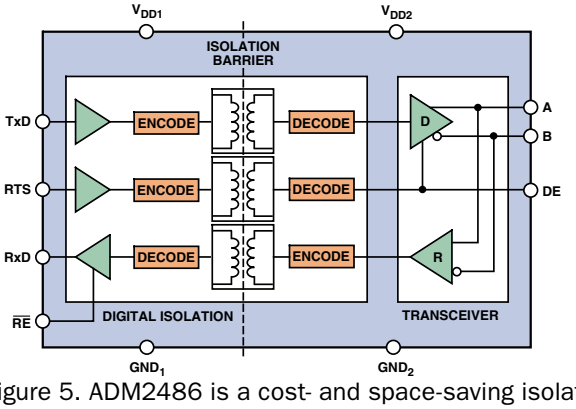


Figure 5. ADM2486 is a cost- and space-saving isolated RS-485 transceiver.

Signal Processing

Power-line monitoring applications require digital signal processing (DSP) to perform complex math calculations. The high-performance, low-cost, low-power ADSP-BF531[15] Blackfin processor is ideally suited for performing these complex DFT or FFT calculations.

This Blackfin[16] processor—a highly integrated system-on-a-chip—includes a CAN 2.0B controller, a TWI controller, two UART ports, an SPI port, two serial ports (SPORTs), nine general-purpose 32-bit timers (eight with PWM capability), a real-time clock, a watchdog timer, and a parallel peripheral interface (PPI). These peripherals provide the flexibility needed to communicate across multiple parts and interfaces in the system.

Blackfin processors such as the ADSP-BF536[17] and ADSP-BF537[18] include an IEEE-compliant 802.3 10/100 Ethernet MAC (media access controller). This is now a standard requirement for many power-line monitoring systems.

Practical Design Considerations

Special consideration should be given to the ADC's location and surroundings when designing the printed circuit board. Analog and digital circuitry should be separated and confined to certain areas of the board. At least one ground plane should be used. Avoid running digital lines under the ADC because they couple noise onto the die. The analog ground plane should be allowed to run under the AD7656 to avoid noise coupling. Clocks and other high-speed switching signals should be shielded with digital ground to avoid radiating noise to other sections of the board, and they should never run near analog signal paths. Crossover of digital and analog signals should be avoided. Traces on different but close layers of the board should run at right angles to each other to reduce the effects of feedthrough.

The power supply lines to the ADC should use the largest possible traces to provide low impedance paths and reduce the effect of glitches on the power supply lines. Good connections should be made between the AD7656 supply pins and the power tracks on the board; this should involve the use of single- or multiple vias for each supply pin. Good decoupling is also important to lower the supply impedance presented to the AD7656 and to reduce the magnitude of the supply spikes. Paralleled decoupling capacitors, typically 100 nF and 10 µF, should be placed on all of the power supply pins, close to—or ideally right up against—these pins and their corresponding ground pins.

CONCLUSION

Increasing worldwide power demands are driving an increase in the number of power lines and power-line substations. As more and more automated monitoring- and fault-detection systems are required, the trend will be toward systems with a large number of channels. With multiple ADCs on each board, efficient use of board area and power dissipation become critical as system designers try to reduce cost while increasing performance.

Higher system performance can be achieved by using high-performance ADCs, such as the AD7656. With six channels and 16-bit resolution, its low power dissipation, high SNR, and small package combine to meet the needs of the next generation of power-line-monitoring system designs.

REFERENCES—VALID AS OF APRIL 2007

[1]ADI website: www.analog.com (Search) AD7865 (Go)
[2]ADI website: www.analog.com (Search) AD7656 (Go)
[3]ADI website: www.analog.com (Search) iCMOS (Go)
[4]ADI website: www.analog.com (Search) ADR421 (Go)
[5]ADI website: www.analog.com (Search) OP1177 (Go)
[6]ADI website: www.analog.com (Search) OP2177 (Go)
[7]ADI website: www.analog.com (Search) OP4177 (Go)
[8]ADI website: www.analog.com (Search) ADA4004 (Go)
[9]ADI website: www.analog.com (Search) OP747 (Go)
[10]ADI website: www.analog.com (Search) ADP3330 (Go)
[11]ADI website: www.analog.com (Search) isolators (Go)
[12]ADI website: www.analog.com (Search) ADuM1402 (Go)
[13]ADI website: www.analog.com (Search) ADM232L (Go)
[14]ADI website: www.analog.com (Search) ADM2486 (Go)
[15]ADI website: www.analog.com (Search) ADSP-BF531 (Go)
[16]ADI website: www.analog.com (Search) Blackfin (Go)
[17]ADI website: www.analog.com (Search) ADSP-BF536 (Go)
[18]ADI website: www.analog.com (Search) ADSP-BF537 (Go)

Ask The Applications Engineer—36

Wideband A/D Converter Front-End Design Considerations II:

Amplifier- or Transformer Drive for the ADC?

By Rob Reeder [rob.reeder@analog.com]
Jim Caserta [jim.caserta@analog.com]

Design of the input configuration, or "front end," ahead of a high-performance analog-to-digital converter (ADC) is critical to achieving desired system performance. Optimizing the overall design depends on many factors, including the nature of the application, system partition, and ADC architecture. The following questions and answers highlight the important practical considerations affecting the design of an ADC front end using amplifier- and transformer circuitry.

Q. *What is the fundamental difference between amplifiers and transformers?*

A. An amplifier is an active element, while a transformer is passive. Amplifiers, like all active elements, consume power and add noise; transformers consume no power and add negligible noise. Both have dynamic effects to be dealt with.

Q. *Why would you use an amplifier?*

A. Amplifier performance has fewer limitations than those of transformers. If dc levels must be preserved, an amplifier must be used, because transformers are inherently ac-coupled devices. On the other hand, transformers provide galvanic isolation if needed. Amplifiers provide gain more easily because their output impedance is essentially independent of gain. On the other hand, a transformer's output impedance increases with the square of the voltage gain—which depends on the turns ratio. Amplifiers provide flatter response in the pass band, free of the ripple due to the parasitic interactions in transformers.

Q. *How much noise does an amplifier typically add, and what can I do to reduce this?*

A. A typical amplifier that might be considered, the ADA4937,[1] for example, when configured for G = 1, has an output noise spectral density of 6 nV/√Hz at high frequencies, compared to the 10-nV/√Hz input noise spectral density of the 80-MSPS AD9446-80[2] ADC. The problem here is that the amplifier has a noise bandwidth equivalent to the full bandwidth of the ADC, around 500 MHz, while the ADC noise is folded to one Nyquist zone (40 MHz). Without a filter, the integrated noise then becomes 155 μV rms for the amplifier and 90 μV rms for the ADC. Theoretically, this degrades the overall system SNR (signal-to-noise ratio) by 6 dB. To confirm this experimentally, the measured SNR, with the ADA4937 driving the AD9446-80, is 76 dBFS, and the noise floor is –118 dB (Figure 1). With a transformer drive, the SNR is 82 dBFS. The driver amplifier has thus degraded the SNR by 6 dB.

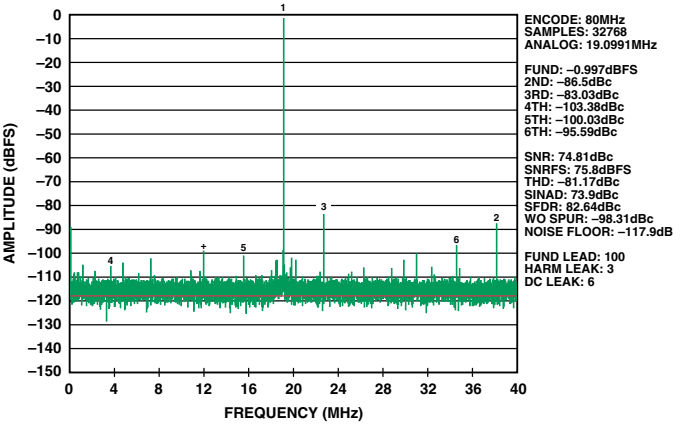


Figure 1. ADA4937 amplifier driving an AD9446-80 ADC at 80 MSPS without a noise filter.

To make better use of the ADC's SNR, a filter is inserted between the amplifier and ADC. With a 100-MHz 2-pole filter, the amplifier's integrated noise becomes 71 μV rms, degrading the ADC's SNR by only 3 dB. Use of the 2-pole filter improves the SNR performance of the Figure 1 circuit to 79 dBFS, with a noise floor of –121 dB, as shown in Figure 2a. The 2-pole filter is built with 24-Ω resistors and 30-nH inductors in series with each of the amplifier's outputs, and a 47-pF differentially connected capacitor (Figure 2b).

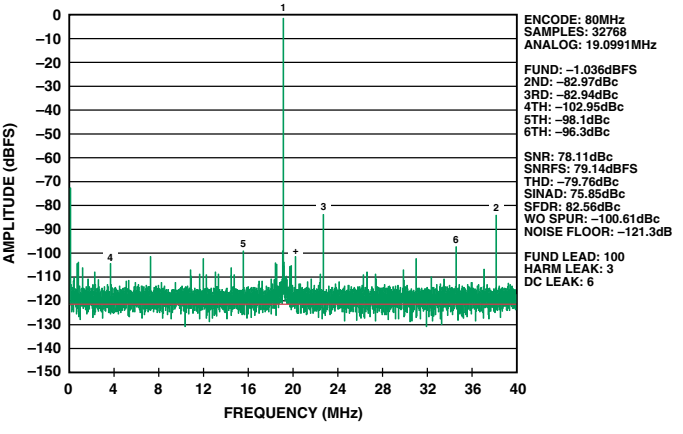


Figure 2a. Driving an AD9446-80 with a 100-MHz noise filter.

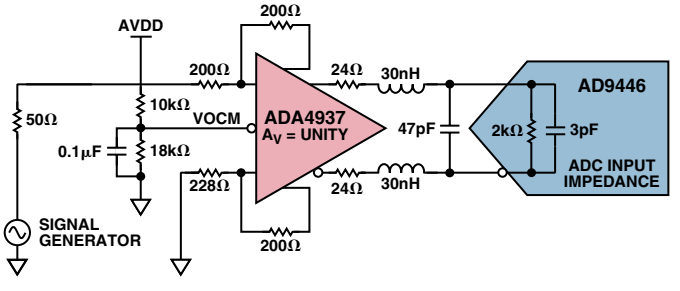


Figure 2b. Schematic diagram of ADA4937 amplifier driving an AD9446-80 ADC at 80 MSPS with a 2-pole noise filter.

Q. *How do high-speed amplifiers and ADCs compare in power consumption?*

A. This depends on the amplifier and ADC used. Two typical amplifiers, with similar power consumption, are the AD8352,[3] which draws 37 mA @ 5 V (185 mW), and the ADA4937, which draws 40 mA @ 5 V (200 mW). Overall power consumption can be reduced by about one-third, with slightly degraded performance, by using a 3.3-V supply. ADCs feature more diversity in power consumption, depending on resolution and speed. The 16-bit, 80-MSPS AD9446-80 draws 2.4 W, the 14-bit, 125-MSPS AD9246-125[4] draws 415 mW, and the 12-bit, 20-MSPS AD9235-20[5] draws only 95 mW.

Q. *When do you need to use a transformer?*

A. Transformers offer the biggest performance advantage compared to amplifiers at very high signal frequencies and when significant additional noise cannot be tolerated at the ADC input.

Q. *How do transformers and amplifiers differ when providing gain?*

A. The main difference is in the impedance they present to the ADC input, which directly affects system bandwidth. A transformer's input- and output impedance are related by the square of the turns ratio, while an amplifier's input and output impedance are essentially independent of gain.

For example, when a G = 2 transformer is used from a 50-Ω source impedance, the impedance seen at the secondary side of the transformer is 200 Ω. The AD9246 ADC has a differential input capacitance of 4 pF which, coupled with the 200-Ω transformer impedance, reduces the ADC's –3-dB bandwidth from 650 MHz to 200 MHz. Extra series resistance and differential capacitance are often needed to improve performance and reduce kickback from the converter, which can limit –3-dB bandwidth further, possibly to 100 MHz.

When a low-output-impedance amplifier—such as the ADA4937—is used, the result is a very low source impedance, usually less than 5 Ω. 25-Ω transient-limiting resistors can be used in series with each ADC input; in the case of the AD9246, the ADC's full 650-MHz analog input bandwidth would be usable.

So far the discussion has been about –3-dB bandwidths. When tighter flatness is needed, say 0.5 dB in a 1-pole system, the –3-dB bandwidth needs to be about 3× wider. For 0.1-dB flatness with one pole, the ratio increases to 6.5×. If 0.5-dB flatness is required at up to 150 MHz, a –3-dB bandwidth greater than 450 MHz is required, which is difficult to attain with a G = 2 transformer but is straightforward with a low-output-impedance amplifier.

Q. *What are the factors to consider in choosing a transformer or an amplifier to drive an ADC?*

A. They can be boiled down to a half-dozen parameters—outlined in this table:

Parameter	Usual Preference
Bandwidth	Transformer
Gain	Amplifier
Pass band flatness	Amplifier
Power requirement	Transformer
Noise	Transformer
DC vs. ac coupling	Amplifier (dc level preservation)
	Transformer (dc isolation)

Applications in which key parameters are in conflict require additional analysis and trade-offs.

Q. *What are some considerations in this analysis?*

A. One must start by understanding the level of difficulty in designing a front end for a given ADC. First, is the ADC internally buffered, or is it unbuffered (for example, a switched-capacitor type)? Naturally, the level of difficulty increases as the frequency increases in either case. But switched-capacitor types are more difficult for the designer to deal with.

If gain is needed to make full use of the ADC's input range, an application that might otherwise favor a transformer becomes more difficult as the required gain (turns ratio) increases.

Of course, the difficulty increases with frequency. Design of an IF system below 100 MHz with a buffered ADC would be relatively simple compared to a high-IF design with low signal levels using an unbuffered ADC, as Figure 3 illustrates. With so many parameters pulling in different directions, trade-offs are sometimes difficult and often puzzling to keep track of as components are changed and evaluated.

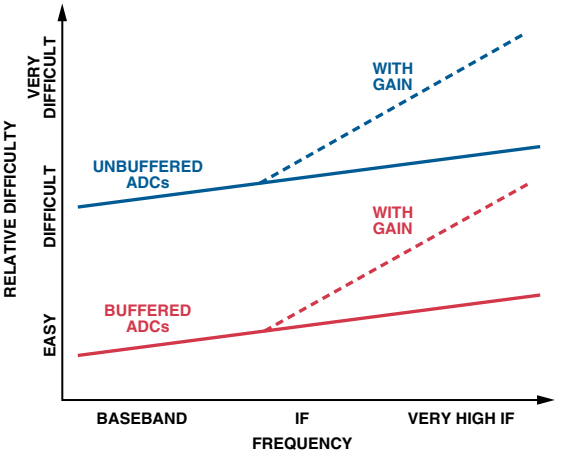


Figure 3. Relative difficulty vs. frequency.

It may be useful to employ a spreadsheet or table to keep all of the parameters straight as the design moves forward. There is no optimum design to satisfy all cases; it will be subject to the available components and the application specifications.

Q. *OK, design can be difficult. Now how about some details regarding system parameters?*

A. First, it is paramount that everything be taken into account when designing an ADC front end! Each component should be viewed as part of the load on the previous stage and maximum power transfer occurs when Z_{SOURCE} = conjugate Z_{LOAD} (Figure 4).

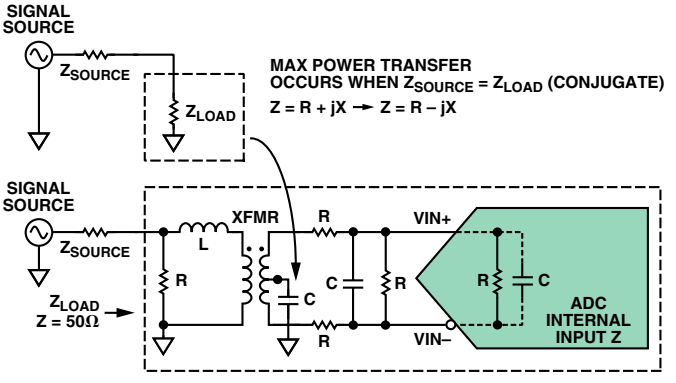


Figure 4. Maximum power transfer.

Now to the design parameters:

Input impedance is the characteristic impedance of the design. In most cases it is 50 Ω, but different values may be called for. The transformer makes a good transimpedance device. It allows the user to couple between different characteristic impedances when needed and fully balance the overall load of the system. In an amplifier circuit, the impedance is specified as an input- and output characteristic that can be designed to not change over frequency as a transformer might.

Voltage standing-wave ratio (VSWR) is a dimensionless parameter that can be used to understand how much power is being reflected into the load over the bandwidth of interest. An important measure, it determines the input drive level required to achieve the ADC's full-scale input.

Bandwidths are ranges of frequencies used in the system. They can be narrow or wide, at baseband, or covering multiple Nyquist zones. Their frequency limits are typically the –3-dB points.

Pass-band flatness (also *gain flatness*) specifies the amount of (positive and negative) variation of response with frequency within a specified bandwidth. It may be a ripple or simply a monotonic roll-off, like a Butterworth filter characteristic. Whatever the case, pass-band flatness is usually required to be *less than or equal to* 1 dB and is critical for setting the overall system gain.

Input drive level is determined by the system gain needed for the particular application. It is closely related to the bandwidth specification and depends on the front-end components chosen, such as the filter and amplifier/transformer; their characteristics can cause the drive level requirement to be one of the most difficult parameters to maintain.

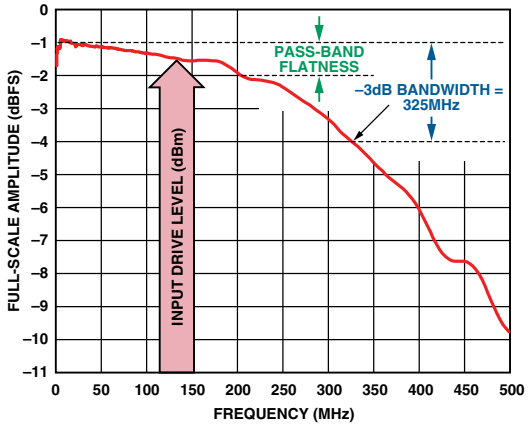


Figure 5. Bandwidth, pass-band flatness, and input drive level defined.

Signal-to-noise ratio (SNR) is the log-ratio of the rms value of the full-scale signal to the root-sum-square of all noise components within a given bandwidth, but not including distortion components. In terms of the front end, SNR degrades with increased bandwidth, jitter, and gain (at high gains, amplifier noise components that may have been negligible at low gain can become significant).

Spurious-free dynamic range (SFDR) is the ratio of the rms full-scale value to the rms value of the largest spurious spectral component. Two major contributors of spurs at the front end are the nonlinearity of the amplifier (or the transformer's lack of perfect balance), which produces mostly second-harmonic distortion—and the input mismatch and its amplification by the gain (at higher gain, matching is more difficult and parasitic nonlinearities are amplified), generally seen as a third-harmonic distortion.

Q. *What is important to know about transformers?*

A. Transformers have many different characteristics—such as voltage gain and impedance ratio, bandwidth and insertion loss, magnitude- and phase imbalance, and return loss. Other requirements may include power rating, type of configuration (such as balun or transformer), and center-tap options.

Designing with transformers is not always straightforward. For example, transformer characteristics change over frequency, thus complicating the model. An example of a starting point for modeling a transformer for ADC applications can be seen in Figure 6. Each of the parameters will depend on the transformer chosen. It is suggested that you contact the transformer manufacturer to obtain a model if available.

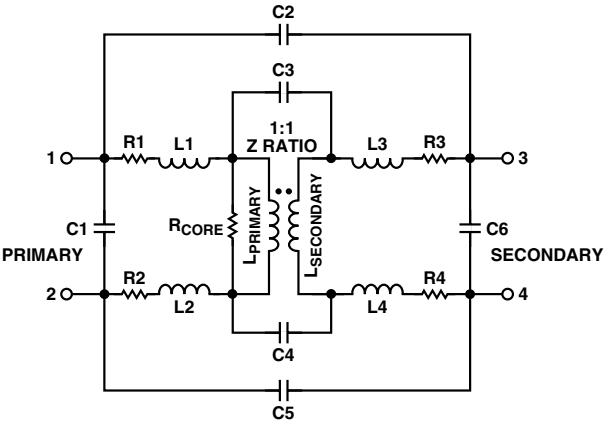


Figure 6. Transformer model.

Among the characteristics of a transformer:

Turns ratio is the ratio of the secondary- to the primary voltage.

Current ratio is inversely related to the turns ratio.

Impedance ratio is the square of the turns ratio.

Signal gain is ideally equal to the turns ratio. Although voltage gains are inherently noise-free, there are other considerations—to be discussed below.

A transformer can be viewed simplistically as a pass-band filter with nominal gain. **Insertion loss,** the filter's loss over the specified frequency range, is the most common measurement specification found in a data sheet, but there are additional considerations.

Return loss is a measure of the mismatch of the effective impedance of the secondary's termination as seen by the primary of a transformer. For example, if the square of the ratio of secondary to primary turns is 2:1, one would expect a 50-Ω impedance to be reflected onto the primary when the secondary is terminated with 100 Ω. However, this relationship is not exact; for example, the reflected impedance on the primary changes with frequency. In general, as the impedance ratio goes up, so does the variability of the return loss.

Amplitude- and **phase imbalance** are critical performance characteristics when considering a transformer. These two specifications give the designer a perspective on how much nonlinearity to expect when a design calls for very high (above 100-MHz) IF frequencies. As the frequency increases, the nonlinearities of the transformer also increase, usually dominated by phase imbalance, which translates to even-order distortions (mainly 2nd-harmonic).

Figure 7 shows typical phase imbalance as a function of frequency for single- and double-transformer configurations.

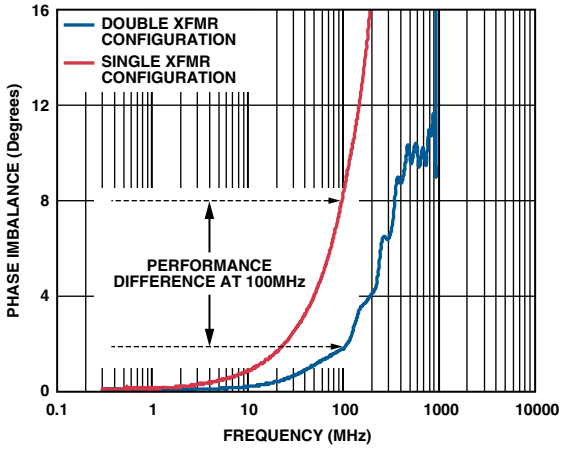


Figure 7. Transformer phase imbalance for single- and double-transformer configurations.

Remember, not all transformers are specified the same way by all manufacturers, and transformers with apparently similar specs may perform differently in the same situation. The best way to select a transformer for your design is to collect and understand the specs of all transformers being considered, and request any key data items not stated on manufacturers' data sheets. Alternatively, or in addition, it may be useful to measure their performance yourself using a network analyzer.

Q. *Which parameters are important in choosing an amplifier?*

A. The principal reason for using an amplifier instead of a transformer is to get better *pass-band flatness*. If this specification is critical to your design, an amplifier should produce less variability, typically ±0.1 dB over the frequency range. Transformers have lumpy response and require "fine tuning" when they must be used and flatness is an issue.

Drive capability is another advantage of amplifiers. Transformers are not made for driving long traces on PC boards. They are intended for direct connection to the ADC. If the system requirements dictate that the "driver/coupler" needs to be located far away from the ADC, or on a different board, an amplifier is strongly recommended.

DC coupling can also be a reason for using an amplifier, since transformers are inherently ac-coupled. Some high-frequency amplifiers can couple at frequencies all the way down to dc, if that part of the spectrum is important in the application. Typical amplifiers to consider include the AD8138 and ADA4937.

Amplifiers can also provide dynamic isolation, roughly 30 dB to 40 dB of reverse isolation, to squelch kickback glitches from current transients in an unbuffered ADC's input.

If the design calls for wideband gain, an amplifier provides a better match than a transformer to the ADC's analog inputs.

Another trade-off is bandwidth vs. noise. For designs involving frequencies greater than 150 MHz, transformers will do a better job of maintaining SNR and SFDR. However, within the first or second Nyquist zone, either a transformer or an amplifier can be used.

Q. *What are the preferred ADI amplifiers for driving high-performance ADCs?*

A. A handful of amplifiers are best for high-speed ADC front ends. These include the AD8138[6] and AD8139;[7] the AD8350,[8] AD8351,[9] and AD8352;[10] and the ADA4937 and ADA4938.

The AD8139 is commonly used for *baseband* designs, i.e., where input frequencies of interest are less than 50 MHz. For higher-IF designs the AD8352 is commonly used. This amplifier shows good noise- and spur rejection over a much wider band of frequencies, up to the 200-MHz region. The ADA4937 can be used for frequencies up to 150 MHz; its main advantage is in dc-coupled applications with ADCs, because it can handle a wide range of common-mode output voltages.

Q. *What are important characteristics of the ADCs that I might use?*

A. The popular CMOS switched-capacitor ADC does not have an internal input buffer, so it has much lower power dissipation than buffered types. The external source connects directly to the ADC's internal switched-capacitor sample-and-hold (SHA) circuit (Figure 8). This presents two problems. First, the input impedance varies with time and as the mode is switched between *sample* and *hold*. Second, the charge injected into the sampling capacitors reflects back onto the signal source; this may cause settling delays for passive filters in the drive circuit.

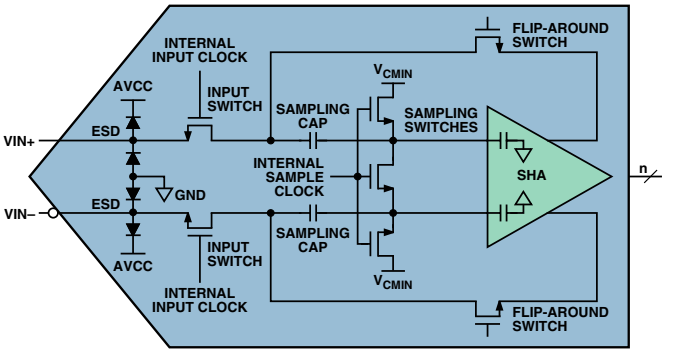


Figure 8. Block diagram of switched-capacitor ADC input stage.

It is important to match the external network to the ADC *track*-mode impedance, displayed in Figure 9. As you can see, the real (resistive) part of the input impedance (blue line) is very high (in the several kilohm range) at lower frequencies (baseband) and rolls off to less than 2 kΩ above 100 MHz.

The imaginary, or capacitive, part of the input impedance, the red line, starts out as a fairly high capacitive load and tapers off to about 3 pF (right-hand scale) at high frequencies.

To match to this input structure is a pretty challenging design problem, especially at frequencies greater than 100 MHz.

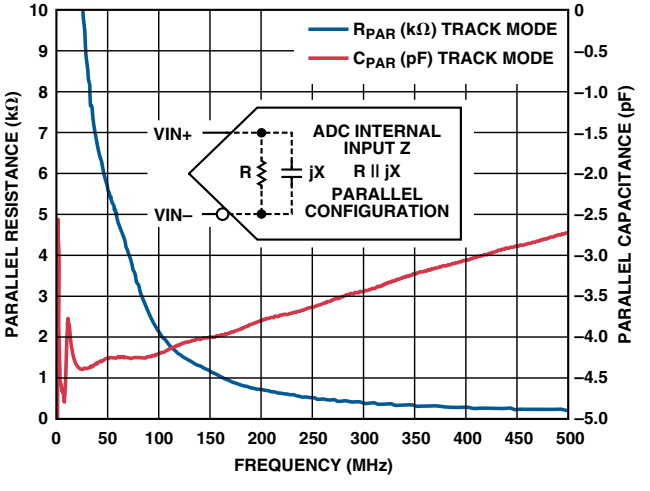


Figure 9. Typical input impedance graph of a switched-capacitor ADC in track mode.

The waveforms in Figures 10 and 11 illustrate the advantage of differential signaling. At first glance, the individual single-ended ADC input waveforms in Figure 10 look pretty bad. However, Figure 11 demonstrates that the corruption of the single-ended traces is almost purely a common-mode effect.

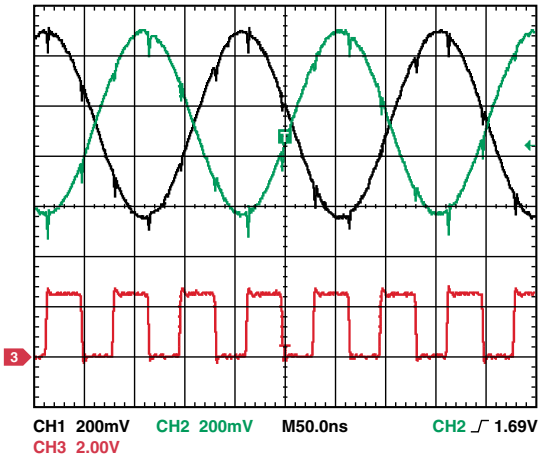


Figure 10. Single-ended measurement of a switched-capacitor ADC input relative to the clock edges.

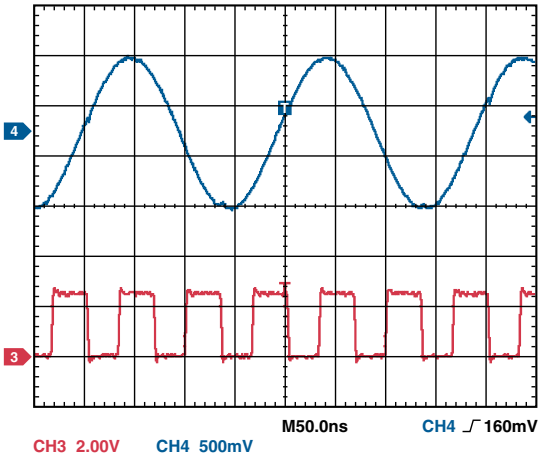


Figure 11. Differential measurement of a switched-capacitor ADC input relative to the clock edges.

Looking at the ADC inputs differentially (Figure 11), one can see that the input signal is much cleaner. The "corrupt" clock-related glitches are gone. The common-mode rejection inherent in differential signaling cancels out common-mode noise, whether from the supply, digital sources, or charge injection.

Buffered-input ADCs are easier to understand and use. The input source is terminated in a fixed impedance. This is buffered by a transistor stage that drives the conversion process at low impedance, so charge-injection spikes and switching transients are significantly reduced. Unlike switched-capacitor ADCs, the input termination has little variation over the ADC's analog input frequency range, so selection of the proper drive circuit is much easier. The buffer is specifically designed to be very linear and have low noise; its only downside is that its power consumption causes the ADC to dissipate more power overall.

Q. *Can you show me some examples of transformer and amplifier drive circuits?*

A. Figure 12 shows four examples of ADC input configurations using a transformer.

In baseband applications (a), the input impedance is much higher so the match is more straightforward than, and not as critical as, the match at higher frequencies. Usually, small-value series resistors will suffice to damp out the charge injection with a differentially connected capacitor. This simple filter attenuates the broadband noise, achieving optimal performance.

In order to get a well-matched input in broadband applications (b), try to make the input's real (resistive) component predominate. Minimize the capacitive terms with inductors or ferrite beads in shunt or series with the analog front end. This can yield good bandwidth, improve gain flatness, and provide better performance (SFDR) as seen using the AD92xx switched-capacitor ADC family.

For buffered high-IF applications (c), a double-balun configuration is shown, with a filter similar to the baseband configuration. This allows inputs of up to 300 MHz and provides good balancing to minimize even-order distortions.

For narrow-band (resonant) applications (d), the topology is similar to broadband. However, the match is in shunt instead of series, to narrow the bandwidth to the frequency specified.

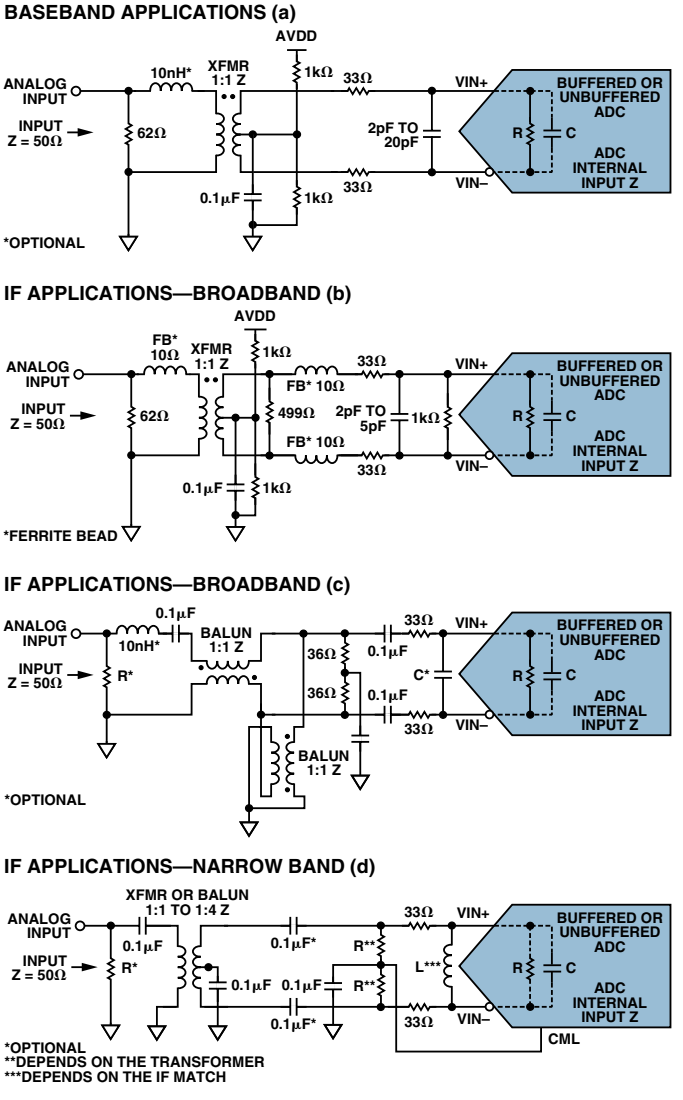


Figure 12. ADC front-end designs with transformer drive.

When using an *amplifier* with a buffered or unbuffered ADC in baseband applications, the design is fairly straightforward (Figure 13). Just make sure that the common-mode voltage of the amplifier is shared with the ADC, and use a simple low-pass filter to get rid of the unwanted broadband noise (a). For IF applications (b and c), the matching network is essentially similar to that in baseband, but usually has shallower roll-off. Inductors or ferrite beads can be used on the outputs of the amplifier to help extend the bandwidth if needed. This is not always necessary, however, because the amplifier's characteristics are less prone to changing over the band of interest than those of transformers. For narrow-band or resonant applications (d), the filter is matched to the output impedance of the amplifier to cancel the input capacitance of the ADC. Usually, a multipole filter is used to get rid of broadband noise outside the frequency region of interest.

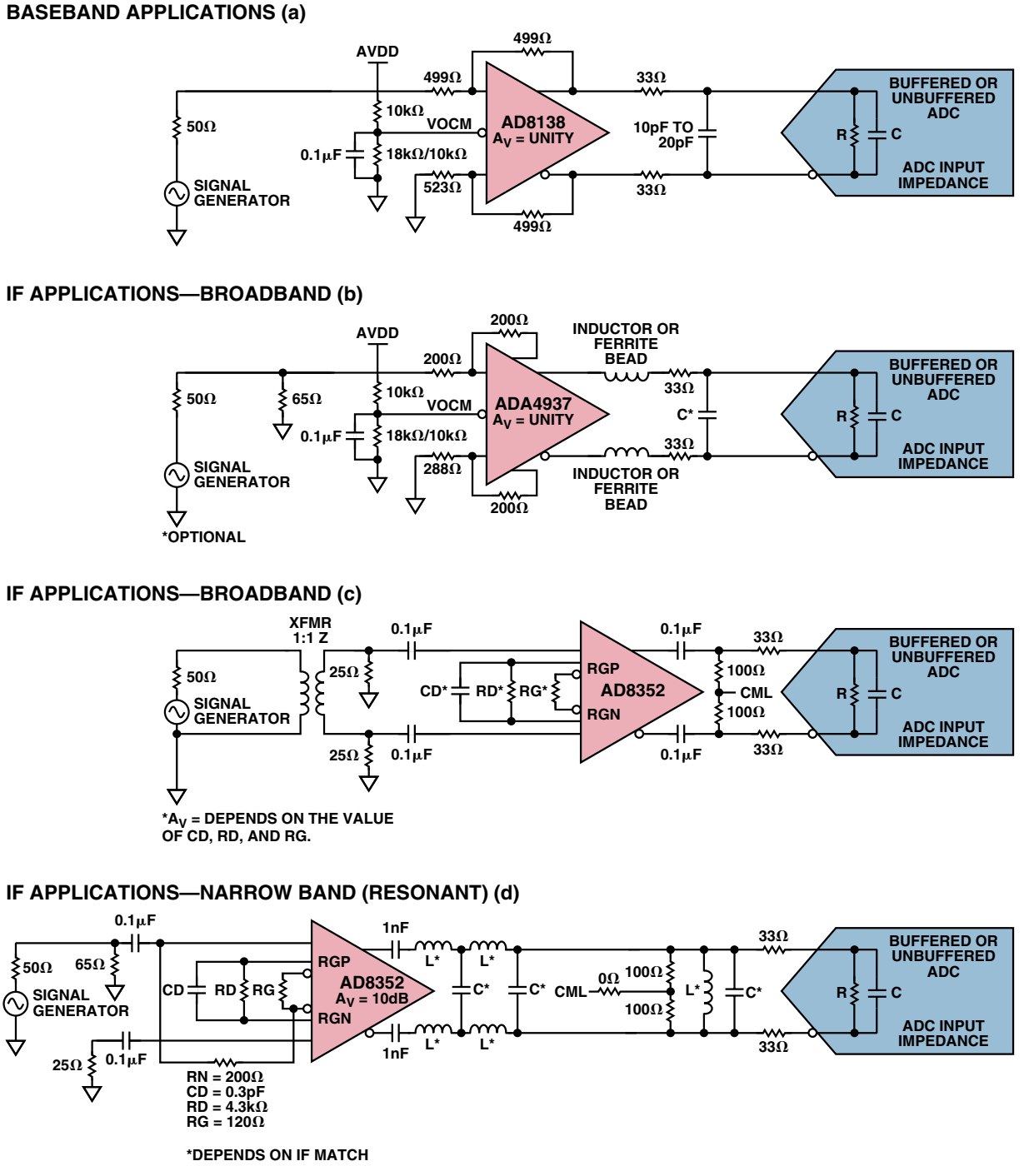


Figure 13. ADC front-end designs with amplifier drive.

Q. *Would you summarize the important points?*

A. When facing a new design, remember to:

- Understand the level of design difficulty.
- Rank the important parameters in your design.
- Include the ADC input impedance and the external components in the input circuit when determining the total load on the transformer or amplifier.

When choosing a transformer, always remember:

- Not all transformers are created equal.
- Understand transformer specifications.
- Ask the manufacturer for parameters that are not given, and/or do modeling.
- High-IF designs are sensitive to transformer phase imbalance.
- Two transformers or baluns may be needed for very high-IF designs to suppress the even-order distortions.

When choosing an amplifier, always remember:

- Note the noise specification.
- Understand amplifier specifications.
- For low-IF or baseband frequencies, use the AD8138/AD8139.
- For mid-IF, use the ADA4937.
- For high-IF designs, use the AD8352.
- Amplifiers are less sensitive to imbalance and automatically suppress even-order distortions.
- Some amplifiers can dc-couple to the ADC's input, e.g., the AD8138/AD8139 and ADA4937/ADA4938.
- Amplifiers inherently isolate the input source from output loading effects and can therefore be more useful than a transformer for dealing with sensitive input sources.
- Amplifiers can drive long distances and are especially useful when system partition dictates two or more boards in a design.
- Amplifiers may require another supply domain and will always add to system power requirements.

When choosing an ADC, always remember:

- Is the ADC internally buffered?
- Switched-capacitor ADCs have a time-varying input impedance and are more difficult to design with at high-IFs.
- If using an unbuffered ADC, always input-match in the *track* mode.
- Buffered ADCs are easier to design with, even at high IFs.
- Buffered ADCs tend to burn more power.

Finally:

- Baseband designs are the easiest with either ADC type.
- Use ferrite beads or low-Q inductors to tune out the input capacitance on switched-capacitor ADCs. This maximizes input bandwidth, creates a better input match, and maintains SFDR.
- Two transformers may be needed to deal with high IFs.

Q. *How about some references for further reading?*

A. Application Notes

AN-742, *Frequency-Domain Response of Switched-Capacitor ADCs.*

AN-827, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs.*

B. Papers

Reeder, Rob. "Transformer-Coupled Front-End for Wideband A/D Converters." *Analog Dialogue* 39-2. 2005. pp. 3-6.

Reeder, Rob, Mark Looney, and Jim Hand. "Pushing the State of the Art with Multichannel A/D Converters." *Analog Dialogue* 39-2. 2005. pp. 7-10.

Kester, Walt. "Which ADC Architecture Is Right for Your Application?" *Analog Dialogue* 39-2. 2005. pp. 11-18.

Reeder, Rob and Ramya Ramachandran. "Wideband A/D Converter Front-End Design Considerations—When to Use a Double Transformer Configuration." *Analog Dialogue* 40-3. 2006. pp. 19-22.

C. Technical Data

AD9246, 80-/105-/125-MSPS 14-Bit, 1.8-V, Switched-Capacitor ADC

AD9445 105-/125-MSPS 14-Bit, 5-/3.3-V, Buffered ADC

AD9446 16-Bit, 80-/100-MSPS Buffered ADC

AD8138 Low-Distortion Differential ADC Driver

AD8139 Ultralow Noise Fully Differential ADC Driver

AD8350 1.0-GHz Differential Amplifier

AD8351 Low-Distortion Fully Differential RF/IF Amplifier

AD8352 2-GHz Ultralow Distortion Differential RF/IF Amplifier

ADA4937 Ultralow Distortion Differential ADC Driver

ADA4938 Ultralow Distortion Differential ADC Driver

ADC Switched-Capacitor Input Impedance Data (S-parameters) for AD9215, AD9226, AD9235, AD9236, AD9237, AD9244, AD9245. Go to their Web pages, click on *Evaluation Boards*, upload Microsoft Excel spreadsheet.

REFERENCES—VALID AS OF APRIL 2007

[1]ADI website: www.analog.com (Search) ADA4937 (Go)
[2]ADI website: www.analog.com (Search) AD9446-80 (Go)
[3]ADI website: www.analog.com (Search) AD8352 (Go)
[4]ADI website: www.analog.com (Search) AD9246-125 (Go)
[5]ADI website: www.analog.com (Search) AD9235-20 (Go)
[6]ADI website: www.analog.com (Search) AD8138 (Go)
[7]ADI website: www.analog.com (Search) AD8139 (Go)
[8]ADI website: www.analog.com (Search) AD8350 (Go)
[9]ADI website: www.analog.com (Search) AD8351 (Go)
[10]ADI website: www.analog.com (Search) AD8352 (Go)

High-Speed Time-Domain Measurements—Practical Tips for Improvement

By John Ardizzoni [john.ardozzoni@analog.com]

Making accurate high-speed time-domain measurements can be challenging, but finding information that will help improve one's techniques shouldn't be. Understanding the basics of oscilloscopes and probes is always helpful, but a few extra tricks of the trade and some good old-fashioned commonsense engineering can be employed to help yield quick and accurate results. The following are some tips and techniques I've accumulated over the past 25 years. Incorporating even a few of these into your measurement kit could help improve your results.

Simply grabbing a scope off the shelf and a probe from the drawer won't do for high-speed measurements. When choosing the right scope and probe for high-speed measurement, first consider: *signal amplitude, source impedance, rise time,* and *bandwidth.*

Selecting Oscilloscopes and Probes

There are hundreds of oscilloscopes available, ranging from very simple portable models to dedicated rack-mount digital storage scopes that can cost hundreds of thousands of dollars (some high-end probes alone can cost upwards of $10,000). The variety of probes that accompany these scopes is also quite impressive, including passive, active, current-measuring, optical, high-voltage, and differential types. It is beyond the scope of this article to provide a complete and thorough description of each and every scope and probe category available, so we will focus on scopes for high-speed voltage measurements utilizing passive probes.

The scopes and probes discussed here are used to measure signals characterized by wide bandwidths and short rise times. Besides these specifications, one needs to know about the circuit's sensitivities to loading—resistive, capacitive, and inductive. Fast rise times can become distorted when high-capacitance probes are used; and in some applications, the circuit may not tolerate the presence of the probe at all (for example, some high-speed amplifiers will ring when capacitance is placed on their output). Knowing the circuit limitations and expectations will help you to select the right combination of scope and probe and the best techniques for using them.

To start, the signal bandwidth and rise time will limit the scope choices. A general guideline is that scope and probe bandwidth should be at least three to five times the bandwidth of the signal being measured.

Bandwidth

Whether the signal being measured occurs in an analog or a digital circuit, the scope needs to have enough bandwidth to faithfully reproduce the signal. For analog measurements, the highest frequency being measured will determine the scope bandwidth. For digital measurements, it is usually the rise time—not the repetition rate—that determines the required bandwidth.

The bandwidth of the oscilloscope is characterized by its –3 dB frequency, the point at which a sine wave's displayed amplitude has dropped to 70.7% of the input amplitude, that is

$$20 \log \frac{V_{OUT}}{V_{IN}} = 20 \log 0.707 = -3 \text{ dB} \quad (1)$$

It is important to ensure that the oscilloscope has sufficient bandwidth to minimize errors. Measurements should never be made at frequencies near the oscilloscope's –3 dB bandwidth, as this would introduce an automatic 30% amplitude error in a sine-wave measurement. Figure 1 is a convenient plot showing typical derating of amplitude accuracy vs. the ratio of the highest frequency being measured to scope bandwidth.

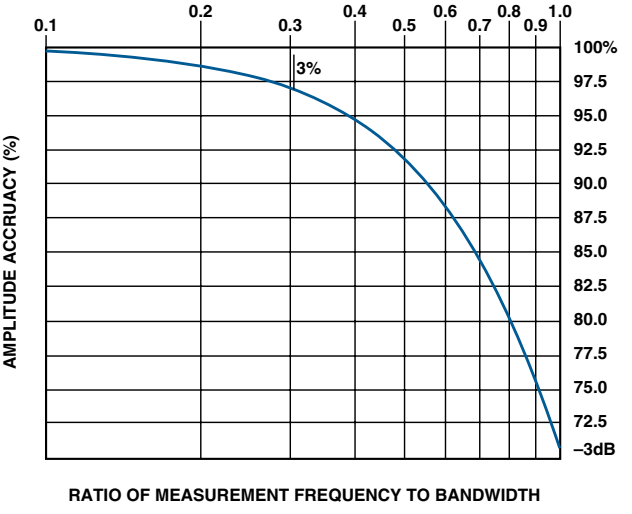


Figure 1. Derating plot.

For example, a 300 MHz scope will have up to 30% error at 300 MHz. In order to keep errors below the 3% mark, the maximum signal bandwidth that can be measured is about 0.3 × 300 MHz, or 90 MHz. Stated another way, to accurately measure a 100 MHz signal (<3% error), you need at least 300 MHz of bandwidth. The plot in Figure 1 illustrates a key point: to keep amplitude errors reasonable, the bandwidth of the scope and probe combination should be at least three to five times the bandwidth of the signal being measured. For amplitude errors to be less than 1%, the scope bandwidth needs to be at least five times the signal bandwidth.

For digital circuits, *rise time* is of particular interest. To ensure that the scope will faithfully reproduce rise times, the expected or anticipated rise time can be used to determine the bandwidth requirements of the scope. The relationship assumes the circuit responds like a single-pole, low-pass RC network, as shown in Figure 2.

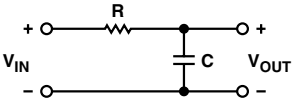


Figure 2. RC low-pass circuit.

In response to an applied voltage step, the output voltage can be calculated using Equation 2.

$$V_{OUT} = V_{IN}(1 - e^{-t/RC}) \quad (2)$$

The rise time in response to a step is defined as the time it takes for the output to go from 10% to 90% of the step amplitude. Using Equation 2, the 10% point of a pulse is 0.1 RC and the 90% point is 2.3 RC. The difference between them is 2.2 RC. Since the –3 dB bandwidth, f, is equal to $1/(2\pi RC)$, and the rise time, t_r, is 2.2 RC,

$$RC = \frac{1}{2\pi f} = \frac{t_r}{2.2}$$

$$\text{and thus } BW = f = \frac{2.2}{2\pi t_r} = \frac{1.1}{\pi t_r} = \frac{0.35}{t_r} \quad (3)$$

So, with a single-pole probe response, one can use Equation 3 to solve for a signal's equivalent bandwidth, knowing the rise time. For example, if a signal's rise time is 2 ns, the equivalent bandwidth is 175 MHz.

$$BW = \frac{0.35}{2\text{ ns}} = 175\text{ MHz} \quad (4)$$

To keep errors to 3%, the scope-plus-probe bandwidth should be at least three times faster than the signal being measured. Therefore a 600 MHz scope should be used to accurately measure a 2 ns rise time.

Probe Anatomy

Given their simplicity, probes are quite remarkable devices. A probe consists of a probe tip (which contains a parallel RC network), a length of shielded wire, a compensation network, and a ground clip. The probe's foremost requirement is to provide a noninvasive interface between the scope and the circuit—disturbing the circuit as little as possible, while allowing the scope to render a near-perfect representation of the signal being measured.

Probes got their start back in the days of vacuum tubes. For measurements at the grids and plates, a high impedance was required to minimize loading of the signal node. This principle is still important today. A high-impedance probe will not significantly load the circuit, thus providing an accurate picture of what is truly going on at the measurement node.

In my experience in the lab, the most commonly used probes are 10× and 1× passive probes; 10× active FET probes are a close second. The 10× passive probe attenuates the signal by a factor of 10. It has 10 MΩ input impedance and 10 pF typical tip capacitance. The 1× probe, with no attenuation, measures the signal directly. It has 1 MΩ input impedance, and tip capacitance as high as 100 pF. Figure 3 shows a typical schematic for a 10×, 10 MΩ probe.

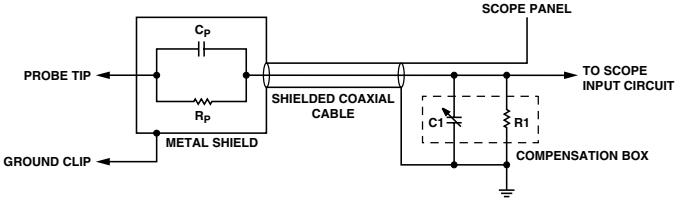


Figure 3. Probe schematic.

R_P (9 MΩ) and C_p are in the probe tip, R1 is the scope input resistance, and C1 combines the scope input capacitance and the capacitance in the compensation box of the probe. For accurate measurements, the two RC time constants (R_pC_p and R_1C_1) must be equal; imbalances can introduce errors in both rise time and amplitude. Thus, it is extremely important to always calibrate the scope and probe prior to making measurements.

Calibration

One of the first things that should be done after acquiring a working scope and probe is to *calibrate* the probe to ensure that its internal RC time constants are matched. Too often this step is skipped, as it is seen as unnecessary.

Figure 4 shows how to properly connect the probe to the probe compensation output of the scope. Calibration is accomplished by turning the adjustment screw on the compensation box with a nonmagnetic adjustment tool until a flat response is achieved.

Figure 4. Calibrating a scope probe.

Figure 5 shows the waveforms produced by a probe that is undercompensated, overcompensated, and properly compensated.

Note how an undercompensated or overcompensated probe can introduce significant errors in rise time and amplitude measurements. Some scopes have built-in calibrations. If your scope has one, make sure you run it before making measurements.

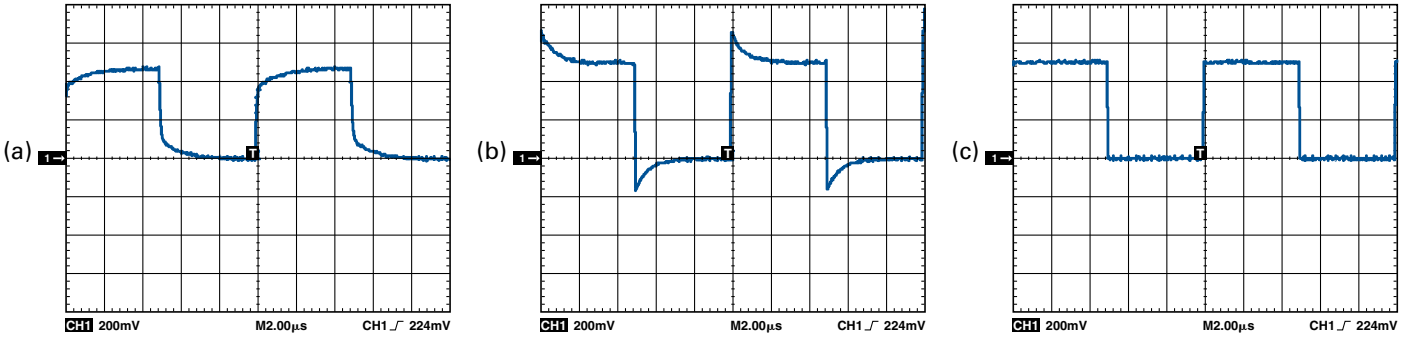


Figure 5. Probe compensation: a) undercompensated. b) overcompensated. c) properly compensated.

Ground Clips and High-Speed Measurements

Their inherent parasitic inductance makes ground clips and practical high-speed measurements mutually exclusive. Figure 6 shows a schematic representation of a scope probe with a ground clip. The probe LC combination forms a series resonant circuit—and resonant circuits are the basis of *oscillators*.

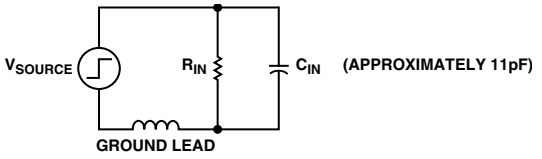


Figure 6. Equivalent probe circuit.

This added inductance is not a desirable feature, because the series-LC combination can add significant overshoot and ringing to an otherwise clean waveform. This ringing and overshoot often go unnoticed due to limited bandwidth of a scope. For example, if a signal containing a 200 MHz oscillation is measured with a 100 MHz scope, the ringing will not be visible, and the signal will be highly attenuated due to the limited bandwidth. Remember that, for a 100 MHz scope, Figure 1 showed 3 dB of attenuation at 100 MHz, with a continuing roll-off of 6 dB per octave. So the 200 MHz parasitic ringing will be down nearly 9 dB, a reduction to almost 35% of the original amplitude, making it difficult to see. With higher-speed measurements and wider-bandwidth scopes, however, the influence of ground clips is clearly visible.

The frequency of the ringing introduced by the ground clip can be approximated by calculating the series inductance of the ground clip using Equation 5. L is the inductance in nanohenrys, l is the length of the wire in inches, and d is the diameter of the wire in inches.

$$L(\text{nH}) = 5.08l\left(\ln\frac{4l}{d} - 1\right) \quad (5)$$

The result of Equation 5 can then be inserted into Equation 6 to calculate the resonant frequency, f (Hz). L is the inductance of the ground clip in henrys and C is the total capacitance (farads) at the node being probed—the probe capacitance plus any parasitic capacitance.

$$f = \frac{1}{2\pi\sqrt{LC}}\ \text{Hz} \quad (6)$$

Let's look at a few examples using different lengths of ground clips. In the first example, an 11 pF probe is used with a 6.5 inch ground clip to measure a fast-rising pulse edge. The result is shown in Figure 7. The pulse response at first glance looks clean, but upon closer inspection, a very low-level 100 MHz damped oscillation can be seen.

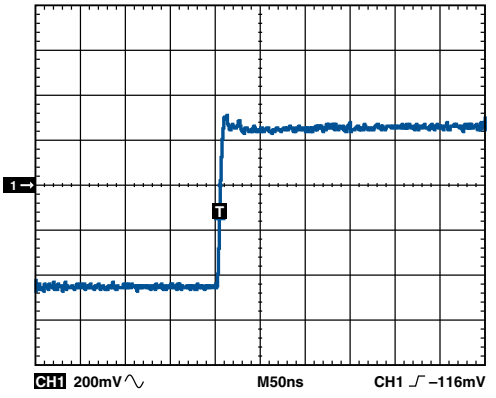


Figure 7. Measurement using 6.5 inch ground clip.

Let's substitute the physical features of the probe in Equations 5 and 6 to check if this 100 MHz oscillation is caused by the ground lead. The ground clip length is 6.5 inches and the diameter of the wire is 0.03 inches; this yields an inductance of 190 nH. Plugging this value into Equation 6, along with C = 13 pF (11 pF from the scope probe and 2 pF of stray capacitance) yields about 101 MHz. This good correlation with the observed frequency allows us to conclude that the 6.5 inch ground clip is the cause of the low-level oscillation.

Now consider a more extreme case, where a faster signal, with a 2 ns rise time, is applied. This is typically found on many high-speed PC boards. Using a TDS2000-series scope, Figure 8a shows that there is significant overshoot and prolonged ringing. The reason is that the faster rise time of 2 ns, with its bandwidth equivalent of 175 MHz, has more than enough energy to stimulate the 100 MHz series LC of the probe lead to ring. The overshoot and ringing is approximately 50% peak to peak. Such effects from typical grounds are clearly visible and are totally unacceptable in high speed measurements.

By eliminating the ground lead, the response to the applied input signal is shown with much better fidelity (Figure 8b).

Readying a Probe for High-Speed Measurements

In order to obtain meaningful scope plots, we need to rid the circuit of the ground clip and dismantle the probe. That's right, take that perfectly good probe apart! The first thing to discard is the press-on probe-tip adapter. Next, unscrew the plastic sleeve that surrounds the probe tip. Next to go is the ground clip. Figure 9 shows the before (a) and after (b) transformation of the scope probe. Figure 9c shows a measurement of a pulse generator's rising edge, using a 6-inch ground clip; and (d) shows the same measurement with the probe configured for high-speed measurements, as shown in 9b. The results, like those of Figure 8, can be dramatic.

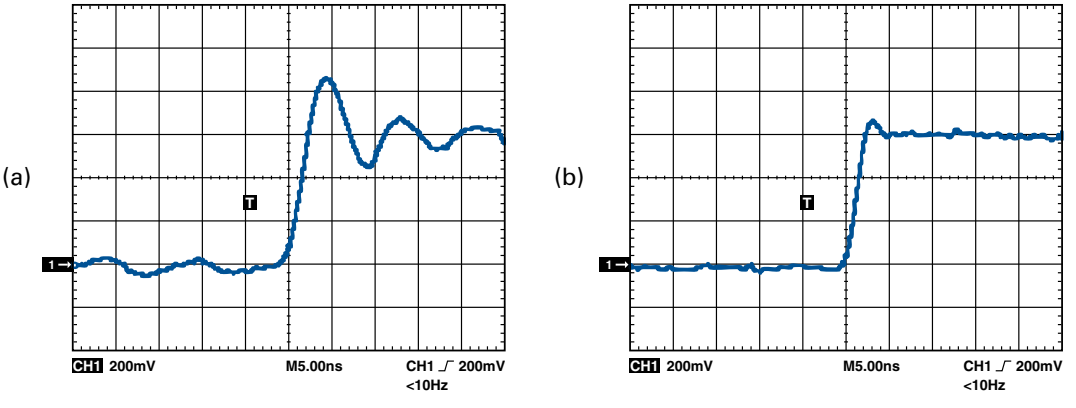


Figure 8. a) Response to step with 2 ns rise time with 6.5 inch ground clip. b) Step response with no ground lead.

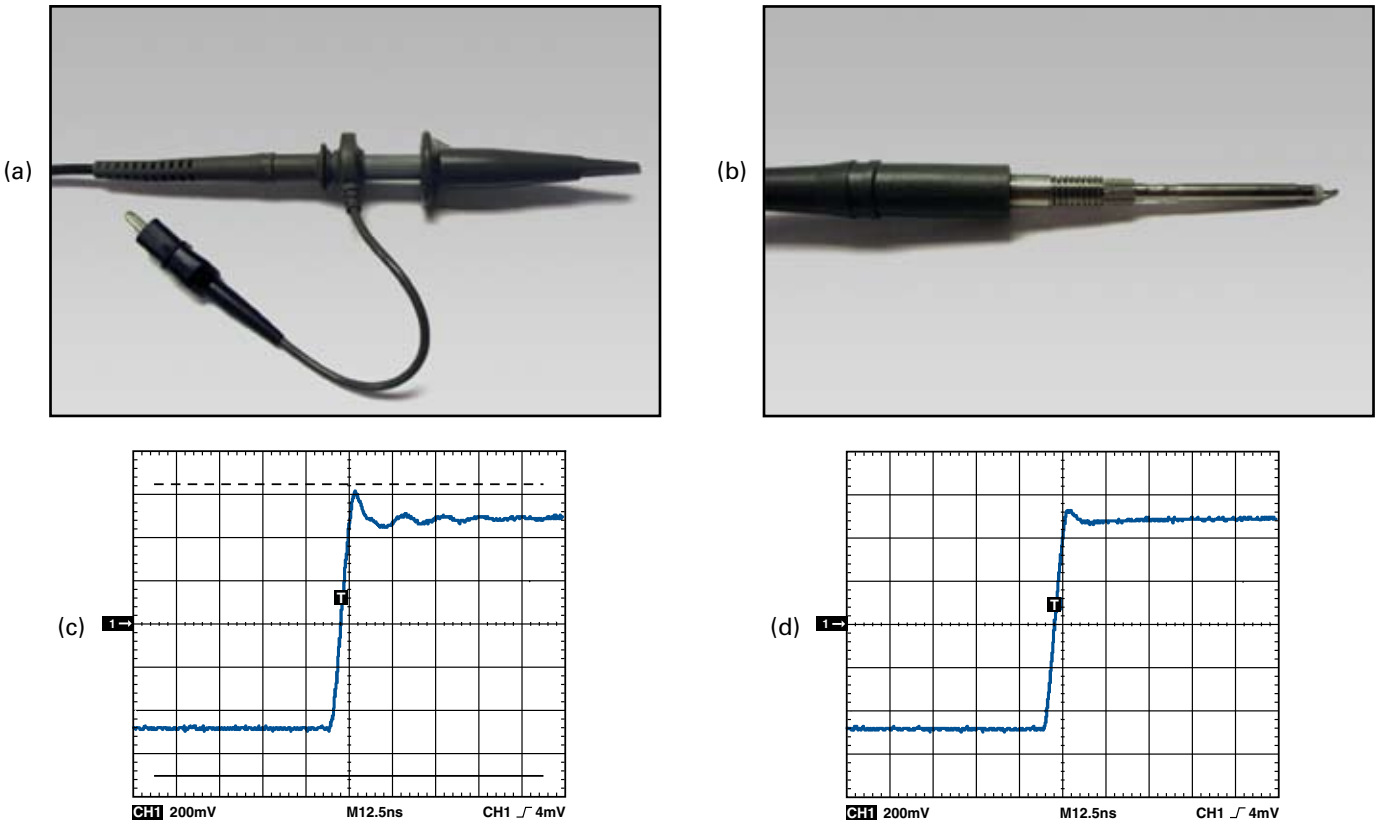


Figure 9. a) Probe right out of the box. b) Probe ready for high-speed measurements. c) Measurement with unmodified probe. d) Measurement with high-speed-ready probe.

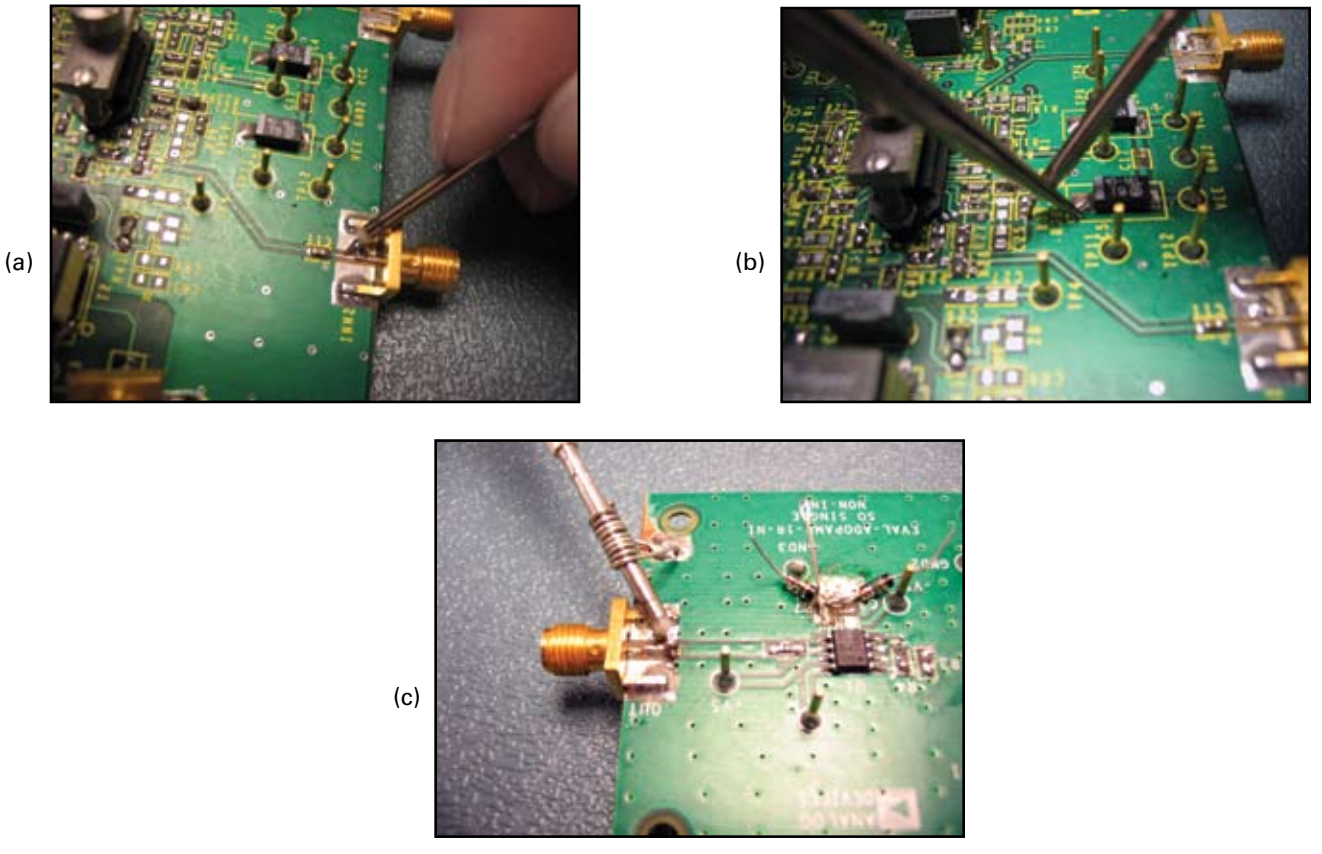


Figure 10. Grounding methods for stripped-down scope probe.

Next, the simplified stripped down probe needs to be calibrated (see Figure 4). Once calibrated, the probe is ready to use. Simply go to a test point and pick up a local ground on the outer metal shield of the probe. The trick is to pick up the ground connection right at the scope probe shield. This eliminates any of the series inductance introduced by using the supplied probe ground clip. Figure 10a shows the proper probing technique for using the streamlined probe. If ground can't be conveniently contacted, use a pair of metal tweezers, a small screwdriver, or even a paper clip to pick up the ground connection, as shown in Figure 10b. A length of bus wire can be wrapped around the tip, as shown in Figure 10c, to allow a little more flexibility and to enable probing of multiple points (within a small area).

Even better, if feasible, is to design in dedicated high-frequency test points on the board (Figure 11). Such probe-tip adaptors provide all of the above-mentioned advantages for using *naked* probe tips, offering the ability to measure numerous points quickly and accurately.

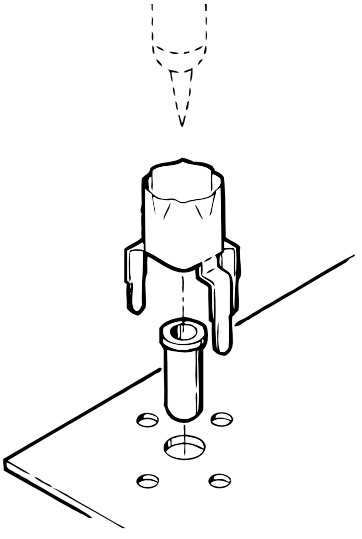


Figure 11. PCB-to-probe-tip adaptor.

Probe-Capacitance Effects

Probe capacitance affects rise time and amplitude measurements; it can also affect the stability of certain devices.

The probe capacitance adds directly to the node capacitance being probed. The added capacitance increases the node time constant, which slows down the rising and falling edges of a pulse. For example, if a pulse generator is connected to an arbitrary capacitive load, where $C_L = C_1$, as shown in Figure 12, then the associated rise time can be calculated from Equation 7, where R_S (= R_1, in Figure 12), is the source resistance.

$$t_r = 2.2R_SC_L \quad (7)$$

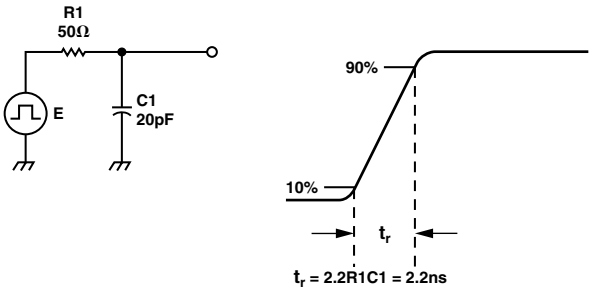


Figure 12. Rise time is determined by RC load.

If R_S = 50 Ω and C_L = 20 pF, then t_r = 2.2 ns.

Next, let's consider the same circuit probed with a 10 pF, 10× probe. The new circuit is shown in Figure 13. The total capacitance is now 31 pF and the new rise time is 3.4 ns, a more than 54% increase in rise time! Clearly this isn't acceptable, but what other choices are there?

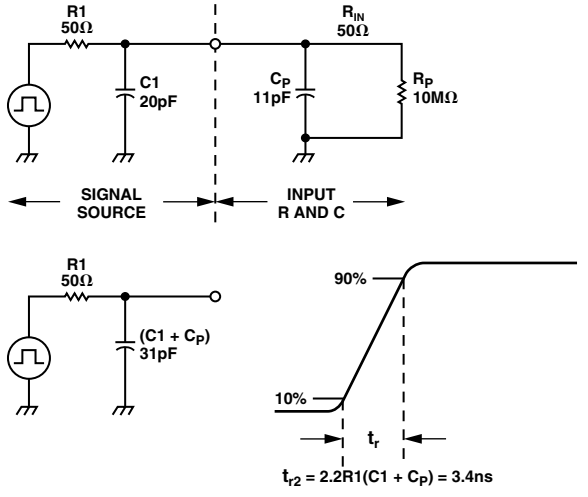


Figure 13. Added probe capacitance.

Active probes are another good choice for probing high speed circuits. Active, or FET, probes contain an active transistor (typically an FET) that amplifies the signal, compared to passive probes that attenuate the signal. The advantage of active probes is their extremely wide bandwidth, high input impedance, and low input capacitance. Another alternative is to use a scope probe with a high attenuation factor. Typically, higher-attenuation-factor probes have less capacitance.

Not only can the probe tip capacitance cause errors in rise time measurements; it can also cause some circuits to ring, overshoot, or, in extreme cases, become unstable. For example, many high-speed operational amplifiers are sensitive to the effects of capacitive loading at their output and at their inverting input.

When capacitance (in this case, the scope probe tip) is introduced at the output of a high-speed amplifier, the amplifier's output resistance and the capacitance form an additional pole in the feedback response. The pole introduces phase shift and lowers the amplifier's phase margin, which can lead to instability. This loss of phase margin can cause ringing, overshoot, and oscillations. Figure 14 shows the output of a high-speed amplifier being probed with a Tektronix P61131 10 pF, 10× scope probe, using proper high-speed grounding. The signal has a 1300 mV overshoot with 12 ns of sustained ringing. Obviously, this is not the right probe for this application.

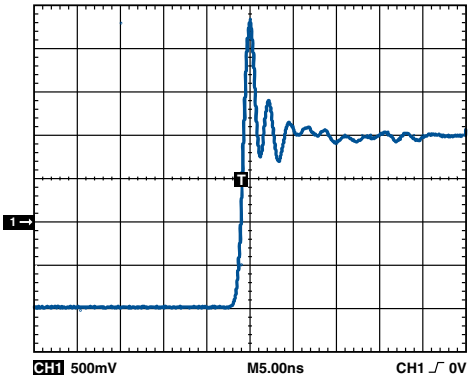


Figure 14. High-speed amplifier output probed with 10 pF probe.

Fortunately, there are a few solutions to this problem. First, use a lower-capacitance probe. In Figure 15, a Tektronix P6204 1.1 GHz *active* 10× FET probe, with 1.7 pF, is used to make the same measurement as is shown in Figure 14, again with proper high-speed grounding.

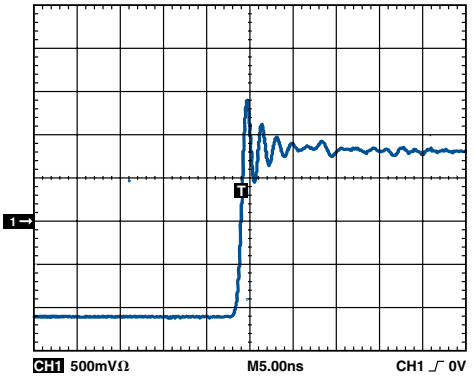


Figure 15. 1.7 pF FET probe at high-speed amplifier output.

In this case, there is significantly lower overshoot (600 mV) and ringing (5 ns) using the lower capacitance active probe.

Another technique is to include a small amount of series resistance, (typically 25 Ω to 50 Ω) with the scope probe. This will help isolate the capacitance from the amplifier output and will lessen the ringing and overshoot.

Propagation Delay

An easy way to measure propagation delay is to probe the device under test (DUT) at its input and output simultaneously. The propagation delay can be readily read from the scope display as the time difference between the two waveforms.

When measuring short propagation delays (<10 ns), however, care must be taken to ensure that both scope probes are the same length. Since the propagation delay in wire is approximately 1.5 ns/ft, sizeable errors can result from pairing probes of different lengths. For example, measuring a signal's propagation delay using a 3-ft probe and a 6-ft probe can introduce approximately 4.5 ns of delay error—a significant error when making single- or double-digit nanosecond measurements.

If two probes of equal length are not available (often the case), do the following: Connect both probes to a common source (e.g., a pulse generator) and record the propagation delay difference. This is the "calibration factor." Then correct the measurement by subtracting this number from the longer-probe reading.

CONCLUSION

While high-speed testing is not overly complicated, numerous factors must be considered when venturing into the lab to make high-speed time-domain measurements. Bandwidth, calibration, rise-time-measuring scope and probe selection, and probe-tip and ground-lead lengths all play important roles in the quality and integrity of measurements. Employing some of the techniques mentioned here will help speed up the measurement process and improve the overall quality of results. For more information, visit www.analog.com and www.tek.com.

REFERENCES

[1] *ABC's of Probes Primer*. Tektronix, Inc. 2005.

[2] Mittermayer, Christoph and Andreas Steininger. "On the Determination of Dynamic Errors for Rise-Time Measurement with an Oscilloscope." *IEEE Transactions on Instrumentation and Measurement*, 48-6. December 1999.

[3] Millman, Jacob and Herbert Taub. *Pulse, Digital, and Switching Waveforms*. McGraw-Hill, 1965. ISBN 07-042386-5.

[4] *The Effect of Probe Input Capacitance on Measurement Accuracy*. Tektronix, Inc. 1996.

ACKNOWLEDGEMENT

Figures 1, 6, 7, 8, 11, 12, and 13 appear courtesy of Tektronix, Inc., with permission.

PRODUCT INTRODUCTIONS: VOLUME 41, NUMBER 1

Data sheets for all ADI products can be found by entering the model number in the Search box at www.analog.com

January

ADC, Pipelined, 14-bit, 150-MSPS, 1.8-V operation **AD9254**
ADC, Pipelined, octal, 10-bit, 40-/65-MSPS, LVDS outputs **AD9212**
ADC, Pipelined, octal 14-bit, 50-MSPS, LVDS output **AD9252**
ADC, Successive-Approximation, 16-bit, 250-kSPS, 1.5-LSB INL .. **AD7610**
ADC, Successive-Approximation, 14-bit, 1-MSPS, 1-LSB INL **AD7951**
Amplifier, Operational, 4-MHz, rail-to-rail outputs, 16-V operation **AD8665**
Amplifier, Operational, dual, low-noise, high-precision, 36-V operation **AD8676**
Amplifiers, Operational, dual/quad, low-power, high-speed, JFET-input **AD8682/AD8684**
Amplifier, Variable-Gain, wideband, dc-coupled, 60-dB gain range **AD8336**
Amplifier, Video, triple, low-power, 100-nA disable current **ADA4853-3**
Audio Processors, SigmaDSP®, 28-/56-bit, two ADCs, four DACs **ADAU1701/ADAU1702**
Codecs, SoundMAX, high-definition audio **AD1988A/AD1988B**
Codec, Video, JPEG2000 ..... **ADV212**
Comparators, Voltage, very fast, rail-to-rail, single-supply **ADCMP60x**
Converter, Synchronous Buck, 2-/3-/4-phase, 6-bit VID, AMD ... **ADP3196**
Converter, Synchronous Buck, 2-/3-/4-phase, 6-bit VID, Intel **ADP3194**
Detector, Threshold, high-voltage **AD8214**
Driver, LED, dual-interface flash/torch **ADP1653**
Driver, Line, high-speed, current-feedback **ADA4310-1**
Driver, Line, quad, current-feedback ADSL/ADSL2+ **AD8392A**
Encoders, Video, multiformat, six video DACs **ADV734x**
Encoders, Video, multiformat, 10-bit, low-power, three video DACs **ADV739x**
Gyroscope, *i*MEMS®, low-power, programmable **ADIS16250**
Isolators, Digital, 2-channel, I²C®, hot-swappable ... **ADuM1250/ADuM1251**
Isolators, Digital, 4-channel, programmable default output **ADuM141x**
Modulator, Quadrature, 300-MHz to 1-GHz **ADL5370**
Modulator, Quadrature, 50-MHz to 2.2-GHz **ADL5385**
Multiplexers, Video, triple 2:1, fast-switching, wideband **AD8188/AD8189**
Processors, SHARC, 32-/40-bit, floating-point, high-performance audio **ADSP-2136x**
Receiver, Differential, triple, high-speed, on-chip auxiliary comparators **AD8145**
Reference, Voltage, precision, 0.5-V/1.0-V, TSOT package **ADR130**
Regulators, Low-Dropout, 150-mA loads **ADP1710/ADP1711**
Signal Processor, CCD, on-chip V-driver and timing generator..... **AD9923A**
Splitter, Signal, 1:2, single-ended, CATV **ADA4303-2**
Switches, CMOS, SPST, wideband, low-voltage **ADG701L/ADG702L**
Switches, *i*CMOS, triple/quad SPDT, 4-ohm **ADG1433/ADG1434**
Transceivers, RS-485/RS-422, 16-Mbps, extended ESD protection **ADM307xE**
Transceivers, RS-485/RS-422, 250-kbps, extended ESD protection **ADM3483E/ADM3488E**
Transmitter, HDMI/DVI, high-performance **AD9389A**

February

ADC, Successive-Approximation, 16-bit, 500-kSPS, 0.5-LSB INL .. **AD7693**
Amplifier, Audio, 1.4-W, Class-D, filterless, monophonic **SSM2301**
Amplifier, Audio, 2-W, Class-D, filterless, stereo **SSM2304**
Controller, Capacitive Touch Sensor, programmable **AD7143**
DAC, Voltage-Output, dual 12-/16-bit, I²C interface **AD5627/AD5667**
DAC, Voltage-Output, dual 12-/14-/16-bit, on-chip reference **AD5627R/AD5647R/AD5667R**
Modulator, Quadrature, 1500-MHz to 2500-MHz **ADL5372**
Transceiver, RS-232, 460-kbps, ESD-protected, single-supply **ADM3232E**

March

ADC, Pipelined, 12-bit, 170-/210-/250-MSPS, 1.8-V supply **AD9230**
ADC, Successive-Approximation, 18-bit, 250-kSPS, 2.5-LSB INL ... **AD7631**
ADC, Successive-Approximation, 18-bit, 670-kSPS, 2.5-LSB INL .. **AD7634**
ADC, Successive-Approximation, 14-bit, 1-MSPS, 1-LSB INL **AD7952**
Amplifier, Instrumentation, dual, JFET-input, rail-to-rail outputs .. **AD8224**
Amplifier, Instrumentation, programmable-gain, 10-MHz bandwidth **AD8250**
Amplifier, Operational, dual, ultralow noise and distortion **AD8599**
Amplifiers, Operational, dual/quad, CMOS, micropower .. **AD8502/AD8504**
Amplifiers, Operational, dual/quad, JFET-Input **ADTL082/ADTL084**
Codecs, SoundMAX, high-definition audio **AD1884/AD1984**
Converter, Capacitance-to-Digital, 24-bit, on-chip temperature sensor **AD7747**
Converter, Resolver-to-Digital, 12-bit, on-chip reference oscillator **AD2S1205**
Isolators, Digital, 3-channel **ADuM1310/ADuM1311**
Modulator, Quadrature, 500-MHz to 1500-MHz **ADL5371**
References, Voltage, shunt-mode, micropower, precision **ADR504x**
Regulators, Low-Dropout, 300-mA loads **ADP1712/ADP1713/ADP1714**
Signal Processor, CCD, 14-bit, on-chip timing generator **AD9979**
Signal Processors, CCD, dual, 14-bit, on-chip timing generator **AD9974/AD9977**
Switch, CMOS, dual, SPDT, low-voltage..... **ADG736L**
Switch, Crosspoint, 16 × 8, audio/video, buffered, 60 MHz **AD8112**
Switch, Crosspoint, 32 × 32, video, buffered, 500 MHz **AD8117**
Switches, *i*CMOS, dual SPST, low capacitance, low charge injection **ADG1221/ADG1222/ADG1223**
Switch, HDMI/DVI, 2:1, on-chip equalization and pre-emphasis **AD8196**
Transceiver, RS-485, isolated, high-speed, on-chip transformer driver **ADM2485**
Transceiver, RS-485/RS-422, 250-kbps, half-duplex, ESD-protected **ADM487E**
Transceivers, RS-485/RS-422, 2.5-Mbps, half-duplex, ESD-protected **ADM485E/ADM1487E**

AUTHORS

John Ardizzoni (page 13) is an applications engineer in ADI's High-Speed Amplifier group. John graduated from Merrimack College in 1988 and joined Analog Devices in 2002. Prior to that, he worked for IBM as an applications engineer and for M/A-COM as a design engineer.

Jim Caserta (page 6) is a design engineer in the ASC Technology group. He received BS and MS degrees in electrical engineering from the University of Florida. Before joining ADI, he worked at Motorola Semiconductor (now Freescale) as a mixed-signal designer, and then at the University of Florida Department of Radiology as an RF engineer. He holds one patent and has authored or co-authored nearly a dozen journal and conference publications.

Rob Reeder (page 6) is a senior converter applications engineer in ADI's High-Speed Converters group in Greensboro, NC. Earlier, he was a designer in a mixed-signal module group for military and space applications. Rob received his BSEE and MSEE in 1996 and 1998 from Northern Illinois University. He has published numerous papers on converters and converter testing. In his spare time, he enjoys mixing music, art-airbrushing, and having fun with his two sons.

Colm Slattery (page 3) graduated in 1995 from the University of Limerick, Ireland, with a bachelor's degree in electronic engineering. After working in test-development engineering at Microsemi, he joined ADI in 1998 as a test-development engineer. In 2001, Colm became an applications engineer for the Precision-Data-Converter product line and is currently based in Shanghai, China.

Analog Devices, Inc.
Worldwide Headquarters
Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA
02062-9106 U.S.A.
Tel: 781.329.4700
(800.262.5643,
U.S.A. only)
Fax: 781.461.3113

Analog Devices, Inc.
Europe Headquarters
Analog Devices, Inc.
Wilhelm-Wagenfeld-Str. 6
80807 Munich
Germany
Tel: 49.89.76903.0
Fax: 49.89.76903.157

Analog Devices, Inc.
Japan Headquarters
Analog Devices, KK
New Pier Takeshiba
South Tower Building
1-16-1 Kaigan, Minato-ku,
Tokyo, 105-6891
Japan
Tel: 813.5402.8200
Fax: 813.5402.1064

Analog Devices, Inc.
Southeast Asia
Headquarters
Analog Devices
22/F One Corporate Avenue
222 Hu Bin Road
Shanghai, 200021
China
Tel: 86.21.5150.3000
Fax: 86.21.5150.3222

Printed in the U.S.A. M02000411-56-4/07

www.analog.com/analogdialogue

ANALOG DEVICES