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In This Issue

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ANALOG DEVICES

Editors' Note

The outpourings of our authors have taken up all of the space in this issue, so you'll have to wait with bated breath for future erudite comments from your Editors. See you next quarter. Meanwhile, as usual, your comments are welcome.

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Analog Dialogue

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PRODUCT INTRODUCTIONS: VOLUME 41, NUMBER 4

Data sheets for all ADI products can be found by entering the model number in the Search box at www.analog.com.

October

Demodulator, Quadrature-, and Phase Shifter, 4-channel **AD8339**
Generators, Clock, 6-output, on-chip VCO **AD9518-x**
Monitor, Remote Thermal-, and Fan Controller **ADT7490**
Sensor, Inertial, 3-axis..... **ADIS16350**
Switch, CMOS SPDT, dual, low-power, routes USB signals... **ADG772**

November

Controller, DC-to-DC, step-down, synchronous PWM .. **ADP1828**
Converter, Capacitance-to-Digital, single-electrode sensors..... **AD7147**
Demodulator, Quadrature, 50 MHz to 2 GHz..... **ADL5387**
Monitor, Voltage, supervises three microprocessors..... **ADM13307**
Monitor, Voltage, watchdog, supervises two microprocessors..... **ADM13305**
Synthesizer, Direct Digital, 14-bit, 1-GSPS **AD9912**
Synthesizer, Frequency, high-resolution, fractional-N, 6 GHz **ADF4157**
Trip Points, Temperature, micropower, SOT-23 package..... **ADT6501/ADT6502**

December

Amplifier, Difference, wideband, broad common-mode voltage range..... **AD8216**
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Amplifier, Operational, dual, micropower, zero crossover distortion **AD8506**
Amplifier, Operational, dual, rail-to-rail, low-power shutdown **AD8647**
Amplifier, Operational, precision, rail-to-rail, 5-V to 16-V supply **AD8638**
Amplifiers, Operational, precision voltage reference **ADR821/ADR827**
Amplifier, Operational, quad, CMOS, low-noise, precision ... **AD8669**
Amplifier, Operational, current-feedback, ADSL/ADSL2+ line-driver **AD8394**
Amplifier, Variable-Gain, dual, 41-dB gain range, 1-dB steps..... **AD8372**
ADC, Pipelined, 10-bit, 200-/250-MSPS, 1.8-V supply **AD9601**
ADC, Pipelined, 12-bit, 170-/210-/250-MSPS, 1.8-V supply... **AD9626**
ADC, Pipelined, dual, 10-bit, 105-/125-/150-MSPS, 1.8-V supply..... **AD9600**
ADC, Pipelined, dual, 11-bit, 105-/150-MSPS, 1.8-V supply **AD9627-11**
ADC, Pipelined, dual, 12-bit, 80-/105-/125-/150-MSPS, 1.8-V supply..... **AD9627**
ADCs, Successive-Approximation, 16-/18-bit, 1.33-MSPS..... **AD7983/AD7984**
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Decoder, Video, RGB Graphics Digitizer, and HDMI/DVI Interface, SDTV/HDTV..... **ADV7441A**
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Receiver, IF Diversity, 14-bit, 80-/105-/125-/150-MSPS..... **AD6655**
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Switch, HDMI/DVI, 4:1, equalization, pre-emphasis, 2.25 Gbps **AD8197A**
Switch, TMDS, 2:1, buffered..... **AD8193**
Switch, TMDS, 2:1, buffered, equalization **AD8194**
Synthesizer, Direct Digital, low-power, 10-bit, 250-MSPS ... **AD9913**
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Transmitter, HDMI/DVI, high-performance, low-power..... **AD9387NK**

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Phase Relations in Active Filters

By Hank Zumbahlen [hank.zumbahlen@analog.com]

In applications that use filters, the amplitude response is generally of greater interest than the phase response. But in some applications, the phase response of the filter is important. An example of this might be where a filter is an element of a process control loop. Here the total phase shift is of concern, since it may affect loop stability. Whether the topology used to build the filter produces a sign inversion at some frequencies can be important.

It might be useful to visualize the active filter as two cascaded filters. One is the ideal filter, embodying the transfer equation; the other is the amplifier used to build the filter. This is illustrated in Figure 1. An amplifier used in a closed negative-feedback loop can be considered as a simple low-pass filter with a first-order response. The gain rolls off with frequency above a certain breakpoint. In addition, there will be, in effect, an additional 180° phase shift at all frequencies if the amplifier is used in the inverting configuration.

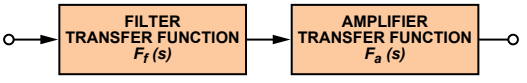

Figure 1. Filter as cascade of two transfer functions.

Filter design is a two-step process. First, the filter response is chosen; then, a circuit topology is selected to implement it. The filter response refers to the shape of the attenuation curve. Often, this is one of the classical responses such as Butterworth, Bessel, or some form of Chebyshev. Although these response curves are usually chosen to affect the amplitude response, they will also affect the shape of the phase response. For the purpose of the comparisons in this discussion, the amplitude response will be ignored and considered essentially constant.

Filter complexity is typically defined by the filter "order," which is related to the number of energy storage elements (inductors and capacitors). The order of the filter transfer function's denominator defines the attenuation rate as frequency increases. The asymptotic filter rolloff rate is $-6n$ dB/octave or $-20n$ dB/decade, where n is the number of poles. An *octave* is a doubling or halving of the frequency; a *decade* is a tenfold increase or decrease of frequency. So a first-order (or single-pole) filter has a rolloff rate of –6 dB/octave or –20 dB/decade. Similarly, a second-order (or 2-pole) filter has a rolloff rate of –12 dB/octave or –40 dB/decade. Higher-order filters are usually built up of cascaded first- and second-order blocks. It is, of course, possible to build third- and, even, fourth-order sections with a single active stage, but sensitivities to component values and the effects of interactions among the components on the frequency response increase dramatically, making these choices less attractive.

The Transfer Equation

First, we will take a look at the phase response of the transfer equations. The phase shift of the transfer function will be the same for all filter options of the same order.

For the single-pole, low-pass case, the transfer function has a phase shift, ϕ, given by

$$\phi(\omega) = \tan^{-1}\left(\frac{\omega}{\omega_0}\right) \qquad (1)$$

where: ω = frequency (radians per second)
ω_0 = center frequency (radians per second)

Frequency in radians per second is equal to 2π times frequency in Hz (f), since there are 2π radians in a 360° cycle. Because the expression is a dimensionless ratio, either f or ω could be used.

The center frequency can also be referred to as the *cutoff* frequency (the frequency at which the amplitude response of the single-pole, low-pass filter is down by 3 dB—about 30%). In terms of phase, the center frequency will be at the point at which the phase shift is 50% of its ultimate value of –90° (in this case). Figure 2, a semi-log plot, evaluates Equation 1 from two decades below to two decades above the center frequency. The center frequency (=1) has a phase shift of –45°.

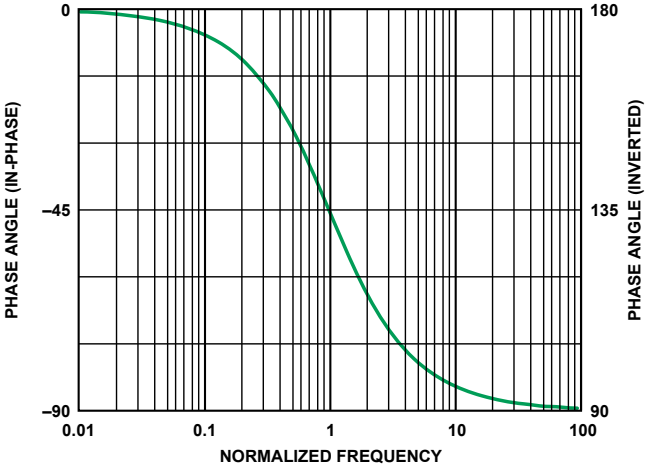

Figure 2. Phase response of a single-pole, low-pass filter about the center frequency (in-phase response, left axis; inverted response, right axis).

Similarly, the phase response of a single-pole, high-pass filter is given by

$$\phi(\omega) = \frac{\pi}{2} - \tan^{-1}\left(\frac{\omega}{\omega_0}\right) \qquad (2)$$

Figure 3 evaluates Equation 2 from two decades below to two decades above the center frequency. The normalized center frequency (=1) has a phase shift of +45°.

It is evident that the high-pass and the low-pass phase responses are similar, only shifted by 90° ($\pi/2$ radians).

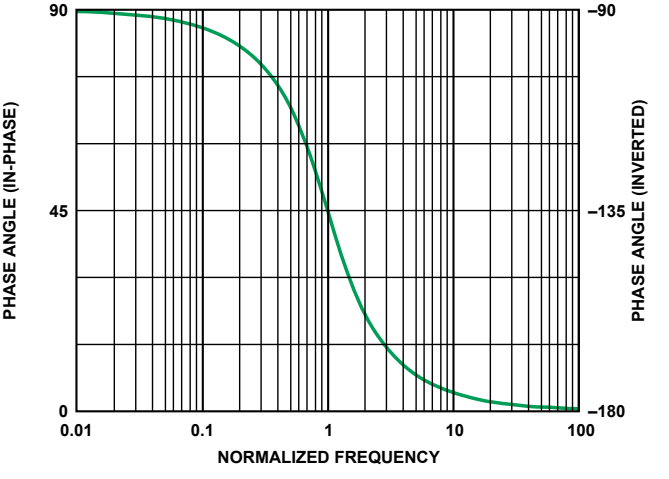

Figure 3. Phase response of a single-pole, high-pass filter with a center frequency of 1 (in-phase response, left axis; inverted response, right axis).

For the second-order, low-pass case, the transfer function has a phase shift that can be approximated by

$$\phi(\omega) = \tan^{-1}\left[\frac{1}{\alpha}\left(2\frac{\omega}{\omega_0} + \sqrt{4-\alpha^2}\right)\right] - \tan^{-1}\left[\frac{1}{\alpha}\left(2\frac{\omega}{\omega_0} - \sqrt{4-\alpha^2}\right)\right] \quad (3)$$

where α is the damping ratio of the filter. It will determine the peaking in the amplitude response and the sharpness of the phase transition. It is the inverse of the *Q* of the circuit, which also determines the steepness of the amplitude rolloff or phase shift. The Butterworth has an α of 1.414 (*Q* of 0.707), producing a maximally flat response. Lower values of α will cause peaking in the amplitude response.

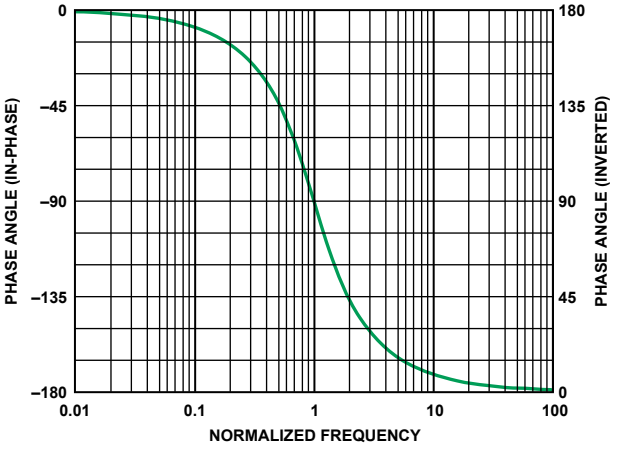

Figure 4. Phase response of a 2-pole, low-pass filter with a center frequency of 1 (in-phase response, left axis; inverted response, right axis).

Figure 4 evaluates this equation (using α = 1.414) from two decades below to two decades above the center frequency. Here the center frequency (=1) shows a phase shift of –90°.

The phase response of a 2-pole, high-pass filter can be approximated by

$$\phi(\omega) = \pi - \tan^{-1}\left[\frac{1}{\alpha}\left(2\frac{\omega}{\omega_0} + \sqrt{4-\alpha^2}\right)\right] + \tan^{-1}\left[\frac{1}{\alpha}\left(2\frac{\omega}{\omega_0} - \sqrt{4-\alpha^2}\right)\right] \quad (4)$$

In Figure 5 this equation is evaluated (again using α = 1.414), from two decades below to two decades above the center frequency (=1), which shows a phase shift of –90°.

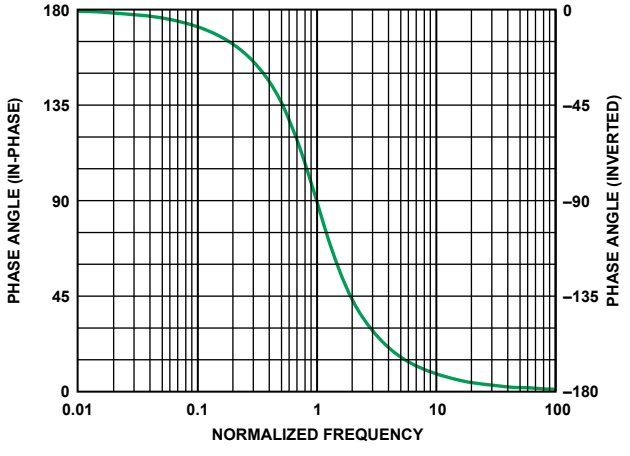

Figure 5. Phase response of a 2-pole, high-pass filter with a center frequency of 1 (in-phase response, left axis; inverted response, right axis).

Again, it is evident that the high-pass and low-pass phase responses are similar, just shifted by 180° (π radians).

In higher-order filters, the phase response of each additional section is cumulative, adding to the total. This will be discussed in greater detail later. In keeping with common practice, the displayed phase shift is limited to the range of ±180°. For example, –181° is really the same as +179°, 360° is the same as 0°, and so on.

First-Order Filter Sections

First-order sections can be built in a variety of ways. The most straightforward way is illustrated in Figure 6, simply using a passive R-C configuration. The center frequency of this filter is 1/(2πRC). It is commonly followed by a noninverting buffer amplifier to prevent loading by the circuit following the filter, which could alter the filter response. In addition, the buffer can provide some drive capability. The phase will vary with frequency as shown in Figure 2, with 45° phase shift at the center frequency, exactly as predicted by the transfer equation, since there are no extra components to modify the phase shift. That response will be referred to as the *in-phase, first-order, low-pass response*. The buffer will add no phase shift, as long as its bandwidth is significantly greater than that of the filter.

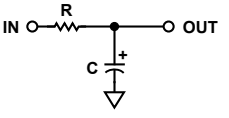

Figure 6. Passive, low-pass filter.

Remember that the frequency in these plots is *normalized*, i.e., the ratio to the center frequency. If, for example, the center frequency were 5 kHz, the plot would provide the phase response to frequencies from 50 Hz to 500 kHz.

An alternative structure is shown in Figure 7. This circuit, which adds resistance in parallel to continuously discharge an integrating capacitor, is basically a *lossy integrator*. The center frequency is again 1/(2πRC). Because the amplifier is used in the inverting mode, the inversion introduces an additional 180° of phase shift. The input-to-output phase variation with frequency, including the amplifier's phase inversion, is shown in Figure 2 (right axis). This response will be referred to as the *inverted, first-order, low-pass response*.

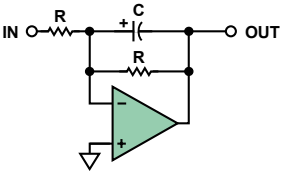

Figure 7. Active, single-pole, low-pass filter using an op amp in the inverting mode.

The circuits shown above, which attenuate the high frequencies and pass the low frequencies, are low-pass filters. Similar circuits also exist to pass high frequencies. The passive configuration for a first-order, high-pass filter is shown in Figure 8; and its phase variation with normalized frequency is shown in Figure 3 (in-phase response).

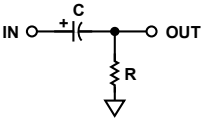

Figure 8. Passive, high-pass filter.

The plot in Figure 3 (left axis) will be referred to as the *in-phase, first-order, high-pass response*. The active configuration of the high-pass filter is shown in Figure 9. The phase variation with frequency is shown in Figure 3 (right axis). This will be referred to as the *inverted, first-order, high-pass response*.

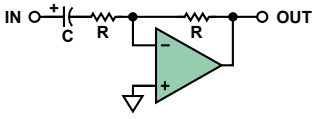

Figure 9. Active, single-pole, high-pass filter.

Second-Order Sections

A variety of circuit topologies exists for building second-order sections. To be discussed here are the *Sallen-Key*, the *multiple-feedback*, the *state-variable*, and its close cousin, the *biquad*. They are the most common and are relevant here. More complete information on the various topologies is given in the References.

Sallen-Key, Low-Pass Filter

The widely used Sallen-Key configuration, also known as a *voltage-controlled voltage source* (VCVS), was first introduced in 1955 by R.P. Sallen and E.L. Key of MIT's Lincoln Labs (see Reference 3). Figure 10 is a schematic of a Sallen-Key, second-order, low-pass filter. One reason for this configuration's popularity is that its performance is essentially independent of the op amp's performance because the amplifier is used primarily as a buffer. Since the follower-connected op amp is not used for voltage gain in the basic Sallen-Key circuit, its gain-bandwidth requirements are not of great importance. This implies that, for a given op amp bandwidth, a higher-frequency filter can be designed using this fixed (unity) gain, as compared to other topologies that involve the amplifier's dynamics in a variable feedback loop. The signal phase is maintained through the filter (noninverting configuration). A phase shift-vs.-frequency plot for a Sallen-Key, low-pass filter with Q = 0.707 (or a damping ratio, α = 1/Q of 1.414—Butterworth response) is shown in Figure 4 (left axis). To simplify comparisons, this will be the standard performance for the second-order sections to be considered here.

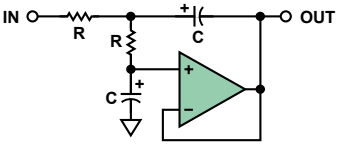

Figure 10. 2-pole, Sallen-Key, low-pass filter.

The Sallen-Key, High-Pass Filter

To transform the Sallen-Key low-pass into a high-pass configuration, the capacitors and the resistors in the frequency-determining network are interchanged, as shown in Figure 11, again using a unity-gain buffer. The phase shift vs. frequency is shown in Figure 5 (left axis). This is the *in-phase, second-order, high-pass response*.

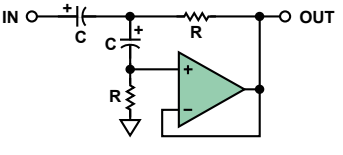

Figure 11. 2-pole, Sallen-Key, high-pass filter.

The amplifier gain in Sallen-Key filters can be increased by connecting a resistive attenuator in the feedback path to the inverting input of the op amp. However, changing the gain will affect the equations for the frequency-determining network, and the component values will have to be recalculated. Also, the amplifier's dynamics are more likely to need scrutiny, since they introduce gain into the loop.

The Multiple-Feedback (MFB), Low-Pass Filter

The multiple feedback filter is a single-amplifier configuration based on an op amp as an integrator (an inverting configuration) inside a feedback loop (see Figure 12). Therefore, the dependence of the transfer function on the op amp parameters is greater than in the Sallen-Key realization. It is hard to generate high-Q, high-frequency sections because of the limited open-loop gain of the op amp at high frequencies. A guideline is that the open-loop gain of the op amp should be at least 20 dB (i.e., ×10) above the amplitude response at the resonant (or cutoff) frequency, including the peaking caused by the Q of the filter. The peaking due to Q will have an amplitude of magnitude

$$A_0 = HQ \tag{5}$$

where H is the gain of the circuit.

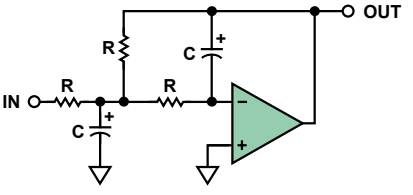

Figure 12. 2-pole, multiple-feedback (MFB), low-pass filter.

The multiple-feedback filter inverts the phase of the signal. This is equivalent to adding 180° to the phase shift of the filter itself. The variation of phase vs. frequency is shown in Figure 4 (right axis). This will be referred to as the *inverted, second-order, low-pass response*. Of interest, the difference between highest- and lowest-value components to achieve a given response is higher in the multiple-feedback case than in the Sallen-Key realization.

The Multiple-Feedback (MFB), High-Pass Filter

Comments made about the multiple-feedback, low-pass case apply to the high-pass case as well. The schematic of a multiple-feedback, high-pass filter is shown in Figure 13, and its ideal phase shift vs. frequency is shown in Figure 5 (right axis). This was referred to as the *inverted, second-order, high-pass response*.

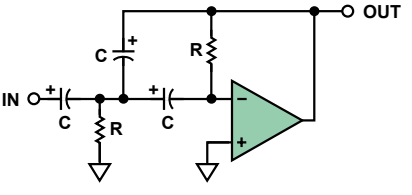

Figure 13. 2-pole, multiple-feedback (MFB), high-pass filter.

This type of filter may be more difficult to implement stably at high frequencies because it is based on a differentiator, which, like all differentiator circuits, maintains greater closed-loop gain at higher frequencies and tends to amplify noise.

State-Variable

A state-variable realization is shown in Figure 14. This configuration offers the most flexible and precise implementation, at the expense of many more circuit elements, including three op amps. All three major parameters (gain, Q, and ω_0) can be adjusted independently; and low-pass, high-pass, and band-pass outputs are available simultaneously. The gain of the filter is also independently variable.

Since all parameters of the state variable filter can be adjusted independently, component spread can be minimized. Also, mismatches due to temperature and component tolerances are minimized. The op amps used in the integrator sections will have the same limitations on op amp gain-bandwidth as described in the multiple-feedback section.

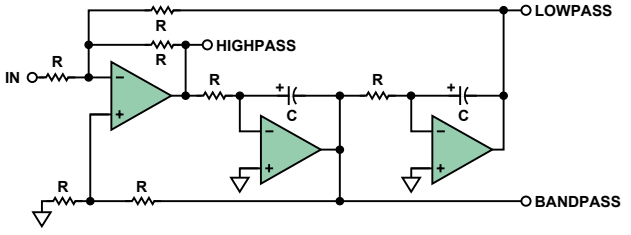

Figure 14. 2-pole, state-variable filter.

The phase shift vs. frequency of the low-pass section will be an inverted second-order response (see Figure 4, right axis) and the high-pass section will have the inverted high-pass response (see Figure 5, right axis).

Biquadratic (Biquad)

A close cousin of the state-variable filter is the *biquad* (see Figure 15). The name of this circuit, first used by J. Tow in 1968 (see Reference 6), and later by L.C. Thomas in 1971 (see Reference 5), is based on the fact that the transfer function is a ratio of two quadratic terms. This circuit is a slightly different form of a state-variable circuit. In this configuration, a separate high-pass output is not available. However, there are two low-pass outputs, one in-phase (LOWPASS1) and one out-of-phase (LOWPASS2).

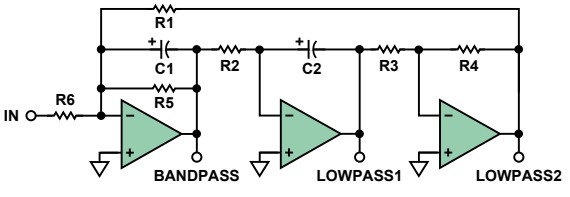

Figure 15. Standard biquad, 2-pole section.

With the addition of a fourth amplifier section, high-pass, notch (low-pass, standard, and high-pass), and all-pass filters can be realized. A schematic for a biquad with a high-pass section is shown in Figure 16.

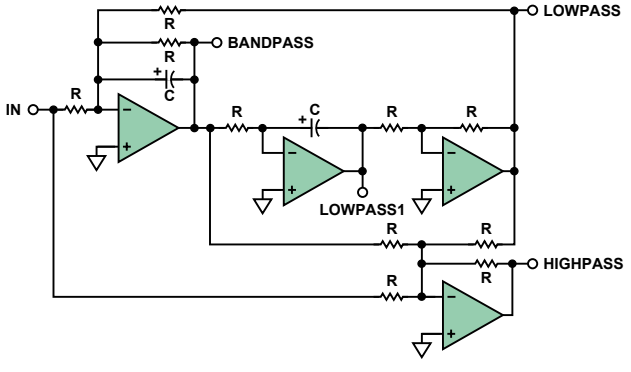

Figure 16. 2-pole biquad filter (with a high-pass section).

The phase shift vs. frequency of the LOWPASS1 section will be the in-phase, second-order, low-pass response (see Figure 4, left axis). The LOWPASS2 section will have the inverted second-order response (see Figure 4, right axis). The HIGHPASS section has a phase shift that inverts (see Figure 5, right axis).

CONCLUSION

We have seen that the topology used to build a filter will have an effect on its actual phase response. This may be one of the factors used in determining the topology used. Table 1 compares the phase-shift ranges for the various low-pass filter topologies discussed in this article.

Table 1. Low-Pass-Filter Topology Phase-Shift Ranges

LOW-PASS FILTERS		
FILTER TOPOLOGY	SINGLE PHASE	PHASE VARIATION
Single-Pole, Passive	In-Phase	0° to –90°
Single-Pole, Active	Inverted	180° to 90°
2-Pole, Sallen-Key	In-Phase	0° to –180°
2-Pole, Multiple Feedback	Inverted	180° to 0°
2-Pole, State Variable	Inverted	180° to 0°
2-Pole, Biquad Lowpass1	In-Phase	0° to –180°
2-Pole, Biquad Lowpass2	Inverted	180° to 0°

Similarly, the various high-pass topologies are compared in Table 2.

Table 2. High-Pass-Filter Topology Phase-Shift Ranges

HIGH-PASS FILTERS		
FILTER TOPOLOGY	SINGLE PHASE	PHASE VARIATION
Single-Pole, Passive	In-Phase	90° to 0°
Single-Pole, Active	Inverted	–90° to –180°
2-Pole, Sallen-Key	In-Phase	180° to 0°
2-Pole, Multiple Feedback	Inverted	0° to –180°
2-Pole, State Variable	Inverted	0° to –180°
2-Pole, Biquad	Inverted	0° to –180°

The Variation of Phase Shift with *Q*

The second-order responses above have all used a Q of 0.707. Figure 17 shows the effect on phase response of a low-pass filter (the results for high-pass are similar) as Q is varied. The phase responses for values of Q = 0.1, 0.5, 0.707, 1, 2, 5, 10, and 20 are plotted. It's worth noting that the phase can start to change well below the cutoff frequency at low values of Q.

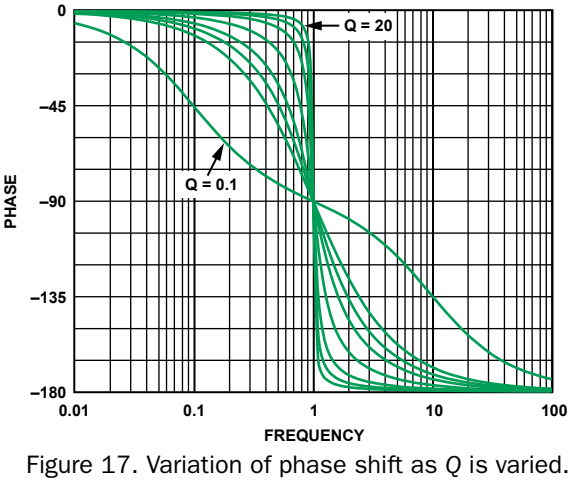

Figure 17. Variation of phase shift as Q is varied.

Although not the subject of this article, the variation of amplitude response with Q may also be of interest. Figure 18 shows the amplitude response of a second-order section as Q is varied over above range.

The peaking that occurs in high-Q sections may be of interest when high-Q sections are used in multistage filters. While in theory it doesn't make any difference in which order the sections are cascaded, in practice it is typically better to place low-Q sections ahead of high-Q sections so that the peaking will not cause the dynamic range of the filter to be exceeded. Although this plot is for low-pass sections, high-pass responses will show similar peaking.

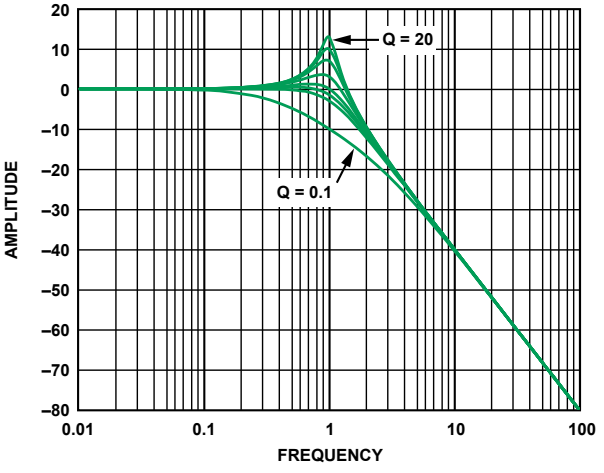

Figure 18. Amplitude peaking in 2-pole filter as Q is varied.

Higher-Order Filters

Transfer functions can be cascaded to form higher-order responses. When filter responses are cascaded, dB gains (and attenuations) add, and phase angles add, at any frequency. As noted earlier, multipole filters are typically built with cascaded second-order sections, plus an additional first-order section for odd-order filters. Two cascaded first-order sections do not provide the wide range of Q available with a single second-order section.

A fourth-order filter cascade of transfer functions is shown in Figure 19. Here we see that the filter is built of two second-order sections.

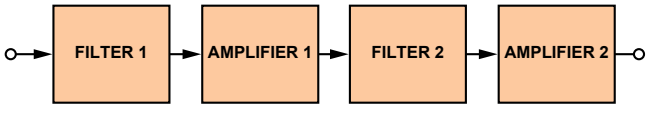

Figure 19. Cascaded transfer functions for a 4-pole filter.

Figure 20 shows the effect on phase response of building a fourth-order filter in three different ways. The first is built with two Sallen-Key (SK) Butterworth sections. The second consists of two multiple-feedback (MFB) Butterworth sections. The third is built with one SK section and one MFB section. But just as two cascaded first-order sections don't make a second-order section, two cascaded second-order Butterworth sections do not equal a fourth-order Butterworth section. The first section of a Butterworth filter has an f_0 of 1 and a Q of 0.5412 (α = 1.8477). The second section has an f_0 of 1 and a Q of 1.3065 (α = 0.7654).

As noted earlier, the SK section is noninverting, while the MFB section inverts. Figure 20 compares the phase shifts of these three fourth-order sections. The SK and the MFB filters have the same response because two inverting sections yield an in-phase response (–1 × –1 = +1). The filter built with mixed topologies (SK and MFB) yields a response shifted by 180° (+1 × –1 = –1).

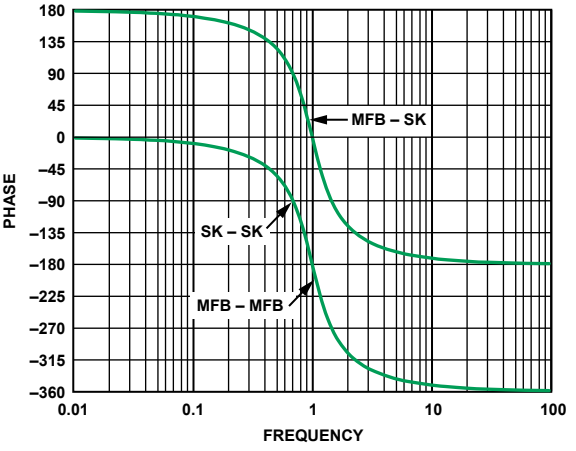

Figure 20. Fourth-order phase response with various topologies.

Note that the total phase shift is twice that of a second-order section (360° vs. 180°), as expected. High-pass filters would have similar phase responses, shifted by 180°.

This cascading idea can be carried out for higher-order filters, but anything over eighth-order is difficult to assemble in practice.

Future articles will examine phase relationships in band-, notch- (band-reject), and all-pass filters.

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Ask The Applications Engineer—38

Better, Faster Open-Loop Gain Measurement

By David Hunter [david.hunter@analog.com]

In systems that utilize feedback, the feedback network is a circuit configured for a particular gain and phase relationship—for example, an adjustable *proportional-integral-differential* (PID) controller to manipulate the loop gain and/or phase to ensure stability (see Figure 1). It is often desirable to measure the performance of this feedback network in a particular configuration so as to model the open-loop behavior. But this type of measurement is often challenging. For example, the low-frequency gain of an integrator can be very high, generally exceeding the measurement range of conventional test and measurement equipment. The goal of such measurements is to characterize the frequency response of the network rapidly and with minimal effort, using available tools and a small amount of special circuitry.

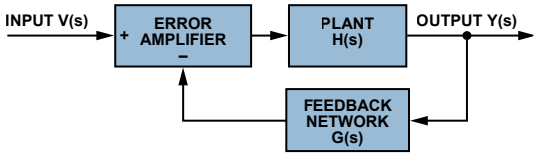


Figure 1. A basic system implementing feedback.

Q. *That makes sense. I have an example of a project that I would welcome suggestions for.*

A. Tell me about it.

Q. *To qualify a recent design, I had been working on a programmable feedback network and needed to collect hard data to verify the expected behavior. To collect the data, I evaluated the available test equipment and pieced together a crude open-loop measurement system using a general-purpose interface-bus (GPIB) IEEE-488 interfacing card, a simple digital oscilloscope, and an arbitrary function generator (see Figure 2).*

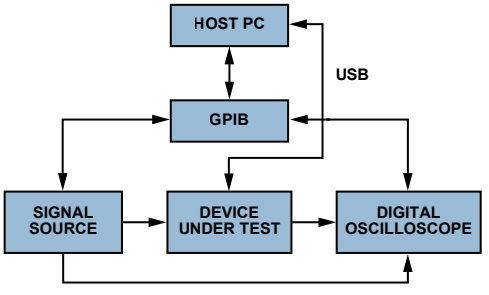


Figure 2. Functional model of the test system.

Using the available developer libraries for the GPIB interface, I wrote software to perform data-point collection for Bode plots. In much the same way that we learned in engineering school to draw a Bode plot by hand, the function generator was set to output a sine wave at a set of frequencies, point by point, as the system's "input." The oscilloscope then measured both the system input and system output to calculate the gain at a given frequency.

A. How did that turn out?

Q. *After performing numerous iterations with the devices-under-test, the faults of performing open-loop measurements on a budget, using standard lab equipment, became apparent. High precision required many data points, and each data point consumed significant amounts of time simply to exchange messages between the software and test equipment. The resolution of the oscilloscope also became a factor: at low input amplitudes, noise dominated the system and made triggering difficult. I also observed intermittent rogue samples of data (see Figure 3). Upon investigating, I found that these erroneous samples occurred before the test equipment had finished updating its settings—in effect a system settling-time issue. In the end, each test consumed an incredible 35 minutes. Analyzing the time usage for the test, I found that, for each sample, most of the time was spent in communication between the host and the test equipment, rather than actually performing the measurement.*

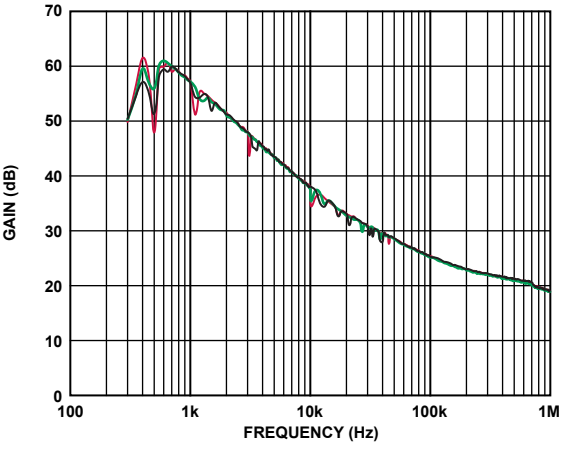


Figure 3. Samples collected in three different tests of the same configuration.

A. Execution time would improve if you were to implement hardware functions to replace software routines. For example, utilizing the available I^2C serial bus on your programmable device, less time would be spent sending ASCII characters to form text-based command messages. By making this change, you're removing several layers of abstraction and interpretation from your test loop, resulting in precise and direct control of the system's operation.

Q. *What hardware devices would it take to implement such a scheme?*

A. Use a wideband *direct digital synthesizer* (DDS) IC, such as the AD5932,[1] to replace the function generator. This DDS provides your design with excellent frequency range and a high-quality sinusoidal output. Gain measurement becomes a simple task with the application of a pair of logarithmic amplifier ICs, such as the AD8307,[2] and a difference amplifier. And the final critical piece of the acquisition system is an analog-to-digital converter IC to replace the digital oscilloscope. Using a multi-input ADC, such as the AD7992[3] or AD7994,[4] will lower the total cost of the system by using two available channels to capture the logarithmic amplifiers' result and perform the difference operation in software. The revised arrangement will look like Figure 4.

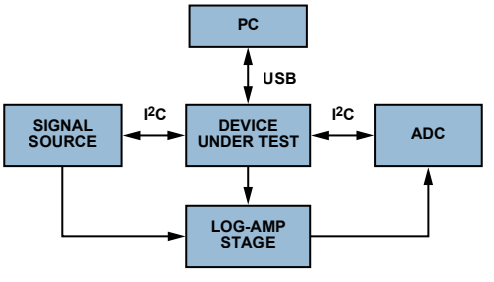


Figure 4. Block diagram of new test system.

Q. *How does gain measurement with a log amp work?*

A. In response to ac inputs, the AD8307 low-cost, easy-to-use logarithmic amplifier produces a dc output—equivalent to 25 mV/dB of input power (0.5 V per *decade* of voltage) into a 50-Ω load. With a wide dynamic range of 92 dB, the device allows the user to measure even the small input signals experienced in high-gain, open-loop circuits. While you will not actually be driving 50-Ω loads, this standard allows calculating gain (in dB) as the difference of two AD8307 device outputs, which measure the signal input and output.

Q. *Can you explain this in more detail?*

A. We start with a brief review of logarithm rules:

$$\log\left(\frac{A}{B}\right) = \log A - \log B \tag{1}$$

$$\log(A \times B) = \log A + \log B \tag{2}$$

$$\log(A^B) = B \times \log A \tag{3}$$

Electrical power gain or attenuation is typically expressed as a log ratio: Since the world of dB deals with ac voltages, V_A and V_B are *rms* voltages, and, consequently, P_A and P_B are *average* power levels.

$$\begin{aligned}\text{decibels (dB)} &= 10\log\left(\frac{P_A}{P_B}\right)\\ &= 10\log\left(\frac{{V_A}^2/R_A}{{V_B}^2/R_B}\right) = 20\log\left(\frac{V_A}{V_B}\right) + 10\log\left(\frac{R_B}{R_A}\right)\end{aligned} \tag{4}$$

For unity impedance-ratios, log 1 = 0. Thus, for equal-resistance loads,

$$\text{dB} = 20\log\left(\frac{V_A}{V_B}\right) \tag{5}$$

In high-impedance voltage-amplifier circuits the focus is on *signal gain*, rather than power gain. So dB is a logarithmic expression of the ratio of output amplitude to input amplitude.

At zero dB, the voltage ratio is unity. To express a given power level measurement in dB, it must be referred to a reference power level. In standard practice, if the measured power is equal to 1 mW, the absolute power level is 0 dBm (or dB above a milliwatt). For a 50-Ω load,

$$\begin{aligned}\text{dBm} &= 10\log\left(\frac{P\,rms\,(\text{watts})}{0.001\,\text{W}}\right) = 10\log\left(\frac{V\,rms^2/50\Omega}{0.001\,\text{W}}\right)\\ &= 10\log\left(1000\times\frac{V\,rms^2}{50\Omega}\right) = 10\log\left(20\times V\,rms^2\right) = 20\log(V\,rms)\end{aligned} \tag{6}$$

Using a low-distortion sine wave, $V\,rms$ and average power—for a 50-Ω system—is calculated using Equations 7 and 8:

$$V\,rms = \frac{V_{amplitude}}{\sqrt{2}} \tag{7}$$

$$\text{Power} = \left(\frac{V\,rms^2}{Z_0}\right) = \frac{\left(V_{amplitude}\right)^2}{2\times 50} \tag{8}$$

Thus, for 0 dBm, or 1 mW, the input voltage amplitude is 316.2 mV (or 223.6 mV rms). If that is the input level, and the output amplitude of the device under test is 3.162 V (a gain of 10 with an rms amplitude of 2.236 V), then from Equation 6 the output power is +20 dBm, the same as one would obtain from the voltage gain expressed by the ratio in Equation 5. The values are consistent so long as the references are consistent. We can therefore find the system gain easily.

Combining Equation 8 and Equation 6,

$$\begin{aligned}\text{dBm} &= 10\log\left(1000\times\frac{V\,rms^2}{50}\right)\\ &= 10\log(1000) + 10\log\left(\frac{{V_{amplitude}}^2}{100}\right)\\ &= 30 + 20\log(V_{amplitude}) - 20\\ &= 20\log(V_{amplitude}) + 10\end{aligned} \tag{9}$$

Apply the log amplifier's conversion gain of 25mV/dB:

$$V_{output} = 0.5\log(V\,p\text{-}p) + 0.25 \tag{10}$$

Applying Equation 1, using two AD8307 log amplifiers to measure output and input, their difference results in an easy measurement of gain.

$$\begin{aligned}V_{gain} &= \left[0.5\log(V_{output}) + 0.25\right] - \left[0.5\log(V_{input}) + 0.25\right]\\ &= 0.5\log\left(\frac{V_{output}}{V_{input}}\right)\\ &= 0.5\text{ V/20 dB}\end{aligned} \tag{11}$$

The AD8307's inherent output at 0 dB is about 2.0 V. However, the constants (when calibrated) drop out of the equation when the output is calculated as the difference of the log amp outputs.

Q. *How do you find the difference?*

A. There are many options to obtain the difference, ranging from an easy-to-apply instrumentation amplifier, such as the AD622[5] or AD627,[6] to a discrete multi-op-amp solution, or even in software after conversion to digital, perhaps using a multichannel ADC like the AD7994. For best accuracy, the designer must, of course, calibrate to eliminate gain- and offset errors between devices. Data sheets available on the Analog Devices website provide this information—as well as excellent tips on frequency-specific issues.

Q. *You mentioned the AD5932 direct digital synthesizer. What is that?*

A. The AD5932 DDS is a simple, programmable, digitally controlled waveform generator. Using a few simple instructions, the user can configure sine waves, for example, with a complete frequency and phase profile. While this device does not possess an I^2C interface, a GPIO device on the I^2C bus can perform bit-banging operations to imitate the expected interface. After configuration is completed, a single *write* to the GPIO device can increment the output frequency.

The output of the AD5932 is 580 mV peak-to-peak, a value that is, in most cases, too large an input for open-loop gain

measurement. The attenuation needed depends on the input level appropriate for gain measurement of the device under test at its specified output level. If the input signal is too large, the output will be distorted, or even clipped, giving false measurements. If the signal is too small, offset errors and noise will dominate the waveform's output and cause problems. A typical signal starts at 10 mV in amplitude, then increases to produce the specified device output value—or the largest value possible without clipping or distortion, as distortion will cause measurement errors.

Q. *Can you give me an example of how it works?*

A. After assembling the circuit building blocks as shown in Figure 4, you can verify (or calibrate) the performance using, first, a unity-gain amplifier, then a gain-of-10 amplifier in place of the device under test.

Figure 5 is an example of measurements showing unity gain and a gain of 10, actually about 1 dB high, with variation held to well within ±1 dB.

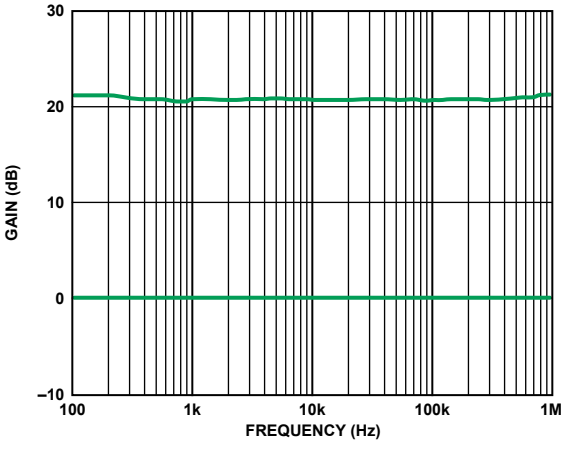


Figure 5. Example of calibration gain data to qualify performance. Note the uncalibrated excess gain of +1 dB for the 20-dB setting.

As another example, once confidence in the technique is gained, a sample device with a known behavior can then be tested. Figure 6 shows a typical result, superimposed on the previously collected data to verify the accuracy of this method vs. that of the method you described. The result of the test revealed an error of about ±0.5 dB, indicating that the new system measurement had the same measurement characteristics, but with far lower noise and faster settling times.

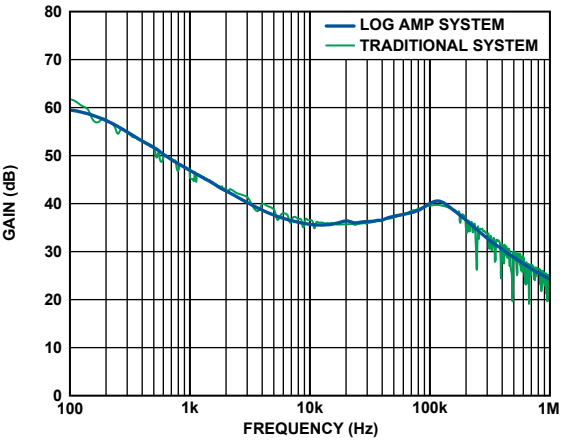


Figure 6. Bode-plot data combining both new (blue) and old (green) data. Note the "sampling noise" of the traditional system.

Equipment:

1. National Instruments Cardbus GPIB adapter
2. Tektronix TDS3032B with GPIB
3. Tektronix AFG320 with GPIB

Q. *The correlation looks good, and there seem to be none of the outliers plotted in the earlier method. How long did it take to scan through this set of measurements?*

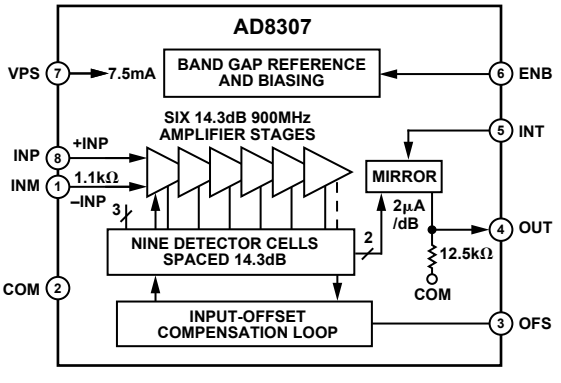
A. Each test run was completed in under 35 seconds.

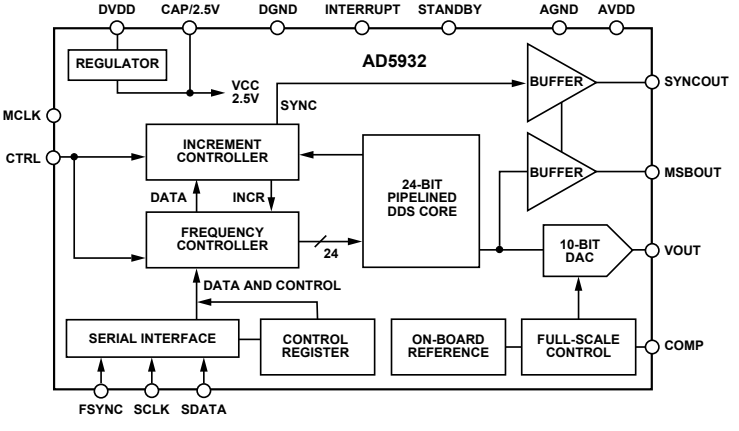
Q. *Wow! That's an improvement of about 6000%.*

A. Yes, and, in addition, the simplicity of the design lends itself easily to use in embedded systems, as the majority of the math operations are managed by the log amplifiers. A clever designer could also integrate a phase-measurement device and turn this system into a true Bode plotter. And you could obtain an all-in-one solution, with high-frequency applications, using the single-chip AD8302[7] gain- and phase-measuring log amp.

REFERENCES—VALID AS OF NOVEMBER 2007

[1]ADI website: www.analog.com (Search) AD5932 (Go)
[2]ADI website: www.analog.com (Search) AD8307 (Go)
[3]ADI website: www.analog.com (Search) AD7992 (Go)
[4]ADI website: www.analog.com (Search) AD7994 (Go)
[5]ADI website: www.analog.com (Search) AD622 (Go)
[6]ADI website: www.analog.com (Search) AD627 (Go)
[7]ADI website: www.analog.com (Search) AD8302 (Go)





DC-to-DC Switching-Regulator Insights—Achieving Longer Battery Life in DSP Systems

By Sridhar Gurram [sridhar.gurram@analog.com]
Oliver Brennan [oliver.brennan@analog.com]
Tim Wilkerson [tim.wilkerson@analog.com]

INTRODUCTION

Attaining high performance and low power consumption in MP3 players, personal media players, digital cameras, and other portable consumer applications has long challenged designers. These battery-powered systems typically employ an embedded digital signal processor (DSP) to achieve maximum processing power when handling multimedia applications and minimum power consumption when in *sleep* mode. Battery life is of prime importance in handheld battery-powered products, making their success directly related to the efficiency of the power system.

A key component of such systems, a *step-down dc-to-dc switching regulator*, efficiently derives a low supply voltage, say 1 V, from a higher-voltage supply, for example, 4.5 V. As a *regulator*, it must maintain a constant voltage, rapidly responding to variations in the upstream supply or the load current. We will discuss here an architecture that provides good regulation, high efficiency, and fast response.

ANATOMY OF A SWITCHING REGULATOR

Figure 1 shows a typical application circuit using the Analog Devices ADP2102[1] low-duty-cycle, 3-MHz, synchronous step-down converter. It is available with a number of fixed-output and resistor-programmable voltage options. Here it is connected in a fixed-voltage configuration, producing a regulated 0.8-V output from a 5.5-V input voltage and driving a 300-mA load. A resistor-programmable application example will follow.

Here is a brief explanation of the circuit's operation: A fraction of the dc output voltage is compared with an internal reference in the error amplifier, whose output is compared with the output of a current-sense amplifier to drive a one-shot that is on for a period of time that depends on the ratio V_{OUT}/V_{IN}. The one-shot turns on the upper gating transistor and the current in inductor L1 ramps up. When the one-shot times out, the transistor is turned off, and the current ramps down. After an interval determined by the minimum off-timer and the minimum ("valley") current, the one-shot is pulsed again. The on-chip one-shot timer employs input voltage feedforward for maintaining a constant frequency in the steady state.

This oscillation continues indefinitely—at approximately 3 MHz, but deviating as necessary to respond to transient line and load changes—maintaining the output voltage at the programmed value and the average inductor current at the value required by the output load.

The approach described above is relatively new. For many years, the principal approach to dc-to-dc conversion has been a *constant-frequency peak-current* approach, also known as *trailing-edge modulation* when implemented in step-down dc-to-dc converters. For a description of that approach, and an evaluation of its strengths and weaknesses vis-à-vis the constant on-time valley current-mode converter described above, see the sidebar.

The ADP2102 also includes undervoltage lockout, soft start, thermal shutdown, short-circuit protection, and ±1% feedback accuracy. This architecture allows the on-time of the main switch to go as low as, or lower than, 60 ns.

Figure 2 shows typical waveforms under various conditions. Figure 2a shows the low duty cycle that accompanies the large voltage reduction from V_{IN} = 5.5 V to V_{OUT} = 0.8 V at I_{LOAD} = 600 mA. As can be seen in the plot, the minimum on-time achieved is 45 ns with a switching frequency of 3 MHz.

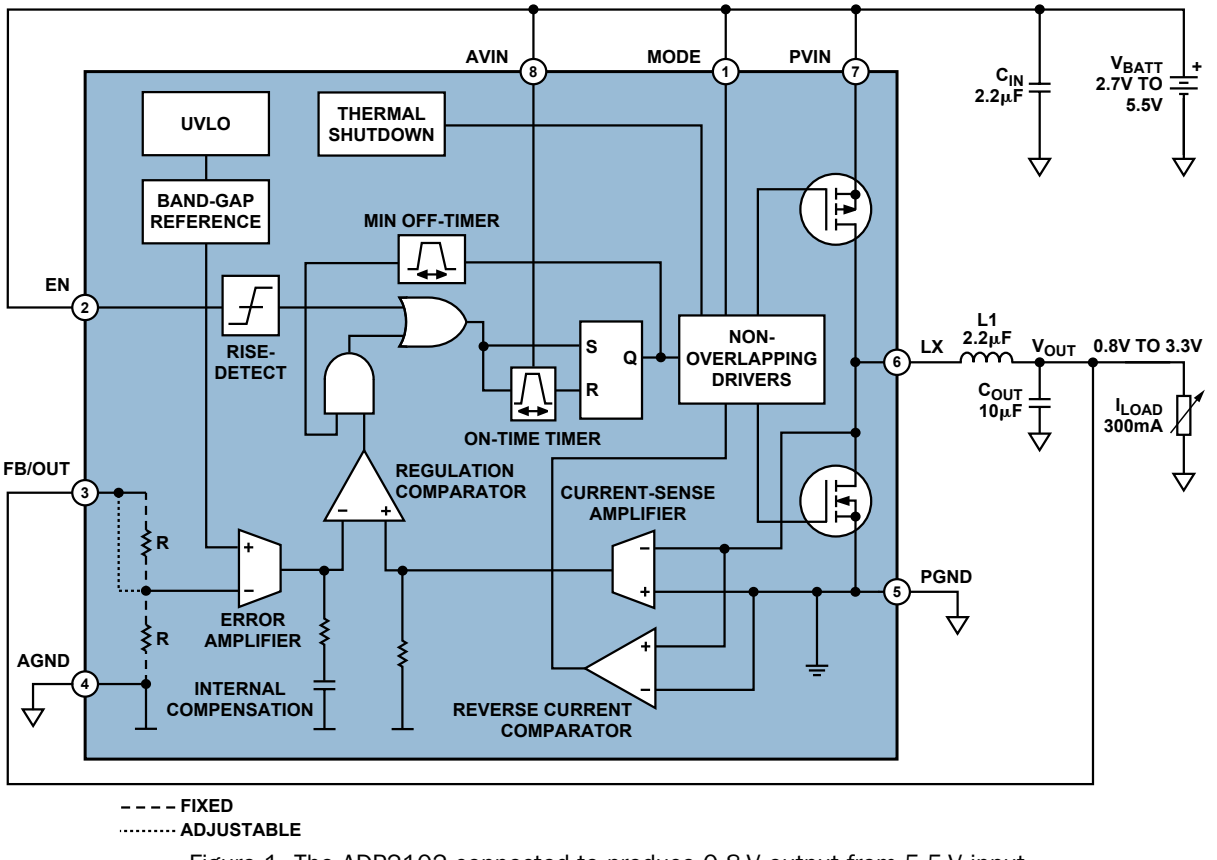


Figure 1. The ADP2102 connected to produce 0.8-V output from 5.5-V input.

Figure 2b shows the load current and inductor current in response to a 300-mA step increase in load current.

Figure 2c shows the load current and inductor current in response to a 300-mA step decrease in load current.

Figure 2d shows that there are no subharmonic oscillations when the part operates at a 50% duty cycle, which is a concern for parts using peak-current-mode control. This freedom from subharmonic oscillations is also the case for duty-cycle values somewhat greater or less than 50%.

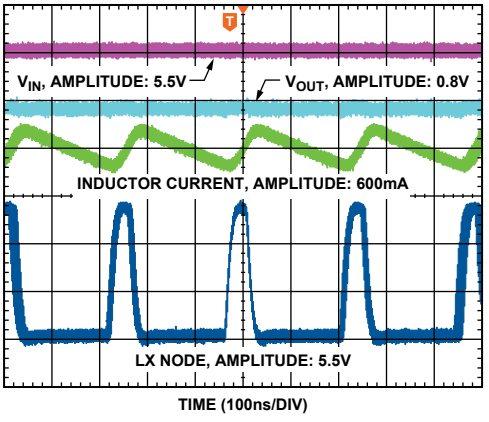


Figure 2a. V_{IN} = 5.5 V, V_{OUT} = 0.8 V, Minimum on-time = 45 ns.

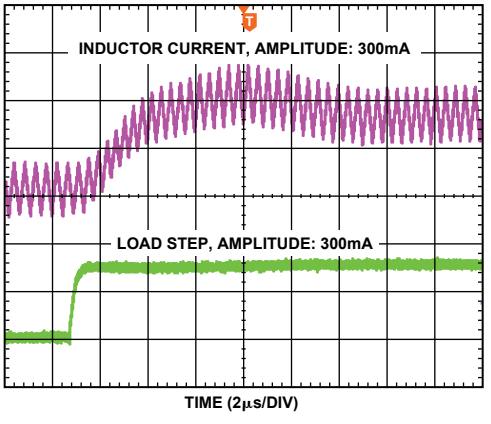


Figure 2b. Positive load transient response (I_{LOAD} = 300 mA).

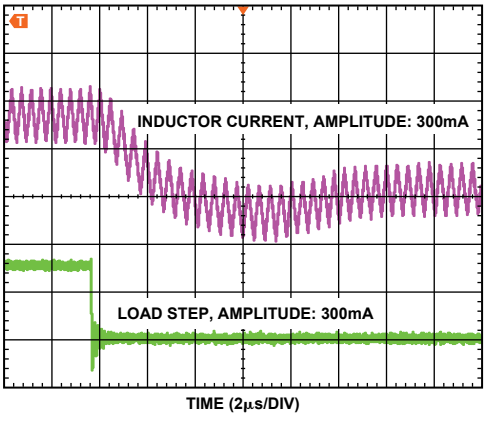


Figure 2c. Negative load transient response (I_{LOAD} = 300 mA).

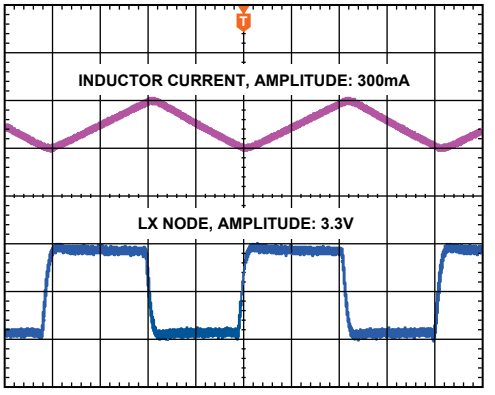


Figure 2d. Duty cycle = 50%, V_{IN} = 3.3 V, V_{OUT} = 1.8 V, I_{LOAD} = 300 mA.

DYNAMIC VOLTAGE ADJUSTMENT IN A DSP APPLICATION

In portable applications employing digital signal processors (DSPs), switching converters typically provide the DSP's core voltage and I/O rails. Both supplies require high-efficiency dc-to-dc converters that are designed for battery applications. The regulator that supplies the core voltage must be able to change the voltage dynamically based on the processor's clock speed or as directed by the software. Small total solution size is also important.

Described here are improvements in system power efficiency that can be attained in battery-powered applications by replacing a Blackfin®[2] processor's internal regulator with an external high-efficiency regulator. Also described is the control software for the external regulator.

Dynamic Power Management

A processor's power dissipation is proportional to the square of the operating voltage (V_{CORE}) and linearly proportional to the operating frequency (F_{SW}). Thus, decreasing the frequency will lower the dynamic power dissipation linearly, while reducing the core voltage will lower it exponentially.

Changing the clock frequency—but not the supply voltage—in a power-sensitive application is useful when the DSP is simply monitoring activity or waiting for an external trigger. In high-performance battery-powered applications, however, merely changing the frequency may not save enough power. Blackfin processors, and other DSPs with advanced power-management features, allow the core voltage to be changed in tandem with frequency changes, thus seeking optimal loading of the battery for each situation.

Dynamic voltage regulation in ADSP-BF53x[3] series Blackfin processors is typically implemented with an internal voltage controller and an external MOSFET. The advantage of this approach is that a single voltage (VDDEXT) can be applied to the DSP subsystem, while the DSP derives the necessary core voltage (VDDINT) from the MOSFET. Internal registers allow the regulated core voltage to be software-controlled in order that the MIPS, and ultimately the consumed energy, can be coordinated to achieve optimal battery life.

To fully implement this internal Blackfin regulator scheme requires an external MOSFET, a Schottky diode, a large inductor, and multiple output capacitors—a relatively expensive solution with poor efficiency that uses a relatively large PCB area. The use of the large inductors and capacitors required by the integrated regulator brings the system designer into conflict with consumer desires for portable devices to be as small as possible. Along with the relatively low efficiency of the integrated

regulator controller—typically 50% to 75%—this approach is less than optimally suited for high-performance, handheld, battery-powered applications.

External Regulation

The native efficiency of the Blackfin integrated approach can be improved to 90% or more by designing in a modern dc-to-dc switching converter. The size of the external components can also be reduced when an external regulator is used.

A variety of *dynamic voltage-scaling* (DVS) control schemes are available, ranging from switched resistors—which in some cases can be implemented by using a DAC—to pulse-width modulation (PWM), which can achieve as fine a granularity as the internal method. Whatever scheme is used must provide the ability to change the regulation level via software control. While this regulation control method is inherent with the internal regulator approach, it must be added in external approaches.

This article describes two ways to adjust the DSP's core voltage by using an ADP2102 synchronous dc-to-dc converter to dynamically adjust the core voltage to values from 1.2 V to 1.0 V when the processor is running at a reduced clock speed.

The ADP2102 high-speed synchronous switching converter can regulate the core voltage as low as 0.8 V when powered with a battery voltage between 2.7 V and 5.5 V. Its constant on-time, current-mode control and 3-MHz switching frequency provide excellent transient response, very high efficiency, and superior line- and load regulation. The high switching frequency allows the use of ultrasmall, multilayer inductors and ceramic capacitors. Available in a space-saving 3-mm × 3-mm LFCSP package, the ADP2102 requires only three or four external components. Functionally complete, it includes safety features such as undervoltage lockout, short-circuit protection, and thermal shutdown.

Figure 3 illustrates a circuit that implements DVS. The 3.3-V system power supply on the ADSP-BF533 EZ-KIT Lite®[4] evaluation board powers the ADP2102 buck converter, whose output voltage is set to 1.2 V using the external resistive dividers R_1 and R_2. A GPIO pin from the DSP is used to select a requested core voltage. Varying the feedback resistor adjusts the core voltage from 1.2 V to 1.0 V. An N-channel MOSFET modifies the voltage divider by inserting resistor R_3 in parallel with R_2. The 0.25-Ω R_{DSon} of the IRLML2402 is small compared to R_3. The 3.3 V GPIO voltage is used to drive the MOSFET gate. Feedforward capacitor C_{FF} is needed for better transient performance and improved load regulation.

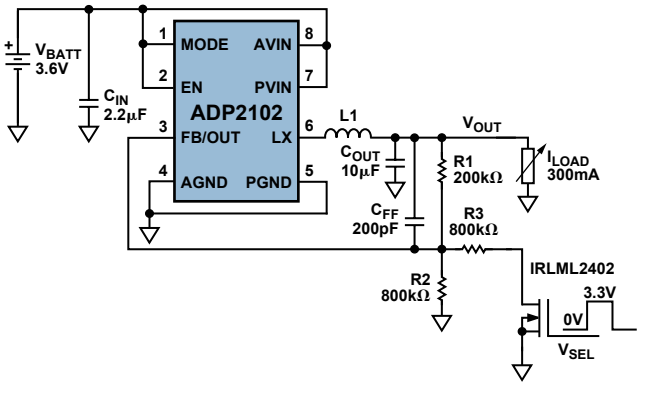


Figure 3. Dynamic voltage scaling of ADP2102 using an external MOSFET and Blackfin PWM control.

The general application requirements for two-level switching are:

1. DSP core voltage (V_{OUT1}) = 1.2 V
2. DSP core voltage (V_{OUT2}) = 1.0 V
3. Input voltage = 3.3 V
4. Output current = 300 mA

High-value resistors are used to minimize power losses through the resistive divider. The feedforward capacitor reduces the effect of the gate-to-drain capacitance during switching. The overshoot and undershoot caused during this transition can be minimized by using smaller feedback resistors and a larger feedforward capacitor, but only at the expense of additional power dissipation.

Figure 4 shows the output current, I_{OUT}, output voltage, V_{OUT}, and control voltage, V_{SEL}. A *low* level on V_{SEL} scales the output voltage to 1.0 V, and a *high* level on V_{SEL} scales it to 1.2 V.

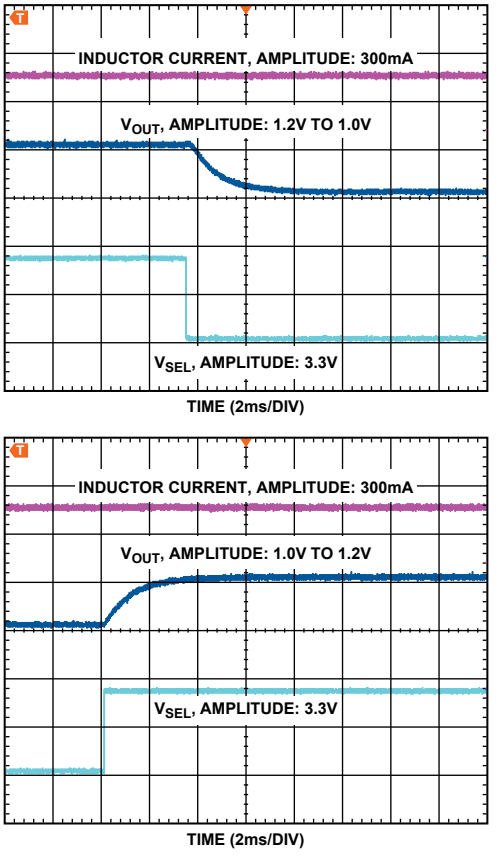


Figure 4. Modulating the bottom feedback resistor with a MOSFET.

A simpler way to generate two different voltages for DVS uses a control voltage, V_C, to inject current into the feedback network through an additional resistor. Adjusting the duty cycle of the control voltage varies its average dc level. A single control voltage and resistor can thus be used to adjust the output voltage. The following equations are used to calculate the values of resistors R_2, R_3, and the control voltage amplitude levels, V_{C_LOW} and V_{C_HIGH}.

$$\frac{V_{FB}}{R_2}+\frac{V_{FB}-V_{OUT1}}{R_1}+\frac{V_{FB}-V_{C\_LOW}}{R_3}=0 \quad (1)$$

$$\frac{V_{FB}}{R_2}+\frac{V_{FB}-V_{OUT2}}{R_1}+\frac{V_{FB}-V_{C\_HIGH}}{R_3}=0 \quad (2)$$

With V_{OUT1} = 1.2 V, V_{OUT2} = 1.0 V, V_{FB} = 0.8 V, V_{C_LOW} = 3.3 V, V_{C_HIGH} = 0 V, and R_1= 49.9 kΩ, R_2 and R_3 can be calculated as follows

$$R_3 = R_1 \frac{V_{C\_HIGH} - V_{C\_LOW}}{V_{OUT1} - V_{OUT2}} = 16.5R_1 \approx 825\,\text{k}\Omega \quad (3)$$

$$R_2 = \frac{16.5V_{FB}}{16.5V_{OUT1} - 17.5V_{FB} + V_{C\_LOW}} \approx 114\,\text{k}\Omega \quad (4)$$

This approach produces much smoother transitions. Any control voltage that can drive resistive loads can be used for this scheme, as opposed to the MOSFET switching approach, which can only be used with control signal sources that can drive capacitive loads. This approach can be scaled to any output voltage combinations and output load currents. Thus, DSP power dissipation can be reduced by scaling the core voltage as needed. Figure 5 shows the implementation of the above scheme. Figure 6 shows the transition between the two output voltages using this current injection method.

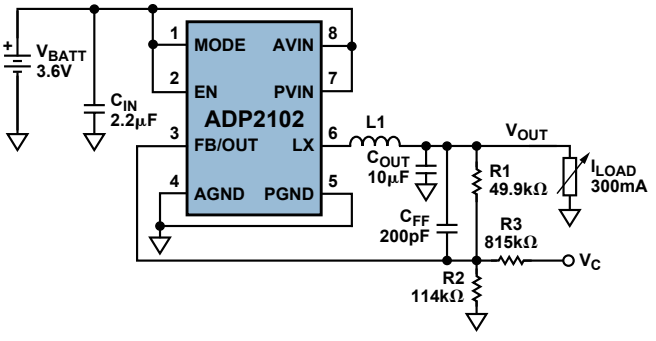


Figure 5. Dynamic voltage scaling of ADP2102 using control voltage V_C.

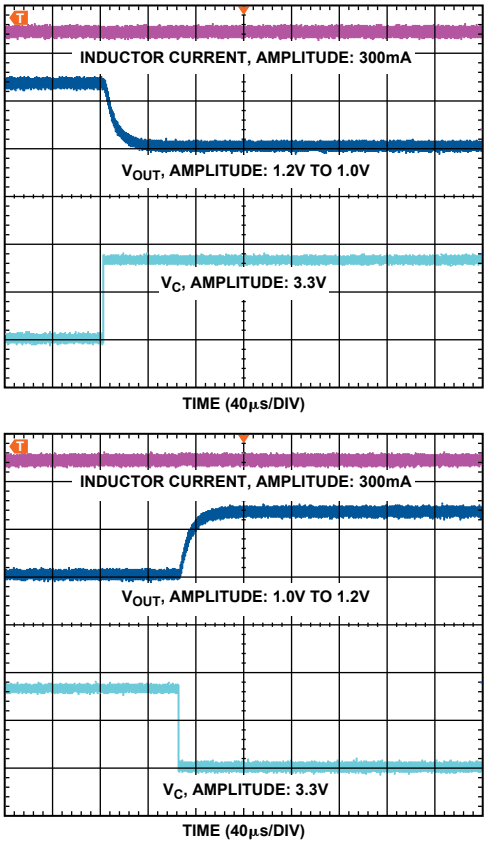


Figure 6. Modulating the bottom feedback resistor with a control voltage.

FURTHER READING

1. ADP2102 data sheet. Analog Devices. www.analog.com.
2. Hariman, George and Chris Richardson. "Control Methods Solve Low Duty-Cycle Dilemmas." *Power Electronics Technology*. September 2006.
3. Ridley, R.B. "A new continuous-time model for current-mode control with constant frequency, constant on-time and constant off-time in CCM and DCM." *IEEE Power Electron. Spec. Conf.* Record. 1990. pp. 382-389.
4. Rossetti, Nazzareno and Seth R. Sanders. "Valley Design Techniques Outperform Peak Current Mode Approach for CPU Supplies." *Power Electronics Technology*. July 2001.

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[1] ADI website: www.analog.com (Search) ADP2102 (Go)
[2] ADI website: www.analog.com (Search) Blackfin (Go)
[3] ADI website: www.analog.com (Search) ADSP-BF53x (Go)
[4] ADI website: www.analog.com (Search) ADSP-BF533 EZ-KIT Lite (Go)

ADVANTAGES OF CONSTANT ON-TIME VALLEY-CURRENT-MODE CONTROL SCHEME IN STEP-DOWN DC-TO-DC CONVERTERS

The constant-frequency peak-current control scheme regulates a high input voltage to produce a low output voltage using two loops, viz., an outer-voltage loop and an inner-current loop. Minimal phase shift exists between the control signal and the output, thus allowing simple compensation.

Inductor current through the NMOS main switch is typically measured by monitoring either the voltage drop across the main switch when it is on or the voltage drop across a series resistor placed between the input and the drain of the main switch. Parasitics on the switch node during inductor current-sensing cause ringing behavior in either case, so blanking time is required before the inductor current can be measured. This reduces the amount of time available for the main switch to stay on and settle during low duty-cycle operation. Figure A shows the inductor current and the current sense signal across the main switch, which consists of blanking time and on-time.

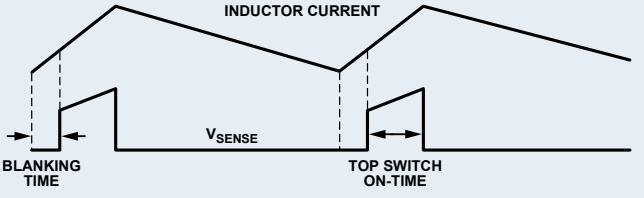

Figure A. The blanking time dictates the minimum on-time that can be achieved by the main switch in a step-down converter that uses fixed-frequency, peak-current-mode control.

During low-duty-cycle operation, i.e., when the output is very small compared to the input, the main switch turn-on is always controlled by the internal clock and is independent of the feedback loop. Thus, a minimum on-time exists, limiting the operation at higher switching frequencies. Also, due to settling-time constraints, it is not possible to sense the current because the pulse is not wide enough. The blanking time dominates the main switch on-time, leaving very little time for current sensing. In portable applications, such as handsets and media players, output voltages of the order of 0.9 V are needed for the DSP core. A high switching frequency is desirable in order to minimize the size of the

inductors and reduce the size of the overall solution; but, using this control scheme, it is difficult to generate a low-duty-cycle voltage from a higher input voltage using a high switching frequency.

A second limitation of trailing-edge modulation control is its poor transient response. Figure B shows typical waveforms in response to positive and negative changes in load current. In portable applications, fast transient response must be achieved while minimizing output capacitor size and cost. When a positive load-current step occurs at the output, the output response can be delayed by as much as one clock period. During a negative load current step, the converter forces a minimal-width high-side on-time, as determined by the speed of the current-control loop. A minimal delay response is, thus, not possible during negative load transients, and severe overshoot and undershoot transients occur. Additional capacitance must be added at the output to minimize them.

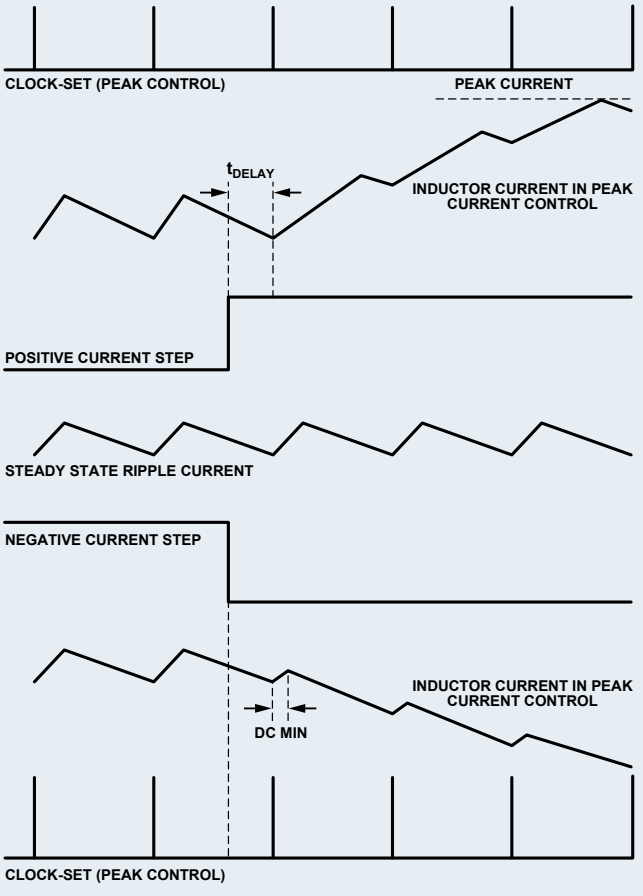

Figure B. Positive and negative load current responses with peak-current-mode control.

A third limitation of peak-current-control converters operating at fixed frequencies is that the instability (Figure C) at duty cycles greater than 50% allows subharmonic oscillations to occur, which cause the average output current to drop and the output current ripple to increase. For duty cycles greater than 50%, an increase in inductor current (ΔIL1) tends to increase with time, resulting in a larger increase of I2 (ΔIL2). In order to overcome this problem, slope compensation or ramp compensation is required, adding complexity to the design. Typically, an external ramp is added to the inductor current sense signal.

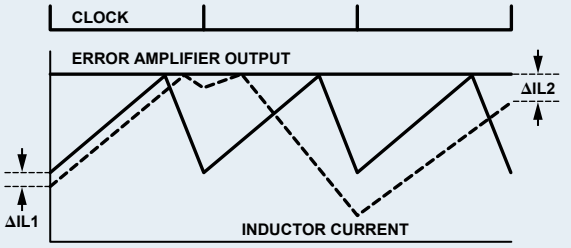

Figure C. Instability problem in fixed-frequency, peak-current-control converters at >50% duty cycle.

These problems can be overcome by using a constant on-time, valley-current-mode control scheme, known as *leading-edge modulation*, in which the on-time of the main switch is fixed by design; the off-time is modulated based on the valley-current-sense signal; and the switching period is adjusted to be equal to the on-time plus the off-time. This architecture facilitates high frequency operation by providing a minimum on-time for the main switch, thus allowing low voltage outputs to be easily generated from a higher input voltage.

In low-voltage dc-to-dc buck converters, the main switch is on for only 10% of the time, while the synchronous switch is on for the remaining 90% of the time. This makes it easier to sample and process the low-side switch current than the main switch current.

Instead of sensing the inductor peak current to determine the main switch current, the inductor valley is sampled during the *off* time of the main switch. Valley current-sensing, coupled with the constant on-time topology, reduces the loop delays, thus enabling a faster transient response.

Ray Ridley (Further Reading 3) demonstrated that the current-loop gain for constant-frequency control with an external ramp equal to the downslope of the current signal is identical to the current-loop gain of the constant on-time system. Thus, the loop gain remains invariant with duty cycle for the constant on-time control, guaranteeing stability under all conditions. In contrast, in constant-frequency peak-current control, the loop gain increases with duty cycle and can lead to instability if insufficient external ramp time is used.

Constant on-time, variable off-time converters overcome the instability problem associated with fixed-frequency operation for duty cycles above 50% without the need for slope compensation. If the load current increases, the disturbance before the start of the cycle and at the end of cycle remains the same, and, hence, the converter remains stable regardless of the duty cycle. The absence of a fixed clock for this architecture makes the slope compensation redundant.

One of the significant benefits of constant on-time, valley-current control is the ability to limit the short-circuit current in buck converters. When the output of the buck converter short circuits and the high-side switch is on, the output voltage goes to zero and the voltage across the inductor equals V_{IN}. The inductor current rises quickly for the duration of t_{ON}. The inductor discharge time, t_{OFF}, increases because it is determined by V_{OUT}/L, where V_{OUT} is effectively a short circuit. The high-side switch doesn't turn on again until the current has dropped to the required valley-current limit. Thus, under short-circuit conditions, this control scheme can only deliver a fixed maximum current.

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