Volume 43, Number 4, 2009

A forum for the exchange of circuits, systems, and software for real-world signal processing

Analog Dialogue

In This Issue

2 Editors' Notes; New Product Introductions

3 Isolation in High-Voltage Battery Monitoring for Transportation Applications

6 Synchronizing Device Clocks Using IEEE 1588 and Blackfin Embedded Processors

11 Using Isolated RS-485 in DMX512 Lighting Applications

13 Designing High-Performance Phase-Locked Loops with High-Voltage VCOs

17 Adjustable-Gain Difference Amplifier Circuit Measures Hundreds of Volts, Rejects Large Common-Mode Signals

19 Automobile Tail-Lamp and Brake-Lamp Controller

www.analog.com/analogdialogue

ANALOG DEVICES

Editors' Notes

IN THIS ISSUE

Isolation in High-Voltage Battery Monitoring for Transportation Applications

Battery stacks for transportation can provide hundreds of volts. These high voltages can prove lethal to human beings—and even lower voltages can damage electronic equipment—so safety is a key concern. Although these stacks are inherently dangerous, they must still communicate with the cell-monitoring electronics. Galvanic isolation is thus required to make the communications method safe and reliable. Page 3.

Synchronizing Device Clocks Using IEEE 1588 and Blackfin Embedded Processors

IEEE 1588 defines a protocol to synchronize distributed clocks on a network. The preferred clock synchronization method for many applications, it is cost-effective, supports heterogeneous systems, and provides nanosecond-level synchronization. The ADSP-BF518 Blackfin® processor includes dedicated hardware support for IEEE 1588. This article shows clock synchronization performance obtained using this solution. Page 6.

Using Isolated RS-485 in DMX512 Lighting Applications

Theatrical lighting applications have evolved from lanterns in open-air theaters into the more complex systems available today. Modern lighting equipment includes dimmers, flashing lights, moving lights, colored lights, and gobos. These lighting systems are often controlled over long distances—up to 4000 feet—using the DMX512 communications protocol. Page 11.

Designing High-Performance Phase-Locked Loops with High-Voltage VCOs

Phase-locked loops are used to provide the local oscillator in radio receivers and transmitters; for clock distribution and noise reduction, and as the clock source for high-sampling-rate ADCs. This article considers the basics of PLLs, examines the current state of the art in PLL design, discusses pros and cons of typical architectures, and introduces some alternatives to high-voltage VCOs. Page 13.

Adjustable-Gain Difference Amplifier Circuit Measures Hundreds of Volts, Rejects Large Common-Mode Signals

To monitor power-line voltages or other large signals, a differential amplifier in a feedback loop with an inverting op amp is useful for measuring differential signals up to 500 V. This circuit also rejects large common-mode voltages and allows the differential gain to be set by a ratio of resistors, enabling the user to select the level of attenuation. Page 17.

Automobile Tail-Lamp and Brake-Lamp Controller

Light emitting diodes (LEDs) are recently finding uses in automobiles, where they provide signaling, daytime running lights, and interior lighting. As this technology hits the road, manufacturers continue to investigate new ways to apply it, taking advantage of the styling possibilities afforded by LED headlights and taillights. Page 19.

Dan Sheingold [dan.sheingold@analog.com]

Scott Wayne [scott.wayne@analog.com]

PRODUCT INTRODUCTIONS: VOLUME 43, NUMBER 4

Data sheets for all ADI products can be found by entering the part number in the search box at www.analog.com.

October

Amplifier, instrumentation, micropower **AD8235**
Controller, dc-to-dc, step-down, 2-output **ADP1877**
Sensor, inertial, six-degrees-of-freedom **ADIS16362**
Supervisor, voltage, 4-channel, ±supplies **ADM12914**

November

ADC, SAR, 16-bit, 2.5-MSPS **AD7985**
ADC, SAR, 16-bit, 10-MSPS, 1.5-LSB INL **AD7626**
Amplifier, operational, quad, rail-to-rail **ADA4692-4**
DAC, TxDAC+, dual, 16-bit, 1.2-GSPS **AD9122**
Gain Blocks, RF/IF, 4-GHz **ADL5601/ADL5602**
Generator, clock, 10-output, Ethernet **AD9571**
Gyroscope, yaw-rate, digital-output **ADIS16265**
Power Supply, 1.2-A, 16-bit level-setting DACs **AD5560**
Regulator, low-dropout, 150-mA **ADP150**
Regulator, low-dropout, dual, 200-mA **ADP5030**
Transceiver, RS-485, 16-Mbps, full-duplex **ADM1490E**

December

Amplifier, difference, dual, gain of ½ or 2 ..... **AD8279**
Amplifier, difference, precision, high-voltage **AD8209**
Amplifier, operational, micropower, rail-to-rail **ADA4051-1**
Amplifier, operational, zero crossover distortion **AD8505**
Amplifier, ultralow-noise, dual, selectable gain **AD8432**
ADC, SAR, 14-bit, 2.5-MSPS **AD7944**
ADC, sigma-delta, 8-channel, 24-bit, 4.8-kHz **AD7194**
ADCs, pipelined, 10-/12-/14-bit, 80-MSPS **AD9609/AD9629/AD9649**
ADCs, pipelined, 14-/16-bit, 125-MSPS **AD9255/AD9265**
Codecs, audio, stereo, 24-bit, 96-kHz **ADAU1381/ADAU1382**
Controller, digital, isolated power supply **ADP1043A**
Controllers, synchronous buck, 20-V **ADP1872/ADP1873**
Driver, current/voltage, programmable **AD5751**
Driver, laser-diode, differential, 11.3-Gbps **ADN2531**
Drivers, MOSFET, dual 2-A **ADP3629/ADP3630ADP3631**
Filter, video, 6-channel, SD/ED/HD **ADA4424-6**
Gyroscopes, yaw-rate, digital-output **ADIS16260/ADIS16265**
Isolators, digital, 4-channel, 1-kV rms isolation **ADuM744x**
Mixer, balanced, 500-MHz to 1700-MHz **ADL5367**
Mixer, balanced, 1200-MHz to 2500-MHz **ADL5365**
Mixer, balanced, dual, 1200-MHz to 2500-MHz **ADL5356**
Multiplexer, CMOS, 4-channel, differential, 4.5-Ω **ADG1439**
Multiplexer, CMOS, 8-channel, 9.5-Ω **ADG1438**
Multiplexer, CMOS, 8-channel, differential, 4.5-Ω **ADG1607**
Multiplexer, CMOS, 16-channel, 4.5-Ω **ADG1606**
Prescaler, divide-by-4, 4-GHz to 18-GHz **ADF5001**
Receivers, IF, dual/quad **AD6642/AD6657**
Regulators, very-low-dropout, 300-mA **ADP122/ADP123**
Reset Circuits, microprocessor, ultralow-power **ADM632x/ADM634x**
Rheostats, digital, 1024-/256-position, 1% accuracy **AD527x**
Switch, digital crosspoint, 4.25-Gbps, 16 × 16 ..... **ADN4604**
Switch, *i*CMOS, octal SPST, 9.5-Ω **ADG1414**
Switch, *i*CMOS, SPDT, 2.1-Ω **ADG1419**
Switches, *i*CMOS, dual SPST, 2.1-Ω **ADG142x**
Switches, *i*CMOS, SPST, 1-Ω **ADG1401/ADG1402**
Transceiver, multiband, 3G femtocell **ADF4602**
Transceivers, RS-485, isolated signal and power **ADM2582E/ADM2587E**

Analog Dialogue

Analog Dialogue, www.analog.com/analogdialogue, the technical magazine of Analog Devices, discusses products, applications, technology, and techniques for analog, digital, and mixed-signal processing. Published continuously for 43 years—starting in 1967—it is currently available in two versions. Monthly editions offer technical articles; timely information including recent application notes, new-product briefs, pre-release products, webinars and tutorials, and published articles; and potpourri, a universe of links to important and relevant information on the Analog Devices website, www.analog.com. Printable quarterly issues feature collections of monthly articles. For history buffs, the *Analog Dialogue* archive includes all regular editions, starting with Volume 1, Number 1 (1967), and three special anniversary issues. If you wish to subscribe, please go to www.analog.com/analogdialogue/subscribe.html. Your comments are always welcome; please send messages to dialogue.editor@analog.com or to *Dan Sheingold*, Editor [dan.sheingold@analog.com] or *Scott Wayne*, Publisher and Managing Editor [scott.wayne@analog.com].

ISSN 0161-3626

Isolation in High-Voltage Battery Monitoring for Transportation Applications

By John Wynne

Cars with wheels driven by battery-powered electric motors, continuously or intermittently, have become a hot topic. These "green" vehicles rely on batteries of series-connected cells to obtain sufficiently high voltage to operate the motor efficiently. Such high-voltage (HV) stacks are used in *all-electric vehicles* (EV)—as well as *hybrid electric vehicles* (HEV), which rely on an internal-combustion engine (ICE) for charging and (in many cases) shared propulsion. EVs must be plugged into a power source for charging; some newer hybrids are designed as *plug-in hybrid electric vehicles* (PHEV), which are considered to be essentially EVs with an ICE for range extension.

HV stacks are already used in many industries and applications outside of the transportation industry—typically in uninterruptible power supplies (UPS) to store energy from the grid in dc form; as emergency dc supplies in 48-V communications equipment; as emergency supplies in crane and lift systems; and in wind turbines for feathering the blades in an emergency. Although we discuss here the use of battery stacks in vehicles, the underlying issues are common to all types of stacks.

Battery stacks for transportation can typically involve 100 or more cells, providing hundreds of volts. Since it is generally accepted that more than 50 V or 60 V can prove lethal to human beings, and even lower voltages can damage electronic equipment—considering the stability concerns about cells using some types of electrochemical reactions—safety is a key concern. Although these stacks are inherently dangerous, they must still communicate with the cell monitoring electronics, which are usually located within the battery enclosure. Thus, the communications method must be safe and reliable.

Organizing Cells in HV Stacks

The original equipment manufacturer generally specifies the physical packing of the cells into enclosures called *packs*, which typically contain from six to 24 cells in series. Packs containing large numbers of cells are physically larger and more awkward to fit into typical vehicle spaces. The cell-monitoring integrated circuits associated with the cells are physically close to the monitored cells and are powered by the cells themselves. Whether it is essential to monitor the voltage of each cell depends on the cell chemistry. For instance, the behavior of HV stacks based upon *nickel-metal hydride* (NiMH) chemistry is very well understood, and generally no effort is made to measure individual cell voltages; it is sufficient to measure the total voltage of all the cells within a particular pack. With stacks based upon *lithium-ion* (Li-Ion) chemistry, however, it will be necessary to monitor the voltage of each cell to detect an over- or undervoltage condition on any individual cell in the string. It is not generally necessary to measure the temperature of each Li-Ion cell, but the facility to do so should be available. The electronics for monitoring a NiMH stack are thus considerably simpler than those for a Li-Ion stack. Figure 1 shows a common approach to building and monitoring an HV stack.

Cell-monitor ICs typically handle six or 12 cells. Currently, two application-specific special-purpose (ASSP) products are available from Analog Devices for cell monitoring: the AD7280,[1] intended for use as a primary monitor, is based on a high-speed multiplexed 12-bit analog-to-digital converter; another device, intended for use as a backup, or redundancy monitor, is based on a series of window comparators. It is beyond the scope of this article to discuss these products in any depth, but it is worth noting how such devices communicate in a stack configuration. Each cell establishes the common-mode level for the measurement input from the one above it. A daisy-chain interface allows each individual AD7280 in a stack to communicate directly with the next AD7280 above it or below it (and thus pass digital information up or down the stack) without needing isolation. The SPI interface of the bottommost AD7280 is used to exchange data and control signals for the whole stack with the system microcontroller. It is at this point that high-voltage galvanic isolation must be employed to protect the low-voltage electronics elsewhere in the system.

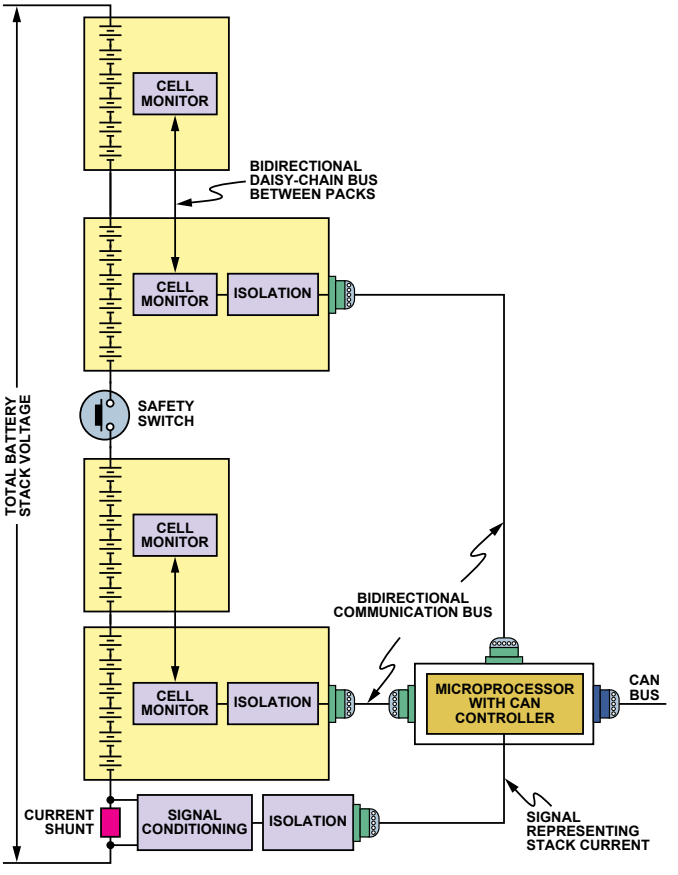


Figure 1. Serial cell monitoring and isolation in a battery stack.

In Figure 1, the string of serially connected cells has a switch or contactor placed in the middle of the string. Normally, this switch is closed at all times, whether the vehicle is in normal operation or parked. For vehicle maintenance or in emergency situations the switch is physically pulled or removed from its position to disable the stack voltage from appearing at the stack terminals. In order not to compromise the isolation provided by the open switch, it is important not to have any electronic components bridging the switch terminals. Thus, the top half of the stack should be electrically isolated from the bottom half with the switch open. This means that cell data from the top half of the stack must be communicated via its bottommost cell monitor across an isolation barrier to the microprocessor or microcontroller that is managing the flow of data into and out of the complete stack. Similarly, the bottom half of the stack must also be isolated from this microprocessor or microcontroller, so it has an identical isolation barrier to that of the top half.

In addition to the cell monitors, a current monitor is positioned somewhere in the stack to measure and report on the stack current. This monitor is generally placed at the bottom of the stack; it also needs to be considered for isolation. Hall-effect

current sensors have inherent galvanic isolation and need no further isolation circuitry. If, however, the current sensor uses a shunt element, the associated shunt monitor circuitry will require an individual isolation barrier. Current sensing using shunts is becoming very popular; it is much more stable and accurate than, yet price competitive with, Hall-effect sensing. The use of low-value shunt resistors with low-cost high-resolution monitoring electronics—such as the AD820x and AD821x families of AEC-Q100 qualified current shunt monitors, which have shipped over 100M channels into automotive sockets to date—minimizes self-heating, a traditional objection to this approach. Thus, the system in Figure 1 requires three separate isolation barriers, unless the current-sense monitor can feed into the bottommost cell monitor, sharing its isolation barrier.

Another popular approach to organizing cells in a battery stack is to group the battery packs into a series of electrically separate clusters (Figure 2). The bottommost monitor of each cluster communicates the local cell conditions across a dedicated isolation barrier back to the microcontroller on the nonisolated side.

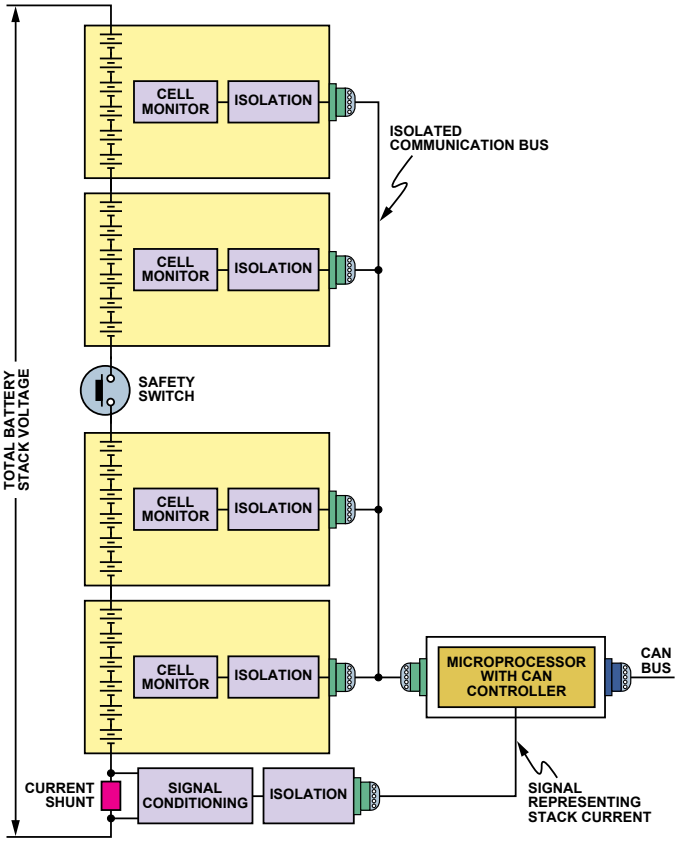


Figure 2. Battery stack with parallel access to packs.

The increased use of digital isolators makes this approach somewhat more expensive than the system shown in Figure 1, but it offers the possibility of reading back all the cell data in a much shorter time, with all cell clusters simultaneously being asked to report on what the cell monitors are seeing within the packs. Another important benefit is that it allows backup monitoring to continue in the presence of problems developing with the daisy chain, such as broken wires or poor connector contacts. The data from "off-the-air" packs can still be determined by correlating the remaining pack voltages with the overall stack voltage.

It does require more cabling, which can be problematic, since up to 75% of *electromagnetic-compatibility* (EMC) problems are considered to occur in relation to input/output (I/O) ports. The I/O port is an open gateway for electrostatic discharges or fast transient discharges or surges to enter a piece of equipment—and for interfering signals to escape, either by conduction of the spurious signals on the I/O lines or by radiation from the I/O cable. Adding more cables to a battery stack can reduce its EMC performance significantly unless careful attention is paid to the robustness of the signals and the communication protocol chosen. Because of this, the EMC performance of the I/O device connected to the port is crucial to the EMC of the entire equipment.

The popular SPI communication protocol is suitable for communicating between devices on the same printed circuit board (PCB); but single-ended signals can be difficult to transmit reliably over 24 to 36 inches of wire, especially in a noisy environment. Where digital signals are to be transmitted off board, prudent system design might include differential transceivers, such as the ADM485. These transceivers can be powered from the low-side power source, so no power is drawn directly from the cells in the stack.

Isolation Technology Is Key to Stack Communications

For battery stack voltages to get higher in order to satisfy the demands of higher power electric motors found in heavier private vehicles, as well as light delivery trucks and vans, the number of cells in battery stacks must increase. In addition to increased numbers of serially connected cells, many battery packs now contain paralleled strings of cells in order to increase the ampere-hour (AH) capacity of the overall battery pack. The cells of each parallel string must be monitored—resulting in the collection of a lot of data. The cell monitor data associated with all of these cells must be transmitted back to the battery-measuring-system (BMS) microcontroller reliably and within the system loop time requirements set by the system integrators.

Accordingly, the difficulties associated with providing reliable data communications across system-to-system boundaries have also increased. A key element to providing reliable communications across so many isolated boundaries inside a typical battery stack is *automotive-qualified isolation technology*, now available from Analog Devices. The basis of the technology is *magnetic isolation*, with transformers fabricated in a planar fashion using cost-effective standard CMOS processes (see Figure 3). This facilitates the integration of multiple isolation channels into a single component—or the integration of isolation channels with other semiconductor functions, such as line drivers and analog-to-digital converters (for example, the AD7400 isolated Σ-Δ modulator).

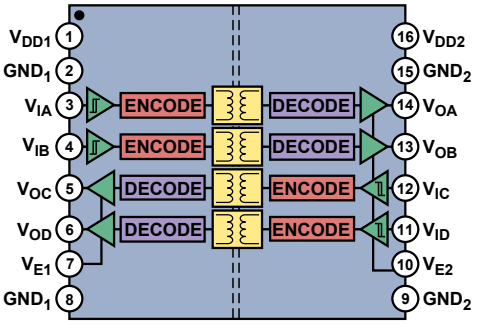


Figure 3. Functional block diagram of ADuM1402 quad isolator.

These *i*Coupler® digital isolators that, unlike optocouplers, do not degrade over the lifetime of the vehicle can accommodate the harsh operating conditions often encountered through the changing seasons. The recently released family of devices listed in Table 1—AEC-Q100 qualified to 125°C—uses the same materials as its well-established counterparts in the ADI family of *i*Coupler products, with more than 300 million channels of isolation shipped to date. The 2-channel, 3-channel, and 4-channel digital isolator

Table 1. AEC Q100-Qualified *i*Coupler Isolators

Part Number	Total Number of Channels	Reverse Direction Options			Max Data Rate (Mbps)	Max Propagation Delay (ns)	Output			Supply Range (V)	Max Temperature (°C)	Package	Price ($U.S.)
		0	1	2			Default		EN				
							H	L	Z				
2.5 kV rms Isolation													
ADuM120xA/WS	2	•	•	—	1	150	•	—	—	3.0 to 5.5	125	8-lead SOIC_N	1.21/2.13
ADuM120xB/WT		•	•	—	10	50	•	—	—	3.0 to 5.5	125	8-lead SOIC_N	1.76/3.11
ADuM120xC/WU		•	•	—	25	45	•	—	—	3.0 to 5.5	125	8-lead SOIC_N	2.44/4.30
ADuM130xA/WS	3	•	•	—	1	100	•	—	•	3.0 to 5.5	125	16-lead SOIC_W	1.61/2.42
ADuM130xB/WT		•	•	—	1	32	•	—	•	3.0 to 5.5	125	16-lead SOIC_W	2.42/3.62
ADuM140xA/WS	4	•	•	•	1	100	•	—	•	3.0 to 5.5	125	16-lead SOIC_W	2.15/3.22
ADuM140xA/WS		•	•	•	10	50	•	—	•	3.0 to 5.5	125	16-lead SOIC_W	2.22/4.82

families in the table have data rates up to 25 Mbps and propagation delays as low as 32 ns.

The planar transformers are inherently bidirectional; therefore, signals can pass in either direction. All possible combinations of drive and receive channels within the total number of channels are available. For instance, the 2-channel ADuM120xW, 3-channel ADuM130xW, and 4-channel ADuM140xW, alone or together, offer seven different channel configurations (4-0, 3-1, 2-2, 3-0, 2-1, 2-0, 1-1), ensuring an optimized solution for all situations. Figure 4 summarizes the various configurations available.

Two of the most distinguishing features of the *i*Coupler technology are the ability to support high data rates and to operate with low supply currents. The supply current drawn by an *i*Coupler channel is largely a function of the data rate it is carrying. For 3-V operation, the total power supply current—for both sides and all four channels of the ADuM140xWS—is 1.6 mA typical (4 mA maximum) at a data rate up to 2 Mbps. Low-power operation is important since, on the isolated or "hot" side of the ADuM140xWS, the power comes from the cells themselves through a voltage regulator. The monitors are also powered from this same voltage source, so the less power taken by all elements of the monitoring and communicating circuitry the better. All isolation products are available in small, low-profile, surface-mount 8-lead SOIC_W or 16-lead SOIC_W packages and come with safety certifications from UL, CSA, and VDE. They feature isolation ratings up to 2.5 kV rms and working voltages up to 400 V rms.

*i*Coupler Technology Begets *iso*Power Devices: Integrated, Isolated Power

One of the most exciting developments of *i*Coupler technology is the integration of both power transmission and signal transmission within the same package. With microtransformers similar to those used for signal isolation, power can now be transferred across an isolation barrier—allowing fully integrated isolation for remotely powering the data isolators in the battery packs. Local power is supplied to an oscillating circuit that switches current through a chip-scale air core transformer. Power transferred to the isolated side is rectified and regulated to either 3.3 V or 5 V. The isolated-side controller provides feedback regulation of the output by creating a PWM control signal that is sent back to the local side by a dedicated *i*Coupler data channel. The PWM control signal modulates the oscillator circuit to control the power being sent to the isolated side. The use of feedback permits significantly higher power and efficiency.

The ADuM540xW devices are 4-channel digital isolators that include an *iso*Power®, integrated, isolated dc-to-dc converter, which provides up to 500 mW of regulated, isolated power at either 5.0 V from a 5.0-V input supply or 3.3 V from a 3.3-V supply. As with the standard *i*Coupler devices, a variety of channel configurations and data rates is available. Because an *iso*Power device uses high-frequency switching elements to transfer power through its transformer, special care must be taken during PCB layout to meet emissions standards. Refer to AN-0971 Application Note, *Recommendations for Control of Radiated Emissions with isoPower Devices*, for details on board-layout considerations. The ADuM540x family is currently undergoing AEC-Q100 qualification.

References

[1] Information on all ADI components can be found at www.analog.com.

Author

John Wynne [john.wynne@analog.com] is a precision converter marketing manager at Analog Devices.

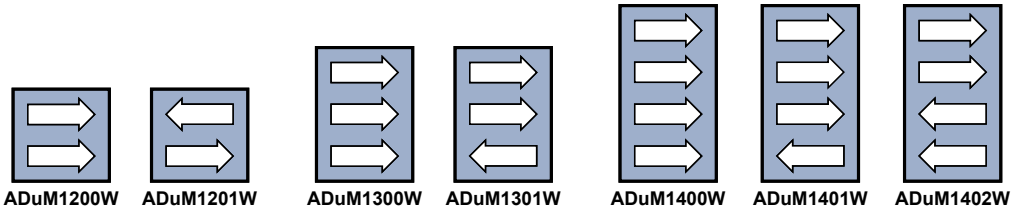


Figure 4. Seven different configurations with the ADuM120xW/ADuM130xW/ADuM140xW.

Synchronizing Device Clocks Using IEEE 1588 and Blackfin Embedded Processors

By Jiang Wu and Robert Peloquin

Introduction

The IEEE 1588 standard, introduced in 2002, defines a protocol to synchronize distributed clocks on a network. It is becoming the preferred clock synchronization method for many different applications, including test and measurement, telecommunications, and multimedia streaming. This standardized method for synchronizing clocks is cost-effective, supports heterogeneous systems, and provides nanosecond-level synchronization precision.

This article provides an introduction to both the original IEEE 1588-2002 standard and the enhancements incorporated as part of the updated IEEE 1588-2008 version. Dedicated hardware support for IEEE 1588 has been integrated into the ADSP-BF518[1] Blackfin® embedded processor because of the increasing importance of IEEE 1588 in some of its targeted applications. An overview of its capabilities is provided, followed by an example showing clock synchronization performance results obtained by an ADSP-BF518 processor solution.

What Time Is It?

It is common for a system to need to maintain its own sense of time using a local oscillator. Figure 1 shows how hardware and software combine to generate time information within a system.

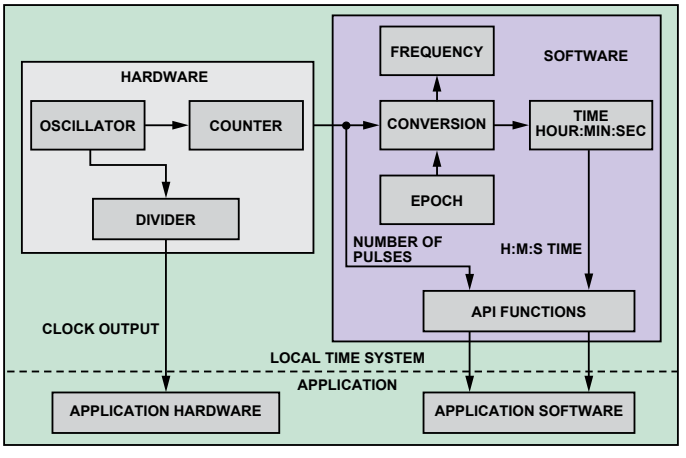


Figure 1. Local timekeeping.

This time information can be used by both hardware and software resources within the system. In hardware, one or more physical clock signals (clock outputs) are derived from the oscillator's clock and can be used to drive or trigger other parts of the system. The time maintained in software is typically referred to as *system time*. The system time can be represented in the form of numbers of clock pulses or in second/nanosecond notation. The system software derives the time from the number of oscillator clock pulses and its frequency information, and provides *application-programming-interface* (API) functions that other parts of the software use to retrieve and set the time. If an absolute time is desired, the provided time is associated with a predefined epoch, which identifies a reference point in time.

Synchronize Your Watches

Many applications require two independent devices to operate in a synchronized fashion. If each device were to rely solely on its own oscillator, differences between the specific characteristics and operating conditions of the individual oscillators would limit the ability of the clocks to operate synchronously. Some possible simplistic solutions to address these limitations include:

- *All the devices could use a single physical oscillator.* This is only feasible for distributed systems in close proximity; a high-frequency clock signal cannot be reliably delivered over a long distance.
- *All the devices could utilize oscillators with nearly identical characteristics*. This approach is impractical due to the difficulty of acquiring nearly identical oscillators and keeping them from drifting apart over time. More importantly, each oscillator will be subjected to different operating conditions.
- *If all the devices are interconnected via a communications network such as Ethernet, they can dynamically adjust their individual clocks to a single "master" clock by exchanging time messages over the network*. With *network time protocol* (NTP), the traditional time synchronization protocol, every device in the system adjusts its clock according to the time information it retrieves from an NTP time server. However, this protocol can only achieve synchronization accuracy on the order of milliseconds.

IEEE 1588 defines a newer protocol capable of nanosecond synchronization accuracy. How it can achieve this level of clock synchronization is discussed in the following sections.

What IEEE 1588 Does

The IEEE 1588 standard defines a protocol for time-synchronizing devices that are geographically dispersed but interconnected by some form of communications technology, for example, Ethernet. By exchanging timing messages between devices they can maintain the same absolute system time, which is represented in seconds and nanoseconds.

An intuitive way to achieve this goal is for one device, which has the "best" (most accurate) clock, and is designated as the *master-clock* device, to broadcast its time to the other devices. The other devices will adjust their times to match the time sent by the master clock. This solution has several limitations, though:

1. The master-clock device cannot broadcast the time at infinitesimal intervals, so the "slave" clock devices have to use their own independent and "inferior" oscillators to interpolate the time points between two broadcasts from the master-clock device. This results in degraded synchronization during the time between updates from the master clock.
2. Delays inevitably exist on the broadcast path, with magnitudes depending on the communications technology—the time that a physical signal takes to travel along a wire from one device to another, for example. This delay results in an additional offset between the master clock and each slave clock.
3. Differences among the broadcast paths between the master-clock device and each slave-clock device will further degrade the synchronization between individual slave-clock devices.

IEEE 1588 specifies a protocol that solves the second and third problems by measuring path delay. It also allows the slave clock to be adjusted to match the master clock's pace so as to mitigate the first problem. Where possible, the first problem can be further reduced by using smaller broadcasting intervals and higher-quality oscillators.

How IEEE 1588 Measures Communication Delay

IEEE 1588-2002[2] defines four messages to measure the communication delay of the forward (*master to slave*) and backward (*slave to master*) paths: *Sync*, *Followup*, *DelayReq*, and *DelayResp*. The newer version, IEEE 1588-2008,[3] provides further mechanisms to measure the *peer-to-peer delay* with three additional messages: *PdelayReq*, *PdelayResp*, and *PdelayRespFollowup*.

Among these messages, Sync, DelayReq, PdelayReq, and PdelayResp, so-called *event* messages, must be *time-stamped* (recording the local time) when they leave and arrive at a device. There are two techniques to time-stamp packets:

1. *Software time-stamp* occurs when the messages are handled by the software. Usually occurring in the message's receive/transmit *interrupt service routine* (ISR), the time-stamp is the current value of the system time.
2. *Hardware time-stamp* occurs when the messages physically arrive at or leave the device. The time-stamp operation is executed by hardware, which maintains its own continuous time information.

Either time-stamp method is acceptable in IEEE 1588, but a hardware time-stamp can provide significantly better precision, as will be shown below.

Delay from Master-Clock Device to Slave-Clock Device

The messages Sync and Followup are sent by the master-clock device; it is a slave-clock device's responsibility to receive them and calculate the communication path delay from the master-clock device to the slave-clock device.

In Figure 2, at time Tm1, the master-clock device software reads the current local system time (Tm1, the software time-stamp), inserts it into a Sync message, and sends the message out. The message leaves the master-clock device at a later time, Tm1', which is the hardware time-stamp. It arrives at slave-clock hardware at Ts1' (slave-clock device local time), and is received by the slave-clock device software at a later time, Ts1. The software will read the hardware time-stamp to get Ts1'. If there is no communication delay, Ts1' should be equal to (Tm1' + Tms), where Tms is the time difference between master clock and slave clock. The protocol's ultimate goal is to compensate for this difference.

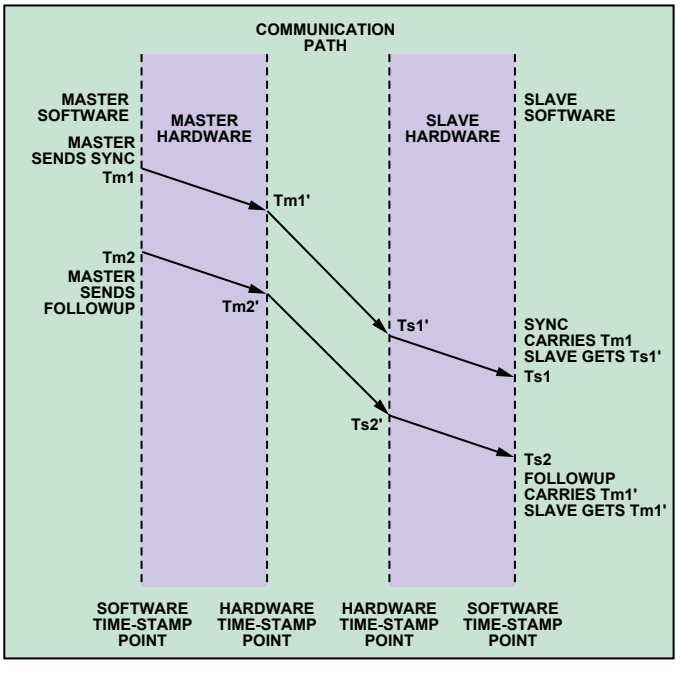


Figure 2. Measuring communication delay between master-clock and slave-clock devices.

After the Sync message has been sent, the master-clock device software reads the Sync message's departure time, Tm1', through the time-stamping unit, inserts it into a Followup message, and sends that message out at Tm2. This message is received by slave-clock device software at Ts2. At this point, the slave-clock device software has the two times, Ts1' (Sync arrival time) and Tm1' (Sync departure time). The master-to-slave path delay, Tmsd, is determined by Equation 1.

$$Tmsd = (Ts1' + Tms) - Tm1' \quad (1)$$

Delay from Slave-Clock Device to Master-Clock Device

The DelayReq message is sent by the slave-clock devices, and the DelayResp message is sent by the master-clock device in response. With these messages, the slave-clock devices can calculate the communication path delay from the slave-clock device to the master-clock device.

At time Ts3 (Figure 3), the slave-clock device software reads the current local system time (Ts3), inserts it into a DelayReq message, and sends the message out. After the message is sent, the slave-clock device software reads the time-stamp to get the departure time of the message, Ts3', and waits for the response from the master-clock device.

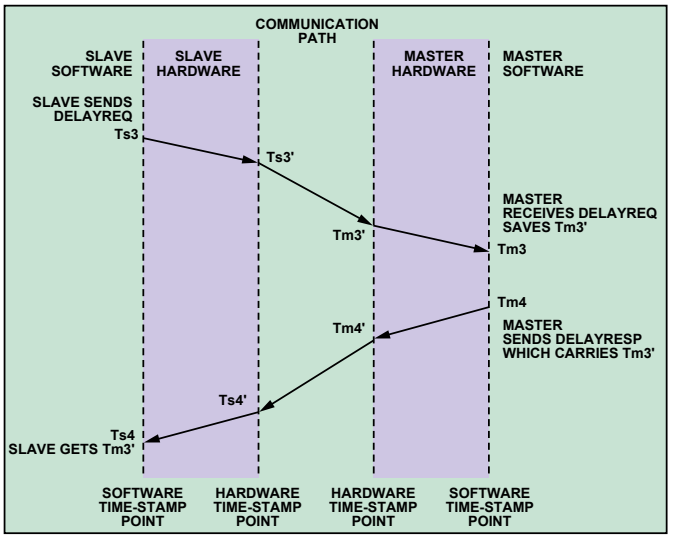


Figure 3. Measuring slave-master communication delay.

The DelayReq message arrives at the master-clock device at a later time, Tm3', and is processed by the master software at Tm3. The software then reads the time-stamp to get the arrival time, Tm3', puts it into the DelayResp message, and sends to a slave-clock device at Tm4. When the slave-clock device software receives the DelayResp message at Ts4, it can extract the time, Tm3', and calculate the slave-to-master delay, Tsmd, by Equation 2.

$$Tsmd = Tm3' - (Ts3' + Tms) \quad (2)$$

In both Equation 1 and Equation 2, there is an unknown variable, the master-slave time difference, Tms. So it is not possible to get either Tmsd or Tsmd individually. However, if one makes the usually acceptable assumption that the communication path is symmetric

$$Tmsd = Tsmd = Td \quad (3)$$

—a key assumption for IEEE 1588 to work correctly—then, adding Equation 1 and Equation 2 gives

$$Td = \frac{1}{2}[(Ts1' - Tm1') + (Tm3' - Ts3')] \quad (4)$$

All these calculations are performed by the slave-clock devices, since it is they who seek to synchronize themselves to the master-clock device. They get Tm1' from master-clock device's Followup message, Ts1' from their Rx (reception) time-stamping, Ts3' from their Tx (transmission) time-stamping, and Tm3' from the master-clock device's DelayResp message.

How to Calculate the Time Difference Between a Slave Clock and Master Clock

Once the communication path delay, Td, is obtained, the slave-master time difference is easy to calculate, using either Equation 1 or Equation 2, as shown in Equation 5 and Equation 6.

$$Tms = Td - (Ts1' - Tm1') \quad (5)$$

$$Tms = (Tm3' - Ts3') - Td \quad (6)$$

How to Adjust the Time of a Slave-Clock Device

With the time difference from the master clock known, each slave-clock device needs to adjust its own local time to match the master clock. This task has two aspects. First, slave-clock devices need to adjust their absolute time by adding the time difference to make their time perfectly match the master-clock time at this moment. Then, each slave-clock device needs to adjust its clock frequency to match the frequency of the master clock. We cannot rely on the absolute time alone, since the time difference is applied only at a certain period and could be either positive or negative; as a result, the adjustment will make the slave-clock time jumpy or even run backward. So, in practice, the adjustment takes two steps.

1. If the time difference is too big, for example, larger than one second, absolute time adjustment is applied.
2. If the time difference is small, a percentage change of frequency is applied to slave clocks.

Generally speaking, the system becomes a control loop, where master-clock time is the reference command, slave-clock time is the output tracking the master-clock time, and their difference drives the adjustable clock. PID control, which is commonly used by many IEEE 1588 implementations, could be used to achieve specific tracking performance. Figure 4 illustrates this control loop.

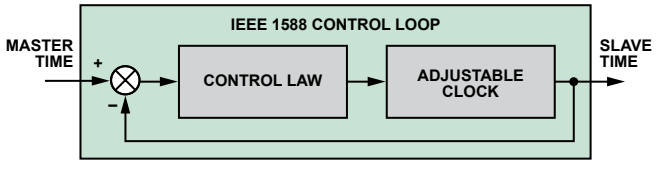


Figure 4. IEEE 1588 control loop.

Peer-to-Peer Delay

The revised version, IEEE 1588-2008, introduces a new mechanism for measuring path delay, called *peer-to-peer* (P2P) delay. By contrast, the master-slave mechanism discussed in the previous sections is *end-to-end* (E2E) delay. In an IEEE 1588-2008-capable network, a master-clock device can be linked to slave-clock devices either directly or through multiple hops (stages). The E2E delay is actually the *total* delay from a master-clock device to a slave-clock device, including all the hops in between. However, the P2P delay is limited to two directly connected devices. The overall delay along the path is the sum of the P2P delay of all the hops. From the perspective of preserving path symmetry, the P2P mechanism provides better accuracy.

As noted earlier, IEEE 1588-2008 includes three additional messages, PdelayReq, PdelayResp, and PdelayRespFollowup, to measure P2P delay. They work in a manner similar to that explained above. Reference 3 provides more details.

Factors Affecting Synchronization Performance

Well-designed IEEE 1588 devices are capable of achieving highly accurate clock synchronization, but it is important to recognize the key factors that directly affect performance. Some of these include:

1. **Path delay**: As noted earlier, the path delay measurement of IEEE 1588 assumes that the communication-path delays are symmetrical, that is, the transmission delay of the forward path is equal to the reverse transmission delay. In addition, the delay should not vary during the delay measurement. Variation in delay during measurement will produce asymmetry and delay jitter, which will have a direct impact on the synchronization precision. While delay symmetry and jitter cannot be controlled *outside* the boundaries of an IEEE 1588 device, both path symmetry and jitter can be improved *within* the device if measurements are based on *hardware* time-stamping. Hardware time-stamping eliminates the significant jitter resulting from software time-stamping—due to interrupt latency, context switch, and thread scheduling.
2. **Drift and jitter characteristics of clocks**: The frequency and phase of the master clock represent the inputs of the tracking control system, and the slave clock is the control object. Any time-varying behavior of the master clock will act as a disturbance to the control system and result in both steady-state- and transient errors. Clocks with less drift and jitter will, therefore, improve synchronization accuracy.
3. **Control law**: The control method determines how the errors in the slave-clock-device time are corrected in the adjustment of the slave clock. The control-law parameters, including settling time, overshoot, and steady-state error, will directly affect clock synchronization performance.
4. **Resolution of the clocks**: As shown in Figure 1, the resolution of the local time is determined by the frequency of the clock; the minimum increment of time is one period of the clock signal. The IEEE 1588 protocol runs on a time with a resolution of 1 ns for IEEE 1588-2002 and 2^{-16} ns for IEEE 1588-2008. It is not practical to have a clock of 2^{16}(!) GHz (or even 1 GHz). The quantization of the local clocks is expected to affect the precision of local time measurement and control.
5. **How often Sync messages are issued**: The frequency with which the slave clocks are updated ultimately affects the precision of synchronization. A longer period usually leads to larger time errors observed at the next Sync, since the time error is the integral accumulation of the slave-clock frequency error.
6. **How often delay measurement is conducted**: Delay measurement is performed periodically, at intervals based on the expectation that the delay does not change significantly between adjacent samples. If the IEEE 1588 network experiences large delay variations, then increasing the delay-measurement frequency will improve clock-synchronization performance.

Which Is the Master-Clock?

Having considered how to accurately determine the time difference between master-clock devices and slave-clock devices, a relevant question is how to determine which device, among possibly hundreds of interconnected devices, will serve as the master clock.

IEEE 1588 defines a method called the *best master clock* (BMC) algorithm to choose the master clock device. For this approach, every device of an IEEE 1588 network maintains a data set describing the nature, quality, stability, unique identifier, and preference of its local clock. When a device joins an IEEE 1588 network, it will broadcast the dataset of its own clock and receive the datasets from all other devices. Using the datasets of all the participating devices, every device runs the same BMC algorithm to decide on the master clock and its own future status (master clock or slave clock). Because the same algorithm is executed independently by all the devices on the same data, all will come

to the same conclusion without requiring any negotiation among them. More information about the details of the BMC algorithm can be found in References 2 and 3.

ADSP-BF518 Processor's Support for IEEE 1588

The Analog Devices ADSP-BF518 processor recently joined ADI's Blackfin DSP family. Like its predecessor, the ADSP-BF537,[4] it has a built-in *Ethernet media-access controller* (EMAC) module. Its capability to support EMAC functionality within the IEEE 1588 standard is extended by an additional *TSYNC* module, as well as extra features to support a wide range of IEEE 1588 applications on Ethernet. Figure 5 shows the block diagram of the TSYNC module. The *ADSP-BF51x Blackfin Processor Hardware Reference* provides additional information.[5]

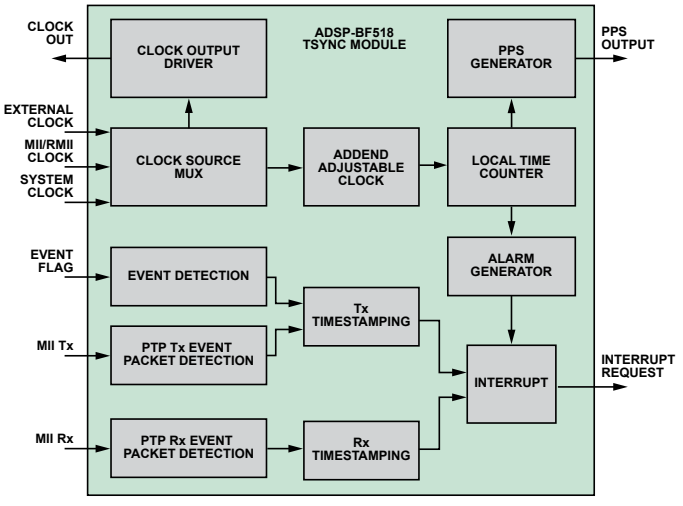


Figure 5. Block diagram of the ADSP-BF518 processor's TSYNC module.

Packet Detection

The ADSP-BF518 processor can detect and provide hardware time-stamps for all IEEE 1588 event messages, including both incoming and outgoing packets. The precision of an IEEE 1588 system depends significantly on both the accuracy of the event-message time-stamps and on where they are taken, as these affect the requirement for symmetry and constancy of path delay. The ADSP-BF518's TSYNC module keeps monitoring the hardware interface between the MAC controller and the Ethernet *physical interface transceiver* (PHY), that is, the *media independent interface* (MII), and produces a hardware time-stamp whenever it detects an event message—a capability promoting higher synchronization precision with the ADSP-BF518.

The detection of event messages, designed to be programmable, can basically be configured to support either IEEE 1588-2002 (default) or IEEE 1588-2008. Furthermore, this programmability allows for the support of future versions of IEEE 1588, as well as other general protocols that require time-stamping—including being configured to time-stamp every Ethernet packet coming into and out of the processor.

Flexible Clock Sources

The properties of local clocks are important for the performance of an IEEE 1588 system. To satisfy requirements of a variety of applications, the ADSP-BF518 processor allows three options for the local clock source: system clock, external clock, or Ethernet clock. If the application has a specific clock requirement, it can choose *external clock* and provide a customized clock source. The *Ethernet clock* option can offer good precision if the master-clock devices and the slave-clock devices are connected back-to-back, since the clock is inferred from the Ethernet lines, and the two devices are running on the same clock. A general application can take the *processor's system clock* as its clock source.

The selected source clock is also driven by the TSYNC module as an output of the processor, via the specific pin *Clockout*, to be used by other parts of the system for local time information.

PPS Output

The *pulse-per-second* (PPS) signal is a physical representation of time information. It is nominally a 1-Hz signal with a pulse at each one-second transition of time. It can be used to control local devices or to provide an auxiliary time channel in case of network failure. It can also be used in testing. The phase difference between PPS signals at two devices is a physical measurement of their time offset.

The ADSP-BF518 processor provides a flexible PPS output. It uses a programmable *start time* (*PPS_ST*) and period (*PPS_P*) to generate a signal with pulses occurring at the times (PPS_ST + $n \times$ PPS_P), where n = 1, 2, 3... In the basic usage, the PPS signal can be created simply by setting PPS_P to 1 second, and PPS_ST to any future instant as a multiple of seconds. This PPS output capability allows for its use as the reference for generation of a periodic signal with a fully programmable frequency and start time.

Auxiliary Snapshot

Some applications may need to time-stamp a certain event indicated by the toggle of a flag signal. The ADSP-BF518's TSYNC module facilitates this request by providing an auxiliary *snapshot* function, using a dedicated pin to accept an external flag. Toggling the flag will trigger the module to capture the current local time in a time-stamp register for software to access.

Alarm

If an application needs to execute a task at a specific time, it can make use of the *alarm* feature of the TSYNC module. This feature allows an absolute local time to be set so as to trigger a processor interrupt when the time arrives. The software can then service the interrupt and run the task.

Adjustable Clock

The adjustable clock of the TSYNC module is an *addend-based* clock. As shown in Figure 6, it takes a fixed input clock signal and outputs a "pulse-steal" version of the input: the value of *addend* is added to the accumulator at each input clock, and each time the accumulator overflows the carry bit drives the *local-time counter*, which gives the local time in terms of the number of pulses counted. The frequency of the local clock can be adjusted by changing the addend, since the addend decides how often the accumulator overflows, and so how often the local-time counter increments. If the frequency of the input clock is F_{in}, and the value of addend is A, then the local clock frequency will be

$$F_{out} = F_{in} \times \frac{A}{2^{32}} \tag{7}$$

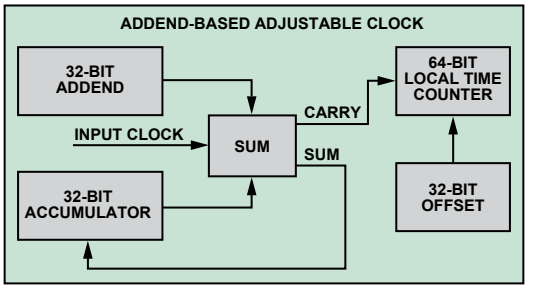


Figure 6. Addend-based adjustable clock.

Implementation of IEEE 1588 on the ADSP-BF518 Processor

A complete IEEE 1588-2008-compliant system was built on an ADSP-BF518 processor as shown in Figure 7.

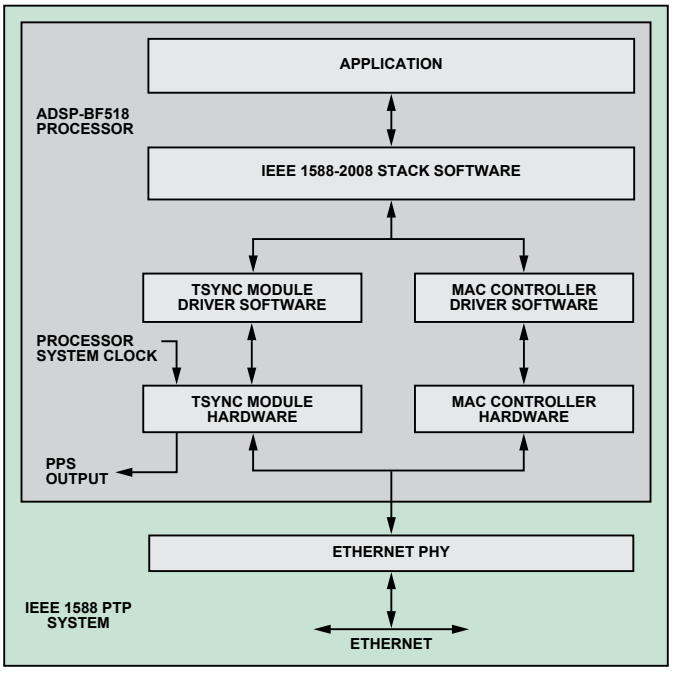


Figure 7. An implementation of IEEE 1588 on the ADSP-BF518.

The TSYNC module of the processor detects incoming and outgoing IEEE 1588 messages and uses hardware to time-stamp event messages. The IEEE 1588 stack software, provided by IXXAT (IXXAT Automation GmbH), implements the message-exchange protocol required by the standard. It makes use of the TSYNC driver to read, write, and adjust the TSYNC clock, and uses the MAC controller driver to send and receive messages on the Ethernet MAC layer (Layer 2 of the Open-Systems Interconnection Model). It also implements the control law and filtering of P2P delay measurements. The Ethernet PHY is National Semiconductor DP83848,[6] chosen because of its low jitter delay characteristics. For simplicity, the processor's system clock (80 MHz) was chosen to be the TSYNC module clock source.

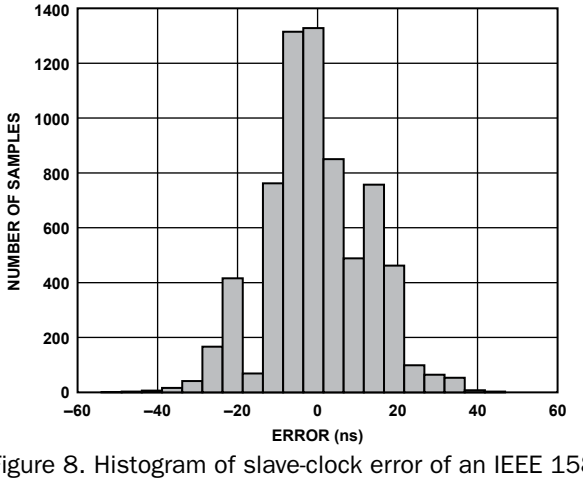


Figure 8. Histogram of slave-clock error of an IEEE 1588 system on ADSP-BF518.

Figure 8 shows the clock synchronization performance of the device as a histogram of the measured error between two identical ADSP-BF518 IEEE 1588 systems. 6938 measurements were taken over a period of approximately 1700 seconds. The resulting mean error is 0.015 ns, and the standard deviation is 12.96 ns. A Sync message interval of 0.25 seconds was used for this test.

Conclusion

The IEEE 1588 standard provides a highly accurate, low-cost method for synchronizing distributed clocks. While hardware support is not explicitly required for IEEE 1588, hardware-assisted message detection and time stamping is critical to achieve the highest level of synchronization precision. The ADSP-BF518 processor provides hardware support for both IEEE 1588-2002 and IEEE 1588-2008, including features that can support a wide range of applications. High-precision clock synchronization has been demonstrated by implementing IEEE 1588 technology using the ADSP-BF518 processor and the IXXAT IEEE 1588-2008 protocol software.

References

[1] ADSP-BF518 data sheet. http://www.analog.com/en/embedded-processing-dsp/blackfin/adsp-bf518/processors/product.html.

[2] IEEE Std. 1588-2002. *IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems*. http://ieee1588.nist.gov/PTTI_draft_final.pdf.

[3] IEEE Std. 1588-2008. *IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems*. http://ieee1588.nist.gov.

[4] ADSP-BF537 data sheet. http://www.analog.com/en/embedded-processing-dsp/blackfin/adsp-bf537/processors/product.html.

[5] *ADSP-BF51x Blackfin Processor Hardware Reference Preliminary, Revision 0.1* (Preliminary). January 2009. Analog Devices, Inc. http://www.analog.com/static/imported-files/processor_manuals/bf51x_hwr_rev_0-1.pdf.

[6] AN-1507: *DP83848 and DP83849 100Mb Data Latency*. 2006. National Semiconductor Corporation. http://www.national.com/an/AN/AN-1507.pdf.

Authors

Dr. Jiang Wu [jiang.wu@analog.com] joined Analog Devices in 2006, where he works on real-time embedded systems and digital processing. In 2004, he received a PhD in electrical engineering from the University of Rhode Island. In 1996 and 1993, respectively, he received MS and BS degrees in automation, both from the Beijing Institute of Technology. His graduate research work was on modeling and instrumentation of biomedical systems. Prior to ADI, Jiang worked as a system engineer at Vivoda Communications.

Robert Peloquin [robert.peloquin@analog.com] joined Analog Devices in 2000. As a senior applications engineer, he contributes to many different aspects of ADI's digital signal processor solutions. Some recent areas include Ethernet AVB and IEEE 1588. Prior to joining ADI, Bob worked at the Naval Undersea Warfare Center performing applied research for unmanned undersea vehicle technologies. He holds a BSEE degree from Syracuse University and a MSEE degree from the University of Massachusetts, Dartmouth.

Using Isolated RS-485 in DMX512 Lighting Applications

By Hein Marais

Introduction

The western theatrical age started in Greece circa 500 B.C. Open-air theaters used the sun as their main lighting source, but often added lanterns to indicate nighttime scenes. These early lighting applications have evolved into the more complex systems available today.

Modern lighting equipment includes dimmers, flashing lights, moving lights, colored lights, and gobos[1] (GOes Before Optics). These lighting systems are often controlled over long distances—up to 4000 feet—using the DMX512 communications protocol.[2]

What is DMX512?

DMX512 is a standard developed by the Entertainment Services and Technology Association (ESTA).[3] This standard describes a method of digital data transmission between controllers and controlled lighting equipment and accessories, including dimmers and related equipment. The physical electrical interface is specified by EIA/TIA-485,[4] also known as RS-485.

The DMX512 standard, which specifies an 8-bit asynchronous serial protocol and 250-kbps data rate, is designed to carry repetitive control data from a single controller to one or multiple receivers. The control data on the primary link consists of up to 513 slots that are sent in packets over a balanced transmission line.

Information, in an 8-bit format, is sent sequentially to the various nodes. Values range from 0 to 255, where 0 indicates the *off* condition and 255 indicates the *on* condition. A *break* condition lasting two frames indicates the start of a sequence of 512 values. A high level for at least 8 µs indicates the start of the first byte.

Discrete DMX512 System Configuration

A DMX512 port consists of four signals (Data1+, Data1–, Data2+, and Data2–) plus a common reference. The primary data link is formed by Data1+ and Data1–. An optional secondary data link is formed by Data2+ a nd Data2–. The paired links are configured as a bidirectional half-duplex RS-485 communications network.

The DMX512 standard specifies a system using ground-referenced transmitting devices and isolated receiving devices. The receiving devices are isolated to protect expensive lighting equipment from harmful current surges.

Figure 1 shows a discrete implementation of an isolated DMX512 receiver. An isolated power supply is generated by a transformer driver driving the primary side of a transformer. The output of the transformer is rectified and regulated to create an isolated 5-V supply. The data and control signals for the RS-485 transceiver are isolated using optical isolation.

The ADM485 RS-485 transceiver converts a control signal received on the A and B pins into a serial output on the RXD pin. This signal is optically isolated and connected to the UART input of the ADuC7020 precision analog microcontroller. The ADuC7020 software decodes the message and outputs logic-level signals to a digital-to-analog converter (DAC). The ADTL084 JFET-input op amps buffer the DAC outputs to provide 0 V to 10 V signals.

The ADuC7020 software sends a response to indicate that the message was received correctly. This signal is optically isolated from the ADM485, which outputs a signal on the A and B pins.

DMX512 System Configuration Using the ADM2487E

Figure 2 shows a simpler, more integrated, isolated DMX512 receiver using the ADM2487E isolated RS-485 transceiver. An on-chip oscillator outputs a pair of square waves that drive an external transformer to provide the 3.3-V isolated power required by the bus side. The logic side of the device is powered with a 3.3-V or 5-V supply. The ADM2487E employs *i*Coupler®[5] digital isolation technology to combine a 3-channel isolator, a 3-state differential line driver, and a differential input receiver into a single package. TXD, RXD, DE, and $\overline{RE}$ pins connect directly to the ADuC7020 UART.

The ADM2487E transceiver, suitable for half-duplex or full-duplex communication on multipoint transmission lines, operates with data rates up to 500 kbps. It provides 2.5-kV rms isolation—certified to Underwriters Laboratory (UL) and VDE standards—and ±15-kV ESD protection.

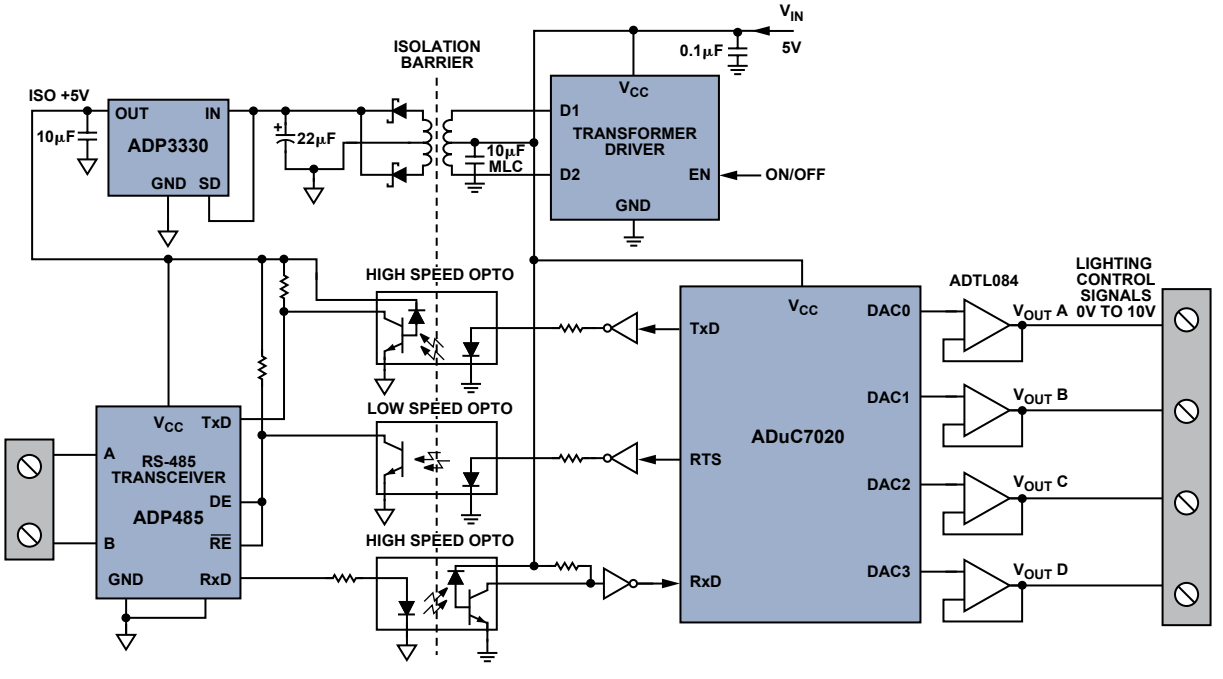


Figure 1. Discrete DMX512 receiver block diagram.

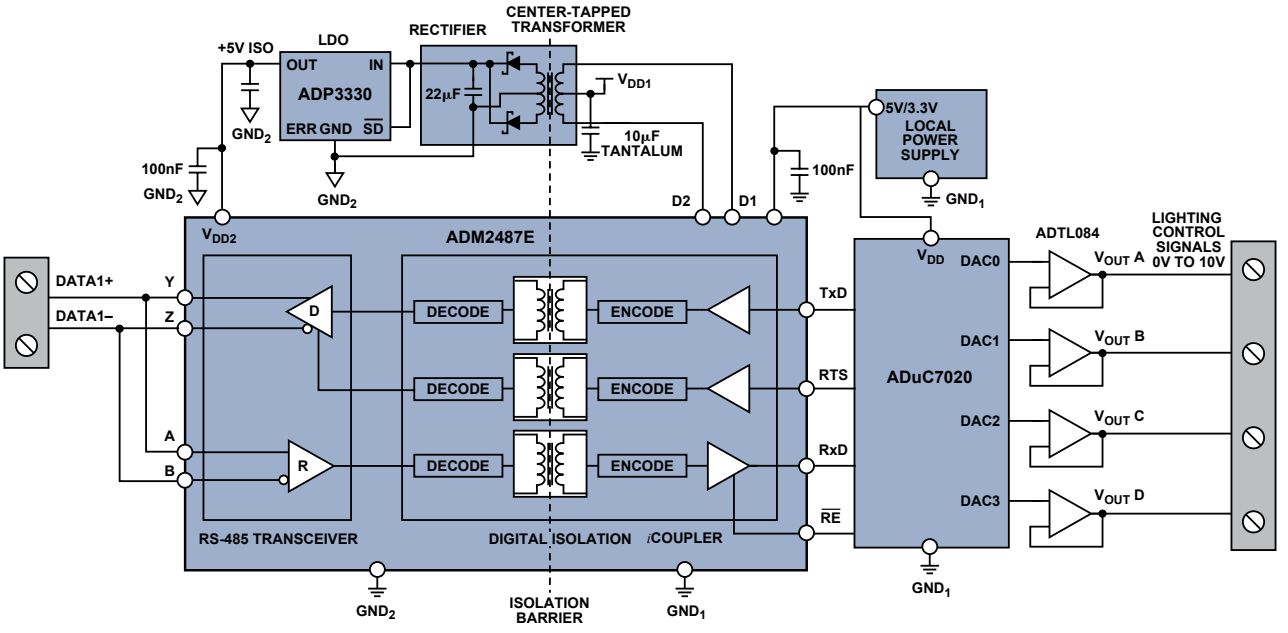


Figure 2. ADM2487E DMX512 receiver block diagram.

For half-duplex operation, the transmitter outputs and receiver inputs share the same transmission line by externally linking transmitter output Pin Y to receiver input Pin A, and transmitter output Pin Z to receiver input Pin B. Designed for balanced transmission lines, the ADM2487E complies with TIA/EIA 485 A-98 and ISO 8482[6]:1993 standards.

Current-limiting and thermal shutdown features protect against output short circuits and situations where bus contention might cause excessive power dissipation. Fully specified over the –40°C to +85°C industrial temperature range, the ADM2487E is available in a 16-lead, wide-body SOIC package.

The ADM2487E features an open- and short-circuit fail-safe receiver input design, eliminating the need for external biasing resistors. The low-input-current receiver design (125 µA) enables up to 256 nodes to be connected on the same bus.

Replacing the discrete DMX512 receiver implementation with the ADM2487E implementation provides a space-saving, more robust, more reliable system.

Why Is Isolation Important?

Sudden voltage surges between two or more interconnected circuits can cause damage to expensive equipment. Electrical isolation is designed to protect expensive equipment from these voltage surges. Because of the distance between nodes, DMX512 transmitters and receivers require different power supplies. This will increase the impedance of the earth ground, making it more likely that ground currents from other sources will find their way into the link's ground wire. Isolating the link reduces or even eliminates these problems. Galvanic isolation, shown in Figure 3, is required if there is no guarantee that the potentials at the earth grounds of different nodes in the system are within the common-mode range of the receiver.

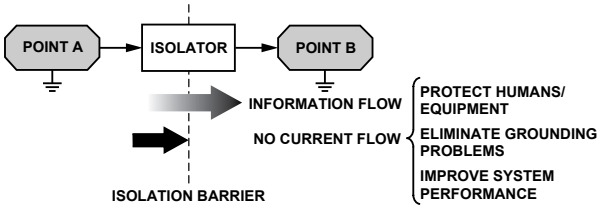


Figure 3. Galvanic isolation allows information flow, prevents ground-current flow.

The ADM2487E integrates galvanic isolation with the transceiver to create robust protection against harmful current surges. An ideal solution to implement an isolated DMX512 receiver, it will reduce the overall form factor, improve reliability, and increase robustness.

References

(*Information on all ADI components can be found at www.analog.com*)

[1] http://en.wikipedia.org/wiki/Gobo_(lighting).

[2] http://en.wikipedia.org/wiki/DMX512.

[3] http://en.wikipedia.org/wiki/Entertainment_Services_and_Technology_Association.

[4] http://en.wikipedia.org/wiki/EIA-485.

[5] www.analog.com/en/interface/digital-isolators/products/CU_over_iCoupler_Digital_Isolation/fca.html.

[6] www.iso.org/iso/catalogue_detail.htm?csnumber=20954.

Further Reading

ANSI E1.11 – 2008: Entertainment Technology—USITT DMX512-A, Asynchronous Serial Digital Data Transmission Standard for Controlling Lighting Equipment and Accessories.

USITT DMX512, DMX512/1990, DMX512-A.

AN-960 Application Note, *RS-485/RS-422 Circuit Implementation Guide*.

Author

Hein Marais [hein.marais@analog.com] graduated from the University of Stellenbosch, South Africa, in 2001 with a bachelors degree in electronics. He started his career in the South African Air Force working on electronic warfare systems. In 2003, he joined Grintek Communication Systems, where he was involved in the design of software and hardware for military radios. In 2007, Hein joined ADI, where he is currently a product applications engineer for the High Speed Interconnect Group, working on RS-485 and LVDS products.

Designing High-Performance Phase-Locked Loops with High-Voltage VCOs

By Austin Harney

Introduction

The *phase-locked loop* (PLL) is a fundamental building block of modern communication systems. PLLs are typically used to provide the *local-oscillator* (LO) function in a radio receiver or transmitter; they are also used for clock-signal distribution and noise reduction—and, increasingly, as the clock source for high-sampling-rate *analog-to-digital* (A/D) conversion.

As feature size has shrunk in integrated-circuit processing, device supply voltages, including supplies for PLLs and other mixed-signal functions, have followed downward. However, the practical technology for *voltage-controlled oscillators* (VCOs), a critical element of PLLs, has not decreased as rapidly. Many high-performance VCO designs are still implemented with discrete circuitry that may require supply voltages as great as 30 V. This imposes a challenge for today's PLL or RF system designer: to interface the low-voltage PLL IC with a higher voltage VCO. The level-shifting interface is typically implemented using active filter circuitry—to be discussed below.

This article will consider the basics of PLLs, examine the current state of the art in PLL design with high voltage VCOs, discuss the pros and cons of typical architectures, and introduce some alternatives to high-voltage VCOs.

PLL Basics

A phase-locked loop (Figure 1) is a feedback system in which a phase comparator or detector drives a VCO in a feedback loop to make the oscillator frequency (or phase) accurately track that of an applied reference frequency. A filter circuit is typically required to integrate and smooth the positive or negative error signal—and promote loop stability. A frequency divider is often included in the feedback path to establish the output frequency (within the range of the VCO) as a *multiple* of the reference frequency. The divider can be implemented so that the frequency multiple, N, will be either an integer or a fractional number, characterizing the PLL as an *integer-N PLL* or a *fractional-N PLL*.

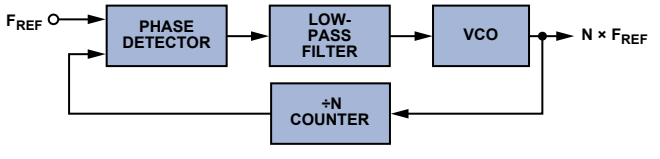


Figure 1. A basic phase-locked loop.

Because a PLL is a negative-feedback control loop, the frequency error signal will be forced to zero at equilibrium to produce an accurate and stable frequency of $N \times F_{REF}$ at the output of the VCO.

PLLs are implemented in various ways, using all-digital, all-analog, or combined circuitry, depending on the required frequency range, noise and spurious performance, and physical size. At present, the architecture of choice for high-frequency, or RF, PLLs combines all-digital blocks, such as feedback dividers and phase detectors, with high-precision analog circuits, such as charge pumps and VCOs. The main features of a mixed-signal PLL are:

1. *Reference frequency*: The stable, accurate frequency reference to which the RF output will be phase locked. It is typically derived from a crystal or *temperature-controlled crystal oscillator* (TCXO).
2. *Phase frequency detector* (PFD): Derives the phase-error signal from the reference and feedback signals.
3. *Charge pump*: Converts the error signal into a train of positive or negative current pulses in proportion to the phase error.
4. *Loop filter*: Integrates the current pulses from the charge pump, providing a clean voltage to the VCO tuning port.
5. *VCO*: Outputs a frequency that depends on the voltage presented to its tuning port (V_{tune}). The VCO has gain, K_V, expressed in MHz/V. The basic VCO expression relating output frequency to the input control voltage is $f_o = f_c + K_v (V_{tune})$, where f_c is the VCO offset frequency.
6. *N divider*: Divides the output frequency down to equal the PFD or reference frequency. It can straightforwardly divide by an integer—or, increasingly, be implemented as a *fractional* divider. The fractional divider can be simply implemented by toggling the divide values in an integer divider to get a fractional average (for example, to get an average of 4.25, count to 4 three times and count to 5 once. Seventeen pulses have been counted and 4 pulses have been created; so the frequency ratio is 17/4 = 4.25). In practice, better results can be achieved by borrowing from techniques used in high-resolution noise-shaped converters. Thus, the fractional engine is usually implemented using a Σ-Δ architecture, which has the advantage of reducing spurious frequencies.

As an example of the highly integrated circuitry used in available devices, Figure 2 shows a block diagram of a fractional-N PLL IC, the ADF4350 wideband synthesizer with integrated VCO; it has an output frequency range of 137.5 MHz to 4400 MHz. (A brief summary of its capabilities can be found in the Wide-Bandwidth PLLs with Integrated VCOs section.)

The key performance-limiting characteristics of PLLs are *phase noise*, *spurious frequencies*, and *lock time*.

Phase noise: Equivalent to jitter in the time domain, phase noise is oscillator or PLL noise as evaluated in the frequency domain. It is the rms sum of the noise contributed by the various components in the PLL. The charge-pump-based PLL will suppress VCO noise inside the loop filter bandwidth. Outside of the loop bandwidth, the VCO noise dominates.

Spurs: Spurious frequency components are caused by the charge pump's periodic updating of the VCO tuning voltage. They will appear at a frequency offset from the carrier by the PFD frequency. In a fractional-N PLL, spurs will also occur due to the action of the fractional divider.

Lock Time: The time taken for the PLL's phase or frequency to return to lock range when changing from one frequency to another or responding to a transient offset. It can be specified in terms of frequency- or phase settling. Its degree of importance as a specification depends on the application.

Why Do VCOs Still Use High Voltages?

High-performance VCOs are among the last electronic components to resist the tide of silicon integration. Only in the past few years have VCOs for cellular handsets been fully integrated into their radio chipsets. However, cellular base stations, microwave point-to-point systems, military and aerospace, and other higher-performance applications are still beyond the capability of silicon-based VCOs and are still implemented using a discrete approach. Here's why:

Most commercially available discrete VCOs use a variable-capacitance *varactor* diode as the tunable element in an LC-based tank circuit. Varying the diode's voltage changes its capacitance and, thus, the resonant frequency of the tank circuit.

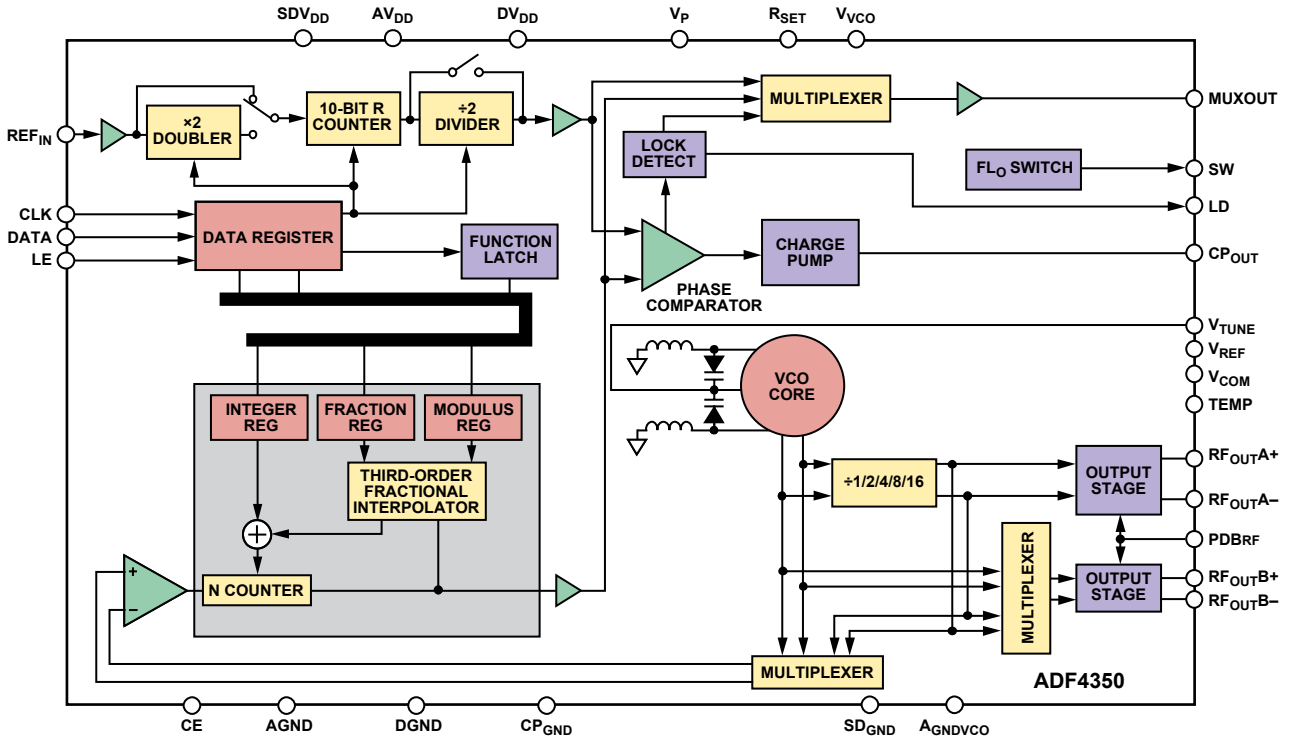


Figure 2. ADF4350 PLL synthesizer block diagram.

Any voltage noise on the varactor will be amplified by the VCO gain, K_V, (expressed in MHz/V) and will translate into phase noise. To keep VCO phase noise to a minimum, K_V must be kept as low as possible, but achieving a reasonably wide tuning range requires a large K_V. Thus, for applications that require low phase noise and a wide tuning range, VCO manufacturers typically design oscillators with low gain and a large input voltage range to satisfy these conflicting requirements.

Typical voltage tuning ranges for narrow-band VCOs are 0.5 V to 4.5 V, while wideband VCOs typically tune over 1 V to 14 V, and in some cases have ranges as wide as 1 V to 28 V.

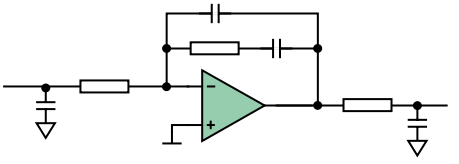
Coaxial resonator oscillators (CROs) are another special type of VCO that uses a very low gain and wide input tuning voltage to achieve ultralow phase-noise performance. They are typically used in narrow-band *private mobile radio* and *land mobile radio* applications.

Interfacing to a High-Voltage VCO

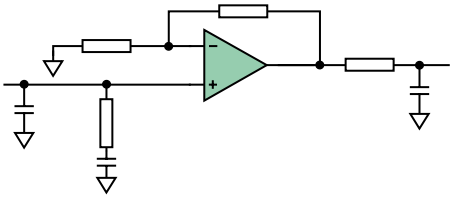
Most commercial PLL synthesizer ICs have charge pump outputs that are limited to a maximum of about 5.5 V, insufficient to directly drive a VCO that requires higher tuning voltages if the loop filter uses passive components alone. An active loop filter topology using op amp circuitry must be employed to reach the higher tuning voltages.

The simplest approach to achieve this would be to add a gain stage after the passive loop filter. Although simple to design, this approach has some pitfalls: an inverting op amp configuration presents a low input impedance that will load the passive loop filter, altering the loop dynamics; a noninverting configuration has input impedance high enough not to load the filter but will amplify any op amp noise by the active filter gain without the benefit of filtering by the preceding passive loop filter. A much better topology is to integrate the gain stage and filter into a single active filter block. Prefiltering is advisable so as not to overdrive the amplifier with the very short current pulses from the charge pump—which could rate-limit the input voltage.

Figure 3 shows two examples of recommended active filter topologies with prefiltering using inverting and noninverting gains. Please note that these amplifier circuits are true time-integrators, which force the PLL's loop to maintain zero error at their inputs. Outside of the loop, the topologies shown could drift to the supply rails.



a. Inverting topology.



b. Noninverting topology.

Figure 3. Active filter using prefiltering.

The inverting topology has the advantage of biasing the charge pump output at a fixed voltage, typically one-half the charge-pump voltage ($V_P/2$)—optimal for spur performance. Care needs to be taken to provide a clean bias voltage, ideally from a dedicated low-noise linear regulator like the ADP150, with adequate decoupling as close as possible to the op amp input pin. The resistance values used in the divider network should be minimized to reduce their noise contribution. When using the inverting topology, it is important to make sure that the PLL IC allows the PFD polarity to be inverted, if necessary, canceling out the op amp's inversion and driving the VCO with the correct polarity. The ADF4xxx family has this property.

The noninverting loop filter configuration does not require a dedicated bias, so it can be a more compact solution. The charge pump voltage, instead of being biased at a fixed level, will now vary across its operating range. For this reason, it is much more critical to use an op amp with rail-to-rail inputs when using this filter type. (Input voltage range requirements are described in the next section.)

Choice of Op Amp

The choice of op amp is the key to maximizing the potential of an active filter. Besides bandwidth, the main performance specifications to consider are:

- Noise voltage density—expressed in nV/√Hz
- Current noise—expressed in pA/√Hz
- Input bias current
- Common-mode voltage range

The output of the filter directly affects the generated frequency and phase; therefore, the op amp's noise-voltage density gives an indication of how much phase noise will be added by the active filter. Amplifier noise is added both within the PLL loop bandwidth and out of band—and is most pronounced at the loop filter's corner frequency, especially for amplifiers with high noise voltage density. Thus, it is important to keep the amplifier's noise low to fulfill the mission of the amplifier and high-voltage VCO: to provide lower phase noise. A good design target would be <10 nV/√Hz. *Current noise* is usually quite small compared to the error current pulses, so its effects tend to be much smaller than those of voltage noise.

Op amps that have significant input bias currents in relation to the PFD output current can result in large spurs on the PLL output spectrum. To keep the VCO tuning voltage constant and the PLL in lock, the charge pump must replace the bias current drawn by the op amp inputs on each PFD cycle. This modulates the V_{TUNE} voltage at the PFD frequency and causes spurs around the carrier at an offset equal to the PFD frequency. The higher the input bias current, the greater the modulation of the V_{TUNE} voltage and the higher the spur amplitudes.

Common-mode voltage range, or *input voltage range* (IVR), another important op amp specification, is often overlooked, causing serious problems in the end design. IVR determines the clearance needed at the input terminals between the maximum/minimum signals and the positive/negative power rails.

Early op amps that ran on ±15 V had typical IVRs of ±12 V. Slow lateral PNP input stages, added later, allowed the IVR to include the negative rail, thus providing single-supply capability. Although any op amp will run on ground and a positive supply, it is necessary to observe the distance from the rails.

For example, the popular OP27 has an IVR of ±12.3 V with a ±15-V supply. This means that the input voltages need to be at least ±2.7 V from the positive and negative rails. This limitation at the lower end of the range would make it unattractive for use with wide input swings in single-supply operation. A dual-supply design option, if available, allows a much greater choice of op amps (and simplifies the input bias question). If single-supply design is necessary, use op amps that allow the input voltage to swing from rail to rail (but many of them may have higher noise-voltage specs). Thus, for best results, one needs an op amp with low noise voltage density for low phase noise, low input bias currents for low spurs, and rail-to-rail inputs for single-supply operation. Table 1 lists some Analog Devices op amps and their specifications in relation to the above design criteria.

Table 1. Recommended Op Amps to Use in PLL Active Loop Filters

Op Amp	Voltage Noise, f = 1 kHz (nV/√Hz)	Current Noise, f = 1 kHz (pA/√Hz)	Input Bias Current (Typ)	Input Voltage Range, Clearance from Lower Rail (V)	V_{SUPPLY} Max, Single-Supply (V)
AD820	16	0.8	2 pA	−0.2	36
OP184	3.9	0.4	60 nA	0	36
AD8661	12	0.1	0.3 pA	−0.1	16
OP27	3	0.4	10 nA	+2.7	36
AD8099	2	8	100 nA	+1.3	12

The choice of op amp depends on the application. If the PFD spurs are far outside the loop bandwidth (for example, in fractional-N synthesizers), then a bipolar-junction-transistor-input (BJT) op amp—like the OP184 or OP27—will be suitable. The PFD spurs caused by the high input bias current of the BJT will be well attenuated by the loop filter, and the PLL can take full advantage of the BJT op amp's low noise voltage density.

If the application requires the PFD-to-loop-bandwidth ratio to be small (for example, in an integer-N synthesizer), a compromise should be reached between noise and spur levels; the AD820 and AD8661 could be good choices here.

It is worth noting that although active filters tend to contribute noise to the PLL, their ability to act as buffers provides a performance advantage over passive filters in some application niches. For example, if the VCO has high leakage current on its tuning port leading to high PFD spurs, an op amp can be used to reduce the spur levels. The op amp's low impedance output can easily supply the tuning port leakage current.

Design Example

Consider an example where the LO has the following specifications:

- Octave tuning range from 1000 MHz to 2000 MHz
- Phase noise requirement of –142 dBc/Hz at 1 MHz offset
- Spurs < –70 dBc
- 250-kHz channel spacing
- Lock time < 2 ms
- Single supply of 15 V or 30 V available

To cover the 1-GHz band, while meeting the phase-noise target, it is necessary to use a high-voltage VCO and an active loop filter. The phase-noise and spur specifications, and single-supply restriction, will drive the choice of op amp. To meet the spur specifications the op amp input bias current must be low, while best phase noise will be achieved with an op amp with low voltage noise. A compromise between the two can be reached by choosing a JFET-input op amp, such as the AD8661, which has an input bias current of 0.3 pA and voltage noise of 12 nV/√Hz. This device can also handle the single-supply requirement. The RFMD UMS-2000-A16 VCO was selected to cover the octave range.

The best place to start is with a simulation involving the active-filter topologies supported in the ADIsimPLL™ tool. Two of the recommended filter types are shown in Figure 3, but ADIsimPLL supports other configurations as well.

For the PLL, the ADF4150, which can be operated in either integer or fractional mode, was chosen; it also has output divider options of 2/4/8/16/32—which allow continuous coverage from 2 GHz down to 31.25 MHz. The ADF4150 is similar to the ADF4350 shown in Figure 2, but it allows the choice of an external VCO for applications that need to meet more stringent phase-noise requirements. In the simulation, the PLL loop filter was set at 20 kHz to attempt to minimize the op amp noise contribution, while keeping the PLL lock time less than 2 ms.

Figure 4 shows a plot of noise (dBc) as a function of frequency offset in simulated and measured systems, using an ADF4150 PLL, a UMS VCO, and an AD8661-based filter. A –90-dBc peak at about 20 kHz, due to the noise added by the active loop filter, can be seen in both noise profiles, but the –142-dBc/Hz target at 1 MHz offset is still being met. To reduce the in-band noise, a lower-noise op amp, such as the OP184 or OP27, could be used at the expense of higher spurs; or the PLL loop bandwidth could be decreased to below 20 kHz.

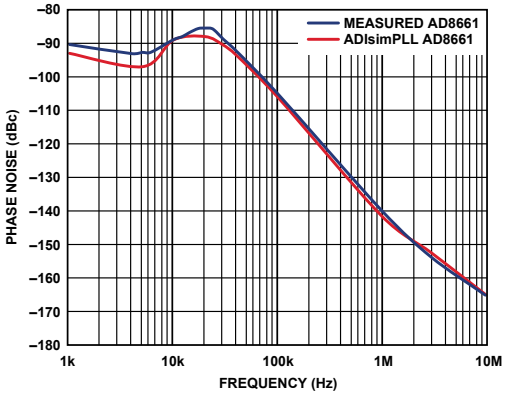


Figure 4. ADIsimPLL simulation vs. measured performance using AD8661 as an op amp in PLL active filter.

Figure 5 shows the approximately 6-dB improvement when the OP27 is used. In this case, spurs do not increase significantly, as the loop bandwidth is relatively narrow. Lowering the bandwidth further will improve phase noise for offsets below 100 kHz at the expense of increased PLL lock-time. All of these trade-offs can be tested with ADIsimPLL simulations prior to going into the lab.

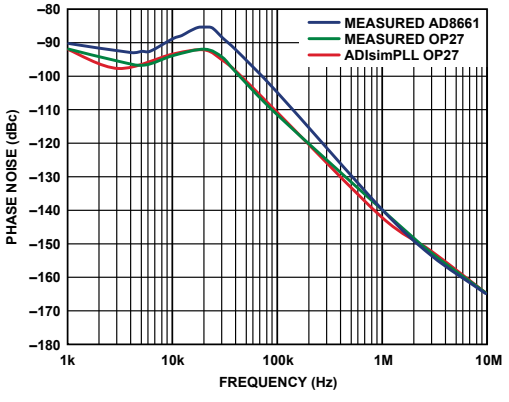


Figure 5. PLL measured performance using AD8661 vs. OP27 in active loop filter.

Breaking News: High Voltage PLLs

Up to this point the discussion has been driven by the need to use active filters to interface a low-voltage PLL device to a high-voltage VCO. *High-voltage PLLs are becoming available, however, greatly reducing the necessity for an active filter.* An example is the ADF4113HV PLL, which integrates a high-voltage charge pump and has –212-dBc/Hz normalized phase-noise floor. In this case, the PLL charge pump output can be as high as 15 V, allowing a simpler passive filter before the VCO.

This family of high-voltage PLLs will soon be further augmented by devices that increase the maximum voltage to 30 V and fractional-N PLLs that have high-voltage charge pumps. Consult the PLL website for updates and new-product information.

Wide-Bandwidth PLLs with Integrated VCOs

Another alternative to using an active filter with high-voltage VCO is to use a *fully integrated high-performance PLL* like the ADF4350, shown in Figure 2. In this case, the VCO is integrated on chip. The inherent trade-off of wide tuning range and low phase noise discussed above is avoided by using a multiband VCO approach. In the ADF4350, three separate VCOs are integrated on chip, each of which has 16 overlapping subbands, giving a total of 48 subbands. Each time the frequency is updated, an automatic calibration is initiated to select the appropriate VCO subband.

This shows the real benefit of moving VCO designs from a discrete to a silicon-based solution: significant levels of integration can be achieved in minimal area, allowing greater design flexibility. For example, the ADF4350 also integrates a programmable output-divider stage that allows frequency coverage from 137.5 MHz all the way up to 4.4 GHz—a very attractive feature for radio designers who want to reuse the same design across multiple frequencies and standards.

The ADF4350 comes in a 5-mm square LFCSP package—as compared with the standard 12.7-mm square VCO package. Performance levels approach those of discrete designs, with phase noise of –114 dBc/Hz at 100-kHz offset and –134 dBc/Hz at 1-MHz offset (see Figure 2).

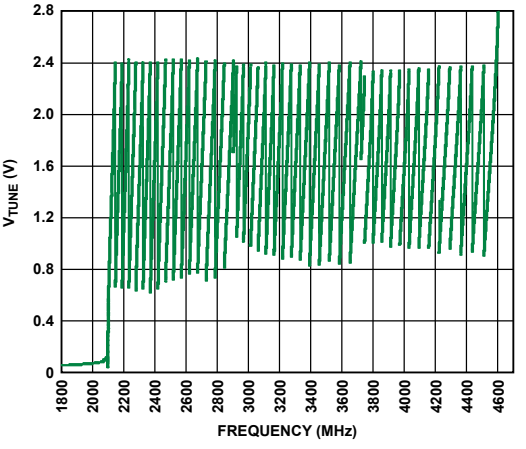


Figure 6. Plot showing the 48 distinct bands in the ADF4350 VCO voltage vs. frequency relationship.

For more on one of the broadest PLL portfolios in the industry, including integer-N, fractional-N, integrated VCO, and high-voltage PLL ICs—pushing performance boundaries and easing design challenges for PLL- and radio designers worldwide—consult the PLL Synthesizers/VCOs website.

References

1. Applied Radio Labs Forums http://www.radiolab.com.au/Forums/default.asp.
2. Best, Roland E. *Phase-Locked Loops. Design, Simulation, and Applications*. McGraw Hill.
3. Curtin, Mike and Paul O'Brien. 1999. "Phase-Locked Loops for High-Frequency Receivers and Transmitters—Part 2." *Analog Dialogue*, Volume 33.
4. Information on all ADI components can be found at www.analog.com.

Author

Austin Harney [austin.harney@analog.com] graduated in 1999 with a BEng from University College, Dublin, Ireland, and joined Analog Devices following graduation. He is currently an applications engineer for the ISM-band wireless product line, based in Limerick. In his spare time, Austin enjoys football, music, and spending time with his daughters.

Adjustable-Gain Difference Amplifier Circuit Measures Hundreds of Volts, Rejects Large Common-Mode Signals

By Moshe Gerstenhaber and Michael O'Sullivan

A high common-mode difference amplifier, in a feedback loop with an inverting op amp, is a useful aid for performing high-voltage differential measurements up to 500 V.

Two common solutions to monitor power-line voltages or other large signals—using low-voltage electronics—involve a high-resistance voltage divider to attenuate the input, followed by an op amp buffer (Figure 1a); or an inverting op amp with high input resistance (Figure 1b). These methods have several shortcomings: they are useful mainly for single-ended measurements, making them prone to ground noise; they cannot reject common-mode voltages; and the resistors dissipate different amounts of power, leading to gain errors.

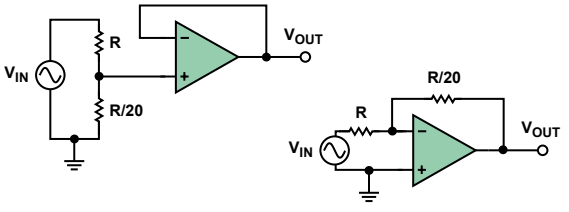


Figure 1. Single-ended measurements using op amps.

A better way involves the use of a difference amplifier. The AD629[1] unity-gain difference amp, shown in Figure 2, can reject extremely high common-mode signals (up to 270 V with 15-V supplies). To achieve this high common-mode voltage range, a precision internal resistor divider attenuates the noninverting signal by a factor of 20. Other internal resistors restore the gain to provide a differential gain of unity. The complete transfer function, with reference inputs grounded, is

$$V_{OUT} = V_{+IN} - V_{-IN} \quad (1)$$

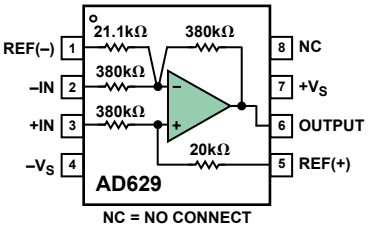


Figure 2. Functional block diagram of the AD629 difference amplifier.

Laser wafer trimming provides resistor matching for common-mode rejection (CMR) of up to 86 dB minimum.

A highly useful application, shown in Figure 3, uses the AD629 and an op amp, such as the AD708,[2] to provide adjustable gain. A differential input signal is applied to difference amplifier A1, which rejects any common-mode voltage on the input. The differential input signal appears at the output with a gain of 1. The output voltage is fed into the input of operational amplifier A2, which is configured as a voltage inverter with a gain of –R2/R1. The inverter's output voltage is applied to the difference amplifier's reference pin (REF+). The voltage applied to this pin is multiplied by a gain of 19, and is added to the output of A1. Solving for the output of this negative feedback loop,

$$V_{OUT} = \frac{V_{+IN} - V_{-IN}}{1 + 19 \times \frac{R2}{R1}} \quad (2)$$

Capacitor C1 (100 nF), with resistor R2 (20 kΩ), provides loop stability and sets the bandwidth at approximately 1 kHz.

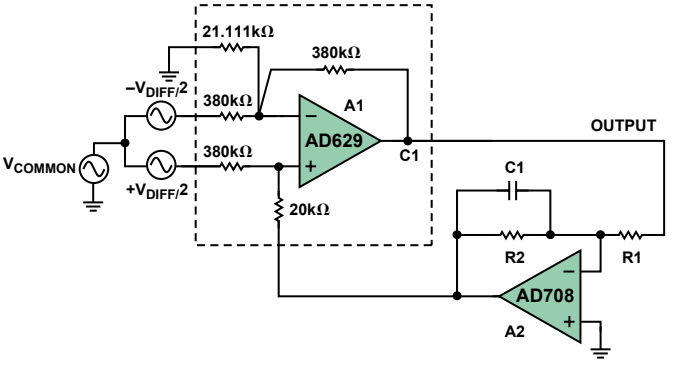


Figure 3. Difference amplifier in adjustable-gain configuration.

The maximum differential signal that the circuit can handle is limited by the output range of amplifiers A1 and A2. When R2/R1 is less than or equal to 1, amplifier A1's output will saturate first. With ±15-V supplies, the circuit can handle differential voltages up to 520 V p-p. Systems with ±10-V or ±5-V supply voltages can handle differential voltages up to 320 V p-p and 120 V p-p, respectively. With ratio R2/R1 greater than 1 and an amplifier with rail-to-rail output for A2, these ranges can be extended closer to 600 V p-p, 400 V p-p, and 200 V p-p.

Negative feedback around the loop helps to reduce the voltage seen by the inputs of op amp A1. This means that the circuit has the input range to reject large common-mode voltages, even in the presence of large differential voltages.

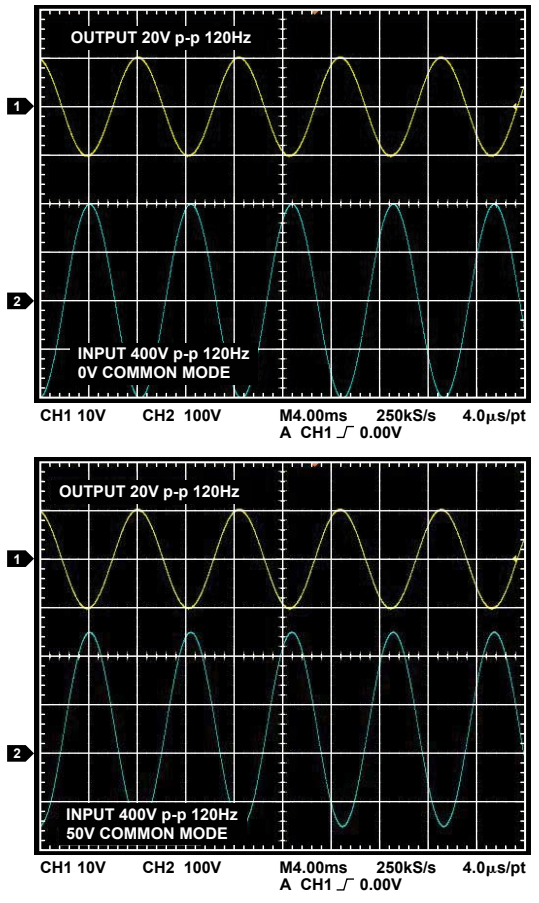


Figure 4. 400-V p-p differential signal measured with 0-V and 50-V common-mode signal.

Figure 4 shows two plots: in the first plot, a differential signal of 400 V p-p is measured using ±15 V supplies; in the second plot, a 400-V p-p differential signal is measured in the presence of a 50-V common-mode voltage. As can be seen, this circuit allows very large differential inputs; rejects common-mode voltages; and allows the differential gain to be set by the ratio of resistors R2 and R1, enabling the user to select the appropriate level of attenuation. The resistors inside the difference amplifier are precision laser-trimmed and manufactured with low-drift thin film material, so the system does not suffer from resistor self-heating errors.

References

[1] www.analog.com/en/amplifiers-and-comparators/current-sense-amplifiers/ad629/products/product.html.
[2] www.analog.com/en/amplifiers-and-comparators/operational-amplifiers-op-amps/ad708/products/product.html.

Authors

Moshe Gerstenhaber [moshe.gerstenhaber@analog.com] is a Division Fellow at Analog Devices. He began his career at ADI in 1978 and has held various senior positions over the years in manufacturing, product engineering, and product design. Moshe is currently the design manager of the Integrated Amplifier Products Group. He has made significant contributions in the field of amplifier design, especially very-high-precision specialty amplifiers, such as instrumentation and difference amplifiers.

Michael O'Sullivan [michael-a.osullivan@analog.com] has worked at Analog Devices since 2004. Currently the product and test engineering manager of the Integrated Amplifier Products Group, he supports product characterization and release of very-high-precision specialty amplifiers, such as instrumentation and difference amplifiers. Mike worked as a product engineer in the semiconductor field for over 14 years.

Automobile Tail-Lamp and Brake-Lamp Controller

By Chau Tran

Light emitting diodes (LEDs), long used in consumer electronic products, are recently finding uses in automotive lighting, where they now provide signaling functions, daytime running lights, and interior lighting in production vehicles. As this lighting technology hits the road, manufacturers continue to investigate new ways to apply it, taking advantage of the styling possibilities afforded by LED headlights and taillights.

Red LEDs are now widespread for rear lighting. Cost remains an issue, but factors such as safety, environmental friendliness, and styling flexibility weigh heavily in favor of LEDs. One of the most popular applications is center brake lights. This design idea shows a way to use the same LED array for both taillights and brake lights.

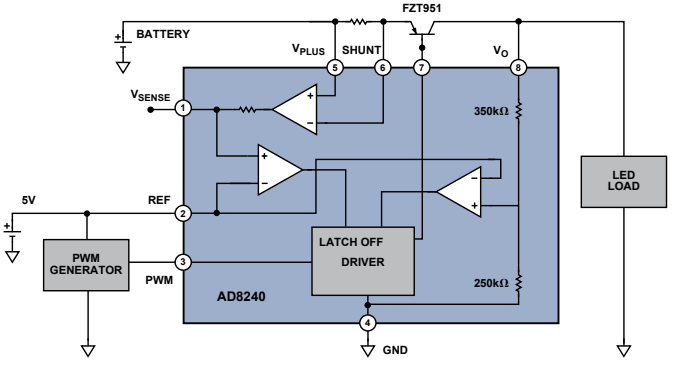


Figure 1. Running braking lamps controller.

The brightness of the LED is controlled by a simple switch, allowing dim lighting while running and bright lighting while braking. The block diagram, shown in Figure 1, includes an AD8240 LED driver/monitor, PNP pass transistor, and PWM generator. The AD8240 supplies a constant voltage to drive LED lamps. It also provides cost-effective LED lamp monitoring and short-circuit protection. The output is regulated at 12 V when the battery is between 12.5 V and 27 V.

Figure 2 shows the PWM generator, which consists of two 555 timers. The PWM signal controls the LED brightness. V_O is turned on when the PWM input is high and turned off when the input is low. The AD8240 is designed to work with a frequency up to 500 Hz and a typical duty cycle of 5% to 95%.

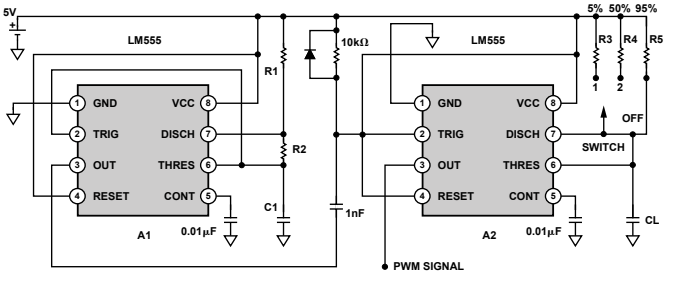


Figure 2. PWM signal generator.

With its low-power operation, the AD8240 provides a low-cost solution in a small package. An internal current-sense amplifier measures the voltage across an external current shunt, detecting an open LED when the measured current drops below a preset threshold. Output current limiting is provided by latching off the output voltage when the current reaches a level set by the value of the external current shunt. When the sense amplifier output exceeds 5 V, an internal comparator causes the driver to latch off the output voltage. The latch is reset during the next PWM cycle. An overcurrent condition can also be detected by measuring the sense amplifier output.

Costs are further reduced by eliminating the inductor required for a switching design; and a switching driver is not required because the LED lamps operate at much lower power than incandescent lamps.

The LEDs are turned on and off depending on the digital voltage on a CMOS-compatible PWM pin (AD8240 Pin 3). This voltage can be continuous for a simple on/off control, or PWM for dimming control. The PWM frequency should be less than 500 Hz, with a duty cycle from 5% to 100%. Typical values are 5% for running and 95% for braking. In Figure 2, the PWM frequency is determined by R1, R2, and C1 of timer A1. The pulse period is:

$$T = 0.693\ (R1 + 2 \times R2)\ C1$$

With R1 = 49.9 kΩ, R2 = 10 kΩ, and C1 = 0.1 µF, the period is 4.84 ms, or about 206 Hz.

Timer A2 converts the signal into a pulse-width-modulated signal with a duty cycle determined by R3, R4, R5, and C2. The pulse width is determined by:

$$Pulse\ width = 1.1 \times R \times C2$$

where R is equal to R5, the parallel resistance of R3 and R5, or the parallel resistance of R4 and R5, depending on the switch position. With R3 = 2.37 kΩ, R4 = 45.7 kΩ, R5 = 42.4 kΩ, and C2 = 0.1 µF, the duty cycle is 5% when the switch is in Position 1, 50% when the switch is in Position 2, and 95% when the switch is in the OFF position.

Note that the brightness of the LEDs increases as the duty cycle increases. When the brake is applied, the duty cycle is 95%, and the LED array is at maximum brightness. During normal operation, the duty cycle is at 5%, and the LED array is dimmed. Using a single LED array for both operations reduces cost.

If a short circuit or an overload condition occurs, the voltage at V_{SENSE} (Pin 1) falls to zero, and the output shuts down. This resets during the next PWM cycle. If the condition persists, the AD8240 attempts to drive the output to 12 V, shutting down and restarting after each PWM cycle.

This circuit presents a way to use a constant voltage, driving and monitoring the LEDs with only two wires (power and ground). In many cases, this can be reduced to one wire when the chassis or shared ground return is used. Currently, these lamps are controlled and driven by the body control ECU (electronic control unit). With this constant voltage architecture, the control and drive function for the LEDs can remain in the ECU with minimal design modifications.

Author

Chau Tran [chau.tran@analog.com] joined Analog Devices in 1984, where he works in the Instrumentation Amplifier Products (IAP) Group in Wilmington, MA. In 1990, he graduated with an MSEE degree from Tufts University. Chau holds more than 10 patents and has authored more than 10 technical articles.

Analog Devices, Inc.
Worldwide Headquarters
Analog Devices, Inc.
Three Technology Way
P.O. Box 9106
Norwood, MA 02062-9106
U.S.A.
Tel: 781.329.4700
(800.262.5643,
U.S.A. only)
Fax: 781.461.3113

Analog Devices, Inc.
Europe Headquarters
Analog Devices, Inc.
Wilhelm-Wagenfeld-Str. 6
80807 Munich
Germany
Tel: 49.89.76903.0
Fax: 49.89.76903.157

Analog Devices, Inc.
Japan Headquarters
Analog Devices, KK
New Pier Takeshiba
South Tower Building
1-16-1 Kaigan, Minato-ku,
Tokyo, 105-6891
Japan
Tel: 813.5402.8200
Fax: 813.5402.1064

Analog Devices, Inc.
Southeast Asia
Headquarters
Analog Devices
22/F One Corporate Avenue
222 Hu Bin Road
Shanghai, 200021
China
Tel: 86.21.2320.8000
Fax: 86.21.2320.8222

M02000434-0-2/11

www.analog.com/analogdialogue

ANALOG DEVICES