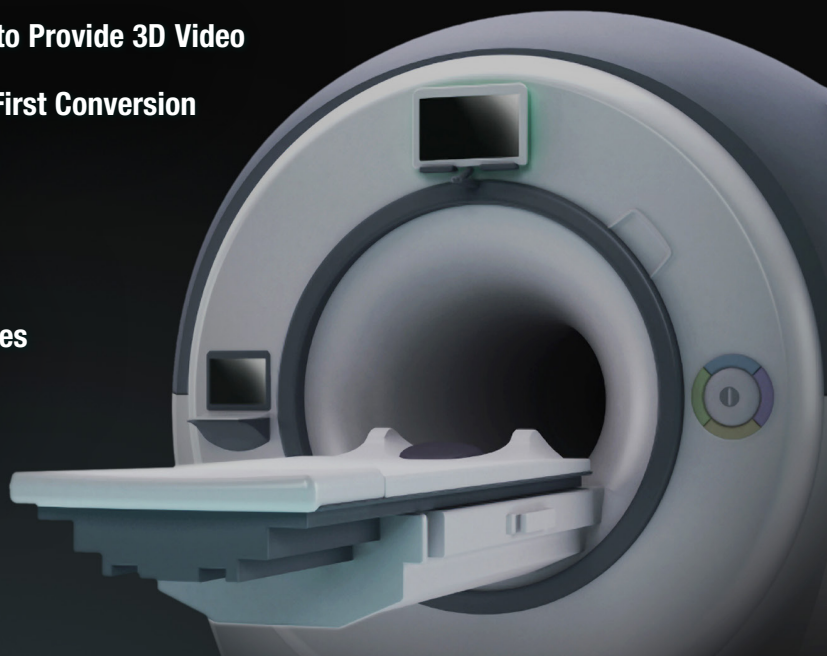


# Analog Dialogue

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### FPGA-Based System Combines Two Video Streams to Provide 3D Video

Video systems are increasingly prevalent in automotive, robotics, and industrial domains. This growth into nonconsumer applications resulted primarily from the introduction of an HDMI® standard and faster, more efficient DSPs and FPGAs. This article outlines the requirements for achieving stereoscopic vision (3D video) using analog or HDMI video cameras. (Page 3)

### Successive-Approximation ADCs: Ensuring a Valid First Conversion

Successive-approximation analog-to-digital converters (ADCs) with up to 18-bit resolution and 10-MSPS sample rates meet the demands of many data-acquisition applications, including portable, industrial, medical, and communications. This article shows how to initialize a successive-approximation ADC to get valid first conversions after power-up and initialization. (Page 8)

### Highest Power Density, Multirail Power Solution For Space-Constrained Applications

As the size of communications, medical, and industrial equipment continues to decrease, power management becomes an increasingly important consideration. This article looks at applications for highly integrated power management solutions, the advantages these new devices bring for powering FPGAs and processors, and a design tool that helps designers to quickly implement a new design. (Page 11)

### MEMS Microphones, the Future for Hearing Aids

Driven by aging populations and increased hearing loss, the market for hearing aids continues to grow, but their conspicuous size and short battery life cause people to look for smaller, more efficient, higher quality devices. At the start of the signal chain, microphones sense voices and other ambient sounds, so improved audio capture can lead to higher performance and lower power consumption. (Page 19)

### High-Performance Data-Acquisition System Enhances Images for Digital X-Ray and MRI

Digital X-ray, magnetic resonance imaging, and other medical devices require high-performance, low-power data-acquisition systems to meet the demands of doctors, patients, and manufacturers in a competitive marketplace. This article showcases a signal chain that is ideal for multichannel applications, as well as those that require low noise, high dynamic range, and wide bandwidth. (Page 22)

### Some Tips on Making a FETching Discrete Amplifier

Low-noise amplifiers for photodiode, piezoelectric, and other instrumentation applications typically call for extremely high input impedance, low 1/f noise, or sub-picoamp bias currents that may not be met with available integrated products. This article discusses the challenges of designing a low-noise amplifier using discrete components, with emphasis on input-referred noise and offset voltage trimming. (Page 27)

Scott Wayne [scott.wayne@analog.com]

## PRODUCT INTRODUCTIONS: VOLUME 47, NUMBER 4

Data sheets for all ADI products can be found by entering the part number in the search box at [www.analog.com](http://www.analog.com).

### October

**Amplifier**, operational, high-voltage, precision.....ADA4700-1  
**DACs**, 12-channel/16-channel,  
24-bit, 192-kHz .....ADAU1962A/ADAU1966A  
**System**, measurement and control, 12-bit .....AD7294-2

### November

**Amplifier**, current-sense, bidirectional, zero-drift .....AD8418  
**Decoders**, video 10-bit, SDTV,  
4× oversampled.....ADV7280/ADV7281/ADV7282  
**Switch**, high-side load, with quad signal switch .....ADP1190A  
**Switches**, SPST/SPDT, high-voltage,  
latch-up proof.....ADG5401/ADG5419  
**Transceiver**, RF agile.....AD9361

### December

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**ADC**, pipelined, 8-channel, 14-bit, 65-MSPS.....AD9681  
**ADC**, pipelined, 16-channel, 14-bit, 65-MSPS.....AD9249  
**ADC**,  $\Sigma$ - $\Delta$ , 2-channel/3-channel, isolated.....ADE7912/ADE7913  
**ADC**,  $\Sigma$ - $\Delta$ , 4-channel, automotive audio .....ADAU1979  
**ADC**,  $\Sigma$ - $\Delta$ , 8-channel/16-channel, 24-bit, 31.25-kSPS.....AD7173-8  
**Amplifier**, operational, quad, high-precision.....ADA4077-4  
**Buffer**, FET-input, quad, precision.....AD8244  
**DAC**, 16-bit, 1600-MSPS, TxDAC+®.....AD9139  
**Detector**, RF, 30-MHz to 4.5-GHz, 45-dB DR.....ADL5506  
**Detector**, rms power, 200-MHz to 6-GHz, 35-dB DR.....ADL5903  
**Driver**, half-bridge, isolated, 4-A.....ADuM7223  
**Driver**, LED 4-string, LCD backlight .....ADD5211  
**Energy Meter**, isolated, polyphase.....ADE7932/ADE7933/ADE7978  
**Isolators**, digital, 4-channel, 2.5-kV .....ADuM1144x  
**PMU**, 4-channel, two buck regulators, two LDOs .....ADP5134  
**Regulators**, ultralow-noise,  
high-PSRR, 800-mA .....ADM7150/ADM7151  
**Sensor**, angular rate, precision,  $\pm 1000^\circ/\text{sec}$  DR.....ADIS16137  
**Supervisor**, watchdog, manual reset .....ADM831x/ADM832x  
**Supervisor**, windowed watchdog, manual reset....ADM8323/ADM8324  
**Switches**, dual SPST, high-voltage,  
latch-up proof.....ADG5421/ADG5423

## Analog Dialogue

*Analog Dialogue*, [www.analog.com/analogdialogue](http://www.analog.com/analogdialogue), the technical magazine of Analog Devices, discusses products, applications, technology, and techniques for analog, digital, and mixed-signal processing. Published continuously for 47 years—starting in 1967—it is available in two versions. Monthly editions offer technical articles; timely information including recent application notes, circuit notes, new-product briefs, webinars, and published articles; and a universe of links to important and relevant information on the Analog Devices website, [www.analog.com](http://www.analog.com). Printable quarterly issues and ebook versions feature collections of monthly articles. For history buffs, the *Analog Dialogue* archive, [www.analog.com/library/analogdialogue/archives.html](http://www.analog.com/library/analogdialogue/archives.html), includes all regular editions, starting with Volume 1, Number 1 (1967), and three special anniversary issues. To subscribe, please go to [www.analog.com/library/analogdialogue/subscribe.html](http://www.analog.com/library/analogdialogue/subscribe.html). Your comments are always welcome: Facebook: [www.facebook.com/analogdialogue](http://www.facebook.com/analogdialogue); EngineerZone: [ez.analog.com/blogs/analogdialogue](http://ez.analog.com/blogs/analogdialogue); Email: [dialogue.editor@analog.com](mailto:dialogue.editor@analog.com) or Scott Wayne, Editor [[scott.wayne@analog.com](mailto:scott.wayne@analog.com)].

# FPGA-Based System Combines Two Video Streams to Provide 3D Video

By Witold Kaczurba

## Introduction

Video systems, already ubiquitous in consumer applications, are increasingly prevalent in automotive, robotics, and industrial domains. This growth into nonconsumer applications resulted primarily from the introduction of an HDMI standard and faster, more efficient DSPs and FPGAs.

This article outlines the requirements for achieving stereoscopic vision (3D video) using analog or HDMI video cameras. It describes an FPGA-based system that combines two video streams into a single 3D video stream for transmission through an HDMI 1.4 transmitter, and a DSP-based system that saves DMA bandwidth compared to that normally required for receiving data from two cameras. Furthermore, it shows one method for achieving a side-by-side format for use with 3D cameras or systems requiring 3D video.

## General Overview

Stereoscopic vision requires two video cameras separated by approximately 5.5 cm, the typical spacing between a person's eyes, as shown in Figure 1.



Figure 1. Two cameras on a stand aligned for stereoscopic vision.

The high-level block diagram shown in Figure 2 uses two synchronized video cameras that use the same video standard, two video decoders, and an FPGA. To ensure the exact same frame rate, the video cameras must be line-locked to a common timing reference. Without synchronization, it will not be possible to combine the outputs without using external memory to store complete video frames.

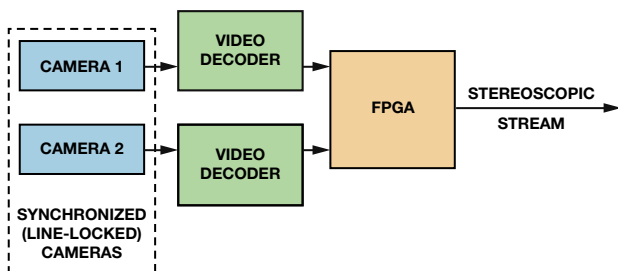


Figure 2. High-level block diagram.

Figure 3 shows two line-locked video streams being merged into a single stereoscopic image. Figure 4 shows how asynchronous video streams cannot be merged without saving the entire video frame in an external memory.

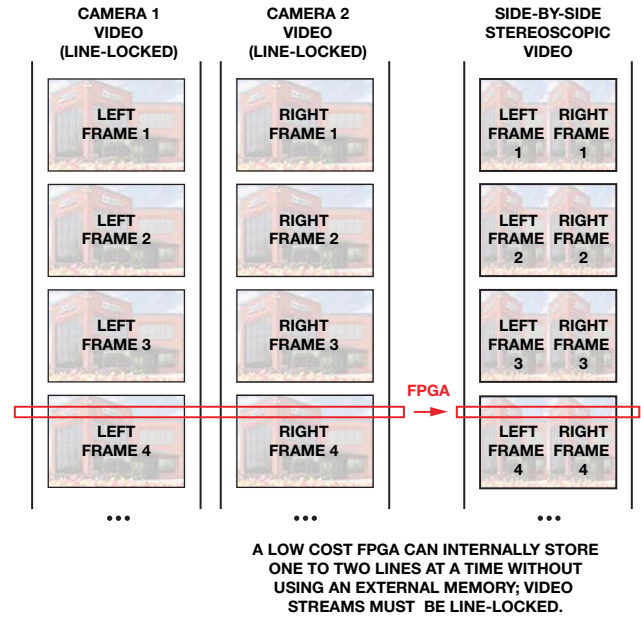


Figure 3. Merging two synchronized video streams.

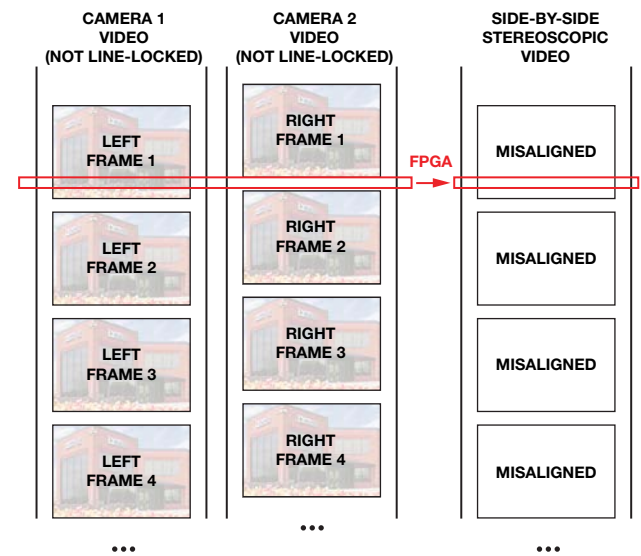


Figure 4. Asynchronous video streams cannot be merged without using an external memory.

The outputs of the two synchronized video cameras are then digitized by video decoders such as the [ADV7181D](#), [ADV7182](#), or [ADV7186](#) for analog video cameras; or by [HDMI receivers](#) such as the [ADV7610](#) or [ADV7611](#) with digital video cameras.

Video decoders and HDMI receivers use internal phase-locked loops (PLLs) to produce clock and pixel data at their output buses. This means that two separate clock domains will be generated for the two cameras when digitizing the analog video or receiving the HDMI stream. Moreover, the two video streams can be misaligned. These timing differences and misalignments must be compensated in a back-end device such as an FPGA, bringing the data to a common clock domain before combining the two video pictures into a single stereoscopic video frame. The synchronized video stream is then sent through an HDMI 1.4 3D-capable [HDMI transmitter](#) such as the [ADV7511](#) or [ADV7513](#)—or it can be presented to a DSP such as the [ADSP-BF609 Blackfin® processor](#)—for further processing.

### Clocking Architectures

Video decoders have two distinct clocking sources depending upon whether they are locked or unlocked. When the video PLL is locked to the incoming synchronization signal—horizontal sync for video decoders or the TMDS clock for HDMI—it generates a clock that is locked to the incoming video source. When video lock is lost, or the PLL is in forced free-run mode, the video PLL is not locked to the incoming synchronization signal and it generates a clock output that is locked to the crystal clock. In addition, the clock may not be output after reset as the LLC clock driver is set to a high impedance mode after reset.

Thus, if the system has two or more video paths from the video decoder or HDMI receiver, it will have two different clock domains with different frequencies and phases, even when the same crystal clock is provided to two video decoders or HDMI receivers, as each device generates its own clock based on its own PLL.

### Synchronous System with Locked Video Decoders

With typical stereoscopic video using two sources, each of the video decoders locks to the incoming video signal and generates its own clock based on incoming horizontal sync or TMDS clock. When two cameras are synchronized—or line-locked to the same timing reference—the frame lines will always be aligned. Because the two separate video decoders receive the same horizontal sync, the pixel clocks will have the same pixel clock frequency. This allows for bringing the two data paths into a common clock domain, as shown in Figure 5.

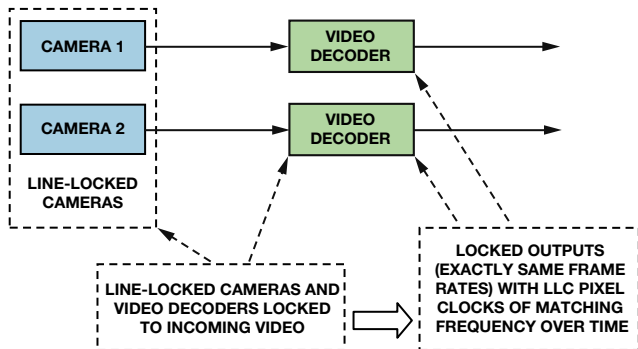


Figure 5. Two video cameras synchronized to a common reference. Both video decoders receive the same sync signal, so they are also locked.

### Asynchronous Video System

Unfortunately, one of the decoders may lose lock due to a poor quality video source signal, as shown in Figure 6; or the cameras may lose synchronization due to a broken video link, as shown in Figure 7. This will lead to different frequencies in the two data paths, which will then lead to asymmetry in the amount of data clocked into the back end.

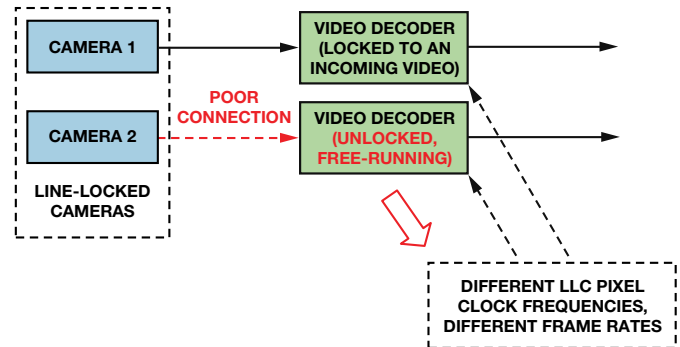


Figure 6. Line-locked cameras with unlocked video decoders.

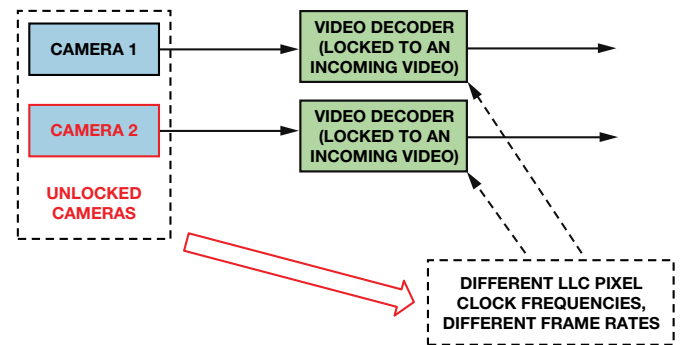


Figure 7. Unlocked cameras with locked video decoder.

Lost video lock can be detected by using an interrupt (SD\_UNLOCK for SD video decoders, CP\_UNLOCK for component video decoders, or TMDSPLL\_LCK registers in HDMI receivers) that kicks in after a delay. Video decoders integrate mechanisms for smoothing unstable horizontal synchronization, so detection of lost video lock can take up to a couple of lines. This delay can be reduced by controlling lost lock within the FPGA.

### Clock Tri-State Mode

When designing FPGA clocking resources, it is important to know that by default, many video decoders and HDMI products put the clock and data lines into tri-state mode after reset. Thus, the LLC pixel clock will not be suitable for synchronous resets.

### Data Misalignment in Two Video Streams

To simplify the system and reduce the memory needed to combine the two pictures, data reaching the FPGA should be synchronized such that the  $N^{\text{th}}$  pixel of the  $M^{\text{th}}$  line from the first camera is received with the  $N^{\text{th}}$  pixel of the  $M^{\text{th}}$  line from the second camera.

This might be difficult to achieve at the input of the FPGA because the two video paths may have different latencies: line-locked cameras can output misaligned lines, different connection lengths can contribute to misalignment, and video decoders can introduce variable startup latencies. Because of these latencies it is expected that a system with line-locked cameras will have a number of pixels of misalignment.

### Line-Locked Camera Misalignment

Even line-locked cameras can output misaligned video lines. Figure 8 shows the vertical sync signals from the CVBS output of two cameras. One camera, the sync master, provides a line-locking signal to a second camera, the sync slave. Misalignment of 380 ns is clearly visible. Figure 9 shows the data transmitted by the video decoders on the outputs of these cameras. An 11-pixel shift can be seen.

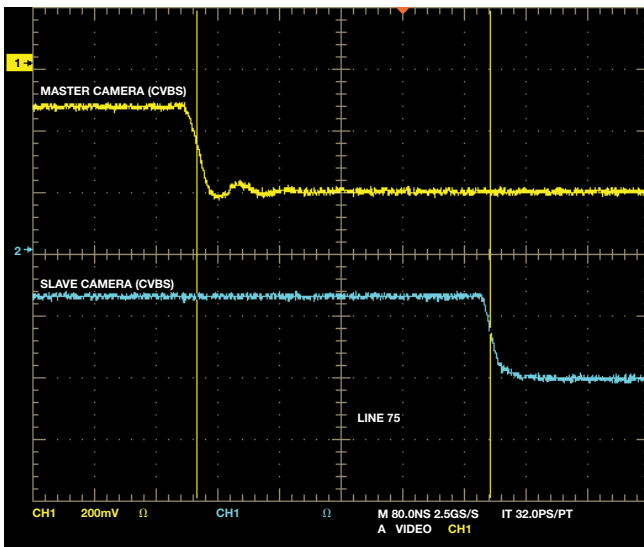


Figure 8. 380-ns video misalignment between line-locked video cameras.

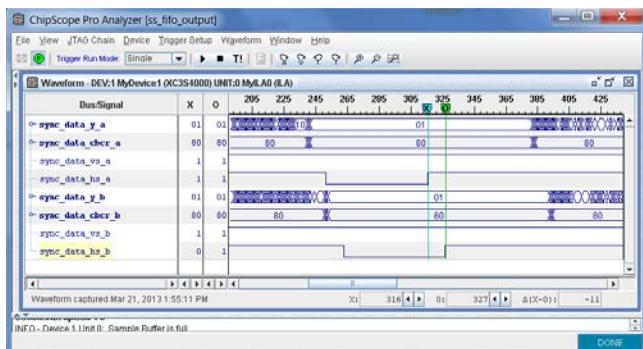


Figure 9. Uncompensated 11-pixel video misalignment in the digital domain.

### Different Connection Lengths

All electrical connections introduce a propagation delay, so make sure that both video paths have the same track and cable lengths.

### Video Decoder/HDMI Receiver Latencies

All video decoders introduce latency that can vary depending on the enabled features. Moreover, some video parts contain elements—such as a deep-color FIFO—that can add random startup latency. A typical stereoscopic system using video decoders may have a random startup delay of around 5 pixel clocks. A system containing HDMI transmitters and receivers, as shown in Figure 10, may have a random startup delay of around 40 pixel clocks.

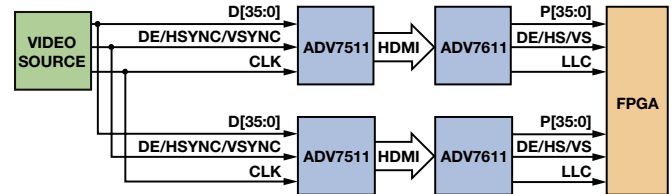


Figure 10. Pipeline delays measurement setup.

### Misalignment Compensation

Figure 11 shows a system where an analog signal from each camera is digitized by a video decoder. The data and clock are separate for each video path. Both video paths are connected to FIFOs, which buffer the incoming data to compensate for data misalignment. When clocking out the data, the FIFOs use a common clock from one of the decoders. In a locked system, the two data paths should have exactly the same clock frequency, ensuring that no FIFO overflows or underflows as long as the cameras are line-locked and the video decoders are locked.

By enabling or disabling FIFOs outputs, the control block maintains FIFO levels to minimize pixel misalignment. If compensation is carried out properly, the output of the FPGA block should be two data paths aligned to the very first pixel. That data is then supplied to an FPGA back end for 3D format production.

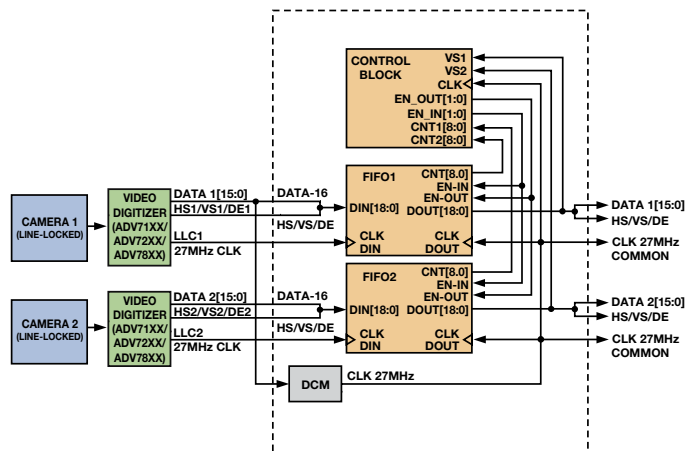


Figure 11. Using digital FIFOs to realign video pictures.

## Misalignment Measurement

Misalignment between two digitized data streams can be measured at the output of the video FIFOs by using a one-clock counter that is reset on the vertical sync (VS) pulse of one of the incoming signals. Figure 12 shows two video streams (vs\_a\_in and vs\_b\_in) misaligned by 4 pixels. Counters measure the misalignment using the method shown in Listing 1. Counting starts on the rising edge of VS1 and stops on the rising edge of VS2.

If the total pixel length of a frame is known, the negative skew (VS2 preceding VS1) can be calculated by subtracting the count value from the length of frame. This negative value should be calculated when the skew exceeds half of the pixel frame length. The result should be used to realign the data stored in the FIFOs.

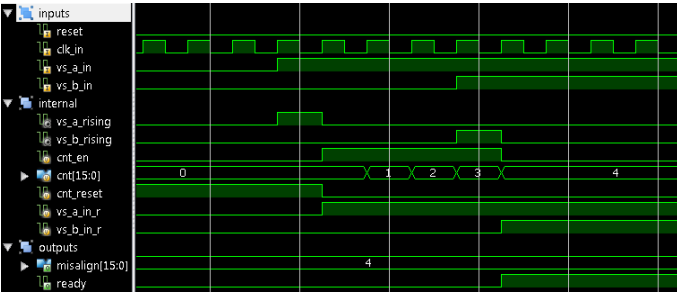


Figure 12. Misalignment measurement.

Listing 1. Simple misalignment measurement (Verilog®).

```

module misalign_measurement(
    input wire reset,
    input wire clk_in,
    input wire vs_a_in,
    input wire vs_b_in,
    output reg [15:0] misalign,
    output reg ready);

reg [15:0] cnt;
reg cnt_en, cnt_reset;
reg vs_a_in_r, vs_b_in_r;
assign vs_a_rising = vs_a_in > vs_a_in_r;
assign vs_b_rising = vs_b_in > vs_b_in_r;

always @(posedge clk_in)
begin
    vs_a_in_r <= vs_a_in;
    vs_b_in_r <= vs_b_in;
end

always @(posedge clk_in)
    if (reset)
        begin
            { ready, cnt_en } <= 2'b00;
            misalign <= 0;
        end else begin
            if ((vs_a_in == 1'b0) && (vs_b_in == 1'b0))
                { ready, cnt_reset } <= 2'b01;
            else
                cnt_reset <= 1'b0;

            /* beginning */
            if (vs_a_rising && vs_b_rising)
                begin
                    misalign <= 0;
                    { ready, cnt_en } <= 2'b10;
                end
            else if ((vs_a_rising > vs_b_in) || (vs_b_rising > vs_a_in))
                { ready, cnt_en } <= 2'b01;

            /* ending */
            if ((cnt_en == 1'b1) && (vs_a_rising || vs_b_rising))
                begin
                    { ready, cnt_en } <= 2'b10;
                    misalign <= vs_a_rising ? -(cnt + 1) : (cnt + 1);
                end
            end

            cnt <= 0;
            else if (cnt_en)
                cnt <= cnt + 1;

        endmodule
    
```

```

/* beginning */
if (vs_a_rising && vs_b_rising)
begin
    misalign <= 0;
    { ready, cnt_en } <= 2'b10;
end
else if ((vs_a_rising > vs_b_in) || (vs_b_rising > vs_a_in))
    { ready, cnt_en } <= 2'b01;

/* ending */
if ((cnt_en == 1'b1) && (vs_a_rising || vs_b_rising))
begin
    { ready, cnt_en } <= 2'b10;
    misalign <= vs_a_rising ? -(cnt + 1) : (cnt + 1);
end
end

always @(posedge clk_in) /* counter */
    if ((cnt_reset) || (reset))

        cnt <= 0;
        else if (cnt_en)
            cnt <= cnt + 1;

endmodule
    
```

## Production of 3D Video from Two Aligned Video Streams

Once pixel, line, and frame data are truly synchronous, an FPGA can form the video data into a 3D video stream, as shown in Figure 13.

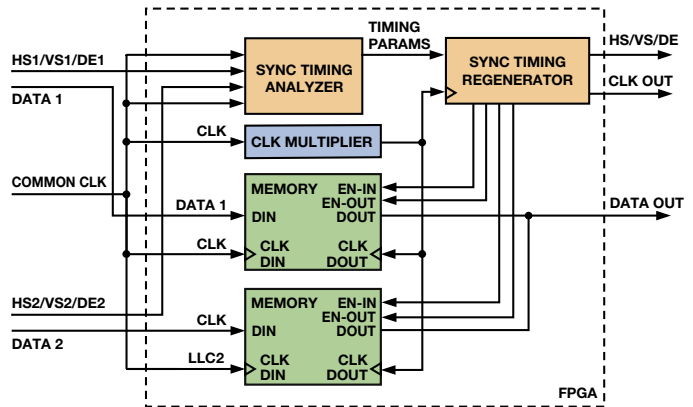


Figure 13. Simplified architecture that achieves 3D formats.

The incoming data is read into memory by a common clock. The sync timing analyzer examines the incoming synchronization signals and extracts the video timing, including horizontal front and back porch lengths, vertical front and back porches, horizontal and vertical sync length, horizontal active line length, the number of vertical active lines, and polarization of sync signals. Passing this information to the sync timing regenerator along with the current horizontal and vertical pixel location allows it to generate timing that has been modified to accommodate the desired 3D video structure. The newly created timing should be delayed to ensure that the FIFOs contain the required amount of data.

### Side-by-Side 3D Video

The least demanding architecture in terms of memory is the side-by-side format, which requires only a 2-line buffer (FIFOs) to store content of lines coming from both video sources. The side-by-side format should be twice as wide as the original incoming format. To achieve that, a doubled clock should be used for clocking the

regenerated sync timing with doubled horizontal line length. The doubled clock used for clocking the back end will empty the first FIFO and then the second FIFO at a double rate, allowing it to put pictures side-by-side, as shown in Figure 14. The side-by-side picture is shown in Figure 15.

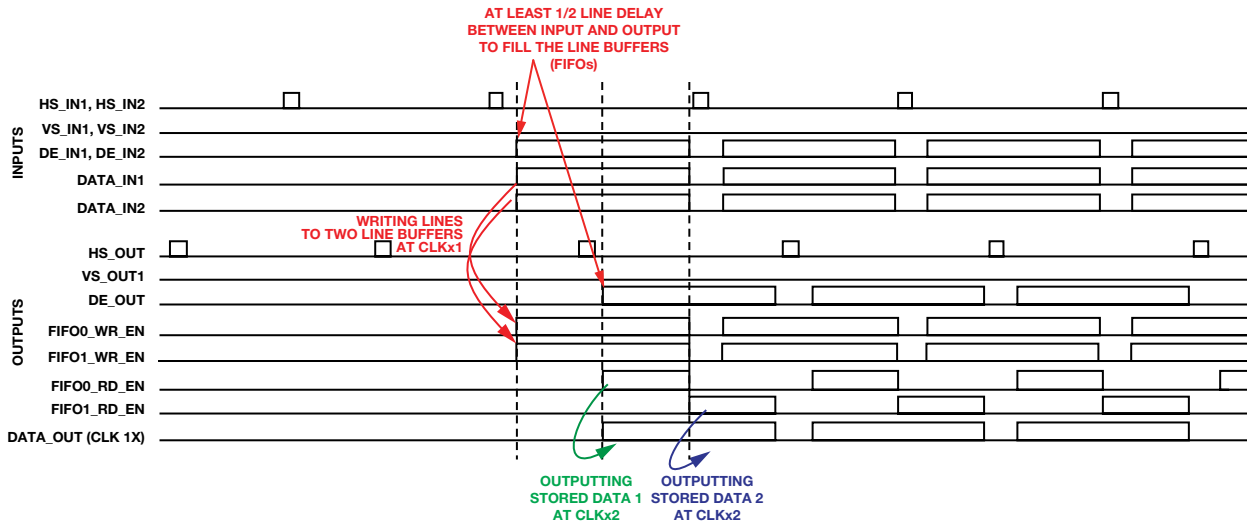


Figure 14. Stitching two pictures side-by-side using simple FPGA line buffers.



Figure 15. Side-by-side 576p picture with video timings

### Conclusion

Analog Devices decoders and HDMI products along with simple postprocessing can create and enable the transmission of true stereoscopic 3D video. As shown, it is possible to achieve 3D video with simple digital blocks and without expensive memory. This system can be used in any type of system requiring 3D vision, from simple video recording cameras to specialized ADSP-BF609 DSP-based systems that can be used for tracking objects and their distances.

### Author

**Witold Kaczurba** [[witold.kaczurba@analog.com](mailto:witold.kaczurba@analog.com)], a senior applications engineer in the Advanced TV group in Limerick, Ireland, supports decoders and HDMI products. He joined ADI in 2007 after graduating from the Technical University of Wroclaw, Poland, with an MSc in electrical engineering. As a student, he worked for small electronic and IT companies, then joined ADI in Ireland as a co-op student and subsequently as an applications engineer.



# Successive-Approximation ADCs: Ensuring a Valid First Conversion

By Steven Xie

## Introduction

Successive-approximation analog-to-digital converters (ADCs) with up to 18-bit resolution and 10-MSPS sample rates meet the demands of many data-acquisition applications, including portable, industrial, medical, and communications. This article shows how to initialize a successive-approximation ADC to get valid conversions.

## Successive-Approximation Architecture

Successive-approximation ADCs comprise four main subcircuits: the sample-and-hold amplifier (SHA), analog comparator, reference digital-to-analog converter (DAC), and successive-approximation register (SAR). Because the SAR controls the converter's operation, successive-approximation converters are often called SAR ADCs.

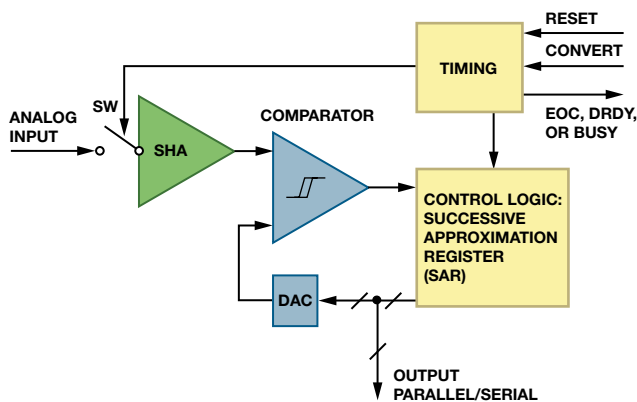


Figure 1. Basic SAR ADC architecture.

After power-up and initialization, a signal on CONVERT starts the conversion cycle. The switch closes, connecting the analog input to the SHA, which acquires the input voltage. When the switch opens, the comparator determines whether the analog input, which is now stored on the hold capacitor, is greater than or less than the DAC voltage. To start, the most significant bit (MSB) is on, setting the DAC output voltage to midscale. After the comparator output has settled, the successive-approximation register turns off the MSB if the DAC output was larger than the analog input, or keeps it on if the output was smaller. The process repeats with the next most significant bit, turning it off if the comparator determines that the DAC output is larger than the analog input, or keeping it on if the output was smaller. This binary search continues until every bit in the register is tested. The resulting DAC input is a digital approximation of the sampled input voltage, and is output by the ADC at the end of the conversion.

## Factors Related To SAR Conversion Code

This article discusses the following factors as they relate to valid first conversions:

- Power Supply Sequence (AD765x-1)
- Access Control (AD7367)
- RESET (AD765x-1/AD7606)

- $REF_{IN}/REF_{OUT}$  (AD765x-1)
- Analog Input Settling Time (AD7606)
- Analog Input Range (AD7960)
- Power-Down/Standby Mode (AD760x)
- Latency Delay (AD7682/AD7689, AD7766/AD7767)
- Digital Interfacing Timing

## Power Supply Sequencing

Some ADCs that operate with multiple supplies have well-defined power-up sequences. The AN-932 Application Note, [Power Supply Sequencing](#), provides a good reference for designing power supplies for these ADCs. Special attention should be paid to the analog and reference inputs, as these typically should not exceed the analog supply voltage by more than 0.3 V. Thus,  $AGND - 0.3\text{ V} < V_{IN} < V_{DD} + 0.3\text{ V}$  and  $AGND - 0.3\text{ V} < V_{REF} < V_{DD} + 0.3\text{ V}$ . The analog supplies should be turned on before the analog input or reference voltage, or the analog core could power up in a latched-up state. In a similar fashion, the digital inputs should be between  $DGND - 0.3\text{ V}$  and  $V_{IO} + 0.3\text{ V}$ . The I/O supply must be turned on before (or at the same time as) the interface circuitry, or ESD diodes on these pins could become forward-biased and power up the digital core in an unknown state.

## Data Access During Power Supply Ramp

Do not access the ADC before the power supplies are stable, as this may put it into an unknown state. Figure 2 shows an example where the host FPGA is trying to read data from an [AD7367](#) while  $DV_{CC}$  is ramping up, which may put the ADC into an unknown state.

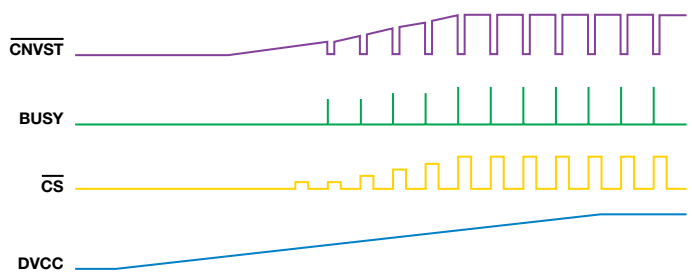


Figure 2. Reading data during  $DV_{CC}$  ramp-up.

## SAR ADC Initialization with Reset

Many SAR ADCs, such as the [AD760x](#) and the [AD765x-1](#), require a RESET for initialization after power-up. After all power supplies are stable, a specified RESET pulse should be applied to guarantee that the ADC starts in the intended state, with digital logic control in the default state and the conversion data register cleared. Upon power up, voltage starts to build up on the  $REF_{IN}/REF_{OUT}$  pin, the ADC is put into acquisition mode, and the user-specified mode is configured. Once fully powered up, the [AD760x](#) should see a rising edge RESET to configure it for normal operation. The RESET high pulse should typically be 50 ns wide.

## Establishing the Reference Voltage

The ADC converts the analog input voltage to a digital code referred to the reference voltage, so the reference voltage must be stable before the first conversion. Many SAR ADCs have a  $REF_{IN}/REF_{OUT}$  pin and a REF or REFCAP pin. An external reference can overdrive the internal reference via the  $REF_{IN}/REF_{OUT}$  pin or the internal reference can drive the buffer



directly. A capacitor on the REFCAP pin decouples the internal buffer output, which is the reference voltage used for conversion. Figure 3 shows a reference circuit example from the AD765x-1 data sheet.

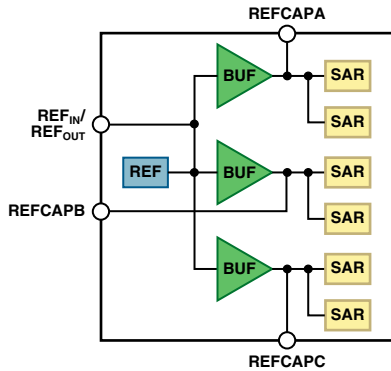


Figure 3. AD765x-1 reference circuit.

Make sure that the voltage on REF or REFCAP has settled before the first conversion. The slew rate and settling time varies for different reservoir capacitors, as shown in Figure 4.

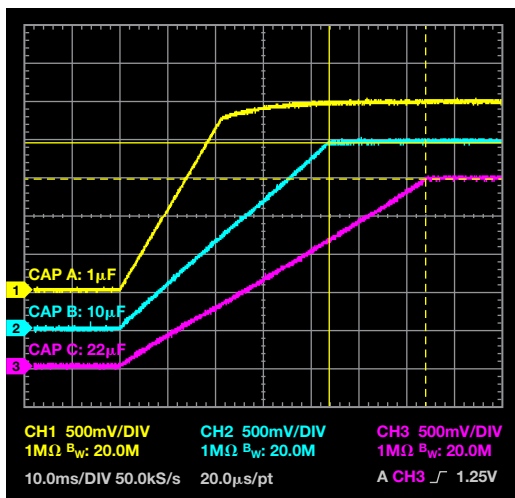


Figure 4. Voltage ramp on AD7656-1 REFCAPA/B/C pins with different capacitors.

In addition, a poorly designed reference circuit can cause serious conversion errors. The most common manifestation of a reference problem is “stuck” codes, which may be caused by the size and placement of the reservoir capacitor, insufficient drive strength, or a large amount of noise on the input. [Voltage Reference Design for Precision Successive-Approximation ADCs](#) by Alan Walsh (*Analog Dialogue* Volume 47, Number 2, 2013) provides details regarding reference design for SAR ADCs.

### Analog Input Settling Time

For multichannel, multiplexed applications, the driver amplifier and the ADC’s analog input circuitry must settle to the 16-bit level (0.00076%) for a full-scale step on the internal capacitor array. Unfortunately, amplifier data sheets typically specify settling to a 0.1% or 0.01% level. The specified settling time could differ significantly from the settling time at a 16-bit level, so verification is required prior to driver selection.

Pay special attention to settling time in multiplexed applications. After the multiplexer switches, make sure to allow enough time for the analog input to settle to the specified accuracy before the conversion starts. When using the AD7606 with a multiplexer, allow at least 80  $\mu$ s for the  $\pm 10$ -V input range and 88  $\mu$ s for the

$\pm 5$ -V range to give the selected channel enough time to settle to 16-bit resolution. [Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter](#) by Alan Walsh (*Analog Dialogue* Volume 46, Number 4, 2012) provides additional details regarding amplifier selection.

### Analog Input Range

Make sure the analog input is within the specified input range, taking special care of differential input ranges with a specified common-mode voltage, as shown in Figure 5.

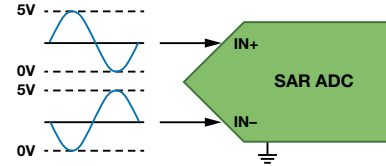


Figure 5. Fully differential input with common-mode voltage.

For example, the AD7960 18-bit, 5-MSPS SAR ADC’s differential input range is  $-V_{REF}$  to  $+V_{REF}$ , but both  $V_{IN+}$  and  $V_{IN-}$  referred to ground should be in the  $-0.1$  V to  $V_{REF} + 0.1$  V range, and the common-mode voltage should be around  $V_{REF}/2$ , as shown in Table 1.

Table 1. Analog Input Specifications for the AD7960

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Voltage Range	$V_{IN+} - V_{IN-}$	$-V_{REF}$		$+V_{REF}$	V
Operating Input Voltage	$V_{IN+}, V_{IN-}$ to GND	-0.1		$V_{REF} + 0.1$	V
Common-Mode Input Range		$V_{REF}/2 - 0.05$	$V_{REF}/2$	$V_{REF}/2 + 0.05$	V

### Bringing the SAR ADC Out of Power-Down or Standby Mode

To conserve power, some SAR ADCs go into power-down or standby mode when they are idle. Make sure that the ADC comes out of this low-power mode before the first conversion starts. For example, the AD7606 family offers two power-saving modes: full shutdown and standby. These modes are controlled by GPIO pins STBY and RANGE.

Figure 6 shows that when  $\overline{STBY}$  and RANGE return high, the AD7606 goes from full shutdown mode into normal mode and is configured for the  $\pm 10$ -V range. At this point, the REGCAPA, REGCAPB, and REGCAP pins power up to the correct voltages as outlined in the data sheet. When placed in standby mode, the power-up time is approximately 100  $\mu$ s, but it takes approximately 13 ms in external reference mode. When powered up from shutdown mode, a RESET signal must be applied after the required power-up time has elapsed. The data sheet specifies the time required between power-up and a rising edge on RESET as  $t_{WAKE-UP SHUTDOWN}$ .

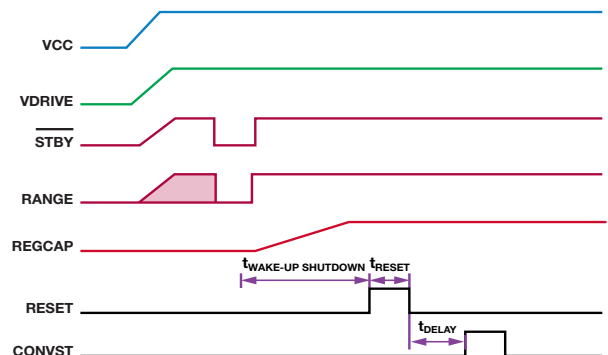


Figure 6. AD7606 initialization timing.

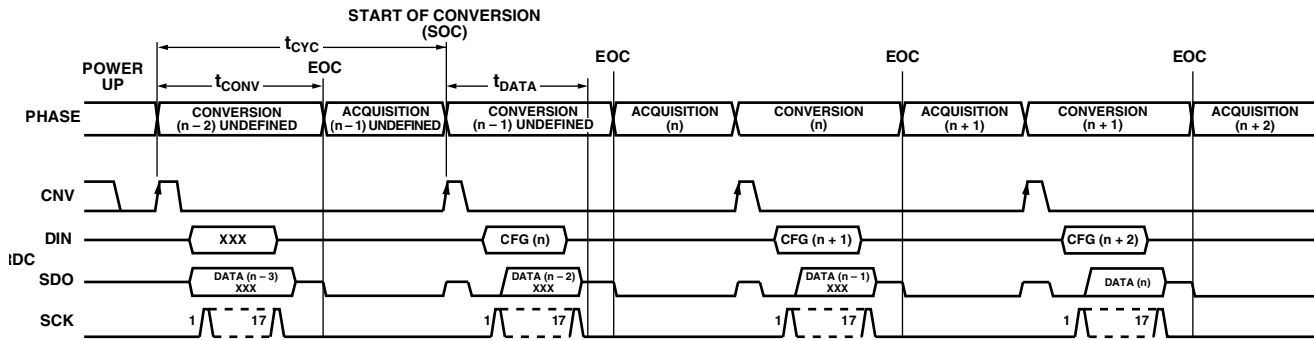


Figure 7. General timing for AD7682/AD7689.

### SAR ADCs with Latency Delay

A common belief is that SAR ADCs have no latency delay, but some SAR ADCs have a latency delay for configuration updates, so the first valid conversion code may be undefined until the latency delay—which may be several conversion periods—has passed.

For example, the [AD7985](#) features two conversion modes of operation: turbo and normal. Turbo mode, which allows the fastest conversion rate of up to 2.5 MSPS, does not power down between conversions. The first conversion in turbo mode contains meaningless data, and should be ignored. In normal mode, on the other hand, the first conversion is meaningful.

For the [AD7682/AD7689](#), the first three conversion results after power-up are undefined, as a valid configuration does not take place until after the second EOC. Therefore, two dummy conversions are required, as shown in Figure 7.

When using the AD765x-1 in hardware mode, the logic state of the RANGE pin is sampled on the falling edge of the BUSY signal to determine the range for the next simultaneous conversion. After a valid RESET pulse, the AD765x-1 defaults to operating in the  $\pm 4 \times V_{REF}$  range, with no latency problem. If, however, the AD765x-1 operates in  $\pm 2 \times V_{REF}$  range, one dummy conversion cycle must be used to select the range at the first falling edge of BUSY.

In addition, some SAR ADCs, such as the [AD7766/AD7767](#) oversampled SAR ADC, have postdigital filters that cause additional latency delay. When multiplexing analog inputs to this type of ADC, the host must wait the full digital filter settling time before a valid conversion result can be achieved; the channel can be switched after this settling time.

As shown in Table 2, the latency of the AD7766/AD7767 is 74 divided by the output data rate (74/ODR). When running at the maximum output data rate of 128 kHz, the AD7766/AD7767 allows a 1.729-kHz multiplexer switching rate.

Table 2. Digital Filter Latency of AD7766/AD7767

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Group Delay			37/ODR		$\mu$ s
Settling Time (Latency)	Complete settling		74/ODR		$\mu$ s

### Digital Interfacing Timing

Last, but not least, the host can access the conversion results from SAR ADCs through some common interface options, such as parallel, parallel BYTE, IIC, SPI, and SPI in daisy-chain mode. To get valid conversion data, make sure to follow the digital interfacing timing specifications in the data sheet.

### Conclusion

To get a first valid conversion code from SAR ADCs, please follow the recommendations discussed in this article. Other specific configuration support may be needed; consult the target SAR ADC data sheet or application note for initialization before the first conversion cycle starts.

### References

- Kester, Walt. [Data Converter Support Circuits](#). Chapter 7, *Data Converter Handbook*.
- Kester, Walt. “Which ADC Architecture Is Right for Your Application?” *Analog Dialogue*, Volume 39, Number 2, 2005.
- Walsh, Alan. “Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter.” *Analog Dialogue*, Volume 46, Number 4, 2012.

### Author

**Steven Xie** [[steven.xie@analog.com](mailto:steven.xie@analog.com)] has worked as an ADC applications engineer with the China Design Center in ADI Beijing since March 2011. He provides technical support for precision ADC products across China. Prior to that, he worked as a hardware designer in the Ericsson CDMA team for four years. In 2007, Steven graduated from Beihang University with a master’s degree in communications and information systems.



# Highest Power Density, Multirail Power Solution for Space-Constrained Applications

By Maurice O'Brien

As the overall size of communications, medical, and industrial equipment continues to decrease, power management becomes an increasingly important design consideration. This article looks at applications for new highly integrated power management solutions, the advantages these new devices bring for powering RF systems, FPGAs, and processors, and a design tool that helps empower designers to quickly implement a new design.

The emergence of femtocells and picocells in communications infrastructure is driving the need for smaller base stations, which have complex requirements for powering digital baseband, memory, RF transceivers, and power amplifiers in the smallest area with the highest power efficiency, as shown in Figure 1. A typical small cell system needs a very dense power supply that can deliver large currents with fast transient response to power the digital baseband, along with low-noise, low-dropout regulators (LDOs) to power the AD9361 RF Agile Transceiver,™ temperature compensated crystal oscillator (TCXO), and other noise-critical rails. Setting the switching frequency of the switching regulators outside of the critical RF bands reduces noise, and synchronizing the switching regulators ensures that beat frequencies do not affect the RF performance. Reducing the core voltage ( $V_{CORE}$ ) of the digital baseband minimizes power consumption for low-power modes, and supply sequencing ensures that the digital baseband processor is up and running before the RF transceiver is enabled. An I<sup>2</sup>C interface between the digital baseband and the power management allows the output voltages of the buck regulators to be changed. To increase reliability, the power management system can monitor its own input voltage and die temperature, reporting any faults to the baseband processor.

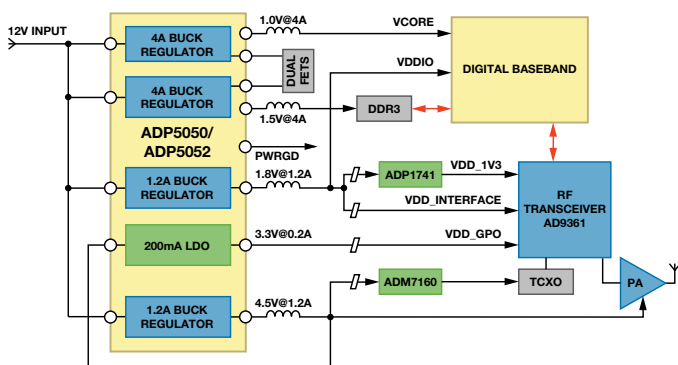


Figure 1. Small base stations require a variety of power supplies.

Similarly, the trend in medical and instrumentation devices—for example, portable ultrasound and handheld instrumentation—is toward significantly smaller form factors, so these products are driving the need for smaller, more efficient ways of powering FPGAs, processors, and memory, as shown in Figure 2. A typical FPGA and memory design needs a very dense power supply that can deliver large currents with fast transient response to power the core and I/O rails, along with a low-noise rail to power on-chip analog circuitry such as a phase-locked loop (PLL). Power supply

sequencing is critical to ensure that the FPGA is up and running before the memory is enabled. Regulators with a precision enable input and a dedicated power-good output allow power supply sequencing and fault monitoring. Power supply designers often want to use the same power IC in different applications, so the ability to change the current limits is important. This design reuse can significantly reduce time to market—a critical element in any new product development process.

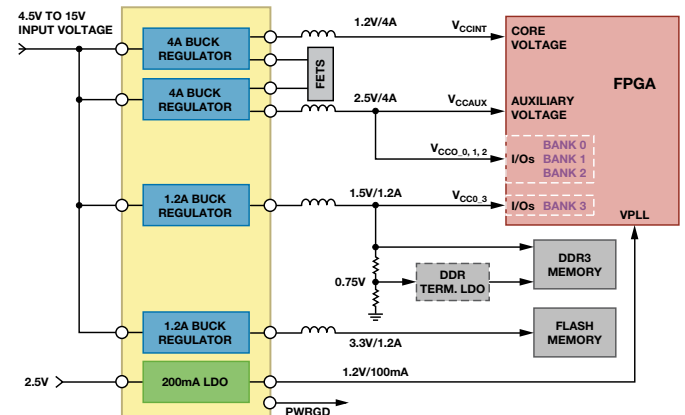


Figure 2. Powering an FPGA-based system.

Consider a common multirail power management design specification for an FPGA with a 12-V input and five outputs:

- Core: 1.2 V @ 4 A
- Auxiliary: 1.8 V @ 4 A
- I/O: 3.3 V @ 1.2 A
- DDR memory: 1.5 V @ 1.2 A
- Clock: 1.0 V @ 200 mA

A typical discrete implementation, shown in Figure 3a, connects four switching regulators to the 12-V input rail. The output of one switching regulator preregulates the LDO to reduce power dissipation. An alternative approach, shown in Figure 3b, uses one regulator to step the 12-V input down to a 5-V intermediate rail, which is then regulated down to produce each of the required voltages. This implementation has a lower solution cost, but also a lower efficiency due to the two-stage power conversion. In both cases, each regulator has to be enabled independently, so supply sequencing may require a dedicated power supply sequencer. Noise may also be an issue, unless all of the switchers can be synchronized to reduce beat frequencies.

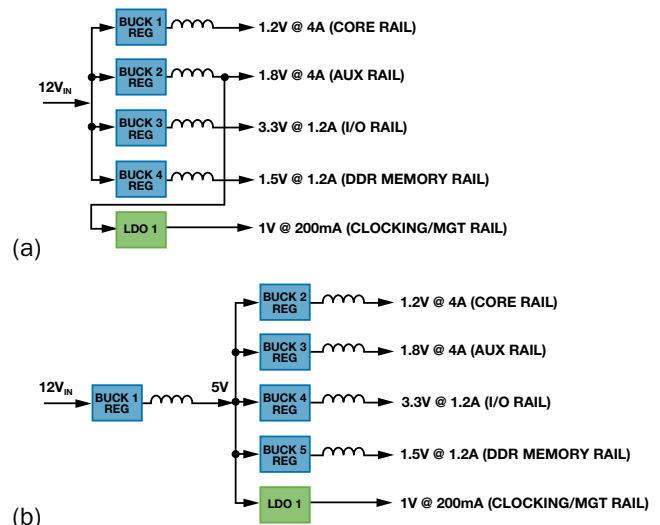


Figure 3. (a) Discrete regulator design and (b) alternative discrete regulator design.

### Integrated Solution Yields High Efficiency, Small Size

Integrating multiple buck regulators and LDOs into a single package can significantly reduce the overall size of a power management design. In addition, smart integrated solutions provide many advantages over traditional discrete implementations. Reducing the number of discrete components can significantly reduce the cost, complexity, and manufacturing cost of the design. The ADP5050 and ADP5052 integrated power management units (PMUs) can implement all these voltages and features in a single IC, using significantly less PCB area and fewer components.

For highest efficiency, each of the buck regulators can be powered directly from 12 V (similar to Figure 3a), removing the need for a preregulator stage. Buck 1 and Buck 2 have programmable current limits (4 A, 2.5 A, or 1.2 A), allowing the power supply designer to quickly and easily change the currents for new designs and significantly reducing the development time. The LDO can be powered from a 1.7-V to 5.5-V supply. In this example, the 1.8-V output from one of the buck regulators powers the LDO to provide a low-noise 1-V rail for the noise-sensitive analog circuitry.

The switching frequency,  $f_{SW}$ , is set between 250 kHz and 1.4 MHz by resistor  $R_{RT}$ . The flexible switching frequency range allows the power supply designer to optimize the design, reducing the frequency for highest efficiency or increasing the frequency for smallest overall size. Figure 4 shows the relationship between  $f_{SW}$  and  $R_{RT}$ . The value of  $R_{RT}$  can be calculated as

$$R_{RT} = (14822/f_{SW})^{1.081}, \text{ with R in k}\Omega \text{ and f in kHz.}$$

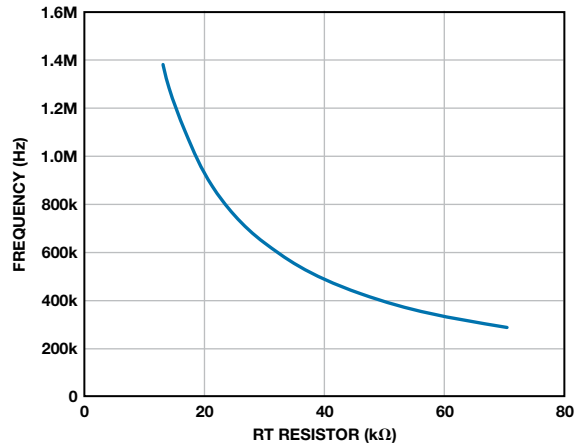
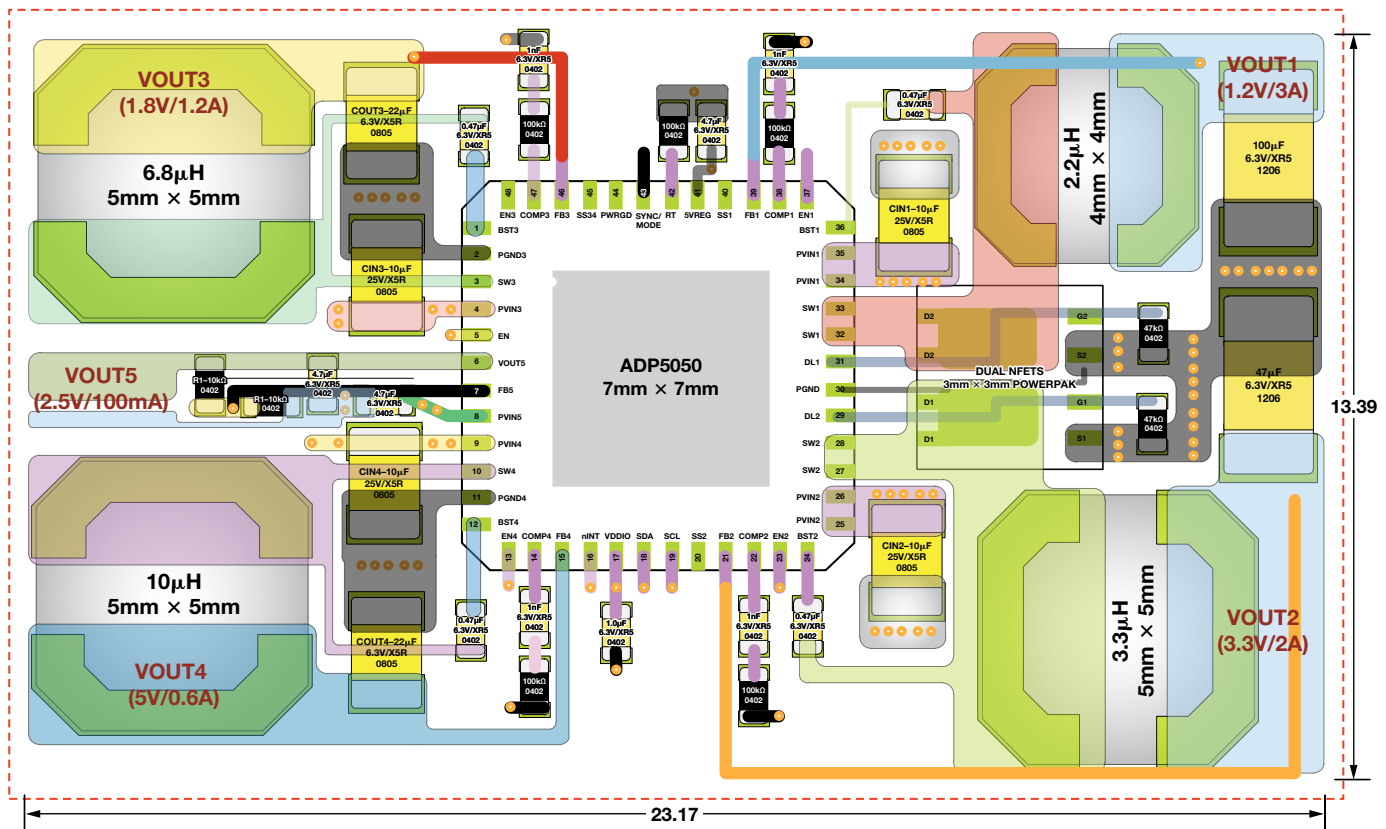


Figure 4. Switching frequency vs.  $R_{RT}$ .

In some designs it is desirable to have both: a lower switching frequency to provide the highest power efficiency for the higher current rails, and a higher switching frequency to reduce inductor size and minimize PCB area for the lower current rails. A divide-by-two option on the master switching frequency allows the ADP5050 to operate at two frequencies, as shown in Figure 5. The switching frequency for Buck 1 and Buck 3 can be set via the I<sup>2</sup>C port to one-half of the master switching frequency.



TOTAL PCB AREA AROUND 23mm × 13.5mm = 310mm<sup>2</sup>

#### LAYOUT EXAMPLE:

- $V_{IN} = 12V$
- BUCK 1: 3A @ 600kHz
- BUCK 2: 2A @ 1.2MHz
- BUCK 3: 1.2A @ 600kHz
- BUCK 4: 0.6A @ 1.2MHz
- LDO: 0.1A

Figure 5. The ADP5050 operates at a low switching frequency for high efficiency on high-current rails and a high frequency for small inductor size on low-current rails.

## Power Supply Sequencing

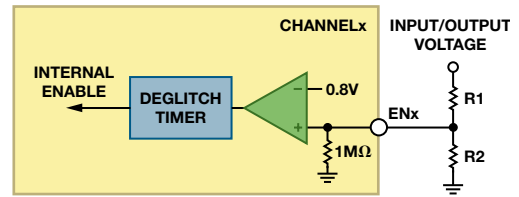
As shown in Figure 6, the ADP5050 and ADP5052 have four features that simplify power supply sequencing that is required for applications using FPGAs and processors: precision enable inputs, programmable soft start, a power-good output, and an active output discharge switch.

**Precision Enable Inputs:** Each regulator, including the LDO, has an enable input with a precise 0.8-V reference (Figure 6-1). When the voltage at an enable input is greater than 0.8 V, the regulator is enabled; when the voltage falls below 0.725 V, the regulator is disabled. An internal 1-M $\Omega$  pull-down resistor prevents errors if the pin is left floating. The precision enable threshold voltage allows easy sequencing within the device, as well as with external supplies. As an example, if Buck 1 is set to 5 V, a resistor divider can be used to set an accurate 4.0-V trip point to enable Buck 2, and so on, setting an accurate power-up sequence for all outputs.

**Programmable Soft Start:** Soft start circuitry ramps the output voltage in a controlled manner, limiting the inrush current. The soft start time is set to 2 ms when the soft start pins are tied to  $V_{REG}$ , or it can be increased up to 8 ms by connecting a resistor divider from the soft start pin to  $V_{REG}$  and ground (Figure 6-2). This configuration may be required to accommodate a specific start-up sequence or an application with a large output capacitor. The configurability and flexibility of the soft start enable large, complex FPGAs and processors to power up in a safe, controlled manner.

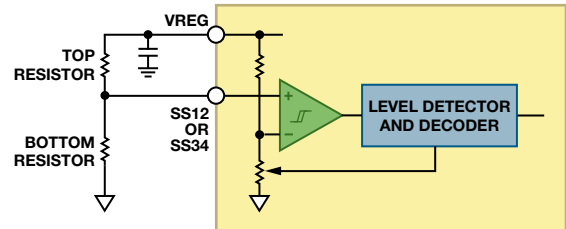
**Power-Good Output:** An open-drain power-good output (PWRGD) goes high when the selected buck regulators are operating normally (Figure 6-3). The power-good pins allow the power supply to signal the host system about its health. By default, PWRGD monitors the output voltage on Buck 1, but other channels can be custom ordered to control the PWRGD pin. The status of each channel (PWRGx bit) can be read back via the I<sup>2</sup>C interface on the ADP5050. A logic high on the PWRGx bit indicates that the regulated output voltage is above 90.5% of its nominal output. The PWRGx bit is set to logic low when the regulated output voltage falls below 87.2% of its nominal output for more than 50  $\mu$ s. The PWRGD output is the logical AND of the internal unmasked PWRGx signals. An internal PWRGx signal must be high for at least 1 ms before PWRGD goes high; if any PWRGx signal fails, PWRGD goes low with no delay. The channels that control PWRGD (Channel 1 to Channel 4) are specified by factory fuse or by setting bits via the I<sup>2</sup>C interface.

**Active Output Discharge Switch:** Each buck regulator integrates a discharge switch from the switching node to ground (Figure 6-4). Turned on when its associated regulator is disabled, the switch helps the output capacitor to discharge quickly. The typical resistance of the discharge switch is 250  $\Omega$  for Channel 1 to Channel 4. The active discharge switch pulls the output to ground when the regulator is disabled, even when a large capacitive load is present. This significantly increases the robustness of the system, particularly when it is power cycled.



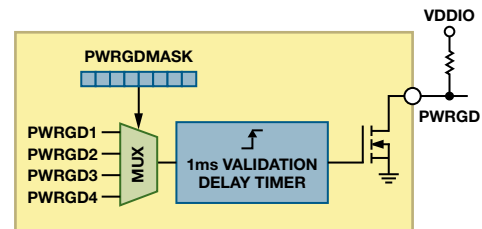
### 1. Precision Enabled Threshold

Above 0.8V to enable the regulator, below 0.72V (hysteresis) to shutdown the regulator.



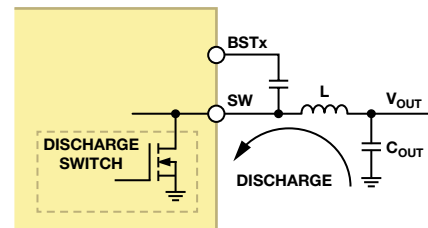
### 2. Programmable Soft Start

The different soft start on each channel can be programmable to be 2ms, 4ms, 8ms.



### 3. PWRGD Output

The desirable PWRGDx from CH1 to CH4 can be configured by the factory fuse or I<sup>2</sup>C.



### 4. Active Output Discharge Switch

The output discharge switch can be turned ON to shorten the discharge period of the output capacitors.

Figure 6. ADP5050 and ADP5052 simplify power supply sequencing.

Figure 7 shows a typical power-up/power-down sequence.

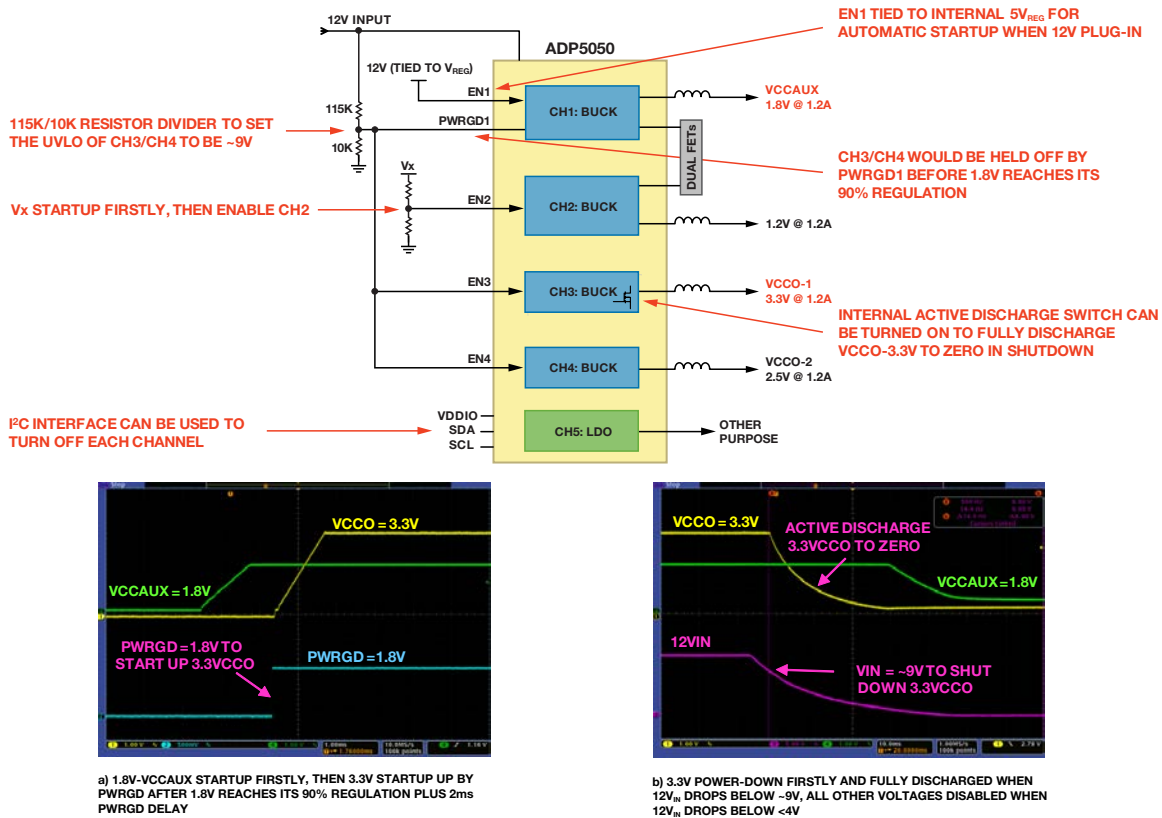


Figure 7. Typical power-up/power-down sequence.

### I<sup>2</sup>C Interface

The I<sup>2</sup>C interface enables advanced monitoring capability and basic dynamic voltage scaling of the two buck regulator outputs (Channel 1 and Channel 4).

**Input Voltage Monitor:** The input voltage can be monitored for faults such as undervoltage conditions. As an example, with 12 V applied to the input, the I<sup>2</sup>C interface is configured to trigger an alert if the input voltage falls below 10.2 V. The signal on a dedicated pin (nINT) tells the system processor that a problem has occurred and shuts the system down for corrective action. The ability to monitor the input voltage increases system reliability.

Figure 8 shows the values that can be programmed to monitor the input voltage of the ADP5050.

**Junction Temperature Monitor:** The junction temperature can be monitored for faults such as overtemperature conditions. If the junction temperature increases above a preset level (105°C, 115°C, or 125°C), an alert is signaled on nINT. Unlike thermal shutdown, this function sends a warning signal, but does not shut down the device. The ability to monitor the junction temperature and alert the system processor to possible systems failures before they happen increases the system reliability, as shown in Figure 9.

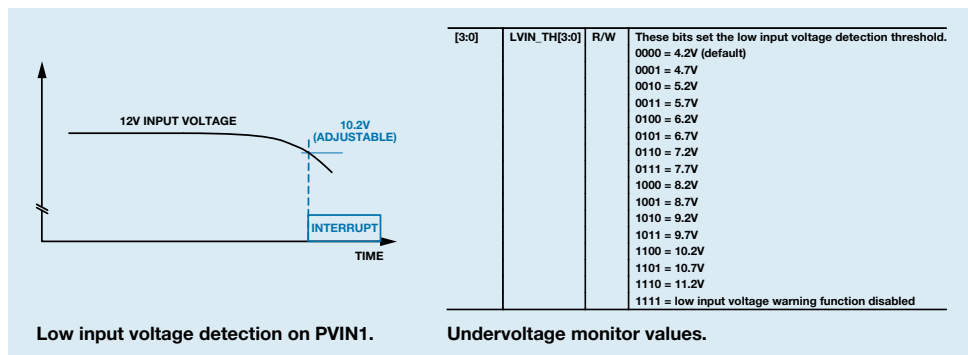


Figure 8. Input undervoltage detection.

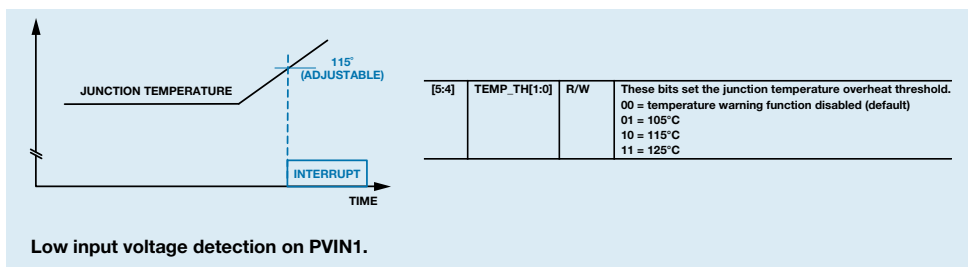


Figure 9. Junction temperature monitoring.

**Dynamic Voltage Scaling:** Dynamic voltage scaling allows the system to reduce power consumption by dynamically lowering the power supply voltage on Channel 1 and Channel 4 for low-power modes, or it can dynamically change the output voltage depending on the system configuration and system loading. Also, the output voltages of all four buck regulators can be set via the I<sup>2</sup>C interface, as seen in Figure 10.

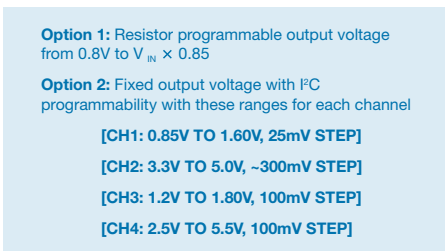


Figure 10. ADP5050 output voltage options.

### Low Noise Features

Several features reduce system noise generated by the power supply:

### Wide Resistor Programmable Switching Frequency Range:

A resistor on the RT pin programs the switching frequency between 250 kHz and 1.4 MHz. This flexibility allows the power supply designer to set the switching frequency to avoid system noise bands.

**Buck Regulator Phase Shifting:** The phase shift of the buck regulators can be programmed via the I<sup>2</sup>C interface. By default, the phase shift between Channel 1 and Channel 2 and between Channel 3 and Channel 4 is 180°, as shown in Figure 11. The benefit of out-of-phase operation is reduced input ripple current and less ground noise on the power supply.

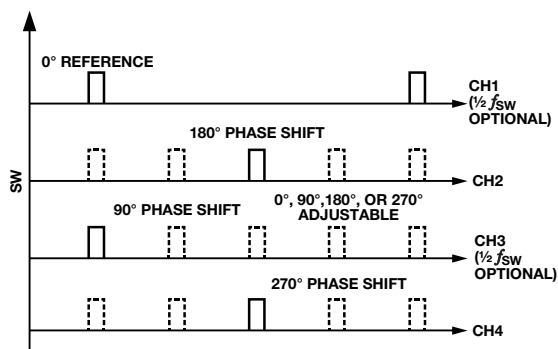


Figure 11. Phase shift of the buck regulators in the ADP5050/ADP5052.

The phase shift of Channel 2, Channel 3, and Channel 4 can be set to 0°, 90°, 180°, or 270° with respect to Channel 1 using the I<sup>2</sup>C interface, as shown in Figure 12. When parallel operation is configured to provide a single combined output of up to 8 A on Channel 1 and Channel 2, the switching frequency of Channel 2 is locked to a 180° phase shift with respect to Channel 1.

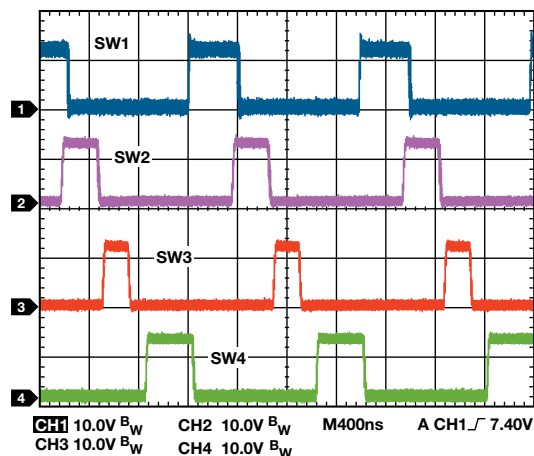


Figure 12. Phase shift of buck regulators can be configured via the I<sup>2</sup>C interface.

**Clock Synchronization:** The switching frequency can be synchronized to an external clock in the 250-kHz to 1.4-MHz range via the SYNC/MODE pin. This ability is important in RF and noise-sensitive applications. When an external clock is detected, the switching frequency transitions smoothly to its frequency. When the external clock stops, the device switches back to the internal clock and continues to operate normally. Synchronizing to an external clock allows the system designer to stay away from critical noise frequency bands and reduces the noise generated by multiple devices in a system.

For successful synchronization, the internal switching frequency must be programmed to a value close to that of the external clock value; a frequency difference of less than ±15% is suggested.

The SYNC/MODE pin can be configured as a synchronization clock output via a factory fuse or the I<sup>2</sup>C interface. A positive clock pulse with a 50% duty cycle is generated at the SYNC/MODE pin with a frequency equal to the internal switching frequency. A short time delay (~15% of  $t_{SW}$ ) occurs between the generated synchronization clock and the Channel 1 switching node.

Figure 13 shows two devices configured in frequency synchronization mode: one device is configured as the clock output to synchronize the other device. A 100 kΩ pull-up resistor should be used to prevent logic errors if the SYNC/MODE pin is left floating.

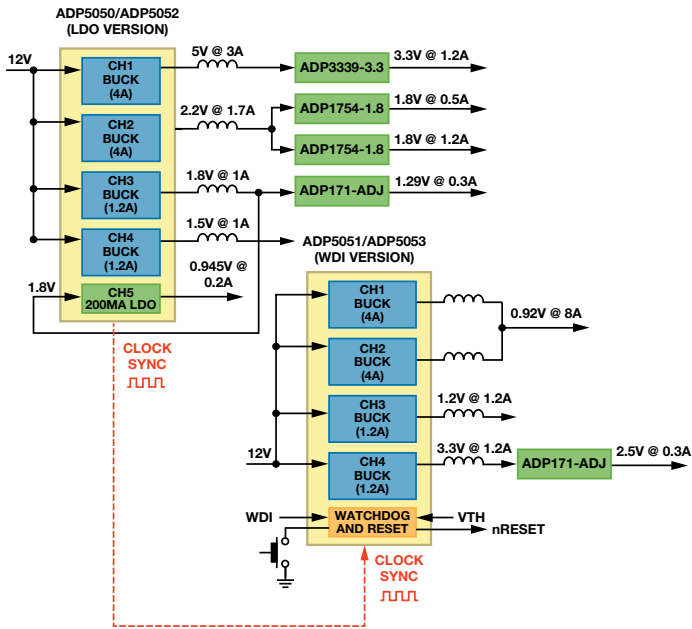


Figure 13. RF application shows two devices synchronized to reduce power supply noise.

Both devices are synchronized to the same clock, so the phase shift between Channel 1 of the first device and Channel 1 of the second device is 0°, as shown in Figure 14.

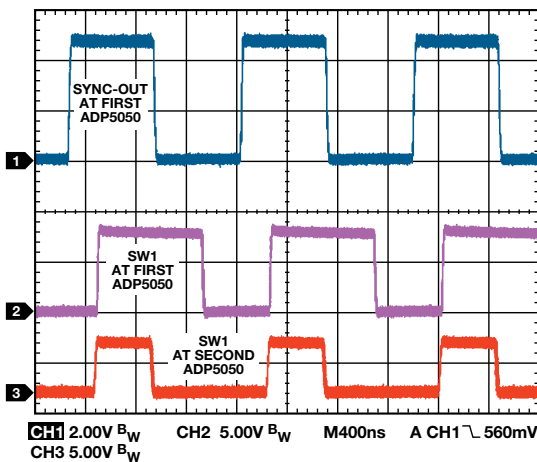


Figure 14. Waveforms of two ADP5050 devices operating in synchronized mode.

### ADIsimPower Design Tool

ADIsimPower™ now supports the ADP5050/ADP5052 multichannel high-voltage PMUs, which power 4/5 channels with load current up to 4 A per channel from inputs up to 15 V. The design tool allows users to optimize the design by cascading channels, placing high-current channels in parallel to create an 8-A rail, and considering the thermal contributions of each channel. With the advanced features, users can independently specify each channel's performance for ripple and transient performance, switching frequency, and channels that support half the master frequency.

ADIsimPower allows the user to quickly and easily input the design requirements on the software interface shown in Figure 15.

#### STEP 1:

OPTIMIZE FOR SIZE, COST, OR EFFICIENCY

#### STEP 2:

SPECIFY EACH CHANNEL'S OPERATING CONDITIONS, INCLUDING "DO NOT USE"



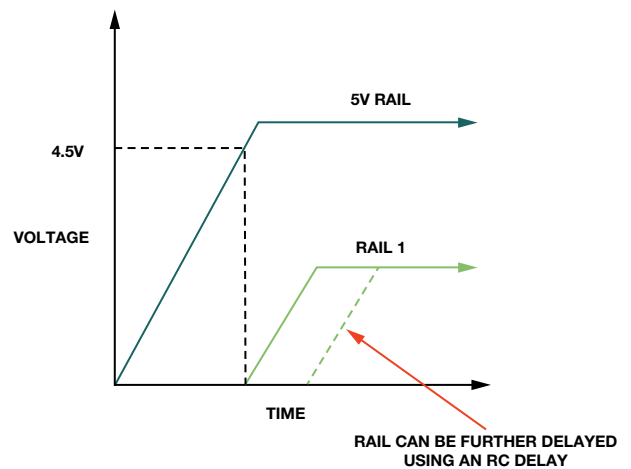
Figure 15. ADIsimPower software interface.

A full bill of materials is generated with intelligent component selection. Evaluation boards can be requested from within the tool. The design tool allows for sophisticated controls for each channel, as shown in Figure 16.

#### Rail 1 (Buck)

Vout Ripple	2	% = 100 mVppk
Istep	30	% = 0.3 Apk
Vstep	5	% = 250 mVpk
Soft Start Time	Automatic	
Enable/UVLO Setting	UVLO from Rail	
UVLO Rail	5	V
UVLO Threshold	90	% = 4.5 V
UVLO (Rising)	4.5	V
UVLO (Falling)	4.1	V
Half Frequency	<input type="checkbox"/>	

(a)



(b)

Figure 16. (a) Ripple, transient, and response can be specified for each rail. (b) Advanced sequencing requirements using precision enable.



ADIsimPower gives the power designer quick access to accurate, tested, reliable performance data, as shown in Figure 17.

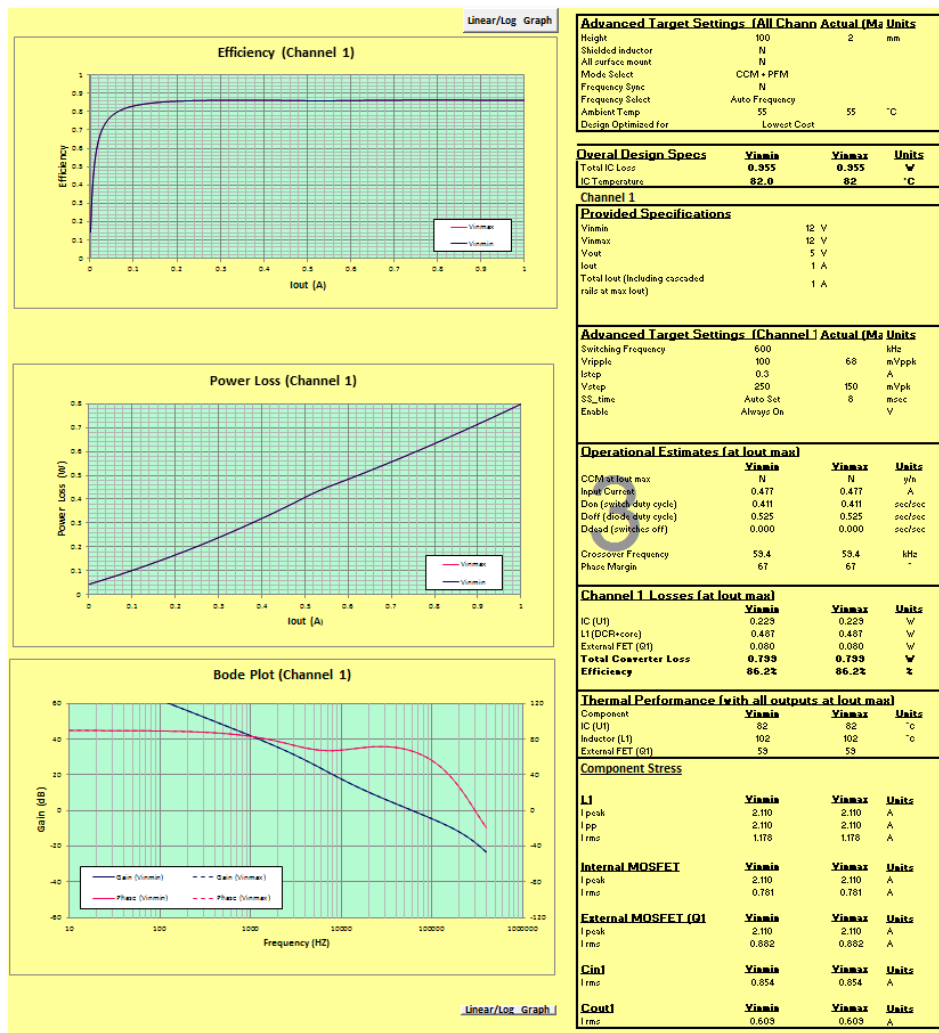


Figure 17. ADIsimPower simulation output.

The design can then be assembled on an evaluation board, as shown in Figure 18.

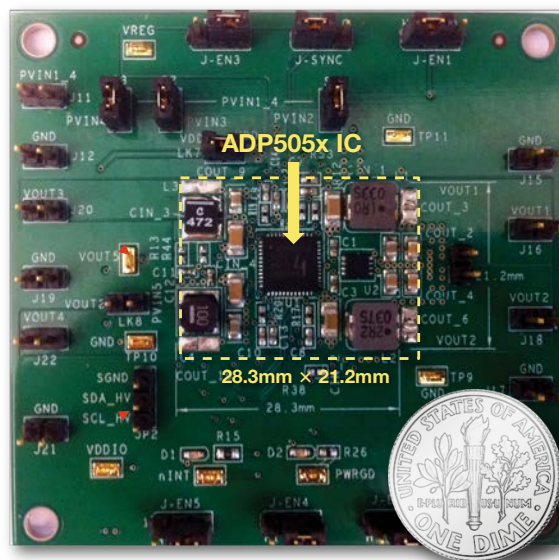


Figure 18. Power supply circuit using ADP5050/ADP5052.

## ADP5050/ADP5052/ADP5051/ADP5053 Specifications

Part Number	Description	V <sub>IN</sub> (V)	V <sub>OUT</sub> (V)	Number of Outputs	Output Current (mA)	I <sup>2</sup> C	Key Features	Package	Price (SU.S.)
ADP5050	Quad Buck Regulator, LDO, I <sup>2</sup> C	Buck: 4.5 to 15	0.8 to 0.85 × V <sub>IN</sub>	2 × Buck	4000, 2500, or 1200	Yes	I <sup>2</sup> C interface with individual enable pins and power good	48-lead LFCSP	4.39
				2 × Buck	1200				
				LDO	200				
ADP5051	Quad Buck Regulator, POR/WDI, I <sup>2</sup> C	Buck: 4.5 to 15	0.8 to 0.85 × V <sub>IN</sub>	2 × Buck	4000, 2500, or 1200	Yes	I <sup>2</sup> C interface with individual enable pins and power good	48-lead LFCSP	4.59
				2 × Buck	1200				
				LDO	200				
ADP5052	Quad Buck Regulator, LDO	Buck: 4.5 to 15	0.8 to 0.85 × V <sub>IN</sub>	2 × Buck	4000, 2500, or 1200	No	Individual enable pins and power good	48-lead LFCSP	3.59
				2 × Buck	1200				
				LDO	200				
ADP5053	Quad Buck Regulator, POR/WDI	Buck: 4.5 to 15	0.8 to 0.85 × V <sub>IN</sub>	2 × Buck	4000, 2500, or 1200	No	Individual enable pins and power good	48-lead LFCSP	3.79
				2 × Buck	1200				
				LDO	200				

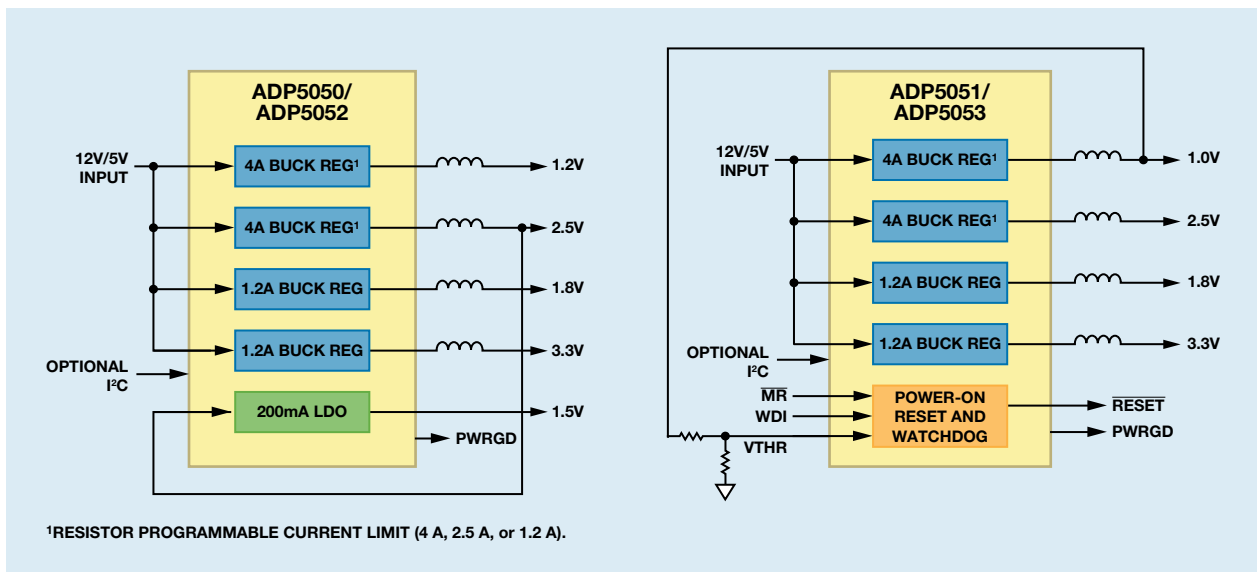


Figure 19. ADP5050/ADP5051/ADP5052/ADP5053: quad buck switching regulators with LDO or POR/WDI in LFCSP.

### Conclusion

New highly integrated PMUs are enabling complex power management solutions with high power efficiency, high reliability, and ultrasmall size; and new design tools combined with flexible integrated circuits reduce the time to market for these complex power supplies. The ADP505x family, the latest addition to ADI's portfolio of [highly integrated multi-output regulators](#), allows a single IC to be used quickly and easily in many different applications, reducing power supply design time. To discuss technical aspects of these devices, please visit the [EngineerZone®](#) forum.

### Author

**Maurice O'Brien** [[maurice.obrien@analog.com](mailto:maurice.obrien@analog.com)] joined Analog Devices in 2002, following his graduation from the University of Limerick, Ireland, with a bachelor's degree in electronic engineering. He currently works as a product marketing manager in the Power Management product line. In his spare time, Maurice enjoys horse riding, outdoor sports, and travel.



# MEMS Microphones, the Future for Hearing Aids

By Jerad Lewis and Dr. Brian Moss

Driven by aging populations and a pronounced increase in hearing loss, the market for hearing aids continues to grow, but their conspicuous size and short battery life turn many people off. As hearing loss becomes ever more common, people will look for smaller, more efficient, higher quality hearing aids. At the start of the hearing aid signal chain, microphones sense voices and other ambient sounds, so improved audio capture can lead to higher performance and lower power consumption throughout the signal chain.

Microphones are transducers that convert acoustical signals into electrical signals that can be processed by the hearing aid's audio signal chain. Many different types of technologies are used for this acoustic-to-electrical transduction, but condenser microphones have emerged as the smallest and most accurate. The diaphragm in condenser microphones moves in response to an acoustic signal. This motion causes a change in capacitance, which is then used to produce an electrical signal.

Electret condenser microphone (ECM) technology is the most widely used in hearing aids. ECMs implement a variable capacitor with one plate built from a material with a permanent electrical charge. ECMs are well established in today's hearing industry, but the technology behind these devices has remained relatively unchanged since the 1960s. Their performance, repeatability, and stability over temperature and other environmental conditions are not very good. Hearing aids, and other applications that value high performance and consistency, present an opportunity for a new microphone technology that improves on these shortcomings, allowing manufacturers to produce higher quality, more reliable devices.

Microelectromechanical systems (MEMS) technology is driving the next revolution in condenser microphones. MEMS microphones take advantage of the enormous advances made in silicon technology over the past decades—including ultrasmall fabrication geometries, excellent stability and repeatability, and low power consumption—all of which have become uncompromising requirements of the silicon industry. Until now, the power consumption and noise levels of MEMS microphones have been too high to make them appropriate for use in hearing aids, but new devices that meet these two key specifications are now enabling the next wave of innovation in hearing aid microphones.

## MEMS Microphone Operation

Like ECMs, MEMS microphones operate as condenser microphones. MEMS microphones consist of a flexibly suspended diaphragm that is free to move above a fixed backplate, all fabricated on a silicon wafer. This structure forms a variable capacitor, with a fixed electrical charge applied between the diaphragm and backplate. An incoming sound pressure wave passing through holes in the backplate causes the diaphragm to move in proportion to the amplitude of the compression and rarefaction waves. This movement varies the distance between the diaphragm and the backplate, which

in turn varies the capacitance, as shown in Figure 1. Given a constant charge, this capacitance change is converted into an electrical signal.

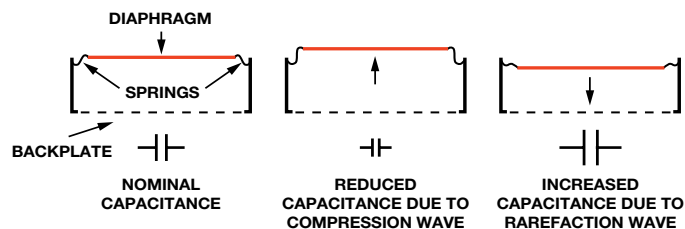


Figure 1. Capacitance of MEMS microphone varies with amplitude of acoustic wave.

The microphone sensor element is constructed on a silicon wafer using similar manufacturing processes to other integrated circuits (ICs). Unlike ECM manufacturing technologies, silicon manufacturing processes are very precise and highly repeatable. Each MEMS microphone element fabricated on a wafer will perform like every other element on that wafer—and like every element on different wafers produced across the many years of the product's lifetime.

Silicon fabrication uses a series of deposition and etching processes in a tightly controlled environment to create the collection of shapes in metal and polysilicon that form a MEMS microphone. The geometries involved in the construction of MEMS microphones are on the order of microns ( $\mu\text{m}$ ). The holes in the backplate through which sound waves pass can be less than  $10\ \mu\text{m}$  in diameter and the diaphragm thickness can be on the order of  $1\ \mu\text{m}$ . The gap between the diaphragm and the backplate is on the order of several microns. Figure 2 shows a SEM image of a typical MEMS microphone transducer element, looking at it from the top (diaphragm) side; Figure 3 shows the cross section through the middle of this microphone element. In this design, sound waves enter the microphone through the cavity in the bottom of the element and pass through the backplate holes to excite the diaphragm.

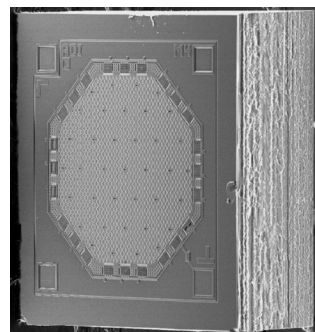


Figure 2. SEM image of MEMS microphone.

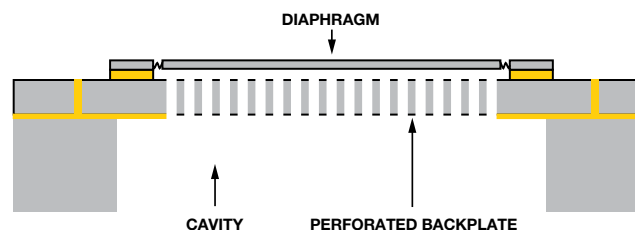


Figure 3. Cross section of a MEMS microphone.

Because the geometries are tightly controlled during the manufacturing process, the measured performance from microphone to microphone is highly repeatable. Another advantage of using MEMS technology to build microphones is that the diaphragm is extremely small, resulting in very low mass and making a MEMS microphone much less susceptible to vibration than an ECM, which has a much more massive diaphragm.

### Evolution, Repeatability, and Stability

MEMS microphones have developed to the point where they are now the default choice for many audio capture applications that require small size and high performance, but most commercial grade microphones are unsuitable for the hearing aid industry, which requires significantly smaller parts with lower power consumption; better noise performance; and improved reliability, environmental stability, and device-to-device repeatability. MEMS microphones technology is now at the stage where all of these can be offered: ultrasmall packages, very low power consumption, and very low equivalent input noise.

Tight controls in the silicon manufacturing process make the stability and device-to-device performance variation of MEMS microphones significantly better than that of ECMs. Figure 4 shows the normalized frequency response of several MEMS microphones of the same model; Figure 5 shows the normalized frequency response of various ECMs. The frequency response of each MEMS microphone is nearly identical, while that of the ECMs shows significant device-to-device variation, especially at high and low frequencies.

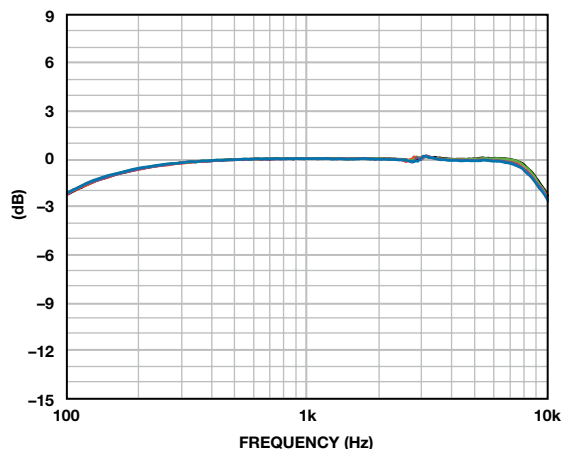


Figure 4. Frequency response of several MEMS microphones.

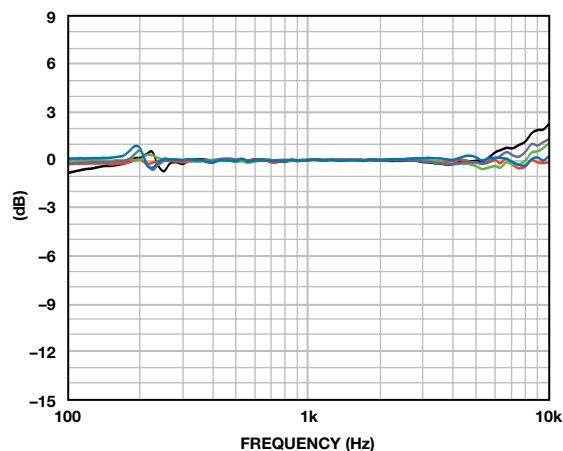
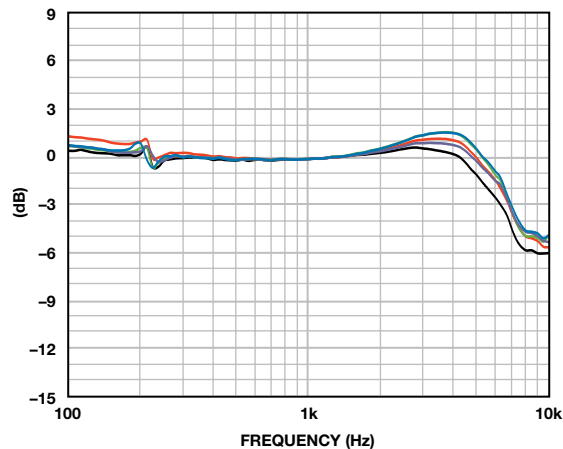
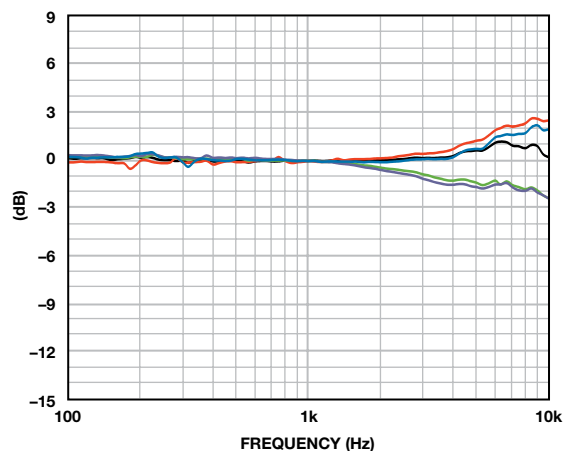


Figure 5. Frequency response of three sets of ECM microphones.

MEMS microphones also exhibit excellent stability across a wide temperature range. Figure 6 shows the change in sensitivity as the ambient temperature is varied between  $-40^{\circ}\text{C}$  and  $+85^{\circ}\text{C}$ . The black line shows less than 0.5-dB variation over the temperature range for the MEMS microphone, while the ECMs show up to 8-dB variation over temperature.

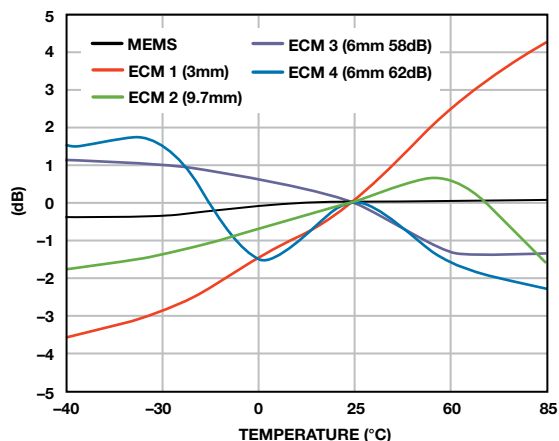


Figure 6. Sensitivity to vibration vs. temperature: MEMS vs. ECMs.

MEMS microphone designs also have significantly improved power supply rejection compared to ECMs, with a typical power supply rejection ratio (PSRR) of better than  $-50$  dB. The output signal and the bias voltage (power) share a common pin on an ECM, so any ripple on the power supply appears directly on the output signal. The exceptional PSRR of MEMS microphones allows freedom in the audio circuit design that is not possible with ECMs. This can result in reduced component count and system cost.

In tiny, battery-powered applications like hearing aids, every microwatt of power is critical. Microphones cannot be power cycled to save power when the hearing aid is operating, so the microphone's active power consumption is of critical importance. Typical ECM microphones used in hearing aids can draw  $35\ \mu\text{A}$  when powered at typical Zn-air battery voltages ( $0.9\text{ V}$ – $1.4\text{ V}$ ). The current draw of MEMS microphones used in hearing aids can be less than half of that at the same voltages, enabling hearing aids to go longer between battery changes.

The latest generation of MEMS microphones has the excellent noise and power performance required by the hearing aid industry. Analog Devices has leveraged more than 20 years of experience in MEMS technology to build high-performance microphones that can be used in the hearing aid market. Typical omnidirectional MEMS microphones specify an equivalent input noise (EIN) of 27.5 dB SPL (A-weighted, 8 kHz bandwidth), which makes them suitable for hearing aid applications. The  $\frac{1}{3}$ -octave EIN noise performance, typically used for specifying hearing aid microphones, is exceptionally good at low frequencies, as shown in Figure 7. This level of noise performance is achieved with only  $17\ \mu\text{A}$  current draw at typical hearing aid battery voltages. The microphones are available in tiny packages with less than  $7.5\ \text{mm}^3$  total volume, as shown in Figure 8.

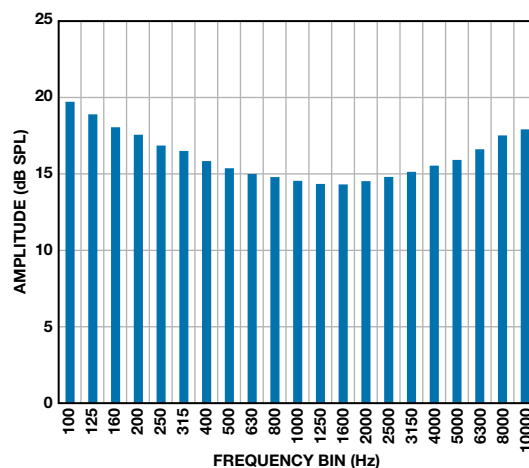


Figure 7. MEMS microphone  $\frac{1}{3}$ -octave noise.

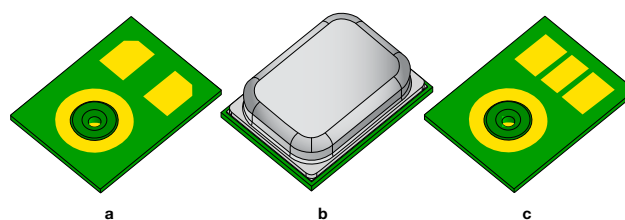


Figure 8. Omnidirectional MEMS microphones for hearing aids. a) bottom view. b) top view. c) bottom view of package that facilitates hand soldering.

## Conclusion

New high-performance, low-power MEMS microphones demonstrate that they will be the next generation of microphone technology for hearing aids. MEMS microphones can compete in performance with many hearing aid ECMs and can surpass ECM technology in many areas, such as repeatability, stability, size, manufacturability, and power consumption. MEMS microphones are the future for hearing aids, and that future is here now.

## Authors

**Jerad Lewis** [[jlewis@invensense.com](mailto:jlewis@invensense.com)] is a MEMS microphone applications engineer at InvenSense, Inc. He received his BSEE from Penn State University in 2001, and is currently pursuing an MEng degree in acoustics. Prior to transferring to InvenSense, Jerad worked at ADI, supporting various audio ICs, including SigmaDSP<sup>®</sup> converters, and MEMS microphones.



**Dr. Brian Moss** is an applications engineer at InvenSense. He received his BEng (Hons) degree from Middlesex University, London in 1996, and was awarded a PhD in 2011 following research entitled, *Constrained Gas Flow Temperature Measurement Using Passive Acoustics*. Prior to transferring to InvenSense, Brian worked at ADI and was a pro-rata lecturer with the University of Limerick.



# High-Performance Data-Acquisition System Enhances Images for Digital X-Ray and MRI

By Maithil Pachchigar

## Introduction

Digital X-ray (DXR), magnetic resonance imaging (MRI), and other medical devices require small, high-performance, low-power data-acquisition systems to meet the demands of doctors, patients, and manufacturers in a competitive marketplace. This article showcases a high-precision, low-power signal chain that solves the challenges of multichannel applications—such as digital X-ray—that multiplex large and small signal measurements from multiple channels, as well as oversampled applications—such as MRI—that require low noise, high dynamic range, and wide bandwidth. The combination of high throughput rate, low noise, high linearity, low power dissipation, and small size makes the AD7960 18-bit, 5-MSPS PulSAR® differential ADC ideal for these high-performance imaging applications as well as other precision data-acquisition systems.

## Digital X-Ray

When X-rays were first discovered in 1895, they were detected using film or scintillation screens. Since their discovery, X-ray technology has been used for medical diagnostics in fields including oncology, dentistry, and veterinary medicine, as well as in a host of other industrial imaging applications. Digital X-ray replaces film detectors with solid-state sensors, including flat-panel and line-scan detectors. Flat panel detectors use two technologies: direct conversion and indirect conversion. With direct conversion, a selenium array forms capacitive elements that directly convert the high-frequency X-ray photons into an electronic current. With indirect conversion, a cesium iodide scintillator first converts the X-ray photons into visible light, and a silicon photodiode array then converts the visible light into an electronic current. Each photodiode represents a pixel. A low-noise analog front end transforms the small current from each pixel into a large voltage, which is then converted into digital data that can be processed by the image processors. A typical DXR system, shown in Figure 1, multiplexes many channels at high sampling rates into a single ADC without sacrificing accuracy.

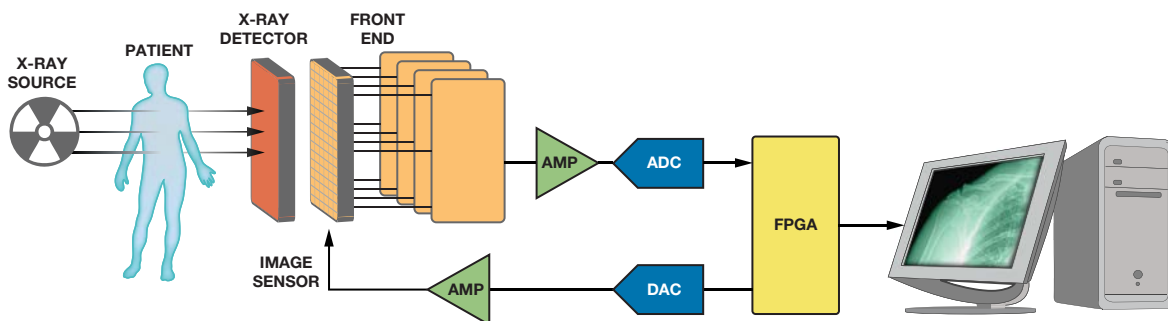


Figure 1. Digital X-ray signal chain.

Today, manufacturers of digital X-ray detectors typically use indirect conversion. Amorphous silicon flat-panel detectors or photodiode arrays with more than one million pixels capture the photon energy, multiplexing the outputs into one or two dozen ADCs. This technology offers effective X-ray photon absorption and a high signal-to-noise ratio to obtain dynamic high-resolution images in real time with a 50% lower X-ray dose. The sampling rate of each pixel is low, from a few hertz for bones and teeth, to a maximum of 120 Hz for capturing images of a baby's heart, which is the fastest organ in the body.

The performance of a digital radiography detector is measured by its image quality, so accurate acquisition and precise processing of the X-ray beam is essential. Digital radiography's increased dynamic range, fast acquisition speed and frame rate, and uniformity using special image processing techniques allows it to display an enhanced image.

Medical imaging systems must provide enhanced images for accurate diagnoses and shorter scanning times for decreased patient exposure to X-ray dosages. High-end radiography systems (dynamic acquisition) are typically used in surgical centers and operating rooms, whereas basic systems are used for emergencies, in small hospitals, or in doctors' offices. Industrial imaging systems must be rugged, as they have long lifetimes and are subject to high radiation dosages in harsh environments. Security or baggage inspection applications can use low X-ray dosages, as the X-ray source remains on for long periods of time.

## MRI Gradient Control

MRI systems, shown in Figure 2, are best suited for brain imaging, or for orthopedic, angiographic, and vascular studies, as the scan provides high contrast on soft tissue without exposing it to ionizing radiation. MRI operates in the 1-MHz to 100-MHz RF frequency band, whereas computed tomography (CT) and DXR operate in the  $10^{16}$ -Hz to  $10^{18}$ -Hz frequency range, subjecting patients to ionizing radiation that can damage living tissue.

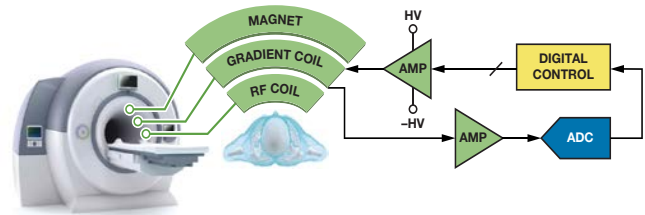


Figure 2. MRI system.

Control systems for MRI specify tight tolerances, thus requiring high-performance components. In MRI systems, a large coil is used to create the main magnetic field of 1.5 T to 3 T. A high voltage—up to 1000 V—is applied to the coil to develop the required current of up to 1000 A. MRI systems use gradient control to linearly vary the main magnetic field by changing the current in special coils. These gradient coils are modulated rapidly and precisely, altering the main magnetic field to target very small locations within the body. The gradient control energizes a thin cross section of the body tissue using RF energy to generate the x-, y-, and z-axis images. MRI demands fast response time, with its gradient precisely controlled to within 1 mA (1 ppm). MRI system manufacturers can control the gradient in either analog or

digital domains. The design of MRI systems involves significant development time, a huge bill-of-material cost, and large risks associated with its overall hardware and software complexity.

### High-Performance Data-Acquisition Signal Chain

Figure 3 shows a high-precision, low-noise, 18-bit data-acquisition signal chain that features  $\pm 0.8$ -LSB integral nonlinearity (INL),  $\pm 0.5$ -LSB differential nonlinearity (DNL), and 99-dB signal-to-noise ratio (SNR). Figure 4 shows its typical FFT and linearity performance using a 5-V reference. The total power consumption of the signal chain is about 345 mW, about 50% lower than competitive solutions.

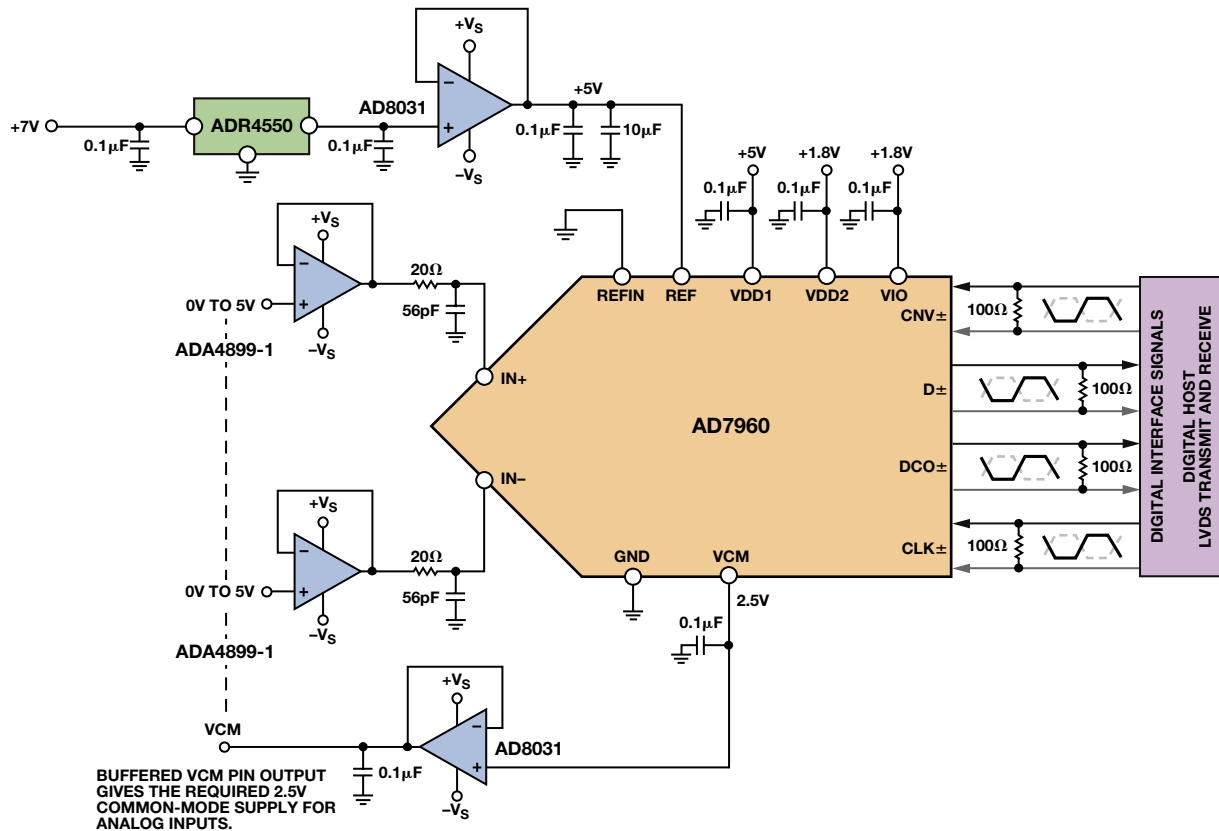


Figure 3. Precision, fast-settling signal chain using AD7960, ADA4899, AD8031, and ADR4550.

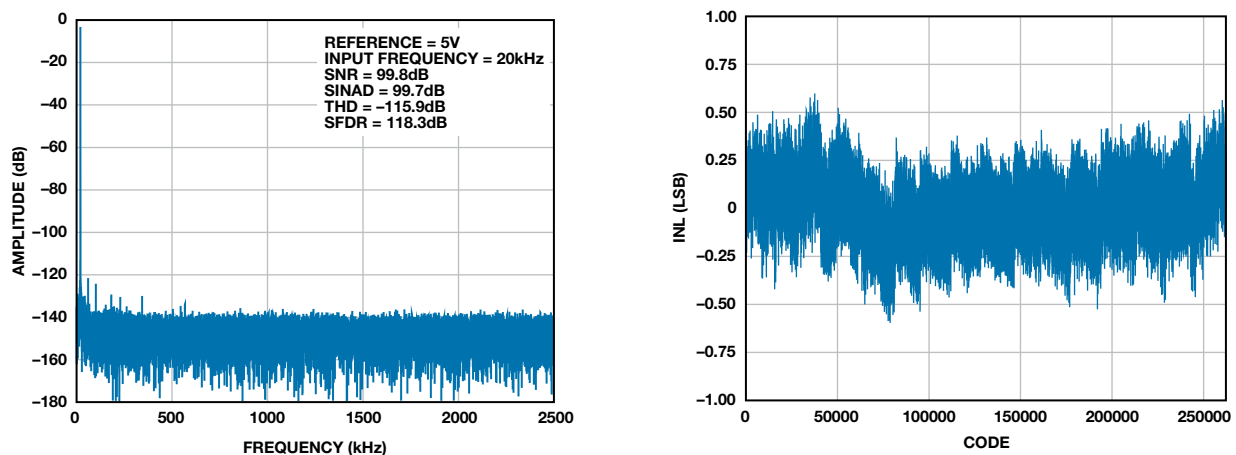


Figure 4. AD7960 typical FFT and linearity performance.

This type of high-speed, multichannel, data-acquisition system could be used in CT, DXR, and other medical imaging applications that require higher sampling rates without sacrificing accuracy. Its 18-bit linearity and low noise provide enhanced image quality, and its 5-MSPS throughput allows a shorter scanning period (more frames per second) and decreased exposure to the X-ray dosage for accurate physician diagnostics and a better patient experience. Multiplexing multiple channels creates higher-resolution images for full analysis of organs such as the heart, and achieves affordable diagnosis while minimizing power dissipation. Accuracy, cost, power dissipation, size, complexity, and reliability are of paramount importance for medical equipment manufacturers.

In CT scanners, the pixel current is captured continuously using one track-and-hold per channel, with outputs multiplexed to a high-speed ADC. A high throughput rate allows many pixels to be multiplexed to a single ADC, saving cost, space, and power. Low noise and good linearity provide a high-quality image. High-resolution infrared cameras could benefit from this solution.

Oversampling is the process of sampling the input signal at a much higher rate than the Nyquist frequency. Oversampling is used for spectroscopy, MRI, gas chromatography, blood analysis, and other medical instruments that require a wide dynamic range to accurately monitor and measure both small and large signals from multiple channels. High resolution and accuracy, low noise, fast refresh rates, and very low output drift can significantly simplify the design, reducing development cost and risk for MRI systems.

One of the key requirements for MRI systems is measurement repeatability and stability over long periods of time in a hospital or doctor's office. For enhanced image quality, these systems also demand tight linearity and high dynamic range (DR) from dc to tens of kilohertz. As a guideline, oversampling the ADC by a factor of four provides one additional bit of resolution, or a 6-dB increase in DR. The DR improvement due to oversampling is  $\Delta DR = \log_2(OSR) \times 3 \text{ dB}$ . In many cases, oversampling is implemented well in  $\Sigma\text{-}\Delta$  ADCs, but these are limited when fast switching between channels and accurate dc measurements are required. Oversampling with a successive-approximation (SAR) ADC also improves antialiasing and reduces noise.

**State-of-the-Art ADC Architecture**

Precision high-speed data-acquisition systems used in CT, DXR, and other multichannel applications—or in spectroscopy, MRI,

and other oversampled applications—require a state-of-the-art ADC. The AD7960 18-bit, 5-MSPS PulsAR differential ADC, shown in Figure 5, uses a capacitive digital-to-analog converter (CAPDAC) to provide unprecedented noise and linearity without latency or pipeline delay. It provides the wide bandwidth, high accuracy (100 dB DR), and fast sampling (200 ns) required for medical imaging applications, and significantly reduces power dissipation and cost in multichannel applications. Available in a small (5 mm × 5 mm), easy-to-use 32-lead LFCSP package, it is specified over the -40°C to +85°C industrial temperature range. The 16-bit AD7961 is pin-compatible with the AD7960, and can be used when 16-bit performance is sufficient.

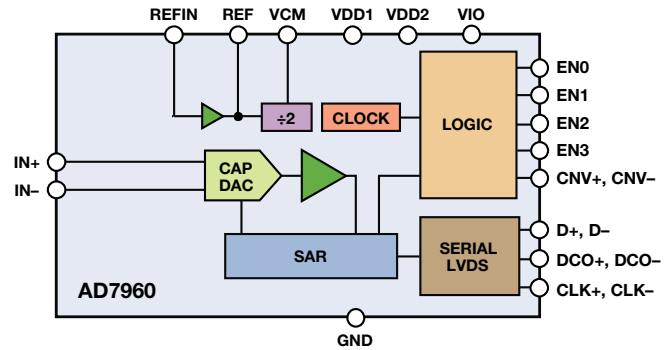


Figure 5. AD7960 functional block diagram.

The capacitive DAC, shown in Figure 6, consists of a differential 18-bit binary weighted capacitor array—which is also used as the sampling capacitor that acquires the analog input signal—a comparator, and control logic. When the acquisition phase is complete, the conversion control input (CNV±) goes high, the differential voltage between inputs IN+ and IN- is captured, and the conversion phase begins. Each element of the capacitor array is successively switched between GND and REF, charge is redistributed, the input is compared to the DAC value, and the bit is kept or dropped depending upon the result. The control logic generates the ADC output code at the completion of this process. The AD7960 returns to acquisition mode about 100 ns after the start of conversion. The acquisition time is approximately 50% of the total cycle time, making the AD7960 easy to drive and relaxing the required settling time of the ADC driver.

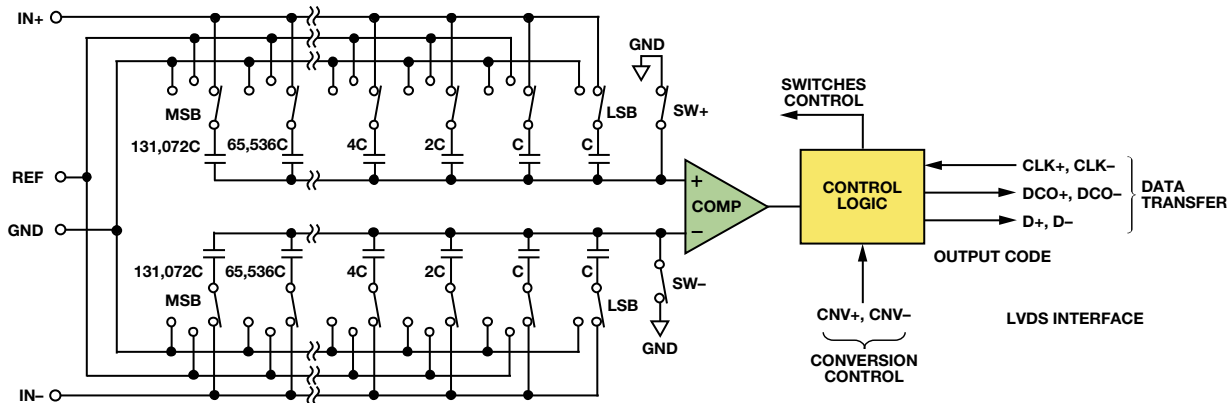


Figure 6. AD7960 simplified internal schematic.



The AD7960 series operates from 1.8-V and 5-V supplies, dissipating only 39 mW at 5 MSPS when converting in self-clocked mode. The power dissipation scales linearly with sample rate, as shown in Figure 7.

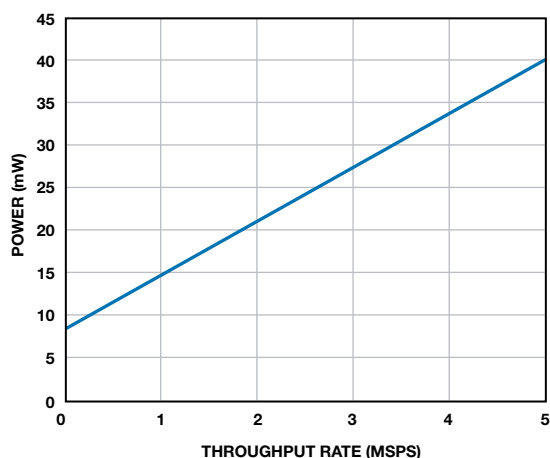


Figure 7. AD7960 power consumption vs. throughput rate.

The power dissipation at very slow sample rates is dominated by the LVDS static power. The AD7960 is twice as fast, dissipates 70% less power, and occupies a 50% smaller footprint than the industry's next fastest 18-bit SAR ADC.

The AD7960 allows three external reference options: 2.048 V, 4.096 V, and 5 V. An on-chip buffer doubles the 2.048-V reference voltage, so the conversions are referred to 4.096 V or 5 V.

The digital interface uses low-voltage differential signaling (LVDS), offering self-clocked and echoed-clock modes to enable high-speed data transfer (up to 300 MHz) between the ADC and the host processor. The LVDS interface reduces the number of digital signals and eases signal routing, as multiple devices can

share a common clock. This also reduces power dissipation, which is especially useful in multiplexed applications. The self-clocked mode simplifies the interface with the host processor, allowing simple timing with a header that synchronizes the data from each conversion. A header is required to allow the digital host to acquire the data output because there is no clock output synchronous to the data. The echoed-clock mode provides robust timing at the expense of an extra differential pair. The AD7960 achieves over 120-dB typical dynamic range at output data rates below 20 kSPS, as shown in Figure 8.

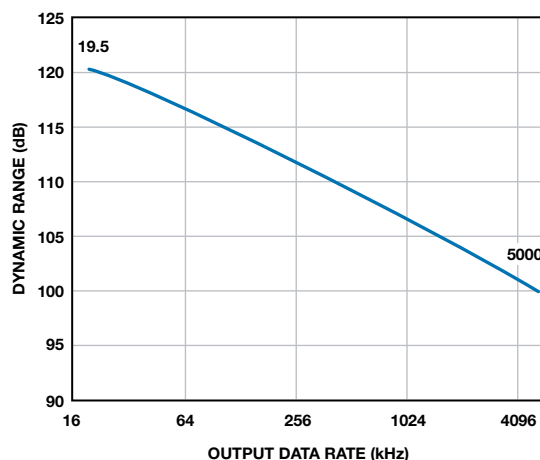


Figure 8. AD7960 dynamic range vs. output data rate.

#### ADC Driver

The acquisition time of the ADC determines the settling time requirements for the ADC driver. Table 1 shows some specifications that must be considered when selecting an ADC driver. As always, the signal chain performance should be verified on the bench to ensure that the desired performance is achievable.

Table 1. AD7960 ADC Driver Selection Benchmark

ADC Driver Specifications	General Formula	Minimum Requirements
Bandwidth ( $f_{-3dB\_amp}$ )	$\frac{N \ln 2}{\pi t_{acq}}$	40 MHz
Slew Rate	$\frac{\text{Single-ended input voltage}}{0.5 t_{acq}}$	100 V/ $\mu$ s
Settling Time	From data sheet	100 ns
SNR	$10 \log \left( \frac{V_{rms\_in}^2}{\sqrt{(2(e_{n\_amp}))^2 \times f_{-3dB\_ADC} \times \frac{\pi}{2})^2}} \right)$	105.5 dB

Notes:  $N = 18$ ,  $t_{acq} = 100$  ns,  $V_{rms\_in}^2 = 5^2/2 = 12.5$  V<sup>2</sup>,  $e_{n\_amp} = 2$  nV/ $\sqrt$ Hz,  $f_{-3dB\_ADC} = 28$  MHz.

The op amp's data sheet usually provides the settling time specification as a combination of the time for linear settling and slewing; the formulas given are first-order approximations assuming 50% for linear settling and 50% for slewing (multiplexed application) using a 5-V single-ended input.

The [ADA4899-1](#) rail-to-rail amplifier features 600-MHz bandwidth, -117-dBc distortion @ 1 MHz, and 1-nV/ $\sqrt{\text{Hz}}$  noise, as shown in Figure 9. It settles to 0.1% within 50 ns when configured as a unity-gain buffer driving the inputs of the AD7960 with a 5-V differential signal.

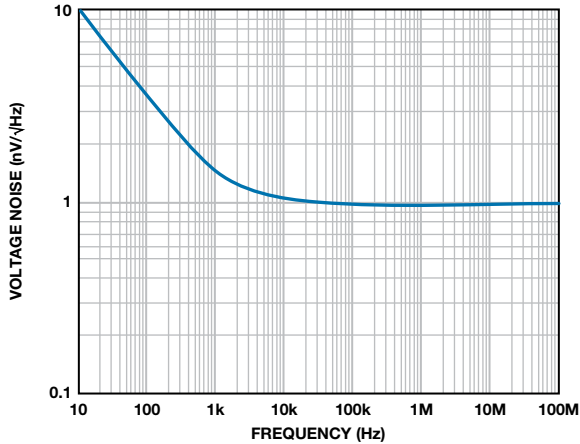


Figure 9. ADA4899 noise spectral density.

#### Reference and Buffers

The low-noise, low-power [AD8031](#) rail-to-rail amplifier buffers the 5-V output from the [ADR4550](#) voltage reference, which

features high precision ( $\pm 0.02\%$  max initial error), low drift (2 ppm/ $^{\circ}\text{C}$  max), low noise (1  $\mu\text{V}$  p-p), and low power (950  $\mu\text{A}$  max). A second AD8031 buffers the ADC's 2.5-V common-mode output voltage. Its low output impedance maintains a stable reference voltage independent of the ADC input voltage to minimize INL. Stable for large capacitive loads, the AD8031 can drive the decoupling capacitors required to minimize spikes caused by transient currents. It is ideal for a wide range of applications, from wideband battery-operated systems to high-speed, high-density systems that demand low power dissipation.

#### Conclusion

A high-precision, low-power signal chain using ADI's proprietary technology offers unprecedented speed, noise, and linearity, solving the difficult challenges of high-performance multiplexed and oversampled data-acquisition systems used for DXR and MRI gradient control. The high-performance signal chain components are available in small footprint packages, saving space and reducing cost in multichannel applications.

#### Author

**Maithil Pachchigar** [[maithil.pachchigar@analog.com](mailto:maithil.pachchigar@analog.com)]



is an applications engineer in ADI's Precision Converters business unit in Wilmington, MA. He joined ADI in 2010 and supports the precision ADC product portfolio and customers in the industrial, instrumentation, medical, and energy segments. Having worked in the semiconductor industry since 2005, Maithil has published several technical articles. He received an MSEE from San Jose State University in 2006 and an MBA from Silicon Valley University in 2010.



# Some Tips on Making a FETching Discrete Amplifier

By George Alexandrov and Nathan Carter

## Introduction

Low-noise amplifiers for photodiode, piezoelectric, and other instrumentation applications typically call for circuit parameters such as extremely high input impedance, low 1/f noise, or sub-picoamp bias currents that cannot be met with available integrated products. This article discusses the requirements and challenges of designing a low-noise amplifier using discrete components, with particular emphasis on input-referred noise and offset voltage trimming.

## Limitations of High Input Gain Topologies

A typical discrete amplifier, shown in Figure 1, uses a high-speed op amp preceded by a differential amplifier stage implemented with dual matched JFETs, which provide high input impedance and some initial gain. The system noise is dominated by the input stage, so a low-noise op amp is not required.

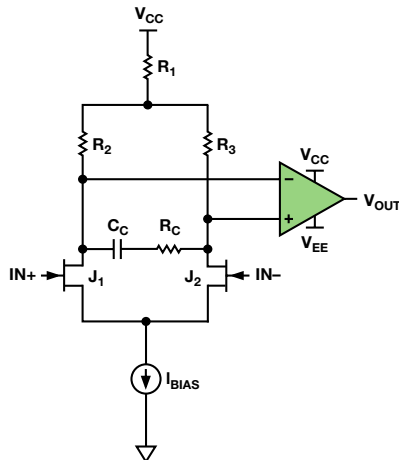


Figure 1. High-speed, low-noise instrumentation amplifier.

Unfortunately, stabilizing the output at low gains and high frequencies is a challenge. Stability is achieved by adding an RC compensation network,  $C_C$  and  $R_C$ , but the optimum values for these components change with gain, complicating the overall design. Also, the large signal response can be too slow for some applications.

The circuit shown in Figure 2 can achieve comparable noise at unity gain, without the need for compensation. The speed is primarily determined by the operational amplifier. The circuit consists of three main parts: the output op amp, the FET input buffers, and the current sources that bias the FETs.

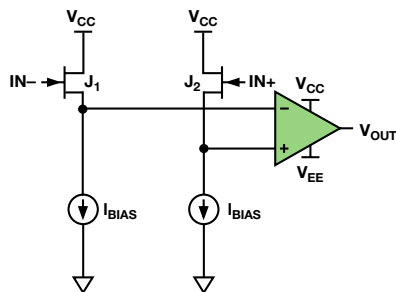


Figure 2. Unity-gain stable version of amplifier.

The unity-gain configuration of the input stage places a tight constraint on the op amp's noise performance. In the circuit shown in Figure 1, the input FETs have finite gain, which reduces the noise impact of the following stage. In the unity-gain configuration, the total noise is split between the input buffers and the op amp, thus requiring a low-noise op amp.

## Input Stage Current Sources

The current sources used to bias the FET input buffer can have a dramatic impact on the overall system noise if not implemented correctly. One way to minimize the bias noise contribution is to add degeneration resistors to a simple current mirror, as shown in Figure 3.

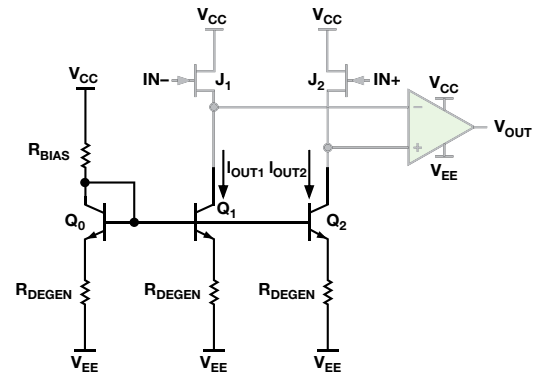


Figure 3. Current mirror with degeneration.

The current flowing in transistor  $Q_0$  is mirrored in transistors  $Q_1$  and  $Q_2$ . The noise sources include the 1/f and shot noise of the transistors. Adding the degeneration resistors decreases the shot noise by a factor of  $1 + g_m R_{DEGEN}$ , but has no effect on the 1/f noise. This noise source, modeled as a current between base and emitter, is not improved by adding  $R_{DEGEN}$ . A different current source architecture is needed to reduce both noise sources simultaneously.

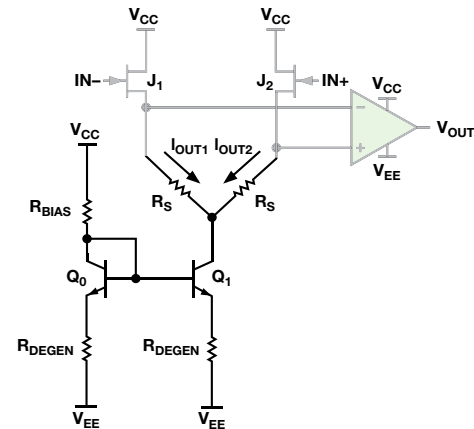


Figure 4. Current mirror with current splitting resistors.

A modified current mirror is shown in Figure 4. This current source requires fewer transistors, allowing the use of a dual transistor pair instead of a quad package, and reduces both size and cost. The noise performance is vastly improved, as both shot noise and 1/f noise are canceled out. The current from transistor  $Q_0$  is mirrored to transistor  $Q_1$ . This current is split at the collector using a pair of resistors, so the 1/f and shot noise will split evenly. Because the noise sources come from the same transistor, they are coherent. The output is differential, so the noise cancels out, as shown in Figure 5.

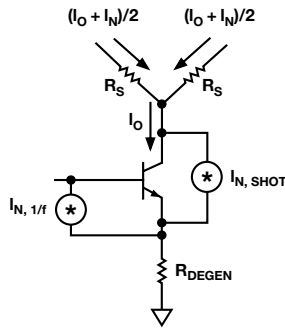


Figure 5. Ideal representation of current source showing noise cancellation.

The current mirror transistors are still degenerated to improve current matching and output impedance. The current is determined by the voltage drop across  $R_{DEGEN}$ , so transistor matching is not as important as in the undegenerated case. This allows the use of almost any matched pair, but the collector capacitance must be low to maintain stability. The differential input capacitance of the two implementations remains unchanged because the coupling between the sources of the two input devices is dominated by the low differential input impedance of the amplifier.

For the purposes of testing, the voltage reference that determines the bias current was set by a resistor connected to  $V_{CC}$ . This leaves the circuit prone to performance issues if  $V_{CC}$  changes. In a real implementation, a Zener, band gap, or [IC voltage reference](#) should be used instead of a resistor.

### Op Amp

The op amp determines the speed, noise, output performance, and distortion of the overall amplifier, so it must be selected based on the application. Table 1 shows some typical values for suitable op amps.

Table 1. Relevant Op Amp Characteristics

	Wideband Noise (nV/ $\sqrt{\text{Hz}}$ )	Supply Current (mA per amplifier)	3-dB Bandwidth (MHz @ G = 1)	Supply Voltage (V)
ADA4897	1.0	3	230	$\pm 1.5$ to $\pm 5$
ADA4898	0.9	8	65	$\pm 5$ to $\pm 18$

The [ADA4897](#) is a good candidate for the low-noise performance necessitated by most high-speed sensing applications. For high-voltage applications, the [ADA4898](#) also performs well. Able to operate with  $\pm 18$ -V supplies, it maintains low noise while consuming only 8 mA of supply current. Both amplifiers result in a composite design with over 50 V/ $\mu\text{s}$  of slew rate.

### Input FETs

The input FETs determine the input characteristics of the amplifier. The best performance requires FETs that have good matching, low noise, and low input bias current. Most importantly, these JFETs determine the input offset voltage, so they must be very well matched. In the case of the LSK389, the maximum  $\Delta V_{GS}$  is 20 mV, corresponding to a  $V_{OS}$  of 20 mV. A technique for reducing this relatively high offset voltage will be discussed later.

Table 2. Relevant JFET Characteristics

	Wideband Noise (nV/ $\sqrt{\text{Hz}}$ @ $f = 1$ kHz)	Differential Gate-to-Source Cutoff Voltage (mV max)	Gate-to-Source Saturation Current Ratio (min)	Gate Current (pA)
LSK389A	0.9 ( $I_D = 2$ mA)	20	0.90	N/A
LSK489	1.8 ( $I_D = 2$ mA)	20	0.90	-2 to -25
2N5564	2.0 ( $I_D = 1$ mA)	5	0.95	-3
2SJ109	1.1 ( $I_D = 3$ mA)	20	0.90	N/A

### Amplifier Performance

The following example uses an amplifier implemented with [LSK389A](#) nJFETs, [PMP4201](#) transistors, and an [ADA4897](#) op amp. The evaluation board is shown in Figure 6.



Figure 6. Evaluation board for amplifier including digital potentiometer connection.

The most glaring error source of this amplifier implementation is the high input offset voltage. Largely determined by the input FET mismatch, this offset voltage can be as high as 10 mV. (The LSK389 data sheet claims mismatch as high as 20 mV, but figures this high were never seen during testing.) A gain of 100 creates a 1-V output offset, making the amplifier virtually useless. Before this amplifier can be used as a preamp, the high input offset voltage needs to be trimmed. This is done with an [AD5292](#) digital potentiometer. Two ways to perform the offset trim based on the placement of the potentiometer are discussed here.

### Input Offset Voltage

The input offset voltage for tested versions of the amplifier varied from 1 mV to 10 mV. The main cause of this offset is the mismatch of the input JFETs. The LSK389 data sheet shows that  $I_{DSS}$  can vary by as much as 10%, affecting the  $V_{GS}$  of the devices and introducing an offset voltage. Fortunately, the offset stems from unequal bias currents through the JFETs, so the current sources that supply these currents can be adjusted to compensate for this error. One method of achieving zero offset voltage is shown in Figure 7.

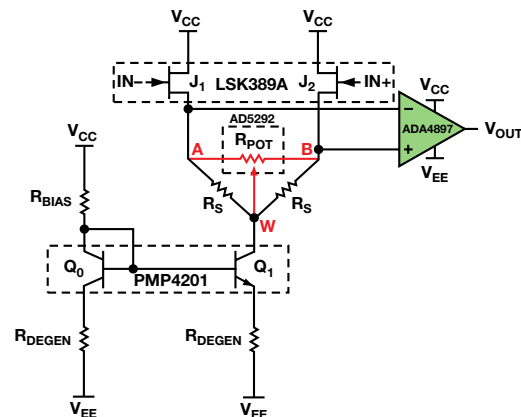


Figure 7. Using a potentiometer to cancel input offset voltage.

A digital potentiometer such as the [AD5141](#) or [AD5292](#) can be used to adjust the current through the input devices. Table 3 shows key characteristics for these devices, which consist of a three-terminal potentiometer controlled through an SPI interface to accurately position the wiper for precise resistance control.

**Table 3. Digital Potentiometer Specifications**

	Supply Voltage (V)	Nominal Resistance (kΩ)	Resistor Tolerance (%)	Resolution (bits)	Operating Temperature (°C)
AD5141	±2.5	10, 100	8	8	-40 to +125
AD5292	±16	20, 50, 100	1	10	-40 to +105

Unfortunately these digital potentiometers have high parasitic capacitances at their terminals (up to 85 pF), which cause stability issues and ringing at high frequencies. Figure 8 shows the step response of the amplifier with and without this potentiometer.

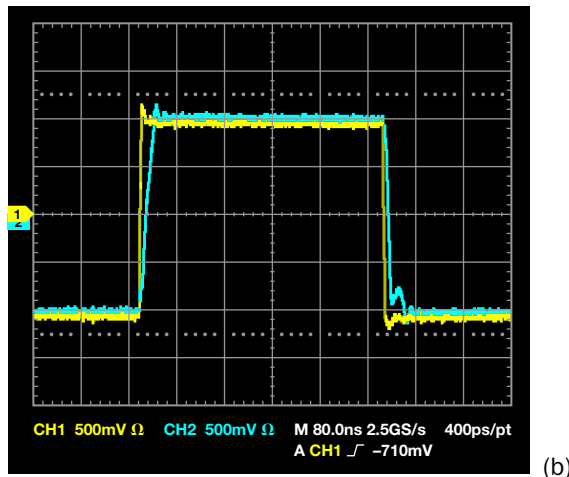
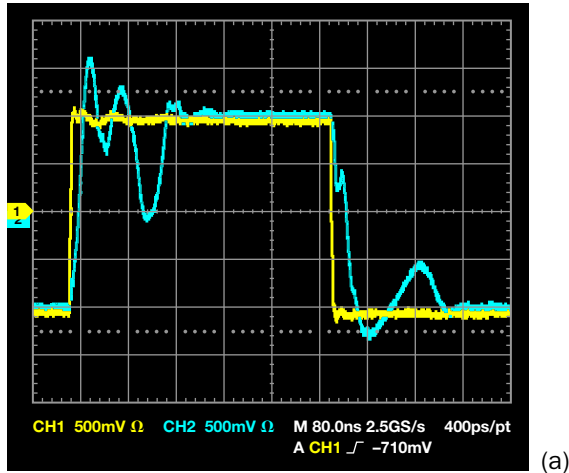


Figure 8. Step response of amplifier a) with and b) without potentiometer for offset trimming.

The 85 pF of parasitic capacitance is connected between the source of the input FETs and ground, causing significant ringing and instability at high frequencies. An alternative biasing setup that reduces input offset voltage while maintaining low noise and stability at high frequencies is shown in Figure 9.

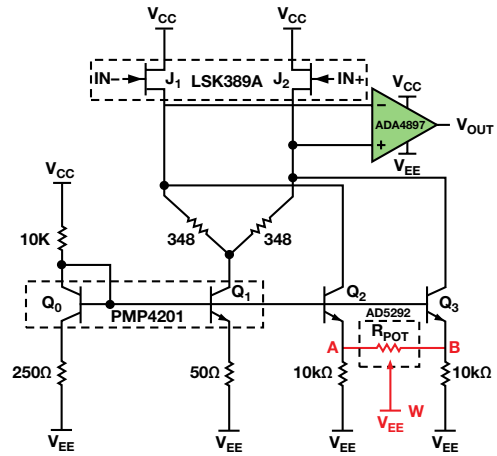


Figure 9. Alternate method for using potentiometer to cancel input offset voltage.

In both of the above biasing methods, the digital potentiometer is used to adjust the current through each FET until their gate-to-source voltages are matched and the input offset voltage is minimized. However, the biasing scheme of Figure 9 ensures that the high parasitic capacitance of the potentiometer does not cause high-frequency instability and ringing. It works by combining the two different current mirror configurations of Figure 3 and Figure 4. The  $Q_0/Q_1$  current mirror provides the majority of the current to the FETs by splitting its collector current, introducing almost no noise from the biasing transistors.  $Q_0/Q_2/Q_3$  form a more traditional, yet noisier, current mirror. These are degenerated so that they only source 1% to 2% of the total FET bias current (about 30  $\mu$ A). This is not enough to introduce significant noise, but allows enough adjustment to easily trim a 10-mV offset. More importantly, it ensures that the parasitic capacitance of the potentiometer does not affect the output. Thus, the noise remains low thanks to the  $R_S$  splitters, the offset can be trimmed reliably based on the degeneration of  $Q_2/Q_3$ , and any potentiometer parasitics have no effect on the output. Figure 10 shows the step response for the mirror trimmed version.

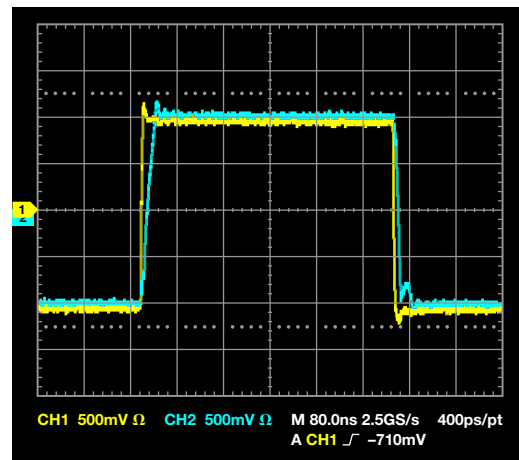


Figure 10. Step response for amplifier trimmed at current mirror.

Digital potentiometers provide an easy way to trim the offset voltage, allowing for a wide range of operating temperatures and voltages under which the offset can be minimized. The AD5292 includes a 20-times programmable memory that allows the wiper position to be stored permanently after adjusting the offset voltage. This circuit implementation used an AD5292 evaluation board to connect the offset trimming potentiometer off-board. For more compact designs, the digital potentiometer could be included on board and programmed using its on-chip serial interface pins.

Using this method, the input offset voltage was successfully reduced to a few microvolts for the LSK389/ADA4897 amplifier using an AD5292 20 kΩ potentiometer.

### Offset Drift

The offset voltage temperature coefficient, or the rate at which the input offset voltage increases with increasing temperature, is about 4 μV/°C for the untrimmed amplifier. The addition of the AD5292 increases this to about 25 μV/°C. These results are shown in Figure 11.

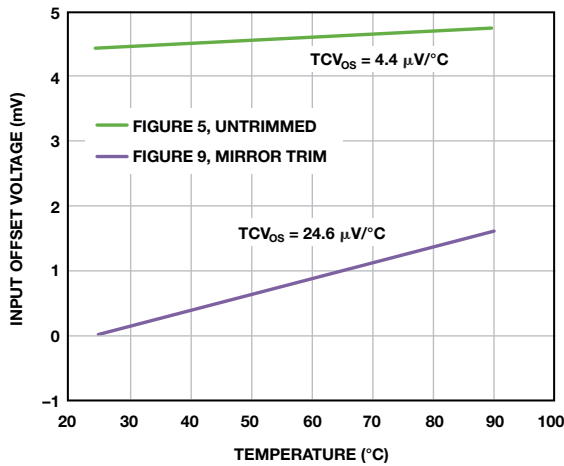


Figure 11. Input offset voltage as a function of temperature.

Despite the large change in drift, the dynamic range of the amplifier is improved considerably. Consider an untrimmed amplifier with 5 mV of offset at a gain of 100 and temperature of 85°C. This creates an output offset of

$$V_{OUT} = (V_{OS} + TCV_{OS} \times T) \times G = (5 \text{ mV} + 4 \text{ } \mu\text{V}/^\circ\text{C} \times 85^\circ\text{C}) \times 100 = 534 \text{ mV}.$$

If the offset was trimmed to 5 μV at the same operating conditions, the output offset would be

$$V_{OUT} = (V_{OS} + TCV_{OS} \times T) \times G = (5 \text{ } \mu\text{V} + 25 \text{ } \mu\text{V}/^\circ\text{C} \times 85^\circ\text{C}) \times 100 = 213 \text{ mV},$$

thus improving dynamic range by more than 300 mV. This also enables field calibration and system level drift calibration and trim techniques that can further improve accuracy.

### Noise

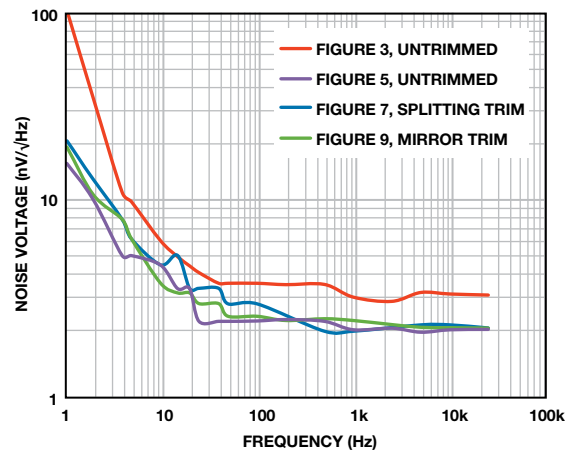


Figure 12. Input-referred noise voltage for different trims.

Figure 12 shows the noise density of various amplifier configurations. This amplifier achieves a wideband noise density of 2 nV/√Hz with an 8-mA supply current, an improvement over existing integrated products. The untrimmed 1/f noise is 4 nV/√Hz at 10 Hz, and 16 nV/√Hz at 1 Hz. Note that both the 1/f and wideband noise are 1.5 to 2 times higher for the conventional current mirror (red curve), and that the overall noise remains virtually unchanged with trimming, as shown in the three other curves.

### Small Signal Transfer Function

Figure 13 and Figure 14 show the frequency response for various gains and trim settings. Note that the R<sub>S</sub> trimmed amplifier is unstable and that the frequency response is the same between the untrimmed and mirror-trimmed versions.

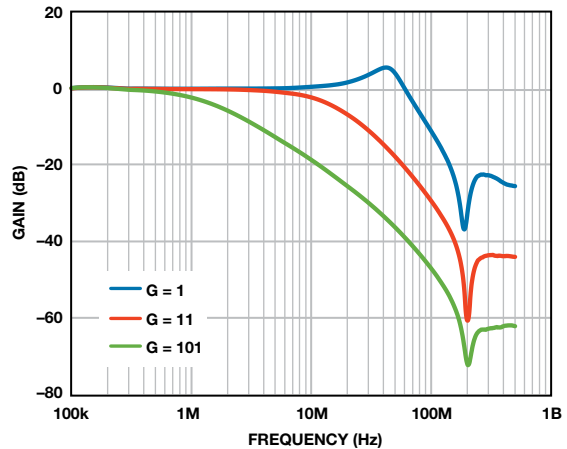


Figure 13. Bandwidth for the untrimmed version of the amplifier at various gains.

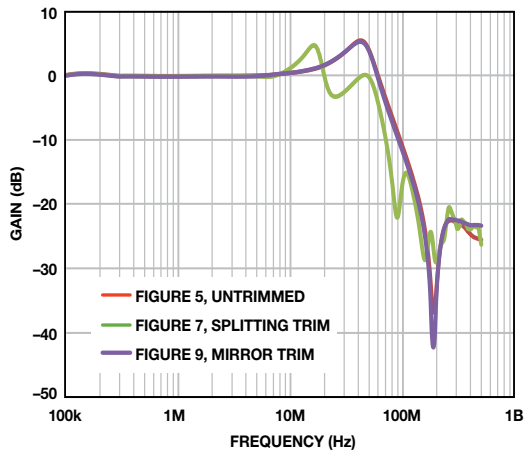


Figure 14. Unity gain bandwidth for different potentiometer placement.

### Input Bias Current

Input bias currents were measured using a gain configuration and sense resistor. Table 4 shows typical ranges for various parts, voltages, and temperatures.

Table 4. Input Bias Current Values

	ADA4897 (25°C)	ADA4897 (125°C)	ADA4898 (±5 V)	ADA4898 (±15 V)
Input Bias Current (pA)	<1	4000– 10,000	<1	15–50

### Conclusion

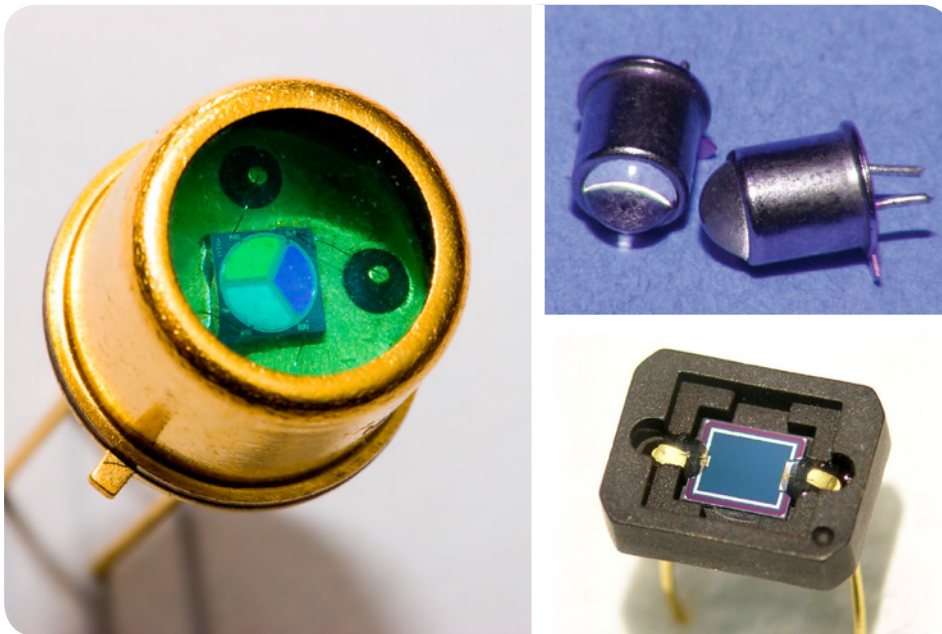
With the growing number of applications that require specialized op amps with high input impedance, low noise, and minimal offset voltage, it becomes increasingly important to be able to design an application-specific circuit using discrete parts. This article described a high-speed, low-noise amplifier with adjustable input offset voltage using only four discrete parts. The design considerations for each stage were discussed, with particular emphasis on the noise performance of the amplifier and the various ways to cancel shot and 1/f noise. Using the ADA4897 op amp and LSK389 JFETs, a unity-gain capable amplifier with 2-nV/√Hz input-referred noise and only 8 mA of supply current was designed and tested. The high input offset voltage, in the range of 10 mV, was digitally trimmed using the AD5292 digital potentiometer. Alternative parts were discussed, in order to suit different applications and environments.

### Authors

**George Alexandrov** [[george.alexandrov@analog.com](mailto:george.alexandrov@analog.com)] is a design engineer intern in the High-Speed Amplifier Group. He has a BS degree from Stanford University and is currently studying at UC Berkeley.



**Nathan Carter** [[nathan.carter@analog.com](mailto:nathan.carter@analog.com)] is a design engineer in the Linear and RF Group, where he has been working for more than 10 years. He has degrees from California Polytechnic State University and Worcester Polytechnic Institute.



**Analog Devices, Inc.**  
**Worldwide Headquarters**

Analog Devices, Inc.  
One Technology Way  
P.O. Box 9106  
Norwood, MA 02062-9106  
U.S.A.  
Tel: 781.329.4700  
(800.262.5643,  
U.S.A. only)  
Fax: 781.461.3113

**Analog Devices, Inc.**  
**Europe Headquarters**

Analog Devices, Inc.  
Wilhelm-Wagenfeld-Str. 6  
80807 Munich  
Germany  
Tel: 49.89.76903.0  
Fax: 49.89.76903.157

**Analog Devices, Inc.**  
**Japan Headquarters**

Analog Devices, KK  
New Pier Takeshiba  
South Tower Building  
1-16-1 Kaigan, Minato-ku,  
Tokyo, 105-6891  
Japan  
Tel: 813.5402.8200  
Fax: 813.5402.1064

**Analog Devices, Inc.**  
**Asia Pacific Headquarters**

Analog Devices  
5F, Sandhill Plaza  
2290 Zuchongzhi Road  
Zhangjiang Hi-Tech Park  
Pudong New District  
Shanghai, China 201203  
Tel: 86.21.2320.8000  
Fax: 86.21.2320.8222