Volume 48, Number 1, 2014

A forum for the exchange of circuits, systems, and software for real-world signal processing

# Analog Dialogue

## In This Issue




www.analog.com/analogdialogue

ANALOG DEVICES

# Editor's Notes

## IN THIS ISSUE

**Precision Resolver-to-Digital Converter Measures Angular Position and Velocity**

Resolvers use the magnetic coupling between primary and secondary windings to measure the precise angular position of a rotating element. Used in industrial motor controls, servos, robotics, power train units in hybrid- and full-electric vehicles, and many other applications, resolvers can withstand severe conditions, making them the perfect choice for military systems in harsh environments. (Page 3)

**Noise-Reduction Network for Adjustable-Output Low-Dropout Regulators**

Noise is extremely important to designers of high-performance analog circuits, especially high-speed clocks, ADCs, DACs, VCOs, and PLLs. A key to reducing noise is keeping the noise gain of the low-dropout regulator (LDO) that drives the circuit close to unity without compromising ac performance or dc gain. A simple RC network can reduce the output noise of an adjustable-output LDO. (Page 9)

**How to Stay Out of Deep Water when Designing with Bridge Sensors**

Electrical signals generated by sensors are typically small, so high gain is required. In addition, they may sit on top of large common-mode voltages or dc offsets. Precision in-amps can provide high gain, selectively amplifying the difference between the two input voltages while rejecting signals common to both inputs. This allows the signals to be digitized, stored, or used to control processes. (Page 12)

**Dual-Loop Clock Generator Cleans Jitter, Provides Multiple High-Frequency Outputs**

As the speed and resolution of data converters continues to increase, the need for higher-frequency sampling clock sources with lower phase noise is growing. The jitter presented to the clock inputs is one of the many performance bottlenecks facing designers when they create cellular base stations, military radar systems, and other designs that require high-speed, high-performance clock signals. (Page 15)

**Electromagnetic Flow Meters Achieve High Accuracy in Industrial Applications**

Industrial applications ranging from oil refineries to vending machines require precision measurements of temperature, pressure, and flow. Accurate control of flow when filling bottles in the food industry or exchanging petroleum between tanks and tankers can directly influence profits. This article presents an overview of flow-meter technologies, focusing on high-accuracy electromagnetic flow meters. (Page 19)

**A Deeper Look into Difference Amplifiers**

The classic four-resistor difference amplifier seems simple, but many circuit implementations perform poorly. Based on actual production designs, this article shows some of the pitfalls encountered with discrete resistors, filtering, ac common-mode rejection, and high noise gain. To achieve a solid, production-worthy design, carefully consider noise gain, input voltage range, impedance ratios, and offset voltage specifications. (Page 27)

*Scott Wayne* [scott.wayne@analog.com]

## PRODUCT INTRODUCTIONS: VOLUME 48, NUMBER 1

*Data sheets for all ADI products can be found by entering the part number in the search box at www.analog.com.*

### January

**Amplifier**, operational, quad, low-noise, RRIO ..... **ADA4084-4**
**Amplifiers**, current-sense, bidirectional, zero-drift ..... **AD8417/AD8418A**

### February

**ADC**, dual, 16-bit, 1-MSPS, successive-approximation ..... **AD7903**
**ADC**, quad, 16-bit, 125-MSPS, pipelined, JESD204B ..... **AD9656**
**DAC**, dual, 16-bit, 1600-MSPS, TxDAC+® ..... **AD9142A**
**Demodulator**, quadrature, 695-MHz to 2700-MHz, PLL, VCO ..... **ADRF6820**
**Isolator**, I²C, 2-channel, hot-swappable, isolated dc-to-dc ..... **ADM3260**
**Isolators**, digital, 2-channel, 2.5-kV, reinforced isolation ..... **ADuM124x**
**Processor**, audio, SigmaDSP® ..... **ADAU1452**
**Transceiver**, HDMI,® on-screen display ..... **ADV7627**
**Transceivers**, HDMI crosspoint, on-screen display ..... **ADV7625/ADV7626**

### March

**ADCs**, 2-channel/4-channel/8-channel, 12-bit, 1-MSPS, successive-approximation ..... **AD7091R-x**
**ADCs**, 6-channel, 16-bit, 250-kSPS, simultaneous-sampling ..... **AD7656A/AD7656A-1**
**ADCs**, 18-bit, 100-kSPS/500-kSPS, successive-approximation ..... **AD7989-1/AD7989-5**
**Amplifier**, operational, low-offset, wide-bandwidth, low-noise ..... **ADA4077-1**
**Controller**, digital, for isolated power supply, PMBus interface ..... **ADP1050**
**Controller**, PWM, for battery test applications, buck/boost ..... **ADP1972**
**DAC**, 16-bit, *nano*DAC® ..... **AD5683**
**DACs**, 10-bit, *nano*DAC, 2-ppm/°C reference ..... **AD5310R/AD5311R**
**DACs**, 12-/14-/16-bit *nano*DAC, 2-ppm/°C reference ..... **AD568xR**
**DAC**, 12-channel, 24-bit, 192-kHz, differential-output ..... **ADAU1962**
**Drivers**, half-bridge, isolated 4-A peak output currents ..... **ADuM3224/ADuM4224**
**Front End**, analog, for testing and monitoring battery cells ..... **AD8450**
**PMUs**, four buck regulators, voltage monitor, watchdog, reset ..... **ADP5051/ADP5053**
**Sensor**, inertial, tactical-grade, 10 degrees of freedom ..... **ADIS16488A**

## Analog Dialogue

*Analog Dialogue*, www.analog.com/analogdialogue, the technical magazine of Analog Devices, discusses products, applications, technology, and techniques for analog, digital, and mixed-signal processing. Published continuously for 48 years—starting in 1967—it is available in two versions. Monthly editions offer technical articles; timely information including recent application notes, circuit notes, new-product briefs, webinars, and published articles; and a universe of links to important and relevant information on the Analog Devices website, www.analog.com. Printable quarterly issues and ebook versions feature collections of monthly articles. For history buffs, the *Analog Dialogue* archive, www.analog.com/library/analogdialogue/archives.html, includes all regular editions, starting with Volume 1, Number 1 (1967), and three special anniversary issues. To subscribe, please go to www.analog.com/library/analogdialogue/subscribe.html. Your comments are always welcome: Facebook: www.facebook.com/analogdialogue; EngineerZone: ez.analog.com/blogs/analogdialogue; Email: dialogue.editor@analog.com or *Scott Wayne*, Editor [scott.wayne@analog.com].

# Precision Resolver-to-Digital Converter Measures Angular Position and Velocity

By Jakub Szymczak, Shane O'Meara, Johnny S. Gealon, and Christopher Nelson De La Rama

## Introduction

Resolvers, electromechanical sensors that measure precise angular position, operate as variable coupling transformers, with the amount of magnetic coupling between the primary winding and two secondary windings varying according to the position of the rotating element (rotor), which is typically mounted on the motor shaft. Employed in industrial motor controls, servos, robotics, power-train units in hybrid- and full-electric vehicles, and many other applications that require precise shaft rotation, resolvers can withstand severe conditions for a very long time, making them the perfect choice for military systems in harsh environments.

Standard resolvers have a primary winding on the rotor and two secondary windings on the stator. Variable reluctance resolvers, on the other hand, have no windings on the rotor. Their primary and secondary windings are all on the stator, but the saliency (exposed poles) of the rotor couples the sinusoidal variation in the secondary with the angular position. Figure 1 shows classical and variable reluctance resolvers.

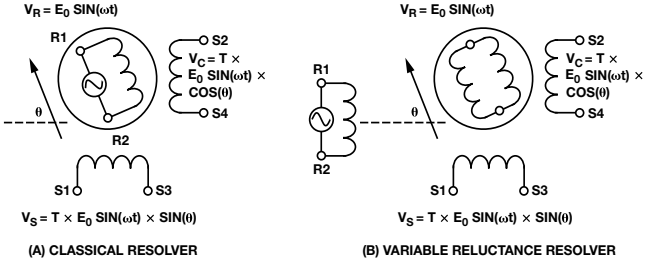



Figure 1. Classical resolver vs. variable reluctance resolver.

When the primary winding, *R1–R2*, is excited with a sinusoidal signal as expressed in Equation 1, a signal is induced in the secondary windings. The amount of coupling onto the secondary windings is a function of the position of the rotor relative to that of the stator, and an attenuation factor known as the resolver transformation ratio. Because the secondary windings are displaced mechanically by 90°, the two output sinusoidal signals are phase shifted by 90° with respect to each other. The relationships between the resolver input and output voltages are shown in Equation 2 and Equation 3. Equation 2 is the sine signal; Equation 3 is the cosine signal.

$$R1-R2 = E_0 \sin \omega t \quad (1)$$

$$S3-S1 = T \times E_0 \sin \omega t \times \sin \theta \quad (2)$$

$$S2-S4 = T \times E_0 \sin \omega t \times \cos \theta \quad (3)$$

where: $\theta$ is the shaft angle, $\omega$ is the excitation signal frequency, $E_0$ is the excitation signal amplitude, and $T$ is the resolver transformation ratio.

The two output signals are modulated by the sine and cosine of the shaft angle. A graphical representation of the excitation signal and the sine and cosine output signals is shown in Figure 2. The sine signal has maximum amplitude at 90° and 270° and the cosine signal has maximum amplitude at 0° and 180°.

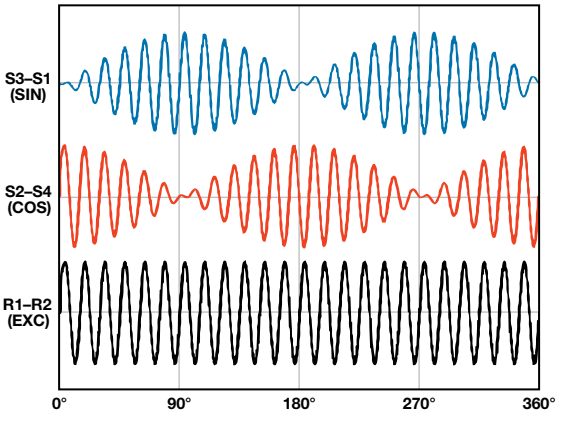



Figure 2. Resolver electrical signal representation.

A resolver sensor has a unique set of parameters that should be considered during the design phase. The most critical electrical parameters and the respective typical specifications are summarized in Table 1.

**Table 1. Resolver Key Parameters**

| Electrical Parameter | Typical Range | Unit | Description |
|---|---|---|---|
| Input Voltage | 3–7 | V rms | Recommended excitation signal amplitude to be applied to resolver primary winding R1–R2 |
| Input Frequency | 50–20,000 | Hz | Recommended excitation signal frequency to be applied to resolver primary winding R1–R2 |
| Transformation Ratio | 0.2–1.0 | V/V | Ratio between the primary and secondary windings signal amplitude |
| Input Impedance | 100–500 | Ω | Input impedance of resolver |
| Phase Shift | ±25 | degrees | Phase shift between excitation signal applied to primary winding (R1–R2) and sine/cosine signals on secondary windings (S3–S1, S2–S4) |
| Pole Pairs | 1–3 | | Number of electrical rotations per mechanical rotation |

### Resolver-to-Digital Converter

The primary winding is excited with the sine wave reference signal, and two differential output signals, sine and cosine, are electromagnetically induced on the secondary windings. Interfacing between the resolver and the system microprocessor, a resolver-to-digital converter (RDC) uses these sine and cosine signals to decode the angular position and rotation speed of the motor shaft.

A majority of RDCs uses a Type-II tracking loop to perform position and velocity calculations. Type-II loops use a second-order filter to ensure that steady-state errors are zero for stationary or constant-velocity input signals. The RDC simultaneously samples both input signals to provide digitized data to the tracking loop. The newest example of an RDC that uses this type of loop is ADI's AD2S1210 complete 10-bit to 16-bit tracking converter, whose on-chip programmable sinusoidal oscillator provides the excitation signal for the primary winding.

As specified in Table 1, a typical resolver requires a low-impedance 3-V rms to 7-V rms signal to drive the primary winding. Operating on a 5-V supply, the RDC typically delivers a 7.2-V p-p differential signal on the excitation outputs. This signal does not have sufficient amplitude and drive capability to meet the resolver's input specifications. In addition, resolvers attenuate signals by up to 5×, so the resolver output amplitude does not meet the RDC's input amplitude requirements, shown in Table 2.

A solution to this problem is to use a differential amplifier to boost the sinusoidal signal to the primary. This amplifier must be able to drive loads as low as 100 Ω. A common practice is to drive the primary with a large signal to obtain a good signal-to-noise ratio. The output sine and cosine signals can then be attenuated with a resistor divider.

In many industrial and automotive applications, RDCs are used in noisy environments, which can induce high-frequency noise into the sine and cosine lines. To solve this, insert a simple differential low-pass filter as close as possible to the RDC. Figure 3 shows a typical resolver-to-digital converter interface including amplifier and filter.

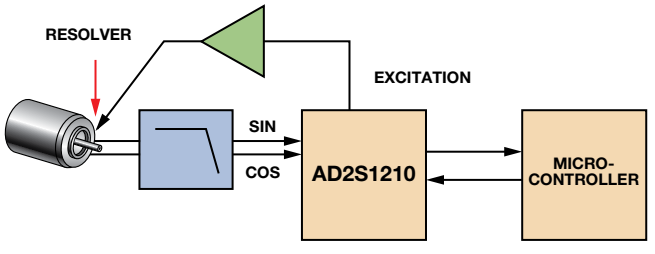



Figure 3. Typical resolver system block diagram.

### Theory of Operation

Figure 4 shows the operational blocks in the RDC. The converter continuously tracks the shaft angle $\theta$ by producing an output angle $\phi$, which is fed back and compared to the input angle. The resulting error between the two angles is minimized when the converter is tracking the position.

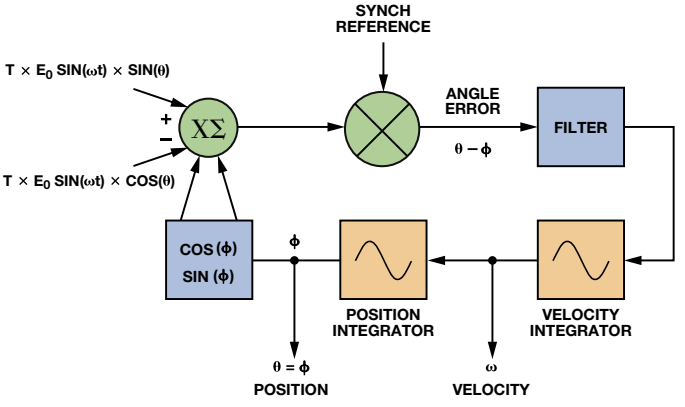



Figure 4. AD2S1210 operational block diagram.

To measure the error, multiply the sine and cosine inputs by cos($\phi$) and sin($\phi$) respectively:

$$E_0 \sin \omega t \times \sin\theta \cos\phi \,(\text{for } S3 - S1) \quad (4)$$

$$E_0 \sin \omega t \times \cos\theta \sin\phi \,(\text{for } S2 - S4) \quad (5)$$

Next, take the difference between the two:

$$E_0 \sin \omega t \times (\sin\theta\cos\phi - \cos\theta \sin\phi) \quad (6)$$

Then, demodulate the signal using the internally generated synthetic reference:

$$E_0 (\sin\theta\cos\phi - \cos\theta \sin\phi) \quad (7)$$

Using a trigonometric identity, $E_0$ (sin $\theta$ cos $\phi$ − cos $\theta$ sin $\phi$) = $E_0$ sin ($\theta - \phi$), which is approximately equal to $E_0(\theta - \phi)$ for small values of angular error ($\theta - \phi$). $E_0(\theta - \phi)$ is the difference between the angular error of the rotor and the digital angle output of the converter. The Type-II tracking loop operates to null the error signal. When this is accomplished, $\phi$ equals the resolver angle $\theta$.

### Key RDC Parameters

Engineers must consider a number of parameters used to characterize resolver-to-digital converters before selecting an appropriate device. Table 2 shows key RDC parameters and specifications for the AD2S1210, which sets the boundaries as the best-in-class converter.

**Table 2. Key RDC Parameters and Values for the AD2S1210**

| Parameter | Typical Value | Unit | Description |
|---|---|---|---|
| Input Voltage | 2.3–4.0 | V p-p | Differential signal range for the sine and cosine inputs |
| Phase Lock Range | ±44 | degrees | Phase shift between the excitation signal generated by the RDC and the sine and cosine inputs |
| Angular Accuracy | ±2.5 | arc min | Angular accuracy of the RDC |
| Resolution | 10, 12, 14, 16 | bits | RDC resolution |
| Velocity Accuracy | 2 | LSB | Velocity precision offered by the RDC |
| Tracking Rate | 3125, 1250, 625, 156 | rps | Tracking capabilities at specific resolutions |
| Settling Time | 2.2, 6, 14.7, 66 | ms | Converter response time to a 179° step change at specific resolutions |

### Error Sources

The accuracy of a complete system is determined by the accuracy of the RDC, as well as errors from the resolver, system architecture, cabling, excitation buffer, and sine/cosine input circuitry. The most common sources of system error are amplitude mismatch, signal phase shift, offsets, and acceleration.

Amplitude mismatch is the difference in the peak-to-peak amplitudes of the sine and cosine signals when they are at their peak amplitudes, 0° and 180° for cosine, 90° and 270° for sine. Mismatch can be introduced by variation in the resolver windings, or by the gain between the resolver and the RDC's sine and cosine inputs. Equation 3 can be rewritten as

$$S2 - S4 = T \times (1 + \delta) \times E_0 \sin \omega t \times \cos \theta \quad (8)$$

where $\delta$ is the percentage amplitude mismatch of the cosine signal relative to the sine signal. The static position error, $\varepsilon$, expressed in radians, is defined as

$$\varepsilon = \frac{\delta}{2} \sin (2\theta) \quad (9)$$

Equation 9 shows that the amplitude mismatch error oscillates at twice the rate of rotation, with a maximum of $\delta/2$ at odd integer multiples of 45°, and no error at 0°, 90°, 180°, and 270°. With a 12-bit RDC, 0.3% amplitude mismatch will result in approximately 1 LSB of error.

The RDC accepts differential sine and cosine signals from the resolver. The resolver removes any dc component from the carrier, so a $V_{REF}/2$ dc bias must be added to ensure that the resolver output signals are in the correct operating range for the RDC. Any offset in the dc bias between SIN and SINLO inputs or COS and COSLO inputs introduces an additional system error.

The error introduced by the common-mode offset is worse in the quadrants where the sine and cosine signal carriers are in antiphase to each other. This occurs for positions between 90° and 180° and 270° and 360°, as shown in Figure 5. Common-mode voltages between the terminals offset the differential signal by twice the common-mode voltage. The RDC is ratiometric, so perceived changes in amplitude of the incoming signals cause an error in position.

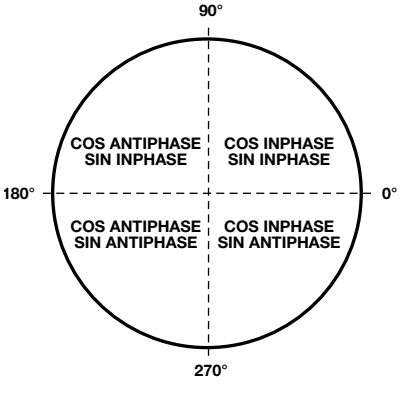



Figure 5. Resolver quadrants.

Figure 6 shows that even when the differential peak-to-peak amplitude of the sine and cosine are equal, the perceived amplitudes of the incoming signals are different. The worst case error will occur at 135° and 315°. At 135°, A = B in an ideal system, but A ≠ B in the presence of offset, so a perceived amplitude mismatch occurs.

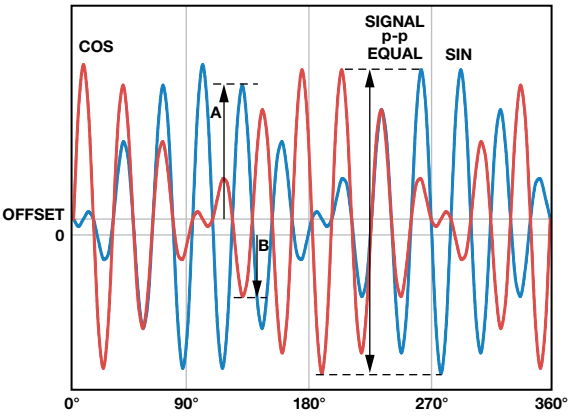



Figure 6. DC bias offset.

Another source of error is differential phase shift, which is the phase shift between the resolver's sine and cosine signals. Some differential phase shift will be present on all resolvers as a result of coupling. A small resolver residual voltage or quadrature voltage indicates a small differential phase shift. Additional phase shift can be introduced if the sine and cosine signal lines have unequal cable lengths or drive different loads.

The differential phase of the cosine signal relative to the sine signal is

$$S2 - S4 = T \times E_0 \sin (\omega t + \alpha) \times \cos \theta \quad (10)$$

where $\alpha$ is the differential phase shift.

Solving for the error introduced by $\alpha$ yields the error term, $\varepsilon$

$$\varepsilon = \frac{\alpha^2}{2} \times 0.5 \quad (11)$$

where $\alpha$ and $\varepsilon$ are expressed in radians.

Most resolvers also introduce a phase shift between the excitation reference signal and the sine and cosine signals, causing an additional error, $\varepsilon$

$$\varepsilon = 0.53 \times \alpha \times \beta \quad (12)$$

where $\beta$ is the phase shift between the sine/cosine signals and the excitation reference signal.

This error can be minimized by choosing a resolver with a small residual voltage, ensuring that the sine and cosine signals are handled identically, and by removing the reference phase shift.

Under static operating conditions, phase shift between the excitation reference and the signal lines will not affect the converter's accuracy, but resolvers at speed generate *speed voltages* due to the reactive components of the rotor impedance and the signals of interest. Speed voltages, which only occur at speed, not at static angles, are in quadrature to the signal of interest. Their maximum amplitude is

$$\text{Speed\_Voltage} = \frac{\text{Motor\_Speed}}{\text{Excitation\_Frequency}} \quad (13)$$

In practical resolvers, rotor windings include both reactive and resistive components. The resistive component produces a nonzero phase shift in the reference excitation that is present when the rotor is both at speed and static. Together with the speed voltages, the nonzero phase shift of the excitation produces a tracking error that can be approximated as

$$\varepsilon = \beta \times \text{Speed\_Voltage} \quad (14)$$

To compensate for the phase error between the resolver reference excitation and sine/cosine signals, the AD2S1210 uses the internally filtered sine and cosine signals to synthesize an internal reference signal in phase with the reference frequency carrier. Generated by determining the zero crossing of either the sine or cosine (whichever is larger, to improve phase accuracy) and evaluating the phase of the resolver reference excitation, it reduces the phase shift between the reference and sine/cosine inputs to less than 10′ and operates for phase shifts of ±44°. A block diagram of the synthetic reference block is shown in Figure 7.

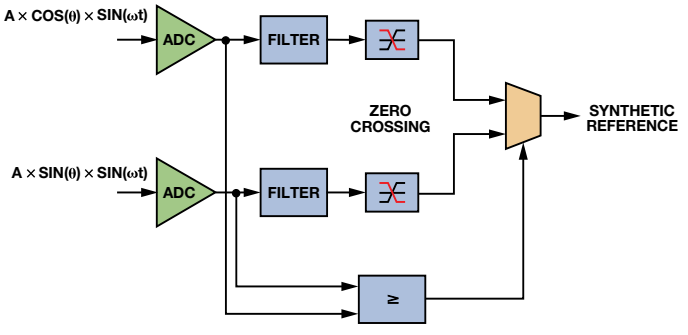



Figure 7. Synthetic reference.

The advantage of Type-II tracking loops over Type-I loops is that no positional error occurs with constant velocity. Even in a perfectly balanced system, however, acceleration will create an error term. The amount of error due to acceleration is determined by the control-loop response. Figure 8 shows the loop response for the AD2S1210.

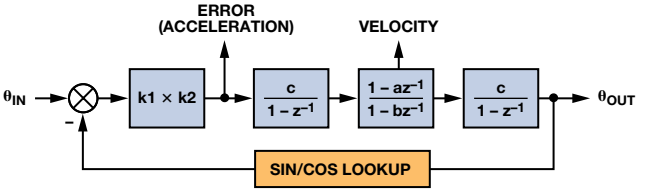



Figure 8. AD2S1210 loop response.

The loop acceleration constant, $K_a$, is

$$K_a = \frac{k1 \times k2 \times c^2 (1 - a)}{T^2 (1 - b)} \quad (15)$$

where the loop coefficients change depending on the resolution, input signal amplitude, and the sampling period. The AD2S1210 samples twice during each $CLK_{IN}$ period.

The tracking error due to acceleration can then be calculated as

$$\text{Tracking Error} = \frac{\text{Input Acceleration}}{K_a} \quad (16)$$

Figure 9 shows the angular error due vs. acceleration for different resolution settings.

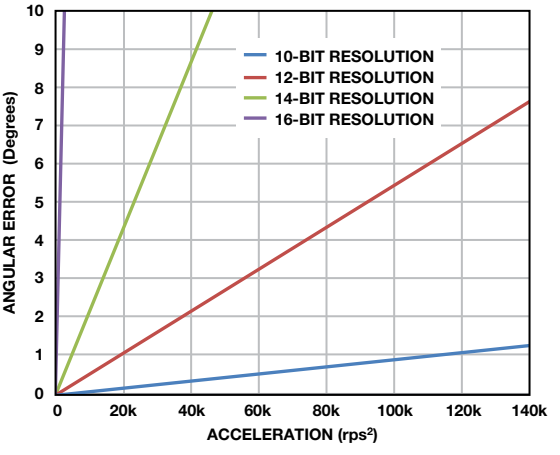



Figure 9. Angular error vs. acceleration.

**Table 3. RDC System Response Parameters**

| Parameter | Description | 10-Bit Resolution | 12-Bit Resolution | 14-Bit Resolution | 16-Bit Resolution |
|---|---|---|---|---|---|
| k1 | ADC gain | Input voltage/ref voltage = (3.15/2)/2.47 (nominal) | | | |
| k2 | Error gain | $12\pi \times 10^6$ | $36\pi \times 10^6$ | $164\pi \times 10^6$ | $132\pi \times 10^6$ |
| a | Compensator zero coefficient | 8187/8192 | 4095/4096 | 8191/8192 | 32,767/32,768 |
| b | Compensator pole coefficient | 509/512 | 4085/4096 | 16,359/16,384 | 32,757/32,768 |
| c | Integrator gain | $1/2^{20}$ | $1/2^{22}$ | $1/2^{24}$ | $1/2^{26}$ |
| T | Sampling period | $1/(CLK_{IN}/2)$ | | | |

### Input Filter

For best system accuracy, connect the resolver outputs directly to the AD2S1210 SIN, COS, SINLO, and COSLO pins to reduce mismatch or phase shifts. This is not always feasible, however. It may be necessary to attenuate the resolver's sine and cosine signals to match the RDC's input specifications, some signal filtering may be required due to the noisy environment, and ESD or short-circuit protection may be required at the resolver connector.

Figure 10 shows a typical interface circuit between the resolver and the AD2S1210. The series resistors and the diodes provide adequate protection to reduce the energy of external events such as ESD or shorts to supply or ground. These resistors and the capacitor implement a low-pass filter that reduces high-frequency noise that couples onto the resolver inputs as a result of driving the motor. It may also be necessary to attenuate the resolver sine and cosine input signals to align with the RDC's input voltage specification. This can be accomplished by the addition of resistor $R_A$. The AD2S1210 has internal circuitry to bias the SIN, SINLO, COS, and COSLO to $V_{REF}/2$. This weak bias can be easily overdriven. A simple method to achieve this is the inclusion of 47-kΩ resistors $R_B$, which will bias the signals to 2.5 V.

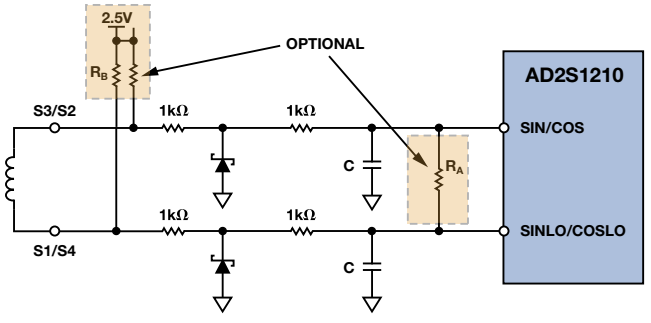



Figure 10. Interface circuit.

### Excitation Buffer

A buffer is typically required to drive the resolver's low-impendence inputs. This excitation buffer can be implemented in many ways, two of which are shown here. The first circuit is commonly used in automotive and industrial designs, while the second simplifies design by replacing the standard push-pull architecture with a high output current amplifier.

The high-current driver shown in Figure 11 amplifies and level shifts the reference oscillator output. The driver uses an AD8662 dual, low-noise, precision op amp and a discrete emitter follower output stage. A duplicate buffer circuit provides a fully differential signal to drive the resolver's primary winding.

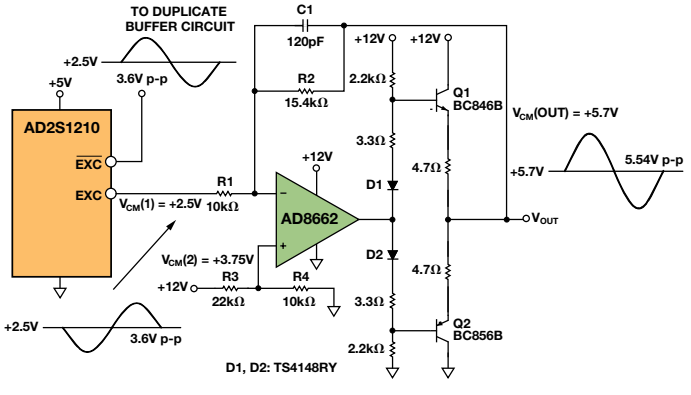



Figure 11. High-current reference buffer uses AD8662 op amp with push-pull output.

This high-current buffer offers drive capability, gain range, and bandwidth optimized for a standard resolver, and it can be adjusted to meet specific requirements of the application and sensor, but the complex design has a number of disadvantages in terms of component count, PCB size, cost, and engineering time needed to alter it to application-specific needs.

The design can be optimized by replacing the AD8662 with an amplifier that provides the high output current required for driving resolvers directly, simplifying the design and eliminating the need for a push-pull stage.

The high-current driver shown in Figure 12 uses the AD8397 high-current dual op amp with rail-to-rail outputs to amplify and level shift the reference oscillator output, optimizing the interface to the resolver. The AD8397 achieves low-distortion, high output current, and wide dynamic range, making it ideal for use with resolvers. With 310-mA current capability for 32-Ω loads, it can deliver the required power to a resolver without the use of the conventional push-pull stage, simplifying the driver circuit and reducing power consumption. A duplicate circuit provides a fully differential signal to drive the primary winding. Available in an 8-lead SOIC package, the AD8397 is specified over the −40°C to +125°C extended industrial temperature range.

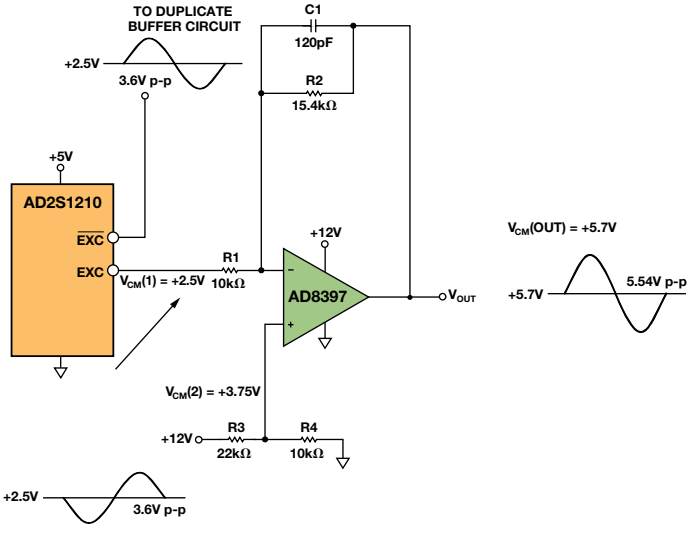



Figure 12. High-current reference buffer based on the AD8397 op amp.

The passive component values can be altered to change the output amplitude and common-mode voltage, with the output amplitude set by the amplifier gain, *R2*/*R1*, and the common-mode voltage set by *R3* and *R4*.

Capacitor *C1* and Resistor *R2* form a low-pass filter to minimize noise on the EXC and $\overline{\text{EXC}}$ outputs. The capacitor should be chosen to minimize phase shift of the carrier. The total phase shift between the excitation output and the sine and cosine inputs should not exceed the phase-lock range of the RDC. The capacitor is optional, as classical resolvers filter out high-frequency components exceptionally well.

Figure 13 shows the AD8397 reference buffer compared with a traditional push-pull circuit. An FFT analyzer measured power of the fundamental and harmonics on the excitation signals of the AD2S1210.

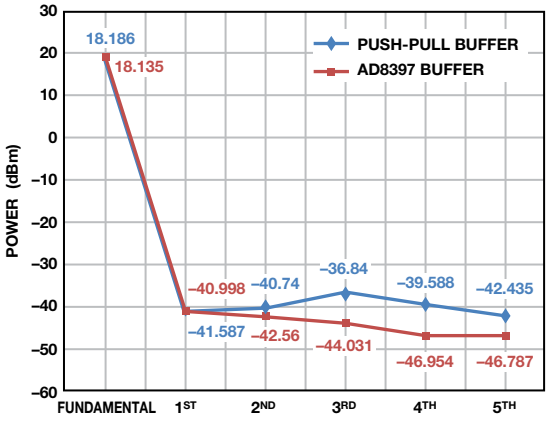



Figure 13. AD8397 buffer vs. AD8662 push-pull buffer.

The power of each fundamental shows little discrepancy between both configurations, but the AD8397 buffer has reduced harmonics. Although the AD8397 circuit offers slightly lower distortion, both buffers provide adequate performance. Eliminating the push-pull stage simplifies the design, uses less space, and consumes less power as compared to a conventional circuit.

## Conclusion

When combined with the AD2S1210 resolver-to-digital converter, resolvers can create a high-precision, robust control system for position and velocity measurements in motor-control applications. To achieve the best overall performance, buffer circuits based on the AD8662 or the AD8397 are required to amplify the excitation signals and provide the drive strength required by the resolver. To complete the system, a basic input circuit can provide signal conditioning as required. As is the case with all mixed-signal mechatronic signal chains, care must be taken to design an accurate system that considers all error sources. With its variable resolution, reference generation, and on-chip diagnostics, the AD2S1210 provides an ideal RDC solution for resolver applications. It is available in industrial and automotive grades.

## References


Circuit Note CN-0276. *High Performance, 10-Bit to 16-Bit Resolver-to-Digital Converter*.

Circuit Note CN-0192. *High Current Driver for the AD2S1210 Resolver-to-Digital Reference Signal Output*.


## Authors


**Jakub Szymczak** [jakub.szymczak@analog.com] is an applications engineer in the Precision Converters Group in Limerick, Ireland. He joined ADI in 2007 after graduating from the Wroclaw University of Technology, Poland, with an MSc in electrical engineering.

**Shane O'Meara** [shane.omeara@analog.com] is an applications engineer at Analog Devices. He joined ADI in 2011 and works in the Precision Converters Applications Group in Limerick, Ireland. He graduated with a BEng in electronic engineering from the University of Limerick.

**Johnny S. Gealon** [johnny.gealon@analog.com] graduated from Mindanao State University–Iligan Institute of Technology, Philippines, with a bachelor's degree in electronics and communications engineering. After three years working as a PCB layout engineer in ROHM LSI Design, Philippines, he earned units in IC design as part of his postgraduate study in National Taipei University, Taiwan. In 2011, he joined ADGT, spending his first year working as a test development engineer on HAD and PMP products, and is currently a product applications engineer on PAD products.

**Christopher Nelson De La Rama** [christopher.delarama@analog.com] is a product applications engineer at Analog Devices. He joined ADI in 2011 and works in the Product Applications Group in General Trias, Cavite, Philippines. He earned his bachelor's degree in electronics and communications engineering from the University of San Carlos–Technological Center, Philippines.

# Noise-Reduction Network for Adjustable-Output Low-Dropout Regulators

By Glenn Morita

### Introduction

Noise is extremely important to designers of high-performance analog circuits, especially high-speed clocks, analog-to-digital converters, digital-to-analog converters, voltage-controlled oscillators, and phase-locked loops. A low-dropout regulator (LDO) can power these circuits. A key to reducing noise is keeping the LDO's noise gain close to unity without compromising either ac performance or dc closed-loop gain.

This article describes how a simple RC network can reduce the output noise of an adjustable-output, low-dropout regulator. Experimental data demonstrates the efficacy of this simple technique. Although noise reduction is its primary focus, the RC network also improves power-supply rejection and load-transient response.

Figure 1 shows a simplified block diagram of a typical adjustable-output LDO. The output voltage, $V_{OUT}$, is the product of the reference voltage and the dc closed-loop gain of the error amplifier: $V_{OUT} = V_R \times (1 + R1/R2)$, where $(1 + R1/R2)$ is the dc closed-loop gain of the error amplifier.

The error-amplifier noise, $V_N$, and reference-voltage noise, $V_{RN}$, are multiplied by the same factor, resulting in output noise that increases in proportion to the programmed output voltage. This results in a modest increase in the output noise for output voltages less than a factor of two greater than the reference voltage, but even this modest increase may be unacceptable in sensitive applications.

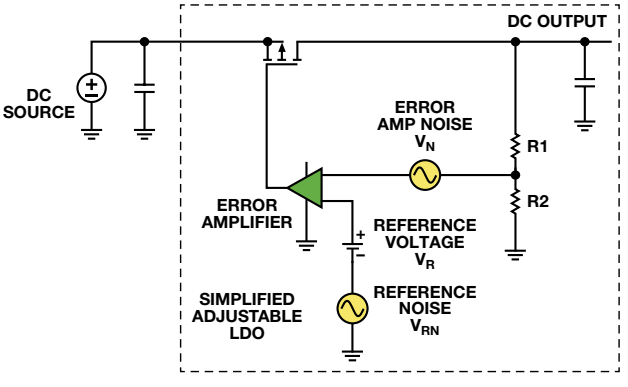



Figure 1. Simplified adjustable LDO block diagram shows internal noise sources.

### LDO Noise

The major sources of noise in LDOs are the internal reference voltage and the error amplifier. Modern devices operate with internal bias currents of a few hundred nanoamps or less to achieve quiescent currents of up to 15 µA. These small currents require bias resistors of up to 1 GΩ, resulting in noisier error-amplifier and reference-voltage circuits as compared to discrete implementations. Typical LDOs use a resistive divider to set the output voltage, so the noise gain is equal to the ac closed-loop gain, which as it turns out, is the same as the dc closed-loop gain.

### Reducing LDO Noise

Two major methods for reducing LDO noise are filtering the reference and reducing the noise gain of the error amplifier. Some LDOs enable an external capacitor to filter the reference. In fact, many so-called ultralow noise LDOs require the use of an external noise-reduction capacitor to achieve their low-noise specifications. The drawback of this technique is that both the error-amplifier noise and any residual reference noise are still amplified by the ac closed-loop gain. This results in noise that is proportional to the output voltage.

Reducing the noise gain of the error amplifier can produce an LDO where the output noise does not increase dramatically with output voltage. Unfortunately, this is not possible for fixed-output LDOs because the feedback node is not accessible. Fortunately, this node is readily accessible in adjustable-output LDOs.

Figure 2 shows an adjustable-output LDO where R1 and R2 set the output voltage. The network formed by R3 and C1 reduces the ac gain of the error amplifier. To ensure stability with LDOs that have low-phase margin or are not unity-gain stable, choose R3 to set the amplifier's high-frequency gain to approximately 1.1. To reduce noise in the 1/f region, choose C1 to set the low-frequency zero to less than 10 Hz.

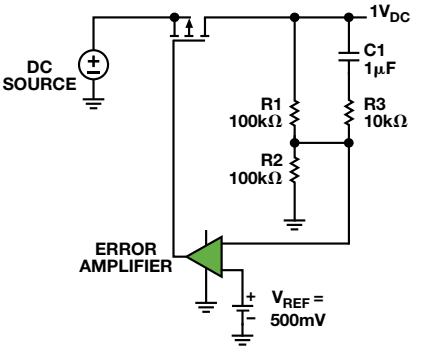



Figure 2. Simple RC network reduces noise gain of an adjustable-output LDO.

Figure 3 compares the ac closed-loop gain with a properly designed noise-reduction network to the open-loop gain and unmodified closed-loop gain. With the noise-reduction network, the ac gain is close to unity for much of the bandwidth, so the reference noise and error amplifier noise are amplified to a lesser degree.

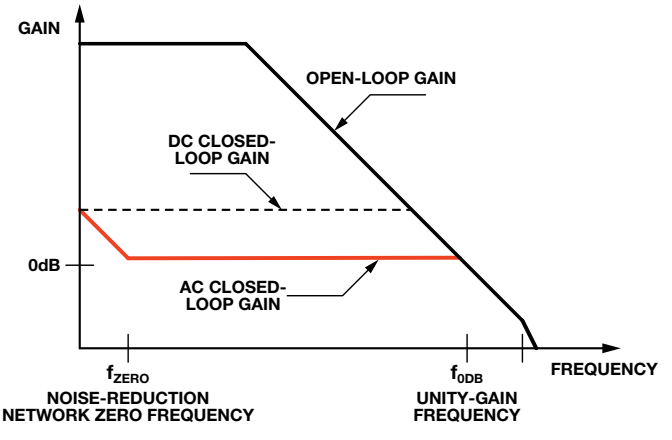



Figure 3. LDO loop gains vs. frequency with noise reduction network.

Figure 4 shows the effect of the noise-reduction network on the noise spectral density of the ADP125 LDO. For comparison, the plot shows the noise spectral density at 4 V with and without the noise-reduction network, as well as the noise spectral density at unity gain.

Note the significant improvement in noise performance between 20 Hz and 2 kHz. Above the zero created by R1 and C1, the noise characteristic with the noise-reduction network is nearly the same as it is at unity gain. Above 20 kHz, the noise spectral density plots converge because the closed-loop gain of the error amplifier meets the open-loop gain, and no further reduction in noise gain is possible.

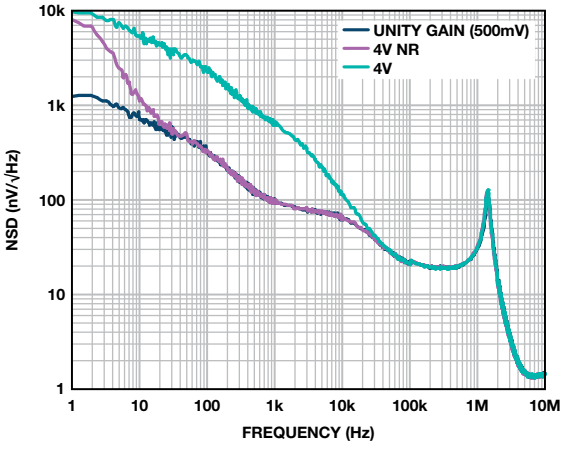



Figure 4. Noise spectral density of the ADP125 adjustable-output LDO.

### Power Supply Rejection

The power-supply rejection ratio (PSRR) over this frequency range also improves. PSRR is a measure of how well a circuit suppresses extraneous signals (noise and ripple) that appear on the power supply input to keep them from corrupting the circuit output. PSRR is defined as PSRR = $VE_{IN}/VE_{OUT}$. This can also be expressed in decibels: PSR = 20 × log($VE_{IN}/VE_{OUT}$), where $VE_{IN}$ and $VE_{OUT}$ are the extraneous signals appearing at the input and output.

For most analog circuits, PSR applies to the pins that supply power to the inner workings of the circuit. With LDOs, however, the input pin supplies power to the internal circuitry as well as load current to the regulated output.

### Improving PSR

An additional benefit of using a noise-reduction network to reduce the output noise of an adjustable-output LDO is that the low-frequency PSR is also improved. R1, R3, and C1 in Figure 2 form a lead-lag network with a zero at approximately 1/(R1 × C1) and a pole at approximately 1/(R3 × C1). The lead-lag network acts as a feedforward function in the compensation loop and therefore improves the PSR. The amount of improvement, in dB, is approximately 20 × log(1 + R1/R3) for frequencies below where the closed-loop gain and open-loop gain converge.

Figure 5 shows the effect of the noise-reduction network on the PSRR of the ADP7102 adjustable-output LDO. With a 9-V output, R1 = 64 kΩ, R2 = 10 kΩ, R3 = 1 kΩ, and C1 = 1 µF. The zero created by R1 and C1 at about 2.5 Hz is evident by the improvement in PSRR above 10 Hz. The overall PSRR increases by about 17 dB from 100 Hz to 1 kHz. The improvement decreases until about 20 kHz where the open-loop gain and closed-loop gain converge.

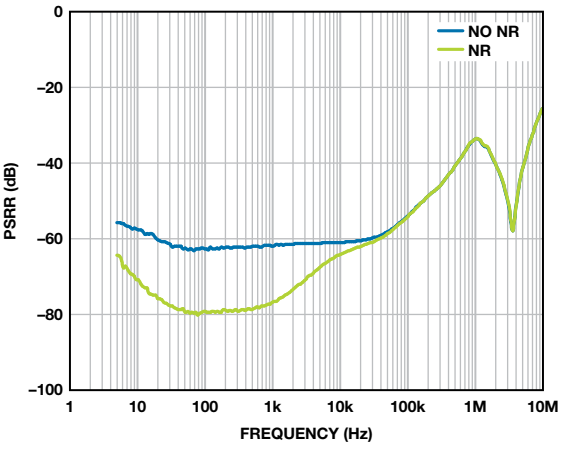



Figure 5. PSRR of the ADP7102/ADP7104 adjustable-output LDO with and without a noise-reduction network.

### Transient-Load Improvement

The noise-reduction network also improves the LDO's transient-load response. Again, R1, R3, and C1 perform a feedforward function in the compensation loop. High-frequency components of the load transient—sensed by the error amplifier without attenuation—allow the error amplifier to respond quickly to the load transient. Figure 6 shows the load transient response of an ADP125 with and without the noise-reduction network. With the noise-reduction network, the LDO is able to respond to the load transient in less than 50 µs, as compared to 500 µs without the network.

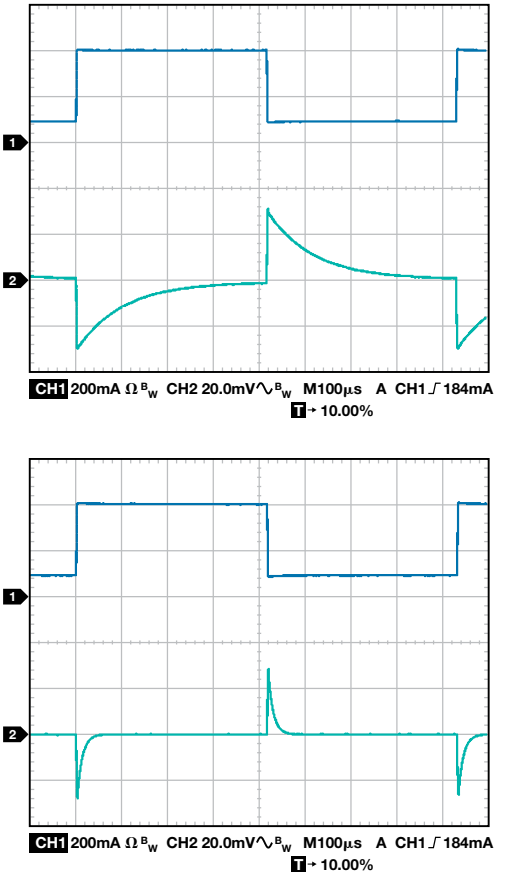



Figure 6. Transient-load response of the ADP125 adjustable-output LDO (a) without noise-reduction network (b) with noise-reduction network.

### Effect on Start-Up Time

One drawback to the noise-reduction network is that it significantly increases the start-up time. Figure 7 shows the start-up time of the ADP125 with and without the noise-reduction network. The normal start-up time is about 600 µs. The start-up time increases to 6 ms with C1 = 10 nF, and to 600 ms with C1 = 1 µF. The increase in start-up time should not be an issue for applications that do not switch the LDO off and on once the circuit is fully powered.

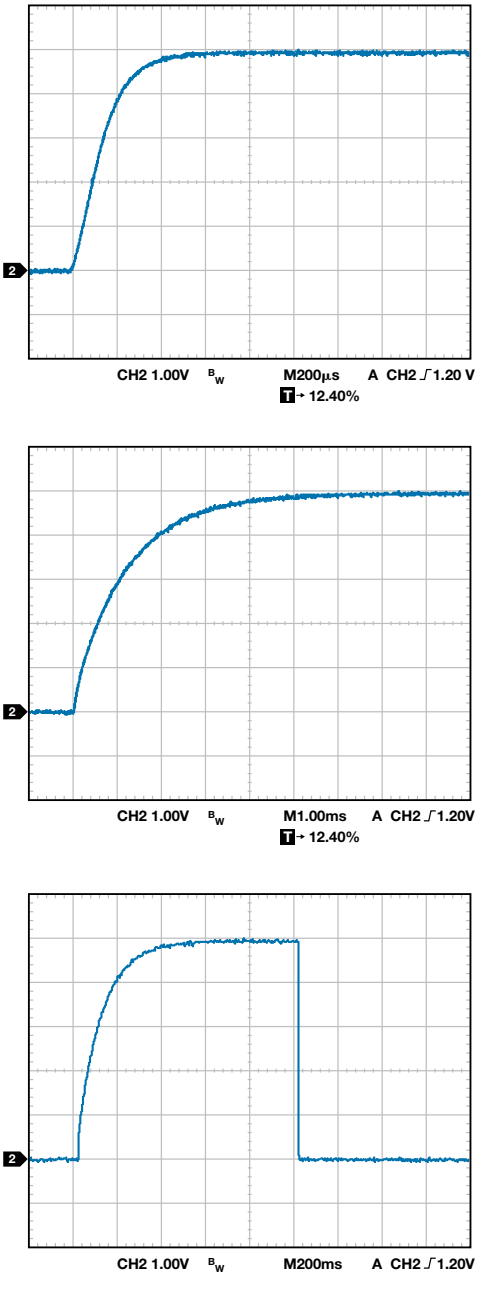



Figure 7. Start-up time of the ADP125 adjustable-output LDO (a) without noise-reduction network (b) with noise-reduction network, C1 = 10 nF, (c) with noise-reduction network, C1 = 1 µF.

### Conclusion

The noise, power-supply rejection, and transient performance of an adjustable-output LDO can be improved significantly by adding a simple RC noise-reduction network, bringing significant benefits to noise-sensitive applications such as high-speed clocks, analog-to-digital converters, digital-to-analog converters, voltage-controlled oscillators, and phase-locked loops.

This technique will work with LDOs with architectures similar to that shown in Figure 2, where both the reference-voltage noise and the error-amplifier noise are amplified by the dc closed-loop gain, such that the output noise scales with the output voltage. LDOs such as the ADP125, ADP171, ADP1741, ADP1753, ADP1755, ADP7102, ADP7104, and ADP7105 all share this general architecture and will benefit greatly from the use of a noise-reduction network.

Newer, ultralow-noise LDOs such as the ADM7151 will not benefit from the noise-reduction network because the architecture uses the LDO error amplifier in unity gain, so the reference voltage is equal to the output voltage. In addition, the internal reference filter has a pole below 1 Hz, heavily filtering the reference voltage and virtually eliminating any reference noise contribution.

### References


Morita, Glenn. "Low-Dropout Regulators—Why the Choice of Bypass Capacitor Matters." *Analog Dialogue*, Volume 45, Number 1, 2011.

Morita, Glenn. AN-1120 Application Note. *Noise Sources in Low-Dropout (LDO) Regulators*. Analog Devices, Inc., 2011.


### Author


**Glenn Morita** [glenn.morita@analog.com]


graduated from Washington State University with a BSEE in 1976. His first job out of school was at Texas Instruments, where he worked on the infrared spectrometer instrument for the Voyager space probe. Since then, Glenn has worked as a designer in the instrumentation, military and aerospace, and medical industries. In 2007, he joined ADI as an applications engineer with the Power Management Products Team in Bellevue, WA. He has over 25 years of linear and switch-mode power supply design experience at power levels ranging from microwatts to kilowatts. Glenn holds two patents for harvesting energy from body heat to power implantable cardioverter defibrillators and an additional patent for extending battery life in external cardioverter defibrillators. In his spare time, he enjoys collecting minerals, faceting gemstones, photography, and visiting the national parks.

# How to Stay Out of Deep Water when Designing with Bridge Sensors

By Gustavo Castro and Scott Hunt

Instrumentation amplifiers (in-amps) can condition the electrical signals generated by sensors, allowing them to be digitized, stored, or used to control processes. The signal is typically small, so the amplifier may need to be operated at high gain. In addition, the signal may sit on top of a large common-mode voltage, or it may be embedded in a substantial dc offset. Precision in-amps can provide high gain, selectively amplifying the difference between the two input voltages while rejecting signals common to both inputs.

Wheatstone bridges are classic examples of this situation, but galvanic cells such as biosensors have similar characteristics. The bridge output signal is differential, so an in-amp is the preferred device for high-precision measurements. Ideally, the unloaded bridge output is zero, but this is true only when all four resistors are exactly equal. Consider a bridge built with discrete resistors, as shown in Figure 1. The worst case differential offset, $V_{OS}$, is

$$V_{OS} = \pm V_{EX} \frac{TOL}{100} \quad (1)$$

where $V_{EX}$ is the bridge excitation voltage and TOL is the resistor tolerance (in percent).

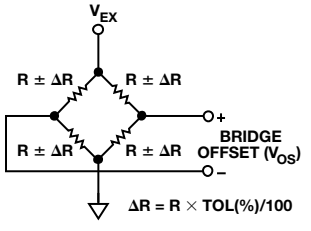



Figure 1. Wheatstone bridge offset.

For example, with 0.1% tolerance for each one of the individual elements and a 5-V excitation voltage, the differential offset can be as high as 5 mV. If a gain of 400 is required to achieve the desired bridge sensitivity, the offset becomes ±2 V at the amplifier output. Assuming that the amplifier is powered by the same supply, and that its output can swing rail-to-rail, more than 80% of the output swing could be consumed by the bridge offset alone. As the industry trends to smaller supply voltages, this problem only gets worse.

The traditional 3-op-amp in-amp architecture, shown in Figure 2, has a differential gain stage followed by a subtractor that removes the common-mode voltage. The gain is applied on the first stage, so the offset is amplified by the same factor as the signal of interest. Thus, the only way to remove it is to apply the opposite voltage to the reference (REF) terminal. The main limitation of this method is that adjusting the voltage on REF cannot correct the offset if the first stage of the amplifier is already saturated. A few approaches to get around this limitation include:

- Shunting the bridge with an external resistor on a case-by-case basis, but this is impractical for automated production and does not allow for adjustments after leaving the factory
- Reducing the first-stage gain, removing the offset by trimming the voltage on REF, and adding a second amplifier circuit to achieve the desired gain
- Reducing the first-stage gain, digitizing the output with a high-resolution ADC, and removing the offset in software

The two last options also need to account for worst-case deviations from the original offset value, further reducing the maximum gain of the first stage. These solutions are not ideal, as they require extra power, board space, or cost to obtain the high first-stage gain needed to obtain high CMRR and low noise. In addition, ac coupling is not an option for measuring dc or very slow-moving signals.

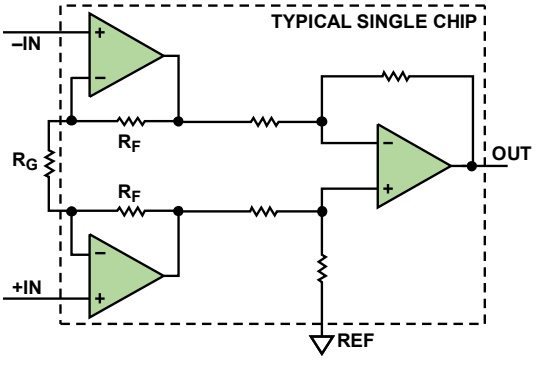



Figure 2. 3-op-amp instrumentation amplifier topology.

Indirect current feedback (ICF) in-amps, such as the AD8237 and AD8420, make it possible to remove the offset before it is amplified. Figure 3 shows a schematic of the ICF topology.

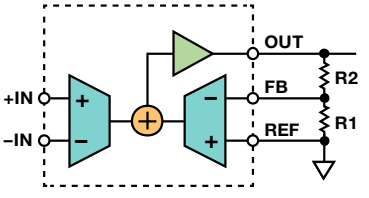



Figure 3. Indirect current feedback in-amp topology.

The transfer function for this instrumentation amplifier is of the same form as that of the classical 3-op-amp topology, and is given by

$$V_{OUT} = \left(1 + \frac{R_2}{R_1}\right)\left(V_{+IN} - V_{-IN}\right) + V_{REF} \quad (2)$$

Because the feedback to the amplifier is satisfied when the voltage between the inputs is equal to the voltage between the feedback (FB) and reference (REF) terminals, we can rewrite this as

$$V_{OUT} = \left(1 + \frac{R_2}{R_1}\right)\left(V_{FB} - V_{REF}\right) + V_{REF} \quad (3)$$

This suggests that introducing a voltage equal to the offset across the feedback and reference terminals allows the output to be adjusted to zero volts even in the presence of a large input offset. As shown in Figure 4, this adjustment can be accomplished by injecting a small current into the feedback node through resistor $R_A$ from a simple voltage source such as a low-cost DAC or a filtered PWM signal from an embedded microcontroller.

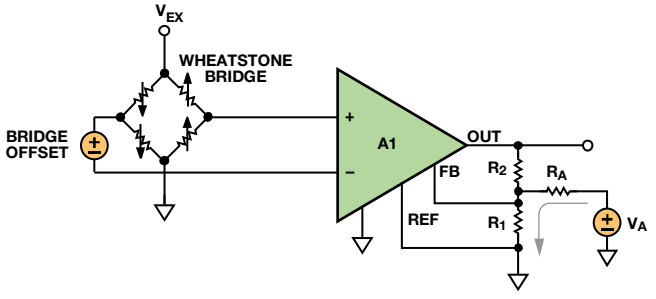



Figure 4. High gain bridge circuit with offset removal.

### Design Procedure

From Equation (3), the ratio of $R_1$ and $R_2$ sets the gain as follows:

$$G = \left(1 + \frac{R_2}{R_1}\right) \quad (4)$$

The designer must determine the resistor values. Larger values reduce power consumption and output loading; smaller values limit the input bias current at FB and input impedance errors. If the parallel combination of $R_1$ and $R_2$ is greater than about 30 kΩ, the resistors start to contribute to the noise. Table 1 shows some suggested values.

**Table 1. Suggested Resistors for Various Gains (1% Resistors)**

| $R_1$ (kΩ) | $R_2$ (kΩ) | Gain |
|---|---|---|
| None | Short | 1 |
| 49.9 | 49.9 | 2 |
| 20 | 80.6 | 5.03 |
| 10 | 90.9 | 10.09 |
| 5 | 95.3 | 20.06 |
| 2 | 97.6 | 49.8 |
| 1 | 100 | 101 |
| 1 | 200 | 201 |
| 1 | 499 | 500 |
| 1 | 1000 | 1001 |

To simplify the process of finding a value for $R_A$, assume dual-supply operation, a grounded REF terminal, and a known bipolar adjustment voltage $V_A$. In this case, the output voltage is given by

$$V_{OUT} = \left(1 + \frac{R_2}{R_1} + \frac{R_2}{R_A}\right)V_{IN} - \frac{R_2}{R_A}V_A \quad (5)$$

Notice that the gain from $V_A$ to the output is inverting. An increase in $V_A$ reduces the output voltage by a fraction given by the ratio of resistors $R_2$ and $R_A$. This ratio allows the adjustment range to be maximized for a given input offset. Because the adjustment range is referred to the input of the amplifier before gain, fine adjustment steps can be achieved even with a low resolution source. Since RA is typically much larger than $R_1$, we can approximate Equation (5) as

$$V_{OUT} = \left(1 + \frac{R_2}{R_1}\right)V_{IN} - \frac{R_2}{R_A}V_A \quad (6)$$

To find a value of $R_A$ that will allow a maximum offset adjustment, $V_{IN(MAX)}$, with a given adjustment voltage range, $V_{A(MAX)}$, set $V_{OUT} = 0$ and solve for $R_A$, giving

$$R_A = \left(\frac{R_1 R_2}{R_1 + R_2}\right)\frac{V_{A(MAX)}}{V_{IN(MAX)}} \quad (7)$$

where $V_{IN(MAX)}$ is the maximum offset expected from the sensor. Equation (5) also shows that the insertion of the adjustment circuit modifies the gain from the input to the output. Even though this will generally have a small effect, the gain can be recalculated as

$$Gain = \left(1 + \frac{R_2}{R_1} + \frac{R_2}{R_A}\right) \quad (8)$$

In general, for single-supply bridge conditioning applications, the voltage on the reference terminal should be above the signal ground. This is especially true if the bridge output can swing positive and negative. If the reference voltage is driven to a voltage, $V_{REF}$, with a low-impedance source such as a resistor divider and a buffer, as shown in Figure 5, Equation (5) becomes

$$V_{OUT} = \left(1 + \frac{R_2}{R_1} + \frac{R_2}{R_A}\right)V_{IN} - \frac{R_2}{R_A}(V_A - V_{REF}) + V_{REF} \quad (9)$$

This same result would be obtained if $V_{OUT}$ and $V_A$ were taken relative to $V_{REF}$ in the original equations. $V_{A(MAX)} - V_{REF}$ should also replace $V_{A(MAX)}$ in Equation (7).

### Design Example

Consider a single-supply bridge amplifier such as that shown in Figure 4, where 3.3 V is used to excite the bridge and power the amplifier. The full-scale bridge output is ±15 mV, and the offset can be in the ±25-mV range. To obtain the desired sensitivity, the amplifier gain needs to be 100, and the input range of the ADC is 0 V to 3.3 V. Because the output of the bridge can be positive or negative, the output is referenced to midsupply, or 1.65 V. Simply by applying a gain of 100, the offset alone would force the amplifier output to be anywhere from –0.85 V to +4.15 V, which exceeds the supply rails.

This problem can be solved with the circuit shown in Figure 5. Bridge Amplifier $A_1$ is an ICF instrumentation amplifier such as the AD8237. Amplifier $A_2$, with $R_4$ and $R_5$, sets the zero level output of $A_1$ at midsupply. The AD5601 8-bit DAC adjusts the output to null the bridge offset through $R_A$. The output of the amplifier is then digitized by the AD7091 micropower 12-bit ADC.

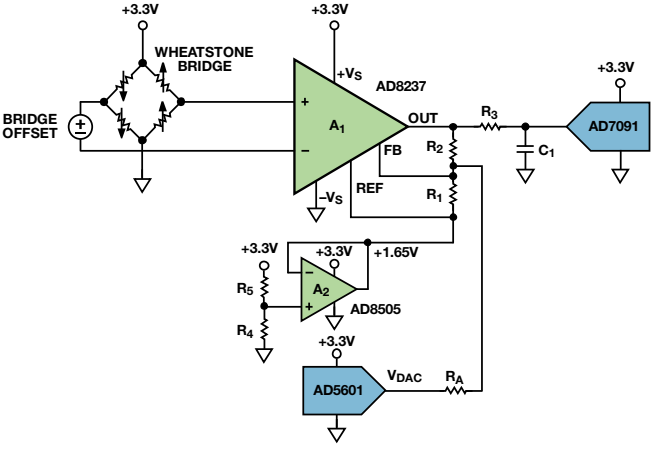



Figure 5. Offset removal circuit modified for single-supply operation.

From Table 1, we find that $R_1$ and $R_2$ need to be 1 kΩ and 100 kΩ for a gain of 101. The circuit includes a DAC that can swing from 0 V to 3.3 V, or ±1.65 V around the 1.65-V reference voltage. To calculate the value of $R_A$ we use Equation (6). With $V_{A(MAX)}$ = 1.65 V and $V_{IN(MAX)}$ = 0.025 V, $R_A$ = 65.347 kΩ. With 1% resistor tolerance, the closest available value is 64.9 kΩ. This leaves no margin for errors caused by source accuracy and temperature variation, however, so we choose a low cost, commonly stocked 49.9-kΩ resistor. The trade-off is reduced adjustment resolution, which results in a slightly larger post-adjustment offset.

From Equation (7), the nominal gain value can be calculated to be 103. If the designer wants to obtain a gain value closer to the target of 100, it is easiest to reduce the value of $R_2$ by about 3% to 97.6 kΩ, which will have very little influence on the value of $R_A$. Under the new conditions, the nominal gain is 100.6.

Because the DAC can swing ±1.65 V, the total offset adjustment range is given by the voltage divider formed by $R_A$ and the parallel combination of $R_1$ and $R_2$, which can be calculated as follows:

$$V_{A\_RANGE} = \left( \frac{R_1 \parallel R_2}{R_1 \parallel R_2 + R_A} \right) V_{A(MAX)} = \frac{0.99\,\text{k}\Omega}{0.99\,\text{k}\Omega + 49.9\,\text{k}\Omega} (\pm 1.65\,\text{V}) = \pm 32.1\,\text{mV} \quad (10)$$

A ±32.1-mV adjustment over the ±25-mV maximum bridge offset provides an additional 28% adjustment margin. With an 8-bit DAC, the step size for the adjustment is

$$V_{A\_STEP} = \frac{2 \times V_{IN(MAX)}}{2^n} = \frac{64.2\,\text{mV}}{256} \approx 250\,\mu\text{V} \quad (11)$$

With a 250-μV adjustment resolution, the maximum residual offset at the output is 12.5 mV.

The values of $R_3$ and $C_1$ can be determined from the values suggested in the ADC data sheet or from Reference 2. For an AD7091 sampling at 1 MSPS, these values are 51 Ω and 4.7 nF. Larger resistor and capacitor combinations can be used when sampling at lower rates to further reduce noise and aliasing effects.

An additional advantage of this circuit is that the bridge offset adjustment can be done at production or installation. If environmental conditions, sensor hysteresis, or long-term drift have an effect on the value of the offset, the circuit can be readjusted.

Because of its true rail-to-rail input, the AD8237 works best in bridge applications that employ very low supply voltages. For traditional industrial applications where higher supply voltages are required, the AD8420 is a good alternative. This ICF in-amp operates with supply voltages from 2.7 V to 36 V and draws 60% less current.

Table 2 compares the two in-amps. Minimum and maximum specifications have been used where available. See the product data sheets for more detailed and up to date information.

**Table 2. Comparison of AD8237 and AD8420**

| Specification | AD8237 | AD8420 |
|---|---|---|
| Technology | CMOS (zero-drift) | Bipolar |
| Quiescent Supply Current | 130 μA | 80 μA |
| Supply Voltage Range | 1.8 V to 5.5 V | 2.7 V to 36 V |
| Input Voltage Range | $-V_S - 0.3$ V to $+V_S + 0.3$ V | $-V_S - 0.15$ V to $+V_S - 2.2$ V |
| Differential Input Voltage Limit | $\pm(V_S - 1.2)$ V | ± 1 V |
| Rail-to-Rail Output | Yes | Yes |
| CMRR (G = 100, dc to 60 Hz) | 114 dB | 100 dB |
| Offset Voltage | 75 μV | 125 μV |
| Offset Voltage Drift | 0.3 μV/°C | 1 μV/°C |
| Voltage Noise Spectral Density | 68 nV/√Hz | 55 nV/√Hz |
| Gain Error (G = 100) | 0.005% | 0.1% |
| Gain Drift | 0.5 ppm/°C | 10 ppm/°C |
| Bandwidth, –3 dB (G = 100) | 10 kHz in HBW mode | 2.5 kHz |
| Package | 8-lead MSOP | 8-lead MSOP |

## References


AN212 Application Note. *Handling Sensor Bridge Offset*. Honeywell International Inc., Rev 05-05.

HMC1001/HMC1002/HMC1021/HMC1022 1- and 2-Axis Magnetic Sensors Data Sheet. Honeywell International Inc., 2008.

Kitchin, Charles and Lew Counts. *A Designer's Guide to Instrumentation Amplifiers*. 3rd Edition. Analog Devices, Inc., 2006.

NPC-410 Series Data Sheet. GE Sensing, 2006.

Product Training Module. *Indirect Current Feedback Instrumentation Amplifier Applications Guide*. Digi-Key Corporation.

Walsh, Alan. "Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter." Analog Dialogue, Volume 46, 2012.


## Authors


**Gustavo Castro** [gustavo.castro@analog.com] is an applications engineer in the Precision Signal Conditioning Group in Wilmington, MA. Prior to joining Analog Devices in January 2011, he worked for 10 years designing high precision instrumentation such as digital multimeters and dc sources. Gustavo received a bachelor's degree in electronics engineering in 2000 from Monterrey Institute of Technology, Mexico. He holds two patents.

**Scott Hunt** [scott.hunt@analog.com] is a product applications engineer in the Linear Products Group in Wilmington, MA. Scott joined Analog Devices in 2011 after receiving a bachelor's degree in electrical engineering from Rensselaer Polytechnic Institute. Scott specializes in integrated precision amplifiers including instrumentation amplifiers, differential amplifiers, and thermocouple amplifiers.

# Dual-Loop Clock Generator Cleans Jitter, Provides Multiple High-Frequency Outputs

By Kyle Slightom

As the speed and resolution of data converters continue to increase, the need for higher-frequency sampling clock sources with lower phase noise is growing. The integrated phase noise (jitter) presented to the clock inputs is one of the many performance bottlenecks facing designers when they create cellular base stations, military radar systems, and other designs that require high-speed, high-performance clock signals. An average system has several low-frequency, noisy signals that a PLL can upconvert to a higher frequency to clock these devices. A single high-frequency PLL can solve the frequency translation problem, but it is difficult to create one with a loop bandwidth that is low enough to filter out the effects of the noisy reference. A PLL with a low-frequency, high-performance VCO/VCXO and low loop bandwidth can clean the noisy reference, but cannot provide the high-frequency outputs. Both high speed and noise filtering can be obtained by combining two PLLs: a low-frequency device with narrow loop bandwidth for jitter cleaning followed by a high-frequency device with a wider loop bandwidth.

Some modern dual-loop analog PLLs are integrated on a single chip, allowing designers to reduce low-frequency reference jitter while providing high-frequency, low-phase-noise outputs. This saves valuable PCB area and allows multiple devices that require different frequencies to be clocked from a single phase-aligned source.

The AD9523, AD9523-1, and AD9524 clock generators, shown in Figure 1, consist of two series-connected analog PLLs. The first PLL (PLL1) cleans the reference jitter, while the second PLL (PLL2) generates high-frequency phase-aligned outputs. PLL2 can also generate a high base frequency from which various lower frequencies can be derived. PLL1 uses an external low-frequency VCXO and a partially embedded third-order loop filter to create a PLL with a loop bandwidth in the 30 Hz to 100 Hz range. The bandwidth of this loop directly affects the amount of reference input phase noise that will propagate to the output. PLL2 uses an internal high-speed VCO centered at 3.8 GHz (3 GHz for the AD9523-1) and a partially embedded third-order loop filter to give it a nominal loop bandwidth of about 500 kHz. The bandwidth and phase noise of this internal VCO directly affect the wideband phase noise of the overall output.

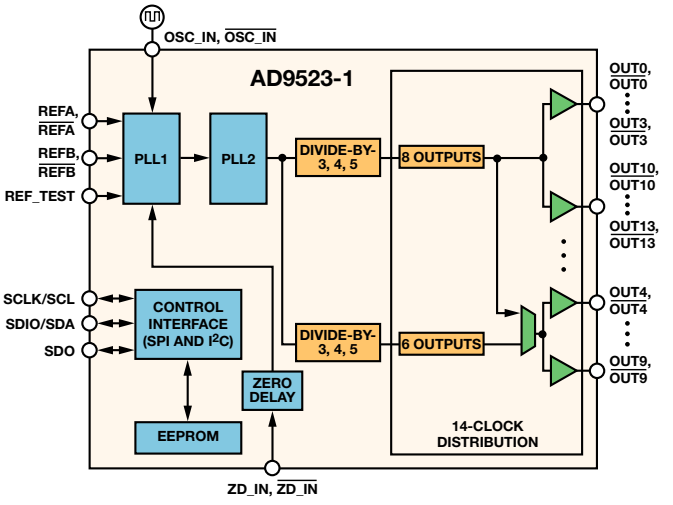



Figure 1. Block diagram of the AD9523-1.

Many engineers think of dual-loop PLLs as frequency translators that reduce the reference input jitter by a fixed amount, but it is more accurate to think of them as low phase noise frequency translators whose performance is affected by each PLL's loop bandwidth and the phase noise profiles of the VCO/VCXOs.

The ADIsimCLK™ simulation tool provides an easy way to determine the effects of reference phase noise on the output phase noise of a dual-loop PLL. This example uses ADIsimCLK to model the effects of a noisy reference on the overall phase noise of the AD9523-1. Figure 2 shows a simulated 122.88-MHz reference with a typical phase noise profile.

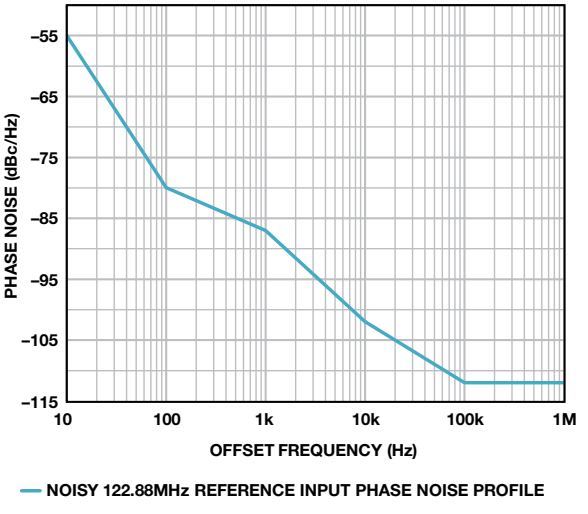



Figure 2. Reference phase noise profile at 122.88 MHz.

PLL1 relies on a high-performance VCXO and low loop bandwidth to attenuate the phase noise of the reference, allowing the phase noise of the VCXO to dominate. This example uses a Crystek CVHD-950 VCXO to generate an output frequency that is identical to the reference input. This shows a direct comparison of how much reference phase noise appears on the output of PLL1. Figure 3 compares the phase noise profile of the Crystek CVHD-950 VCXO and the reference input phase noise.

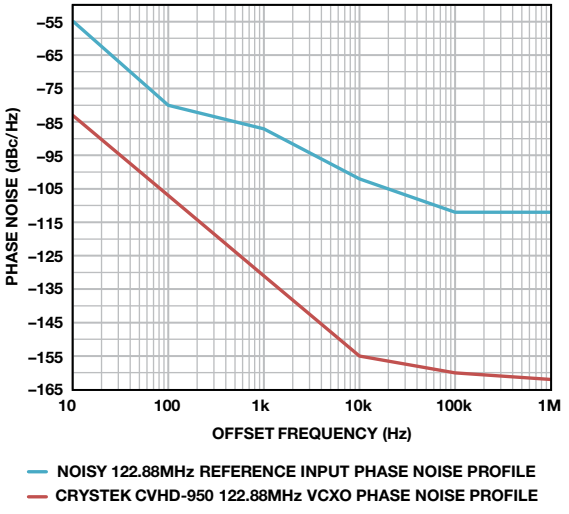



Figure 3. Crystek CVHD-950 phase noise profile at 122.88 MHz.

Figure 4 and Table 1 show the ADIsimCLK configuration parameters used to simulate the AD9523-1's PLL1 output phase noise response for the reference input and PLL1 VCXO phase noise profiles shown in Figure 3. Table 2 shows the PLL1 loop filter values generated by ADIsimCLK given these settings.

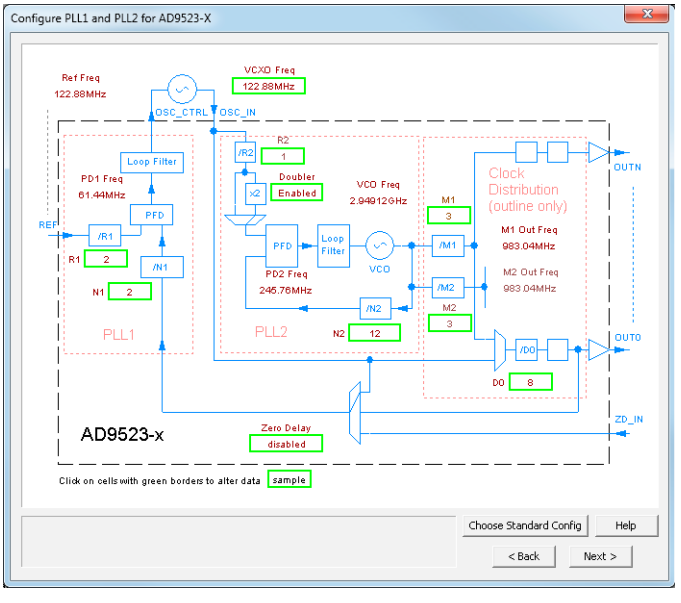



Figure 4. AD9523-1 configuration in ADIsimCLK v1.5.

**Table 1. PLL1 Configuration Parameters**

| Variable | Value |
|---|---|
| VCXO Operating Frequency | 122.88 MHz |
| Reference Frequency | 122.88 MHz |
| Output Frequency | 122.88 MHz |
| R Divider | 2 |
| N Divider | 2 |
| Charge Pump Current | 6 µA |
| $K_{VCO}$ of Crystek CVHD-950 | 3.07 kHz/V |
| Desired Loop BW | 30 Hz |
| Desired Phase Margin | 75° |

**Table 2. PLL1 Loop Filter Component Values Generated by ADIsimCLK**

| Variable | Value |
|---|---|
| $C_{POLE1}$ | 1.5 nF |
| $R_{ZERO}$ | 10 kΩ |
| $C_{EXT}$ | 4.7 µF |
| $R_{POLE2}$ | 165 kΩ |
| $C_{POLE2}$ | 337 pF |

Figure 5 shows the simulated output of PLL1 at 122.88 MHz (solid line) from ADIsimCLK along with the original phase noise profile of the noisy 122.88 MHz reference (dashed line). Note that the phase noise of PLL1's output is much lower than the original reference input phase noise. The loop bandwidth of PLL1 attenuates the phase noise of the reference significantly, allowing the low phase noise profile of the VCXO to dominate after the 30-Hz loop filter cutoff frequency. If the reference phase noise is increased across all offset frequencies, the output phase noise will only increase as a function of PLL1's loop bandwidth.

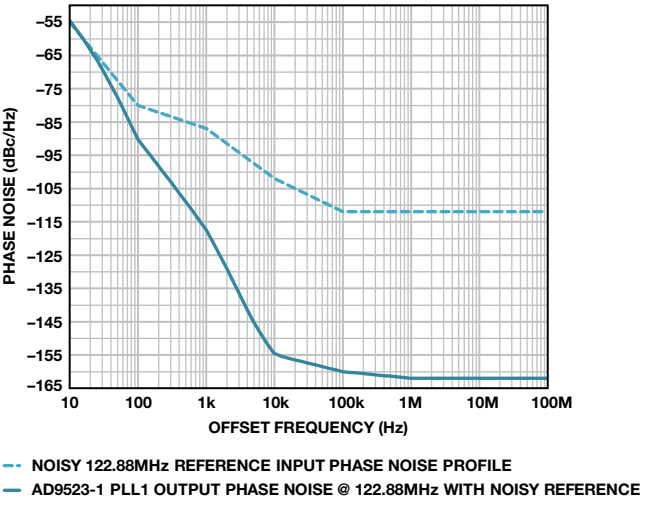



Figure 5. PLL1 output phase noise using jittery reference.

Figure 6 and Figure 7 show the AD9523-1 PLL1 output with 6 dB and 12 dB higher phase noise than the noisy reference shown in Figure 2. Beyond an offset frequency of about 20 kHz, PLL1's output phase noise is dominated by its loop settings and the VCXO's performance. Thus, with an integration range starting from a 20-kHz offset, jitter performance will only change slightly, despite the 12 dB increase in reference input phase noise. This is a direct result of designing PLL1 to have a low loop bandwidth and using a low phase noise VCXO. A low-frequency, high-performance VCXO with a low $K_{VCO}$ must be used to create a PLL1 loop bandwidth small enough to perform this jitter cleaning.

The low phase noise output of PLL1 now serves as the reference to PLL2 to create a phase-aligned, higher-frequency output.

PLL2 contains an internal VCO centered at 3 GHz to allow output frequencies of up to 1 GHz. To compare the noisy input reference with the overall phase noise of the AD9523 family, examine the resultant phase noise at 122.88 MHz ($F_{VCO}$ divided by 24). Note that PLL2's outputs are normally used for frequency translations or high-frequency outputs. Table 3 shows the PLL2 configuration parameters entered into ADIsimCLK. Table 4 shows the PLL2 loop filter values generated by ADIsimCLK given these settings.

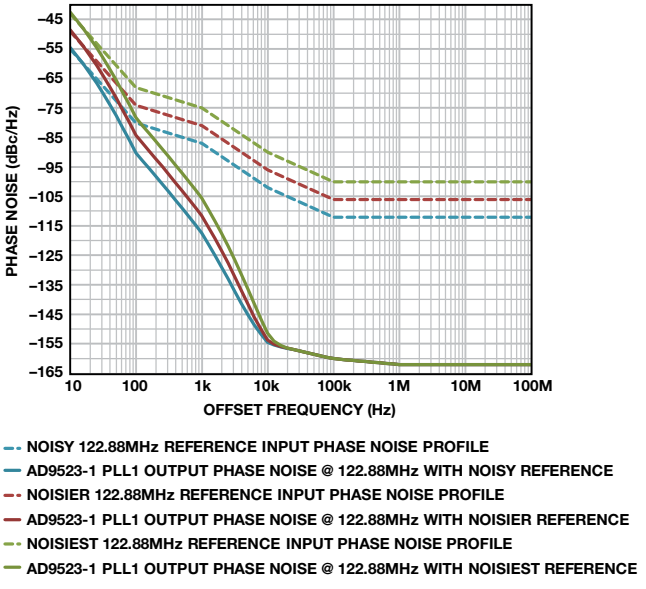



Figure 6. PLL1 output phase noise using various references.

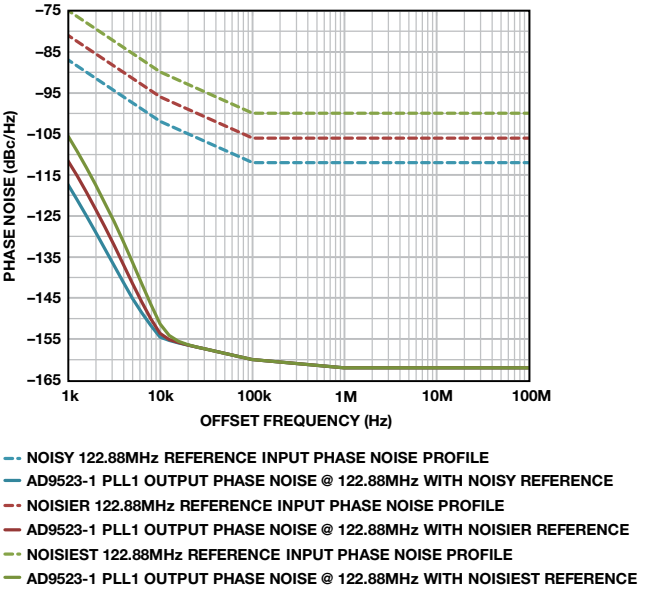



Figure 7. Zoomed PLL1 output phase noise using various references.

**Table 3. PLL2 Configuration Parameters**

| Variable | Value |
|---|---|
| VCO Operating Frequency | 2949.12 MHz |
| Reference Frequency from PLL1 | 122.88 MHz |
| Doubler Enabled? | Yes |
| Output Frequency | 122.88 MHz |
| R Divider | 1 |
| N Divider | 12 |
| M1 Divider | 3 |
| Output Divider | 8 |
| Charge Pump Current | 417 µA |
| Desired Loop BW | 450 kHz |
| Desired Phase Margin | 70° |

**Table 4. PLL2 Loop Filter Component Values from ADIsimCLK**

| Variable | Value |
|---|---|
| $C_{POLE1}$ | 16 pF |
| $R_{ZERO}$ | 1.85 kΩ |
| $C_{EXT}$ | 1.2 nF |
| $R_{POLE2}$ | 900 Ω |
| $C_{POLE2}$ | 16 pF |

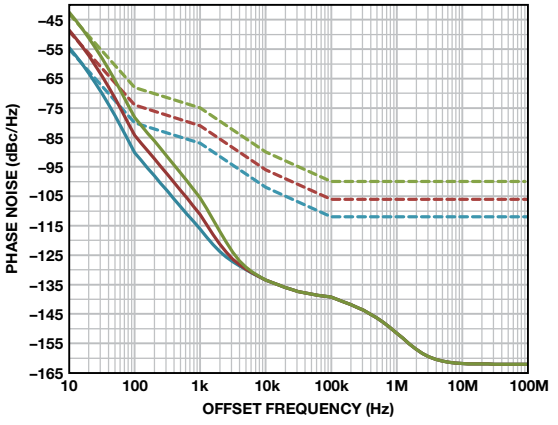



Figure 8. PLL2 output phase noise using various references.

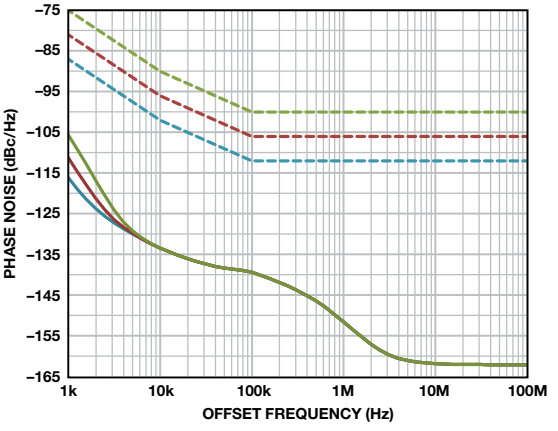



Figure 9. Zoomed PLL2 output phase noise using various references.

Figure 8 and Figure 9 compare each reference input phase noise with the resultant output phase noise from the AD9523-1 as simulated with ADIsimCLK. Notice the added phase noise pedestal between 10 kHz and 1 MHz. This is due to the internal VCO phase noise of PLL2.

The internal VCO phase noise in PLL2 is high enough after about 5 kHz offset frequency that it begins to dominate the overall output phase noise of the device. The added reference phase noise has minimal effect on output phase noise after the 5 kHz offset region.

## Conclusion

The jitter cleaning aspect of PLL1 prevents most of the reference input phase noise from reaching PLL2. A noisy reference input does affect close-in phase noise (sub 10 kHz offset), but the overall output jitter of the device is dominated by the performance of the device, rather than the performance of the reference. In cases where integrated jitter is calculated from 12 kHz to 20 MHz, output jitter will likely be the same regardless of input jitter. Rather than claiming how much jitter a dual-loop analog PLL can attenuate, the real performance measure should be how much jitter it generates.

## Author

**Kyle Slightom** [kyle.slightom@analog.com] is a product applications engineer in the Clocks and Signals Group in Greensboro, NC. He joined ADI in 2012 after graduating from North Carolina State University with a bachelor's degree in electrical engineering.

# Electromagnetic Flow Meters Achieve High Accuracy in Industrial Applications

By Li Ke and Colm Slattery

### Introduction

Industrial applications ranging from oil refineries to vending machines require precision measurements of temperature, pressure, and flow to control complex and simple processes. Within the food industry, for example, the accurate control of flow when filling bottles and cans can directly influence profits, so flow measurement errors must be minimized. Similarly, custody transfer applications, such as the exchange of raw and refined petroleum between tanks and tankers in the oil industry, require high-accuracy measurements. This article presents an overview of flow meter technologies, focusing on electromagnetic flow meters, which are among the most accurate for liquid flow measurement.

Figure 1 shows a basic process control system that uses a flow meter and actuator to control liquid flow rate. At the lowest level, process variables such as temperature, flow rate, and gas concentration are monitored via an input module that is typically part of a programmable logic controller (PLC). The information is processed locally by a proportional-integral-derivative (PID) loop. Using this information, the PLC sets the output to control the process in a steady state. Process data, diagnostics, and other information can be passed up to the operations level, and commands, parameters, and calibration data can be passed down to the sensors and actuators.

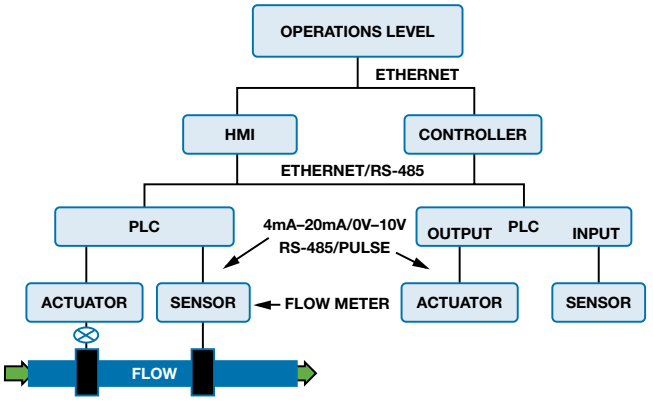



Figure 1. Basic system for measuring and controlling liquid flow rate.

Many different technologies are used to measure flow rate, including differential pressure, Coriolis, ultrasound, and electromagnetic. Differential pressure flow meters are the most common, but they are sensitive to pressure changes in the system. Coriolis flow meters can provide the highest accuracy, up to 0.1%, but they are large and expensive. Ultrasonic flow meters are reasonably small and low cost, but have limited accuracy (0.5% typical). Ultrasonic flow meters use a noninvasive measurement technique that improves reliability and minimizes degradation of the sensing element over time, but they can't be used with dirty or contaminated liquids.

Electromagnetic flow meters also offer noninvasive sensing. They can be used with acidic, alkali, and ionized fluids with electrical conductivities ranging from 10 S/m to $10^{-6}$ S/m, and with clean, dirty, corrosive, erosive, or viscous liquids and slurries, but are not suited for use in hydrocarbon or gas flow measurement. They can achieve relatively high system accuracies (0.2%) at low and high volume flow rates with a minimum diameter of about 0.125 inches and a maximum volume of about 10 cubic feet, and the readings remain repeatable at even slower velocities. They can measure bidirectional flow, either upstream or downstream. Table 1 compares several common flow meter technologies.

Electromagnetic flow meters use Faraday's law of electromagnetic induction, which states that a voltage will be induced in a conductor moving through a magnetic field. The liquid serves as the conductor; the magnetic field is created by energized coils outside the flow tube. The magnitude of the induced voltage is directly proportional to the velocity and type of conductor, the diameter of the tube, and the strength of the magnetic field, as shown in Figure 2.

Mathematically, we can state Faraday's law as $E = kBLV$

where V is the velocity of a conductive fluid, B is the magnetic field strength, L is the spacing between the pickup electrodes, E is the voltage measured across the electrodes, and k is a constant. B, L, and k are either fixed or can be calibrated, so the equation reduces to $E \propto V$.

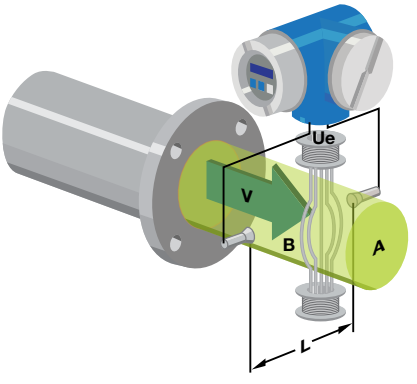



Figure 2. Electromagnetic flow meter.

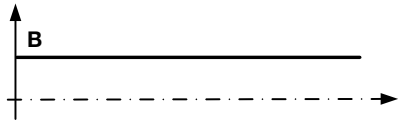
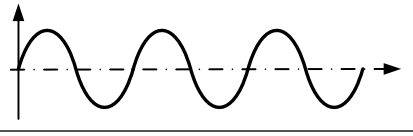
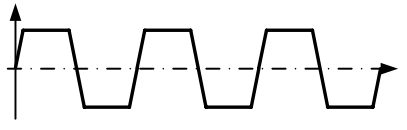
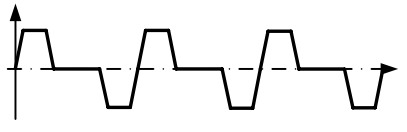
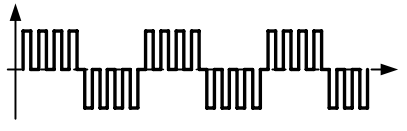
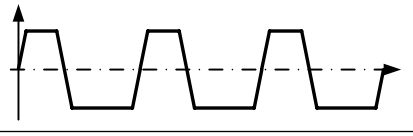
**Table 1. Industrial Flow Meter Technologies**

| | Electromagnetic | Differential Pressure | Ultrasound | Coriolis |
|---|---|---|---|---|
| **Measurement Technique** | Faraday's law of electromagnetic induction | Differential: capacitive or bridge based | Transducer/sensor cross correlation, time to digital, Doppler | Differential phase |
| **Average Accuracy** | 0.2%–1% | 0.5%–2% | 0.3%–2% | 0.1% |
| **Average Cost** | $300–$1000 | $300–$1000 | $300–$1000 | $3000–$10000 |
| **Advantages** | No moving parts<br>Useful with corrosive liquids<br>Bidirectional flow measurement | No moving parts<br>Versatile, can be used for liquids/gases | No moving parts<br>Versatile, can be adopted post-installation | Versatile, can be used for nearly all liquids/gases<br>Independent of pressure and temperature |

A current passing through the field coils of a solenoid generates a controlled magnetic field. The particular excitation waveform is an important aspect of electromagnetic flow meters, and many types are used, including low-frequency rectangle wave, power-line frequency sine wave, dual frequency wave, and programmable pulse width. Table 2 shows various sensor coil excitation waveforms.

Most applications use a low-frequency dc rectangle to excite the sensor coil at 1/25, 1/16, 1/10, 1/8, 1/4, or 1/2 of the power-line frequency (50 Hz/60 Hz). Low-frequency excitation uses a constant amplitude, alternating direction current to achieve low zero drift. The direction of current flow is switched with a transistor or MOSFET H-bridge. When SW1 and SW4 are on, and SW2 and SW3 are off (Figure 3a), the sensor coil is excited in the positive phase; and the constant current enters EXC+ and exits EXC–. When SW1 and SW4 are off, and SW2 and SW3 are on (Figure 3b), the sensor coil is excited in the negative phase; and the constant current enters EXC– and exits EXC+.

**Table 2. Sensor Excitation Types, Waveform, and Features**

| Excitation Type | Waveform | Features |
|---|---|---|
| DC Current Excitation |  | Used since 1832. Used in liquid state metal flow measurement in nuclear energy industry. No polarization, but eddy current. |
| AC Sine Wave |  | Used since 1920. Commercialized in 1950. Low polarization voltage, electromagnetic disturbance, zero-point drift. |
| Low Frequency DC Rectangle |  | Used since 1975. Frequency is 1/16–1/2 of power-line frequency. Low zero-point drift, less immune to noisy serofluid. |
| Tri-State Low Frequency DC |  | Used since 1978. Calibrate zero point during absence of excitation current. Low power. Duty cycle is 1/2 that of rectangle. |
| Dual Frequency |  | Modulate 1/8 power-line frequency with a higher frequency. Can minimize serofluid noise. Low zero-point drift. Fast response. Complex operation. |
| Programmable Pulse Width |  | Use microprocessor to control excitation pulse width and frequency. Immune to serofluid noise. |

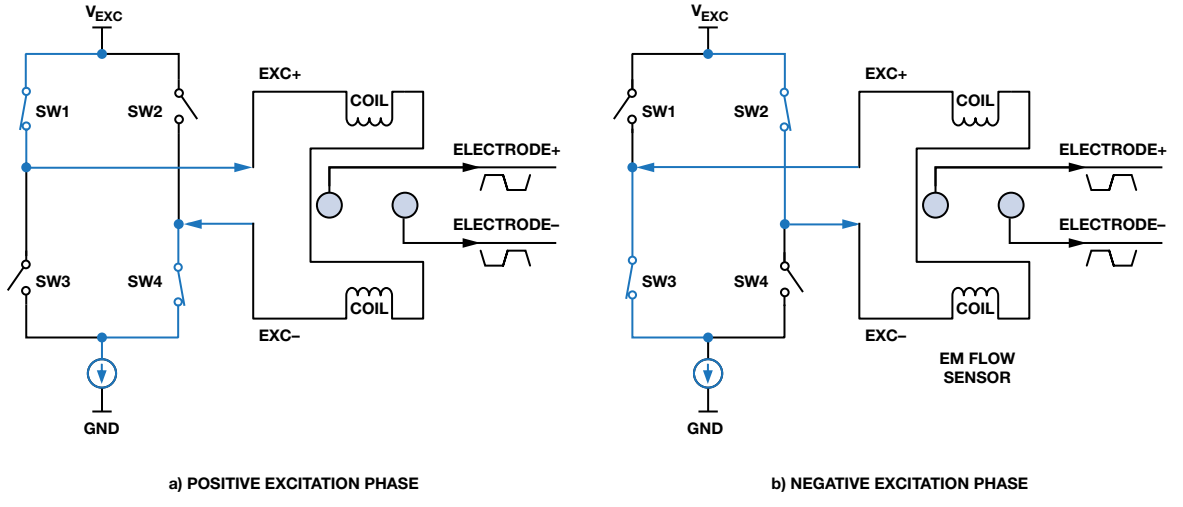



Figure 3. An H-bridge controls the sensor coil excitation phase.

Excitation currents for electromagnetic flow meters tend to be quite large relative to other flow techniques, with 125 mA to 250 mA covering a majority of ranges for line-powered flow meters. Current up to 500 mA or 1 A would be used for larger diameter pipes. Figure 4 shows a circuit that can generate a precision 250 mA sensor coil excitation. The ADR3412 8-ppm/°C voltage reference provides a 1.2-V set point to bias the current.

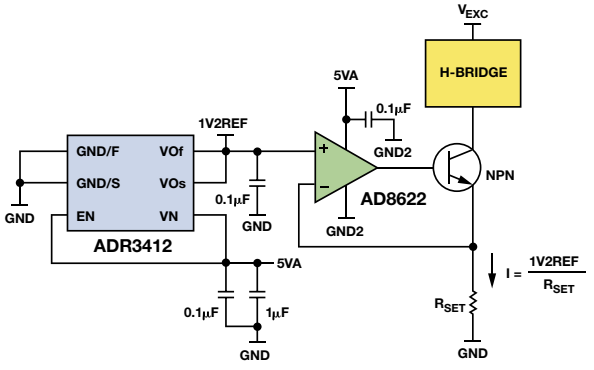



Figure 4. Linear regulated current sink.

Although this traditional method for current excitation using the reference, amplifier, and transistor circuit provides good performance with low noise, it suffers from significant power loss due to the linear drop of the large current across a large voltage. It thus needs heat sinks that add to system cost and area. A constant current sink with switch-mode power supply is becoming a more popular way to excite the sensor coil. Figure 5 shows the ADP2441 synchronous step-down dc-to-dc regulator configured to provide a constant current output. This technique eliminates the losses in standard current sinks and greatly improves system performance.

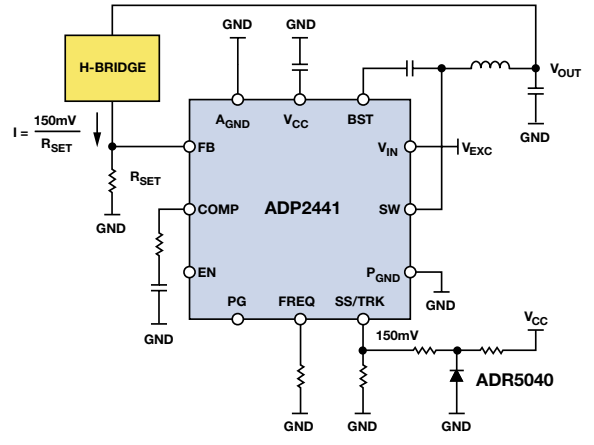



Figure 5. Switch-mode constant current excitation circuit.

Higher power systems use a current sense diagnostic function to monitor current variation over load, power supply, time, and temperature; and can also detect open sensor coils. The AD8219 current shunt amplifier can be used to monitor the excitation current with 60 V/V gain and 0.3% accuracy over an 80-V common-mode range. An isolated current amplifier using the AD7400A isolated Σ-Δ modulator and the AD8646 rail-to-rail op amp is shown in Figure 6. The AD7400 output is processed through a 4th-order low-pass filter to reconstruct the sensed output.

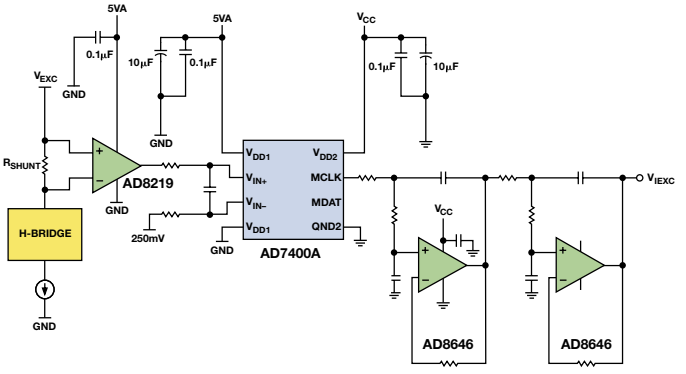



Figure 6. Isolated excitation current monitoring.

The electrode or sensing element is also an important consideration. The two main measurement techniques are capacitive, with electrodes mounted outside of the tube; or, more commonly, with the electrodes inserted through the tube, flush with the liquid.

Many different material options are available, each with unique characteristics including temperature drift, corrosion rate, and electrode potential. The best combination uses a high-temperature material (>100°C) with a low corrosion rate (<0.02 inches per year). Table 3 shows some representative sensor materials and their standard voltage potentials.

**Table 3. Sensor Materials and Voltage Potentials**

| Metal | Standard Voltage Potential (V) | Metal | Standard Voltage Potential (V) |
|---|---|---|---|
| **Magnesium** | –2.34 | **Nickel** | –0.25 |
| **Beryllium** | –1.70 | **Lead** | –0.126 |
| **Aluminum** | –1.67 | **Copper** | +0.345 |
| **Manganese** | –1.05 | **Silver** | +0.800 |
| **Zinc** | –0.762 | **Platinum** | +1.2 |
| **Chromium** | +0.71 | **Gold** | +1.42 |

Platinum is a good example of a high-quality electrode material; it has corrosion rates of less than 0.002 inches per year and can operate in environments up to 120°C. The 1.2-V electrode potential of platinum is relatively high, however, and will become the common-mode voltage (CMV) that needs rejection at the sensor output. Stainless steel electrodes have only a couple hundred millivolts of CMV, so the common mode can be more easily rejected. Stainless steel material is widely used with non-corrosive fluids.

Equal potential should appear on both electrodes if they use the same material and have the same surface condition. In reality, however, the polarization potential fluctuates slowly as a low-frequency ac signal because of physical friction or electrochemical effects between the fluid and electrodes. Any mismatch would also show up as differential-mode noise. The bias voltage, together with the electrode potential, presents a common-mode voltage of a few hundred millivolts to about 1 V to the first stage amplifier input, so the electronics must have adequate common-mode rejection. Figure 7 shows the one-electrode potential from a differential system with 0.28 $V_{DC}$ bias and 0.1 V p-p noise on #316 stainless steel electrodes installed on a 50 mm diameter water pipe.

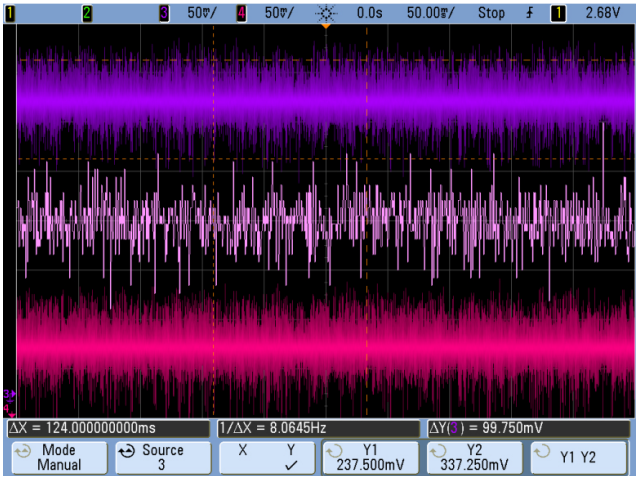



Figure 7. Electrode potential in differential system with 0.28 $V_{DC}$ bias and 0.1 V p-p common-mode noise.

Typical flow rates are in the 0.01 m/s to 15 m/s range—a 1500:1 dynamic range. The sensitivity of a typical line-powered electromagnetic flow meter is 150 µV/(m/s) to 200 µV/(m/s). Thus, a 150 µV/(m/s) sensor will provide a 3 µV p-p output with a 0.01 m/s bidirectional flow. For a 2:1 signal-to-noise ratio, the total input-referred noise should not exceed 1.5 µV p-p. The flow rate changes quite slowly in the dc to low frequency range, so the 0.1 Hz to 10 Hz noise bandwidth is critical. In addition, the sensor's output resistance can be quite high. To satisfy these requirements, the front-end amplifier must have low noise, high common-mode rejection, and low input bias current.

The sensor's common-mode output voltage is attenuated by common-mode rejection of the front-end amplifier. With 120 dB CMR, the 0.28 $V_{DC}$ bias is reduced to 0.28 $\mu V_{DC}$. This offset can be calibrated out or removed by ac coupling the signal. The ac component appears as noise at the amplifier output, degrading the minimum detectable level. With 120 dB CMR, the 0.1 V p-p is reduced to 0.1 µV p-p.

The sensor output resistance varies from a few tens of ohms to $10^7$ Ω depending on the electrode type and fluid conductivity. To minimize loss, the input impedance of the front-end amplifier must be far greater than the output resistance of the sensor. A JFET or CMOS input stage with high input resistance is required. The low bias current and low offset current of the front-end amplifier are key parameters to minimize the current noise and common-mode voltage. Table 4 shows the specifications of several recommended front-end amplifiers.

**Table 4. Specifications of Representative Instrumentation Amplifiers**

| Model | Gain | $Z_{IN}$ | CMR (dB min) DC to 1 kHz, G = 10 | 1/f Noise (µV p-p) | $I_{BIAS}$ (pA) | Power Supply (V) |
|---|---|---|---|---|---|---|
| **AD620** | 1 to 10,000 | $10^9$ Ω \|\| 2 pF | 100 | 0.55 | 500 | ±2.3 to ±18 |
| **AD8220** | 1 to 1000 | $10^{13}$ Ω \|\| 5 pF | 100 | 0.94 | 10 | ±2.25 to ±18 |
| **AD8221** | 1 to 1000 | $10^{11}$ Ω \|\| 2 pF | 110 | 0.5 | 200 | ±2.3 to ±18 |
| **AD8228** | 10, 100 | $10^{11}$ Ω \|\| 2 pF | 100 | 0.5 | 400 | ±2.3 to ±18 |
| **AD8421** | 1 to 10,000 | $3\times10^{10}$ Ω \|\| 3 pF | 114 | 0.5 | 100 | ±2.5 to ±18 |

Figure 8 shows a flow meter using the AD8228 precision instrumentation amplifier. The front-end amplifier rejects the common-mode voltage while amplifying the small sensor signal. Its matched layout and laser-trimmed resistors allow it to provide guaranteed specifications for gain error, gain drift, and common-mode rejection. To minimize leakage current, the high-impedance sensor output can be guarded by sampling the input voltage and connecting the buffered voltage to an unmasked trace around the input signal path.

The first-stage gain is typically 10 to 20, but not higher, because the low-level signal must be amplified for postprocessing while the dc offset is kept small to avoid saturating downstream stages.

The input stage is followed by an active band-pass filter that removes the dc component and sets the gain to fully use the dynamic range of the downstream ADC. The sensor excitation frequency ranges between 1/25 and 1/2 of the power-line frequency, setting the band-pass cutoff frequencies. Figure 9 shows the band-pass filter used in the flow meter.

The first stage is an ac-coupled unity-gain high-pass filter with 0.16 Hz cutoff frequency. Its transfer function is

$$H(\omega) = \frac{j\omega R_{91} C}{1 + j\omega R_{91} C} \cdot \left(1 + \frac{R_{97}/R_{98}}{1 + j\omega R_{97} C_{162}}\right) \cdot \frac{j\omega R_{94} C_{152}}{1 + j\omega R_{94} C_{152}} \cdot \frac{-R_{95}/R_{89}}{1 + j\omega R_{95} C_{160}}$$

The following stages combine with the first to form a complete band-pass filter with 0.37-Hz low-frequency cutoff, 37-Hz high-frequency cutoff, 35.5-dB peak at 3.6 Hz, –40 dB/decade roll-off, and 49-Hz noise equivalent bandwidth. The amplifier chosen for this stage must not contribute additional system noise.

Using the AD8622 low-power precision op amp, which specifies 0.2 µV p-p 1/f noise and 11 nV/√Hz wideband noise, the noise referred to the filter input is 15 nV rms. When referred to the amplifier input, this noise becomes 1.5 nV rms, which can be ignored compared to the ±1.5 µV p-p noise for 0.01 m/s flow rate. Adding together the noise sources from the common-mode voltage, front-end amplifier, and band-pass filter, the root-sum-square noise referred to the AD8228 input is 0.09 µV rms, or about 0.6 µV p-p.

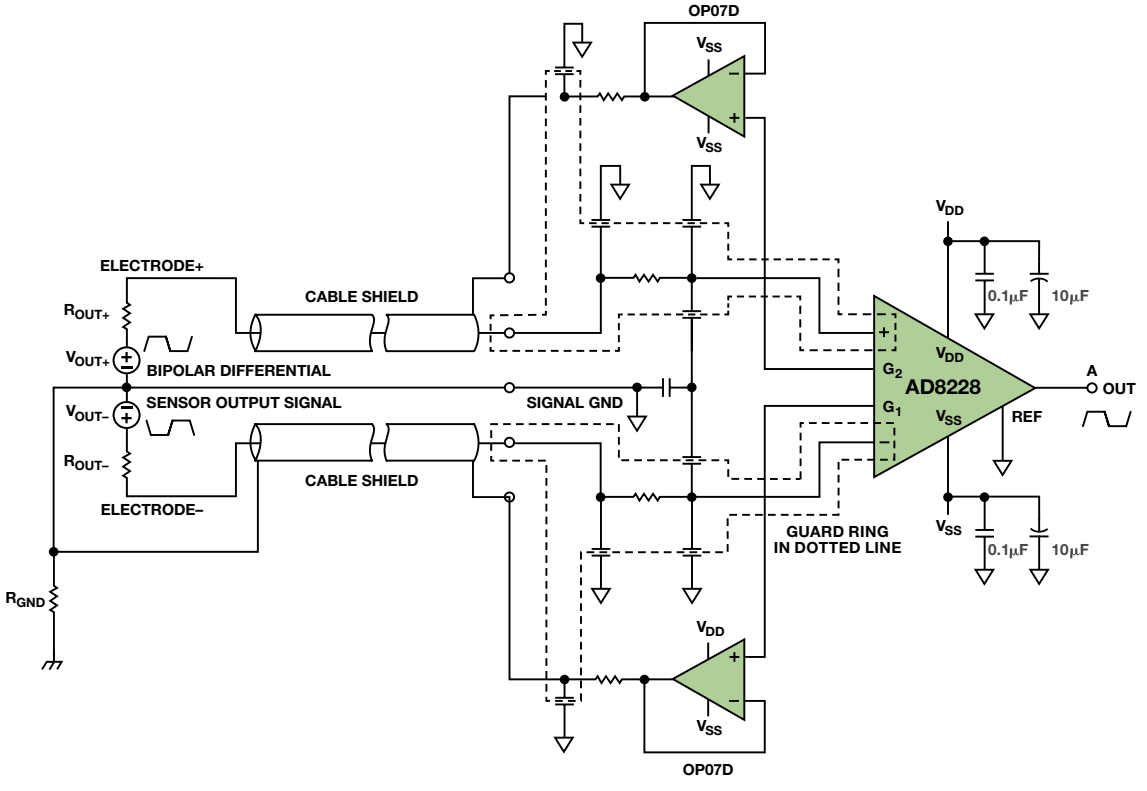



Figure 8. Interface between front-end amplifier and electromagnetic flow sensor.

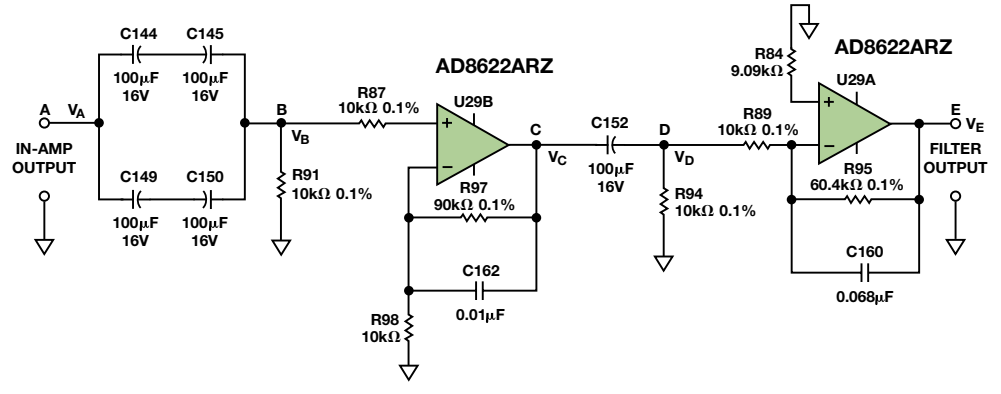



Figure 9. Band-pass filter following the input amplifier.

The filter output contains the flow rate in the amplitude and the flow direction in the phase. The bipolar signal is demodulated with analog switches, hold capacitors, and a difference amplifier, as shown in Figure 10. The analog switches must have low on resistance and medium switching speed. The ADG5412 high-voltage, latch-up proof, quad SPST switches, which feature 9.8 Ω typical $R_{ON}$ and 1.2 Ω $R_{ON}$ flatness, add little gain error or distortion to the signal.

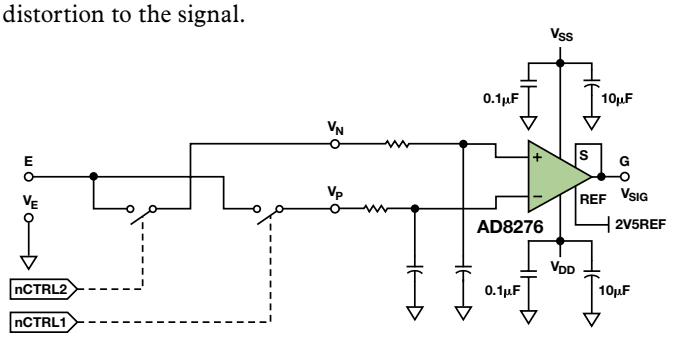



Figure 10. Synchronous demodulation circuit.

The AD8276 low-power, low-cost, unity-gain difference amplifier interfaces to an ADC with a 5-V full-scale input range. Thus, its REF pin is tied to a 2.5-V reference that level shifts the bipolar output to a unipolar range. Outputs above 2.5 V represent forward flow, while outputs below 2.5 V represent reverse flow.

### Selecting the ADC

When determining system error budgets, the sensor generally dominates, and may account for 80% to 90% of the total error. The international standard for electromagnetic flow meters specifies that measurement repeatability should not exceed ⅓ of the maximum system deviation at 25°C and constant flow rate. With a total error budget of 0.2%, the repeatability should not exceed 0.06%. If the sensor accounts for 90% of this budget, the transmitter electronics must have a maximum error of 60 ppm.

To minimize errors, we can average ADC samples. For example, for every five samples, discard the maximum and minimum, and average the remaining three. The ADC would need to get five samples during each settled interval, which occurs during the final 10% of the excitation period. This requires the ADC sampling rate to be at least 50 times the sensor excitation frequency. To accommodate the fastest excitation of 30 Hz, the minimum sampling rate needs to be 1500 Hz. Faster sampling would allow more data samples to be averaged to suppress noise and achieve better accuracy.

These ADC requirements are ideally suited towards Σ-Δ technology, which delivers excellent noise performance at moderate speeds. The AD7192 ultralow noise Σ-Δ ADC is ideal for electromagnetic flow meters, as it specifies 16.5 bit noise-free resolution at 4800 Hz output data rate. Table 5 shows its effective resolution vs. gain and output data rate.

Figure 11 shows the ADC subcircuit, including the demodulator output and the ADR3425 micropower, high-accuracy 2.5-V reference.

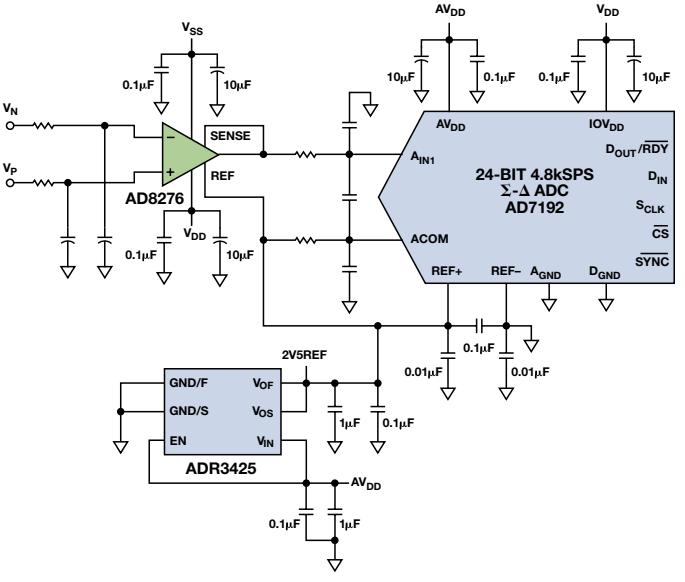



Figure 11. ADC subcircuit.

Some applications, such as beverage filling, need higher frequency sensor excitation. 150 Hz sensor coil excitation allows the filling process to be done in about one second. Noise requirements remain the same, but the ADC must be faster. The AD7176-2 Σ-Δ ADC settles in 20 µs, with 17-bit noise-free resolution at 250 kSPS and 85 dB rejection of 50 Hz and 60 Hz tones.

**Table 5. AD7192 Effective Resolution vs. Gain and Output Data Rate**

| Filter Word (Decimal) | Output Data Rate (Hz) | Settling Time (ms) | Gain of 1[1] | Gain of 8[1] | Gain of 16[1] | Gain of 32[1] | Gain of 64[1] | Gain of 128[1] |
|---|---|---|---|---|---|---|---|---|
| 1023 | 4.7 | 852.5 | 24 (22) | 24 (22) | 24 (21.5) | 24 (21.5) | 23.5 (21) | 22.5 (20) |
| 640 | 7.5 | 533 | 24 (22) | 24 (21.5) | 24 (21.5) | 23.5 (21) | 23 (20.5) | 22.5 (20) |
| 480 | 10 | 400 | 24 (21.5) | 23.5 (21) | 23.5 (21) | 23.5 (21) | 23 (20.5) | 22 (19.5) |
| 96 | 50 | 80 | 22 (19.5) | 22 (19.5) | 22 (19.5) | 22 (19.5) | 21.5 (19) | 21 (18.5) |
| 80 | 60 | 66.7 | 22 (19.5) | 22 (19.5) | 22 (19.5) | 21.5 (19) | 21.5 (19) | 20.5 (18) |
| 40 | 120 | 33.3 | 22 (19.5) | 21.5 (19) | 21.5 (19) | 21.5 (19) | 21 (18.5) | 20.5 (18) |
| 32 | 150 | 26.7 | 21.5 (19) | 21.5 (19) | 21.5 (19) | 21 (18.5) | 21 (18.5) | 20 (17.5) |
| 16 | 300 | 13.3 | 21.5 (19) | 21.5 (19) | 21 (18.5) | 21 (18.5) | 20.5 (18) | 19.5 (17) |
| 5 | 960 | 4.17 | 20.5 (18) | 20.5 (18) | 20.5 (18) | 20 (17.5) | 19.5 (17) | 19 (16.5) |
| 2 | 2400 | 1.67 | 20 (17.5) | 20 (17.5) | 19.5 (17) | 19.5 (17) | 19 (16.5) | 18 (15.5) |
| 1 | 4800 | 0.83 | 19 (16.5) | 19 (16.5) | 19 (16.5) | 18.5 (16) | 18.5 (16) | 17.5 (15) |

[1]The output peak-to-peak (p-p) resolution is listed in parenthesis.

### Analog Signal Chain Testing

The building blocks described here were used to excite and test an electromagnetic flow sensor in a calibration laboratory. The complete front end, including high CMRR input stage, band-pass filter, and gain stage were also tested in a real flow system. Two test boards achieved ±0.2% accuracy on the 1 m/s to 5 m/s range, with a repeatability of 0.055%. This correlates well with industrial standards. The signal chain for an electromagnetic flow meter is shown in Figure 12.

The sensor excitation and measurement dictates overall system performance, as the millivolt signal developed at the electrodes is ultimately converted into a flow result. The flow rate is communicated to the system controller via several protocols, including RS-485 and a 4-mA to 20-mA current loop. Key advantages of the current loop are that it is not affected by the voltage drop in the wiring, can communicate over long distances, and is less susceptible to noise interference than voltage communications. In factory automation applications, digital bus protocols are more common, offering high-speed communications over shorter distances using a differential voltage mode signal. Figure 13 shows a 4-mA to 20-mA signaling circuit with HART® communications. Figure 14 shows an isolated RS-485 solution.

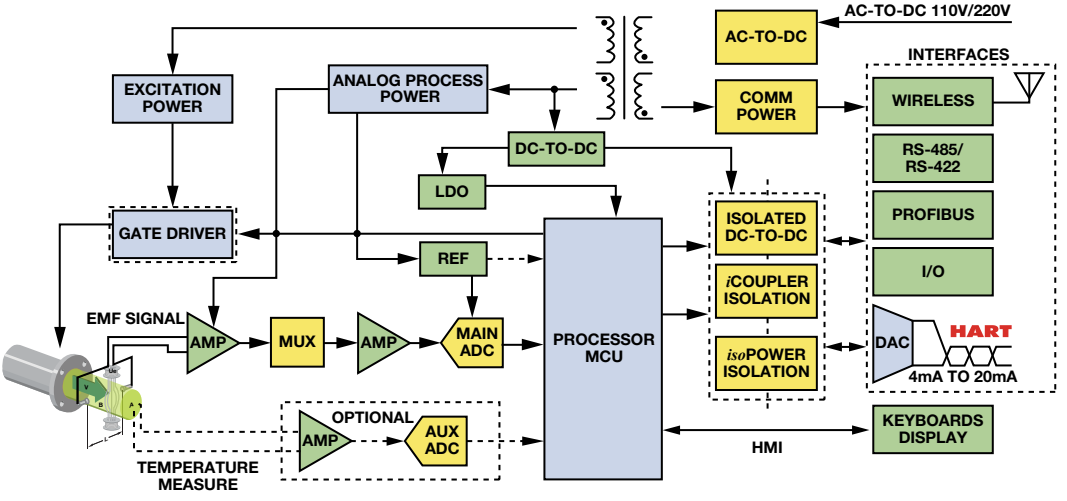



Figure 12. Electromagnetic flow meter.

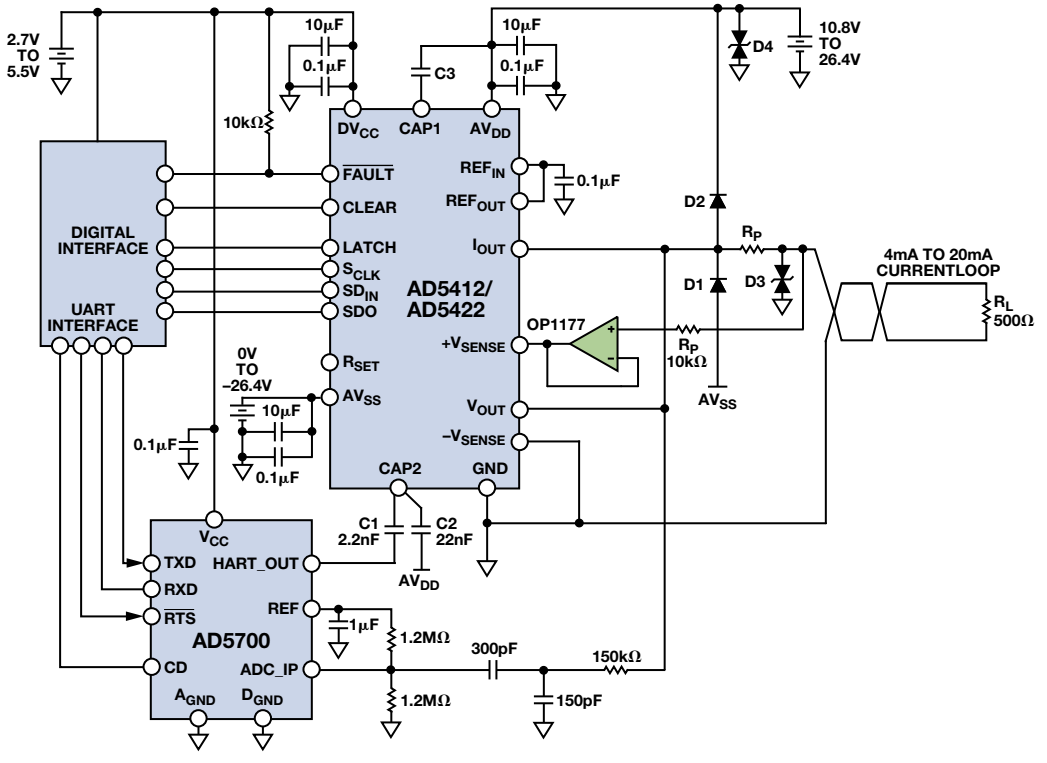



Figure 13. 4-mA to 20-mA current loop with HART.

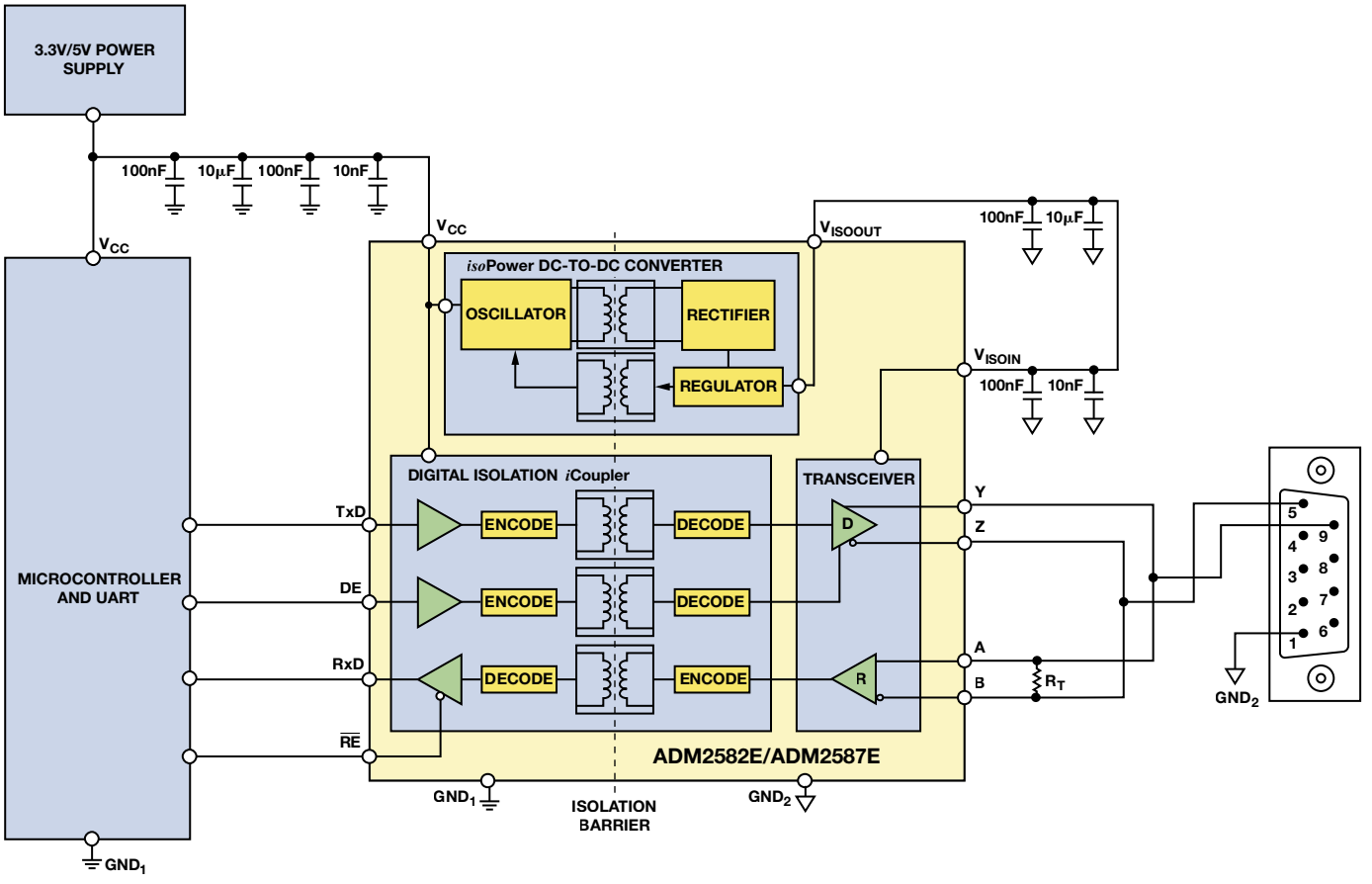



Figure 14. Isolated RS-485 circuit.

To maintain safe voltages at the user interface and to prevent transients from being transmitted from the sources, galvanic isolation is usually required between each communication channel and the system controller. Table 6 shows a list of components that provide the highest levels of integration for these communications standards.

**Table 6. Integrated Circuits for Industrial Data Acqusition**

| Output | Solution | Description | Advantages |
|---|---|---|---|
| 4-mA to 20-mA | AD5410/AD5420 | Single-Channel, 16-Bit, Current Source DAC | Open/short diagnostics. Overtemperature fault<br>Output slew rate control<br>Software-programmable current/voltage ranges |
| 4-mA to 20-mA | AD5412/AD5422 | Single-Channel, 16-Bit, Current Source and Voltage Output DAC, HART Connectivity | Open/short diagnostics. Overtemperature fault<br>Output slew rate control<br>Software-programmable current/voltage ranges |
| 4-mA to 20-mA | AD5750 | Industrial Current/Voltage Output Driver with Programmable Ranges | Open/short diagnostics. Overtemperature fault<br>Output slew rate control<br>CRC error checking<br>Negative current ranges |
| HART | AD5700 | Low-Power HART Modem | 115 µA maximum supply current in receive mode<br>Integrated band-pass filter<br>Minimal external components |
| RS-232 | ADM3251E | Isolated Single-Channel RS-232 Line Driver/Receiver | ESD protection on $R_{IN}$ and $T_{OUT}$ pins<br>±8 kV: contact discharge<br>±15 kV: air gap discharge |
| CAN BUS | ADM3053 | 2.5 kV rms Signal and Power Isolated CAN Transceiver | Current limiting and thermal shutdown features to protect against output short circuits |
| RS-485 | ADM2582E | 2.5 kV Signal and Power Isolated, ±15 kV ESD-Protected, Full-/Half-Duplex RS-485 | Open- and short-circuit, fail-safe receiver inputs<br>Thermal shutdown protection |

*(continued on Page 29)*

# A Deeper Look into Difference Amplifiers

By Harry Holt

### Introduction

The classic four-resistor difference amplifier seems simple, but many circuit implementations perform poorly. Based on actual production designs, this article shows some of the pitfalls encountered with discrete resistors, filtering, ac common-mode rejection, and high noise gain.

College electronics courses illustrate applications for ideal op amps, including inverting and noninverting amplifiers. These are then combined to create a difference amplifier. The classic four-resistor difference amplifier, shown in Figure 1, is quite useful and has been described in textbooks and literature for more than 40 years.

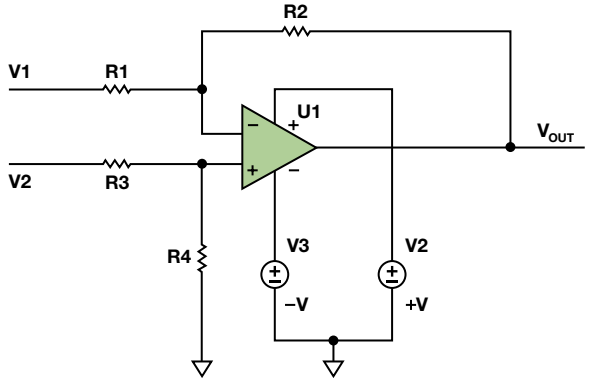



Figure 1. Classic difference amplifier.

The transfer function of this amplifier is

$$V_{OUT} = \left(\frac{R4}{R3+R4}\right) \times \left(\frac{R1+R2}{R1}\right) \times V2 - \frac{R2}{R1} V1 \qquad (1)$$

With R1 = R3 and R2 = R4, Equation 1 simplifies to

$$V_{OUT} = \left(\frac{R2}{R1}\right)(V2 - V1) \qquad (2)$$

This simplification occurs in textbooks, but never in real life, as the resistors are never exactly equal. In addition, other modifications of the basic circuit can yield unexpected behavior. The following examples come from real application questions, although they have been simplified to show the essence of the problem.

### CMRR

An important function of the difference amplifier is to reject signals that are common to both inputs. Referring to Figure 1, if V2 is 5 V and V1 is 3 V, for example, then 4 V is common to both. V2 is 1 V higher than the common voltage, and V1 is 1 V lower. The difference is 2 V, so the "ideal" gain of R2/R1 would be applied to 2 V. If the resistors are not perfect, part of the common-mode voltage will be amplified by the difference amplifier and appear at $V_{OUT}$ as a valid difference between V1 and V2 that cannot be distinguished from a real signal. The ability of the difference amplifier to reject this is called common-mode rejection (CMR). This can be expressed as a ratio (CMRR) or converted to decibels (dB).

In a 1991 article, Ramón Pallás-Areny and John Webster showed that the common-mode rejection, assuming a perfect op amp, is

$$CMRR \cong \frac{A_d + 1}{4t} \qquad (3)$$

where $A_d$ is the gain of the difference amplifier and $t$ is the resistor tolerance. Thus, with unity gain and 1% resistors, the CMRR is 50 V/V, or about 34 dB; with 0.1% resistors, the CMRR is 500 V/V, or about 54 dB—even given a perfect op amp with infinite common-mode rejection. If the op amp's common-mode rejection is high enough, the overall CMRR is limited by resistor matching. Some low-cost op amps have a minimum CMRR in the 60 dB to 70 dB range, making the calculation more complicated.

### Low Tolerance Resistors

The first suboptimal design, shown in Figure 2, was a low-side current sensing application using an OP291. R1 through R4 were discrete 0.5% resistors. From the Pallás-Areny paper, the best CMR would be 64 dB. Luckily, the common-mode voltage is very close to ground, so CMR is not the major source of error in this application. A current sense resistor with 1% tolerance will cause 1% error, but this initial tolerance can be calibrated or trimmed. The operating range was more than 80°C, however, so the temperature coefficient of the resistors must be taken into account.

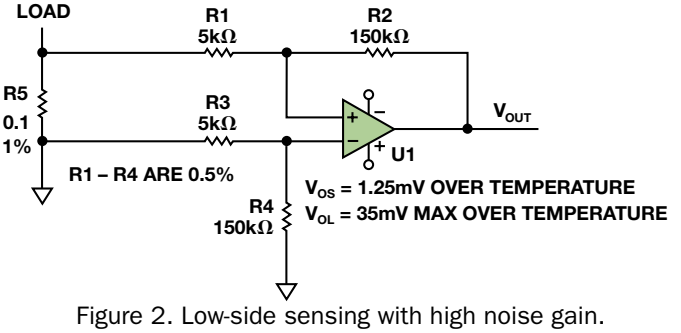



Figure 2. Low-side sensing with high noise gain.

For very low value current shunts, use a 4-terminal, Kelvin sense resistor. With a high-accuracy 0.1-Ω resistor, make the connections directly to the resistor, as a few tenths of an inch of PCB trace can easily add 10 mΩ, causing more than 10% error. But the error gets worse; the copper trace on the PCB has a temperature coefficient greater than 3000 ppm.

The value of the sense resistor must be chosen carefully. Higher values develop larger signals. This is good, but power dissipation ($I^2R$) increases, and could reach several watts. With smaller values, in the milliohm range, parasitic resistance from wires or PCB traces can cause significant errors. To reduce these errors, Kelvin sensing is usually employed. A specialized 4-terminal resistor (Ohmite LVK series, for example) can be used, or the PCB layout can be optimized to use standard resistors, as described in "Optimize High-Current Sensing Accuracy by Improving Pad Layout of Low-Value Shunt Resistors." For very small values, a PCB trace can be used, but this is not very accurate, as explained in "The DC Resistance of a PCB Trace."

Commercial 4-terminal resistors, such as those from Ohmite or Vishay, can cost several dollars or more for 0.1% tolerance with very low temperature coefficients. A complete error budget analysis can show where the accuracy can be improved for the least increase in cost.

One complaint regarding a large offset (31 mV) with no current through the sense resistor was caused by a "rail-to-rail" op amp that couldn't swing all the way to the negative rail, which was tied to ground. The term rail-to-rail is misleading: the output will

get close to the rail—a lot closer than classical emitter follower output stages—but will never quite reach the rail. Rail-to-rail op amps specify a minimum output voltage, $V_{OL}$, of either $V_{CE(SAT)}$ or $R_{DS(ON)} \times I_{LOAD}$, as described in "MT-035, Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues." With a noise gain of 30, the output will be ±1.25 mV × 30 = ±37.5 mV due to offset voltage. But the output can only get down to 35 mV, so the output will be between 35 mV and 37.5 mV for a load current of 0 A. Depending on the polarity of $V_{OS}$, the output could be as big as 72.5 mV with no load current. With a max $V_{OS}$ of 30 µV and a maximum $V_{OL}$ of 8 mV, a modern zero-drift amplifier, such as the AD8539, would reduce the total error to the point that the error due to the sense resistor would dominate.

### Another Low-Side Sensing Application

The next example, shown in Figure 3, had a lower noise gain, but it used a low-precision quad op amp, with 3-mV offset, 10-µV/°C offset drift, and 79 dB CMR. An accuracy of ±5 mA over a 0-A to 3.6-A range was required. With a ±0.5% sense resistor, the required ±0.14% accuracy cannot be achieved. With a 100-mΩ resistor, ±5 mA throughput creates a ±500-µV drop. Unfortunately, the op amp's offset voltage over temperature is 10 times greater than the measurement. Even with $V_{OS}$ trimmed to zero, a 50°C change would consume the entire error budget. With a noise gain of 13, any change in $V_{OS}$ will be multiplied by 13. To improve performance, use a zero-drift op amp, such as the AD8638, ADA4051, or ADA4528, a thin-film resistor array, and a higher precision sense resistor.

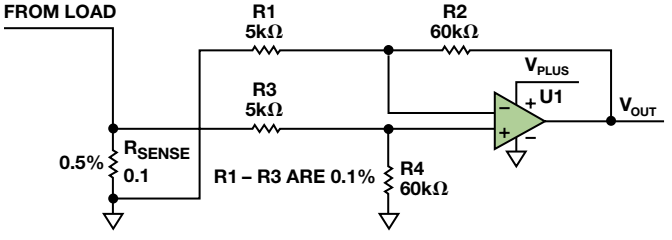



Figure 3. Low-side sensing, example 2.

### High Noise Gain

The design shown in Figure 4 attempts to measure high-side current. The noise gain is 250. The OP07C op amp specifies 150-µV max $V_{OS}$. The maximum error is 150 µV × 250 = 37.5 mV. To improve this, use the ADA4638 zero-drift op amp, which specifies 12.5 µV offset from −40°C to +125°C. With high noise gains, however, the common-mode voltage will be very close to the voltage across the sense resistor. The input voltage range (IVR) for the OP07C is 2 V, meaning that the input voltage must be at least 2 V below the positive rail. For the ADA4638, IVR = 3 V.

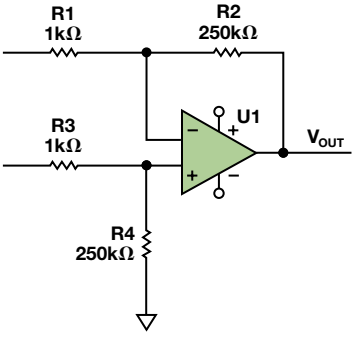



Figure 4. High-side current sensing.

### Single Capacitor Roll-Off

The example shown in Figure 5 is a little more subtle. So far, all of the equations focused on the resistors; but, more correctly, the equations should have referred to impedances. With the addition of capacitors, either deliberate or parasitic, the ac CMRR depends on the ratio of impedances at the frequency of interest. To roll off the frequency response in this example, capacitor C2 was added across the feedback resistor, as is commonly done for inverting op amp configurations.

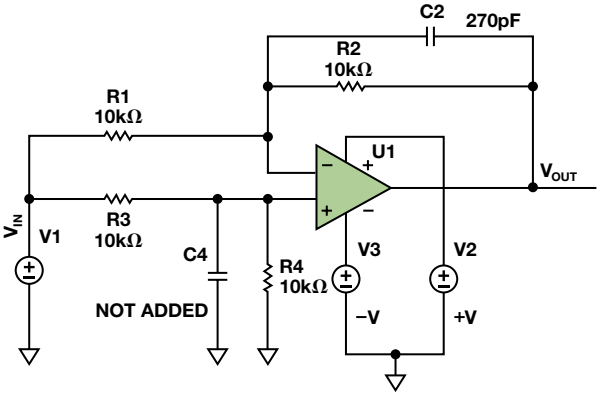



Figure 5. Attempt to create a low-pass response.

To match the impedance ratios Z1 = Z3 and Z2 = Z4, capacitor C4 must be added. It's easy to buy 0.1% or better resistors, but even 0.5% capacitors can cost more than $1.00. At very low frequencies the impedance may not matter, but a 0.5-pF difference on the two op amp inputs caused by capacitor tolerance or PCB layout can degrade the ac CMR by 6 dB at 10 kHz. This can be important if a switching regulator is used.

Monolithic difference amplifiers, such as the AD8271, AD8274, or AD8276, have much better ac CMRR because the two inputs of the op amp are in a controlled environment on the die, and the price is often lower than that of a discrete op amp and four-precision resistors.

### Capacitor Between the Op Amp Inputs

To roll off the response of the difference amplifier, some designers attempt to form a differential filter by adding capacitor C1 between the two op amp inputs, as shown in Figure 6. This is acceptable for in-amps, but not for op amps. $V_{OUT}$ will move up and down to close the loop through R2. At dc, this isn't a problem, and the circuit behaves as described in Equation 2. As the frequency increases, the reactance of C1 decreases. Less feedback is delivered to the op amp input, so the gain increases. Eventually, the op amp is operating open loop because the inputs are shorted by the capacitor.

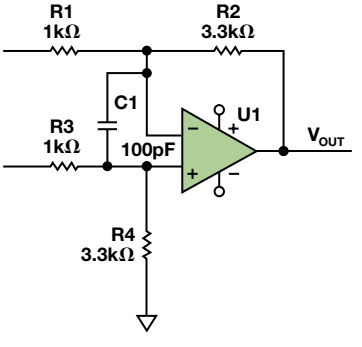



Figure 6. Input capacitor decreases high-frequency feedback.

On a Bode plot, the open-loop gain of the op amp is decreasing at –20 dB/dec, but the noise gain is increasing at +20 dB/dec, resulting in a –40 dB/dec crossing. As taught in control systems class, this is guaranteed to oscillate. As a general guideline: never use a capacitor between the inputs of an op amp. (There are very few exceptions, but they won't be covered here.)

## Conclusion

The four-resistor difference amplifier, whether discrete or monolithic, is widely used. To achieve a solid, production worthy design, carefully consider noise gain, input voltage range, impedance ratios, and offset voltage specifications.

## References


Kitchin, Charles and Lew Counts. *A Designer's Guide to Instrumentation Amplifiers*, 3rd edition. Analog Devices, Inc., 2006. Page 2-1.

Miller, Eric M. The DC Resistance of a PCB Trace.

O'Sullivan, Marcus. "Optimize High-Current Sensing Accuracy by Improving Pad Layout of Low-Value Shunt Resistors." *Analog Dialogue*, Volume 46, Number 2, 2012.

Pallás-Areny, Ramón and Webster, John G. Common Mode Rejection Ratio in Differential Amplifiers. *IEEE Transactions On Instrumentation and Measurement*, Volume 40, Number 4, August 1991. Pages 669–676.

MT-035 Tutorial. *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues*.


## Author


**Harry Holt** [harry.holt@analog.com] is a senior applications engineer in ADI's Central Applications Group. Previously, he worked five years in the Precision Amplifiers Group, following 27 years in both field and factory applications at National Semiconductor, where he was responsible for a variety of products, including data converters, op amps, references, audio codecs, and FPGAs. Harry has a BSEE degree from San Jose State University; he is a Life Member of Tau Beta Pi and a Senior Member of the IEEE.



*(continued from Page 26)*


## Conclusion

Electromagnetic flow meters are among the most common types of flow technologies used today. They dominate in liquid flow measurement and are particularly popular in Europe due to the focus on waste management systems. The main trends are towards PCB area reduction and higher performance. The system performance is dictated by the analog input block, necessitating a high-impedance, low-noise, high-CMRR input amplifier and a low-noise, high-resolution Σ-Δ ADC. Future trends will dictate the need for even faster ADCs. The AD719x family of ADCs suits current system-level requirements, while the AD7176 family is well positioned to meet future requirements. ADI's portfolio of high-efficiency dc-to-dc regulators, integrated communications, high-resolution ADCs, precision amplifiers, and high-accuracy voltage references will allow designers to exceed these requirements in new designs.

## Authors


**Li Ke** [ke.li@analog.com] joined Analog Devices in 2007 as an applications engineer with the Precision Converters product line, located in Shanghai, China. Previously, he spent four years as an R&D engineer with the Chemical Analysis group at Agilent Technologies. Li received a master's degree in biomedical engineering in 2003 and a bachelor's degree in electric engineering in 1999, both from Xi'an Jiaotong University. He has been a professional member of the Chinese Institute of Electronics since 2005.



**Colm Slattery** [colm.slattery@analog.com] graduated in 1995 from the University of Limerick, Ireland, with a bachelor's degree in electronic engineering. After working in test development engineering at Microsemi, he joined Analog Devices in 1998. He spent three years in an applications role in Shanghai and is currently working as a system applications engineer for the Industrial and Instrumentation segment.

# Notes

# Notes

**Analog Devices, Inc.**
**Worldwide Headquarters**
Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA 02062-9106
U.S.A.
Tel: 781.329.4700
(800.262.5643,
U.S.A. only)
Fax: 781.461.3113

**Analog Devices, Inc.**
**Europe Headquarters**
Analog Devices, Inc.
Wilhelm-Wagenfeld-Str. 6
80807 Munich
Germany
Tel: 49.89.76903.0
Fax: 49.89.76903.157

**Analog Devices, Inc.**
**Japan Headquarters**
Analog Devices, KK
New Pier Takeshiba
South Tower Building
1-16-1 Kaigan, Minato-ku,
Tokyo, 105-6891
Japan
Tel: 813.5402.8200
Fax: 813.5402.1064

**Analog Devices, Inc.**
**Asia Pacific Headquarters**
Analog Devices
5F, Sandhill Plaza
2290 Zuchongzhi Road
Zhangjiang Hi-Tech Park
Pudong New District
Shanghai, China 201203
Tel: 86.21.2320.8000
Fax: 86.21.2320.8222



M02000481-0-4/14

**www.analog.com/analogdialogue**

ANALOG DEVICES