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Analog Dialogue

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ANALOG DEVICES

Editor's Notes

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An Introduction to MEMS Vibration Monitoring

Inertial MEMS sensors play a significant role in the massive expansion of today's personal electronic devices. Their small size, low power, ease of integration, high level of functionality, and superb performance encourage and enable innovation in gadgets such as smartphones, gaming controllers, activity trackers, and digital picture frames; and their high reliability and reduced cost allows them to be deployed in most automotive safety systems. (Page 3)

Complex Power-Supply Sequencing Made Easy

Power-supply sequencing is required for microcontrollers, FPGAs, DSPs, ADCs, and other devices that operate from multiple voltage rails. This article discusses the advantages and disadvantages of using discrete components to sequence the power supplies, and describes a simple, yet effective, method of achieving sequencing by using the internal precision enable pins of the ADP5134. (Page 6)

Creative Compensation Enables Tiny Amplifier to Drive 200-mW Loads

Some amplifiers must deliver a moderate amount of power to a load while maintaining dc accuracy. A precision op amp can drive loads requiring less than 50 mW, and a compound amplifier can drive loads requiring watts, but no good solution exists in the middle of the range. Either the op amp can't drive the load, or the circuit becomes large, complex, and expensive. (Page 9)

Simple Circuit Allows Backward Compatibility for Digital Power Controllers

Digital power control enables system configuration through the power management bus. Its advanced control algorithms improve performance, and its programmability allows application optimization. As digital power management replaces many analog controllers, it must maintain backward compatibility so that both digital power modules and analog power modules can operate in the same system. (Page 13)

Capacitance-to-Digital Converter Facilitates Level Sensing in Diagnostic Systems

In blood analyzers, in-vitro diagnostic systems, and other chemical-analysis applications, fluids must be moved between vessels to aspirate samples from cuvettes or reagents from bottles. These lab-based systems frequently handle numerous samples, so minimizing processing time is essential. This article demonstrates a novel use of CDCs to sense fluid levels with a high degree of confidence. (Page 16)

Current-Output Circuit Techniques Add Versatility to Your Analog Toolbox

Current mirrors and current sources offer advantages in a number of situations, including analog current-loop signaling in high-noise environments and level shifting an analog signal across a large potential difference without the use of optical or magnetic-isolation techniques. This article summarizes some of the techniques available and suggests a number of useful circuits. (Page 19)

Scott Wayne [scott.wayne@analog.com]

PRODUCT INTRODUCTIONS: VOLUME 48, NUMBER 2

Data sheets for all ADI products can be found by entering the part number in the search box at www.analog.com.

April

ADC, dual, 16-bit, 1-MSPS, successive-approximation..... **AD7902**

Clock/Data Recovery, continuous-rate, 6.5-Mbps to 8.5-Gbps..... **ADN2913**

Controller, digital, isolated dc-to-dc power supplies **ADP1055**

DACs, 12-/14-/16-bit, 2-ppm/°C reference..... **AD5691R/AD5692R/AD5693R**

Transceiver, agile RF..... **AD9364**

May

Clock Translator, 4-input, 8-output, adaptive, multiservice line cards..... **AD9554**

Front-End, analog, controller for testing/monitoring battery cells **AD8451**

Integrated Power Solution, high-efficiency, multicell Li-Ion batteries **ADP5080**

Regulator, dual 1-A, 18-V, synchronous step-down **ADP2311**

June

ADC, 12-bit, 2.0-GSPS, pipelined..... **AD9625**

ADC, dual, 14-bit, 1-GSPS, pipelined **AD9680**

Amplifier, power, 2.5-W, Class-D, boost converter **SSM4567**

Clock/Data Recovery, continuous-rate, 8.5-Mbps to 11.3-Gbps..... **ADN2917**

Comparator, quad, accurate reference voltage **ADCMP396**

Front-End, mixed-signal (MxFE®) **AD9993**

LNA, 3-GHz, variable-gain, 500-mW driver amplifier..... **ADL5246**

Modulator, 16-bit, isolated, Σ-Δ **AD7403**

Modulator, quadrature, wideband, fractional-N PLL, four VCOs **ADRF6720**

Processors, embedded, Blackfin® **ADSP-BF51xF16**

Regulators, buck, dual, 3-MHz, 800-mA **ADP5133**

Synthesizer, PLL, integer-N/fractional-N **ADF4155**

Analog Dialogue

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An Introduction to MEMS Vibration Monitoring

By Mark Looney

Introduction

Inertial MEMS sensors play a significant role in the massive expansion of today's personal electronic devices. Their small size, low power, ease of integration, high level of functionality, and superb performance encourage and enable innovation in gadgets such as smartphones, gaming controllers, activity trackers, and digital picture frames. In addition, inertial MEMS sensors have substantially improved reliability and reduced cost in automotive safety systems, allowing them to be deployed in most automobiles.

The continuous advancement in functional integration and performance has also helped MEMS accelerometers and gyroscopes find their way into many different industrial systems. Some of these applications offer lower-cost alternatives to present products and services, while others are integrating inertial sensing for the very first time. Vibration monitoring is emerging as an application that has both types of users. Traditional instruments that monitor machine health for maintenance and safety often use piezoelectric technology. High-speed automation equipment monitors vibration to trigger feedback control of lubrication, speed, or belt tension—or to shut down equipment for quick attention from maintenance staff.

Although piezoelectric devices have a mature user base, MEMS accelerometers offer easy integration and reduced cost to an emerging group of new users. In addition, their advanced functional integration allows devices such as the ADIS16229 digital MEMS vibration sensor with embedded RF transceiver to provide a complete solution including signal processing and communications. This type of programmable device can wake itself up periodically, capture time-domain vibration data, perform a fast Fourier transform (FFT) on the data record, apply user-configurable spectral analysis on the FFT result, offer simple pass/fail results over an efficient wireless transmission, provide access to data and results, and then go back to sleep. New adopters of vibration sensing are finding that quick deployment and the reasonable cost of ownership are good reasons to evaluate fully integrated MEMS devices.

Vibration-Monitoring Applications

When using vibration to observe machine health, the objective is to correlate observable vibration with typical wear-out mechanisms, such as bearings, gears, chains, belts, brushes, shafts, coils, and valves. In a typical machine, at least one of these mechanisms requires regular maintenance. Figure 1 shows three examples of the vibration vs. time relationship for a normal wear-out mechanism. Although it takes time and experience to develop this type of relationship, a well-correlated vibration signature can be a cost-saving alternative to regular maintenance that follows short cycle times. Using actual observations, such as vibration, provides an opportunity to take quick action when warning conditions are detected (red curve), while avoiding premature maintenance on machines that have more life remaining (blue and green curves).

Figure 1 also shows two alarm settings (warning, critical) and three stages of the machine's maintenance cycle (early, middle, end). The warning level defines the maximum vibration during normal operation, where the observed vibration contains no indication of potential hazard for the machine or support staff. When in the normal range, some instruments can support infrequent vibration measurements. The critical level indicates that the asset is at risk of severe damage, creating unsafe conditions for support staff or the environment. Obviously, machine operators want to avoid operation at this level, and typically take the machine off line. When the vibration is above the warning level, but below the critical level, the machine can still perform its task, but it should be observed more frequently and may likely require additional maintenance.

Sometimes, these three zones of operation (normal, warning, critical) can correlate to the three stages of a machine's maintenance cycle: early life, midlife, and end of life, in which case they may influence the vibration monitoring strategy. For example, during early life, an instrument might only require daily, weekly, or monthly observation of key vibration attributes. As it moves into midlife, this might change to hourly observation, and as it approaches end of life, vibration monitoring might occur even more often, especially in cases where people or the asset are at risk. At this stage, machines that monitor vibration using portable equipment will accumulate recurring costs that might become prohibitive when compared to the cost of maintenance. While major assets can justify special attention, many other instruments cannot bear the recurring cost. To complement manual measurements, embedded MEMS-based sensors provide a more cost-effective approach for equipment that requires real-time vibration data.

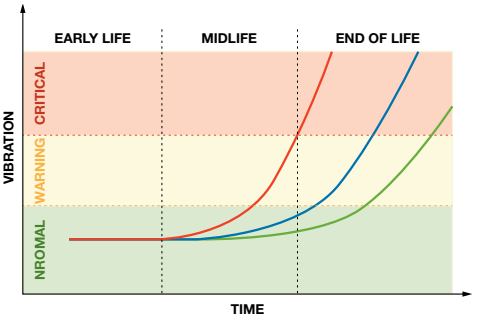

Figure 1. Example vibration vs. time.

Nature of Vibration

Vibration is a repetitive mechanical motion. A number of attributes are important for developing a vibration-sensing instrument. First, an oscillating motion often has both linear and rotational components. Most vibration-sensing relationships tend to focus on the magnitude of the oscillation, not on absolute position tracking, so linear sensors such as MEMS accelerometers are sufficient for capturing motion information. When the motion is mostly linear, understanding the direction can be important, especially when using single-axis sensors. Conversely, a 3-axis sensor can offer more mounting flexibility, as the orthogonal orientation enables pickup on one or more axes regardless of the vibration direction.

Since vibration is periodic, spectral analysis offers a convenient way to characterize the vibration profile (the relationship between vibration magnitude and frequency). The profile shown in Figure 2 has both broadband and narrow-band components, with primary vibration at ~1350 Hz, four harmonics, and some low-level wideband content. Every piece of moving equipment will have its own vibration profile, with the narrow-band response often representing the natural frequencies of the equipment.

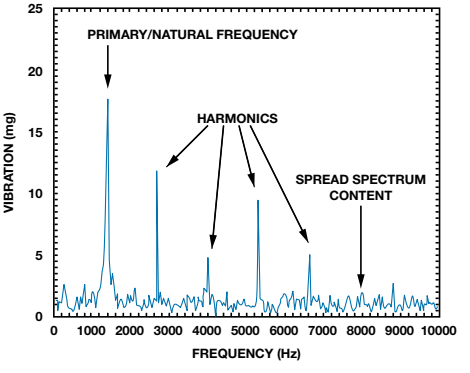

Figure 2. Example vibration profile, natural frequency ~1350 Hz.

Signal Processing

The sensor selection and signal-processing architecture depends on the application's objectives. As an example, the signal chain shown in Figure 3 continuously monitors a specific frequency band, providing warning and critical lights on a nearby control panel. The manufacturer's insight into the mechanical design aids with the band-pass filter design, specifically with the start frequency, stop frequency, and pass-band roll-off rates. Rotation speed, natural frequencies of the mechanical structure, and fault-specific vibration behaviors can all influence the band-pass filter. While this type of approach is simple, vibration-monitoring requirements can change as historical data from a particular machine becomes available. Changes in monitoring requirements can lead to changes in the filter structure, which can present a recurring engineering cost. Developers can trade complexity for flexibility by digitizing the sensor response, implementing key signal processing functions such as filter, rms computation, and level detectors, and leveraging auxiliary I/O outputs to control indicator lights or provide a numerical output.

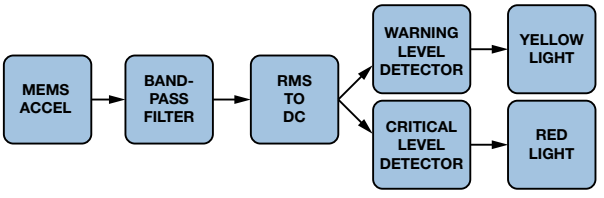

Figure 3. Time-domain vibration signal chain example.

Figure 4 shows a signal chain for the ADIS16228, which uses a digital triaxial vibration sensor with FFT analysis and storage to monitor the spectral content of equipment vibration.

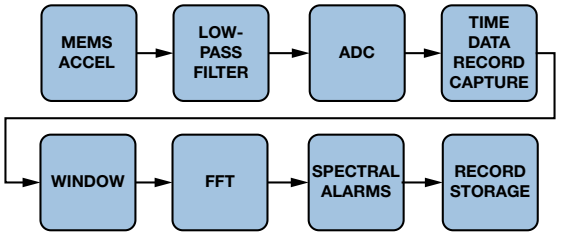

Figure 4. ADIS16228 signal chain for spectral vibration analysis.

Core Sensor

The core sensor for either approach can be a MEMS accelerometer. The most important attributes for selecting a core sensor will be the number of axes, package/assembly requirements, electrical interface (analog/digital), frequency response (bandwidth), measurement range, noise, and linearity. While many triaxial MEMS accelerometers support direct connection with most embedded processors, capturing the best available level of performance might require single- or dual-axis solutions that have analog outputs. For example, the ADXL001 high-performance wideband *i*MEMS® accelerometer leverages its 22-kHz resonance to provide one of the widest available bandwidths, but it is only available as a single-axis, analog-output device. Analog outputs can enable a quick interface in systems that have an available analog-to-digital channel, but the present trend of development seems to favor those sensors that have digital interfaces.

The core sensor's frequency response and measurement range determine the maximum vibration frequency and amplitude that it can support before saturating the output. Saturation degrades the spectral response, creating spurious content that can cause false alarms, even when the saturation frequency does not interfere with a frequency of interest. The measurement range and frequency response are related by

$$A_{p\text{-}p} = D_{p\text{-}p} \times \omega^2$$

where D is the physical displacement, ω is the vibration frequency, and A is the acceleration.

While the frequency response and measurement range place upper boundaries on the sensor's response, its noise and linearity place limits on the resolution. The noise will establish the lower limit of the vibration that will cause a response in the output, while the linearity will determine how much false harmonic content is generated by a vibration signal.

Analog Filter

The analog filter limits the signal content to one Nyquist zone, which represents one half of the sample rate in the example system. Even when the filter cut-off frequency is within the Nyquist zone, it is impossible to have infinite rejection of higher-frequency components, which can still fold back into the pass band. For a system monitoring only the first Nyquist zone, this fold-back behavior can create false failures and distort the view of the vibration content at a particular frequency.

Windowing

Time-coherent sampling is often not practical in vibration-sensing applications, as nonzero sample values at the start and end of the time record result in large spectral leakage, which can degrade the FFT resolution. Applying a window function before calculating the FFT can help manage the spectral leakage. The best window function is dependent on the actual signal, but in general, the trade-offs include process loss, spectral leakage, lobe location, and lobe levels.

Fast Fourier Transform (FFT)

The FFT is an efficient algorithm for analyzing discrete time data. The process transforms a time record into a discrete spectral record, where each sample represents a discrete frequency segment of the Nyquist zone. The total number of output samples is equal to the number of samples in the original time record, which in most cases represents a number in the binomial series (1, 2, 4, 8 …). Spectral data has both magnitude and phase information, which can be represented in either rectangular or polar form. When in rectangular form, one half of the FFT bins contain magnitude information, while the other half contains phase information. When in polar form, one half of the FFT bins contain the real result, while the other half contains the imaginary result.

In some cases, both magnitude and phase information are helpful, but the magnitude/frequency relationship often contains enough information for detecting key changes. For devices that offer only magnitude results, the number of FFT bins is equal to one half of the samples in the original time-domain record. The FFT bin width equals the sample rate divided by the total number of records. In a way, each FFT bin is like an individual band-pass filter in the time domain. Figure 5 provides an example of an actual MEMS vibration sensor, which samples at 20480 samples per second (SPS) and starts with 512-point records. In this case, the sensor only provides the magnitude information, so the total number of bins is 256 and the bin width is equal to 40 Hz (20480/512).

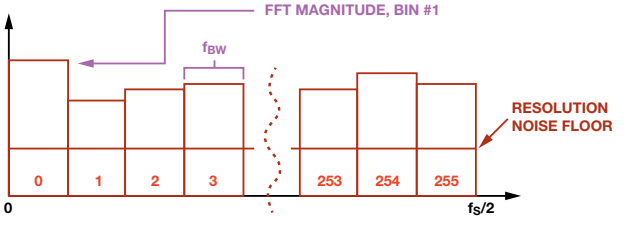

Figure 5. ADIS16228 FFT output.

The bin width is important because it establishes the frequency resolution as the frequency shift from one bin to an adjacent bin, and because it determines the total noise the bin will contain. The total noise (rms) is equal to the product of the noise density (~240 μg/√Hz) and the square root of the bin width (√40 Hz), or ~1.5 mg rms. For low-frequency applications, where noise tends to have the most influence on resolving vibration, a decimation filter prior to the FFT process can help improve the frequency and magnitude resolution without requiring a change in the ADC's sample frequency. Decimating the 20480 SPS sample rate by a factor of 256 enhances the frequency resolution by a factor of 256 while reducing the noise by a factor of 16.

Spectral Alarms

One of the key advantages of using an FFT is that it enables simple application of spectral alarms. Figure 6 provides an example that includes five independent spectral alarms that monitor the natural frequency in the machine (#1), its harmonics (#2, #3, and #4), and the wideband content (#5). The warning and critical levels correspond to the levels in the machine-health vibration vs. time profile. The start and stop frequencies complete the process variable definition represented by this relationship. When using an embedded processor, the spectral alarm definition variables (start/stop frequencies, warning/critical alarm levels) can be in configurable register locations that use digital codes for configuration. Using the same scale factors and bin numbering scheme can greatly simplify this process.

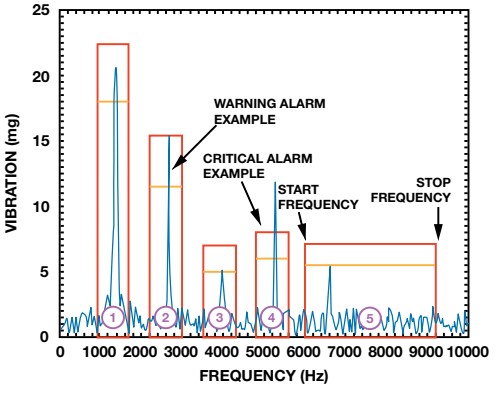

Figure 6. Example FFT with spectral alarms.

Record Management

One of the key functions associated with process-variable relationships is record management. Storing FFT records from different stages of each machine's lifetime enables analysis of a variety of behaviors that may lead to a wear-out curve that contributes to maintenance and safety planning. In addition to compiling historical vibration data, some will find value in capturing condition data associated with parameters such as power supply, temperature, date, time, sample rate, alarm settings, and filtering.

Interface

The interface depends on the existing infrastructure in a particular plant. In some cases, industrial cable-ready communication standards such as Ethernet or RS-485 are readily available, so the interface between a smart sensor and the communication system might be an embedded processor. In other cases, that same embedded processor might be used to interface the smart sensor with an existing wireless protocol, such as Wi-Fi, ZigBee, or a system-specific standard. Some smart sensors, such as the ADIS16000 wireless gateway node for remote sensors and the ADIS16229, come with a ready-to-deploy wireless interface that is available through common embedded interfaces such as SPI or I²C.

Conclusion

Inertial MEMS technology is ushering in a new era of vibration monitoring and is enabling a wider user base for this type of instrumentation. Performance, packaging, and familiarity may contribute to continued use of piezoelectric technology, but vibration monitoring is clearly growing and evolving. Through functional integration and ease of adoption, MEMS devices are gaining increasing attention in new vibration monitoring applications. Convenience, through advanced signal processing at the point of sensing, reduces the monitoring burden to a simple state (normal, warning, critical) for most situations. In addition, remote data access through convenient communication channels is creating new applications for vibration monitoring instruments. Future advances in key performance metrics (noise, bandwidth, and dynamic range) and the high level of functional integration will help this trend to continue in the near future.

References

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Scannell, Bob. MS-2507. *Enabling Continuous and Reliable Process Monitoring with Wireless Vibration Sensors*.

Author

Mark Looney [mark.looney@analog.com] is an *i*Sensor® applications engineer at Analog Devices in Greensboro, North Carolina. Since joining ADI in 1998, he has accumulated experience in sensor-signal processing, high-speed analog-to-digital converters, and dc-to-dc power conversion. He earned a B.S. (1994) and M.S. (1995) degree in electrical engineering from the University of Nevada, Reno, and has published several articles. Prior to joining ADI, he helped start IMATS, a vehicle electronics and traffic-solutions company, and worked as a design engineer for Interpoint Corporation.

Complex Power-Supply Sequencing Made Easy

By Jess Espiritu

Introduction

Power-supply sequencing is required for microcontrollers, FPGAs, DSPs, ADCs, and other devices that operate from multiple voltage rails. These applications typically require that the core and analog blocks be powered up before the digital I/O rails, although some designs may require other sequences. In any case, proper power-up and power-down sequencing can prevent both immediate damage from latch-up and long-term damage from ESD. In addition, sequencing the supplies staggers the inrush current during power-up, an especially helpful technique in applications operating from current-limited supplies.

This article discusses the advantages and disadvantages of using discrete components to sequence the power supplies, and describes a simple, yet effective, method of achieving sequencing by using the internal precision enable pins of the ADP5134, which combines two 1.2-A buck regulators with two 300-mA LDOs. It also shows some sequencer ICs that may be useful for applications that require more accurate and flexible sequencing.

Figure 1 shows an application that requires multiple supply rails. These rails are the core supply (V_{CCINT}), I/O supply (V_{CCO}), auxiliary supply (V_{CCAUX}), and system memory supply.

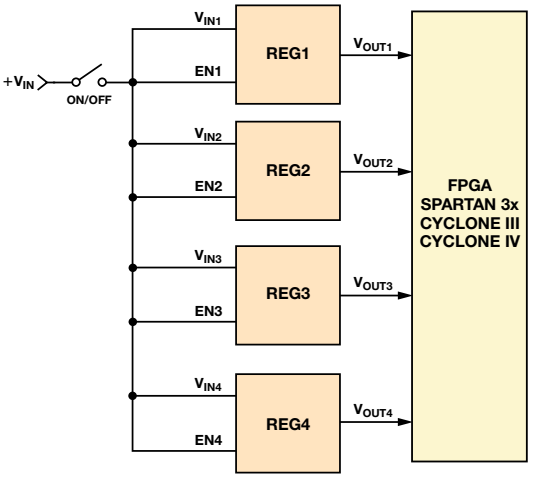

Figure 1. Typical method for powering processors and FPGAs.

As an example, the Xilinx® Spartan-3A FPGA has a built-in power-on reset circuit that ensures that all supplies have reached their thresholds before it allows the device to be configured. This reduces the strict requirement for power sequencing, but to minimize inrush current levels and observe sequencing requirements of circuits attached to the FPGA, the supply rails should be powered up as follows: V_{CC_INT} ⇨ V_{CC_AUX} ⇨ V_{CCO}. Note that some applications require specific sequences, so always read the power requirements section of each data sheet.

Simple Power-Supply Sequencing Using Passive-Delay Networks

A simple way to sequence power supplies is to delay the signal going to a regulator's enable pin with passive components such as resistors, capacitors, and diodes, as shown in Figure 2. When the switch closes, D1 conducts while D2 is left open. Capacitor C1 charges, with the voltage at EN2 rising at a rate determined by R1 and C1. When the switch opens, capacitor C1 discharges to ground through R2, D2, and R_{PULL}. The voltage at EN2 falls at a rate determined by R2, R_{PULL}, and C2. Changing the values of R1 and R2 changes the charging and discharging times, thereby setting the regulator's turn-on and turn-off times.

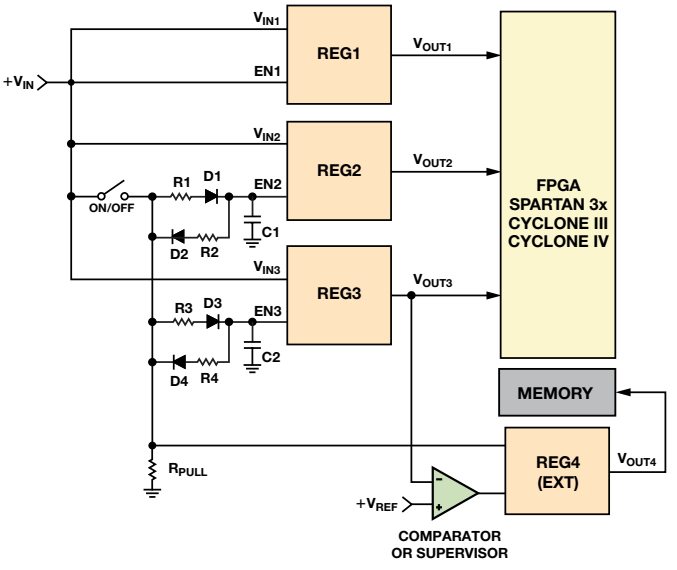

Figure 2. Simple power-supply sequencing method using resistors, capacitors, and diodes.

This method may be useful for applications that don't require precise sequencing, and some applications, where simply delaying signals is sufficient, may require only the external R and C. The disadvantage of using this method with standard regulators is that the logic threshold of the enable pins may vary widely with voltage and temperature. In addition, the delay in the voltage ramp depends on the values and tolerances of the resistor and capacitor. A typical X5R capacitor will vary by about ±15% over the –55°C to +85°C temperature range and another ±10% due to dc bias effects, making the timing imprecise and sometimes unreliable.

Precision Enables Make Sequencing Easy

In order to get stable threshold levels for precise timing control, most regulators require an external voltage reference. The ADP5134 overcomes this problem by integrating a precision reference, saving significant cost and PCB area. Each regulator has an individual enable input. When the voltage at the enable input rises above V_{IH_EN} (0.9 V minimum), the device comes out of shutdown and the housekeeping block is turned on, but the regulator is not activated. The voltage at the enable input is compared to a precise internal reference voltage (0.97 V typical). Once the voltage at the enable pin goes above the precision enable threshold, the regulator is activated and the output voltage starts to rise. The reference varies by only ±3% over input voltage and temperature corners. This small range ensures precise timing control, resolving the issues seen with using discrete components.

When the voltage at the enable input drops 80 mV (typical) below the reference voltage, the regulator is deactivated. When the voltage on all enable inputs drops below V_{IL_EN} (0.35 V maximum), the device enters shutdown mode. In this mode, the current consumption falls to less than 1 µA. Figure 3 and Figure 4 demonstrate the accuracy of the ADP5134 precision-enable thresholds for Buck1 over temperature.

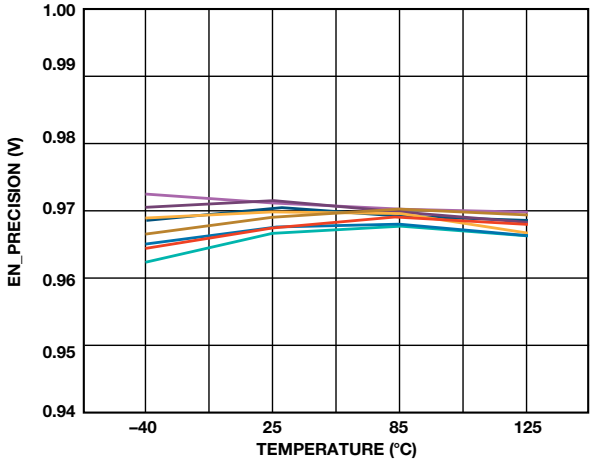

Figure 3. Precision-enable turn-on threshold over temperature, 10 samples.

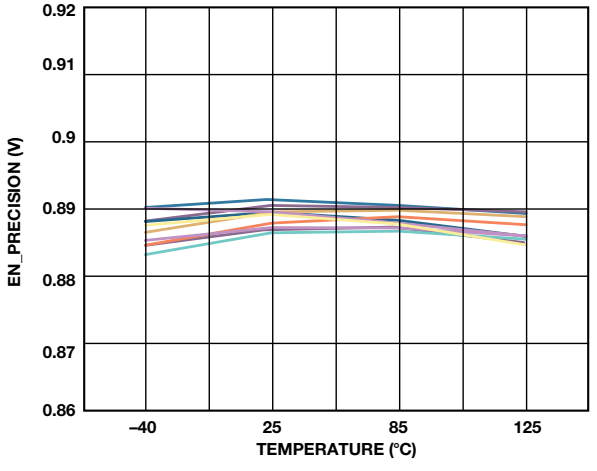

Figure 4. Precision-enable turn-off threshold over temperature, 10 samples.

Simple Power-Supply Sequencing Using Resistor Dividers

Multichannel supplies can be sequenced by connecting an attenuated version of one regulator's output to the enable pin of the next regulator to be powered up, as shown in Figure 5, where the regulators turn on or off sequentially: Buck1 ⇨ Buck2 ⇨ LDO1 ⇨ LDO2. Figure 6 shows the power-up sequence after EN1 is connected to V_{IN1}. Figure 7 shows the power-down sequence after EN1 is disconnected from V_{IN1}.

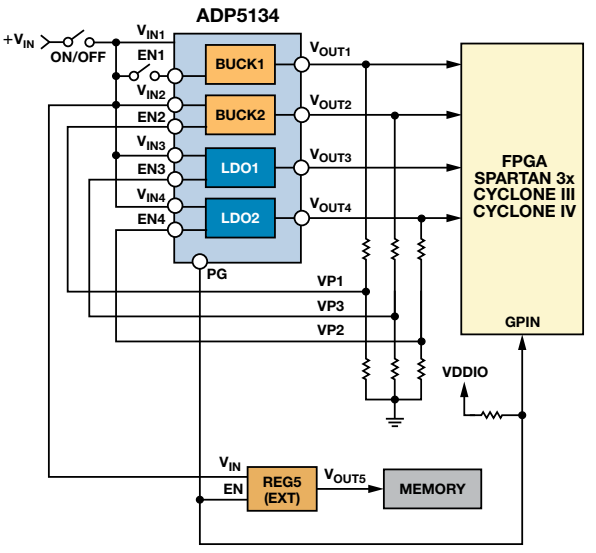

Figure 5. Simple sequencing with the ADP5134.

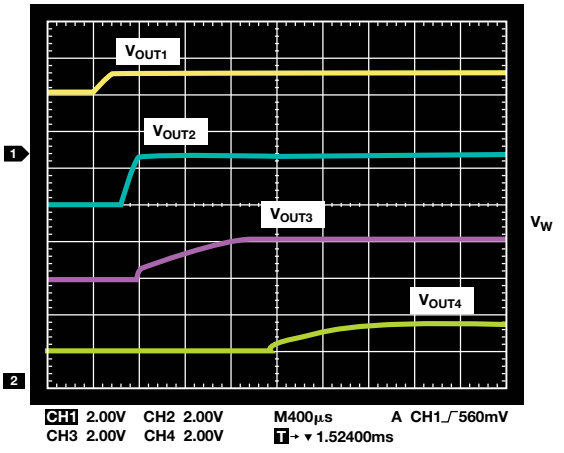

Figure 6. ADP5134 start-up sequence.

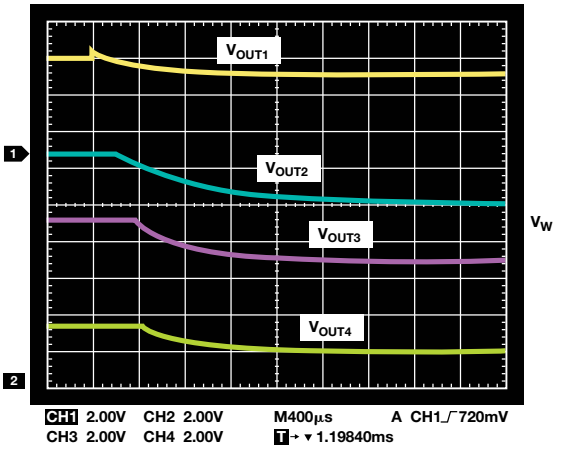

Figure 7. ADP5134 shutdown sequence.

Sequencer ICs Improve Timing Accuracy

In some cases, achieving precise timing is more important than reduced PCB area and cost. For these applications, a voltage monitoring and sequencer IC such as the ADM1184 quad voltage monitor, which offers ±0.8% accuracy over voltage and temperature, can be used. Or, the ADM1186 quad voltage sequencer and monitor with programmable timing may be useful in applications that require more elaborate control of the power-up and power-down sequence.

The ADP5034 4-channel regulator includes two 3-MHz, 1200-mA buck regulators and two 300 mA LDOs. A typical sequencing function can be implemented by using the ADM1184 to monitor the output voltage of one regulator and provide a logic-high signal to the enable pin of the next regulator once the output voltage being monitored reaches a certain level. This method, shown in Figure 8, can be used with regulators that don't provide a precision-enable function.

Conclusion

Sequencing using the ADP5134's precision-enable inputs is simple and easy to implement, requiring only two external resistors per channel. More elaborate sequencing can be achieved by using the ADM1184 or ADM1186 voltage monitors.

References

Application Notes

Murnane, Martin and Chris Augusta. AN-932 Application Note. *Power Supply Sequencing*. Analog Devices, Inc., 2008.

External Resources

Xilinx DS529 Spartan-3A FPGA Family Data Sheet

Product Pages

Power Management

Sequencing

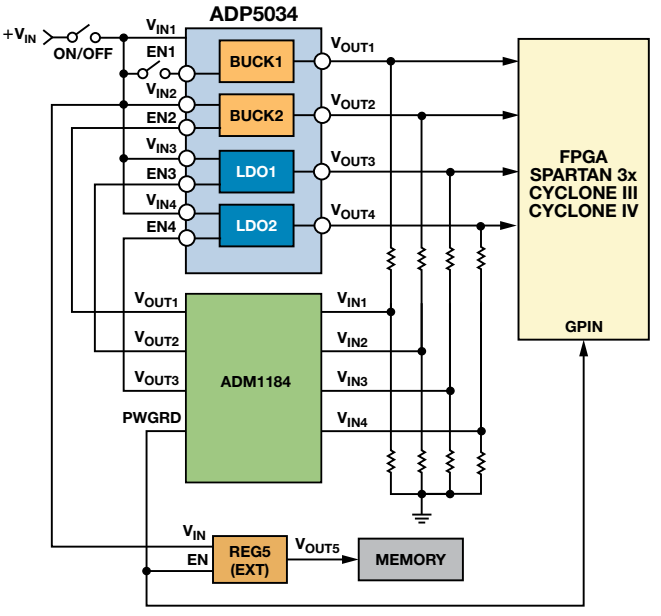

Figure 8. Sequencing the ADP5034 4-channel regulator using the ADM1184 quad voltage monitor.

Author

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Creative Compensation Enables Tiny Amplifier to Drive 200-mW Loads

By Mark Reisiger

Overview

Many applications need an amplifier that delivers a moderate amount of power to a load while maintaining good dc precision, with the size of the load determining the type of circuit required. A precision op amp can drive loads requiring less than 50 mW, and a compound amplifier with a precision-op-amp input stage and discrete-power-transistor output stage can be constructed to drive loads that require watts. However, no good solution exists in the middle of the power range. Either the op amp can't drive the load, or the circuit becomes large, complex, and expensive.

Recently this dilemma arose in the design of a Wheatstone bridge driver. The excitation voltage directly affects the offset and span, so dc precision is required. In this case, the application can tolerate less than 1 mV of error between the source voltage and the bridge. Operating with 7-V to 15-V power supplies, the circuit must drive the bridge with unity gain from 100 mV to 5 V.

To further complicate the problem, a variety of different bridge resistances can be used. Strain gages, for example, have standard impedances of 120 Ω or 350 Ω. With a 120-Ω bridge, the amplifier must source 42 mA to maintain a 5-V bridge drive. In addition, the circuit must be able to drive up to 10 nF. This accounts for both the cable and the bridge decoupling capacitor.

Amplifier Selection

The first step in designing this circuit is selecting an amplifier capable of driving the load. Its dropout voltage (V_{OH}) must be less than the available headroom for the circuit at the required load current. For this design, the minimum power supply is 7 V and the maximum output is 5 V. Providing 250 mV for margin, the available headroom ($V_{DD} - V_{OUT}$) is 1.75 V. The required load current is 42 mA.

The ADA4661-2 precision, dual op amp has rail-to-rail inputs and outputs. Its large output stage is capable of driving significant amounts of current. The data sheet specifies a 900-mV dropout voltage when sourcing 40 mA, so it should easily meet the 1.75-V headroom requirement.

While the dropout voltage limits circuit operation with low-voltage power supplies, power dissipation will limit operation with high-voltage power supplies. The die temperature rise can be calculated to determine the maximum safe operating temperature. The MSOP package simplifies prototyping, but the LFCSP package has much better thermal performance, so it should be used if possible. The thermal resistance (θ_{JA}) is 142°C/W for the MSOP and 83.5°C/W for the LFCSP. The maximum die temperature rise is calculated by multiplying the thermal resistance by the maximum power dissipation. With a 15-V supply and a 5-V output, the headroom is 10 V. The maximum current is 42 mA, which results in 420-mW power dissipation. The resulting die temperature rise (60°C for the MSOP or 35°C for the LFCSP) limits the maximum ambient temperature to 65°C for the MSOP or 90°C for the LFCSP.

The thermal performance of the die and package combination is also critical to maintaining an accurate bridge excitation voltage. Unfortunately, the performance of some op amps is severely degraded when driving large output currents. Power dissipation in the output stage causes large thermal gradients across the die, unbalancing the matched transistors and trim circuitry. The ADA4661-2 was designed to drive significant power while rejecting these thermal gradients.

Feedback Loop Stabilization

Meeting the load-capacitance specification is tricky, as most op amps can't drive 10 nF without external compensation. One classic technique for driving large capacitive loads is to use the multiple feedback topology, as shown in Figure 1, where isolation resistor R_{ISO} shields the amplifier output from load capacitor C_{LOAD}. The dc precision is maintained by feeding back output-signal V_{OUT} through feedback-resistor R_F. The loop stability is maintained by feeding back the amplifier output through capacitor C_F.

For this circuit to be effective, R_{ISO} must be large enough such that the total load impedance looks purely resistive at the amplifier's unity-gain frequency. This is difficult because of the IR drop across this resistor. The maximum size of R_{ISO} can be determined by allocating the remaining voltage headroom in the worst-case conditions. A 6.75-V power supply with a 5-V output allows for 1.75 V of total dropout. The amplifier V_{OH} takes up 900 mV of this, leaving 850 mV left to drop across the resistor. This limits the maximum value of R_{ISO} to 20 Ω. A 2-nF load capacitance places a pole at 4 MHz, which is the unity-gain crossover frequency of this amplifier. Clearly, multiple feedback will not meet the requirements.

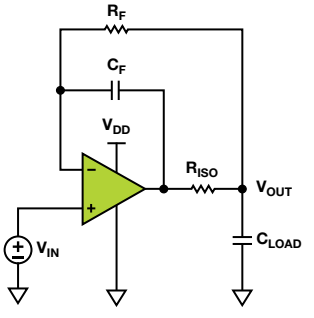

Figure 1. Multiple feedback topology.

A different technique for stabilizing a heavily loaded buffer is to use a hybrid-unity follower topology, as shown in Figure 2. Rather than trying to move the load-capacitance pole, this approach forces the feedback loop to crossover at a lower frequency by reducing the feedback factor. Stability is achieved by forcing the loop to crossover before the phase shift becomes excessive due to the load pole.

The feedback factor is the inverse of the noise gain, so one may conclude that this approach abandons the unity-gain signal path. This would be true if this were a traditional inverting or noninverting configuration, but a closer inspection of the schematic reveals that both inputs are driven. An easy way to think about this circuit is the superposition of an inverting gain of $-R_F/R_S$ and a noninverting gain of $(1 + R_F/R_S)$. The result is a circuit that operates with a signal gain of +1 and a noise gain of $(R_S + R_F)/R_S$. Independent control over the feedback factor and signal gain allows this circuit to stabilize any size load at the expense of circuit bandwidth.

The hybrid unity follower circuit has several drawbacks, however. The first problem is that the noise gain is high for all frequencies, so dc errors such as offset voltage (V_{OS}) are multiplied by the noise gain. This makes achieving the dc specifications extremely challenging. The second drawback requires some knowledge of the internal operation of the amplifier. This amplifier has a three-stage architecture with nested Miller compensation. The output stage has its own fixed internal feedback. This makes it possible for the external feedback loop to be stable while the output stage feedback loop is unstable.

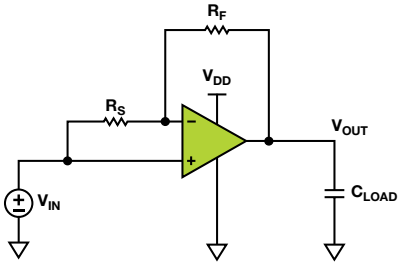

Figure 2. Hybrid-unity follower topology.

By combining the operating principles of both circuits, both issues can be overcome, as shown in Figure 3. Multiple feedback separates low-frequency and high-frequency feedback paths, adding enough capacitive load isolation to minimize output-stage stability problems. The low-frequency feedback is driven from the bridge voltage through feedback-resistor R_F. The high-frequency feedback is driven from the amplifier output through feedback-capacitor C_F.

The circuit also behaves like the hybrid unity follower at high frequency. The high-frequency noise gain, determined by the impedance of the capacitors, is equal to $(C_S + C_F)/C_F$. This noise gain allows the feedback loop to crossover at a low enough frequency where its stability is not degraded by the load capacitance. Since the low-frequency noise gain is unity, the dc precision of the circuit is maintained.

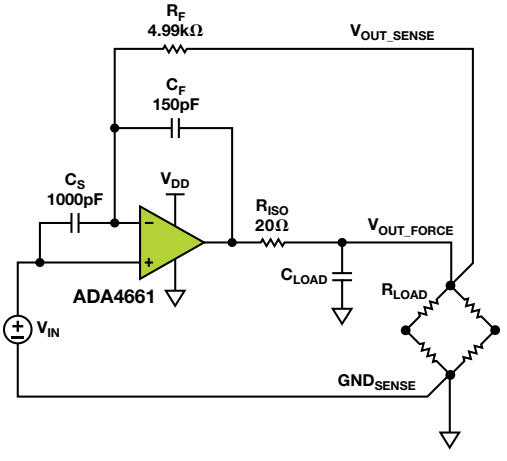

Figure 3. Bridge-driver schematic.

Maintaining the dc precision requires careful attention to the signal routing because of the large currents involved. It only takes 7 mΩ to create a 300 μV drop from the 42-mA maximum load current; this error is as large as the amplifier's offset voltage.

A practical way of dealing with this problem is the 4-wire Kelvin connection, which uses two current-carrying connections (typically called "force") to drive the load current and two voltage-measurement connections (typically called "sense"). The sense connections must be made as close to the load as possible to prevent any load current from flowing in them.

For the bridge-driver circuit, the sense connections should be made directly at the top and bottom of the bridge. None of the PCB traces or cabling should be shared between the force and sense lines. The GND_{SENSE} connection should be routed back to voltage source V_{IN}. For example, if the stimulus is a DAC, then GND_{SENSE} should be connected to REF_{GND} of the DAC. The GND_{FORCE} connection of the bridge should have its own dedicated trace all the way back to the power supply, as allowing bridge currents to flow through a ground plane will generate undesirable voltage drops.

Error Budget

The dc error budget for this circuit, shown in Table 1, is dominated by the amplifier's offset voltage and offset-voltage drift. It assumes a worst-case range of operating conditions. The total error meets the 1-mV requirement by a comfortable margin.

Table 1. Error Budget

Parameter	Conditions	Calculation	Error
Offset Voltage	0 V < V_{CM} < 5 V; 6.75 V < V_{DD} < 15 V		300 μV
Offset-Voltage Drift	0 V < V_{CM} < 5 V; 6.75 V < V_{DD} < 15 V; −40°C < T < +70°C	300 μV/°C × 110°C	341 μV
Power Dissipation	V_{DD} = 15 V; 0 V < V_{CM} < 5 V	Equation 1	168 μV
Gain Error	0 V < V_{CM} < 5 V ; −40°C < T < +125°C	5 V × 1/(105 dB + 1)	27 μV
Power-Supply Rejection	6.75 V < V_{DD} < 15 V	8.25 V/120 dB	8 μV
Total Error			844 μV

The third term in the table is the power-dissipation error. The power dissipated by the amplifier increases the die temperature, which causes the offset voltage to drift from that of ambient temperature with no load current. The worst-case error is calculated with the highest power-supply voltage, highest-output voltage, and smallest resistive load, as shown in Equation 1. Note that the worst-case voltage drop across the amplifier is reduced somewhat by the R_{ISO} resistor.

$$V_{PDISS} = V_{DROP} I_{LOAD} \Theta_{JA} TC_{VOS}$$
$$V_{PDISS} = \left[15V - 5V\left(1 + \frac{20\,\Omega}{120\,\Omega}\right)\right]\left[\frac{5V}{120\,\Omega}\right]\left[142\frac{^{\circ}C}{W}\right]\left[3.1\frac{\mu V}{^{\circ}C}\right] \quad (1)$$
$$V_{PDISS} = 168\,\mu V$$

DC-Measurement Results

The error voltage is the difference between the input voltage, V_{IN}, and the load voltage, V_{OUT}. Figure 4 shows the prototype circuit's error voltage vs. load voltage. The largest error sources in the bridge-driver circuit are the offset voltage and offset-voltage drift. An additional error is dependent on the bridge voltage due to the power dissipation in the amplifier. The effect of power-supply voltage on power dissipation can be seen with the different color curves. The black curve dissipates the smallest amount of power (50 mW) with the minimum supply voltage (7 V). The die temperature rise is only 7°C, so this curve represents the room temperature offset voltage vs. common-mode voltage behavior of this part.

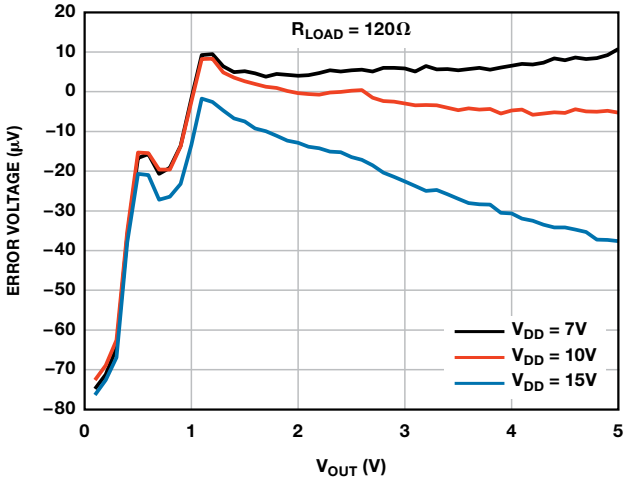

Figure 4. Error voltage vs. output voltage.

The red (10 V) and blue (15 V) curves represent the performance with maximum power dissipation of 175 mW and 385 mW, respectively. As the output voltage increases, the extra power dissipation causes the die temperature to increase by 25°C to 55°C, which causes the offset voltage to drift. The shape of this additional thermal error will be parabolic since the maximum power dissipation occurs when V_{OUT} is one-half of V_{DD}.

The strong dependence of power supply on the offset voltage suggests that the power-supply rejection of this circuit should be considered. Figure 5 shows the error voltage as the supply voltage is swept while the output voltage is fixed. The black curve shows the lightly loaded case, which is dominated by the amplifier's power-supply rejection (PSR). For this device, the 10 µV change represents 118 dB PSR. The red and blue curves show the results when the output dissipates extra power due to being loaded with typical bridge resistances of 350 Ω and 120 Ω. The effective PSRs of the red and blue curves are 110 dB and 103 dB, respectively.

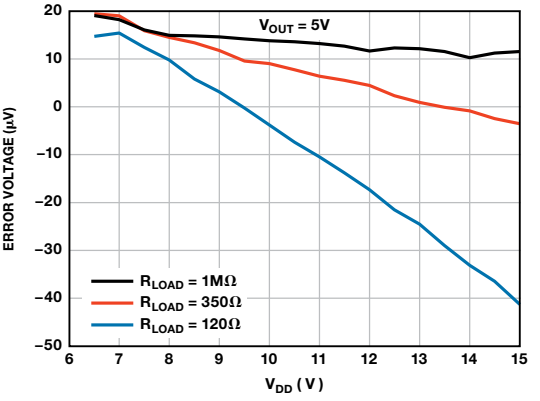

Figure 5. Error voltage vs. supply voltage.

The performance of this circuit clearly depends on the offset drift vs. temperature. So far, the TCV_{OS} specification has been used for all calculations of temperature-dependent error. This assumption must be justified because die temperature increases due to amplifier power dissipation are different than ambient temperature changes. The former creates large thermal gradients across the surface of the die, which can upset the sensitive balance of the amplifier. These gradients can result in offset voltage drifts significantly worse than the data sheet specifications. The ADA4661-2 has been specifically designed to dissipate significant power without degrading its offset-drift performance.

Figure 6 shows the measured offset drift vs. temperature. The specified performance is replicated in the black curve with low power-supply voltages and high-resistance loads (–1.2 µV/°C). The red curve shows the results for a 120-Ω bridge load. The important thing to notice is that the shape of the curve does not change; it is just shifted to the left by the die temperature rise (6.4°C). The blue curve shows the results when the power supply is increased to 15 V—the condition where the circuit's maximum power dissipation can be measured. Once again, the shape of the curve does not change, being shifted left due to the 55°C rise in die temperature. The internal power dissipation is known (385 mW), so the actual thermal impedance (θ_{JA}) of the system can be calculated (143°C/W). It is important to consider the ambient temperature range of operation. The maximum die temperature should not exceed 125°C; this means that the maximum ambient temperature is 70°C for the worst-case load.

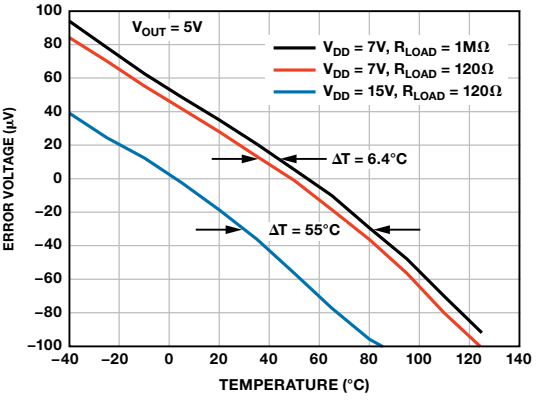

Figure 6. Error voltage vs. ambient temperature.

Transient-Measurement Results

The step response of the circuit is a simple way to evaluate the loop stability. Figure 7 shows the measured step response for a range of capacitive loads for high-resistance bridges; Figure 8 shows the same measurement for low-resistance bridges. The circuit has a characteristic overshoot in the step response due to the pole-zero doublet in the feedback network. This doublet response is fundamental because the circuit's feedback factor drops from unity at low frequency to 0.13 at high frequency. Since the zero is at a higher frequency than the pole, the step response will always overshoot, even with more than adequate phase margin. In addition, the doublet has the longest time constant in the circuit, so it tends to dominate the settling time. The worst-case stability and output stage ringing is seen with high-resistance loads and 1-nF capacitive loads.

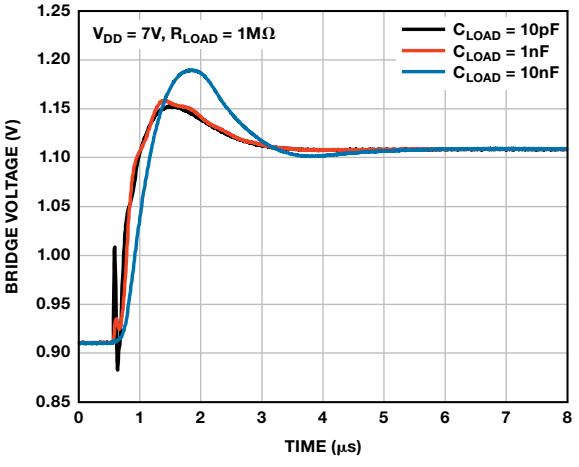

Figure 7. Unloaded step response.

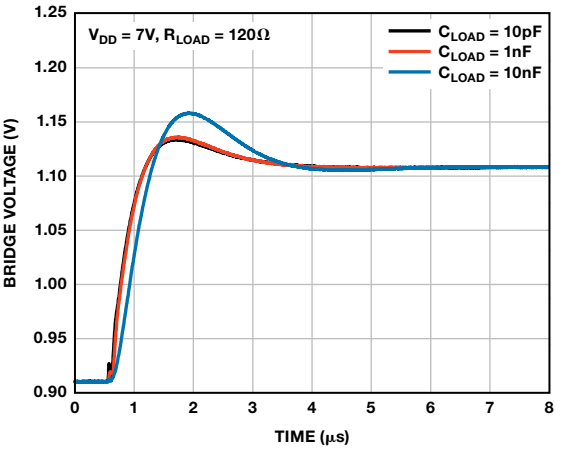

Figure 8. Loaded step response.

Conclusion

The load-driver circuit presented here can apply 5 V to resistive loads as low as 120 Ω with less than 1-mV of total error and stably drive up to 10 nF of total capacitance. The circuit meets its rated performance while operating with a wide range of power supplies from 7 V to 15 V and dissipating almost 400 mW. The basic circuit can be extended to drive positive and negative loads by powering the amplifier with ±7-V power supplies. All of this capability is accomplished with one tiny 3-mm × 3-mm amplifier and four passive components.

Author

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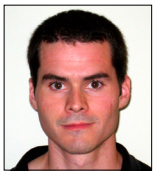

Simple Circuit Allows Backward Compatibility for Digital Power Controllers

By Irvin Ou

Recent progress in the area of very-large-scale integration (VLSI) has broadened the application of digital control, especially in power electronics. Digital control ICs can achieve benefits such as smaller die size, fewer passive components, and reduced cost. Furthermore, digital control enables system configuration through the power management bus (PMBus™); advanced control algorithms improve performance; and programmability allows application optimization. As digital power management becomes increasingly pervasive, replacing many analog controllers, it must maintain backward compatibility with existing features so that both digital power modules and analog power modules can operate in the same system.

Output-voltage trimming is typically used in analog power modules, allowing the end user to change the power module's output voltage via an external resistor. This enhances flexibility by allowing a few select, standard modules to be applied to virtually any application, regardless of the voltage requirements. Figure 1 shows a typical configuration for trimming output voltage in the AGF600-48S30 analog power module.

The output voltage is adjusted by varying the resistance connected to the power module's positive output or ground terminals. The output voltage can be trimmed up (above the nominal output voltage) by connecting external resistor R_{UP} while floating R_{DOWN}, or trimmed down (below the nominal output voltage) by connecting external resistor R_{DOWN} while shorting R_{UP} (resistance equals to zero).

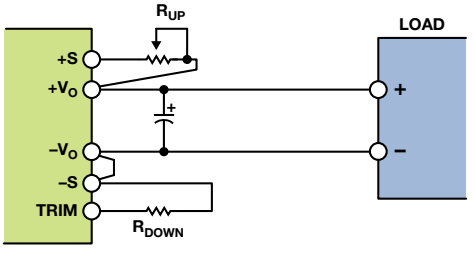

Figure 1. Trimming the output voltage of the AGF600-48S30 dc-to-dc converter.

In the analog solution, R_{UP} and R_{DOWN} change the reference voltage to the error amplifier. The error amplifier senses the output voltage via a resistor divider connected to its inverting input using negative feedback. The output voltage of the error amplifier controls the duty cycle of the drive signals that set the output voltage. The output voltage thus follows the reference voltage, which is changed by R_{UP} or R_{DOWN}, thereby trimming the output voltage up or down.

Figure 2 shows two implementations that are widely adopted in analog power modules. The analog controller shown in Figure 2(a) has a pin that allows external resistor R_{DOWN} to reduce the voltage on the noninverting input of the error amplifier, thus decreasing the output voltage. External resistor R_{UP} is placed in series with the resistive divider to reduce the voltage applied at the inverting input of the error amplifier, thus increasing the output voltage. The analog controller shown in Figure 2(b) doesn't provide access to the internal reference voltage, but an external error amplifier and voltage reference can be added to allow output-voltage trimming. The output of the external amplifier is connected to the output of the internal amplifier, effectively bypassing the internal error amplifier. Then, the voltage reference can be configured with the same circuit as before, allowing both power modules to be trimmed in the same way.

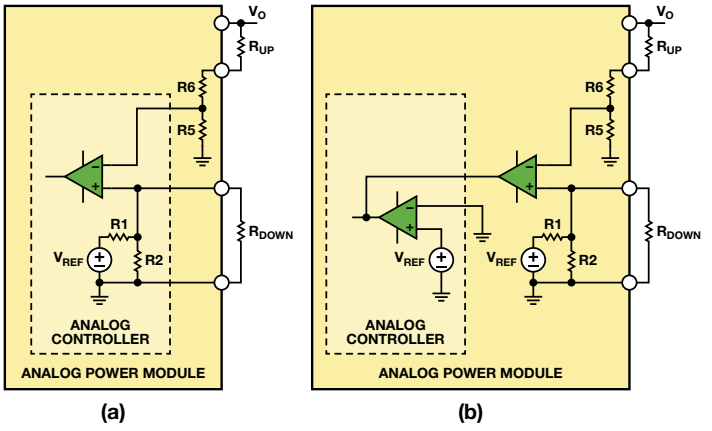

Figure 2. Trimming the output voltage of an analog power module using (a) an analog controller with a configurable internal reference, and (b) an analog controller with a fixed internal reference.

With a digital controller, all of the control functions are implemented using digital logic. Figure 3 shows a functional block diagram of the ADP1051 advanced digital controller with PMBus interface. Ideal for high-density dc-to-dc power conversion, it has six programmable pulse-width modulation (PWM) outputs capable of controlling most high-efficiency power supply topologies. It also controls synchronous rectification (SR) and integrates six analog-to-digital converters (ADCs) that sample the analog input voltage, input current, output voltage, output current, temperature, and other parameters. Once converted into data, these signals are sent to the digital core block for processing. Based on a flexible state machine architecture with all features implemented in hardware, it provides a robust, reliable solution, but it cannot be programmed to implement a function for which it was not inherently designed. All of its functions, including output-voltage trimming, are processed digitally. To trim the output voltage, a command to change the value of the digital reference is sent via the PMBus interface.

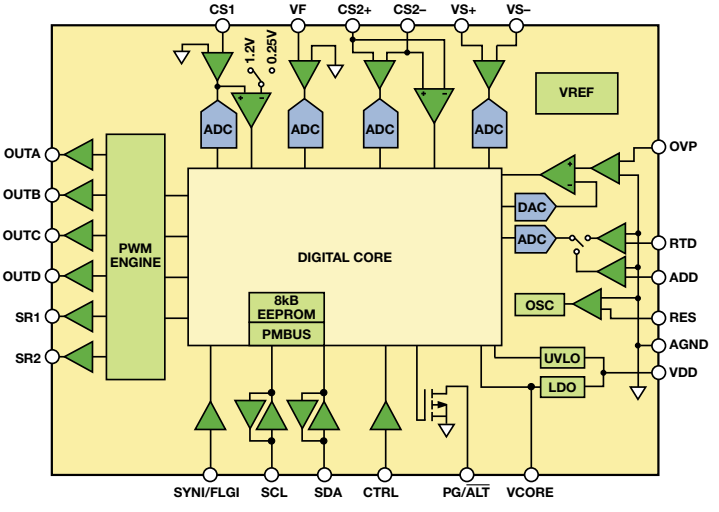

Figure 3. Functional block diagram of the ADP1051 digital controller.

In the control-loop feedback path, the output voltage, scaled by a resistor divider or operational amplifier, is fed to the VS+ pin. An ADC samples this voltage. The digital core knows the programmed output voltage and the digital reference voltage that is set via the PMBus interface. A digital comparator and compensation filter compares the digital reference voltage with the sensed scaled output voltage and generates an error signal that controls the PWMs, just as with the analog controller. Unfortunately, the digital comparator can only use the digital reference voltage via the PMBus. The digital comparator, digital reference voltage, and digital compensation filter all operate with logic-level signals, so it is impossible for them to use an external reference voltage and bypass the internal comparator and filter. Limited by this fixed hardware configuration, the only way to achieve backward compatibility with existing analog trimming functions is to adjust the voltage sensed by the ADC at the VS+ pin. One way do this is to reconfigure the feedback network.

In Figure 4, R_{D1} and R_{D2} form the standard feedback network—a simple resistive divider that scales the output voltage before it is sensed by the ADC. The sensed voltage is

$$V_{-VS+} = \frac{R_{D2}}{R_{D1} + R_{D2}} \times V_O \qquad (1)$$

where V_O is the actual output voltage of the power module. With the standard feedback network, the output voltage cannot be trimmed in the analog way. Reconfiguring the feedback network by adding R_{UP}, R_{T0}, and V_{TRIM}, as shown in Figure 4, allows the scaled output voltage to be adjusted. Now, the sensed voltage is

$$V_{-VS+} = \frac{R_{T0} \,||\, R_{D2}}{R_{D1} + R_{UP} + R_{T0} \,||\, R_{D2}} \times V_O + \frac{(R_{D1} + R_{UP}) \,||\, R_{D2}}{R_{T0} + (R_{D1} + R_{UP}) \,||\, R_{D2}} \times V_{TRIM} \qquad (2)$$

The nominal voltage at the VS+ pin is 1 V. If V_{TRIM} is around 1 V and the value of R_{T0} is relatively large compared with that of R_{D2}, the additional branch can be neglected. The composite network works as a simple divider, and adjusting the resistance of R_{UP} provides a similar characteristic as the analog controller, allowing up-trimming compatibility with analog power modules.

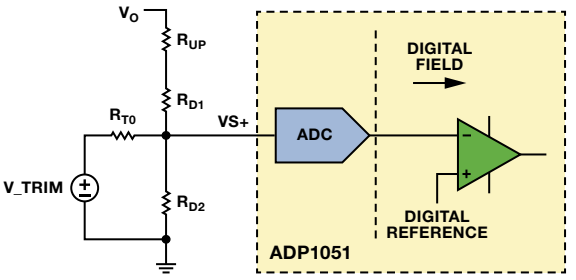

Figure 4. Trimmable feedback network for the ADP1051.

Providing down-trimming compatibility is more complicated, however. The digital controller won't know the exact output voltage that the system should output, so it will try to minimize the error between V_{VS+} and the internal digital reference. V_{VS+} will always follow the internal digital reference, which is typically set at 1 V. Equation 2 shows that V_O and V_{TRIM} have a linear relationship. From Figure 2, the mechanism for trimming the output voltage down is to generate an error voltage representing the voltage difference between the desired output voltage and nominal output voltage. This error voltage will be subtracted by the internal voltage reference before it is applied to the noninverting input of the error amplifier. If the same voltage difference is added to the inverter input of the error amplifier, both circuits will provide the same result. Therefore, rather than being fixed, V_{TRIM} should be proportional to the voltage difference between the desired output voltage and the nominal voltage.

Figure 5 shows a circuit that provides up-trimming and down-trimming compatibility. Two resistor dividers generate two voltage references, one representing the desired output-voltage reference and one representing the internal voltage reference of an analog controller. A voltage follower is used to avoid interaction between desired output-voltage reference and the following circuit. The desired output-voltage reference (V1) is subtracted by the internal voltage reference of an analog controller (V2) by an AD822 FET-input op amp to generate the desired voltage difference. The linear gain ensures that V_{TRIM} is large enough to affect V_{VS+} when the desired output-voltage difference is related large.

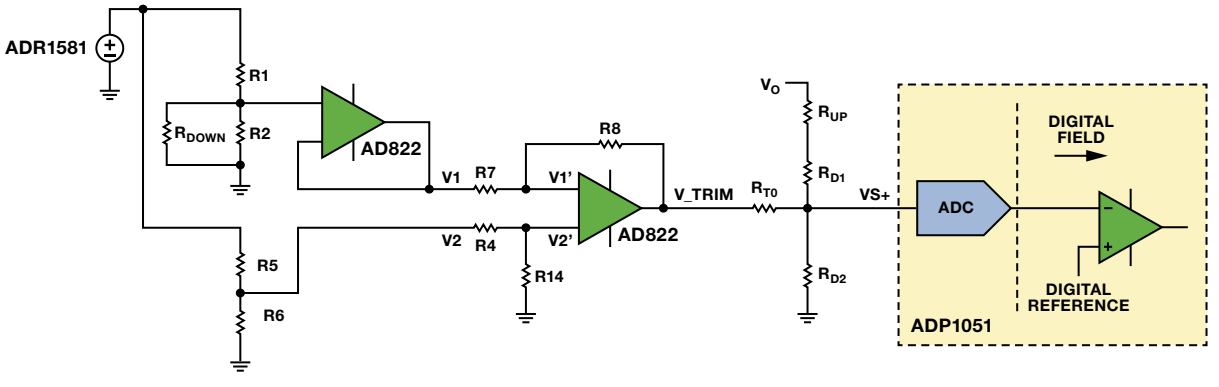

Figure 5. Reconfigured feedback network facilitates analog-output trimming.

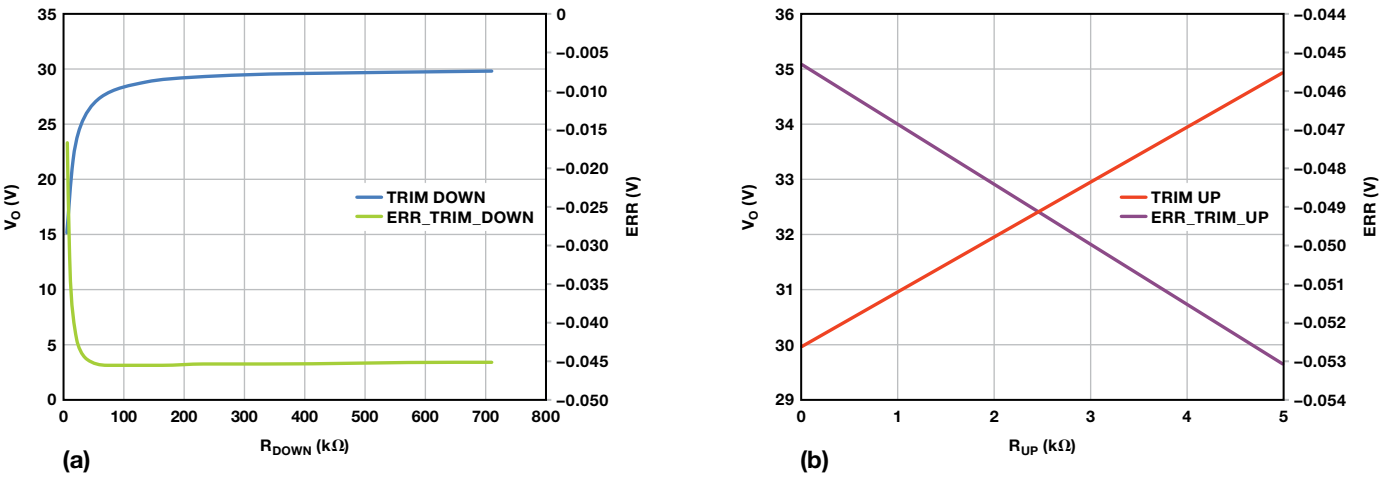

Figure 6. Calculated results of trimming the output voltage of the ADP1051 using the reconfigured feedback network: (a) trimming down, and (b) trimming up.

The target output-voltage trimming characteristics are defined in the AGF600-48S30 data sheet. Table 1 shows a set of resistor values that provides compatibility with this power module.

Table 1. Resistor Values for the Circuit Shown in Figure 5

R1	7.5 kΩ	R5	5.6 kΩ	R4	120 kΩ	R7	120 kΩ
R2	30 kΩ	R6	30.9 kΩ	R14	2200 kΩ	R8	2200 kΩ
R10	20 kΩ	R13	1 kΩ	R12	29 kΩ	RT0	17.8 kΩ

Using Equation 2 and the values shown in Table 1, the output-voltage trimming characteristic can be calculated. Figure 6 shows a plot of the results. The error between the target and calculated values is based on the reconfigured feedback network. This error is very small (less than 0.1 V with a 30-V nominal output voltage), which means this circuit provides very good results.

The calculations verify this method of reconfiguring the feedback network to trim the output voltage, and provide a path for other digital power controllers—such as the ADM1041A, ADP1046A, ADP1050, and ADP1053—that use a digital voltage reference to provide backward compatibility with analog controllers, enhancing the flexibility of the digital power solution.

References

ADIsimPower® Design Tool

Ask the Power Management Experts at ADI

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Video: ADuM3190 (Isolated Error Amp) and ADP1051 (Digital Controller)

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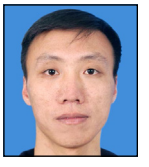

Capacitance-to-Digital Converter Facilitates Level Sensing in Diagnostic Systems

By Jim Scarlett

In blood analyzers, in-vitro diagnostic systems, and many other chemical-analysis applications, fluids must be moved from one vessel to another to aspirate samples from cuvettes or reagents from bottles. These lab-based systems will frequently handle a large number of samples, so minimizing processing time is essential. To enhance efficiency, the probes used for aspiration must be moved at high speed, making it necessary to accurately determine the location of the probe in relation to the surface of the fluid being drawn. This article demonstrates a novel use of a capacitance-to-digital converter (CDC) to perform this function with a high level of confidence.

CDC Technology

At a basic level, Σ-Δ ADCs make use of a simple charge-balancing circuit, with a known reference voltage and an unknown input voltage applied across fixed on-chip input capacitors. Charge balancing determines the unknown input voltage. Σ-Δ-based CDCs differ in that the unknown value is the input capacitor. A known excitation voltage is applied to the input, and charge balancing detects changes in the unknown capacitor, as shown in Figure 1. The CDC retains the resolution and linearity of the ADC.

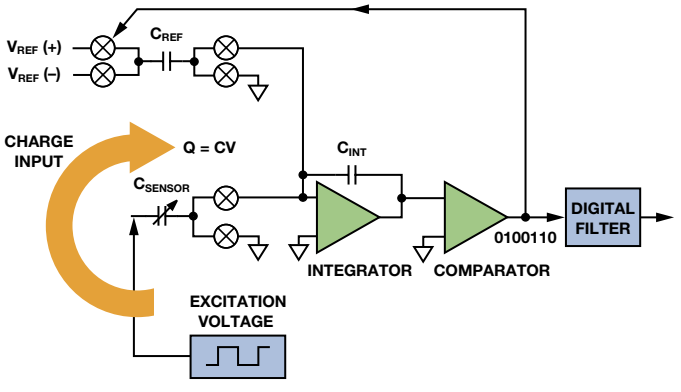

Figure 1. Basic CDC architecture.

Integrated CDCs are implemented in two ways. The single-channel AD7745 and two-channel AD7746 24-bit CDCs operate with one capacitor electrode connected to the excitation output and the other connected to the CDC input. Single-electrode devices, such as the AD7747 24-bit CDC with temperature sensor or the AD7147 16-bit CapTouch™ programmable controller, apply the excitation and read the capacitance at the same electrode. The other electrode, which is grounded, can be an actual electrode, or a user's finger in touch-screen applications. Either type of CDC can be used for level sensing.

The Capacitor

In its simplest form, a capacitor can be described as a dielectric material between two parallel plates. The capacitance value varies with plate area, distance between the plates, and the dielectric constant. By taking advantage of these variables, we can measure the changing value of an unusual capacitor to determine the probe position relative to the surface of the fluid.

In this application, the capacitor is made up of a conductive plate that sits beneath the cuvette and the moving probe, as shown in Figure 2. The excitation signal is applied to one electrode, and the other is connected to the CDC input. The measured capacitance is the same regardless of which electrode is connected to the excitation signal and which is connected to the CDC input. The absolute value of the capacitor depends on the form factors of the plate and the probe, the makeup of the dielectric, the distance from the probe to the plate, and other environmental factors. Note that the dielectric includes air, the cuvette, and the fluid contained therein. This application takes advantage of the changing nature of this dielectric mix as the probe approaches the plate, and more importantly as it approaches the fluid surface.

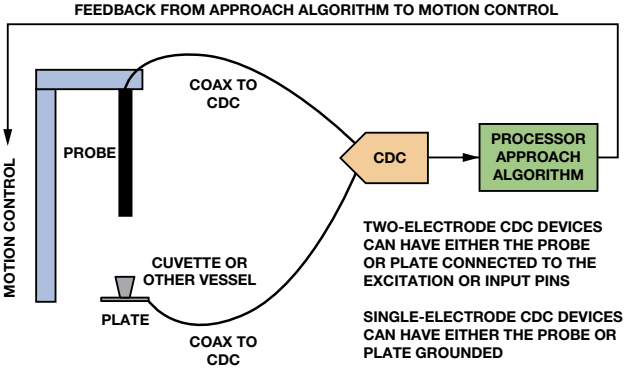

Figure 2. Level-sensing system diagram.

Figure 3 shows the capacitance increase as the probe approaches a dry cuvette. By observation, the change is a power series function (quadratic), but the coefficients change in the presence of a fluid. The fluid has a much larger dielectric constant than air, so the capacitance increases more rapidly as the fluid becomes a higher percentage of the dielectric.

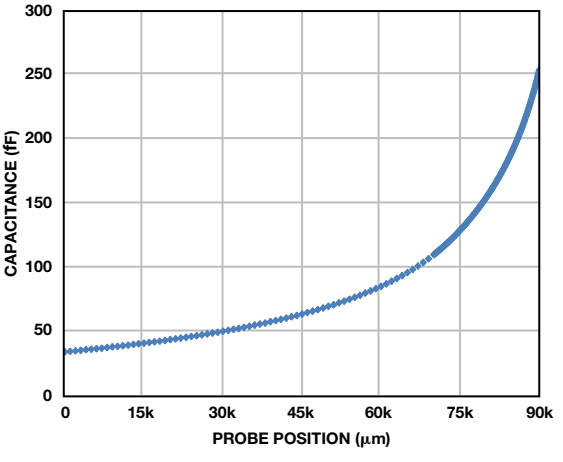

Figure 3. Capacitance measurements with dry cuvette.

As the probe gets very close to the fluid surface, the measured capacitance value accelerates, as shown in Figure 4. This large change can be used to determine proximity to the fluid surface.

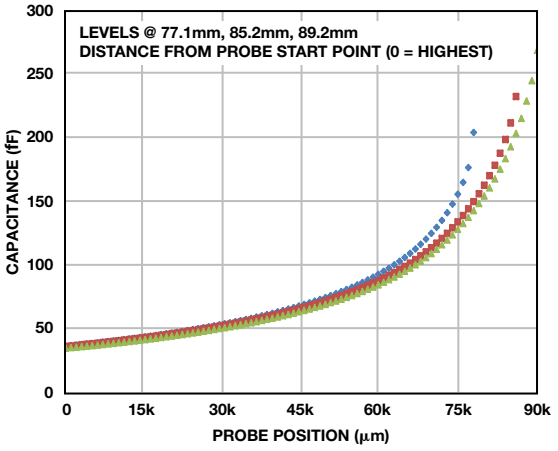

Figure 4. Capacitance measurements with filled cuvette.

Normalizing Data

Determination of the fluid level can be made even more robust by normalizing the data. If the probe location with respect to some reference point is accurately known, the system can be characterized at various points with no fluid present. Once the system has been characterized, the data collected while approaching the fluid surface can be normalized by subtracting the dry data from the approach data, as shown in Figure 5.

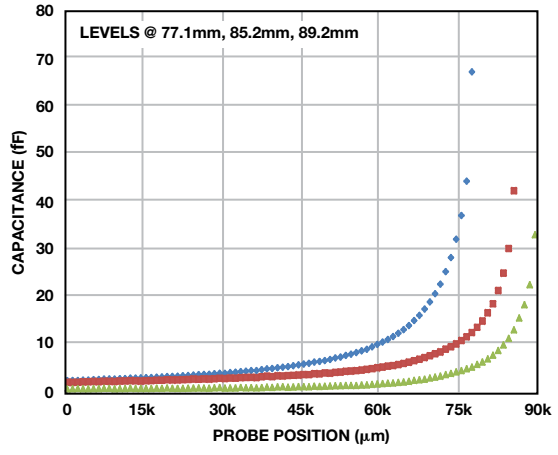

Figure 5. Normalized capacitance measurements.

Excluding temperature, humidity, and other environmental changes, normalization removes the systematic factors of the capacitance measurement. Electrode size, distance from probe to plate, and the dielectric effects of air and the cuvette are removed from the measurement. The data now represents the effect of adding fluid to the dielectric mix, making control of the approach easier and more consistent.

Normalized data cannot always be used, however. The motion-control system may not be precise enough to determine position accurately, for example, or the communications link with the motor controller may be relatively slow with respect to the output rate of the CDC. The methodology described will still work well even if normalized data is not available.

Using Slope and Discontinuities

As shown, the measured capacitance accelerates as the probe approaches the fluid surface, but this information can't easily be used to control the probe speed as it nears the surface. When the fill level is lower, the raw capacitance will be larger than when the container has a higher fill level. When using normalized data, the reverse is true. This makes it more difficult to find a threshold that might trigger at the best time to change the probe speed.

The slope, or rate of change in capacitance vs. change in position, can be used in place of the absolute capacitance. When moving the probe at constant speed, the slope can be approximated by subtracting one capacitance reading from the next. As shown in Figure 6, the slope data behaves in the same manner as the raw capacitance data.

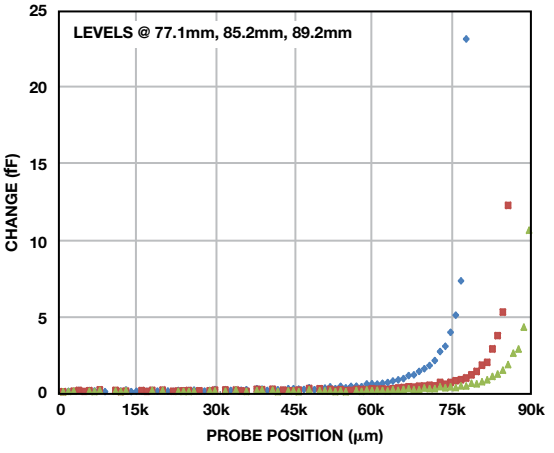

Figure 6. Slope data using normalized capacitance.

The slope of the raw or normalized capacitance readings is much more consistent for varying fill levels than the readings themselves, and it is relatively straightforward to find a slope threshold that works consistently regardless of the fill level. The slope data is a little noisier than the capacitance data, so averaging is helpful. When the calculated slope value rises above the noise, the probe is very near the fluid surface. This technique can create a very robust approach profile.

The data presented so far shows the behavior of the system as the probe approaches the fluid surface, but a key characteristic of this method becomes clear once the probe makes contact with the fluid. A large discontinuity occurs at this point, as shown in Figure 7. This is not a part of the normal acceleration of the capacitance curve, as demonstrated by the post-contact data points. The capacitive reading at this point is more than twice the precontact reading. This relationship may vary with system configuration, but is stable and consistent. The size of the discontinuity makes it relatively easy to find a capacitance threshold that will reliably indicate penetration of the fluid surface. An objective of this application is to insert the probe a known, small distance into the fluid, so this behavior is important.

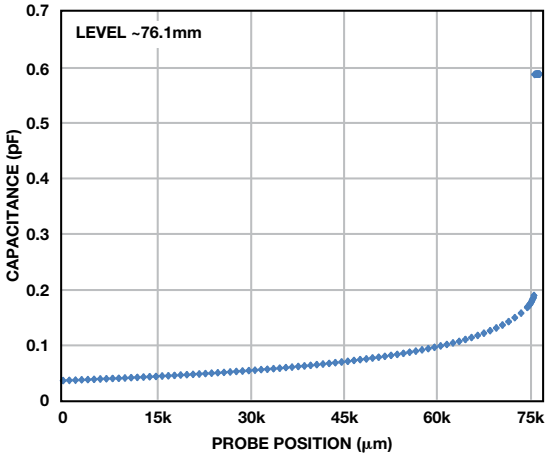

Figure 7. Discontinuity at fluid surface.

To maximize throughput, the probes should be moved at the highest practical speed, while minimizing the danger of damage from driving the probe too far. A high-precision motor-control system may not be available, so the solution must work even if the precise probe location is not known. The measurements described thus far allow this to be done with high confidence.

The Method

The flow chart shown in Figure 8 outlines the technique used to approach the fluid.

The probe is moved at the highest speed possible until it gets very close to the fluid surface. Depending upon the positional information, the computing power available, and the ability to characterize the system in advance, this point can be determined by a calculated power series, a capacitance threshold, or the slope of the capacitance curve, as presented here. Averaging the data can make the determination more robust. Normalizing the capacitance data makes for a more robust system as well.

When the probe has come close enough to the surface, the speed of the probe is greatly reduced for the final approach to the fluid surface. To maximize efficiency, this point should be as close to the surface as possible, but the approach speed must be reduced prior to penetration of the fluid surface to ensure good control of the distance penetrated before the probe is stopped.

Contact with the fluid surface is determined by the discontinuity that occurs at this point, using the capacitance value, as done here, or the slope of the capacitance curve. Averaging can reduce noise, but the large shift can be detected reliably without it. Normalization of the capacitance data can improve the robustness, but the impact is not as great as in the approach phase.

The probe can then be driven a predetermined distance below the surface. This is simple when precise motor control is available. If not, a speed estimate can be made, and the probe can be moved for a fixed length of time.

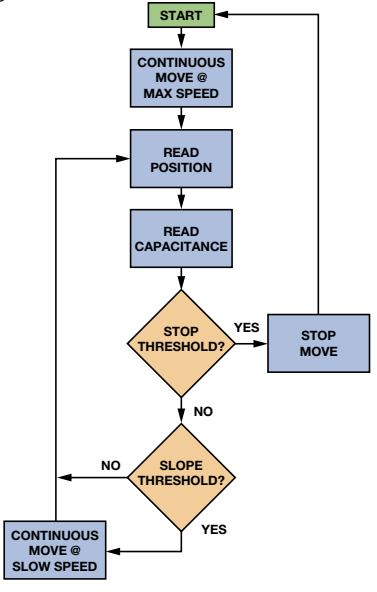

Figure 8. Simplified control flow.

The capacitance reading has two interesting characteristics once the fluid has been penetrated. First, the measured value changes relatively little as the probe is moved through the fluid. It had been hoped that a consistent rate of change might help determine penetration depth, but this was not observed. Second, the measured value varied very little for different levels of fluid, as shown in Figure 9. The capacitance measured after just penetrating the surface with a full vessel or a nearly empty vessel were essentially the same.

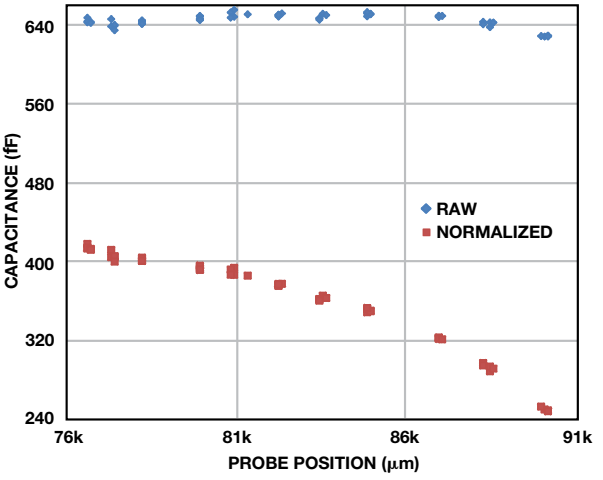

Figure 9. Capacitance vs. fluid level.

Normalized data shows a difference, however. As the fluid level became lower, the normalized capacitance value became smaller. This may be useful for determining if the fluid level is getting low in a situation where reliable position data is not available.

How quickly the probe can be stopped once the fluid surface has been penetrated depends on several factors, including the motor-control system itself, but a well thought-out approach profile can ensure tight control of probe penetration while maximizing probe speed. In the lab, a probe that moved approximately 0.45 mm between capacitance readings at maximum speed could be stopped within 0.25 mm of penetrating the surface. With a faster sampling rate, a probe moving approximately 0.085 mm between samples could be stopped within 0.05 mm of the fluid surface. In both cases, the probe was operated at the maximum speed until within about 1 mm to 3 mm of the fluid surface, allowing for maximum efficiency and throughput.

Conclusion

This nontraditional use of an integrated capacitance-to-digital converter enables a simple, robust level-sensing solution. An approach profile using both capacitance and slope measurements controls the probe motion. Alternative implementations allow greater robustness or provide additional information. This solution reliably stopped the probe very quickly after surface penetration, while still allowing maximum probe speed until the last possible moment. This article has only scratched the surface of using CDC technology for level sensing. Skilled engineers can use the ideas expressed here as a starting point for an improved solution tailored to specific situations.

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Current-Output Circuit Techniques Add Versatility to Your Analog Toolbox

By James Bryant

Although current mirrors and circuits such as the Howland current source are taught in analog circuit courses, a surprising number of engineers tend to think exclusively in terms of voltage when defining the output of precision analog circuitry. This is a pity, as current outputs offer advantages in a number of situations, including analog current-loop signaling (0 mA to 20 mA and 4 mA to 20 mA) in high-noise environments, and level shifting an analog signal across a large potential difference without the use of optical or magnetic-isolation techniques. This article summarizes some of the techniques available and suggests a number of useful circuits.

It is remarkably easy to obtain a steady current output. The simplest method uses a current mirror: two identical transistors—manufactured on the same chip so that their process, geometry, and temperatures are all identical—are connected as shown in Figure 1. The base-emitter voltage is the same for both devices, so the output current flowing in the collector of T2 is the same as the input current flowing in the collector of T1.

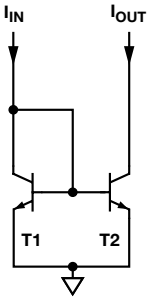

Figure 1. Basic current mirror.

This analysis assumes that T1 and T2 are identical and isothermal, and that their current gain is so large that the base currents can be disregarded. It also ignores the Early voltage, which causes the collector current to vary with varying collector voltage.

These current mirrors can be made with NPN or PNP transistors. By forming T2 with *n* transistors connected in parallel, the output current will be *n* times the input current, as shown in Figure 2a. If T1 consists of *m* transistors and T2 of *n* transistors, then the output current will be *n*/*m* times the input current, as shown in Figure 2b.

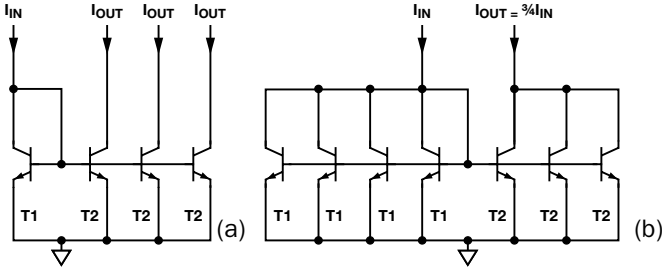

Figure 2. (a) Multistage current mirror, and (b) noninteger-ratio current mirror. The three T2 collectors may be joined to give $3I_{IN}$.

If the effect of Early voltage is important, it can be minimized by using the slightly more complex Wilson current mirror. Both three-transistor and four-transistor versions are shown in Figure 3. The four-transistor version is more accurate and has a wider dynamic range.

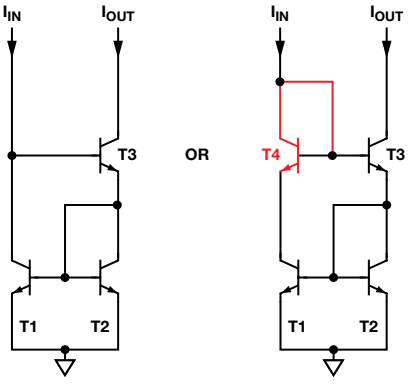

Figure 3. Wilson current mirror. T4 is optional but improves accuracy and dynamic range.

When a transconductance amplifier (voltage_in/current_out) is required, it can be made with a single-supply op amp, a BJT or FET (a MOSFET is usually the best choice as there is no base current error), and a precision resistor that defines the transconductance, as shown in Figure 4.

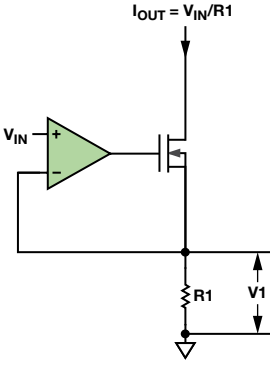

Figure 4. Transconductance amplifier. $V_{IN} – I_{OUT}$.

This circuit is both simple and inexpensive. The voltage on the MOSFET gate sets the current in the MOSFET and R1 such that V1, the voltage across R1, equals the input voltage, V_{IN}.

If a current mirror is required inside a monolithic IC, the simple transistor current mirrors are ideal. With discrete circuitry, however, the high price of matched transistors (due to their limited demand, rather than any manufacturing difficulties) makes the op-amp current mirror shown in Figure 5 the least expensive technique. This current mirror uses a transconductance amplifier plus one additional resistor.

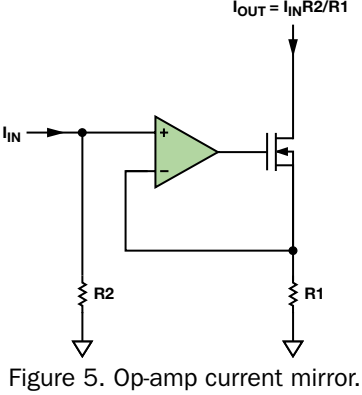

Figure 5. Op-amp current mirror.

Current mirrors have relatively high, sometimes nonlinear input impedance, so they must be fed by a current from a high-impedance current source (sometimes known as a *stiff* current source). An op amp is required if the input current must have a low-impedance sink. Figure 6 shows two low Z_{IN} current mirrors.

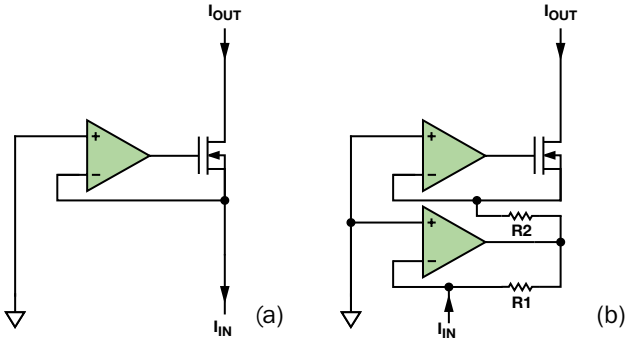

Figure 6. (a) Inverting low Z_{IN} current mirror, and (b) noninverting low Z_{IN} current mirror.

With basic current mirrors and sources, the input and output current polarities are the same. Usually the emitters/sources of the output transistors are grounded, directly or through a sense resistor, and the output current flows from the collector/drain to a load, the other terminal of which is connected to a dc supply. This is not always convenient, especially when one terminal of the load must be grounded. This is not a problem if the circuit may be built with its emitter/source on the dc supply, as shown in Figure 7.

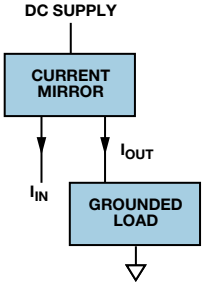

Figure 7. Current mirror for grounded load.

If the current or voltage input is referred to ground, level shifting must be used. Various circuits are possible, but the system shown in Figure 8 is suitable in many situations. This simple circuit uses a current source on ground to drive a current mirror on the dc supply, which drives the load. Note that the current mirror may have gain, so the signal current need not be as large as the load current.

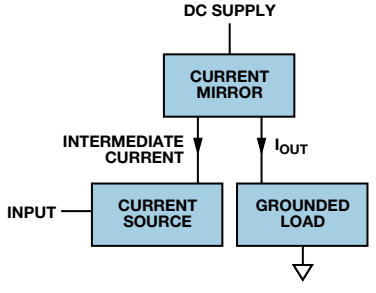

Figure 8. Level-shifting current mirrors.

The circuits we have discussed so far are unipolar—the current flows in one direction—but it is also possible to make bipolar current circuits. The simplest and best known is the Howland current pump, illustrated in Figure 9. This simple circuit has a number of problems: it requires very precise resistor matching to obtain high output impedance; the input source impedance adds to the resistance of R1, so it must be very low to minimize the matching error; the supply voltages must be substantially higher than the maximum output voltage; and the CMRR of the op amp must be reasonably good.

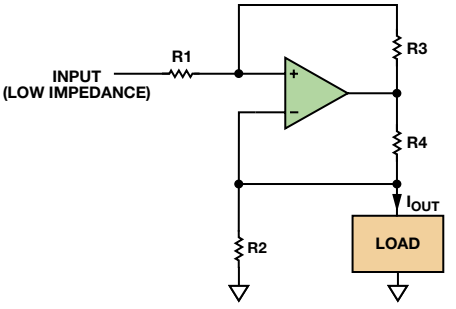

Figure 9. Howland current pump. Bipolar current output.

Today's high-performance instrumentation amplifiers (in-amps) are not expensive, so it is quite simple to make a bipolar current source using an op amp, an in-amp, and a current-sense resistor, as shown in Figure 10. Such circuits are simpler than the Howland pump, are not dependent on a resistor network (except the one integrated with the in-amp), and may have a voltage swing to within about 500 mV of each supply.

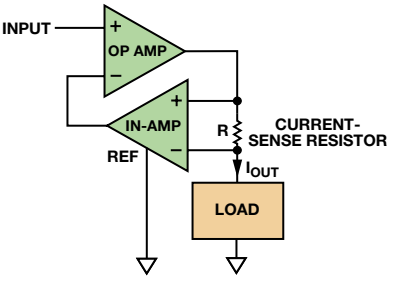

Figure 10. Bipolar-current op amp.

The circuits we have considered up to this point are amplifiers with precision current outputs. They may, of course, be used with a fixed input as accurate current sources, but it is possible to build simpler 2-terminal current sources. The ADR291 low-current voltage reference has about 10 μA standby current with a 20 nA/°C typical temperature coefficient. Adding a load resistance as shown in Figure 11, the reference current over a 3-V to 15-V supply range is (2.5/R + 0.01) mA, where R is the load resistance in kΩ.

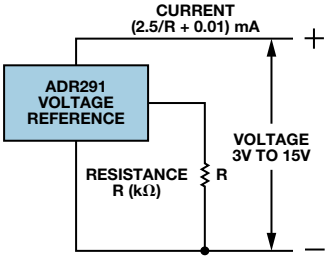

Figure 11. 2-terminal current source.

If precision is not an issue, and all that is required is a stiff unipolar current source, a current source can be built with a depletion-mode JFET and a resistor. This arrangement, shown in Figure 12, is not particularly temperature stable and, for a given value of R, the current can vary considerably from device to device, but it is simple and inexpensive.

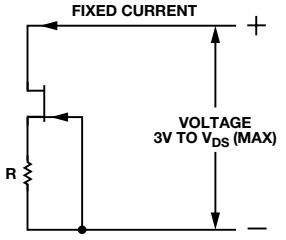

Figure 12. JFET current source.

I recently needed power for some LEDs. Several engineer friends thought that I would have trouble making the variable current supply that is required for them to be dimmed. In fact, I quickly modified some "black-brick" laptop power supplies (bought for pennies at a car boot sale) to do the job. Figure 13 shows a simple modification that supplies constant current to the LEDs. With small output currents, it operates normally with a fixed-output voltage.

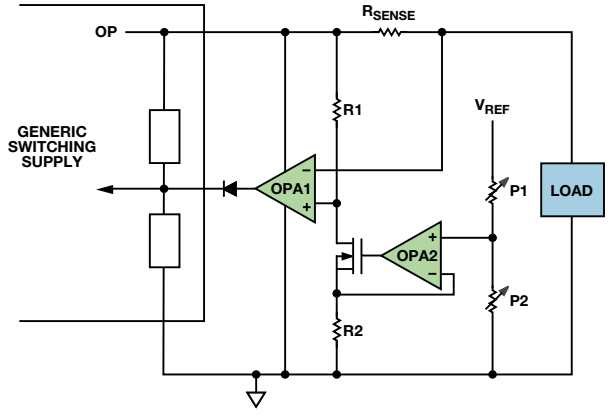

Figure 13. Black-brick switching supply modified for current-limit output.

To make a variable current, a voltage reference—from the black brick or local—is applied to a potentiometer represented by P1 and P2. OPA2 and the MOSFET send a small current through R1, causing a voltage drop across it. The load current flows in the sense resistor. If the voltage drop in the sense resistor due to the load current exceeds the drop across R1, the output of OPA1 will rise, overriding the voltage control in the brick, and limiting its output voltage to prevent the output current from exceeding the limit.

This discussion of basic current-source ideas is not a detailed application note. Some of the circuits require further design work to limit (or dissipate) heat, to ensure amplifier stability and that no absolute-maximum ratings are exceeded, and to calculate practicable performance limits. For more detailed analyses of these circuits, consult a good electronics textbook, the Analog Devices website, or even Wikipedia.

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