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# Editor's Notes

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## Product Introductions: Volume 48, Number 3

Data sheets for all ADI products can be found by entering the part number in the search box at analog.com.

## Analog Dialogue

# Designing Robust, Isolated I²C/PMBus Data Interfaces for Industrial, Telecommunications, and Medical Applications

**By Maurice O'Brien**

### Introduction

A key requirement for industrial and instrumentation (I&I), telecommunications, and medical applications is a reliable interface for transmitting data. The inter-integrated circuit (I²C) bus is a 2-wire, bidirectional bus used for low-speed, short-distance communication between integrated circuits. Developed by Philips in the early 1980s for ICs on a single board, I²C usage is still increasing. The power management bus (PMBus), a relatively slow, 2-wire communications protocol based on I²C, is targeted at digital management of power supplies. The PMBus protocol defines an open-standard, digital-power-management protocol that facilitates communication with a power converter or other connected device.

Figure 1 shows how an isolation barrier galvanically isolates the I²C interface from each system connected to it, allowing digital data to travel between two points, but preventing the flow of ground current; this reduces signal distortion and errors by removing noise that gets coupled onto the communications bus.

PC boards used in telecommunications applications often include digitally controlled power converters and circuits that operate at different ground potentials. To ensure trouble-free card insertion/removal and robust operation, each interface must be isolated, but isolating I²C interfaces is complicated because the bus is bidirectional. This requirement is not compatible with optocouplers, which are unidirectional. Figure 2 shows a PMBus communications link that isolates the ADM1075 −48-V hot swap and digital power monitor on the primary side from the secondary side, which operates with 12-V and 3.3-V supplies. The ADM3260 dual I²C isolator with dc-to-dc converter isolates the SDA and SCL signals. Its isolated power supply (3.3 V_ISO) powers the ADuM3200 2-channel digital isolator that isolates the SHDN and RESTART signals.

Isolation is required because the primary side is referenced to −48 V, while the secondary side is referenced to ground in a low-voltage domain. Isolation prevents permanent damage that could occur if the I²C port was inadvertently connected
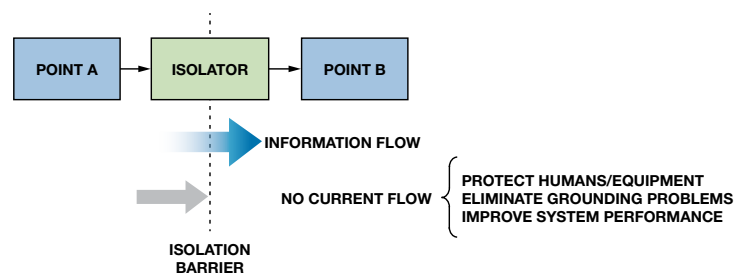


*Figure 1. Isolation function.*
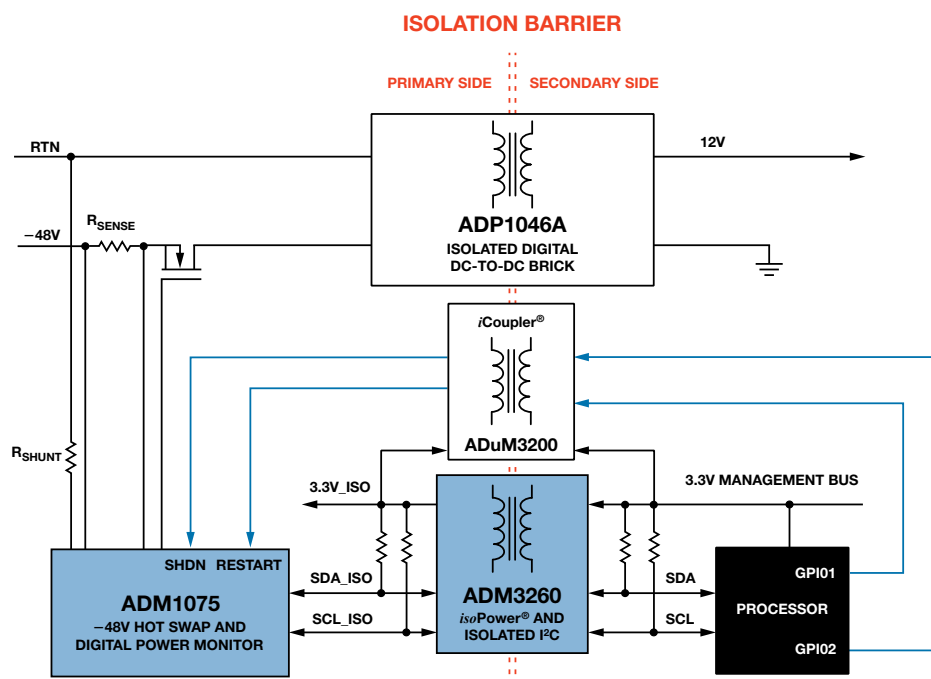


*Figure 2. Typical isolated PMBus communications link.*

directly to the −48-V supply. Isolation also provides protection against high voltages or currents caused by the line surges or ground loops that can occur in a system with multiple grounds. The isolated power channel (3.3 V_ISO) allows the primary-side circuitry to be powered from the secondary side, removing the requirement for a separate low-voltage power source, which is not commonly available in the −48-V domain and is problematic to generate. All additional I/O signals crossing the isolation barrier require isolators that can also be powered by the ADM3260. To achieve a robust data communications link, each I²C device connected to the I²C bus must be isolated.

Examples of isolated I²C applications include:

- Isolated I²C, SMBus, or PMBus interfaces
- Level-translating I²C interfaces for power supplies
- Networking
- Power-over-Ethernet
- Central office switching
- Telecommunication and data communication equipment
- Isolated data acquisition systems
- −48-V distributed power systems
- −48-V power supply modules

It is often necessary to bring data from a precision converter (ADC or DAC) across an isolation barrier via an I²C bus. Figure 3 shows two isolated data-acquisition systems. These applications also require an isolated power supply to power the converters and amplifiers on the secondary side.
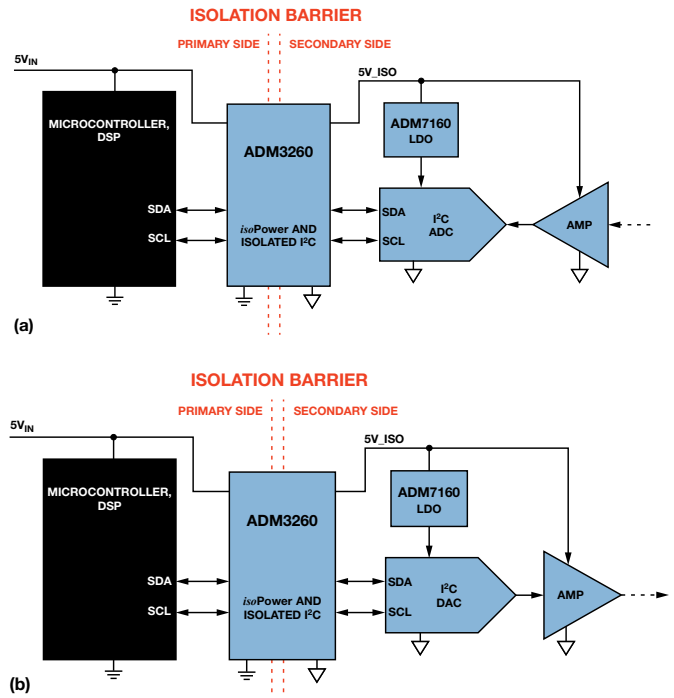


**Figure 3.** (a) Isolated I²C ADC and amplifier, and (b) Isolated I²C DAC and amplifier.

Some applications require channel-to-channel isolation, where each channel is isolated from every other channel, as shown in Figure 4.
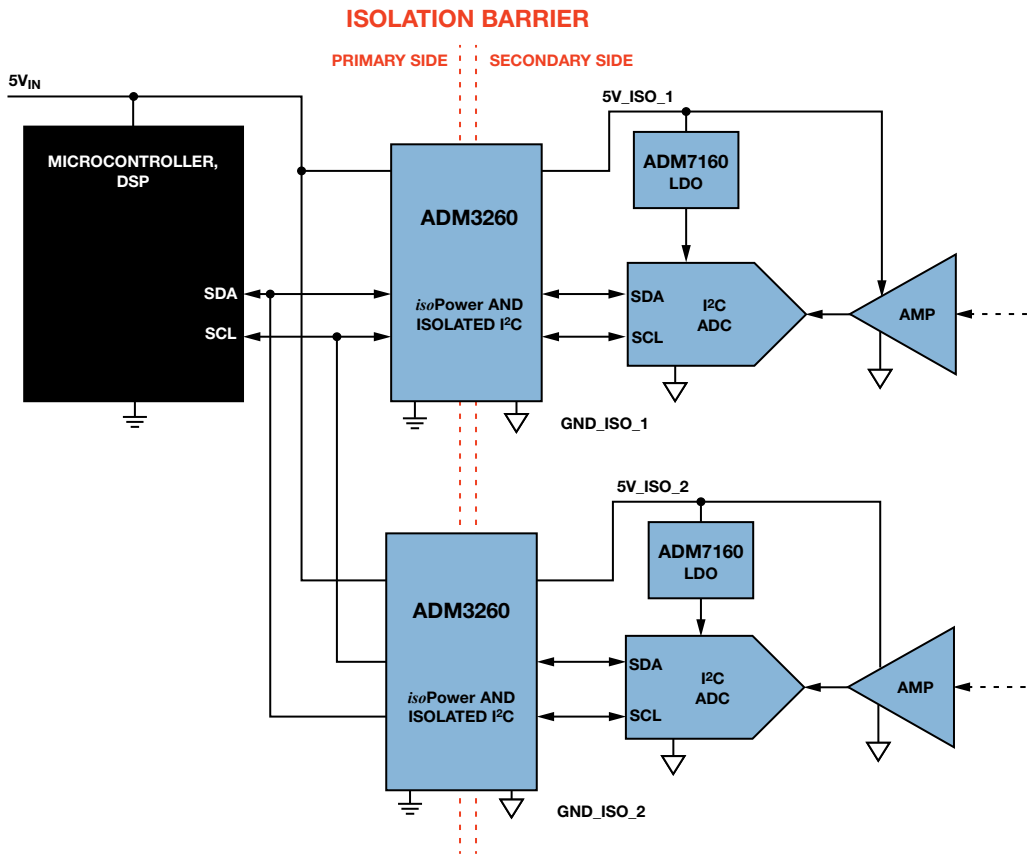


**Figure 4.** Channel-to-channel isolated I²C ADC and amplifier.

In larger systems, level translation is required between different voltage domains. An example of this is isolating the PMBus on each line card in a telecommunications rack-mounted system. Figure 5 shows a typical telecommunications application featuring multiple line cards that can be inserted into a −48-V backplane. In this application, the isolators level shift the I²C logic signals from the −48-V backplane to the fully isolated +12-V system.

Isolated power for the I²C communication link is obtained by using an isolated dc-to-dc power supply or *iso*Power integrated dc-to-dc converter technology from Analog Devices. Signal isolation is implemented using optocouplers or *i*Coupler technology from Analog Devices.

## Implementing an Isolated I²C Interface

Bidirectional data must pass between an intelligent device (such as an ADC or DAC) on the primary side to a processor on the secondary side, and power must pass from the primary side to the secondary side. To isolate a data link, the data lines and the power supply must all be isolated. For an I²C link,

all connected devices must be isolated from the I²C bus, as shown in Figure 6.
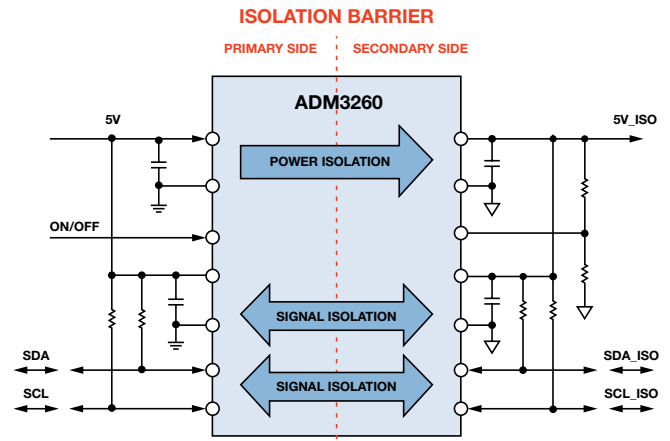
**Figure 6.** *Isolated I²C interface.*
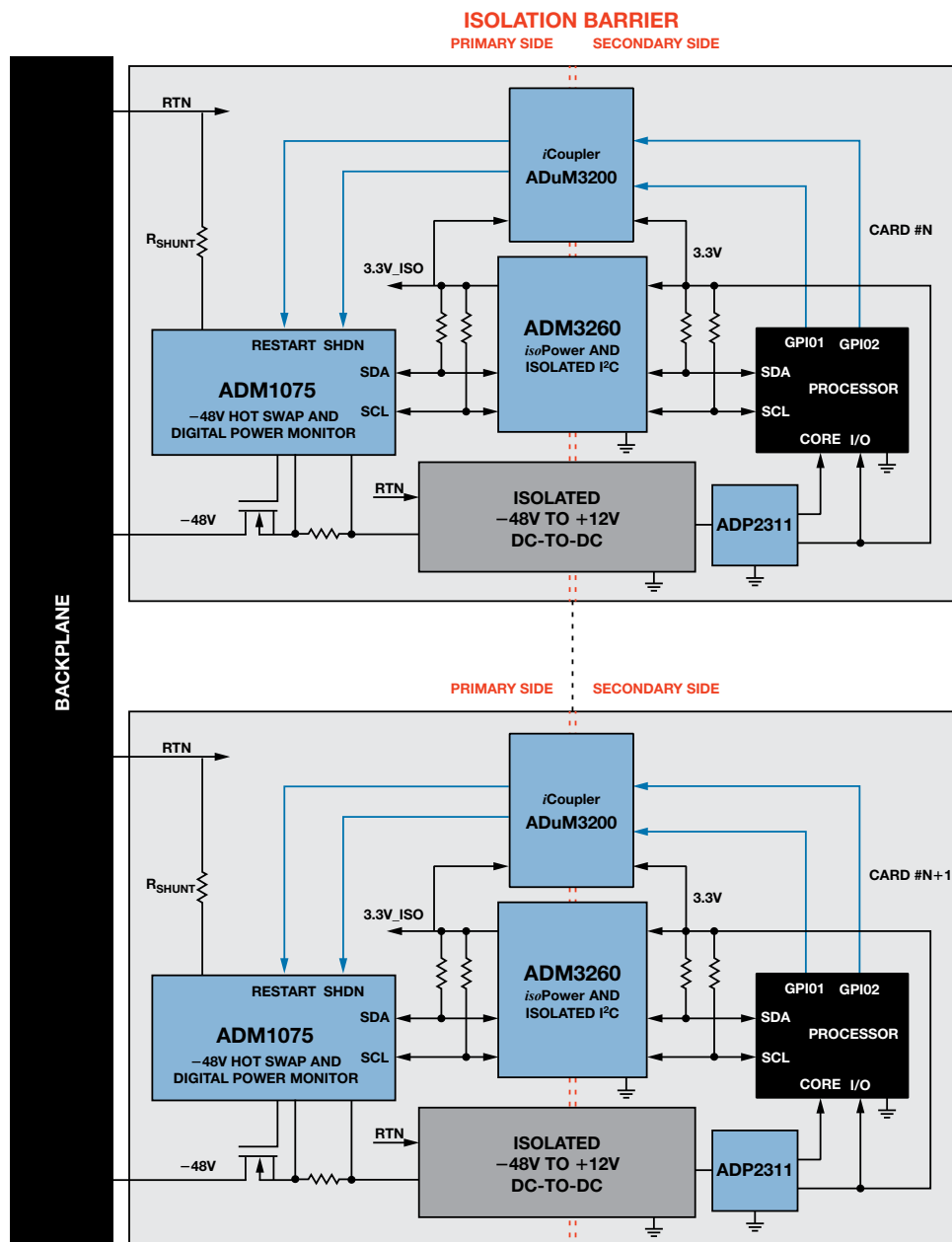
**Figure 5.** *Isolating and level translating PMBus signals in a −48-V application.*

## The Challenge of Isolated I²C Interfaces

Because the I²C interface is bidirectional, providing isolation while avoiding bus glitches and lock-up can be a challenge. Figure 7 shows an optocoupler-based interface. Optocouplers are inherently unidirectional, so each bidirectional I²C line must be split into two unidirectional lines. Isolating a complete I²C interface requires four optocouplers and several passive components. The resulting cost, PC board area, and complexity diminishes the inherent value of the otherwise simple, low-cost, 2-wire I²C interface. Note that an isolated power supply is also required.
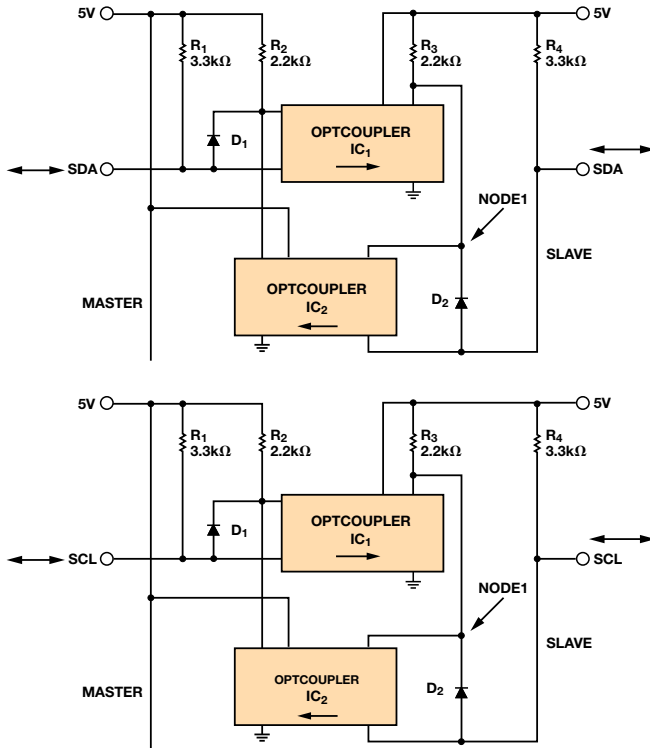


*Figure 7. An optocoupler-based I²C interface.*

## Isolation Technology: Data and Power

Figure 8 compares two principal isolation technologies. *i*Coupler technology (a) uses thick-film processing techniques to build microscale on-chip transformers that achieve 2.5-kV isolation. The older, but widely employed, optocoupler solution (b) uses light-emitting diodes (LEDs) and photodiodes. The LEDs convert electrical signals to light, and photodiodes convert the light back to electrical signals. The intrinsically low conversion efficiency for electrical-to-light conversion leads to relatively high power consumption, the slow response of photodiodes limits their speed, and aging limits their lifetime.

Using wafer-level processing to fabricate on-chip transformers allows low-cost integration of *i*Coupler channels with each other and with other semiconductor functions. One example is the ADM3260 hot swappable, dual I²C isolator with integrated dc-to-dc converter. *i*Coupler isolation overcomes the limitations imposed by optocouplers in many ways: these easy to use devices reduce overall solution size, system cost, and power consumption, while increasing performance and reliability. In addition, *i*Coupler technology does not suffer performance degradation caused by current transfer ratio (CTR) aging of standard optocouplers over time and *i*Coupler is bidirectional technology, whereas optocoupler technology is inherently unidirectional.

Until recently, creating a low-voltage supply on the isolated side required either a separate dc-to-dc converter, which is

relatively large and expensive, or a custom discrete circuit as shown in Figure 9. These approaches were the only viable alternatives, even for I²C data communication or other applications requiring only a small amount of isolated power.
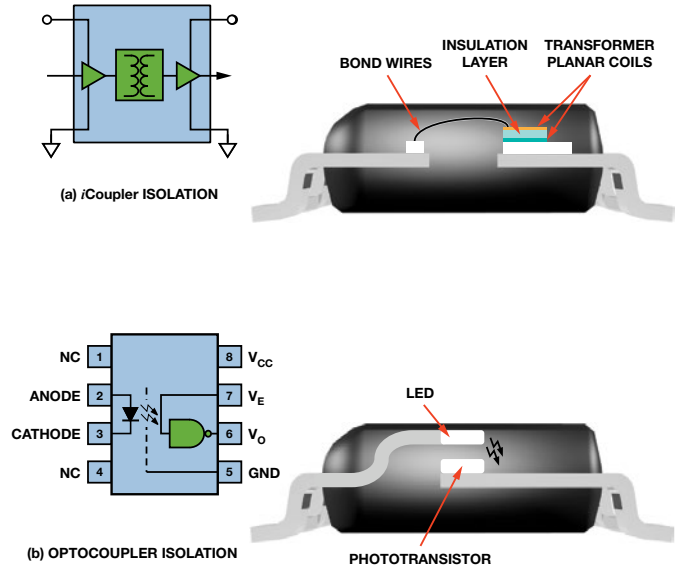


*Figure 8. Isolation technologies compared: (a) iCoupler isolation. (b) Optocoupler isolation.*
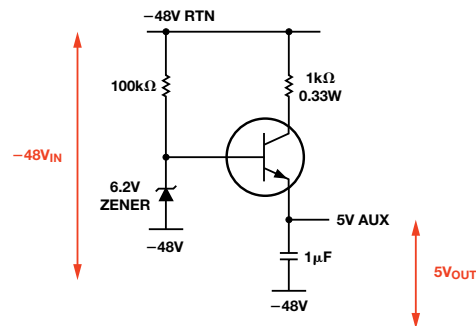


*Figure 9. Discrete −48-V-to-+5-V power solution to power isolators.*

To solve this problem, Analog Devices developed a complete, fully integrated solution that combines signal and power transfer across an isolation barrier using microtransformers. An extension of the well-established *i*Coupler technology, *iso*Power is a breakthrough alternative. Achieving up to 5-kV signal and power isolation within a single component, it eliminates the need for an isolated power supply, and significantly reduces PC board area, design time, and total system cost for a typical I²C bus.

## Dual I²C Isolators with Integrated DC-to-DC Converter

Figure 10 compares PMBus isolation using discrete components with a fully integrated solution. The discrete approach requires four optocouplers for isolation, an isolated power supply, and complex analog circuits to prevent latch-up and suppress glitches. The isolated power supply uses a transformer driver IC to drive a discrete transformer, along with a simple rectifier and low-dropout regulator to clean up the isolated rail. This design requires eight ICs and several passive components, and burdens the interface with higher cost, increased PC board area, and lower reliability.

The integrated solution provides a fully isolated bidirectional I²C interface and isolated power with a single IC, plus the decoupling capacitors and pull-up resistors associated with any I²C interface. The ADM3260 is free of glitch and lock-up

issues, has UL approved 2.5-kV rms-isolation ratings, and is offered in a 20-lead SSOP package. It provides bidirectional isolated data and clock lines and isolated power without the size, cost, and complexity of optocouplers.

This single-chip solution significantly reduces the cost, design time, and PC board area required for an isolated I²C interface, while enhancing reliability. It operates from 3.3-V or 5-V supplies without modification, avoiding the design changes that would be necessary with a discrete design, and provides 150 mW of output power at 5 V or 65 mW at 3.3 V, allowing it to power ADCs, DACs, or other small systems on the isolated side.

### Transient Protection

To allow the isolated interface to operate under the harsh operating conditions found in industrial applications, *i*Coupler and *iso*Power isolation technologies provide >25-kV/µs common-mode transient immunity. This specifies the maximum slew rate on the rising and falling edges of the potential difference between primary and isolated sides, ensuring that transients coupled onto the bus will not damage devices connected to the bus or corrupt the transmitted data and enhancing the reliability of the data link.

### 2.5-kV Isolation Protection and Approvals

The isolated solution specified 2.5-kV rms isolation between the primary and isolated side of the device. This isolation rating ensures that current cannot flow from the primary side to the I²C bus, and that voltages or transients coupled onto the bus won't reach the logic side. The 2.5-kV isolation protection also means that people and equipment on the logic side are protected from high voltages or transients on the bus side. Approval is pending for the 2.5-kV isolation rating of the ADM3260 at the following agencies: Underwriters Laboratories (UL), Verband Deutscher Elektrotechniker (VDE), and Canadian Standards Association (CSA). UL 1577 approval requires the isolation barrier of all devices to be 100% production tested. The ADM3260 provides:

- UL recognition
- 2500 V rms for 1 minute per UL 1577
- VDE certificate of conformity
- IEC 60747-5-2 (VDE 0884, Part 2)
- $V_{IORM}$ = 560 $V_{PEAK}$
- CSA Component Acceptance Notice #5A

### PCB Layout

Proper PCB layout is critically important to ensure that the specified 2.5-kV isolation is achieved in an actual design. The principal considerations are creepage (shortest distance along the surface between two conductors) and clearance (shortest distance through the air) between the logic-side GND and the bus-side GND. The ADM3260 requires no external circuitry for its logic interfaces. Power-supply bypassing is required at the input and output supply pins, as shown in Figure 11. Further information on PCB layout guidelines for controlling electromagnetic interference (EMI) can be found in AN-0971 Application Note, *Recommendations for Control of Radiated Emissions with isoPower Devices.*
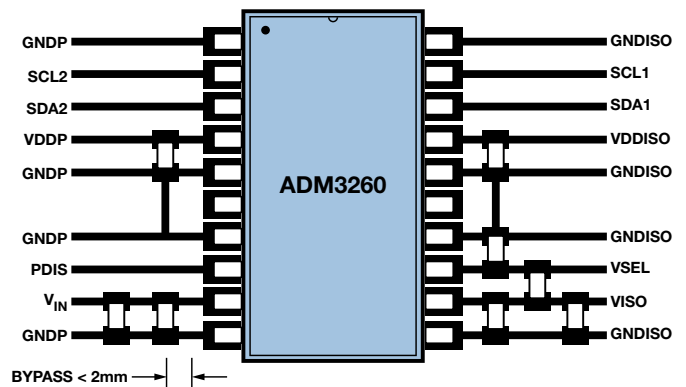


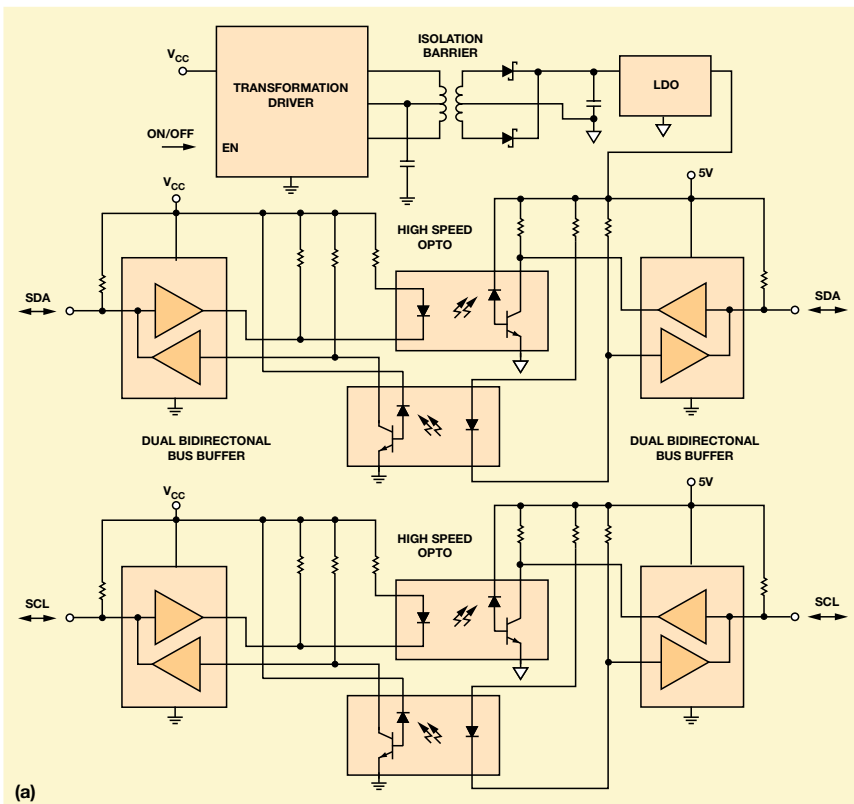**Figure 11:** *ADM3260 recommended printed circuit board layout.*



**Figure 10.** *Isolated I²C designs compared: (a) Discrete solution and (b) Integrated solution.*

## ADM3260 Applications and Benefits

The ADM3260 hot swappable isolator provides both data and power isolation. Two nonlatching, bidirectional communication channels support a complete isolated I²C/PMBus interface, and an integrated dc-to-dc converter provides up to 150 mW of isolated power at 3.15 V to 5.25 V. The bidirectional channels eliminate the need for splitting I²C/PMBus signals into separate transmit and receive signals for use with standalone optocouplers, and the integrated dc-to-dc converter enables a complete isolated I²C/PMBus interface to be implemented in a small form factor. The ADM3260, shown in Figure 12, is available in a 20-lead SSOP package with 5.3-mm creepage, operates from −40°C to +105°C, and is priced at $2.99 in 1000s.

In addition to isolating I²C buses for hot-swappable central-office line cards, the ADM3260 can be used to isolate data-acquisition equipment in harsh industrial environments, to provide power and level translation over Ethernet, and in many other applications.

## Conclusion

Isolated I²C/PMBus links in industrial and instrumentation, telecommunications, and medical applications need to be small, robust, and inexpensive. By integrating chip-scale transformer isolation, a single chip can implement a fully isolated I²C/PMBus data link including isolated power. The ADM3260 hot-swappable, dual I²C isolator with integrated dc-to-dc converter can provide a compact, reliable, low-cost, high-performance solution for these demanding applications while significantly reducing circuit complexity and design time.

### References

Digital Isolators

Digital Isolator Product Selection and Resource Guide

*i*Coupler Products with *iso*Power Technology: Signal and Power Transfer Across Isolation Barrier Using Microtransformers



**Figure 12.** *ADM3260 isolated I²C/PMBus interface.*

## I²C Digital Isolators

| Part Number | Insulation Rating (kV rms) | Max Data Rate (Mbps) | Serial Check | Serial Data | Min P$_{OS}$ Supply | Max P$_{OS}$ Supply | Supply Current (mA) | Max Operating Temp (°C) | Automotive Recommended | Price ($U.S.)[1] |
|---|---|---|---|---|---|---|---|---|---|---|
| ADM3260 | 2.5 | 1 | Bidirectional | Bidirectional | 3 | 5.5 | 9.5 | 105 | – | $2.99 |
| ADUM2551 | 5 | 1 | Unidirectional | Bidirectional | 3 | 5.5 | – | 105 | – | $2.77 |
| ADUM2250 | 5 | 1 | Bidirectional | Bidirectional | 3 | 5.5 | – | 105 | – | $3.00 |
| ADUM1251 | 2.5 | 1 | Unidirectional | Bidirectional | 3 | 5.5 | – | 105 | Yes | $2.20 |
| ADUM1251 | 2.5 | 1 | Bidirectional | Bidirectional | 3 | 5.5 | 5 | 105 | Yes | $2.20 |

[1]All prices are in USD in quantities of 1000 to 4999.

Maurice O'Brien [maurice.obrien@analog.com] joined Analog Devices in 2002, following his graduation from the University of Limerick, Ireland, with a bachelor's degree in electronic engineering. He currently works as a product marketing manager in the Power Management product line. In his spare time, Maurice enjoys horse riding, outdoor sports, and travel.

**Maurice O'Brien**

Also by this author:

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Volume 47, Number 4

# Demystifying High-Performance Multiplexed Data-Acquisition Systems

By Maithil Pachchigar

## Introduction

High-channel-density data-acquisition systems used for medical imaging, industrial process control, automatic test equipment, and 40G/100G optical communication systems multiplex signals from many sensors to a small number of ADCs that can convert every channel in a sequence. Multiplexing allows the use of fewer ADCs per system, offering significant savings in power, size, and cost. Successive-approximation ADCs—often called SAR ADCs for their successive-approximation register—have low latency, making them popular in multiplexed systems that demand fast response to a full-scale input step (worst case) without any settling time issues. Easy to use, SAR ADCs offer low power and small size. This article focuses on the key design considerations, performance results, and application challenges associated with multiplexed data-acquisition systems using high-performance precision SAR ADCs.

## Multiplexed Data–Acquisition System Challenges

Multiplexed data-acquisition systems demand wideband amplifiers that settle quickly while driving the ADC's full-scale (FS) input range. In addition, switching and sequential sampling of the multiplexer channels must be synchronized with the ADC conversion cycle. The large voltage differential between adjacent inputs makes these systems prone to channel-to-channel crosstalk. To avoid errors, the complete signal chain, including multiplexer and amplifier, must settle to the required accuracy, typically specified as crosstalk error or settling error. Figure 1 shows a block diagram of a data-acquisition system that includes a multiplexer, ADC driver, and SAR ADC.
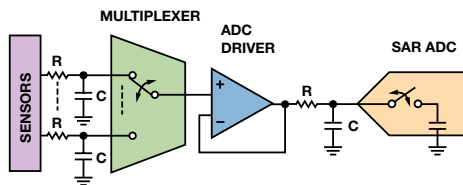


*Figure 1. Block diagram of multiplexed data–acquisition system.*

## Multiplexer

Fast input switching and wide bandwidth of the multiplexer are critical for high performance. The multiplexer's turn-on or turn-off times specify the delay between application of the digital control input and the output crossing 90% of $V_{OUT}$, as shown in Figure 2.
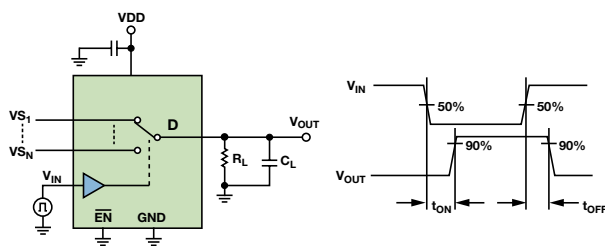


*Figure 2. Switching time in a typical multiplexer.*

A voltage glitch or kickback occurs at the multiplexer input when it switches channels. This kickback is a function of the turn-on and turn-off times, on-resistance, and load capaci-

tance. Large switches with low on-resistance typically result in a large output capacitance that must be charged to a new voltage each time the input is switched. If the output doesn't settle to a new voltage, crosstalk error will occur. Therefore, the multiplexer's bandwidth must be sufficient, and a buffer amplifier or large capacitors must be used at the multiplexer input to settle a full-scale step. In addition, the leakage current flowing through the on-resistance will introduce a gain error, so both should be kept small.

## ADC Driver

When the multiplexer input channel is switched, the ADC driver amplifier must settle a large voltage step within the specified sample period. The input can change from negative full scale to positive full scale, or vice versa, so a large input voltage step can be created in a small time. The amplifier must have a wide large-signal bandwidth and fast settling time to handle this step. In addition, nonlinear effects appear as a result of slew rate or output current limitations. Also, the driver amplifier must settle the kickback caused by charge rebalancing on the SAR ADC input at the start of the acquisition period. This could become a bottleneck in settling the inputs in a multiplexed system. Settling time issues can be reduced by lowering the throughput rate of the ADC to provide longer acquisition time, thus allowing the amplifier sufficient time to settle to the required accuracy.

Figure 3 shows a timing diagram of a multiplexed data-acquisition system when its input makes a full-scale change. The cycle time of the ADC, which consists of the conversion time plus the acquisition time ($t_{CYC} = t_{CONV} + t_{ACQ}$), is usually specified as 1/throughput rate in the data sheet. The capacitive DAC of the SAR ADC is disconnected from the inputs at the start of the conversion, and the multiplexer channel can be switched to the next channel after a small switching delay($t_S$). This allows the maximum time to settle the selected channel. To guarantee performance at maximum throughput, all of the components in the multiplexed system must settle at the ADC input between the time that the multiplexer switches and the end of the acquisition time. The multiplexer channel switching must be properly synchronized with the ADC conversion time. The achievable throughput rate in a multiplexed system is the single ADC throughput rate divided by the number of channels being sampled.
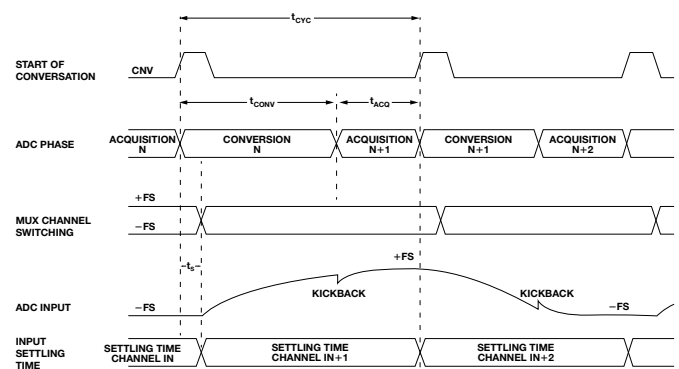


*Figure 3. Typical timing diagram of a multiplexed data–acquisition system.*

## RC Filter at Inputs of Multiplexer

Some designers use a low-output-impedance buffer to handle the kickback from the multiplexer inputs. The input bandwidths of the SAR ADC (tens of MHz) and ADC driver (tens to hundreds of MHz) are higher than the sampling frequency, and the desired input signal bandwidth is typically in the tens to hundreds of kHz range, so an RC antialiasing filter may be required at the input of the multiplexer to eliminate unwanted signals (aliases) from folding back into the bandwidth of interest and to reduce settling time issues. The value of the filter capacitance used at each input channel should be carefully selected based on the following trade-off; if the capacitance is large, it will help attenuate the kickback from the multiplexer, but it can also make the previous amplifier stage unstable by degrading its phase margin. C0G or NP0 type capacitors are recommended for an RC filter that has high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages. A reasonable value of series resistance should be chosen to keep the amplifier stable and limit its output current. The resistance cannot be too large, or the amplifier will not be able to recharge the capacitor after the multiplexer kickback.

## Multiplexed Data–Acquisition Signal Chain

Figure 4 shows a simplified signal chain for a multiplexed data-acquisition system. One of two differential channels is selected by the ADG774 CMOS multiplexer. To evaluate this system, the positive and negative differential inputs of the ADG774 are switched continuously to generate a full-scale step. Two ADA4899-1 ultralow-distortion op amps buffer the

multiplexer outputs and drive the AD7960 18-bit, 5-MSPS PulSAR® ADC. The RC filter (33 Ω/56 pF) helps to reduce the kickback coming from the capacitive DAC input of the AD7960 and limits the noise going to the AD7960 inputs.

The ADG774 quad 2:1 CMOS multiplexer offers fast switching speed ($t_{ON}$ = 7 ns, $t_{OFF}$ = 4 ns), low on-resistance ($R_{ON}$ = 2.2 Ω), wide bandwidth ($f_{-3dB}$ = 240 MHz), and low power dissipation (5 nW), making it ideally suitable for portable and battery-powered instruments. The inputs of the ADG774 are tied to a fixed 5-V reference and a ground, so the output should swing from positive full scale to negative full scale. Figure 5 shows a typical profile of on-resistance vs. input voltage over the full 0-V-to-5-V analog-input range and −40°C to +85°C temperature range. This level of performance ensures excellent linearity and low distortion for fast-switching signals.

The output of the ADG774 is connected to a high-input-impedance amplifier stage. The ADA4899-1 high-speed op amp features ultralow noise (1 nV/√Hz) and distortion (−117 dBc), 600-MHz bandwidth, and 310-V/µs slew rate. Operating on +7-V and −2.5-V supplies allows enough headroom to achieve low system noise and distortion. The amplifier's 50-ns settling time of 0.1% for a 2-V p-p input signal, shown in Figure 6, makes it ideal for driving the AD7960.

The AD7960 precision differential ADC offers best-in-class noise and linearity without latency or pipeline delay, high accuracy (18-bit resolution, ±0.8-LSB INL, 99-dB SNR, and −117-dB THD), fast sampling (5 MSPS), low power dissipation, and low cost. Powered from +5 V (VDD1) and +1.8 V



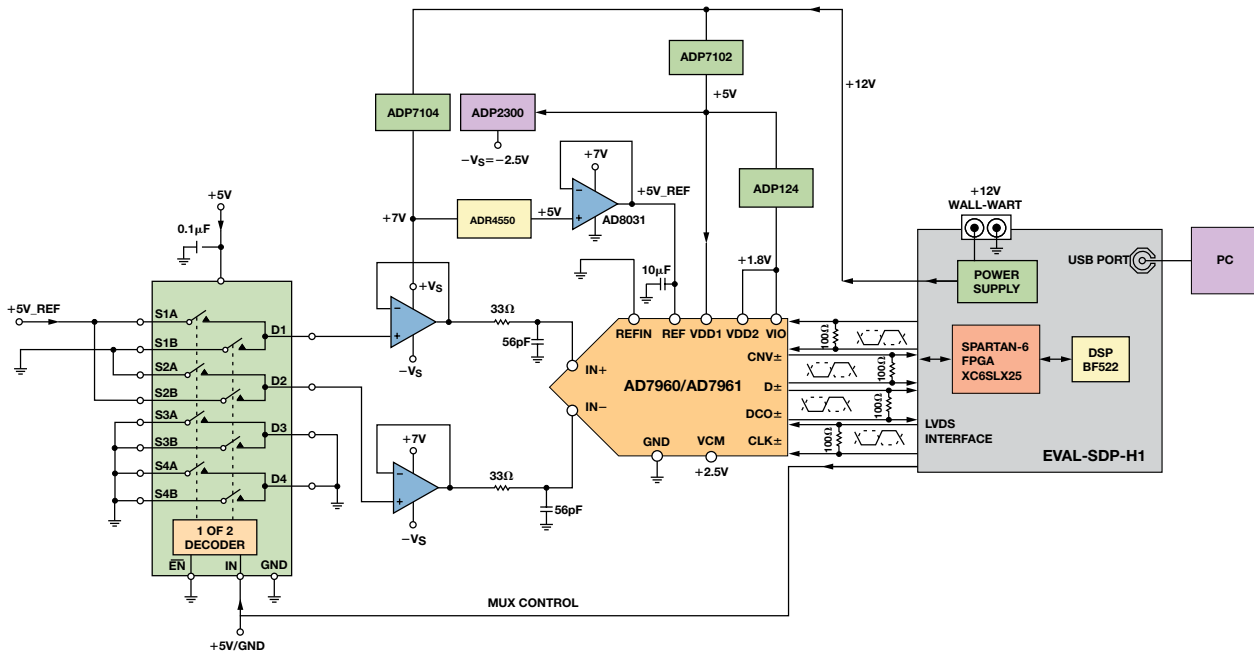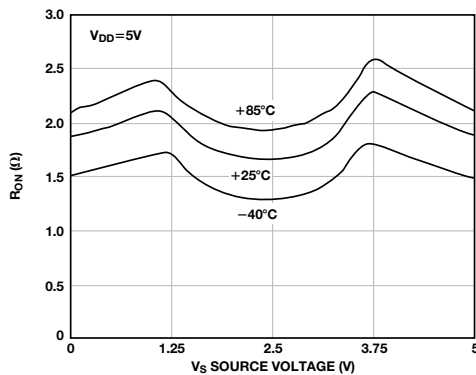**Figure 4.** Simplified signal chain for a multiplexed data–acquisition system.



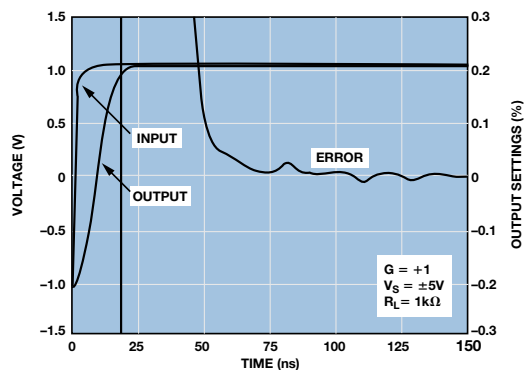**Figure 5.** ADG774 on–resistance vs. input voltage.



**Figure 6.** Typical settling time of the ADA4899–1.

(VDD2 and VIO) supplies, it dissipates only 46.5 mW at 5 MSPS when converting in echoed-clock mode. Its core power dissipation scales linearly with throughput, making it well-suited for low-power applications with high channel density. The 5 V and 1.8 V supplies can be generated by low-noise LDOs such as ADP7104 and ADP124.

The ADC's full-scale differential input range is set to 5 V or 4.096 V by an external reference. To fully use its dynamic range, the input signals must swing from 0 to $V_{REF}$. In this signal chain, the 5-V reference is supplied by the ADR4550 high-precision (±0.02% max initial error), low-power (950 μA max operating current) voltage reference, which features excellent temperature stability and low output noise. The AD8031 rail-to-rail op amp buffers the external reference. Stable with large capacitive loads, it can drive the decoupling capacitors required to minimize voltage spikes caused by transient currents. The AD8031 is ideal for a wide range of applications, from battery-operated systems with wide bandwidth to high-speed systems where high component density requires low power dissipation.

The AD7960 digital interface offers self-clocked and echoed-clock modes using low-voltage differential signaling (LVDS) to enable high-speed data transfer up to 300 MHz (CLK± and D±) between the ADC and the digital host. The LVDS interface allows multiple devices to share a common clock, reducing the number of digital lines and easing signal routing. The lower power dissipation as compared to parallel interfaces is especially useful in multiplexed applications.

The AD7960 returns to acquisition mode about 115 ns after the start of conversion, leaving about 40% of the total 200-ns cycle time to acquire the signal. This relatively long acquisition time relaxes the burden on the amplifier's bandwidth and settling time requirements and makes the differential inputs easier to drive. The 5-MSPS throughput rate allows multiple channels to be multiplexed at fast scan rates, so fewer ADCs are required in high-channel-count systems.

During the conversion, the AD7960 has a quiet-time requirement at 90 ns to 110 ns where the multiplexer inputs must not be switched. Thus, to avoid corrupting the ongoing conversion, the external multiplexer must be switched to less than 90 ns or more than 110 ns after the rising edge of the CNV± start signal. If the analog inputs are switched during this quiet time, the current conversion may be corrupted by up to 15 LSBs. The analog inputs should be switched as early as possible to allow the maximum time to slew a full-scale signal and settle the input.

After every 16 conversions, the multiplexer switches between −5 V and +5 V about 10 ns after the rising edge of CNV±, as shown in Figure 7. This creates a full-scale differential step, so the ADC output change from negative full-scale to positive full-scale as shown in Figure 8.
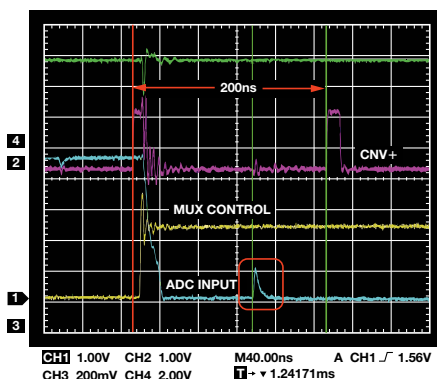


*Figure 7. Oscilloscope plot shows kickback from the internal CAP DAC.*
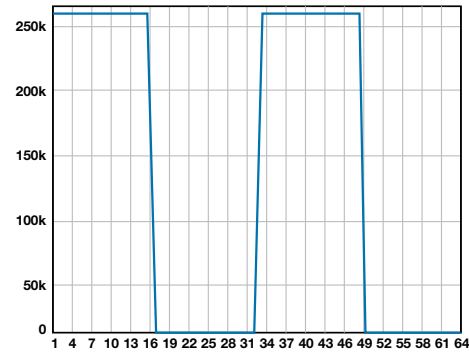


*Figure 8. AD7960 output shows the ADG774 switching after every 16 conversions.*

This switching time delay must be greater than the ADC's 1.6-ns aperture delay. The signal measured at the ADC input shows about 1-V p-p kickback (Figure 7, highlighted in red) from the capacitive DAC in the AD7960. To ensure that the output is fully settled, the driver amplifier must settle this transient before the next conversion starts, within the approximately 80-ns acquisition time of the ADC when running at 5 MSPS. Running the ADC at lower throughput rates provides more acquisition time to settle this kickback, resulting in a lower crosstalk error between the multiplexer input channels and better settling time to a full-scale step.

The signal measured at the multiplexer input also shows a kickback from the channel switching. A buffer amplifier at the multiplexer inputs helps to settle this kickback. If the input buffer amplifier cannot be used for cost or space reasons, an optimized RC filter can be added to the inputs to reduce the effect of the kickback and crosstalk. The value of RC filter used on the multiplexer inputs impacts the overall noise and settling time of the signal chain.

When the multiplexer is static, the output of the data-acquisition system with the AD7960 running at its maximum 5-MSPS throughput rate is about 14 LSBs away from nominal full scale, representing the system's overall gain and offset error. When the multiplexer is switching, the ADA4899-1 driver amplifier helps to settle the output to positive and negative full scale within an acceptable channel-to-channel crosstalk error for most applications. The output error scales exponentially with throughput, reaching a maximum of 0.01% at 5 MSPS, as shown in Figure 9. The zero crosstalk error at lower throughput rates shows that the ADC output settles to its final value during the first conversion.



*Figure 9. Crosstalk error vs. throughput as a percentage of full-scale amplitude.*

As shown in Figure 10, the crosstalk error relative to full scale is less than 0.001% at 1 V p-p (10% of full scale), and scales linearly with differential input amplitude. The crosstalk error relative to step amplitude is almost flat over the full input span and is always less than 0.01%.

*Figure 10. Crosstalk error vs. differential input signal.*
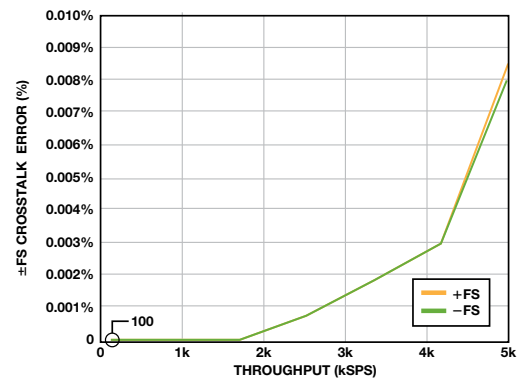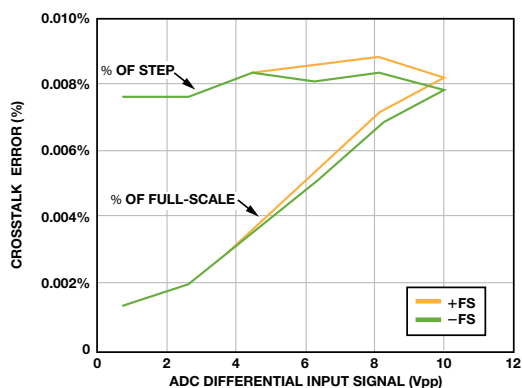
This multiplexed signal chain offers optimized performance with the best noise vs. settling time trade-off. These results demonstrate that a wide bandwidth, fast-settling amplifier is required to settle the large voltage step and kickback from the ADC input and to reduce the magnitude of the crosstalk error when multiplexing.

## Multiplexed Data–Acquisition System Layout Considerations

The printed circuit board (PCB) layout is critical for preserving signal integrity and achieving the expected performance from the signal chain. Figure 11 shows the top of the 69-mm × 85-mm, four-layer evaluation board. Care must be taken with the placement of individual components and routing of various signals on the board. In this case, the input signal is routed from left to right. All of the power supplies and reference pins of the ADC must be decoupled with capacitors placed close to the DUT and connected using short, wide, low-impedance traces, to provide a path for high-frequency currents, minimize EMI susceptibility, and reduce the effect of glitches on the power-supply lines. From the data sheet, recommended values are typically 10 µF and 100 nF. Ground and power planes should be removed beneath the input and output pins of the multiplexer, amplifiers, and ADC to avoid undesired parasitic capacitance. The exposed paddle of the device should be soldered directly to the ground plane of the PCB using multiple vias. Separate sensitive analog and digital sections while keeping the power supply circuitry away from the analog signal path. Fast switching signals, such as CNV± or CLK±, should not run near or cross over analog signal paths to prevent noise coupling to the ADC.

## Multiplexed Data–Acquisition Applications

The high-performance, multichannel data-acquisition systems used in industrial automation and medical imaging demand wide bandwidth, high accuracy, and fast sampling—all in a small, low-cost form factor. The 5-MSPS throughput rate of the 18-bit AD7960 and 16-bit AD7961 allows more channels to be multiplexed into fewer ADCs, while significantly reducing the cost, power dissipation, and package size. This helps designers meet space, thermal, power, and other key design challenges common to high-channel-density systems.

The excellent linearity and low noise provide enhanced image quality in computed tomography (CT) and digital X-ray (DXR) applications. Switching many channels at high sampling rates into fewer ADCs allows a shorter scanning period and decreased exposure to the X-ray dosage, providing an accurate, affordable diagnosis and a better patient experience. In CT scanners, the pixel current is captured continuously using a single integrator and track-and-hold per channel, with outputs multiplexed to a high-speed ADC. A low-noise analog front end transforms the small current from each pixel into a large voltage, which is then converted into digital data that can be processed.

Multiplexed medical imaging systems, especially CT and DXR, specify typical pixel-to-pixel crosstalk error of ±0.1% from adjacent pixels and ±0.01% from nonadjacent pixels. The results presented here suggest that the crosstalk error generated from this multiplexed signal chain is well within the acceptable limits, even at maximum throughput and full-scale range.
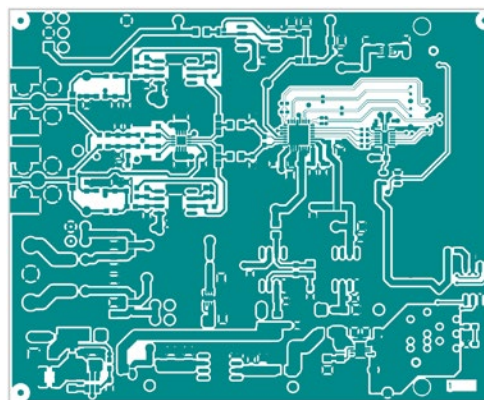


*Figure 11. Top layer of evaluation board for a multiplexed data–acquisition system.*

## Conclusion

High-performance, high-channel-density, multiplexed data-acquisition systems demand reliable performance, functional flexibility, and high accuracy, while meeting power, space, and thermal constraints. This article provides guidelines for choosing multiplexed signal chain components with key design considerations to meet the expected performance, and insights on the trade-offs among throughput, settling time, and noise. This signal chain achieves optimized performance with less than 0.01% of crosstalk error at 5 MSPS at full-scale range.

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Also by this Author:

High–Performance Data–Acquisition System Enhances Images for Digital X–Ray and MRI

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# Accurate Analog Controller Optimizes High-Efficiency Li-Ion Battery Manufacturing

By Wenshuai Liao and Luis Orozco

Energy conservation and environmental protection play an important role in people's daily lives, with the introduction of affordable hybrid and electric vehicles increasing awareness even more. Both technologies use a large quantity of rechargeable batteries, with high-quality, high-power Li-Ion cells representing the best solution at this time. These batteries have been widely used in laptop computers, cell phones, digital still cameras, camcorders, and other portable equipment, but manufacturing efficiency has not been a major concern because of their low storage capacity, typically fewer than 5 Ah per cell or cell pack. A typical cell pack contains fewer than a dozen cells, so matching is also not a major concern.

One approach to energy conservation is storing energy during nonpeak times to compensate for peak usage. Batteries used for vehicles or energy storage have much higher capacity, typically in the hundreds of amp-hours. This is achieved with a large number of small cells or a few high-capacity batteries. For example, one electric vehicle model uses about 6800 type-18650 Li-Ion cells, weighing up to 450 kg. Because of this, faster battery manufacturing with higher efficiency and better control is required to meet market needs at a lower cost.

## Li-Ion Battery Manufacturing Overview

Figure 1 shows an overview of the Li-Ion battery manufacturing process. Battery formation and testing at the end-of-line conditioning step are the process bottlenecks, in addition to having the greatest impact on battery life and quality.

With today's technology, formation must be done at the cell level, and can take hours, or even days, depending on the battery chemistry. A 0.1-C (C is the cell capacity) current is typically used during formation, so it would take 20 hours to go through a full charge and discharge cycle. Formation can account for 20% to 30% of the total battery cost.
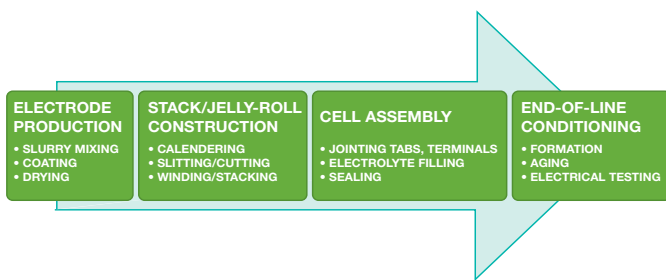


*Figure 1.* Li-Ion battery manufacturing process.

Electrical testing typically uses a 1-C charging current and a 0.5-C discharge current, but each cycle still requires one hour to charge the battery and two hours to discharge it, and a typical test sequence encompasses several charge-discharge cycles.

Formation and electrical testing have stringent accuracy specifications, with the current and voltage controlled to within ±0.05%. In contrast, the accuracy can be ±0.5% for voltage and ±10% for current when charging batteries in portable equipment such as cell phones and laptops. Figure 2 shows typical Li-Ion charge and discharge profiles.
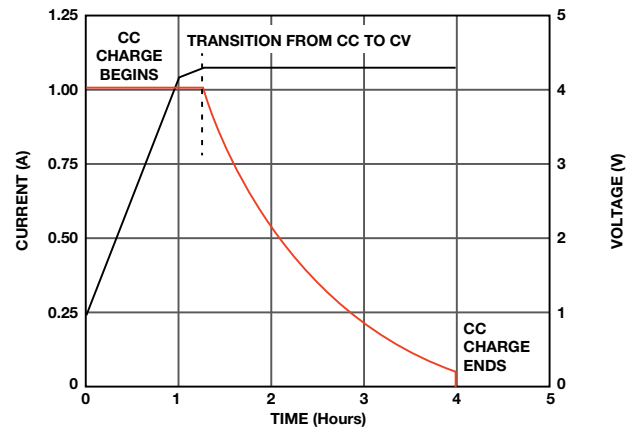


*Figure 2.* Typical Li-Ion cell charge and discharge profiles.

## Linear or Switching Formation and Testing System

The top factors that must be taken into account when selecting a manufacturing method are power efficiency, system accuracy, and cost. Other factors like small size and easy maintenance are also important, of course.

To meet the high-accuracy requirements in battery manufacturing, system designers traditionally use linear voltage regulators, which easily meet the accuracy requirements but have low efficiency. With low-capacity batteries, this may be a good trade-off, but some manufacturers can still use switching technology to their advantage. The decision hinges on efficiency, channel cost, and current. As a guideline, switching technology will provide higher efficiency at the same per-channel cost for cells with higher than 3 Ah capacity. Table 1 shows a comparison of different cell categories in terms of power capacity and end function.

## Table 1. Comparison of Linear and Switching Systems

| Battery Size | Small | Medium | Large |
|---|---|---|---|
| Capacity (Ah) | Less than 2 | 10 to 15 | 30 to 100 |
| Applications | Cell phone, digital still camera, camcorder | Laptop computer | HEV, EV, scooter |
| Number of Channels | ~512 | ~768 | 16 to 64 |
| Technical Requirements | Lower drift over temperature and time | Higher accuracy over temperature and time | Highest accuracy over temperature and time; current sharing |
| Tester Topology | Linear; lower efficiency | Linear or switching; trend toward switching | Switching; higher efficiency; energy recycling |

To produce batteries faster and at lower cost, systems use hundreds or thousands of channels in the formation and testing steps, with the topology of the tester depending on the system's total energy capacity. High current flow in the tester will cause the temperature to rise significantly, increasing the challenge of maintaining high measurement accuracy and repeatability over time.

During the discharge phase, the stored energy must go somewhere. One solution is to discharge the batteries into resistive loads, converting the energy into wasted heat. A much better solution is to recycle the energy, using precision control to feed current from the discharging cells into another group of charging cells. This technique achieves significantly higher tester efficiency.

The energy balance is typically implemented via a dc bus and a bidirectional PWM converter on each cell. The dc bus voltage, which depends on the particular system, can be 12 V, 24 V, or even up to 350 V. For the same amount of power, lower voltage buses have higher currents and higher losses due to conductor resistance. Higher voltages have additional safety concerns and require expensive power and isolation electronics.

Figure 3 shows a typical switching topology for energy recycling. The energy can be recycled directly between cells (red path), between cells via a dc-link bus (green path), or it can be returned to the power grid (purple path). These flexible, high-efficiency designs can result in lower production costs and can achieve better than 90% efficiency.

Although this technology offers many benefits, it also introduces several technical challenges. The voltage and current control loops must be fast enough, and must maintain high accuracy over time and temperature. Using air or water cooling is helpful, but it's more important to start with low-drift circuits. The system includes switching power supplies, so the supply ripple must be suppressed at a reasonable cost. It is also important to minimize the time it takes to calibrate the system, as it does not generate revenue when down for calibration.

## Control–Loop Design: Analog or Digital

Each system has one loop for voltage control and another for current control, as shown in Figure 4. For cells used in vehicles, fast-ramping current is required during vehicle acceleration, so this has to be simulated during testing. The fast rate of
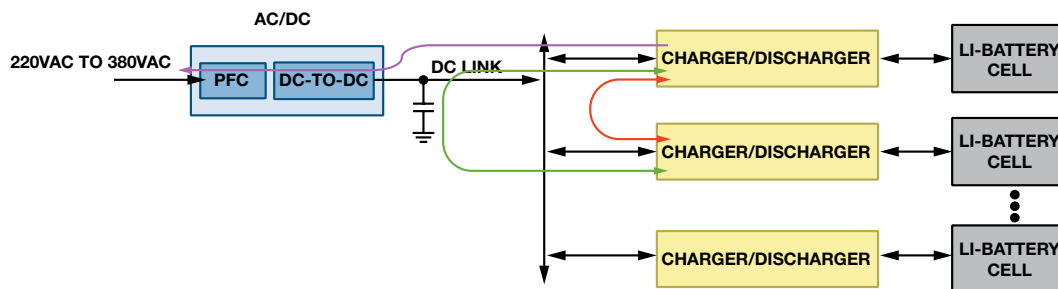


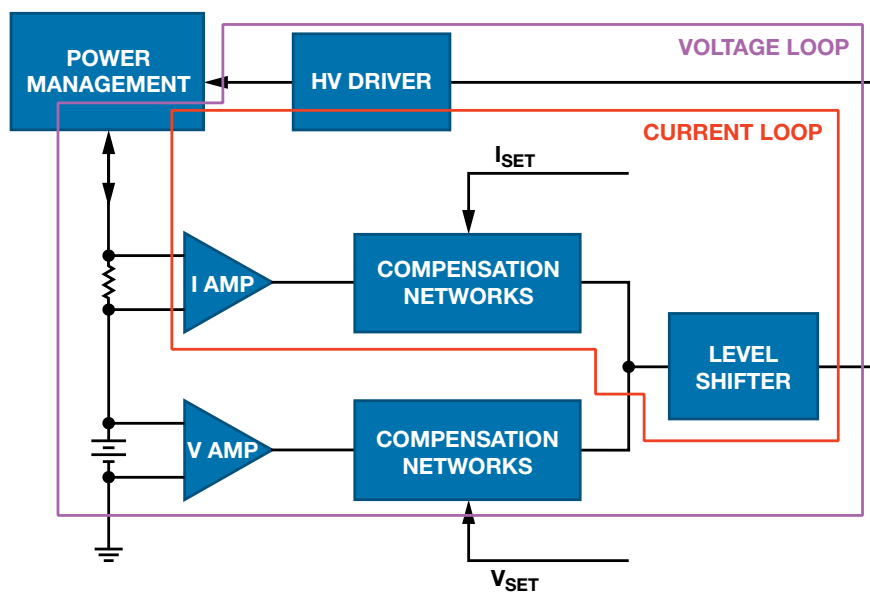Figure 3. Switching systems with power–recycling feature.



Figure 4. Control loops in battery manufacturing systems.

change and wide dynamic range make the current control loop a challenge to design.

A system requires four different control loops, which may be implemented in either analog or digital domains: constant current (CC) charge, CC discharge, constant voltage (CV) charge, and CV discharge. Switching between CC and CV modes must be clean, without glitches or peaks.

Figure 5 shows a block diagram of a digital control loop. The microcontroller or DSP continuously samples the voltage and current; a digital algorithm determines the duty cycle for the PWM power stage. This flexible method allows field upgrades and bug fixes, but has a few drawbacks. The ADCs must sample at more than twice the loop bandwidth, with most systems sampling at 10 times the loop bandwidth. This means that the bipolar-input ADC must run at 100 kSPS to

cover charge and discharge modes with a single converter and shunt resistor. Some designers use 16-bit, 250-kSPS ADCs for faster, higher-accuracy systems. As part of the control loop, the ADC's accuracy sets the overall system accuracy, so it is important to select fast, low-latency, low-distortion ADCs, such as the 6-channel, 16-bit, 250-kSPS AD7656.

In multichannel systems, each channel will typically require a microcontroller and a set of dedicated ADCs. The microcontroller handles the data acquisition, digital control loop, PWM generation, control, and communication functions, so its processing capability must be very high. In addition, because the processor has to handle multiple parallel tasks, jitter in the PWM signal can be a problem, especially when the PWM duty cycle is low. As part of the control loop, the microprocessor affects the loop bandwidth.
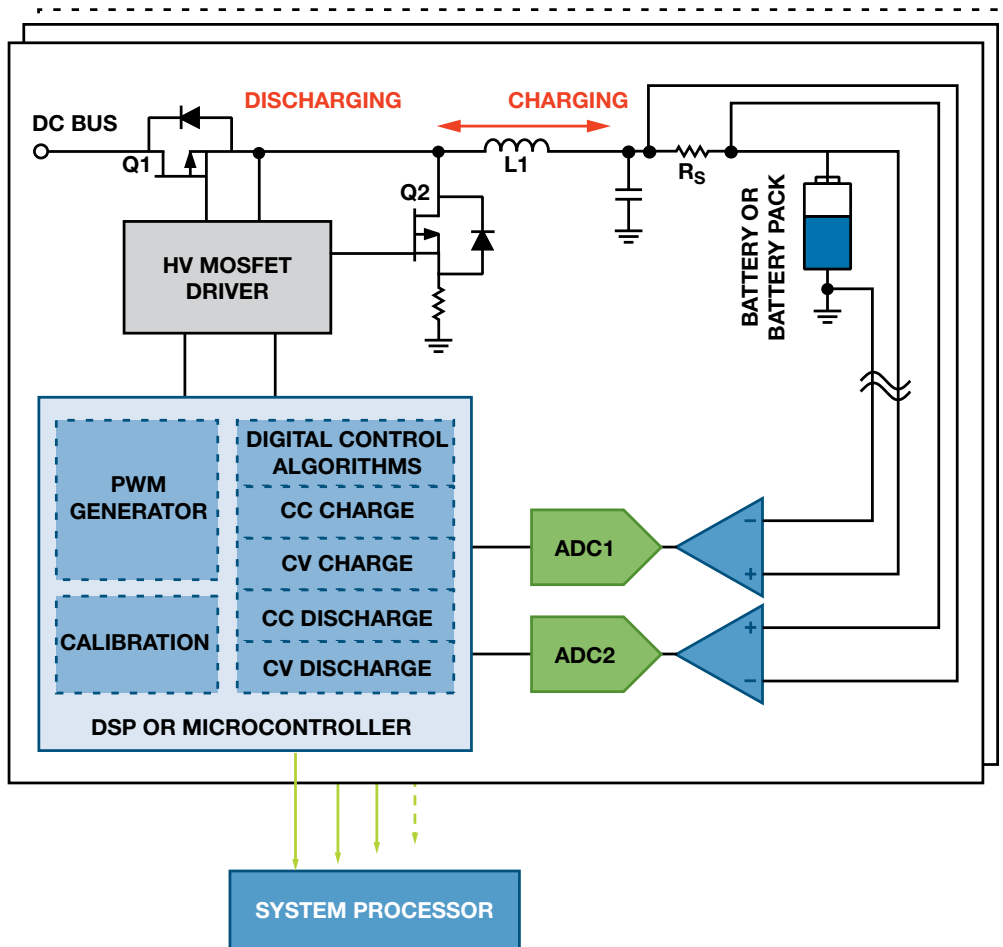


Figure 5. Digital control loops.

Figure 6 shows a battery test system that uses analog control loops. Two DAC channels control the CC and CV set points. The AD8450/AD8451 precision analog front end and controller for battery test and formation systems measures the battery voltage and current, and compares it to the setpoints. The CC and CV loops determine the duty cycle of the MOSFET power stage. When the mode changes from charge to discharge, the polarity of the in-amp that measures the battery current reverses to ensure that its output remains positive and switches inside the CC and CV amplifiers select the correct compensation network. This entire function is controlled via a single pin with standard digital logic.

In this implementation, the ADC monitors the system, but it's not part of the control loop. The scan rate is unrelated to control-loop performance, so a single ADC can measure cur-rent and voltage on a large number of channels in multichannel systems. This is true for the DAC as well, so a low-cost DAC can be used for multiple channels. In addition, a single processor only needs to control the CV and CC set points, mode of operation, and housekeeping functions, so it can interface with many channels. The processor doesn't deter-mine the control-loop performance, so high performance isn't required.

The ADP1972 PWM generator uses a single pin to control buck- or boost-mode operation. The interface between the analog controller and the PWM generator consists of low-impedance analog signals that don't suffer from the jitter that causes problems in the digital loop. Table 2 shows how an analog loop can offer higher performance and lower cost than a digital loop.
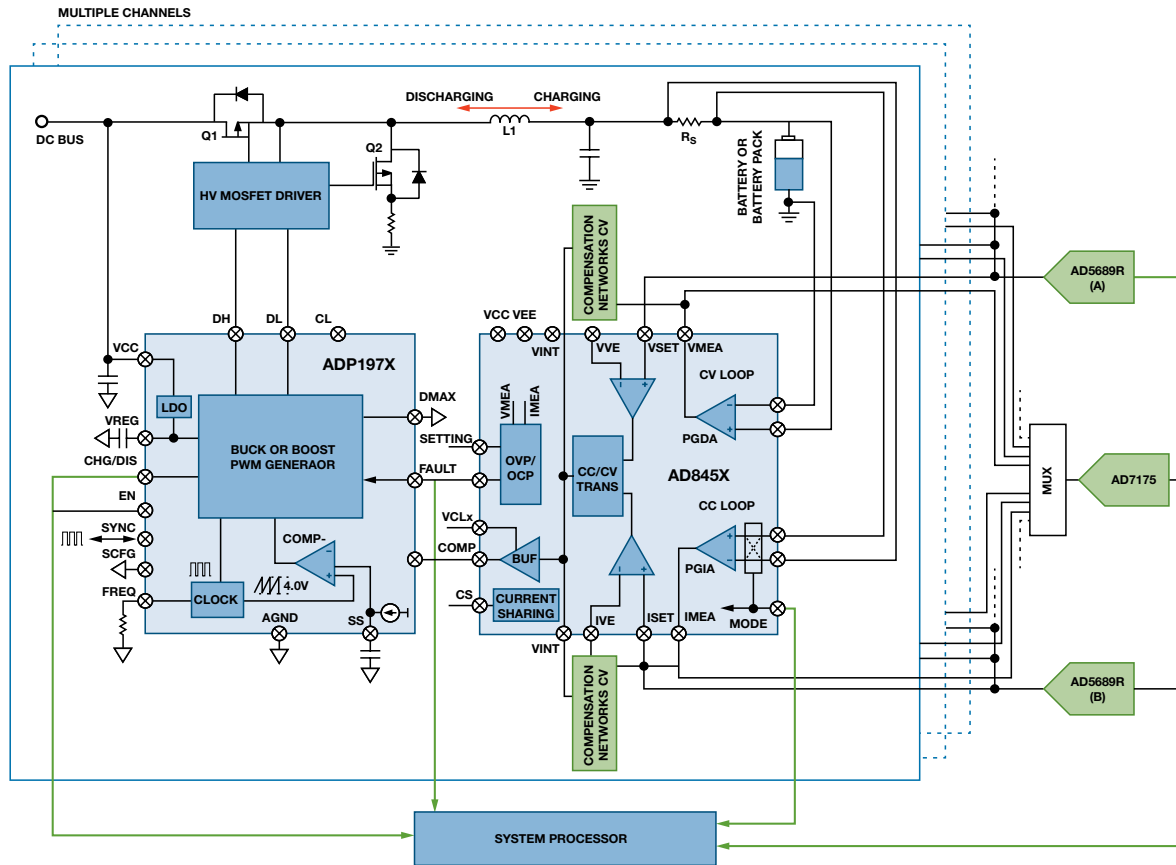


Figure 6. Analog control loop.

### Table 2. Comparison of Analog and Digital Control Loops

|  | Digital Solution | Analog Solution | Analog Benefits |
|---|---|---|---|
| Loop Bandwidth | Varies with amplifier, ADC, microprocessor; 20 kHz with 250–kSPS ADC | Depends on amplifiers; 1.5 MHz for AD845x at G = 66 | Faster control |
| Accuracy | 0.05% or worse; depends on ADC and algorithm | 0.04% or better; depends on AD845x | Higher accuracy |
| Switching Frequency | Depends on algorithm and microprocesor speed; low–frequency jitter | Up to 300 kHz; depends on ADP1972; clean PWM output | Lower–cost power solution |
| Power Efficiency | Trade-off between resources and buck/ boost switching frequency | 90%+; no limitation from chipset | Higher efficiency |
| Power Electronics | Large, expensive components | Small, low-cost component | Smaller; lower cost |
| Converter Sharing | No; expensive, dedicated bipolar–input ADC | Yes; multichannel, low voltage unipolar ADC | Lower cost |
| Total Solution | Expensive ADCs and power electronics; large software investment | Low-cost ADCs and power electronics; no software required | Lower cost including hardware, calibration, and operation; higher performance |

## System Accuracy over Temperature

Calibration will remove most of the initial system errors. Remaining errors include the amplifier CMRR, the nonlinearity of the DAC used to control the current and voltage set points, and errors due to temperature drift. Manufacturers specify different temperature ranges, but 25°C ± 10°C is one of the most common, and will be used in this example.

This design uses a battery that varies from 2.7 V when fully discharged to 4.2 V when fully charged, a full-scale current of 12 A using a 5-mΩ shunt, a gain of 66 for the AD8450's current-sense amplifier, and a gain of 0.8 on the diff-amp that measures the battery voltage.

The current-sense resistor drift can account for a large part of the total system error. A Vishay bulk metal resistor; part number Y14880R00500B9R, with a 15-ppm/°C maximum temperature coefficient, reduces drift. The AD5689 dual 16-bit *nano*DAC+™ digital-to-analog converter, which specifies 2-LSB maximum INL, reduces nonlinearity. The ADR4540 4.096-V reference, which specifies a 4-ppm/°C maximum temperature coefficient, is a good compromise between current and voltage setpoints. The DAC INL adds about 32 ppm of full-scale error after dividing by the current-sense amplifier gain of 66, and the reference contributes 40 ppm of gain error.

The current-sense amplifier has 116-dB minimum CMRR at a gain of 66. If the system is calibrated with a 2.7-V battery, a 40-ppm full-scale error would occur with a 4.2-V battery. In addition, the CMRR will vary by 0.01 μV/V/°C, or 0.1μV/V

over the 10°C temperature range. The offset voltage drift of the current-sense amplifier is 0.6 μV/°C max, so a 10°C temperature excursion would result in 6 μV of offset, or 100 ppm of full scale.

Finally, the gain drift of the current-sense amplifier is 3 ppm/°C max, for a total drift of 30 ppm over 10°C. The sense resistor drift is 15ppm/°C, so it adds 150-ppm gain drift over 10°C. Table 3 summarizes these error sources, which produce a total full-scale error of just under 0.04%. A big percentage of this error is from the shunt resistor, so a lower drift shunt resistor can be used to improve system accuracy if necessary.

Similarly, for the voltage input, the 2-LSB DAC INL is equivalent to 31 ppm error referred to the 5.12-V full-scale input. As the battery voltage changes between 2.7 V and 4.2 V, the diff-amp's 78.1-dB CMRR creates 187-μV offset error, or 36.5 ppm of full scale. The additional error from CMRR drift is well under 1 ppm, so we can neglect it.

The offset drift of the diff-amp is 5 μV/°C, or 10 ppm of full scale over 10°C. The gain drift of the diff-amp is 3 ppm/°C, or 30 ppm over 10°C. The reference drift is 40 ppm over 10°C. The total voltage error is 0.015% maximum, as summarized in Table 4.

Achieving high accuracy on the current measurement is more difficult than on the voltage measurement because of the smaller signal level and wider dynamic range. The shunt resistor and in-amp offset drift cause the largest errors over temperature.

### Table 3. Current Measurement Error over 10°C Range

| Error Source | Error | Units |
|---|---|---|
| AD5689R INL | 31 | ppm FS |
| AD8450 CMRR | 40 | ppm FS |
| AD8450 Offset Drift | 100 | ppm FS |
| AD8450 CMRR Drift | 3 | ppm FS |
| **Total Offset Error** | **174** | **ppm FS** |
| ADR4540A Drift | 40 | ppm reading |
| AD8450 Gain Drift | 30 | ppm reading |
| Shunt–Resistor Drift | 150 | ppm reading |
| **Total Gain Drift** | **220** | **ppm reading** |
| **Total Error** | **0.039** | **% FS** |

### Table 4. Voltage Measurement Error over 10°C Range

| Error Source | Error | Units |
|---|---|---|
| AD5689R INL | 31 | ppm FS |
| AD8450 CMRR | 36 | ppm FS |
| AD8450 Offset Drift | 10 | ppm FS |
| AD8450 CMRR Drift | Negligible | ppm FS |
| **Total Offset Error** | **77** | **ppm FS** |
| ADR4540A Drift | 40 | ppm reading |
| AD8450 Gain Drift | 30 | ppm reading |
| **Total Gain Drift** | **70** | **ppm reading** |
| **Total Error** | **0.015** | **% FS** |

## Reducing Calibration Time

The system calibration time can be several minutes per channel, so reducing it can reduce manufacturing cost. At 3 minutes per channel, it would take 4.8 hours to calibrate a 96-channel system. The voltage and current measurement paths are different due to the change in current polarity, and the offset and gain errors will be different for each mode, so they must be calibrated separately. Without low-drift components, temperature calibration would have to be done for each mode, making the calibration time very long.

When the AD845x changes between charge and discharge mode, an internal multiplexer changes the current polarity before it reaches the in-amp and other signal conditioning circuits. Thus, the in-amp will see the same signal regardless of whether it is in charge or discharge mode, and the gain error will be the same in both modes, as shown in Figure 7. The multiplexer resistance will differ in charge and discharge modes, but the high input impedance of the in-amps allows this error to be neglected.

From the system design point of view, having the same offset and gain error in both modes means a single calibration can remove the initial errors in both charge and discharge modes, cutting the calibration time in half. In addition, the very low drift of the AD845x makes a single, room-temperature calibration sufficient, rather than having to calibrate at different temperatures. The time savings can turn into significant cost savings considering the calibration required over the life of the system.

## Reducing Ripple

One of the concerns for system designers moving from linear topology to switching topology is the ripple in the voltage and current signals. Every switching power system will have some ripple, but the technology is evolving fast, driven by the voltage-regulator modules in PCs and other high-volume power management applications that require high efficiency at low cost. With careful circuit design and PCB layout, the ripple can be reduced to a level where a switching power supply can power a 16-bit ADC without degrading its performance, as explained in AN-1141 Application Note, *Powering a Dual Supply Precision ADC with Switching Regulators*. In addition, the data sheet of the ADP1878 synchronous buck controller provides more information on high-power applications. Most switching supplies use a single-stage LC filter, but a two-stage LC filter can be helpful if better ripple and higher system accuracy are needed.

## Current Sharing

The AD8450 allows easy, pure analog current sharing, making it a fast, cost-effective way to combine multiple channels for formation and testing of high-capacity cells. For example, a 5-V, 20-A single-channel design can be leveraged to generate a 5-V, 60-A system by combining three identical channels. The current sharing bus and control circuits are implemented by the AD8450 and a few passive parts. Compared with single-channel design, this can be cost effective because low-cost power electronics can be used and no extra development time is needed. Details can be found on the AD8450 data sheet.
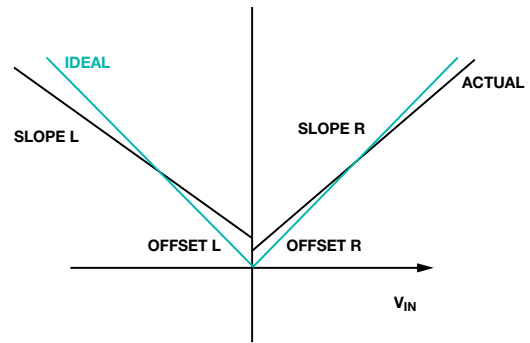


**OFFSET VOLTAGE AND SLOPE ARE DIFFERENT IN TRADITIONAL SOLUTION**
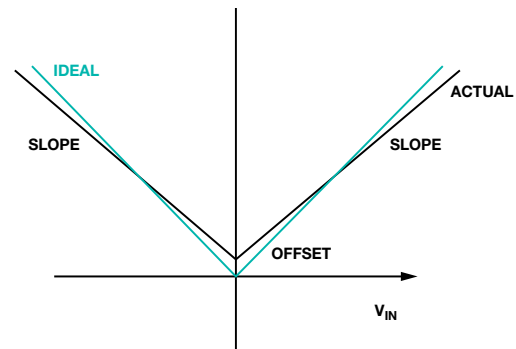


**OFFSET VOLTAGE AND SLOPE ARE THE SAME IN AD845x**

*Figure 7. The AD845x has the same offset and slope in both charge and discharge modes.*

# Understanding Switching Regulator Output Artifacts Expedites Power Supply Design

By Aldrick S. Limjoco

## Introduction

Minimizing output ripple and transients from a switching regulator can be important, especially when powering noise-sensitive devices such as high-resolution ADCs, where the output ripple can appear as a distinct spur on the ADC's output spectrum. To avoid degrading the signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR), the switching regulator is often replaced with a low-dropout regulator (LDO), trading the high efficiency of the switching regulator for the cleaner output of the LDO. Understanding these artifacts will allow designers to successfully integrate switching regulators in a wider range of high-performance, noise-sensitive applications.

This article describes effective techniques for measuring output ripple and switching transients in switching regulators. Measuring these artifacts requires great care, as a poor setup can lead to incorrect readings, with the loops formed by the oscilloscope probe's signal and ground leads introducing parasitic inductance. This increases the amplitude of the transients associated with fast switching transitions so short connections, good techniques, and wide bandwidth must be maintained. Here, the ADP2114 dual 2-A/single 4-A synchronous step-down dc-to-dc converter is used to demonstrate techniques for measuring output ripple and switching noise. This buck regulator provides high efficiency and operates at switching frequencies up to 2 MHz.

## Output Ripple and Switching Transients

Output ripple and switching transients depend on the regulator's topology, as well as the values and characteristics of the external components. Output ripple is a residual ac-output voltage that is coherently related to the switching operation of the regulator. Its fundamental frequency is the same as the regulator's switching frequency. Switching transients are high-frequency oscillations that occur during switching transitions. Their amplitude, expressed as a maximum peak-to-peak voltage, is difficult to measure accurately since it is highly dependent on the test setup. Figure 1 shows an example of output ripple and switching transients.
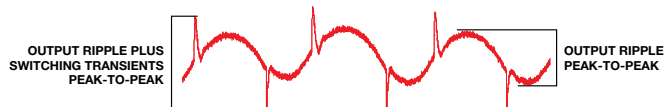


*Figure 1. Output ripple and switching transients.*

## Output Ripple Considerations

The regulator's inductor and output capacitor are the main components that affect output ripple. A small inductor gives faster transient response at the expense of higher current ripple, while a large inductor leads to lower current ripple at the expense of slower transient response. Using a capacitor with low effective series resistance (ESR) minimizes the output ripple. A ceramic capacitor with X5R or X7R dielectric is a good choice. A large capacitance is often used to lower the output ripple, but the size and number of output capacitors comes at the expense of cost and PCB area.

## Frequency Domain Measurement

When measuring unwanted output signal artifacts, it is useful for power engineers to think of the frequency domain, as this provides a better perspective as to which discrete frequencies the output ripple and its harmonics occupy with each corresponding power level. Figure 2 shows an example spectrum. This type of information helps engineers to determine whether the chosen switching regulator is appropriate for their wide-band RF or high-speed converter applications.

To make a frequency domain measurement, connect a 50-Ω coaxial cable probe across the output capacitor. The signal goes through a dc-blocking capacitor and ends with a 50-Ω termination at the input of the spectrum analyzer. The dc-blocking capacitor prevents dc from passing to the spectrum analyzer and avoids dc-loading effects. The 50-Ω transmission environment minimizes high-frequency reflections and standing waves.

The output capacitor is the main source of output ripple, so the measurement point should be as close as possible. The loop from signal tip to ground should be kept as small as possible to minimize additional inductance that may affect the measurement. Figure 2 shows output ripple and harmonics in the frequency domain. The ADP2114 generates 4-mV p-p output ripple at the fundamental frequency under the specified operating conditions.
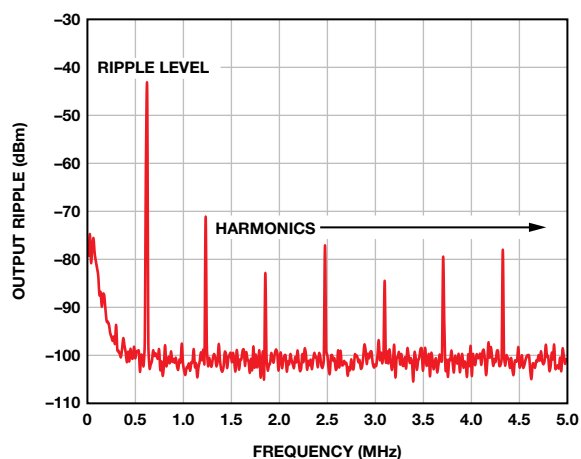


*Figure 2. Frequency domain plot using spectrum analyzer.*

## Time Domain Measurement

When using an oscilloscope probe, avoid ground loops by eliminating long ground leads, as loops formed by the signal tip and long ground leads create additional inductance and higher switching transients.

When measuring low-level output ripple, use a 1× passive probe or a 50-Ω coaxial cable rather than a 10× oscilloscope probe, as the 10× probe attenuates the signal by a factor of 10, pushing the low-level signal down toward the scope noise floor. Figure 3 shows a suboptimal probing method. Figure 4 shows the resulting waveform measured using a 500-MHz bandwidth setting. The high-frequency noise and transients are measurement artifacts due to the loop formed by the long ground lead, and are not inherent to the switching regulator.



*Figure 3. Ground loop causes output errors.*



CH1 5.00Vᴮᵥ  CH3 10.0mV√ᴮᵥ  1.00μs  1.00GS/s  CH1 ⌐ 1.90V
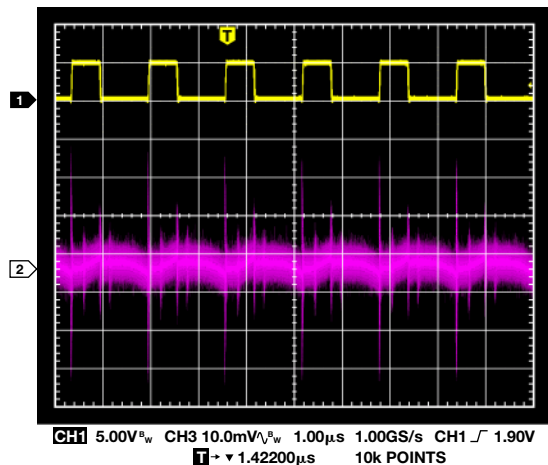T→ ▼ 1.42200μs        10k POINTS

*Figure 4. Switch node (1) and ac-coupled output waveform (2).*

There are a few ways to reduce the stray inductance. One method is to remove the long ground lead from the standard oscilloscope probe, instead connecting the probe's barrel body to the ground reference. Figure 5 shows the tip-and-barrel method. In this case, however, the tip is connected at the wrong point of the regulator output, rather than directly on the output capacitor as it should be. The ground lead was removed, but the inductance caused by the trace on the PC board remains. Figure 6 shows the resulting waveform using a 500-MHz bandwidth setting. The high-frequency noise is smaller because the long ground lead was removed.
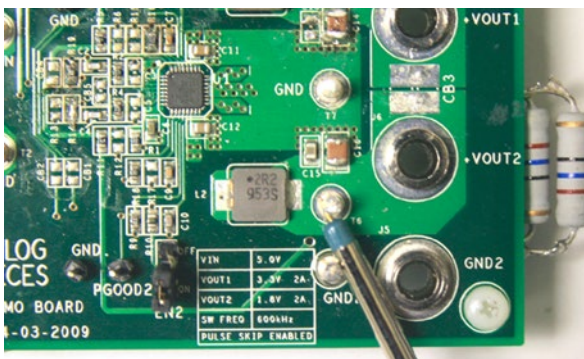


*Figure 5. Tip-and-barrel method probed on random point of switcher's output.*



CH1 5.00Vᴮᵥ  CH3 10.0mV√ᴮᵥ  1.00μs  1.00GS/s  CH1 ⌐ 1.90V
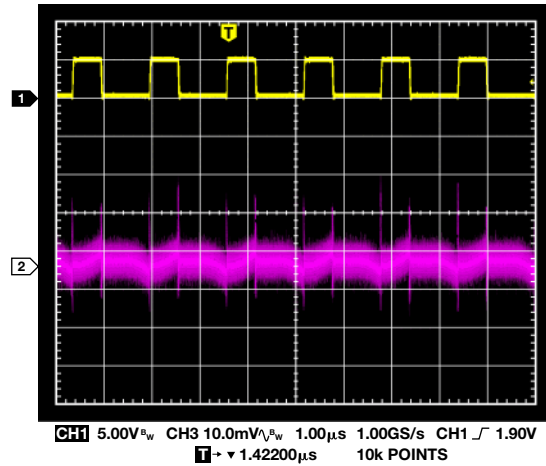T→ ▼ 1.42200μs        10k POINTS

*Figure 6. Switch node (1) and ac-coupled output waveform (2).*

As shown in Figure 7, probing directly on the output capacitor using a grounded coil wire produces nearly optimal detail in the output ripple. Noise at the switching transition is improved, and trace inductance on the PCB is significantly reduced. However, a low-amplitude signal silhouette is still superimposed on the ripple, as shown in Figure 8.
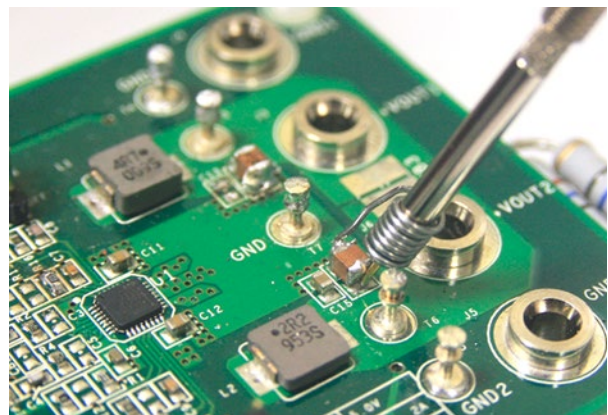


*Figure 7. Tip-and-barrel method probed on output capacitor using coil wire ground.*



CH1 5.00Vᴮᵥ  CH3 10.0mV√ᴮᵥ  1.00μs  1.00GS/s  CH1 ⌐ 1.90V
T→ ▼ 1.42200μs        10k POINTS
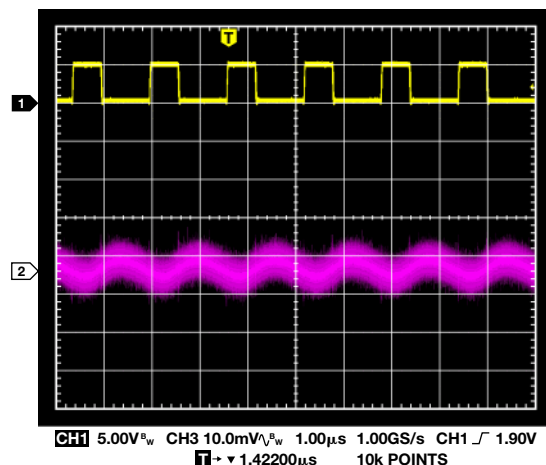
*Figure 8. Switch node (1) and ac-coupled output waveform (2).*

## Best Method

The best method for probing the switcher's output uses a 50-Ω coaxial cable maintained in a 50-Ω environment, and terminated by the oscilloscope's selectable 50-Ω input impedance. A capacitor placed between the regulator's output capacitor and the oscilloscope's input blocks dc flow. The

other end of the cable can be soldered directly to the output capacitor using very short flying leads, as shown in Figure 9 and Figure 10. This preserves signal integrity when measuring very low-level signals over a wide bandwidth. Figure 11 shows a comparison of the tip-and-barrel method and the 50-Ω coaxial method probed on the output capacitor using a 500-MHz measurement bandwidth.
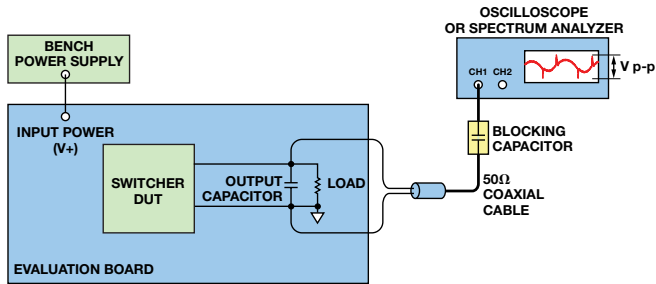


*Figure 9. Best probing method uses an end–terminated 50–Ω coaxial cable.*
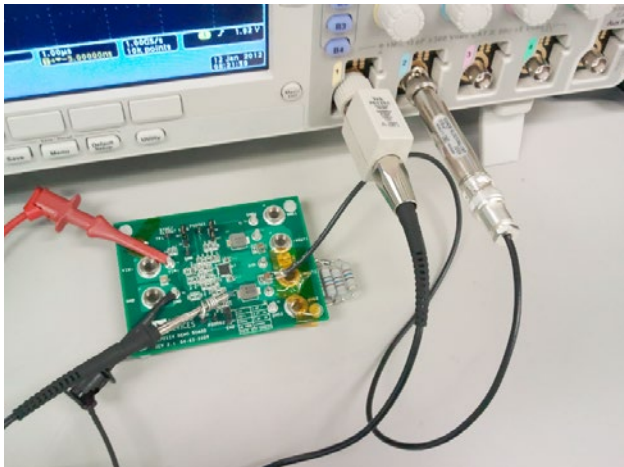


*Figure 10. Example of best probing method.*
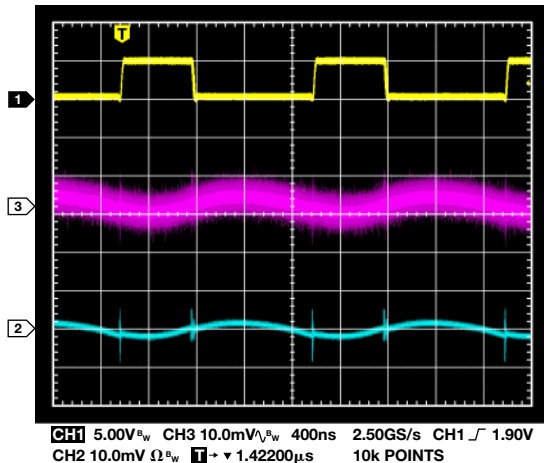


*Figure 11. Switch node (1), tip–and–barrel method (3), and 50–Ω coaxial method (2).*

A comparison of the techniques shows that the coaxial cable in a 50-Ω environment provides more accurate results with less noise, even with a 500-MHz bandwidth. Changing the scope bandwidth to 20 MHz removes the high frequency noise, as shown in Figure 12. The ADP2114 generates an output ripple of 3.9 mV p-p in the time domain, which closely correlates with the measured value of 4 mV p-p using the 20-MHz band-width setting in the frequency domain.
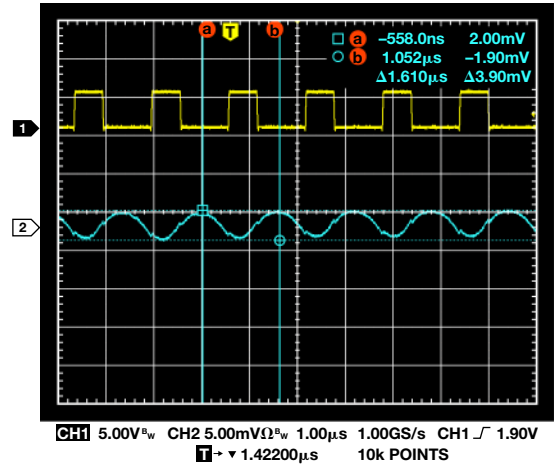


*Figure 12. Switch node (1) and output ripple (2).*

## Measuring Switching Transients

Switching transients have lower energy but higher frequency content than output ripple. This occurs during switching transitions and is often standardized as a peak-to-peak value including the ripple. Figure 13 shows a comparison of switching transients measured using a standard oscilloscope probe with long ground lead and a 50-Ω coaxial termination in a 500-MHz bandwidth. Typically, the ground loop due to the long ground lead generates larger switching transients than expected.
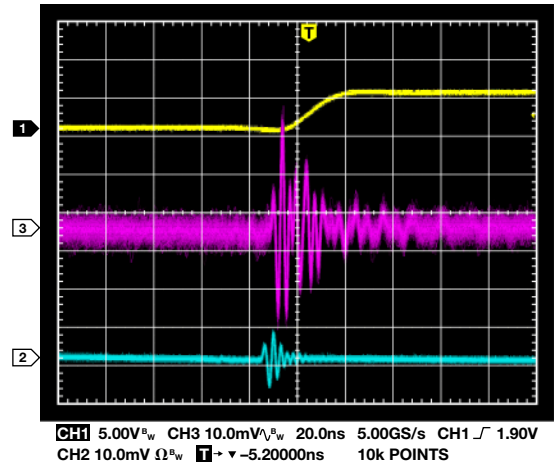


*Figure 13. Switch node (1), standard oscilloscope probe (3), and 50–Ω coaxial termination (2).*

## Conclusion

Output ripple and switching transient measurement techniques are important to consider when designing and optimizing the system power supply for low-noise, high-performance converters. These measurement techniques provide an accurate, reproducible result in both time and frequency domains. It is important to maintain a 50-Ω environment when measuring low-level signals over a wide range of frequencies. A simple, low-cost way to do this is to use a 50-Ω coaxial cable that is properly end terminated. This method can be used with a wide range of switching regulator topologies.

## Acknowledgments

Special thanks to those who contributed to this article: Pat Meehan for his great supervision and technical guidance, Donal O'Sullivan for his technical expertise on test and measurement, Rob Reeder for his valuable comments and technical expertise on analog-to-digital converters, and Manny Malaki and Miles Ramirez for providing their support.

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## Conclusion

A switching power supply provides a high-performance, cost-effective solution for modern rechargeable-battery manufacturing. The AD8450, AD8451, and ADP1972 simplify the system design with better than 0.05% system accuracy and more than 90% power efficiency, helping to solve the rechargeable-battery manufacturing bottleneck problem and contribute to the wider adoption of environmentally friendly technologies.

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Volume 44, Number 4

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Volume 47, Number 2

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# Ask the Applications Engineer—41 LDO Operational Corners: Low Headroom and Minimum Load

## LDO Headroom and Its Effects on Output Noise and PSRR

### By Glenn Morita

The latest multigigahertz analog circuits, built on deep submicron processes, require ever-lower power supply voltages, in some cases less than 1 V. These high-frequency circuits often require a considerable amount of supply current, so thermal management can become difficult. A design goal is to reduce power dissipation to that which is absolutely necessary for circuit performance.

Switch-mode dc-to-dc converters make the most efficient power supplies, with some devices exceeding 95% efficiency, but this high efficiency comes at the cost of increased power-supply noise, often over a wide bandwidth. Low-dropout linear regulators (LDOs) are frequently used to clean up noisy supply rails, but they also present trade-offs, dissipating power and increasing the system's thermal load. To minimize these problems, LDOs can be operated with a smaller difference (headroom voltage) between input and output voltages. This article discusses the impact of low-headroom voltage operation on power-supply rejection and total output noise.

### LDO Power—Supply Rejection vs. Headroom

The LDO power-supply rejection ratio (PSRR) is strongly dependent on headroom voltage—the difference between the input and output voltages. For a fixed headroom voltage, PSRR decreases as the load current increases; this is especially true with large load currents and small headroom voltages. Figure 1 shows the PSRR for the ADM7160 ultralow-noise, 2.5-V linear regulator with 200-mA load current and 200-mV, 300-mV, 500-mV, and 1-V headroom voltages. As the headroom voltage decreases, the PSRR decreases, and the difference can be dramatic. For example, at 100 kHz, changing the headroom voltage from 1 V to 500 mV results in a 5-dB decrease in PSRR. However, a smaller change in headroom voltage, from 500 mV to 300 mV, causes the PSRR to drop more than 18 dB.
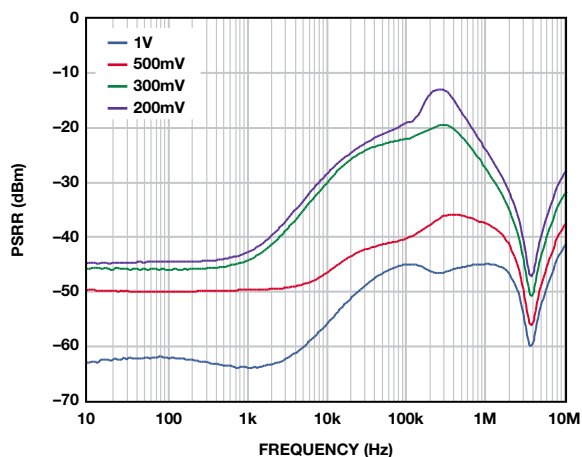


*Figure 1. ADM7160 PSRR vs. headroom.*

Figure 2 shows a block diagram of the LDO. As the load current increases, the gain of the PMOS pass element decreases as it leaves saturation and enters the triode region. This causes the overall loop gain to decrease, resulting in lower PSRR. The smaller the headroom voltage, the more dramatic the reduction in gain. As the headroom voltage continues to decrease, it reaches a point at which the gain of the control loop drops to 1, and the PSRR falls to 0 dB.

Another factor that reduces the loop gain is the resistance of the pass element, which includes the FET's on resistance, the on-chip interconnect resistance, and the wire bonds. An estimate of this resistance can be derived from the dropout voltage. For example, the ADM7160 in the WLCSP package has a maximum dropout voltage of 200 mV at 200 mA. Using Ohm's law, the resistance of the pass element is about 1 $\Omega$. The pass element can be approximated as a fixed resistor plus a variable resistance.

Voltage drops due to the load current flowing through this resistance subtract from the drain-to-source operating voltage of the FET. For example, with a 1-$\Omega$ FET, a load current of 200 mA reduces the drain-to-source voltage by 200 mV. When estimating the PSRR of LDOs operating with 500-mV or 1-V headroom, the voltage drop across the pass element must be taken into account, as the pass FET is effectively operating with only 300 mV or 800 mV.
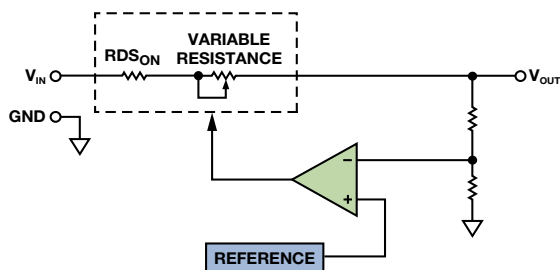


**NOTES**
1. ERROR AMP CONTROLS VALUE OF VARIABLE RESISTOR TO REGULATE OUTPUT VOLTAGE.
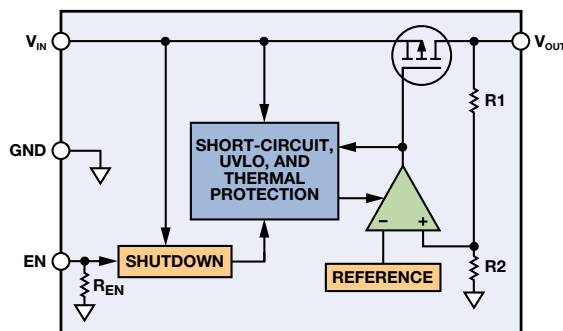2. AT LOW HEADROOM VOLTAGE, THE VARIABLE RESISTOR IS NEARLY 0$\Omega$.

*Figure 2. Block diagram of a low–dropout regulator.*

## Effect of Tolerances on LDO Headroom

Customers often ask applications engineers to help them select an LDO to generate low-noise voltage X from input voltage Y at load current Z, but one factor frequently ignored when setting these parameters is the tolerance of the input and output voltages. As headroom voltage falls to lower and lower values, the tolerance of the input and output voltages can dramatically affect the operating conditions. The worst-case tolerance of the input and output voltages always results in a lower headroom voltage. For example, the worst-case output voltage can be 1.5% high and the input voltage can be 3% low. When a 3.3-V regulator is powered by a 3.8-V source, the worst-case headroom voltage is 336.5 mV, far lower than the expected 500 mV. With the worst-case load current of 200 mA, the drain-to-source voltage of the pass FET is only 136.5 mV. The PSRR of the ADM7160 in this case can be expected to fall far short of the published 55 dB at 10 mA.

## PSRR of an LDO Operating in Dropout

Customers frequently ask applications engineers about an LDO's PSRR in dropout. Initially this may seem like a reasonable question, but a glance at the simplified block diagram will show it to be meaningless. When the LDO is in dropout, the variable resistance portion of the pass FET is zero, and the output voltage is equal to the input voltage minus the voltage drop due to the load current through the $RDS_{ON}$ of the pass FET. The LDO is not regulating and has no gain to reject noise on the input; it is simply operating as a resistor. The $RDS_{ON}$ of the FET forms an RC filter with the output capacitor, providing a small amount of residual PSRR, but a simple resistor or ferrite bead could perform the same job much more cost effectively.

## Maintaining Performance when Operating with Low Headroom

It is imperative to consider the effect of headroom voltage on PSRR when operating at low headroom, as failure to do so will result in a noisier output voltage than expected. PSRR vs. headroom voltage plots, such as that shown in Figure 3, are usually found in the data sheet and can be used to determine the amount of noise rejection possible for a given set of conditions.
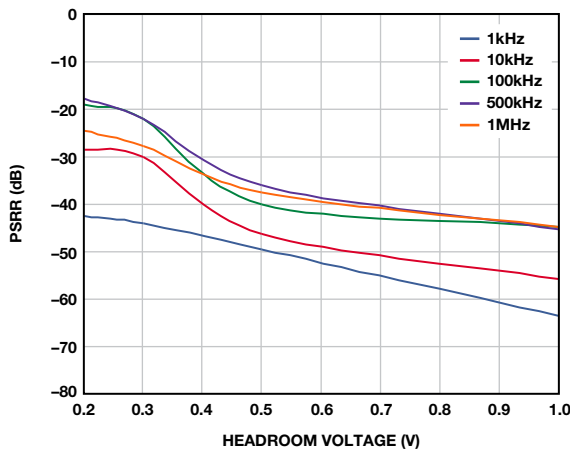


Figure 3. PSRR vs. headroom voltage.

However, it's sometimes easier to see how to apply this information by demonstrating how the LDO's PSRR effectively filters out the noise of the source voltage. The following plots show the impact on the total output noise of an LDO when operating at different headroom voltages.

Figure 4 shows the output noise of a 2.5-V ADM7160 with 500-mV headroom and 100-mA load compared to the baseline noise of an E3631A bench supply, which specifies less than 350-μV-rms noise from 20 Hz to 20 MHz. The many spurs below 1 kHz are harmonics related to rectification of the 60-Hz line frequency. The broad spur above 10 kHz is from the dc-to-dc converter that generates the final output voltage. The spurs above 1 MHz are due to RF sources in the environment unrelated to the power-supply noise. The measured noise of the supply used for these tests is 56 μV rms from 10 Hz to 100 kHz and 104 μV rms including the spurs. The LDO rejects all of the noise on the power supply, and has about 9-μV-rms output noise.
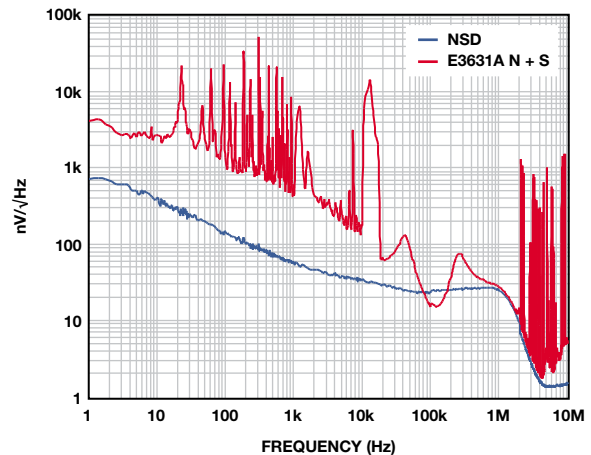


Figure 4. ADM7160 noise spectral density with 500 mV headroom.

As the headroom voltage drops to 200 mV, the noise spurs above 100 kHz begin to poke though the noise floor as the high-frequency PSRR approaches 0 dB. The noise rises slightly to 10.8 μV rms. As the headroom falls to 150 mV, rectification harmonics start to affect the output noise, which rises to 12 μV rms. A moderate peak appears at about 250 kHz, so sensitive circuitry may be adversely affected even though the increase in total noise is modest. As the headroom voltage drops further, performance becomes compromised, and spurs related to rectification become visible in the noise spectrum. Figure 5 shows the output with 100-mV headroom. The noise has risen to 12.5 μV rms. The harmonics contain very little energy, so the noise with spurs is only slightly higher at 12.7 μV rms.
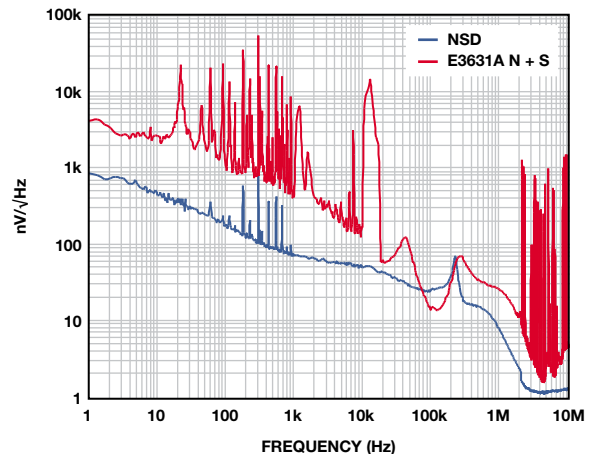


Figure 5. ADM7160 noise spectral density with 100 mV headroom.

With 75-mV headroom, the output noise becomes severely compromised, and rectification harmonics appear throughout the spectrum. The rms noise rises to 18 μV rms and the noise plus spurs rises to 27 μV rms. The noise beyond ~200 kHz is attenuated because the LDO loop has no gain and acts as a passive RC filter. With 65-mV headroom, the ADM7160 is operating in dropout. As shown in Figure 6, the output voltage noise of the ADM7160 is essentially the same as the input noise. The rms noise is now 53 μV rms and the noise plus spurs is 109 μV rms. The noise beyond ~100 kHz is attenuated because the LDO is acting as a passive RC filter.
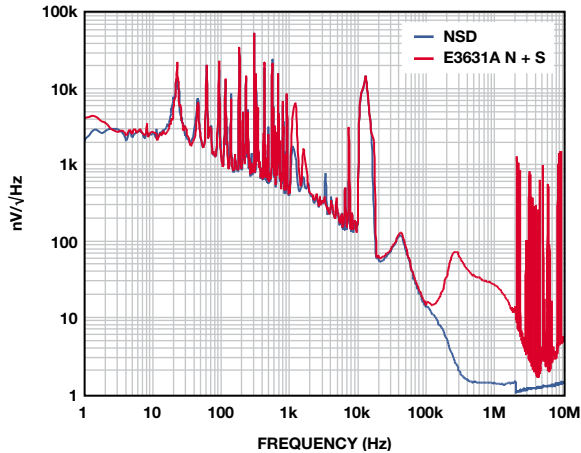


*Figure 6. ADM7160 noise spectral density in dropout.*

## Ultralow–Noise LDOs with High PSRR

A new class of LDOs such as the ADM7150 ultralow-noise, high-PSRR regulator essentially cascade two LDOs, so the resulting PSRR is approximately the sum of that of the individual stages. These LDOs require somewhat higher headroom voltages but are able to achieve PSRRs exceeding 60 dB at 1 MHz and well over 100 dB at lower frequencies.

Figure 7 shows the noise spectral density of a 5-V ADM7150 with 500-mA load current and 800-mV headroom. The output noise is 2.2 μV rms from 10 Hz to100 kHz. As the headroom drops to 600 mV, the rectification harmonics start to become apparent, but the effect on the noise is small as the output noise rises to 2.3 μV rms.
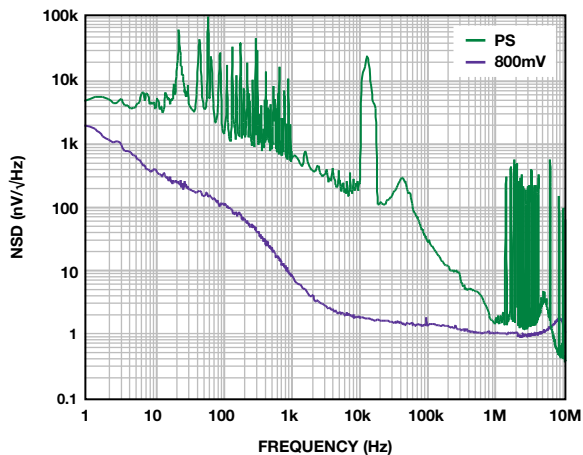


*Figure 7. ADM7150 noise spectral density with 800–mV headroom.*

With 500-mV headroom, rectification harmonics and a peak at 12 kHz are clearly visible, as shown in Figure 8. The output voltage noise rises to 3.9 μV rms.
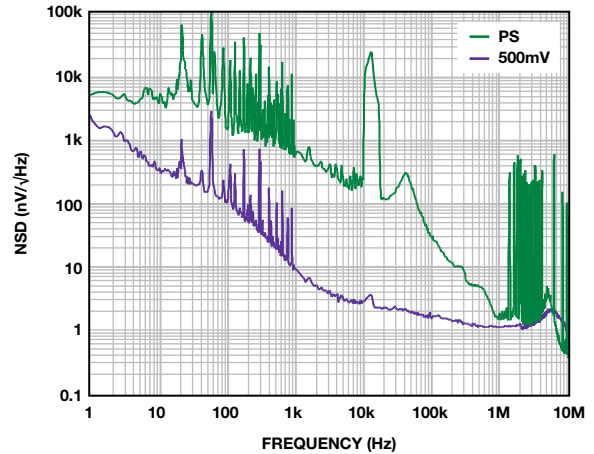


*Figure 8. ADM7150 noise spectral density with 500–mV headroom.*

With 350-mV headroom, the LDO is in dropout. No longer able to regulate the output voltage, the LDO acts like a resistor, and the output noise has risen to nearly 76 μV rms, as shown in Figure 9. The input noise is only attenuated by the pole formed by the $RDS_{ON}$ of the FET and the capacitance at the output.
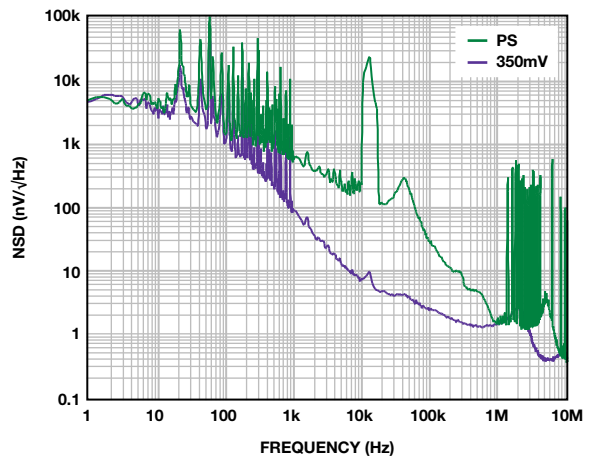


*Figure 9. ADM7150 noise spectral density in dropout.*

## Conclusion

Modern LDOs are increasingly being used to clean up dirty power-supply rails, which are often implemented with switching regulators that generate noise over a broad spectrum. The switching regulators create these voltage rails at high efficiency, but the dissipative LDOs reduce both noise and efficiency. Therefore, LDOs should be operated with as little headroom voltage as possible.

As shown, their PSRR is a function of both load current and headroom voltage, decreasing as the load current increases or the headroom voltage decreases due to the reduced loop gain as the operating point of the pass transistor moves from the saturation region to the triode region.

Considering the input source noise characteristics, PSRR, and worst-case tolerances allows designers to optimize both the power dissipation and output noise to achieve an efficient, low-noise power supply for sensitive analog circuits.

When operating at very low headroom voltages, the worst-case tolerance of the input and output voltages can affect the PSRR. Designing for worst-case tolerances will ensure a robust design; failure to do so will yield a power solution with lower PSRR resulting in higher than expected total noise.

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# Minimum Load Current Operation—Zero–Load Operation

## By Luca Vassalli

As an applications engineer, I am frequently asked about operating regulators with no load. Most modern LDOs and switching regulators are stable with no load, so why do people repeatedly ask? Some older power devices require a minimum load to guarantee stability, as one of the poles that must be compensated is affected by the effective load resistance, as discussed in "Low-Dropout Regulators (Ask the Applications Engineer—37)." For example, Figure A shows that the LM1117 requires a 1.7-mA minimum load current (up to 5 mA).

### LM1117-N ELECTRICAL CHARACTERISTICS (continued)

Typicals and limits appearing in normal type apply for $T_J$ = 25°C. Limits appearing in **Boldface** type apply over the entire junction temperature range for operation, 0°C to 125°C.

| Symbol | Parameter | Conditions | Min[1] | Typ[2] | Max[1] | Units |
|---|---|---|---|---|---|---|
| $I_{LIMIT}$ | Current Limit | $V_{IN} - V_{OUT}$ = 5V, $T_J$ = 25°C | 800 | 1200 | 1500 | mA |
| | Minimum Load Current[5] | LM1117-N-ADJ $V_{IN}$ = 15V | | 1.7 | **5** | mA |

*Figure A. LM1117 minimum load current specifications.*

Most newer devices are designed to operate with no load, and exceptions to this rule are very limited. The same design techniques that allow LDOs to be stable with any output capacitor, especially low ESR caps, are used to guarantee stability at no load. For those few modern devices that require a load, the limitation is usually a result of leakage current through the pass element, not the stability. So, how can you tell? Read the data sheet. If the device requires a minimum load, the data sheet would surely say something.

The ADP1740 and other low-voltage, high-current LDOs fall into this category. The worst-case leakage current from the integrated power switch is about 100 µA at 85°C and 500 µA at 125°C. Without a load, the leakage current would charge the output capacitor until the switch VDS was low enough to reduce the leakage current to a negligible level, raising the no-load output voltage. The data sheet says that a 500 µA minimum load is required, so a dummy load is advisable if the device will operate at high temperature. This load is small compared to the device's 2-A rating. Figure B shows the minimum load current specification from the ADP1740 data sheet.

### ADP1740/ADP1741     Data Sheet

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SENSE INPUT BIAS CURRENT (ADP1740) | $SNS_{I-BIAS}$ | 1.6 V ≤ $V_{IN}$ ≤ 3.6 V | | 10 | | µA |
| OUTPUT NOISE | $OUT_{NOISE}$ | 10 Hz to 100 kHz, $V_{OUT}$ = 0.75 V | | 23 | | µV rms |
| | | 10 Hz to 100 kHz, $V_{OUT}$ = 2.5 V | | 65 | | µV rms |
| POWER SUPPLY REJECTION RATIO | PSRR | $V_{IN}$ = $V_{OUT}$ + 1 V, $I_{OUT}$ = 10 mA | | | | |
| | | 1 kHz, $V_{OUT}$ = 0.75 V | | 65 | | dB |
| | | 1 kHz, $V_{OUT}$ = 2.5 V | | 56 | | dB |
| | | 10 kHz, $V_{OUT}$ = 0.75 V | | 65 | | dB |
| | | 10 kHz, $V_{OUT}$ = 2.5 V | | 56 | | dB |
| | | 100 kHz, $V_{OUT}$ = 0.75 V | | 54 | | dB |
| | | 100 kHz, $V_{OUT}$ = 2.5 V | | 51 | | dB |

[1] Minimum output load current is 500 µA.
[2] Accuracy when $V_{OUT}$ is connected directly to ADJ. When $V_{OUT}$ voltage is set by external feedback resistors, absolute accuracy in adjust mode depends on the tolerances of the resistors used.
[3] Based on an endpoint calculation using 10-mA and 2-A loads. See Figure 6 for typical load regulation performance.
[4] Dropout voltage is defined as the input to output voltage differential when the input voltage is set to the nominal output voltage. This applies only to output voltages above 1.6 V.
[5] Start-up time is defined as the time between the rising edge of EN to $V_{OUT}$ being at 95% of its nominal value.
[6] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 1.0-V output voltage is defined as the current that causes the output voltage to drop to 90% of 1.0 V, or 0.9 V.

*Figure B. ADP1740 minimum load current specification.*

What if the data sheet doesn't explicitly specify a minimum load? In most cases, a minimum load is not required. It may not sound very convincing, but if a minimum load was required, the data sheet would certainly say so. The confusion often comes into play because data sheets will often include graphs showing the specifications over some operating range. Most of these graphs are logarithmic, allowing them to show multiple decades of load ranges, but a log scale cannot go to zero. Figure C shows the ADM7160 output voltage and ground current vs. load current over the 10-µA-to-200-mA range. Other graphs, such as ground current vs. input voltage, show measurements at multiple load currents, but don't show data at zero current. In addition, parameters such as PSRR, line regulation, load regulation, and noise specify a certain load current range that does not include zero, as shown in Figure D. None of this means that a minimum load is required, though.
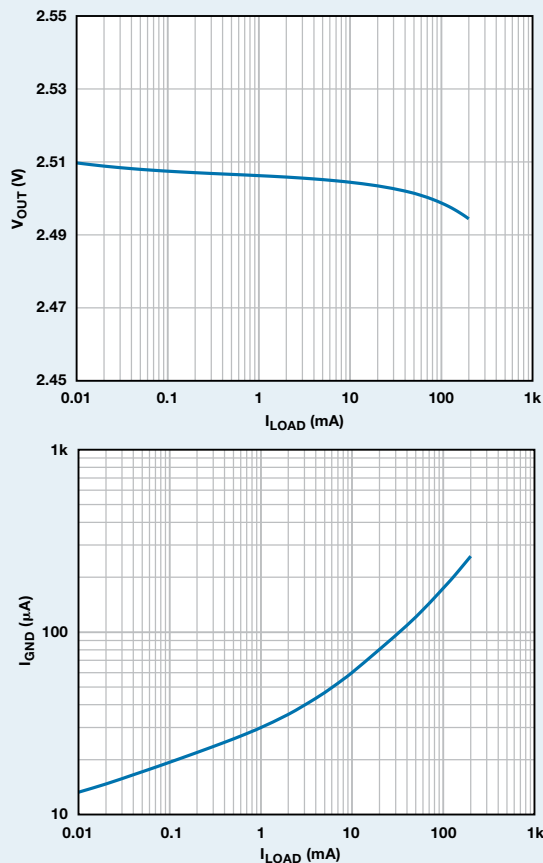


*Figure C. ADM7160 output voltage and ground current vs. load current.*

| LOAD REGULATION | $\Delta V_{OUT}/\Delta I_{LOAD}$ | | | |
|---|---|---|---|---|
| $V_{OUT} < 1.8\,V$ | $I_{LOAD}$ = 100 µA to 200 mA | 0.006 | | %/mA |
| | $I_{LOAD}$ = 100 µA to 200 mA, $T_J$ = −40°C to +125°C | | 0.012 | %/mA |
| $V_{OUT} \geq 1.8\,V$ | $I_{LOAD}$ = 100 µA to 200 mA | 0.003 | | %/mA |
| | $I_{LOAD}$ = 100 µA to 200 mA, $T_J$ = −40°C to +125°C | | 0.008 | %/mA |

*Figure D. ADM7160 load regulation.*

Users of switching regulators with power-saving mode (PSM) are often worried about operation at light loads because PSM reduces the operating frequency, skips pulses, provides a burst of pulses, or some combination of these. PSM reduces power consumption and increases efficiency at light loads. Its disadvantage is a noticeable increase in output ripple, but the device remains stable and can easily operate with no load.

As shown in Figure E, the ADP2370 high-voltage, low-quiescent-current buck regulator produces increased ripple due to PSM operation when the load switches between 800 mA and 1 mA. The fact that the test was done at 1 mA does not indicate that 1 mA is the minimum load.
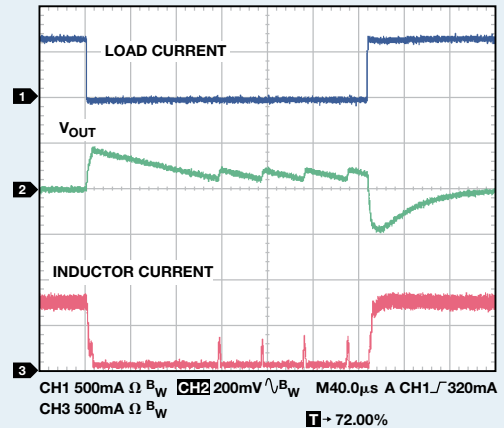


*Figure E. ADP2370 load transient in power–saving mode.*

Figure F shows the ripple voltage changing with load current. In this case the graph goes all the way to zero, indicating both that the load can be zero and that the noise at no load may not be any worse than the noise at 1 mA or 10 mA.
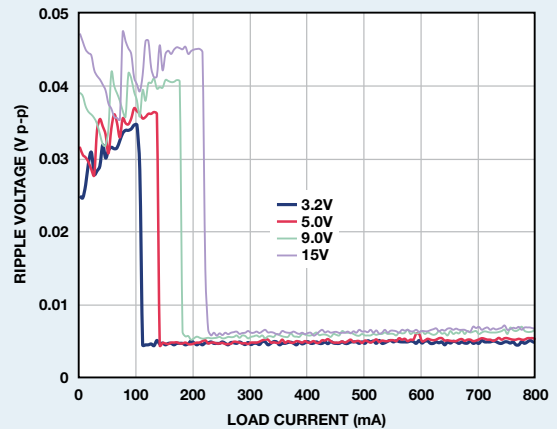


*Figure F. ADP2370 output ripple vs. load current.*

## Conclusion

Most modern regulators are stable with zero load current, but when in doubt, consult the data sheet. Be careful, though. Logarithmic graphs don't go to zero, and tests aren't always done with zero load current, so you shouldn't infer that the regulator won't work with no load even though no-load data isn't shown. With switching regulators, ripple in power-saving mode is normal, not a sign of instability.

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Caveat Emptor

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Also by this Author:

Noise-Reduction Network for Adjustable-Output Low-Dropout Regulators

Volume 48, Number 1

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### Luca Vassalli

# Configure Controller Area Network (CAN) Bit Timing to Optimize Performance

By Dr. Conal Watterson

## Introduction

Controller area network (CAN) offers robust communication between multiple network locations, supporting a variety of data rates and distances. Featuring data-link layer arbitration, synchronization, and error handling, CAN is widely used in industrial, instrumentation, and automotive applications. Standardized under ISO 11898, with distributed multimaster differential signaling and built-in fault handling, various protocols such as DeviceNet and CANopen define implementations for physical and data-link layers. This article describes how to optimize settings for a given application, considering hardware restrictions such as controller architecture, clocks, transceivers, and logic-interface isolation. It addresses network configuration—both data rate and cable length—explaining when reconfiguration of CAN nodes is necessary and how nodes can be optimally configured from the beginning.

## Isolating the Logic Interface

For harsh industrial and automotive environments, system robustness can be further enhanced by isolating the logic interface to the CAN transceiver, allowing large potential differences between ground nodes and providing immunity to high-voltage transients. An isolated CAN node can be formed by integrating a CAN transceiver with digital isolators. The ADM3052, ADM3053, and ADM3054 isolated CAN transceivers provide various options for powering the interface. For DeviceNet networks, the isolated side can be powered from the bus, so the ADM3052 integrates a linear regulator to provide a 5-V supply from the 24-V bus supply. The ADM3053, shown in Figure 1, integrates an *iso*Power dc-to-dc convertor to power the transceiver and bus side of the digital isolator. Systems that already have an isolated dc-to-dc convertor to provide power across the barrier can use the ADM3054, which integrates only the digital isolator and CAN transceiver.
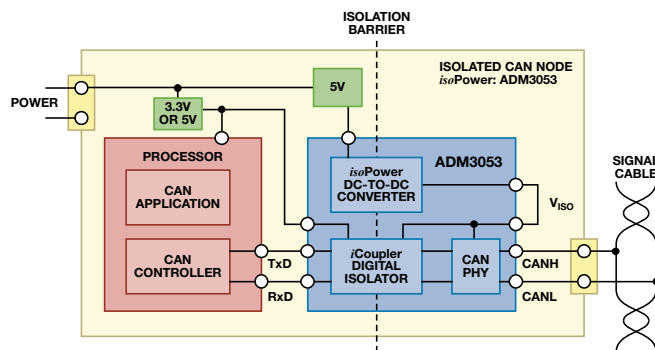


*Figure 1. Isolated CAN node with ADM3053 transceiver powered by isoPower dc–to–dc.*

## Effect of Propagation Delay

Implementing a CAN node requires an isolated or nonisolated CAN transceiver and a CAN controller or processor with the appropriate protocol stack. Standalone CAN controllers can be used, even without a standard protocol stack, but microprocessors used in CAN applications may already include the CAN controller. In either case, the CAN controller must be configured to reconcile the data rate and timing on the bus with the hardware oscillator used for the controller.

As cable length increases, the high frequency content of the signal is attenuated, so data rates are limited for long distances. The bus is a multimaster, so all nodes can attempt transmission at the same time, and arbitration depends on the physical layer signaling. Propagation delay, which also increases with cable length, can interfere with the synchronization and arbitration between nodes.

The differential signal on a CAN bus can be one of two states: dominant (Logic 0, a differential voltage between signal lines CANH and CANL) or recessive (Logic 1, no differential voltage, all CAN transceiver outputs are high impedance). If two nodes attempt to transmit at the same time, a dominant bit transmission will overwrite a concurrent recessive bit transmission, so all nodes must monitor the bus state while transmitting and cease transmission if overwriting occurs when they transmit a recessive bit. Thus, the node transmitting the dominant bit wins arbitration, as shown in Figure 2.

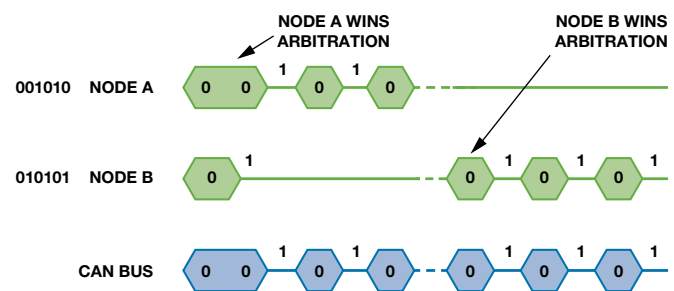

*Figure 2. Arbitration logic between two CAN nodes.*

CAN 2.0b, which defines the implementation of the data-link layer, specifies the structure of CAN frames used for transmission. An arbitration field, which includes a message ID, starts the message. A lower message ID (more initial zeroes) will have higher priority, so the node is more likely to win arbitration when transmitting a message.

Although CAN nodes synchronize to the bus transmissions, two nodes that transmit together will not be exactly concurrent due to the propagation delay between them. For arbitration to work, the propagation delay must not be too large, or the faster node may sample the bus before detecting the bit state transmitted by the slower node. The worst-case propagation delay is twice the delay between the two furthest nodes. If nodes A and B in Figure 3 are the furthest apart on the bus, the critical parameter is the round trip time of $T_{PropBA}$ plus $T_{PropBA}$.
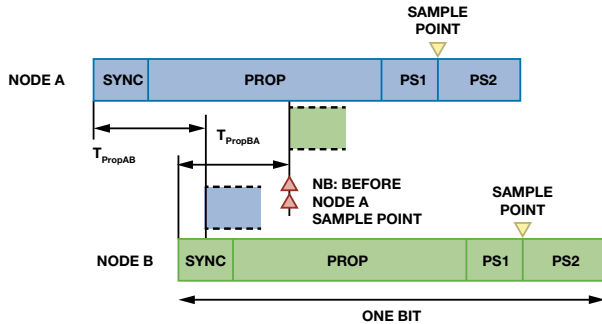


**Figure 3.** *Arbitration between two CAN nodes in practice, with propagation delay.*

The total propagation delay comprises the round trip time through the cable, two CAN controllers I/O, and two CAN transceivers. The CAN controller I/O is not a major contributor, and can often be ignored, but a thorough assessment will allow for it. Loop time comprises the propagation delay from TxD to CANH/CANL and back to RxD. The cable propagation delay depends on the cable and distance, with 5 ns/m being a typical value.

At lower data rates, the allowed bit time is longer, so the propagation delay (and thus the cable distance) can also be longer. At the maximum standard CAN data rate of 1 Mbps, the allowed propagation delay is more limited, though ISO 11898-2 specifies a bus length of 40 meters for operation at 1 Mbps.

## Impact of Isolation

With isolation, an extra element must be considered in the round trip propagation delay calculation. Digital isolators reduce the propagation delay compared to optocouplers, but even the fastest isolated CAN transceivers will be comparable to the slower nonisolated transceivers. If the total allowable propagation delay remains the same, the maximum cable length will be shorter in isolated systems, but it may be possible to reconfigure the CAN controller to increase the total allowed propagation delay.

## Compensating for Propagation Delay

To compensate for propagation delays added by longer buses or isolation, specific parameters related to timing and synchronization must be set up for the CAN controller. When configuring the controller, instead of simply selecting a data rate, set the variables that dictate the bit time used by the controller. The baud rate prescaler (BRP) for the oscillator or internal clock sets the time quantum (TQ), and the bit time is a multiple of TQ. The hardware selection of the oscillator, and the software configuration of the BRP and number of TQ per bit time set the data rate.

The controller's bit time is broken into three or four segments as shown in Figure 3. The total number of TQ per bit time includes one for synchronization, plus programmed numbers for propagation delay (PROP), Phase Segment 1 (PS1), and

Phase Segment 2 (PS2). Sometimes PROP and PS1 are combined. Configuration adjusts the sample point to allow for propagation delay and resynchronization.

Setting the sample point later in the bit time allows for longer propagation delays, but like the overall data rate, the sample point is dependent on other timing variables, each of which has its own restrictions. For example, the internal clock/oscillator may be fixed and only integer BRP and TQ numbers can be used. Thus, the ideal data rate required for a certain cable length may be impossible to achieve, so either the cable must be shortened or the data rate must be reduced.

Resynchronization results in PS1 being lengthened or PS2 being shortened by the number of TQ specified by the synchronization jump width (SJW), so PS2 can never be shorter than SJW. The number of TQ required for SJW depends on the clock tolerance of CAN controllers, with crystal oscillators typically allowing the minimum TQ for SJW and PS2.

## Configuring a CAN Controller

To achieve a robust network with reliable timing and synchronization between nodes, the system must be able to tolerate the propagation delay with the chosen data rate and CAN-controller clock. If it this is not possible, the options are to reduce the data rate, shorten the bus, or use a different CAN-controller-clock rate. A three-step configuration process follows.

## Step 1: Check Clock and Prescaler—Match Data Rate

First check the possible configurations given the desired data rate and the CAN-controller clock. The TQ interval must be calculated based on the clock and various BRP values, and only the combinations where the TQ interval divides into the bit time by an integer number are possible. Depending on the system design stage, it may be possible to consider other CAN-controller-clock rates as well. Table 1 shows example calculations given a 1-Mbps maximum data rate using a Microchip® MCP2515 standalone CAN controller and an ADSP-BF548 Blackfin processor with built-in CAN controller. The MCP2515 $f_{OSC}$ depends on the external-hardware oscillator used, while the ADSP-BF548 $f_{SCLK}$ is determined by the hardware CLKIN and internal PLL settings (CLKIN multiplier for VCO, VCO divide-down for SCLK). Only certain combinations of CAN-controller clock and BRP (an integer number of TQ) will allow a 1-Mbps data rate, as shown in bold. This limits the settings for the bit timing, as only certain options are available once a bus data rate has been chosen.

**Table 1. Number of TQ for 1–Mbps Operation Given *f* and BRP**

| MCP2515: #TQ for 1-Mbps Operation | | | | |
|---|---|---|---|---|
| $f_{OSC}$ | BRP = 1 | BRP = 2 | BRP = 3 | BRP = 4 |
| **40** | **20** | **10** | *6.667* | **5** |
| **38** | **19** | *9.5* | *6.333* | *4.75* |
| **30** | **15** | *7.5* | **5** | *3.75* |
| **20** | **10** | **5** | *3.333* | *2.5* |
| **10** | **5** | *2.5* | *1.667* | *1.25* |

| ADSP-BF548: #TQ for 1-Mbps Operation | | | | |
|---|---|---|---|---|
| $f_{SCLK}$ | BRP = 5 | BRP = 6 | BRP = 7 | BRP = 8 |
| **133** | *26.6* | *22.167* | **19** | *16.625* |
| **100** | **20** | *16.667* | *14.286* | *12.5* |
| **50** | **10** | *8.3333* | *7.143* | *6.25* |
| **40** | **8** | *6.667* | *5.714* | **5** |

## Step 2: Determine Bit Segment Configuration

The next step is to determine the number of TQ required for each bit segment. The most difficult case is supporting the maximum propagation delay at a 1-Mbps data rate, with a 40-m cable and isolated nodes, for example. Ideally, the bit time segments should be configured so that the sample point is as late as possible in the bit. For each integer total number of TQ in Table 1, one TQ must be allowed for the SYNC segment, and the PS2 (or TSEG2) segment must be large to accommodate the CAN-controller-information processing time (2 TQ for MCP2515, <1 TQ for ADSP-BF548 as long as BRP > 4). Also, for the MCP2515, PROP and PS1 can be 8 TQ maximum each; for the ADSP-BF548, TSEG1 (PROP + PS1) can be 16 TQ maximum.

Figure 4 and Figure 5 show the possible total TQ configurations for MCP2515 and ADSP-BF548 respectively, with the latest sample point possible for the valid combinations of clock and BRP for 1-Mbps operation. The optimum total TQ for the MCP2515 is 19, requiring a hardware oscillator of 38 MHz and BRP of 1. For the ADSP-BF548, all the configurations except for a total of 5 TQ are at least 85% sample point, but the optimum setting is 10 TQ, requiring $f_{SCLK}$ = 50 MHz with BRP = 5.
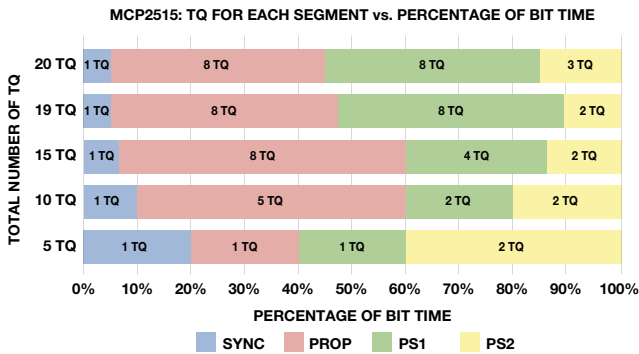
**MCP2515: TQ FOR EACH SEGMENT vs. PERCENTAGE OF BIT TIME**



*Figure 4. Possible total TQ configurations for MCP2515, 1–Mbps maximum propagation delay.*

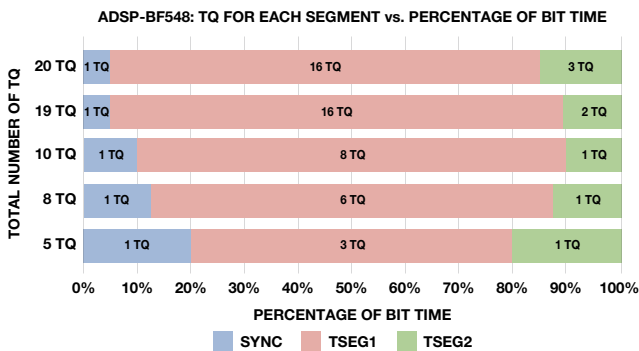**ADSP-BF548: TQ FOR EACH SEGMENT vs. PERCENTAGE OF BIT TIME**



*Figure 5. Possible total TQ configurations for ADSP–BF548, 1–Mbps maximum propagation delay.*

## Step 3: Match Transceiver/Isolation Delay and Bus Length to Configuration

Having achieved the optimum sample point for the CAN controller, the last step is to compare the allowable propagation delay with the CAN transceiver/isolation and bus length used. Assuming the ADSP-BF548 optimum configuration of 10 TQ ($f_{SCLK}$ = 50 MHz, BRP = 5), the maximum propagation delay possible is 900 ns. For the ADM3053 isolated CAN transceiver with integrated isolated power, the data-sheet maximum loop delay (TxD off to receiver inactive) is 250 ns. This must be doubled (500 ns) to include both transmit and receive delays at two nodes at the furthest ends of the bus.

Assuming a 5-ns/m cable propagation delay, a bus length of 40 meters (maximum for 1 Mbps per ISO 11898) could be accommodated with the ADSP-BF548 having a total of 10 TQ in bit time with only 1 TQ for the TSEG2 bit segment. In practice, slightly earlier sample points may suffice, as even an extreme transceiver propagation delay on one node would likely result in a simple retransmission (handled automatically by the CAN controller at the data-link layer), but the small delay between the CAN-controller I/O and the CAN transceiver makes it advisable to configure the sample point to the latest point possible.

### Conclusion

Isolation adds robustness, but it will also add a propagation delay, in both transmit and receive directions. This delay must be doubled to account for two nodes in arbitration. If the allowed propagation delay in the system is fixed, then the cable length or data rate may be decreased if isolation is added. An alternative is to reconfigure CAN controllers to allow the maximum possible propagation delay to ensure that the desired data rate and bus length are possible, even with isolated nodes.

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