Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing • Volume 48, Number 4, 2014

Analog Dialogue Since 1967

analog.com/analogdialogue

ANALOG DEVICES

Editor's Notes

IN THIS ISSUE

RF-to-Bits Solution Offers Precise Phase and Magnitude Data for Material Analysis

When analyzing materials in remote locations, placing probes within the material may not be viable. A high-frequency transceiver can provide a practical method for accurately quantifying the material's volume fractions without the adverse effects of direct exposure to the material. Quadrature demodulators offer a novel, robust way to measure magnitude and phase shift. (Page 3)

Synchronous Detectors Facilitate Precision, Low-Level Measurements

Synchronous detectors can extract small signals, buried in the noise, to measure properties such as very small resistance, light absorption or reflection against bright backgrounds, or strain accompanied by high noise levels. The noise often increases as the frequency nears zero. Moving the measurement away from the low-frequency noise increases the SNR, allowing weaker signals to be detected. (Page 8)

Wearable Electronic Devices Monitor Vital Signs, Activity Level, and More

Wearable devices for vital-sign monitoring are transforming the healthcare industry, allowing us to monitor our vital signs and activity anytime, anywhere. To be effective, wearable devices must be small, low cost, and low power. This two-part article describes some low-power products for wearable and personal health applications, in this fast growing, exciting, rapidly changing market. (Page 13)

Two New Devices Help Reinvent the Signal Generator

In the past, the most difficult part of an arbitrary waveform generator was designing the output stage. Typical signal generators offer output ranges from 25 mV to 5 V. To drive a 50-Ω load, traditional designs used high-performance discrete devices, a large number of integrated devices in parallel, or an expensive ASIC. Now, amplifiers can drive these loads, reducing output stage complexity. (Page 19)

ADC Modeling Tools Speed Up Evaluation

System designers are faced with a common dilemma: design a new product on a known platform, making only minor changes; or use a brand-new platform with the most advanced products and capabilities. A new suite of simulation tools now enables quick prototyping in software, minimizing development risk, providing confidence that products will work as expected, and delaying hardware decisions to save time and money. (Page 23)

Understand Low-Dropout Regulator (LDO) Concepts to Achieve Optimal Designs

This brief tutorial introduces some common terms used with LDOs, explaining fundamental concepts such as drop-out voltage, headroom voltage, quiescent current, ground current, shutdown current, efficiency, dc line-and-load regulation, transient line-and-load response, power-supply rejection ratio (PSRR), output noise, and accuracy, using examples and plots. (Page 27)

Scott Wayne [scott.wayne@analog.com]

Product Introductions: Volume 48, Number 4

Data sheets for all ADI products can be found by entering the part number in the search box at analog.com.

October

ADC/DAC, 8-channel, 12-bit, on-chip reference **AD5592R/AD5593R**
Power Monitor, digital, PMBus interface **ADM1293/ADM1294**
Switches, quad SPST, bipolar fault protection **ADG5412BF/ADG5413BF**
Switches, quad SPST, fault protection **ADG5412F/ADG5413F**

November

ADC, PulSAR, 16-bit, 600-kSPS, high-temperature **AD7981**
Amplifier, operational, dual, EMI/OV protection **ADA4177-2**
Amplifier, operational, dual, low-drift, 105-MHz **ADA4805-2**
Clock Generator, Ethernet/Gigabit Ethernet **AD9574**
Comparator, single, accurate reference voltage **ADCMP394**
DACs, dual, 11-/16-bit, 2.8-GSPS, TxDAC+® **AD9134/AD9136**
Demodulator, synchronous, analog filter **ADA2200**
Isolator, digital, 6-channel, SPI, 5-kV isolation **ADuM4150**
Isolator, digital, 7-channel, SPI, multiple slave, 5-kV **ADuM4154**
Isolators, digital, 7-channel, SPI, 3.75-kV isolation **ADuM4151/ADuM4152/ADuM4153**
Modulator, quadrature, fractional-N PLL, four VCOs **ADRF6720-27**
Modulator, Σ-Δ, 16-bit, isolated, LVDS **AD7405**
Regulator, boost, ultralow-power, MPPT **ADP5090**
Regulator, linear, ultralow-noise, 600-mA **ADM7154**
Regulators, low-dropout, 150-mA, very low I_Q **ADP165/ADP166**
Regulators, low-dropout, 20-V, 200-mA, low-noise **ADP7112/ADP7118**
Regulators, low-dropout, 40-V, 200-mA, low-noise **ADP7142**

December

ADC, Σ-Δ, 24-bit, 31.25-kSPS, rail-to-rail **AD7172-2**
Amplifier, digital-gain, 3.2-GHz, low-distortion **ADA4961**
Clock Generator, JESD204B, 14 LVDS/HSTL outputs **AD9528**
Comparator, quad, accurate reference voltage **ADCMP395**
DACs, *nano*DAC+, octal, 12-/16-bit, reference, I²C **AD5671R/AD5675R**
DACs, *nano*DAC+, octal, 12-/16-bit, reference, SPI **AD5672R/AD5676R**
DAC, *nano*DAC+, octal, 16-bit, SPI **AD5676**
Gyroscope, dual-axis, ultralow-noise **ADXRS290**
Receiver, wideband IF **AD6676**
Regulators, step-down, 5-A/6-A, high-efficiency **ADP2165/ADP2166**
Regulator, synchronous buck, dual, 2-MHz, 800-mA **ADP2230**
Sensor, angle, AMR, signal conditioning **ADA4571**
Synthesizer, phase-locked loop, dual, precision **AD9578**
Synthesizer, ultra-wideband, 13.6-GHz, low-noise VCO **ADF5355**
Synthesizer, wideband, 4.4-GHz, low-noise VCO **ADF4355-2**

Analog Dialogue

Analog Dialogue, www.analog.com/analogdialogue, the technical magazine of Analog Devices, discusses products, applications, technology, and techniques for analog, digital, and mixed-signal processing. Published continuously for 48 years—starting in 1967—it is available in two versions. Monthly editions offer technical articles; timely information including recent application notes, circuit notes, new-product briefs, webinars, and published articles; and a universe of links to important and relevant information on the Analog Devices website, www.analog.com. Printable quarterly issues and ebook versions feature collections of monthly articles. For history buffs, the *Analog Dialogue* archive, www.analog.com/library/analogdialogue/archives.html, includes all regular editions, starting with Volume 1, Number 1 (1967), and three special anniversary issues. To subscribe, please go to www.analog.com/library/analogdialogue/subscribe.html. Your comments are always welcome: Facebook: www.facebook.com/analogdialogue; EngineerZone: ez.analog.com/blogs/analogdialogue; Email: dialogue.editor@analog.com or *Scott Wayne*, Editor [scott.wayne@analog.com].

RF-to-Bits Solution Offers Precise Phase and Magnitude Data for Material Analysis

By Ryan Curran, Qui Luu, and Maithil Pachchigar

Introduction

When analyzing materials in remote locations, where placing probes within the material is not viable, a high-frequency transceiver can provide a practical method for accurately quantifying the material's volume fractions without the adverse effects of direct exposure to the material. Quadrature demodulators offer a novel, robust way to measure magnitude and phase shift in these applications. The receiver signal chain presented here uses the ADL5380 broadband quadrature demodulator, the ADA4940-2 ultralow power, low distortion, fully differential ADC driver, and the AD7903 dual, differential, 16-bit, 1-MSPS PulSAR® ADC to provide accurate data while ensuring safe, economical operation.

In the receiver shown in Figure 1, a continuous wave signal is sent from the transmit (Tx) antenna, through the material to be analyzed, to the receive (Rx) antenna. The received signal will be attenuated and phase shifted relative to the original transmitted signal. This amplitude change and phase shift can be used to determine the content of media.

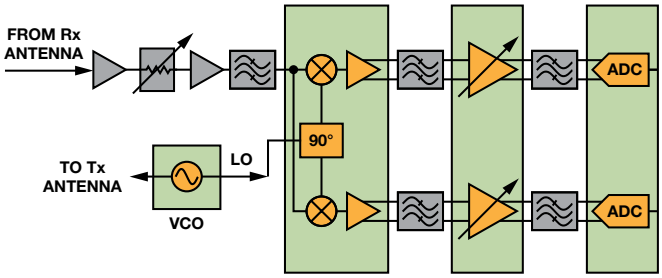


Figure 1. Receiver block diagram.

Magnitude and phase shifts can be directly correlated to the transmittance and reflectance properties of an element, as shown in Figure 2. In the case of oil-gas-water flow, for example, the permittivity, loss, and dispersion is high for water, low for oil, and extremely low for gas.

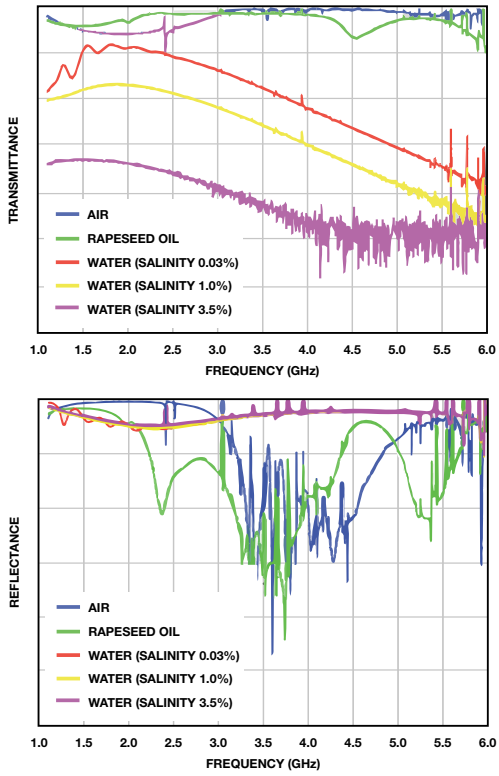


Figure 2. Transmittance and reflectance for different homogeneous media.

Receiver Subsystem Implementation

The receiver subsystem shown in Figure 3 converts an RF signal to digital to accurately measure magnitude and phase. The signal chain comprises a quadrature demodulator, a dual differential amplifier, and a dual, differential SAR ADC. The key goals of this design are high-precision phase and magnitude measurements with wide dynamic range for high-frequency RF inputs.

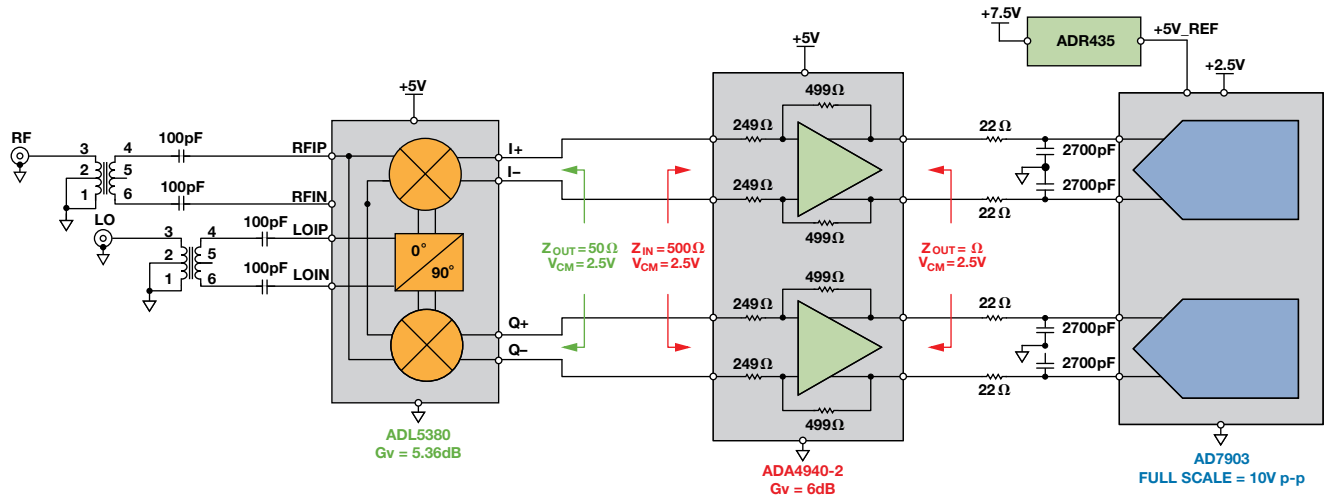
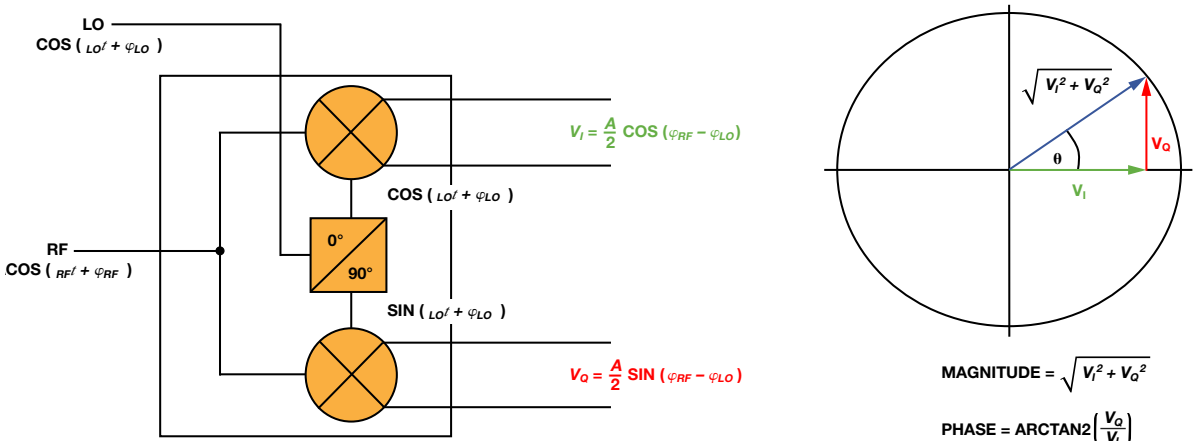


Figure 3. Simplified receiver subsystem for material analysis.

Quadrature Demodulator

A quadrature demodulator provides an in-phase (I) signal and a quadrature (Q) signal that is exactly 90° out of phase. The I and Q signals are vector quantities, so the amplitude and phase shift of the received signal can be calculated using trigonometric identities, as shown in Figure 4. The local-oscillator (LO) input is the original transmitted signal and the RF input is the received signal. The demodulator generates a sum and difference term. Both signals are at the exact same frequency, $\omega_{LO} = \omega_{RF}$, so the high-frequency sum term will get filtered, while the difference term resides at dc. The received signal will have a different phase, ϕ_{RF}, than that of the transmitted signal, ϕ_{LO}. This phase shift, $\phi_{LO} - \phi_{RF}$, is due to the permittivity of the media and will help define the material content.



$$I = A\cos(\omega_{RF}t + \varphi_{RF}) \times \cos(\omega_{LO}t + \varphi_{LO}) = \frac{A}{2}[\cos(\omega_{RF}t - \omega_{LO}t + \varphi_{RF} - \varphi_{LO}) + \cos(\omega_{RF}t + \omega_{LO}t + \varphi_{RF} + \varphi_{LO}]$$

$$V_I = \frac{A}{2}[\cos(\varphi_{RF} - \varphi_{LO})]$$

Let $\omega_{RF} = \omega_{LO}$ difference term at dc; Sum term gets filtered

(1)

$$Q = A\cos(\omega_{RF}t + \varphi_{RF}) \times \sin(\omega_{LO}t + \varphi_{LO}) = \frac{A}{2}[\sin(\omega_{RF}t - \omega_{LO}t + \varphi_{RF} - \varphi_{LO}) + \sin(\omega_{RF}t + \omega_{LO}t + \varphi_{RF} + \varphi_{LO}]$$

$$V_Q = \frac{A}{2}[\cos(\varphi_{RF} - \varphi_{LO})]$$

Let $\omega_{RF} = \omega_{LO}$ difference term at dc; Sum term gets filtered

(2)

Figure 4. *Magnitude and phase measurement using a quadrature demodulator.*

A real-world I/Q demodulator has many imperfections, including quadrature phase error, gain imbalance, and LO-to-RF leakage, all of which could degrade the quality of the demodulated signal. To select a demodulator, first determine the requirements for RF input frequency range, amplitude accuracy, and phase accuracy.

Powered from a single 5-V supply, the ADL5380 accepts RF or IF input frequencies from 400 MHz to 6 GHz, making it ideal for the receiver signal chain. Configured to provide a 5.36-dB voltage conversion gain, its differential I and Q outputs can drive a 2.5-V p-p differential signal into a 500-Ω load. Its 10.9-dB NF, 11.6-dBm IP1dB, and 29.7-dBm IIP3 @ 900 MHz provide outstanding dynamic range, while its 0.07-dB amplitude balance and 0.2° phase balance achieve excellent demodulation accuracy. Manufactured using an advanced SiGe bipolar process, it is available in a tiny 4-mm × 4-mm, 24-lead LFCSP package.

ADC Driver and High Resolution Precision ADC

The ADA4940-2 fully differential dual amplifier's excellent dynamic performance and adjustable output common mode make it ideal for driving high-resolution, dual SAR ADCs. Powered from a single 5-V supply, it provides ±5-V differential outputs with a 2.5-V common mode. Configured to provide a gain of 2 (6 dB), it drives the ADC inputs to full scale. The RC filter (22 Ω/2.7 nF) helps to limit the noise and reduces the kickback coming from the capacitive DAC at the ADC input. Manufactured using a proprietary SiGe complementary bipolar process, it is available in a tiny 4-mm × 4-mm, 24-lead LFCSP package.

The AD7903 dual, 16-bit, 1-MSPS successive-approximation ADC offers excellent precision, with ±0.006% FS gain error and ±0.015-mV offset error. Operating from a single 2.5-V power supply, it dissipates only 12 mW at 1 MSPS. The main goal of using a high-resolution ADC is to achieve ±1° phase accuracy, especially when the input signal has a small dc magnitude. The 5-V reference required by the ADC is generated by the ADR435 low-noise reference.

As shown in Figure 5, the receiver subsystem is implemented using the ADL5380-EVALZ, EB-D24CP44-2Z, EVAL-AD7903SDZ, and EVAL-SDP-CB1Z evaluation kits. These circuit components are optimized for interconnection in the subsystem. Two high-frequency, phase-locked input sources provide the RF and LO input signals.

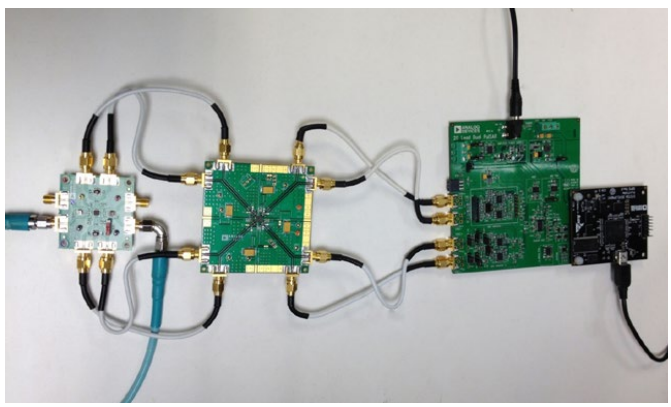


Figure 5. *Receiver subsystem evaluation platform.*

Table 1 summarizes the input and output voltage levels for each of the components in the receiver subsystem. An 11.6-dBm signal at the demodulator's RF input will produce an input within –1 dB of the ADC's full-scale range. The table assumes a 500-Ω load, 5.3573-dB conversion gain, and –4.643-dB power gain for the ADL5380, and 6-dB gain for the ADA4940-2. The calibration routine and performance results achieved for this receiver subsystem will be discussed in the following sections.

Table 1. Input and Output Voltage Levels at Each Component in the Receiver Subsystem.

RF Input (dBm)	ADL5380 Output		AD7903 Input (dBFS)
	(dBm)	(V p-p)	
+11.6	+6.957	4.455	–1.022
0	–4.643	1.172	–12.622
–20	–24.643	0.117	–32.622
–40	–44.643	0.012	–52.622
–68	–72.643	466µ	–80.622

Receiver Subsystem Error Calibration

The receiver subsystem contains three major error sources: offset, gain, and phase.

The individual differential dc magnitudes of the I and Q channels have sinusoidal relationships with respect to the relative phase of the RF and LO signals. As a result, the ideal dc magnitude of the I and Q channels can be calculated as follows:

$$Voltage\ I_{CHANNEL} = max\ I/Q\ output \times cos(\theta) \quad (3)$$

$$Voltage\ Q_{CHANNEL} = max\ I/Q\ output \times sin(\theta) \quad (4)$$

As the phase moves through the polar grid, some locations should ideally produce the same voltage. For example, the voltage on the I (cosine) channel should be identical with phase shifts of +90° or –90°. However, a constant phase-shift error, independent of the relative phase of RF and LO, will cause the subsystem channel to generate different results for input phases that should produce the same dc magnitude. This is illustrated in Figure 6 and Figure 7, where two different output codes are generated when the input should be at 0 V. In this case, the –37° phase shift is much larger than expected in a real-world system containing phase-locked loops. The result is +90° actually appearing as +53° and –90° as –127°.

Results were gathered in 10° steps from –180° to +180°, with the uncorrected data generating the elliptical shapes shown in Figure 6 and Figure 7. This error can be accounted for by determining the amount of additional phase shift present in the system. Table 2 shows that the system phase-shift error is constant throughout the transfer function.

Table 2. Summary of Receiver Subsystems Measured Phase Shift for 0-dBm RF Input Amplitude.

Input Phase RF to LO	Average I-Ch Output Code	Average Q-Ch Output Code	I-Ch Voltage	Q-Ch Voltage	Measured Phase	Measured Receiver Subsystem Phase Shift
–180°	–5851.294	+4524.038	–0.893	+0.690	+142.29°	–37.71°
–90°	–4471.731	–5842.293	–0.682	–0.891	–127.43°	–37.43°
0°	+5909.982	–4396.769	+0.902	–0.671	–36.65°	–36.65°
+90°	+4470.072	+5858.444	+0.682	+0.894	+52.66°	–37.34°
+180°	–5924.423	+4429.286	–0.904	+0.676	+143.22°	–36.78°

System Phase Error Calibration

With a step size of 10°, the average measured phase shift error was –37.32° for the system shown in Figure 5. With this additional phase shift known, the adjusted subsystem dc voltages can now be calculated. The variable ϕ_{PHASE_SHIFT} is defined as the average observed additional system phase shift. The dc voltage generated in the phase-compensated signal chain can be computed as:

$$Voltage\ I_{CHANNEL} = max\ I/Q\ output \times \left(cos(\theta_{TARGET})cos(\varphi_{PHASE\_SHIFT}) - sin(\theta_{TARGET})sin(\varphi_{PHASE\_SHIFT})\right) \quad (5)$$

$$Voltage\ Q_{CHANNEL} = max\ I/Q\ output \times \left(sin(\theta_{TARGET})cos(\varphi_{PHASE\_SHIFT}) + cos(\theta_{TARGET})sin(\varphi_{PHASE\_SHIFT})\right) \quad (6)$$

Equation 5 and Equation 6 provide the target input voltage for a given phase setting. The subsystem has now been linearized and the offset error and gain error can now be corrected. The linearized I- and Q-channel results can also be seen in Figure 6 and Figure 7. A linear regression on the data sets generates the best fit line shown in the figures. This line is the measured subsystem transfer function for each conversion signal chain.

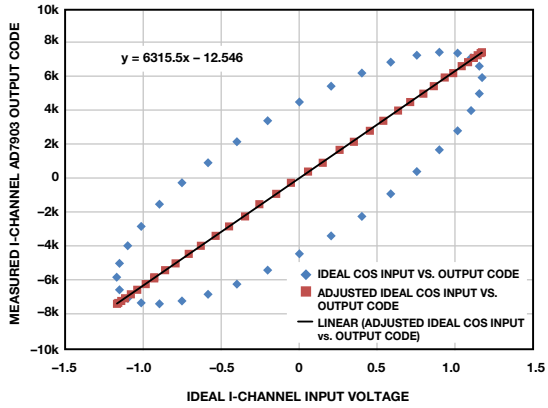


Figure 6. Linearized I-channel results.

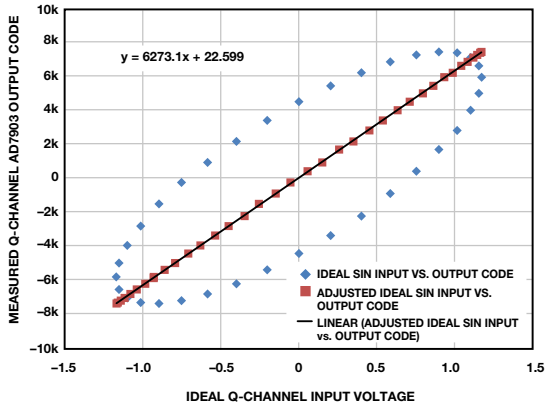


Figure 7. Linearized Q-channel results.

System Offset Error and Gain Error Calibration

The offset of each signal chain within the receiver subsystem should ideally be 0 LSB, but the measured offsets were –12.546 LSB and +22.599 LSB for I and Q channels, respectively. The slope of the best fit line represents the slope of the subsystem. The ideal subsystem slope can be calculated as:

$$Ideal\ Slope = \frac{Max\ Code - Min\ Code}{+V_{REF} - -V_{REF}} = \frac{65535 - 0}{+5 - -5} = 6553.5\ \frac{Codes}{V} \quad (7)$$

The results in Figure 6 and Figure 7 show that the measured slopes were 6315.5 and 6273.1 for the I and Q channels, respectively. These slopes must be adjusted to correct the system

gain error. Correcting for gain error and offset error ensures that the signal magnitude computed using Equation 1 matches the ideal signal magnitude. The offset correction is just the opposite of the measured offset error:

$$Offset\ Error\ Correction = -Measured\ Offset\ Error \quad (8)$$

The gain error correction coefficient is:

$$Gain\ Error\ Correction = \frac{Ideal\ Slope}{Measured\ Slope} \quad (9)$$

The received conversion result can be corrected by:

$$Corrected\ Output\ Code = \frac{Received\ Output\ Code \times Ideal\ Slope}{Measured\ Slope} + Offset\ Error\ Correction \quad (10)$$

The subsystem's calibrated dc input voltage is calculated as:

$$Measured\ Signal\ Input\ Voltage = \frac{2 \times V_{REF} \times Corrected\ Output\ Code}{2^N - 1} \quad (11)$$

Equation 11 should be used on both I and Q channels to compute the perceived analog input voltage for each subsystem signal chain. These fully adjusted I- and Q-channel voltages are used to compute the RF signal amplitude as defined by the individual dc-signal magnitudes. To evaluate the accuracy of the full calibration routine, the collected results can be converted to ideal subsystem voltages produced at the output of the demodulator as if no phase-shift error was present. This can be done by multiplying the average dc magnitude computed previously by the sinusoidal fraction of the measured phase at each trial with the computed phase shift error removed. The calculation appears as follows:

$$Fully\ Corrected\ I\text{-}Channel\ Voltage = Average\ Post\ Calibration\ Magnitude \times \left(cos(\theta_{MEASURED})cos(\varphi_{PHASE\_SHIFT}) + sin(\theta_{MEASURED})sin(\varphi_{PHASE\_SHIFT})\right) \quad (12)$$

$$Fully\ Corrected\ Q\text{-}Channel\ Voltage = Average\ Post\ Calibration\ Magnitude \times \left(sin(\theta_{MEASURED})cos(\varphi_{PHASE\_SHIFT}) - cos(\theta_{MEASURED})sin(\varphi_{PHASE\_SHIFT})\right) \quad (13)$$

The ϕ_{PHASE_SHIFT} is the phase error previously computed and the average post calibration magnitude is the dc magnitude result from Equation 1 that has been compensated for offset error and gain error. Table 3 shows the results of the calibration routine at various target phase inputs for the 0-dBm RF input amplitude case. The calculations performed in Equation 12 and Equation 13 are the correction factors to be built into any system intended to sense phase and magnitude in the manner presented here.

Receiver Subsystem Evaluation Results

Table 3. Results Achieved at Certain Target Phase Inputs with 0-dBm RF Input Amplitude

Target Phase	I-Ch Fully Corrected Input Voltage	Q-Ch Fully Corrected Input Voltage	Fully Corrected Phase Result	Absolute Measured Phase Error
–180°	–1.172 V	+0.00789 V	–180.386°	0.386°
–90°	–0.00218 V	–1.172 V	–90.107°	0.107°
0°	+1.172 V	+0.0138 V	+0.677°	0.676°
+90°	+0.000409 V	+1.171 V	+89.98°	0.020°
+180°	–1.172 V	+0.0111 V	+180.542°	0.541°

Figure 8 is a histogram of the measured absolute phase error showing better than 1° accuracy for every 10° step from –180° to +180°.

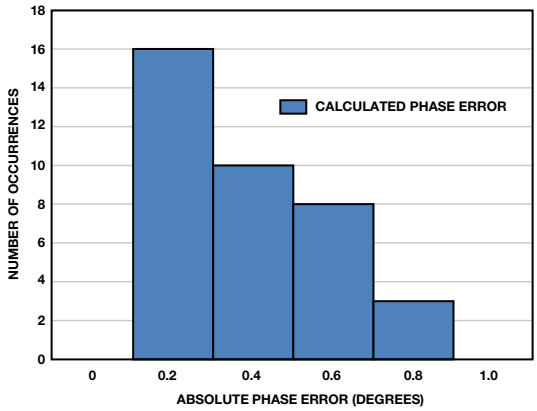


***Figure 8.** Measured absolute phase error histogram for 0-dBm input level with 10° phase steps.*

For accurate phase measurements at any given input level, the perceived phase-shift error (ϕ_{PHASE_SHIFT}) of RF relative to LO should be constant. If the measured phase-shift error begins to change as a function of the target phase step (ϕ_{TARGET}) or amplitude, then the calibration routine presented here will begin to lose accuracy. Evaluation results at a room temperature show that the phase-shift error is relatively constant for RF amplitudes ranging from a maximum of +11.6 dBm to approximately –20 dBm at 900 MHz.

Figure 9 demonstrates the dynamic range of the receiver subsystem along with the corresponding amplitude induced additional phase error. As the input amplitude decreases past –20 dBm, the phase-error calibration accuracy begins to degrade. The system user will need to determine the acceptable level of signal chain error to determine the minimum acceptable signal magnitude.

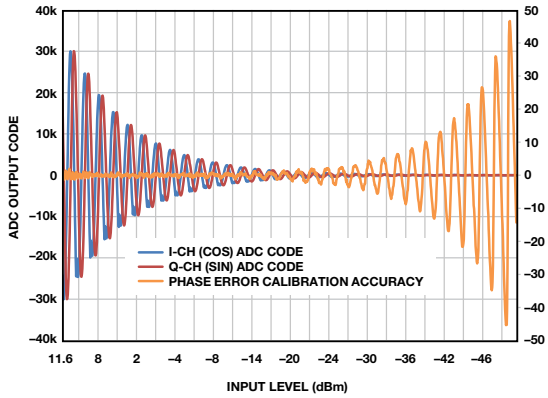


***Figure 9.** Dynamic range of receiver subsystem and corresponding additional phase error.*

The results presented in Figure 9 were collected with a 5-V ADC reference. The magnitude of the ADC reference can be reduced, providing a smaller quantization level for the system. This will provide an incremental improvement in phase error accuracy for small signals, but increases the chance for system saturation. To increase system dynamic range, another attractive option is implementing an oversampling scheme that will increase the noise-free bit resolution of the ADC. Every doubling in samples averaged will provide a ½ LSB increase in system resolution. The oversampling ratio for a given resolution increase is calculated as follows:

$$Oversampling\ Ratio = 2^{2N}\ where\ N = \#\ of\ bits\ increase \quad (14)$$

Oversampling will reach a point of diminishing returns when the noise amplitude is no longer sufficient to randomly change the ADC output code from sample to sample. At this point, the effective resolution of the system can no longer be increased. The bandwidth reduction from oversampling is not a significant concern because the system is measuring signals with a slowly changing magnitude.

The AD7903 evaluation software is available with a calibration routine that allows the user to correct the ADC output results for the three sources of error: phase, gain, and offset. The user will need to collect uncorrected results with their system to determine the calibration coefficients calculated in this article. Figure 10 shows the GUI with the calibration coefficients highlighted.

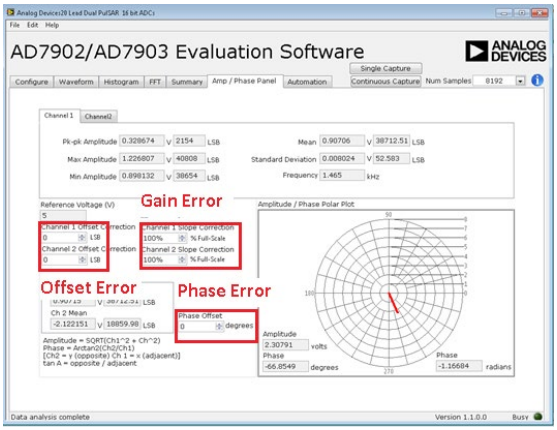


Figure 10. *Receiver subsystem calibration GUI.*

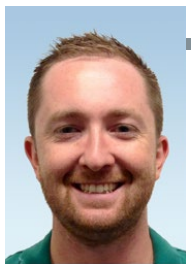
Once the coefficients are determined, this panel can also be used to deliver phase and magnitude results from the demodulator. The polar plot provides a visual indication of the observed RF input signal. The amplitude and phase calculations are performed using Equation 1 and Equation 2. The oversampling ratio can be controlled by adjusting the number of samples per capture using the "Num Samples" drop-down box.

Conclusion

This article presented key challenges associated with remote sensing applications and proposed a novel solution using the ADL5380, ADA4940-2, and AD7903 receiver subsystem to accurately and reliably measure the material content. The proposed signal chain features a wide dynamic range and achieves a 0° to 360° of measurement range with better than 1° accuracy at 900 MHz.

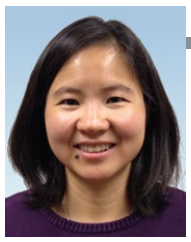
References

Mallach, Malte and Thomas Musch, "Ultra-Wideband Microwave Tomography: A Concept for Multiphase Flow Measurement" *GeMiC* 2014, Aachen, Germany, March 10–12, 2014.



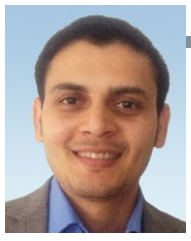
Ryan Curran

Ryan Curran [ryan.curran@analog.com] is a product applications engineer within the Precision Converters business unit at Analog Devices. He joined ADI in 2005 and has focused on SAR ADCs since joining the company. Ryan received his B.S.E.E. from the University of Maine in Orono, ME, and is currently pursuing an M.B.A. from the Isenberg School of Management at UMass Amherst.



Qui Luu

Qui Luu [qui.luu@analog.com] is an RF applications engineer at Analog Devices since June 2000. Qui received her B.S.E.E. from Worcester Polytechnic Institute in Worcester, MA, in 2000 and her M.S.E.E. from Northeastern University in Boston, MA, in 2005.



Maithil Pachchigar

Maithil Pachchigar [maithil.pachchigar@analog.com] is an applications engineer within the Precision Converters business unit at Analog Devices. He joined ADI in 2010 and supports the precision ADC product portfolio and customers in the industrial, instrumentation, medical, and energy segments. Having worked in the semiconductor industry since 2005, Maithil has published several technical articles and application notes. He received an M.S.E.E. from San Jose State University in 2006 and an M.B.A. from Silicon Valley University in 2010.

Also by this Author:

Demystifying High-Performance Multiplexed Data-Acquisition Systems

Volume 48, Number 3

Synchronous Detectors Facilitate Precision, Low-Level Measurements

By Luis Orozco

Introduction

Synchronous detectors can extract small signals, buried in the noise floor, to measure properties such as very small resistance, light absorption or reflection against bright backgrounds, or strain in the presence of high noise levels.

In many systems, the noise increases as the frequency approaches zero. For example, op amps have 1/f noise and light measurement is subject to noise from changing ambient light conditions. Moving the measurement away from the low-frequency noise increases the signal-to-noise ratio, allowing weaker signals to be detected. For example, modulating a light source at a few kilohertz facilitates measurement of reflected light that would otherwise be buried in the noise. Figure 1 shows how modulation enables recovery of a signal that was originally below the noise floor.

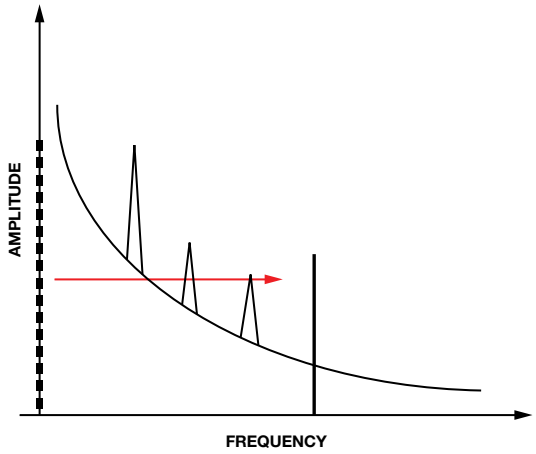


***Figure 1.** Modulating the signal moves it away from the noise sources.*

There are several methods to modulate the excitation signal. The easiest way is to repeatedly turn it on and off. This works well for driving LEDs, the voltage powering a strain gage bridge, and other types of excitation. With incandescent bulbs used in spectroscopy instruments, and other excitation sources that cannot be easily switched on and off, modulation can be accomplished by chopping the light with a mechanical shutter.

A narrow band-pass filter could remove all but the frequency of interest, allowing the original signal to be recovered, but designing the required filter with discrete components can be difficult. Alternatively, a synchronous demodulator can move the modulated signal back to dc while rejecting signals that are not synchronized to the reference. A device that uses this technique is called a lock-in amplifier.

Figure 2 shows a simple application of a lock-in amplifier. A light source modulated at 1 kHz illuminates a test surface. A photodiode measures the light reflected off the surface, which is proportional to the amount of contamination that has accumulated. The reference and measured signals are sine waves of the same frequency and phase, but different amplitudes. The reference signal driving the photodiode has a fixed amplitude, while the amplitude of the measured signal changes with the amount of light reflected.

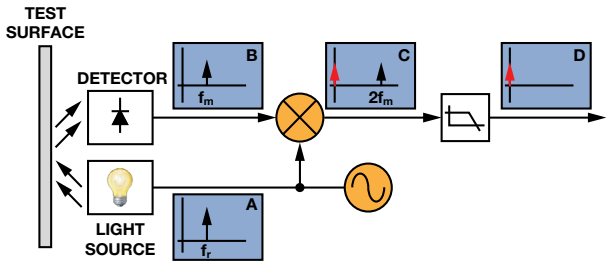


***Figure 2.** Measuring surface contamination with a lock-in amplifier.*

The result of multiplying two sine waves is a signal with frequency components at the sum and difference frequencies. In this case, the two sine waves have the same frequency, so the result is one signal at dc and another at twice the original frequency. The negative sign indicates it has a 180° phase shift. A low-pass filter removes everything but the dc component of the signal.

$$A \sin(2\pi f_m t) \times B \sin(2\pi f_m t) = \frac{1}{2} AB - \frac{1}{2} AB \cos(4\pi f_m t) \quad (1)$$

The advantage of using this technique becomes evident when considering a noisy input signal. The output of the multiplication results in only the signal at the modulation frequency moving back to dc, with all other frequency components moving to other, nonzero frequencies. Figure 3 shows a system with strong noise sources at 50 Hz and 2.5 kHz. A very weak signal of interest is modulated with a 1-kHz sine wave. The result of multiplying the input with the reference is a signal at dc, and other signals at 950 Hz, 1050 Hz, 1.5 kHz, 2 kHz, and 3.5 kHz. The dc signal contains the desired information, so a low-pass filter can remove the other frequencies.

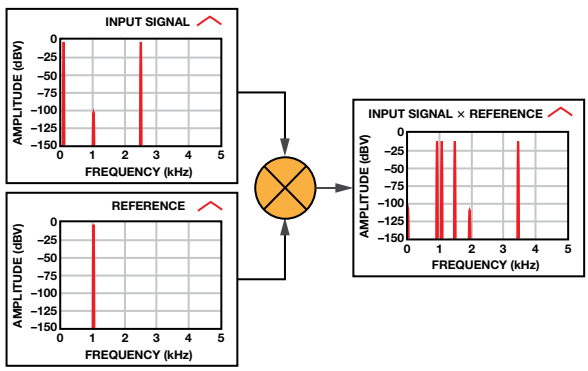


***Figure 3.** Synchronous demodulation picks out a weak signal at 1 kHz in the presence of strong noise sources at 50 Hz and 2.5 kHz.*

Any noise components that are close to the signal of interest will appear at frequencies close to dc so it is important to pick a modulation frequency that does not have strong noise sources near it. If this is not possible, a low-pass filter with a very low cutoff frequency and sharp response, at the expense of long settling time, will be required.

Practical Lock-In Implementations

Generating a sine wave to modulate the signal source can be impractical, so some systems use a square wave instead. Generating a square-wave excitation is much simpler than generating a sine wave, because it can be done with something as simple as a microcontroller pin that toggles an analog switch or a MOSFET.

Figure 4 shows an easy way to implement a lock-in amplifier. A microcontroller or other device generates a square wave excitation that causes the sensor to respond. The first amplifier would be a transimpedance amplifier for a photodiode, or an instrumentation amplifier for a strain gage.

The same signal that excites the sensor controls the ADG619 SPDT switch. When the excitation signal is positive, the amplifier is configured for a gain of +1. When the excitation is negative, the amplifier is configured for a gain of –1. This is mathematically equivalent to multiplying the measured signal by the reference square wave. The output RC filter removes signals at other frequencies, so the output voltage is a dc signal equal to half the peak-to-peak voltage of the measured square wave.

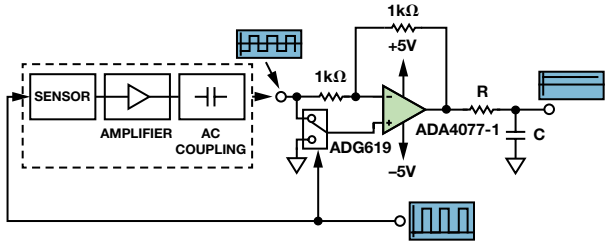


Figure 4. Lock-in amplifier using square-wave excitation.

Although the circuit is simple, choosing the right op amp is important. The ac-coupled input stage removes most of the low-frequency input noise, but will not remove the 1/f noise and offset error from the last amplifier. The ADA4077-1 precision amplifier has 250 nV p-p noise from 0.1 Hz to 10 Hz and 0.55 μV/°C offset drift, making it an ideal candidate for this application.

A square-wave-based lock-in amplifier is simple, but its noise rejection is inferior to those using sine waves. Figure 5 shows the frequency domain representation of square wave excitation and reference signals. A square wave comprises an infinite sum of sine waves at the fundamental and all odd harmonics. Multiplying two square waves of the same frequency involves multiplying each sine component of the reference times each sine component of the measured signal. The result is a dc signal that contains energy from every harmonic of the square wave. Unwanted signals that appear at odd harmonic frequencies will not be filtered out, although they will be scaled down depending on the harmonic they fall in. Thus, it is important to choose a modulation frequency whose harmonics are not at the frequency or harmonic of any known noise sources. To reject line noise, for example, choose a modulation frequency of 1.0375 kHz, which does not coincide with harmonics of 50 Hz or 60 Hz, instead of using 1 kHz, which is the 20th harmonic of 50 Hz.

Even with this drawback, the circuit is simple and low cost. Using a low-noise amplifier and choosing the right modulation frequency can still result in a great improvement over trying to make a dc measurement.

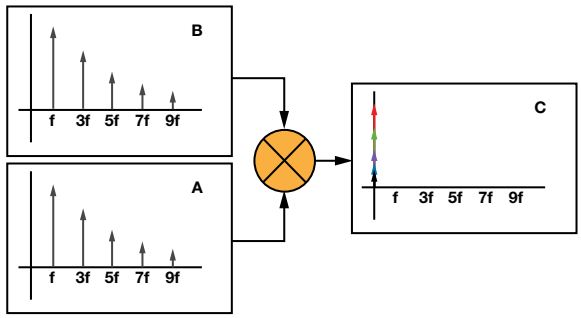


Figure 5. If the input signal (A) and the reference (B) are both square waves, multiplying them together (C) effectively demodulates every harmonic of the input signal.

A Simple, Integrated Alternative

The circuit shown in Figure 4 requires an op amp, a switch, and some discrete components, plus a reference clock from a microcontroller. An alternative is to use an integrated synchronous demodulator, as shown in Figure 6. The ADA2200 includes a buffered input, a programmable IIR filter, a multiplier, and a block that shifts the reference signal by 90°, making it easy to measure or compensate for phase shifts between the reference clock and the input signal.

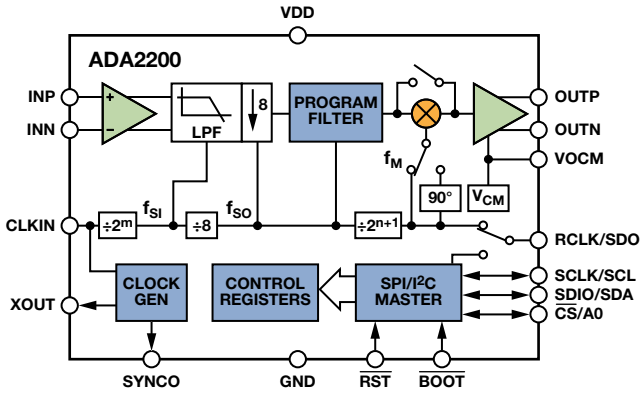


Figure 6. ADA2200 block diagram.

Implementing a lock-in detection circuit with the ADA2200 simply requires applying a clock frequency that is 64× the desired reference frequency, as shown in Figure 7. The default configuration of the programmable filter is a band-pass response, removing the need to ac couple the signal. The sampled analog output generates images around multiples of the sampling rate, so an RC filter followed by a Σ-Δ ADC can remove these images and measure only the demodulated dc component of the signal.

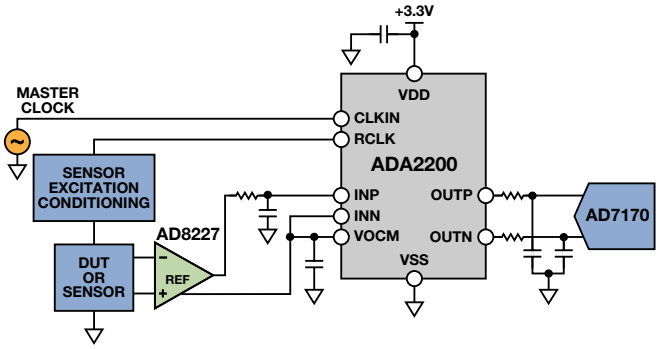


Figure 7. Lock-in amplifier implementation with the ADA2200.

Improving the Square-Wave Lock-In Circuit

Figure 8 shows an improvement to a square-wave modulated circuit. The sensor is excited with a square wave, but the measured signal is multiplied with a sine wave of the same frequency and phase. Now, only the signal content at the fundamental frequency will move to dc, while all of the other harmonics will move to nonzero frequencies. This makes it easy to use a low-pass filter to eliminate everything but the dc component of the measured signal.

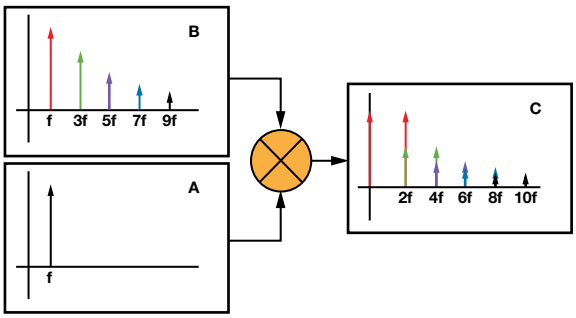


Figure 8. Using a sine wave as the reference signal prevents noise from demodulating to dc.

One additional difficulty is that any phase shift between the reference signal and the measured signal will produce a smaller output than if they were perfectly in phase. This can occur if the sensor signal conditioning circuit includes filters that introduce phase delay. With an analog lock-in amplifier, the only way to address this is to include additional phase-compensation circuits in the reference signal path. This is not trivial, because the circuit must be adjustable to compensate for different phase delays, and will vary with temperature and component tolerance. An easier alternative is to add a second stage that multiplies the measured signal with a 90° phase-shifted version of the reference. The result of this second stage will be a signal proportional to the out-of-phase component of the input, as shown in Figure 9.

The outputs of the low-pass filters after the two multiplier stages are low-frequency signals proportional to the in-phase (I) and quadrature (Q) components of the input. To calculate the magnitude of the input signal, simply take the sum of the squares of the I and Q outputs. An additional benefit of this architecture is that it allows the phase between the excitation/reference signal and the input to be calculated.

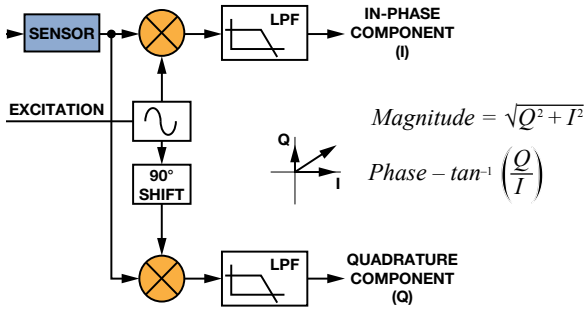


Figure 9. Using a quadrature version of the reference signal to calculate magnitude and phase.

All of the lock-in amplifiers discussed so far generate a reference signal that excites a sensor. One final refinement is to allow an external signal to act as a reference. For example, Figure 10 shows a system that uses a broadband incandescent light to test the optical properties of a surface. A system like this can measure parameters such as the reflectivity of mirrors or the amount of contamination on a surface. It is much simpler to use a mechanical chopper disk to modulate an incandescent source than to apply electronic modulation. A low-cost position sensor near the chopper disk generates a square-wave reference signal to feed the lock-in amplifier. Rather than using this signal directly, a phase-locked loop generates a sine wave of the same frequency and phase as the input reference. One caveat of this approach is that the internally generated sine wave must have low distortion.

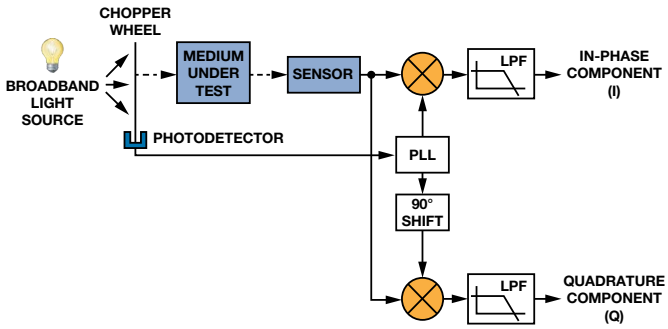


Figure 10. Using a PLL to lock on to an external reference signal.

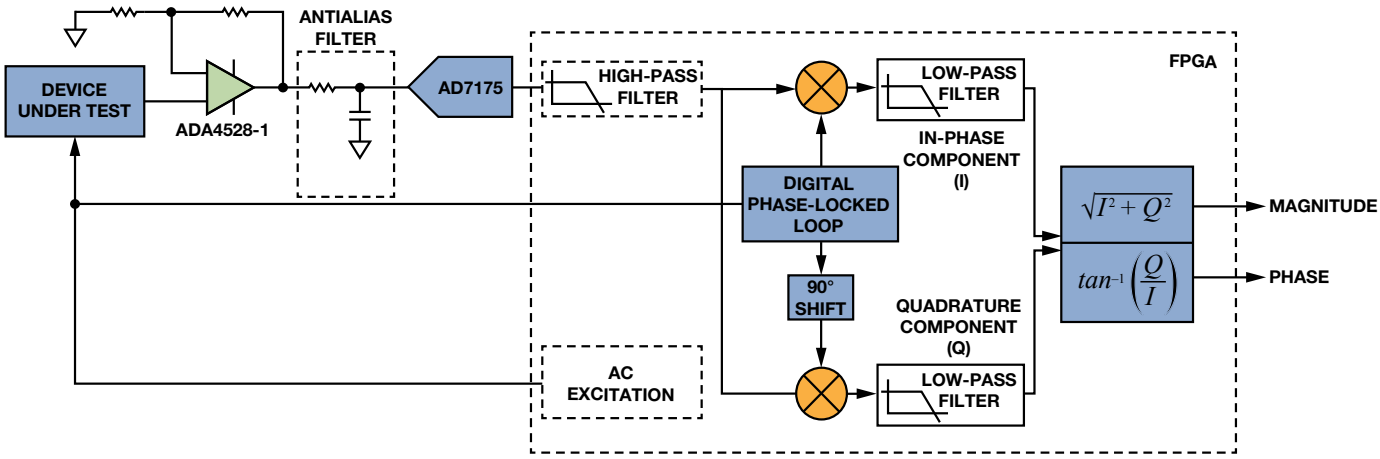


Figure 11. *FPGA–based lock–in amplifier.*

Although this system could be implemented using a discrete PLL and multipliers, using an FPGA to implement the lock-in amplifier function results in several performance benefits. Figure 11 shows a lock-in amplifier built with an FPGA using a front end based on the ADA4528-1 zero-drift amplifier and an AD7175 24-bit Σ-Δ ADC. This application does not need very high bandwidth, so the lock-in amplifier's equivalent noise bandwidth can be set to 50 Hz. The device under test is any sensor that can be excited externally. The amplifier is configured with a noise gain of 20 to take advantage of the full-scale range of the ADC. Although dc errors do not affect the measurement, it is important to minimize offset drift and 1/f noise because they will decrease the available dynamic range, especially when the amplifier is configured for high gain.

The ADA4528-1's 2.5 µV max input offset error represents only 10 ppm of the AD7175's full-scale input range with a 2.5-V reference. The digital high-pass filter after the ADC removes any dc offset and low-frequency noise. To calculate the output noise, first calculate the voltage noise density of the AD7175. The data sheet specifies the noise at 5.9 µV rms with an output data rate of 50 kSPS, using the sinc5 + sinc1 filter and with the input buffer enabled. The equivalent noise bandwidth with these settings is 21.7 kHz, which results in a voltage noise density of 40 nV/√Hz.

The 5.9-nV/√Hz broadband input noise of the ADA4528 appears at the output as 118 nV√Hz, resulting in a combined noise density of 125 nV/√Hz. Since the digital filter has an equivalent noise bandwidth of only 50 Hz, the output noise is 881 nV rms. With a ±2.5 V input range, this results in a system with 126-dB dynamic range. Bandwidth can be traded for dynamic range by adjusting the frequency response of the low-pass filter. For example, setting the filters for a bandwidth of 1 Hz results in 143-dB dynamic range, and setting the bandwidth to 250 Hz results in 119-dB dynamic range.

The digital phase-locked loop generates a sine wave locked to the excitation signal, which can be internally or externally generated, and does not have to be a sine wave. Any harmonics in the reference sine wave will multiply with the input signal, demodulating noise and other unwanted signals present at the harmonic frequencies, just like when two square waves are multiplied. One advantage of digitally generating the reference sine wave is that very low distortion can be obtained by adjusting the numeric precision.

Figure 12 shows four digitally generated sine waves using 4-, 8-, 16-, and 32-bit precision. Obviously, using 4-bit precision results in performance not much different from that of Figure 5, but the situation quickly improves by using higher precision. With 16-bit precision, generating an analog signal with such low total harmonic distortion (THD) would be difficult, and with 32 bits, the THD is over –200 dB, making it impossible to match with an analog circuit. In addition, these are digitally generated signals, so they are perfectly repeatable. Once the data has been converted to digital and enters the FPGA, no additional noise or drift will be added.

After the multipliers, the low-pass filters remove any high-frequency components and output the in-phase and quadrature components of the signal. With an equivalent noise bandwidth of only 50 Hz, there is no reason to deliver data at the original sampling rate of 250 kSPS. The low-pass filters can include a decimation stage to reduce the output data rate. The last step is to calculate the magnitude and phase of the input signal from the in-phase and quadrature components.

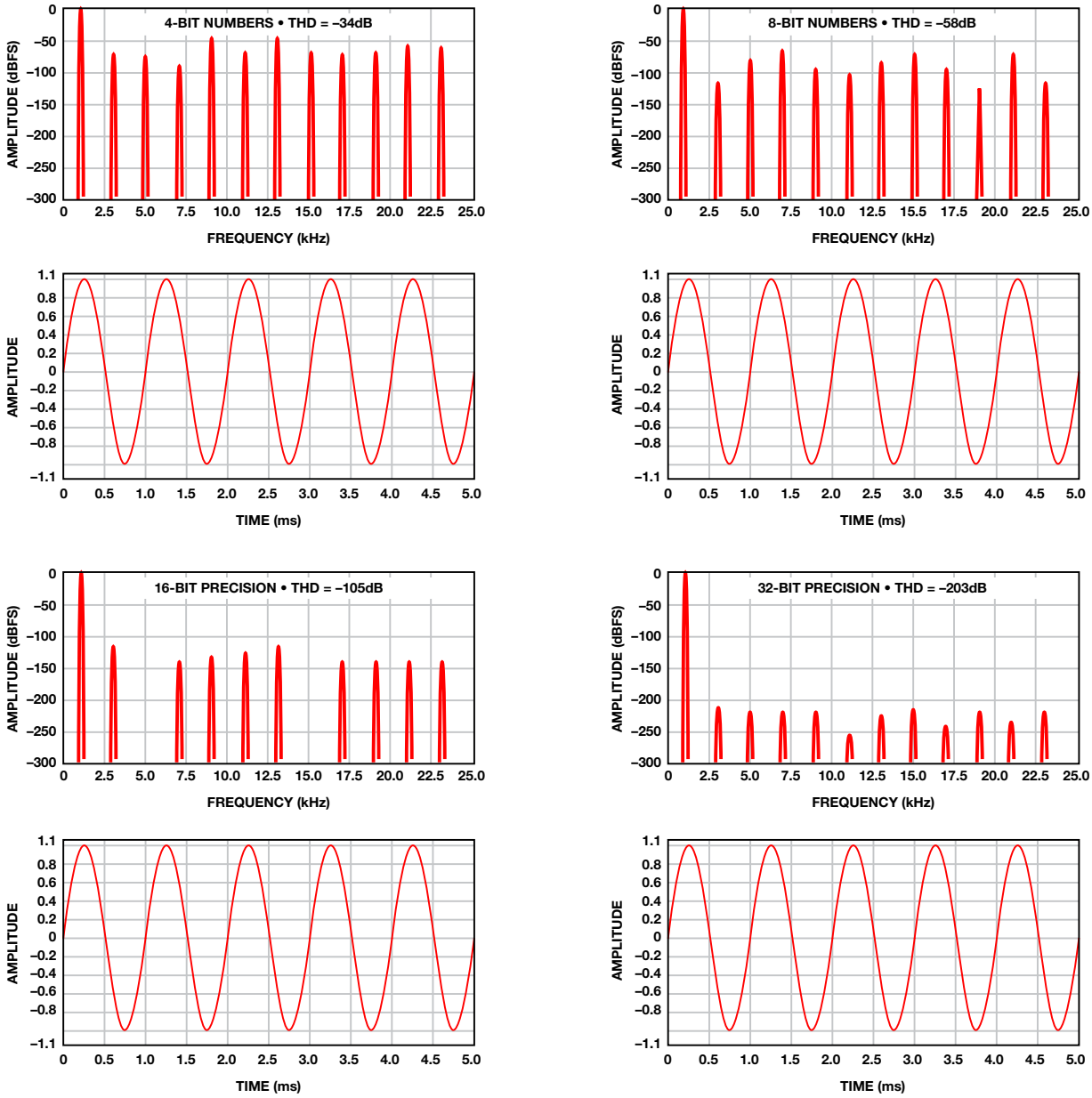
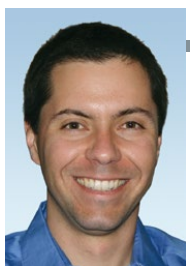


Figure 12. Numerically generated sine waves with different numeric precision.

Conclusion

Small low-frequency signals buried in the noise floor can be difficult to measure, but applying modulation and lock-in amplifier techniques can provide high-precision measurements. In its simplest form, a lock-in amplifier can be an op amp that switches between two gains. Although this does not result in the lowest noise performance, the simplicity and low cost of the circuit make it attractive when compared with a simple dc measurement. An improvement on this circuit is to use a sine wave reference and a multiplier, but this can be challenging to implement in the analog domain. For the ultimate performance, consider using a low-noise, high-resolution Σ-Δ ADC to digitize the input signal, generating the reference sine wave and all of the other elements in the digital domain.

Luis Orozco [luis.orozco@analog.com] is a system applications engineer in ADI's industrial and instrumentation segment. He focuses on precision instrumentation, chemical analysis, and environmental monitoring applications. Luis joined ADI in February 2011. Prior to joining ADI, he designed data acquisition equipment for over 10 years.



Luis Orozco

Also by this Author:

Accurate Analog Controller Optimizes High-Efficiency Li-Ion Battery Manufacturing

Volume 48, Number 3

Wearable Electronic Devices Monitor Vital Signs, Activity Level, and More

Health Monitoring Is Going Wearable

By Jan-Hein Broeders

When I was a little boy, my mom always made sure that I had enough change to make a phone call in case of emergency. Twenty years later, mobile phones allowed us to make calls at any time and place. After another 20 years of innovation, the phone is no longer the key feature of our smart devices, which can take beautiful pictures, stream audio and video, provide access to a wide variety of services—and are now becoming our personal trainers. The devices, loaded with sensors or connected to bodily worn sensors, monitor day-to-day activity and personal health. An increasing awareness of our health has fueled interest in measuring vital parameters—such as heart rate, temperature, oxygen saturation, blood pressure, activity level, and calories burned—and following their daily trends.

Now, a universal sensor front end with multiple sensors can monitor these parameters. The biggest challenges are to minimize size and maximize battery lifetime. This article discusses solutions for the rapidly growing market for wearable electronics.

The Most Important Vital Sign

Without a heartbeat we would be in serious trouble, so pulse or heart rate is by far the most important parameter to be monitored. In addition to the number of beats per minute, we want to check the behavior of the heart as a function of activity. The rhythm is also important, as rapidly changing heart rates are a sign of cardiac disease.

Monitoring heart rate and heart activity is classically done by measuring biopotential with an electrocardiogram (ECG). Electrodes connected to the body measure signals caused by electric activity in the cardiac tissue. This principle is used in professional diagnostic systems, where up to 10 electrodes can be connected to the chest and limbs. ECGs provide detailed information regarding the various components (P-, QRS-, and T-wave) of one heartbeat.

Single-lead ECGs are more common in the sports world, with a two-electrode chest strap measuring heart activity. ECG waveforms can be detected, but most systems just measure heart rate. These straps are uncomfortable, so the sports and wellness industry is looking for alternatives, such as integrating the electrodes into a sport shirt. The AD8232 single-lead heart rate monitor front end, shown in Figure 1, was developed for this kind of low-power wearable application. It includes an instrumentation amplifier with a gain of 100 V/V and a high-pass filter to block the offset voltage generated by the half-cell potential of the electrodes on the skin. An output buffer and low-pass filter reject the high-frequency component generated by muscle activity (EMG signals). This low-power front end, which draws 170 μA, can be used with the ADuCM350 16-bit meter-on-a-chip to perform high-performance, single-lead ECG measurements.

New Method for Measuring Heart Rate

A new trend for measuring heart rate is the photoplethysmogram (PPG), an optical technique that retrieves cardiac information without measuring the biopotential. PPG has mainly been used to measure blood oxygen saturation (SpO_2), but can provide cardiac information without a biopotential measurement. With PPG technology, heart-rate monitors can be integrated in wearable devices such as wristwatches or bracelets. This is not possible with biopotential systems due to the tiny signal levels.

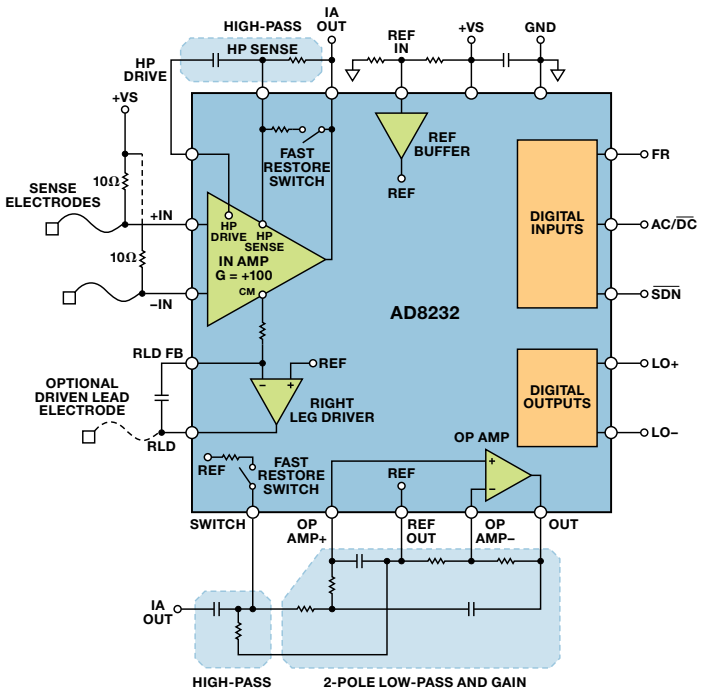


Figure 1. AD8232 single-lead ECG front end.

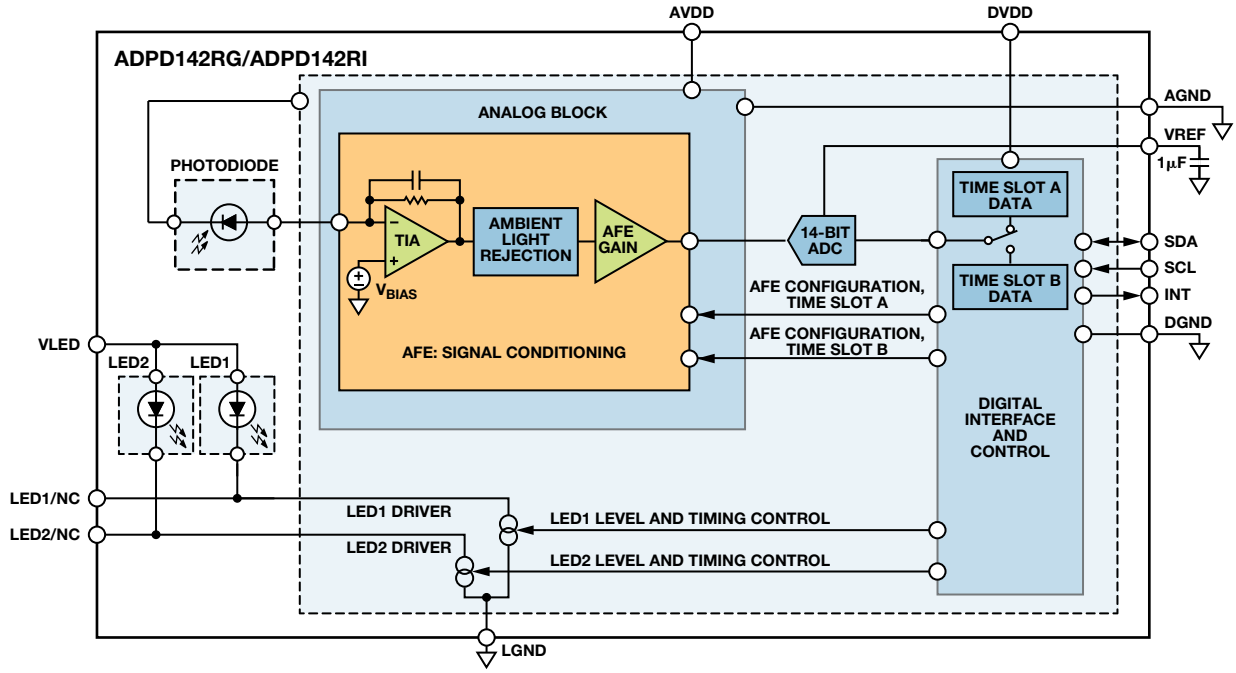


Figure 2. ADPD142 optical module.

In optical systems, light is transmitted through the surface of the skin. Light absorbed by the red blood cells is measured with a photosensor. As the heart beats, the changing blood volume scatters the amount of light received. When measured on a finger or earlobe, where considerable arterial blood is available, a red or infrared light source provides the best accuracy. Arteries are rarely located on top of the wrist, however, so with wrist worn devices, pulsatile components must be detected from veins and capillaries just under the surface of the skin, making green light better.

The ADPD142 optical module, shown in Figure 2, features a complete photometric front end, with integrated photosensor, current sources, and LEDs. Designed for reflective measurement, it can be used to implement a PPG measurement. All components are mounted in a small module.

Challenges with Optical VSM

The main challenges for measuring PPG on a wrist-worn device are due to ambient light and motion-generated artifacts. The Sun, which generates dc errors, is relatively easy to cancel out, but light from fluorescent and energy-saving lamps carry frequency components that cause ac errors. The analog front end uses two structures to reject interferers from dc to 100 kHz. After the analog signal conditioning, a 14-bit, successive-approximation analog-to-digital converter (ADC) digitizes the signal, which is transmitted via an I²C interface to a microcontroller for final post processing.

A synchronized transmit path is integrated in parallel with the optical receiver. Its independent current sources can drive two separate LEDs with current levels programmable up to 250 mA. The LED currents are pulsed, with pulse lengths in the microsecond range, so the average power dissipation is kept low to maximize battery lifetime.

The LED driving circuit is dynamic and configurable on-the-fly, making it independent of environmental conditions such as ambient light, the tint of the wearer's skin and hair, or sweat between the sensor and the skin that would otherwise decrease sensitivity. The excitation LEDs can be configured easily to build an autoadaptive system. All timing and synchronization is handled by the analog front end, so no overhead is required from the system processor.

Two versions of the ADPD142 are available: the ADPD142RG integrates red and green LEDs to support optical heart-rate monitoring; and the ADPD142RI integrates red and infrared LEDs for oxygen saturation (SpO_2) measurement.

Influence of Motion

Motion also disturbs optical systems. When optical heart-rate monitors are used for sleep studies, this may not be an issue, but sport watches and bracelets worn during exercise have a hard time cancelling out motion artifacts. Motion between the optical sensors (LED and photodetector) and the skin will decrease the sensitivity of the optical signal. In addition, the frequency components of the motion might be seen as a heart-rate measurement, so the motion must be measured and compensated. The tighter the device is attached to the body, the lower the impact, but it is nearly impossible to cancel this out mechanically.

Various methods are used to measure motion. One is optical, using multiple LED wavelengths. The common signals indicate motion, while the differential signals detect the heart rate. It's better to use a real motion sensor, however. Not only will this allow accurate measurement of motion applied to the wearable device, but it can also be used for additional features, such as tracking activity, counting steps, or starting an application when a certain *g*-force is detected.

The ADXL362 micropower, 3-axis MEMS (microelectromechanical system) accelerometer is ideal for sensing motion in battery-operated wearable applications. Its 12-bit ADC converts acceleration into a digital signal with 1-m*g* resolution. The power consumption dynamically scales with the sampling rate, and is only 1.8 µA with a 100-Hz output data rate and 3.0 µA at 400 Hz. These higher data rates are useful for user interface, such as tap/double-tap detection.

For starting an application when motion is detected, high-speed sampling is not needed, so that the data rate can be reduced to 6 Hz, resulting in an average power consumption of 300 nA. This makes this sensor attractive for low-power applications and implantable devices, in which batteries cannot be replaced easily. The ADXL362 is available in a 3.0-mm × 3.25-mm package. Figure 3 shows the supply current vs. output data rate for several supply voltages.

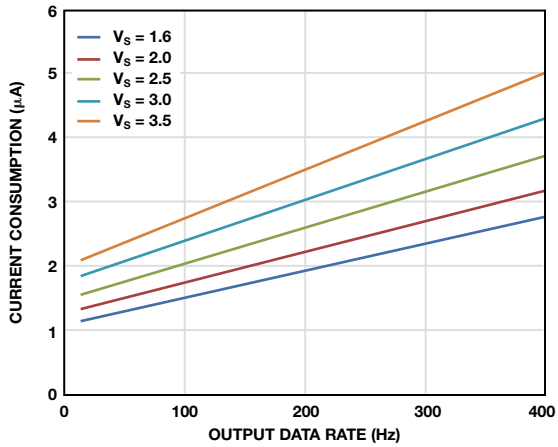


Figure 3. ADXL362 supply current as function of the output data rate.

Connecting the Sensors in the System

The heart of the system that connects all these sensors, runs the required software, and stores, displays, or transmits the results is the ADuCM350 mixed-signal meter-on-a-chip, which integrates a high-performance analog front end (AFE) with a 16-MHz ARM® Cortex®-M3 processor core, as shown in Figure 4. The flexibility of the AFE and rich feature set of the microprocessor make this chip ideal for portable and wearable applications. The configurable AFE allows it to be used with nearly any sensor, and its programmable waveform generator powers analog sensors with ac or dc signals. The high-performance receive signal chain conditions sensor signals and converts them to digital with a true 16-bit, 160-kSPS ADC, which features ±1-LSB max INL and DNL, and no missing codes. It can be used with any type of input signal, including voltage, current, potentiostat, photocurrent, and complex impedance.

The AFE can be operated in standalone mode without involvement of the Cortex-M3 processor. A programmable sequencer controls the measurement engine, with results stored into memory via DMA. Before starting a measurement, a calibration routine can be performed to correct offset and drift errors in the transmit-and-receive signal chains. For complex impedance measurements such as blood glucose, body mass index (BMI), or tissue discrimination applications, a built-in DSP accelerator provides a 2048-point, single-frequency discrete Fourier transform (DFT) without involvement of the Cortex-M3 processor. These high-performance AFE features make the ADuCM350 unique vs. other integrated solutions.

The Cortex-M3 processor supports various communication ports including I²S, USB, MIPI, and an LCD display driver (static). In addition, it includes flash memory, SRAM, and EEPROM, and supports five different power modes to maximize battery life.

Designed for use with ultralow-power sensors, the ADuCM350 is limited to low-speed devices. Applications that require more processing power could use Cortex-M3 cores that operate up to 80 MHz or Cortex-M4 processor cores.

What About Power?

Power is always a critical factor in portable and wearable devices. The devices described in this article are designed for high performance, small size, and low power, but integrating everything, including the battery, in a small package is still a challenge. Despite new battery technologies that bring more capacity per mm³, the battery is still large compared to the electronics.

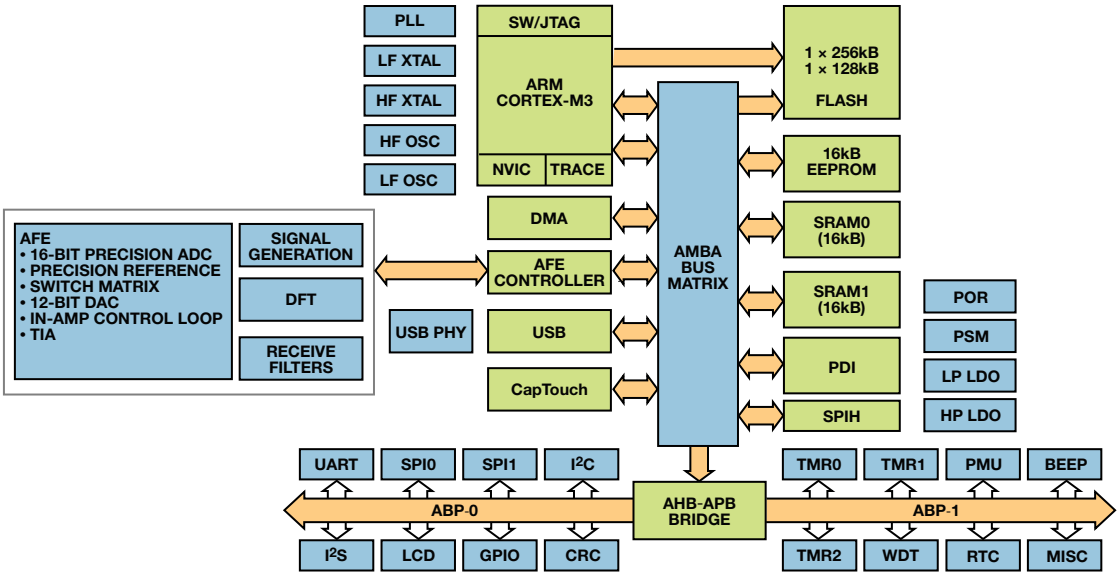


Figure 4. Cortex-M3 with integrated AFE.

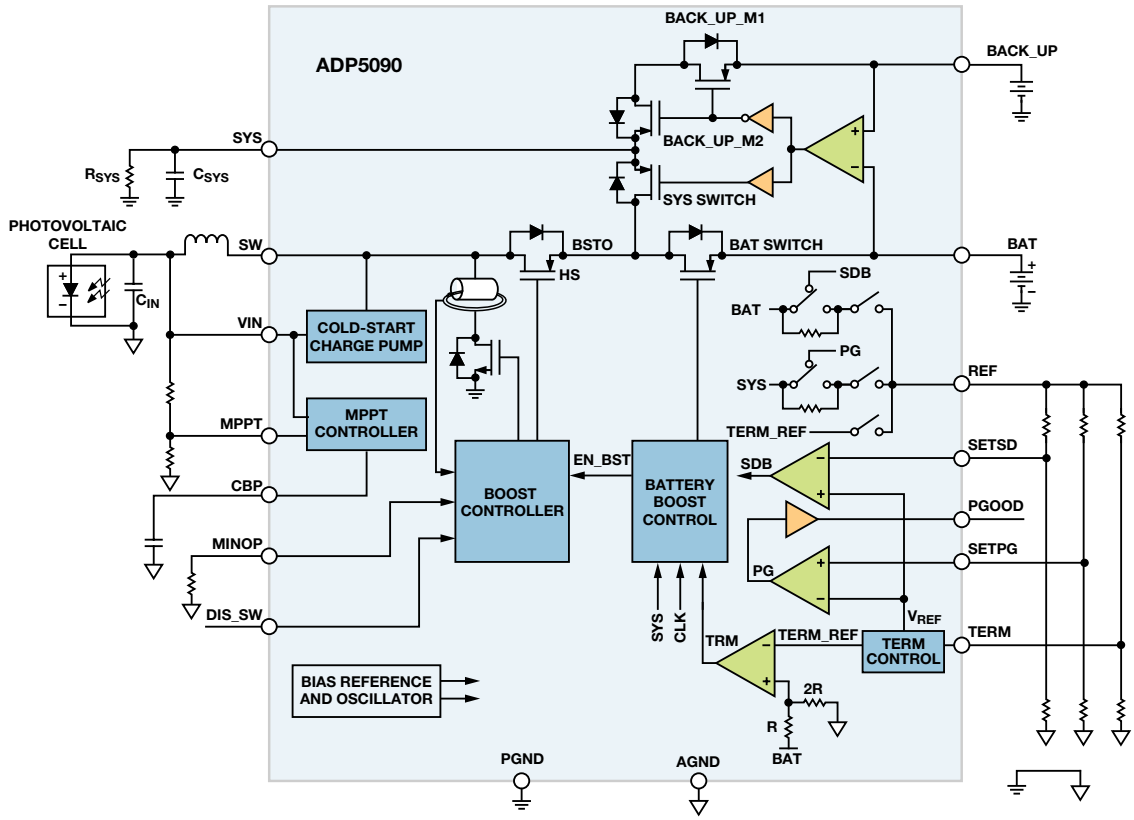


Figure 5. ADP5090 energy harvester.

Energy harvesting can reduce battery size and extend battery life. Various technologies are used to harvest energy, including thermoelectric, piezoelectric, electromagnetic, and photovoltaic, with light and heat being the most appropriate for wearable devices. The sensors usually don't provide a lot of output power, so every joule generated should be caught and used. The ADP5090 ultralow-power boost regulator, shown in Figure 5, bridges the gap between harvester and battery. This efficient switch-mode power supply boosts input voltages from as low as 100 mV up to 3 V. During a cold start, with the battery completely discharged, a 380-mV minimum input voltage is required, but in normal operation, where either the battery is not completely drawn down or some energy is left in the super capacitor, any input signal down to 100 mV can be converted to a higher potential and stored for later use.

Housed in a tiny 3-mm × 3-mm package, the chip is programmable for use with various harvester sensors. It draws 250-nA maximum quiescent current and works with almost any battery technology from Li-Ion to thin-film batteries and super capacitors. Integrated protection circuits ensure safe operation.

Conclusion

This article describes some low-power products for wearable and personal health applications, but this fast growing market is changing rapidly. ADI technology can convert challenging problems into complete products and turnkey solutions. Watch for more to come.

References

www.analog.com/healthcare

Bioimpedance Circuit Design Challenges for Body-Worn Systems

By José Carlos Conchell

Introduction

Wearable devices for vital-sign monitoring (VSM) are transforming the healthcare industry, allowing us to monitor our vital signs and activity anytime, anywhere. The most relevant information about some of these key parameters can be obtained by measuring body impedance.

To be effective, wearable devices must be small, low cost, and low power. In addition, measuring bioimpedance entails challenges related to the use of dry electrodes and safety requirements. This article provides some solutions to these issues.

Electrode Half-Cell Potential

The electrode is an electrical transducer that makes contact between an electronic circuit and a nonmetallic object such as human skin. This interaction produces a voltage, known as the half-cell potential, which reduces the dynamic range of the ADC. The half-cell potential varies with the electrode material, as shown in Table 1.

Table 1. Half-Cell Potentials for Common Materials

Metal and Reaction	Half-Cell Potential (V)
$Al \rightarrow Al^{3+} + 3e^-$	–1.706
$Ni \rightarrow Ni^{2+} + 2e^-$	–0.230
$Ag + Cl^+ \rightarrow AgCl + e^-$	+0.223
$Ag \rightarrow Ag^+ + e^-$	+0.799
$Au \rightarrow Au^+ + e^-$	+1.680

Electrode Polarization

When no current flows through the electrode, the half-cell potential is observed. The measured voltage increases when dc current flows. This overvoltage impedes current flow, polarizing the electrode, and diminishing its performance, especially under conditions of motion. For most biomedical measurements, nonpolarizable (wet) electrodes are preferred over polarizable (dry) electrodes, but portable and consumer devices typically use dry electrodes due to their low cost and reusability.

Electrode–Skin Impedance

Figure 1 shows an equivalent circuit of the electrode. R_d and C_d represent the impedance associated with the electrode-skin interface and polarization at this interface, R_s is the series resistance associated with the type of electrode materials, and E_{hc} is the half-cell potential.

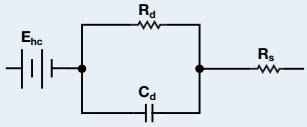


Figure 1. Equivalent circuit model for biopotential electrode.

The electrode-skin impedance is important when designing the analog front end due to the high impedances involved. Dominated by the series combination of R_s and R_d at low frequencies, the impedance decreases to R_d at high frequencies due to the capacitor's effect. Table 2 shows typical values for R_d, C_d, and the impedance at 1 kHz.

Table 2. Typical Electrode-Skin Impedance

Material	R_d	C_d	$\lvert R_d//C_d \rvert$ @ 1 kHz
Wet Ag/AgCl	350 kΩ	25 nF	6 kΩ
Metal Plate	1.3 MΩ	12 nF	13 kΩ
Thin Film	550 MΩ	220 pF	724 kΩ
MEMS	650 kΩ	Negligible	650 kΩ

IEC 60601

IEC 60601 is a series of technical standards for the safety and effectiveness of medical electrical equipment published by the International Electrotechnical Commission. It specifies 10 µA maximum dc-leakage current through the body under normal conditions and 50 µA maximum under worst-case, single-fault conditions. The maximum ac-leakage current depends on the excitation frequency. If the frequency (f_E) is less than or equal to 1 kHz, the maximum allowed current is 10 µA rms. If the frequency is greater than 1 kHz, the maximum allowed current is $\frac{f_E}{1000\ \text{Hz}} \times 10\ \mu\text{A rms}$. These patient current limits are important circuit design parameters.

Circuit Design Solution

The impedance measurement requires a voltage/current source and a current/voltage meter, so DACs and ADCs are commonly used. A precision voltage reference and voltage/current control loops are essential, and a microcontroller is typically required to process data and obtain the real and imaginary parts of the impedance. Additionally, wearable devices are typically powered by a unipolar battery. Finally, integration of as many components as possible in a single package is very beneficial. The ADuCM350 ultralow-power, integrated, mixed-signal meter-on-a-chip includes a Cortex-M3 processor and a hardware accelerator that can perform a single-frequency discrete Fourier transform (DFT), making it a powerful solution for wearable devices.

To meet IEC 60601 standards, the ADuCM350 is used with the AD8226 instrumentation amplifier to make high-precision measurements using a 4-wire technique, as shown in Figure 2. Capacitors C_{SIO1} and C_{ISO2} block dc current flow between the electrode and the user, eliminating the polarization effect. An ac signal generated by the ADuCM350 is propagated into the body.

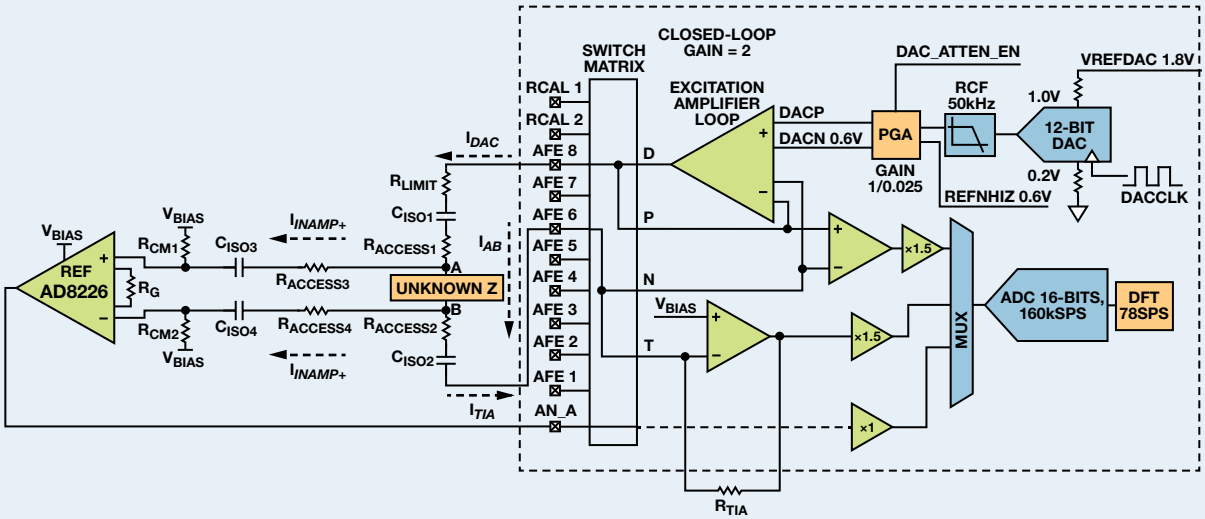


Figure 2. Four-wire isolated measurement circuit using ADuCM350 and AD8226.

Capacitors C_{ISO3} and C_{ISO4} block the dc level from the ADC, solving the half-cell potential problem and maintaining maximum dynamic range at all times. C_{ISO1}, C_{ISO2}, C_{ISO3}, and C_{ISO4} isolate the user, ensuring zero dc current in normal mode and in the first case of failure, and zero ac current in the first case of failure. Finally, resistor R_{LIMIT} is designed to guarantee that the ac current in normal operation is below the limit. R_{ACCESS} symbolizes the skin-electrode contact.

The ADuCM350 measures the current from the transimpedance amplifier (TIA) and the output voltage of the AD8226 to calculate the unknown bodyimpedance. R_{CM1} and R_{CM2} must be as high as possible to ensure that most of the current flows through the unknown impedance and the TIA. The recommended value is 10 MΩ.

Design Limitations

This design presents some limitations when the eletrode-skin impedance is close to 10 MΩ at the excitation frequency. The electrode-skin impedance must be significantly smaller than R_{CM1} and R_{CM2} (10 MΩ), or V_{INAMP+} will not be equal to *A* and V_{INAMP-} will not be equal to *B*, and the measurement accuracy will be degraded. The electrode-skin impedance is typically much smaller than 1 MΩ when the excitation frequency is greater than 1 kHz, as shown in Table 2.

Validation

To prove the accuracy of this design, the system was tested with different unknown impedances, with the results compared to those measured by an Agilent 4294A impedance analyzer. The magnitude error was less than ±1% in all the tests. The absolute phase error was less than 1° at 500 Hz and 5 kHz. The 9° phase offset error at 50 kHz could be corrected in software.

Conclusion

Designs for battery-powered, body-worn devices that measure bioimpedance must consider low power, high SNR, electrode polarization, and IEC 60601 safety requirements. A solution using the ADuCM350 and AD8226 was described here. Additional details, including complete design equations, can be found at www.analog.com/library/analogdialogue/archives/48-12/bio_imp.pdf.

References

Neuman, Michael R. "Biopotential Electrodes." *The Biomedical Engineering Handbook*, Fourth Edition. CRC Press, 2015

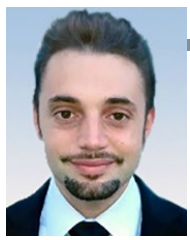
Chi, Mike Yu, Tzyy-Ping Jung, and Gert Cauwenberghs. "Dry-Contact and Noncontact Biopotential Electrodes: Methodological Review." *IEEE Reviews in Biomedical Engineering*, Volume 3, 2010.

http://en.wikipedia.org/wiki/IEC_60601

Jan-Hein Broeders

Jan-Hein Broeders [jan.broeders@analog.com] is ADI's healthcare business development manager in Europe, the Middle East, and Africa. Working closely with healthcare professionals, he translates their present and future requirements into solutions. Jan-Hein has more than 20 years of experience in the semiconductor industry. He joined ADI as global FAE for Philips in 2005, and has been in his current role since 2008. He holds a bachelor's degree in electrical engineering from the University of 's-Hertogenbosch, the Netherlands.

José Carlos Conchell



José Carlos Conchell [jose.conchell@analog.com] received his degree in electronic engineering from Universitat de València, Spain, in 2010, then joined ADI as a system applications engineer in the Healthcare Group.

Two New Devices Help Reinvent the Signal Generator

By David Hunter

In the past, the most difficult part of an arbitrary waveform generator was designing the output stage. Typical signal generators offer output ranges from 25 mV to 5 V. To drive a 50-Ω load, traditional designs used high-performance discrete devices, a large number of integrated devices in parallel, or an expensive ASIC, with designers spending countless hours to create a stable, high-performance output stage with a wide programmable range. Now, advancements in technology have produced amplifiers that can drive these loads, reducing output stage complexity while decreasing cost and time to market.

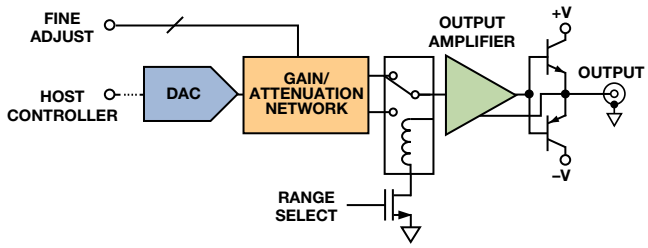


***Figure 1.** A typical signal generator model.*

When using general-purpose signal generators, a frequency is entered, a button is pressed, and the instrument produces a new frequency. Next, the desired output power is entered, and another button is pressed. Relays click as they switch internal networks to adjust the output level. This discontinuous operation is required to compensate for the lack of a wide programmable range. This article proposes a new architecture that also solves this half of the problem with the output stage design.

The two key components that solve this front-end design challenge are: a high-performance output stage that provides high speed, high voltage, and high output current; and a variable-gain amplifier (VGA) with continuous linear-in-dB tuning. This design targets 20-MHz performance, with 22.4-V amplitude (+39 dBm) into a 50-Ω load.

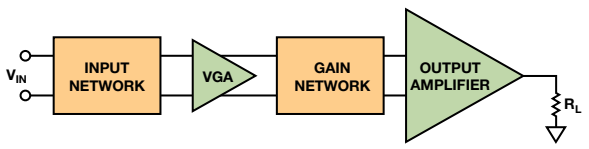


***Figure 2.** The smaller, simpler, signal generator output stage.*

New Compact Output Stage

The initial signal may come from a digital-to-analog converter (DAC) for a complex waveform, or from a direct-digital synthesis (DDS) device for sine-wave generation. In either case, its specifications and power adjustment capabilities may not be ideal. The first requirement is to provide attenuation or gain using a VGA. The gain provided by many VGAs is limited, however, and is seldom enough to be useful for this application.

If the output of the VGA can be set to a target level, then no matter what the input is, the output can be forced to a *known* amplitude. For example, if the desired output amplitude is 2 V, and the power output stage has a gain of 10, then the output amplitude of the VGA should be regulated to 0.2 V. When the output stage is correctly designed, the output amplitude is ultimately set by the output of the VGA. Unfortunately, most VGAs become the bottleneck due to their limited programmable range.

A typical, high-quality signal generator offers an output amplitude range of 25 mV to 5 V. This 46-dB adjustable range exceeds the capabilities of most commercially available VGAs. The AD8330 was the first VGA to achieve a 50-dB range, but the bar was raised further with the AD8338, a new low-power VGA with an 80-dB programmable range. Under ideal conditions, the output amplitude of a classic signal generator could then range from 0.5 mV to 5 V, without the use of relays or switched networks. The full range would be continuously adjustable, free of the discontinuities associated with switches and relays. In addition, eliminating the relays increases instrument lifetime and system reliability.

Modern DACs and DDS devices often have differential outputs, requiring designers to use a transformer, lose half of the signal with a single-ended connection, or add a differential-to-single-ended converter. The AD8338 provides a natural fit, having a fully differential interface, as shown in Figure 3. For a sine-wave application, the DAC would be replaced with a DDS.

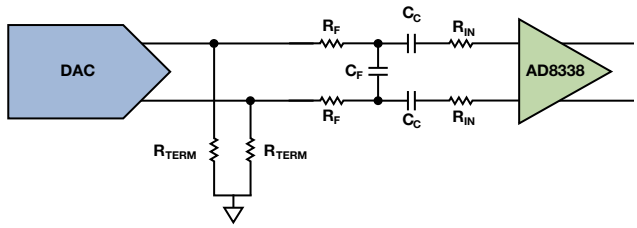


***Figure 3.** Example of a network that interfaces a DAC to the AD8338.*

A major feature of the AD8338 is the flexible input stage. As an input-VGA, it manipulates the input currents using the "H-amp" topology invented by ADI Fellow Barrie Gilbert. This design uses feedback to balance the input currents while maintaining the internal nodes at 1.5 V. Under normal conditions, using the 500-Ω input resistors, the maximum 1.5-V input signal produces a 3-mA current. If the input amplitude were larger, say 15 V, a larger resistor would be connected to the "direct" input pins. This resistor is sized such that the same 3-mA current is obtained:

$$\frac{15.00\ \text{V}}{3\ \text{mA}} = 5\ \text{k}\Omega \qquad (1)$$

The single-ended 15-V signal would output 1.141 V differentially. In this case, at minimum gain, the AD8338 would provide 28.4-dB attenuation, so the maximum possible gain is +51.6 dB. As a low-power part, it has a 1.5-V typical output swing into a 1-kΩ load.

The power of the input VGA is that its total gain range can be located around different set points. First, determine the output level required to produce the signal generator's maximum output. Many commercial generators only provide a 250 mW rms (+24 dBm) maximum output power into a 50-Ω load (sine wave). This is not enough to cover applications that need more output power, such as testing high-output HF amplifiers or ultrasound pulse generation, for example.

Advances in current-feedback amplifier (CFA) technology mean that this no longer has to be a problem. The ADA4870 CFA can drive 1 A at 17 V on ±20-V supplies. For sine waves, it can output frequencies up to 23 MHz at full load, making it an ideal front-end driver for the next generation of general-purpose arbitrary waveform/signal generators.

For 50-Ω systems that are sensitive to reflections, the ADA4870 requires some passive devices to match the source impedance to the 50-Ω load: a resistive pad and a 1.5:1 RF autotransformer. Allowing 1 V of margin, 8-W peak power is obtained when the effective amplifier loading is 16 Ω. Alternatively, if reflections are not a concern, the resistive pad can be eliminated, and the autotransformer can be replaced with one with a 0.77:1 ratio. Without the resistive padding the output power increases to 16-W peak (28.3-V amplitude).

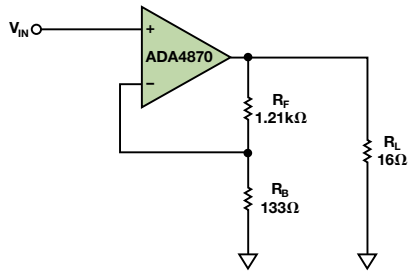


***Figure 4.** The basic connection for the ADA4870 for driving 16 Ω, gain = 10.*

To optimize the output signal swing, the ADA4870 is configured for a gain of 10, so the required input amplitude is 1.6 V. The ADA4870 has a single-ended input, and the AD8338 has a differential output, so an AD8130 differential-receive amplifier, with its 270-MHz gain-bandwidth product and 1090-V/µs slew rate, provides both the differential-to-single-ended conversion and the required gain. The AD8338's output is constrained to ±1.0 V, so the AD8130 must provide an intermediate gain of 1.6 V/V. When combined, the three devices form a complete signal generator output stage.

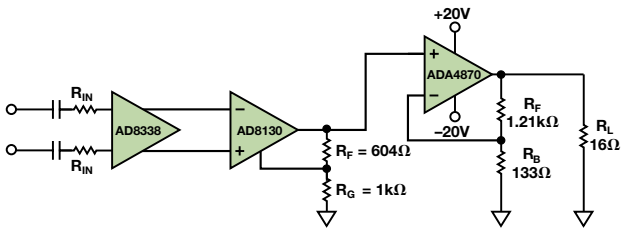


***Figure 5.** Signal generator output stage.*

Two final steps are required to complete the design: configuring the input network for maximum input signal plus antialiasing, and designing the output network for an impedance transformation.

The AD8338 Input Network

For this design, the differential output amplitude will be ±1.0 V. With factory default settings, the internal 500 Ω resistors, and maximum gain, the input amplitude would have to be 100 µV. Adding resistors to the direct-input pins allows the designer to adjust this requirement. The gain range, as determined by the input resistors, is:

$$Gain\ (dB) = 80 \times (V_{GAIN} - 0.1) + 20 \log\left(\frac{19000}{R_P + R_N}\right) - 34 \quad (2)$$

Using 40.2-kΩ resistors at each input provides a good balance between noise power and input attenuation. With V_{GAIN} = 1.1 V (maximum gain), the gain is:

$$Gain\ (dB) = 80 + 20 \log\left(\frac{19000}{80400}\right) - 34 = 33.5\ \text{dB} \quad (3)$$

In this case, the differential input only needs to be 21 mV.

When V_{GAIN} = 0.1 V, the gain is:

$$Gain\ (dB) = 0 - 12.5 - 34 = -46.5\ \text{dB} \quad (4)$$

For the same 21 mV input, the output will be about 100 µV.

Factoring in the total gain of the AD8130 and the ADA4870, which amounts to 24.1 dB, the output amplitude of the ADA4870 will range from 1.6 mV to 16 V. After the resistive pad and autotransformer, the voltage on the output will range from 2 mV to 20 V.

Interfacing the AD8338 to a device such as a DDS requires accounting for the antialiasing and input attenuation. For example, the differential output AD9834C DDS requires 200-Ω resistors to ground for proper swing. Each output produces only half of the sine-wave signal, as shown in Figure 6.

Each output peaks at 0.6 V, making an effective input of ±0.6 V. The required attenuation is 26 dB. With 200-Ω resistors, the attenuation is easily achieved by creating a simple resistive divider. Since the signal does not swing uniformly, the peak of the signal should reach the expected attenuated value.

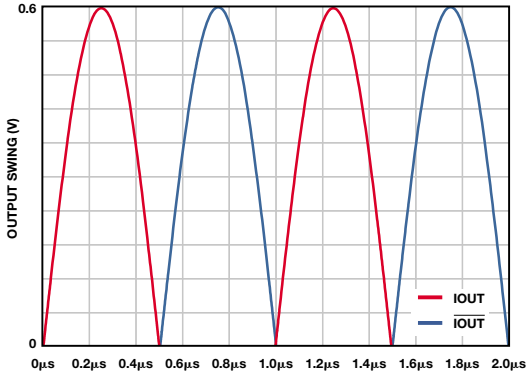


***Figure 6.** Output swing of the 9834C IOUT and $\overline{IOUT}$. Aliasing artifacts are not shown.*

$$0.021 = 0.6\left(\frac{R_{BOT}}{R_{TOP} + R_{BOT}}\right);\ R_{TOP} = 193\ \Omega \text{ and } R_{BOT} = 7\ \Omega \quad (5)$$

Using standard 6.98-Ω and 191-Ω resistor values will contribute 0.7% error.

Finally, some antialiasing will be necessary. With a 75-MSPS sample rate, the Nyquist-rate output would be 37.5 MHz, which exceeds the 20-MHz bandwidth of this design. Setting the antialiasing pole at 20 MHz, the required capacitor is:

$$C_{FILT} = \frac{1/R_{BOT}}{2\pi \times f} = \frac{0.142}{2\pi \times 20 \times 10^6} = 1100\ \text{pF} \quad (6)$$

This is a standard value, so the complete input network is as shown in Figure 7:

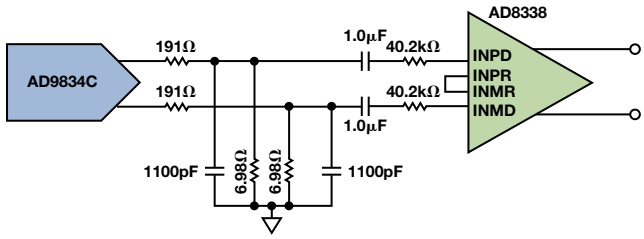


Figure 7. DDS + attenuation and filter network + AD8338.

This stage was constructed and measured. The overall variation was within ±0.6 dB, as shown in Figure 8.

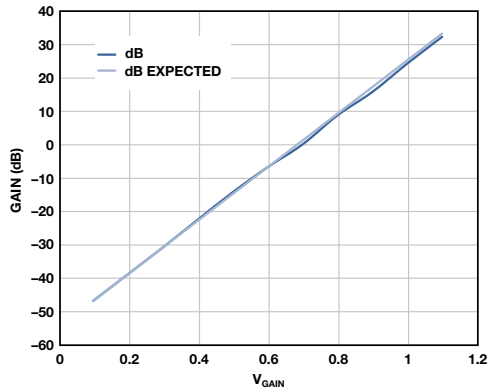


Figure 8. Calculated vs. measured gain for AD8338 configuration.

ADA4870 Output Stage

With the single-ended output provided by the AD8130, the ADA4870 will perform the final gain of 10. Two resistors are needed to set this gain, and the stage is stable without external compensation. The only work that will be left is shaping the output network to conform to the application's need. There are three general implementations:

1. Direct output from amplifier to 50 Ω
2. Padded, autotransformer output to 50 Ω
3. Unpadded, autotransformer output to 50 Ω

For a direct output, the amplifier output is tied directly to the output connector, without any network to transform the source, as shown in Figure 9. Perfect for the true-dc-connected source, this method doesn't use the device's full potential, yet still does better than the typical signal generator's 10-V output amplitude. In this case, the maximum peak power will be 5.12 W.

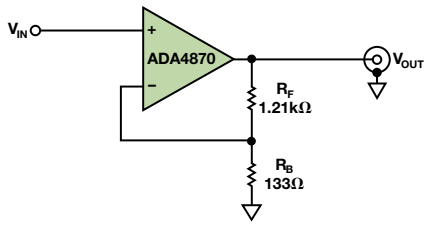


Figure 9. Connections for direct output drive.

With the padded design, the 16-Ω load is split between an 8-Ω series pad, and the filtered 1.5:1 autotransformer, as shown in Figure 10. In this mode, the low impedance of the design enables the designer to use 6.25× smaller values for the inductors than those used for 50-Ω designs. The low-pass filter and autotransformer convert the effective 8-Ω source impedance to a well matched 50 Ω. While the total peak output power will be 8 W, this design method is best suited to applications that need a matched 50-Ω source where reflections might be of concern, such as when long transmission lines are involved.

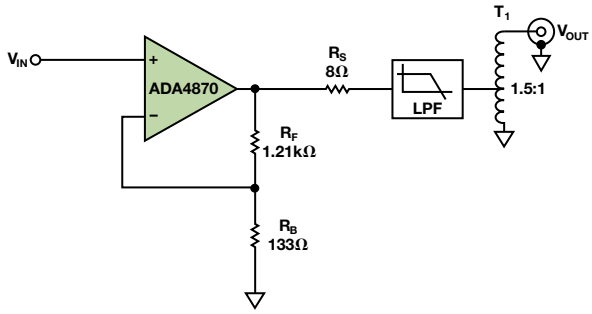


Figure 10. ADA4870 connections for padded-output design. Input impedance appears as 50 Ω to any reflections within the band of interest.

The last option, and probably the most useful for signal generators, skips the use of the 8-Ω pad, and permits twice the output power. An LC ladder filter is still recommended, as shown in Figure 11, but the ladder values will be 3.125× smaller than values which would be used for a 50-Ω system (design to 16-Ω nominal impedance). In this case, the autotransformer will use a 0.77:1 ratio. In this mode, the peak sine-wave output amplitude will be 28.3 V, and the ADA4870 will drive approximately 16 W into a 50-Ω load (8-W rms or 39 dBm).

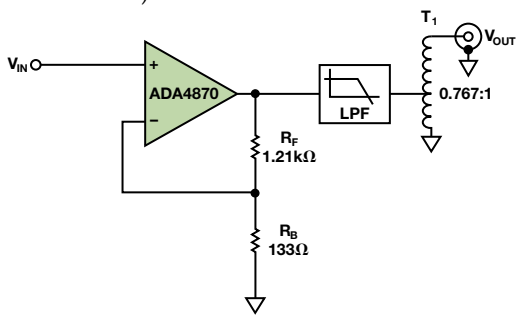


Figure 11. Connections for optimal power output for driving 50-Ω loads.

The Total Solution

In the real world, simulations and equations are meaningless if they don't match the real world. It is thus important to build a complete system and measure its performance against expectations. Figure 12 shows the schematic of an actual padded-output design.

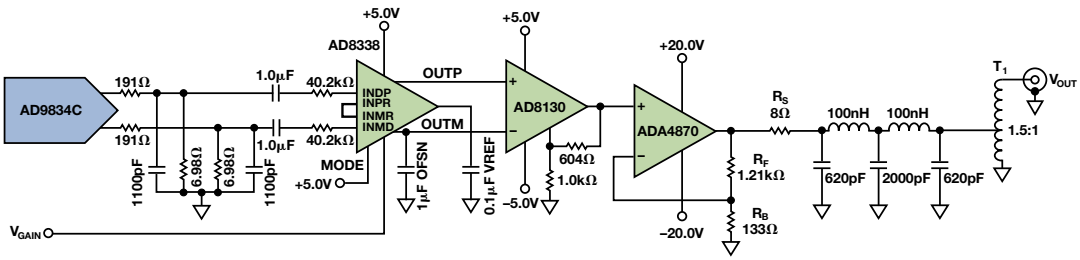


Figure 12. Simplified, complete schematic.

Figure 13 shows measured results without a filter. The system has a ±1-dB gain conformance worst case up to the 2.75 W rms (5.5-W peak) output power (P1dB compression point at 34 dBm). Most notably, the total gain range exceeded 62 dB, offering 16 dB more range than many standard generators.

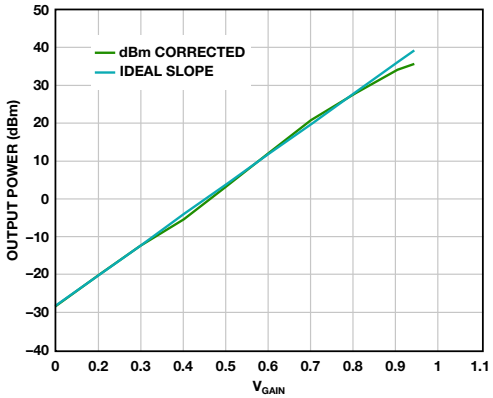


Figure 13. *Padded, unfiltered, output power results. Without the filter, system exhibits a P1dB point at 36 dBm. F_{TEST} = 14.0956 MHz.*

The gain range can be improved with better filtering at the DDS output, as well as by reducing system noise. Figure 14 shows the same measurements with a filter. The filtered output does not suffer the same P1dB level, producing a full +36 dBm output into a 50-Ω load. The overall gain linearity is better (≤0.65 dB), with errors only present around midscale.

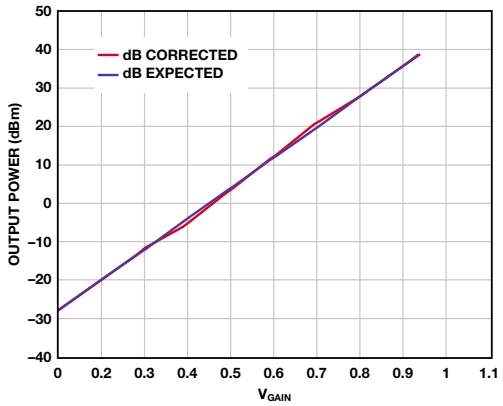


Figure 14. *Measured output with a 5th order low-pass filter (f_c = 20 MHz). F_{TEST} = 14.0956 MHz.*

If even higher output powers were required for particular modes of operation, multiple output amplifiers could be used to drive a specialty transformer for the given application. Alternatively, the design methods described here could be applied to lower supply systems, as long as the methods described here are used within the constraints of the alternate designs.

Note that the upper end of the measurement stopped at V_{GAIN} = 0.9375 V as a result of accumulated input attenuation and gain errors. This can be resolved by trimming the initial attenuation network to account for the total system errors. Once corrected, the total system gain range increased to 74 dB.

Conclusion

By pairing a high-performance VGA and a high-performance, high-output CFA, a simple front end for a new generation of signal generator can be constructed. Total PC board area and cost are reduced due to the high integration of these parts.

For additional versatility, a log amplifier, such as the AD8310, can be used in a closed-loop feedback system. With this addition, working in conjunction with a DDS like the AD9834C, the designer can incorporate various forms of envelope modulation, such as frequency-shift keying (FSK), on-off keying (OOK), and phase-shift keying (PSK), as an intrinsic feature, offering countless options through the novel use of two fundamental blocks.

References

Current Feedback Amplifiers.

Log Amps/Detectors.

Variable Gain Amplifiers (VGA).

MT-034 Tutorial. Current Feedback (CFB) Op Amps.

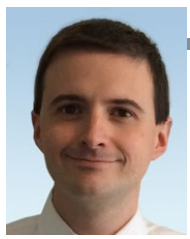
MT-057 Tutorial. High Speed Current Feedback Op Amps.

MT-060 Tutorial. Choosing Between Voltage Feedback and Current Feedback Op Amps.

MT-072 Tutorial. Precision Variable Gain Amplifiers.

MT-073 Tutorial. High Speed Variable Gain Amplifiers.

David Hunter



David Hunter [david.hunter@analog.com] is an applications engineer in the Linear Products Group at ADI's Wilmington campus. He joined ADI in 2006 as a field applications engineer working out of the Northwest Labs Design Center, serving the test and measurement field, as well as industrial customers. David graduated from Portland State University with a B.S.E.E. in 2007, specializing in RF engineering. Prior to graduating, he published and coauthored papers on self-healing hardware systems and evolvable hardware. He is also an active amateur radio operator using call sign KE7BJB.

ADC Modeling Tools Speed Up Evaluation

By Umesh Jayamohan

Introduction

Consumer demand for faster, smarter, better products is pushing innovation to previously unseen levels. System designers are thus faced with a common dilemma: design a new product on a known platform, making only incremental changes; or use a brand-new platform with the most advanced products and capabilities. The former may be quick and low risk, but offers a low reward; whereas the latter offers better versatility, functionality, and value, but with higher risk.

Now, a new suite of simulation tools enables quick prototyping in software, minimizing development risk and providing designers with confidence that their new products will work as expected. The software offers insight into the capabilities of individual products such as analog-to-digital converters, clock ICs, and amplifiers, and makes it possible to combine devices (ADC and clock, for example) without having to obtain actual components. The decision to purchase hardware can be made after the software evaluation is complete, saving time and money.

This article demonstrates the versatility of ADIsimADC™, ADIsimCLK,™ and the VisualAnalog® software suite to predict an ADC's performance when combined with a sampling clock. The example uses the AD9467 16-bit, 250-MSPS analog-to-digital converter and the AD9523-1 low-jitter clock generator. The first section describes the software evaluation, simulating the ADC's performance over frequency and showing how to connect the devices in software. The second section details a real-world hardware setup, using the evaluation boards and SPIController software. The example clocks the AD9467 at 245.76 MSPS. The AD9523-1 evaluation board uses an interactive GUI to configure the clock outputs.

Cosimulation Using ADIsimADC and ADIsimCLK

First, download and install VisualAnalog and the AD9523-1 evaluation software. ADIsimADC is packaged along with VisualAnalog. Upon starting VisualAnalog, a pop-up window will ask the user to choose a Canvas, as shown in Figure 1.

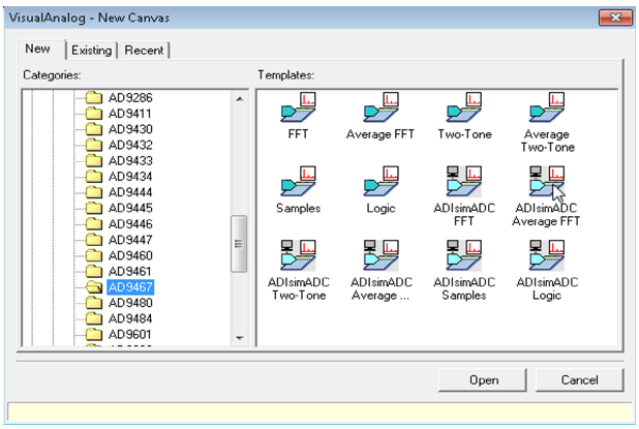


Figure 1. *VisualAnalog New Canvas window.*

The ADIsimADC model for the AD9467 is available under the **ADC→Single→AD9467** menu selection. Figure 2 shows the ADIsimADC Average FFT Canvas.

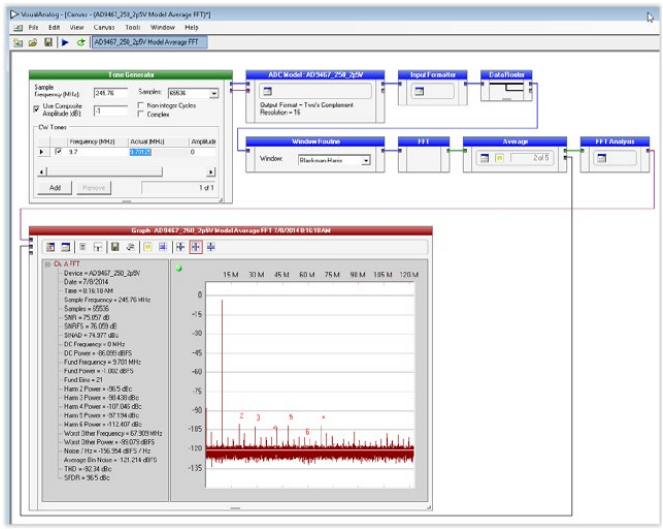


Figure 2. *ADIsimADC Canvas showing AD9467 with single-tone FFT at 9.7 MHz.*

Setting up ADIsimADC to Predict ADC Behavior

Input a frequency in the **Tone Generator** block and hit **Tab**. ADIsimADC automatically converts this frequency into a coherent frequency based on the sample rate and the sample size. Figure 3 shows the FFT of a single-tone input at 9.7 MHz using default settings.

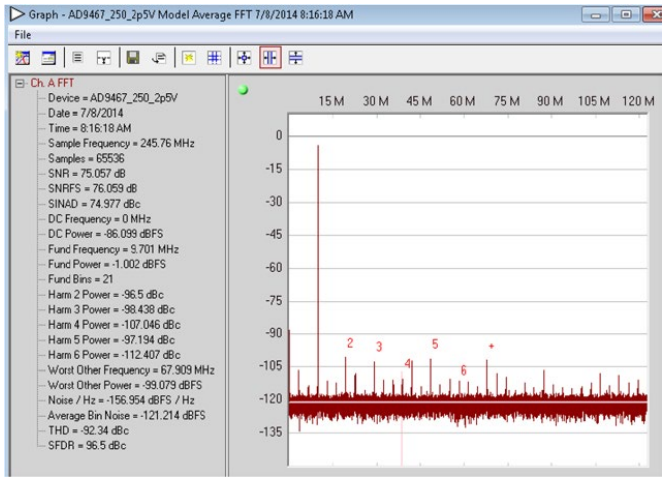


Figure 3. *ADIsimADC single-tone FFT at 9.7 MHz.*

Setting up ADIsimCLK to Predict AD9523-1 Behavior

Next, download and install the ADIsimCLK software. Once installed, open the program and select **File→New**. A window appears with a selection of devices, as shown in Figure 4.

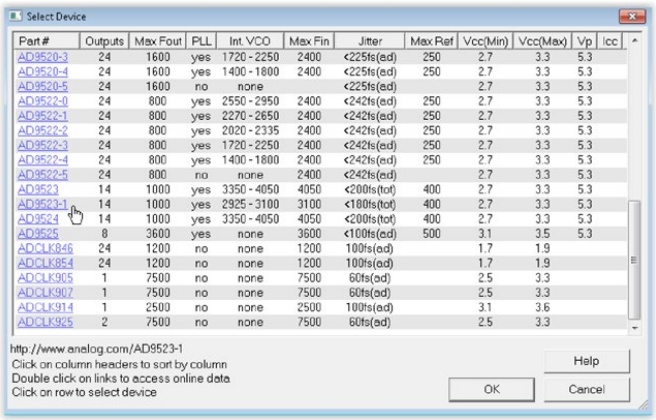


Figure 4. ADIsimCLK device selection.

Follow the setup method that best resembles the actual intended system implementation. In this example, an external 30.72-MHz clock provides the reference to the first PLL. A Crystek CVHD-950 is used as the VCXO for the first loop of the dual-loop PLL. The internal VCO frequency is set to 2949.12 MHz and internally divided by 3. A divide-by-4 on OUT7 provides a 245.76-MHz clock. This setup is shown in Figure 5.

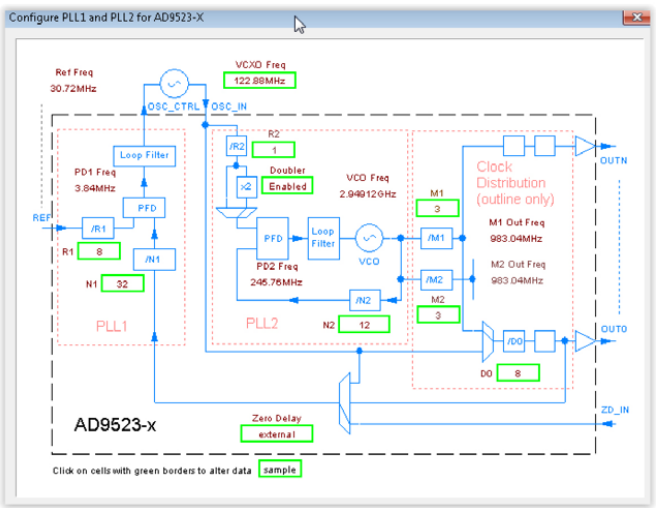


Figure 5. AD9523-1 setup in ADIsimCLK.

ADIsimCLK also generates a report on the clock outputs, including output phase noise and jitter at various integration ranges. These reports are available on the tabs corresponding to the various outputs. In this setup, OUT7 is being used to clock the AD9467 evaluation board. The report page is shown in Figure 6. The key specification, **Broadband Jitter**, is highlighted.

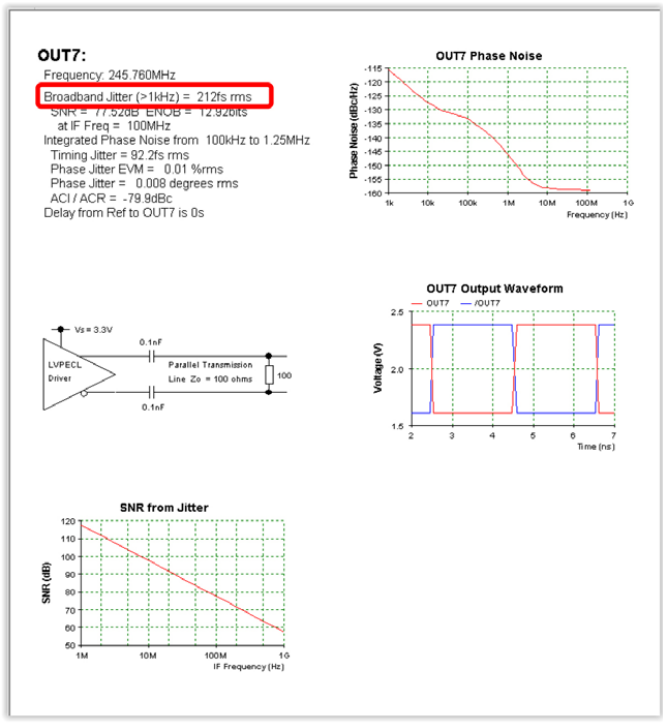


Figure 6. OUT7 report in ADIsimCLK.

Simulating the AD9467 with the AD9523-1

ADIsimADC can predict the performance of the AD9467 when clocked with the AD9523-1. The broadband jitter specification from the ADIsimCLK report can be passed to the ADIsimADC canvas. In the FFT canvas, the **ADC Model** block enables the user to update the total jitter specification, as shown in Figure 7.

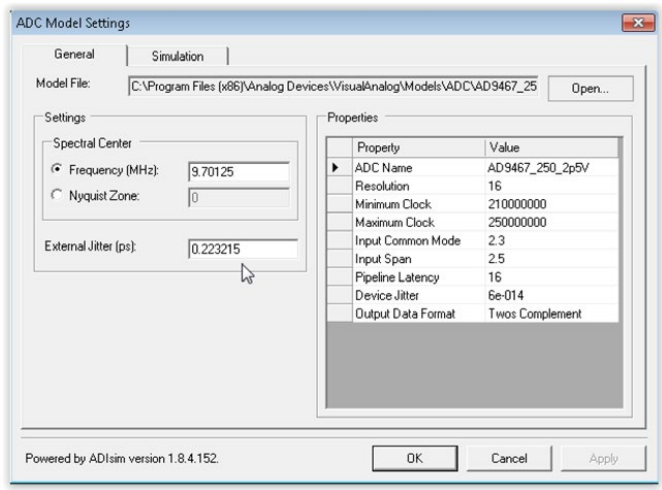


Figure 7. Updating the jitter in the ADIsimADC model.

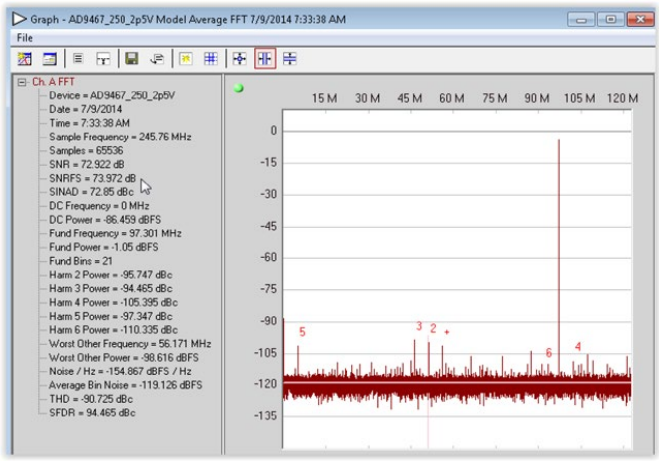


Figure 8. *Single-tone FFT at 97 MHz input with updated jitter specification in ADIsimADC.*

The total jitter can be calculated as the root-sum-square (rss) of the individual jitter components. In this case, the aperture jitter is 60 fs and the broadband jitter is 215 fs. The rss jitter passed to ADIsimADC is 223.2 fs, producing the 97-MHz, single-tone FFT shown in Figure 8. Using the updated jitter, ADIsimADC can predict the expected performance at any input frequency.

A Short Note on Jitter

An ADC must take regular time samples of an analog signal. A stable sampling clock is required, as any nonideal clock source will produce some phase noise. Jitter is the integration of the phase noise over the period between two specified frequency offsets from the sample clock carrier. For ADCs, wideband noise is generally considered to be most important. ADIsimCLK calculates broadband jitter, which integrates the phase noise above a 1-kHz offset. This broadband jitter is passed to the ADIsimADC model to understand the effect of jitter on the ADC performance. For more detailed information on how sample clock jitter affects ADC performance, please refer to AN-756 Application Note: *Sampled Systems and the Effects of Clock Phase Noise and Jitter*.

Measured Performance

The ADIsimADC prediction was tested using the AD9467 evaluation board and the AD9523-1 evaluation board. The AD9523-1 was configured to produce a 245.76-MHz LVPECL clock on OUT7. This output was coupled to the AD9467 evaluation board, which was modified to accept a differential clock input on J200 and J201. This setup is shown in Figure 9.

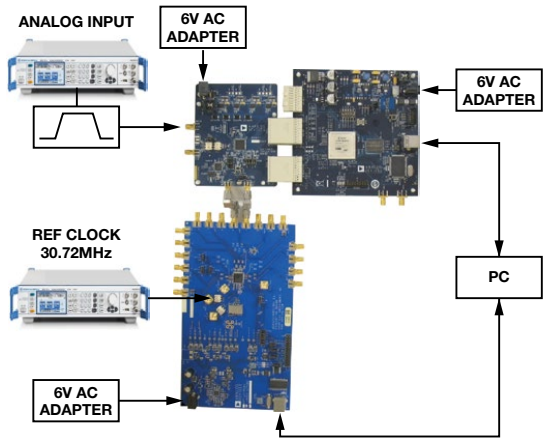


Figure 9. *Hardware setup showing the AD9523-1 and AD9467 evaluation boards.*

The setup gathered data using analog input frequencies from 2 MHz to 400 MHz. Single-tone FFTs were captured using VisualAnalog, and data was compiled and plotted against the ADIsimADC prediction. Figure 10 shows the SNR vs. frequency. Note how well the simulation matches the actual measurements.

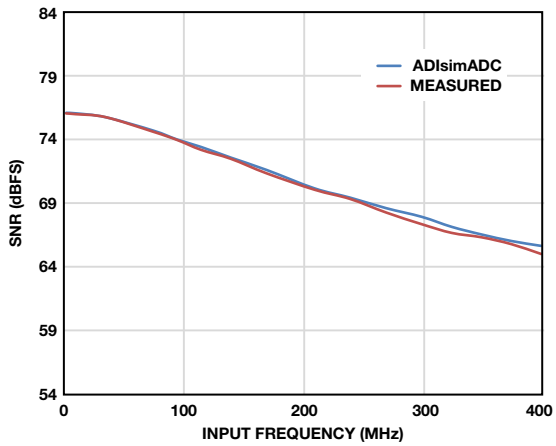


Figure 10. *SNR vs. analog input frequency comparing ADIsimADC and actual measured data.*

Figure 11 shows the SFDR data. These numbers do not completely agree, but the overall trend between simulated and measured data across frequency matches well. SFDR is highly dependent on PC board layout, components, and clock amplitude, which can explain the discrepancy.

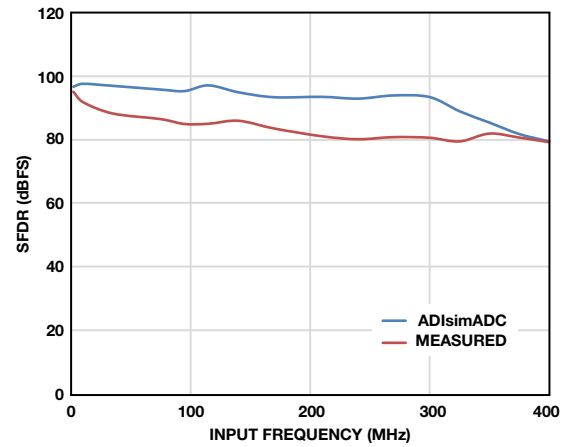


Figure 11. *SFDR vs. analog input frequency comparing ADIsimADC and actual measured data.*

A better measure of distortion would compare the simulated and measured data for second and third harmonic distortion, as shown in Figure 12 and Figure 13. The simulated and measured HD2 performance matches very well, proving that the differential signal going into the ADC in the evaluation board is well balanced in terms of amplitude and phase, and that the layout of the evaluation board is good enough to not significantly affect the differential signal balance.

On the other hand, predicting HD3 performance over frequency can be tricky. The ADIsimADC model is developed by looking at the ADC performance and DNL data during characterization. The algorithm uses interpolation and extrapolation techniques to predict dynamic range at certain frequencies, but cannot accurately predict the HD3 performance at all points.

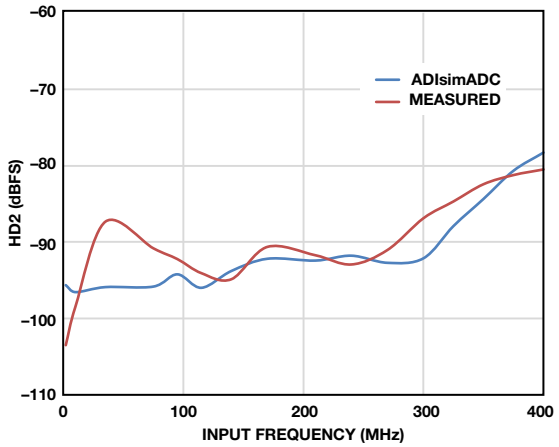


Figure 12. *HD2 vs. analog input frequency comparing ADIsimADC and actual measured data.*

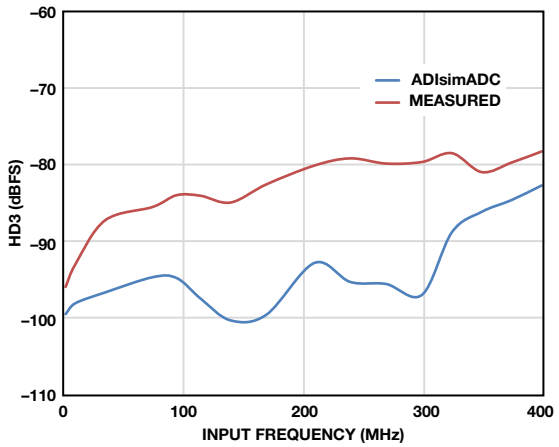


Figure 13. *HD3 vs. analog input frequency comparing ADIsimADC and actual measured data.*

The actual HD3 performance is heavily dependent on real-world factors such as supply voltage, component selection, ADC input buffer, and clock signal quality.

The HD3 prediction may not always be spot on, but the overall trend over frequency provides good agreement between the simulated and measured data.

In many system designs, the primary performance metric is SNR. SFDR and dynamic range are dependent on a lot of other factors. The SNR numbers between the simulation and the measured data match very well, which gives system designers confidence in the choice of ADC and clock.

Conclusion

The need for shorter design cycles puts enormous pressure on system designers to evaluate new products for their designs. Hardware evaluation is almost always a necessity, but choosing the wrong hardware combination could end up costing money and time. Software evaluation can act as a quick and easy first look at ADC products. ADIsimADC and ADIsimCLK offer a simple and effective way for system designers to select an ADC and clocking IC. These software tools allow system designers to mix and match various ADCs and clocking ICs, allowing them to develop enough confidence in the selected components to perform a hardware evaluation.

Acknowledgements

Thanks to Jillian Walsh for all the hard work in the lab collecting the data for this article and thanks to Kyle Slightom for helping with the AD9523-1 evaluation board and software setup.

References

AN-905 Application Note. *VisualAnalog™ Converter Evaluation Tool Version 1.0 User Manual.*

Analog Devices High Speed Converter Division. AN-878 Application Note. *High Speed ADC SPI Control Software.* Analog Devices, Inc., 2007.

Brannon, Brad. AN-756 Application Note. *Sampled Systems and the Effects of Clock Phase Noise and Jitter.* Analog Devices, Inc., 2004.

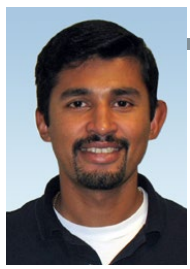
Brannon, Brad and Tom MacLeod. AN-737 Application Note. *How ADIsimADC Models an ADC.* Analog Devices, Inc., 2009.

MT-003 Tutorial. *Understand SINAD, ENOB, SNR, THD, THD + N, and SFDR So You Don't Get Lost in the Noise Floor.*

Reeder, Rob. "Test High-Speed ADCs for Analog-Input Phase Imbalance." *Test & Measurement World,* 2011.

Slightom, Kyle. "Dual-Loop Clock Generator Cleans Jitter, Provides Multiple High-Frequency Outputs." *Analog Dialogue* Volume 48, Number 1, 2014.

Umesh Jayamohan [umesh.jayamohan@analog.com] is an applications engineer in the High Speed Converter Group at Analog Devices in Greensboro, NC. Umesh received a B.S.E.E. from University of Kerala, India, in 1998 and an M.S.E.E. from Arizona State University in 2002, and has over seven years of experience as a design and applications engineer.



Umesh Jayamohan

Also by this Author:

Understanding How Amplifier Noise Contributes to Total Noise in ADC Signal Chains

Volume 47, Number 1

Understand Low-Dropout Regulator (LDO) Concepts to Achieve Optimal Designs

By Glenn Morita

Low-dropout regulators (LDOs) are deceptively simple devices that provide critical functions such as isolating a load from a dirty source or creating a low-noise source to power sensitive circuitry.

This brief tutorial introduces some common terms used with LDOs, explaining fundamental concepts such as dropout voltage, headroom voltage, quiescent current, ground current, shutdown current, efficiency, dc line-and-load regulation, transient line-and-load response, power-supply rejection ratio (PSRR), output noise, and accuracy, using examples and plots to make them easy to understand.

LDOs are often selected late in the design process with little analysis. The concepts presented here will enable designers to select the best LDO based on system requirements.

Dropout Voltage

Dropout voltage ($V_{DROPOUT}$) is the input-to-output voltage difference at which the LDO is no longer able to regulate against further decreases in the input voltage. In the dropout region, the pass element acts like a resistor with a value equal to the drain-to-source on resistance (RDS_{ON}). The dropout voltage, expressed in terms of RDS_{ON} and load current, is

$$V_{DROPOUT} = I_{LOAD} \times RDS_{ON}$$

RDS_{ON} includes resistance from the pass element, on-chip interconnects, leads, and bond wires, and can be estimated by the LDO's dropout voltage. For example, the ADP151 in the WLCSP has a worst-case dropout voltage of 200 mV with a 200-mA load, so the RDS_{ON} is about 1.0 Ω. Figure 1 shows a simplified schematic of an LDO. In dropout, the variable resistance is close to zero. The LDO cannot regulate the output voltage, so other parameters such as line-and-load regulation, accuracy, PSRR, and noise are meaningless.

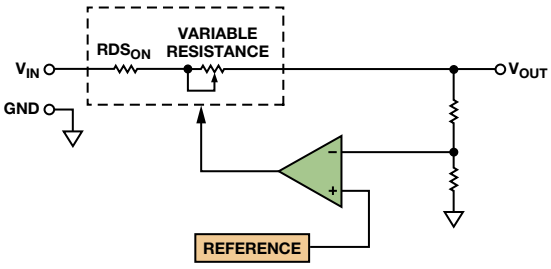


Figure 1. Simplified schematic of an LDO.

Figure 2 shows the output voltage vs. input voltage of the 3.0-V ADM7172 LDO. The dropout voltage is typically 172 mV at 2 A, so RDS_{ON} is about 86 mΩ. The dropout region extends from about 3.172-V input voltage down to 2.3 V. Below 2.3 V, the device is nonfunctional. At smaller load currents, the dropout voltage is proportionately lower: at 1 A, the dropout voltage is 86 mV. A low dropout voltage maximizes the regulator's efficiency.

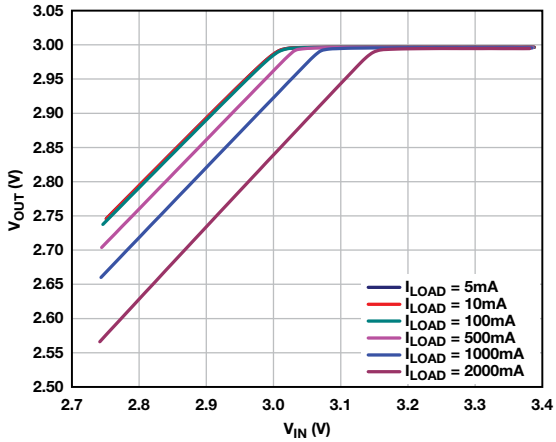


Figure 2. Dropout region of the 3.0-V ADM7172 LDO.

Headroom Voltage

Headroom voltage is the input-to-output voltage difference required for an LDO to meet its specifications. The data sheet usually shows the headroom voltage as the condition at which the other parameters are specified. The headroom voltage is typically around 400 mV to 500 mV, but some LDOs require as much as 1.5 V. Headroom voltage should not be confused with dropout voltage, as they are the same only when the LDO is in dropout.

Quiescent and Ground Current

Quiescent current (I_Q) is the current required to power the LDO's internal circuitry when the external load current is zero. It includes the operating currents of the band-gap reference, error amplifier, output voltage divider, and overcurrent and overtemperature sensing circuits. The amount of quiescent current is determined by the topology, input voltage, and temperature.

$$I_Q = I_{IN} \text{ @ no load}$$

The quiescent current of the ADP160 LDO is nearly constant as the input voltage varies between 2 V and 5.5 V, as shown in Figure 3.

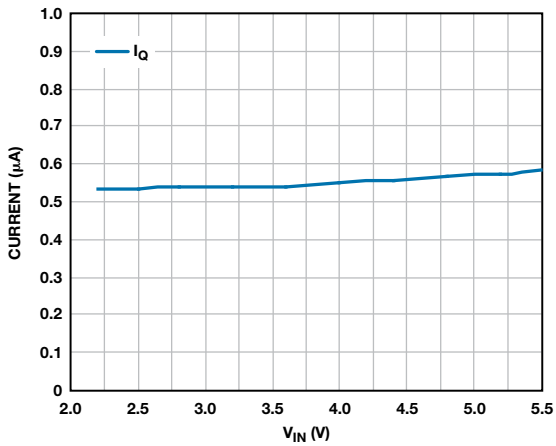


Figure 3. Quiescent current vs. input voltage of the ADP160 LDO.

Ground current (I_{GND}) is the difference between the input and output currents, and necessarily includes the quiescent current. A low ground current maximizes the LDO efficiency.

$$I_{GND} = I_{IN} - I_{OUT}$$

Figure 4 shows the ground current variation vs. load current for the ADP160 LDO.

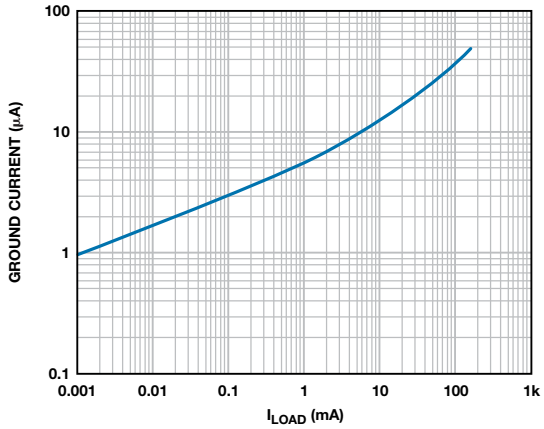


Figure 4. Ground current vs. load current of the ADP160 LDO.

For high-performance CMOS LDOs, the ground current is typically much less than 1% of the load current. Ground current increases with load current because the gate drive to the PMOS pass element must increase to compensate for the voltage drop caused by its R_{ON}. In the dropout region, the ground current can also increase as the driver stage starts to saturate. CMOS LDOs are essential in applications where low power consumption or small bias currents are critical.

Shutdown Current

Shutdown current is the input current drawn by the LDO when the output is disabled. The reference and error amplifier are not powered in shutdown mode. Higher leakage currents cause the shutdown current to increase with temperature, as shown in Figure 5.

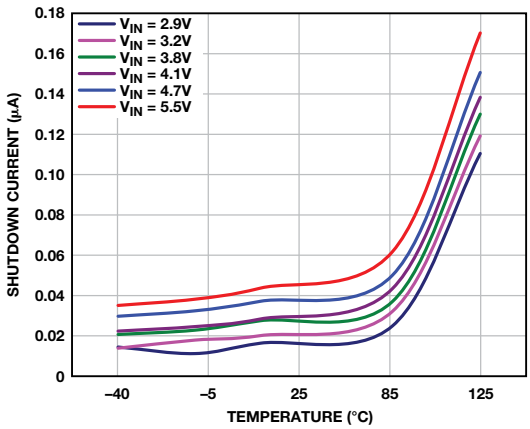


Figure 5. Shutdown current vs. temperature of the ADP160 LDO.

Efficiency

The efficiency of an LDO is determined by the ground current and input/output voltages:

$$\text{Efficiency} = I_{OUT}/(I_{OUT} + I_{GND}) \times V_{OUT}/V_{IN} \times 100\%$$

For high efficiency, the headroom voltage and ground current must be minimized. In addition, the voltage difference between input and output must be minimized. The input-to-output voltage difference is an intrinsic factor in determining the efficiency, regardless of the load conditions. For example, the efficiency of a 3.3-V LDO will never exceed 66% when powered from 5 V, but it will rise to a maximum of 91.7% when the input voltage drops to 3.6 V. The power dissipation of an LDO is $(V_{IN} - V_{OUT}) \times I_{OUT}$.

DC Load Regulation

Load regulation is a measure of the LDO's ability to maintain the specified output voltage under varying load conditions. Load regulation, shown in Figure 6, is defined as

$$\text{Load regulation} = \Delta V_{OUT}/\Delta I_{OUT}$$

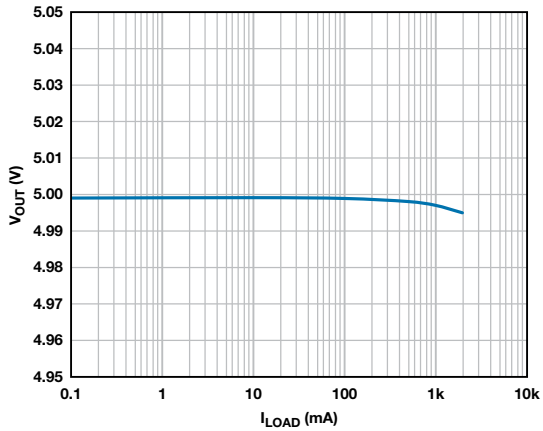


Figure 6. Output voltage vs. load current for the ADM7172 LDO.

DC Line Regulation

Line regulation is a measure of the LDO's ability to maintain the specified output voltage with varying input voltage. Line regulation is defined as

$$\text{Line regulation} = \Delta V_{OUT}/\Delta V_{IN}$$

Figure 7 shows the output voltage of the ADM7172 vs. input voltage at different load currents. The line regulation gets worse as the load current increases because the LDO's overall loop gain decreases. Also, the LDO's power dissipation increases as the input-to-output voltage differential increases. This causes the junction temperature to rise and in this case, the band-gap voltage and internal offset voltages to decrease.

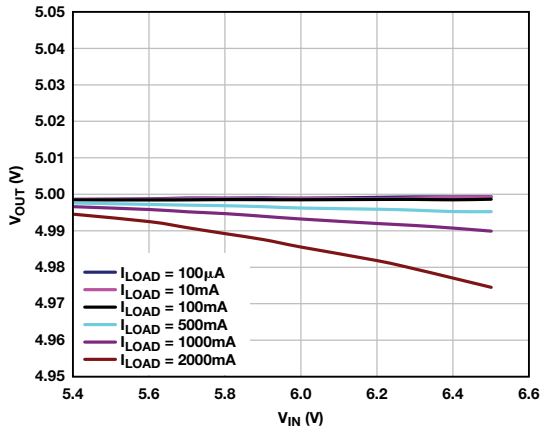


Figure 7. Output voltage vs. input voltage for the ADM7172 LDO.

DC Accuracy

The overall accuracy considers the effects of line-and-load regulation, reference voltage drift, and error amplifier voltage drift. The output voltage variation in a regulated power supply is due primarily to temperature variation of the reference voltage and the error amplifier. If discrete resistors are used to set the output voltage, the tolerance of the resistors may well be the largest contributor to overall accuracy. Line-

and-load regulation and error amplifier offsets normally account for 1% to 3% of the overall accuracy.

For example, calculate the total accuracy of a 3.3-V LDO over the 0°C to 125°C temperature span with the following operating characteristics: ±100 ppm/°C resistor temperature coefficient, ±0.25% sampling resistor tolerance, ±10 mV and ±5 mV output voltage change due to load regulation and line regulation, respectively, and 1% reference accuracy.

Error due to temperature = 125°C × ±100 ppm/°C = ±1.25%

Error due to sampling resistor = ±0.25%

Error due to load regulation =
100% × (±0.01 V/3.3 V) = ±0.303%

Error due to line regulation =
100% × (±0.005 V/3.3 V) = ±0.152%

Error due to reference = ±1%

The worst-case error assumes that all errors vary in the same direction.

Worst-case error =
±(1.25% + 0.25% + 0.303% + 0.152% + 1%) = ±2.955%

Typical error assumes random variations, so a root square sum (rss) of the errors is used.

Typical error =
$\pm\sqrt{(1.25^2 + 0.25^2 + 0.303^2 + 0.152^2 + 1^2)} = \pm 1.655\%$

The LDO will never exceed the worst-case error, while the rss error is the most likely. The error distribution will center on the rss error and spread to include the worst-case error at the tails.

Load Transient Response

The load transient response is the output voltage variation for a load current step change. It is a function of the output capacitor value, the capacitor's equivalent series resistance (ESR), the gain-bandwidth of the LDO's control loop, and the size and slew rate of the load current change.

The slew rate of the load transient can have a dramatic effect on the load transient response. If the load transient is very slow, say 100 mA/µs, the control loop of the LDO may be able to follow the change. If, however, the load transient is faster than the loop can compensate, undesirable behavior such as excessive ringing due to low phase margin may occur.

Figure 8 shows the response of the ADM7172 to a 1 mA to 1.5 A load transient with a 3.75 A/µs slew rate. The 1.5 µs recovery time to 0.1% and minimal ringing indicate good phase margin.

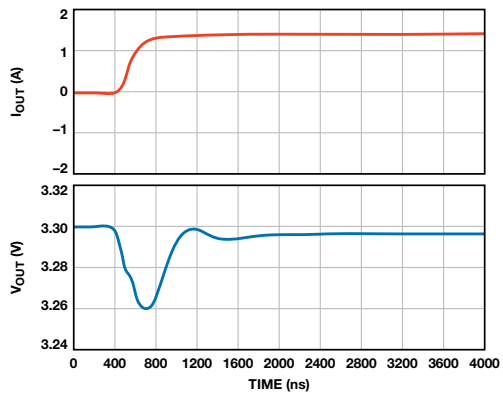


Figure 8. ADM7172 load transient response. 1 mA to 1.5 A load step in 400 ns (red). Output voltage (blue).

Line Transient Response

The line transient response is the output voltage variation for an input voltage step change. It is a function of the gain-bandwidth of the LDO's control loop, and the size and slew rate of the input voltage change.

Figure 9 shows the response of the ADM7150 to a 2-V input voltage step change. The output voltage deviation provides an indication of the loop bandwidth and the PSRR (see next section). The output voltage changes about 2 mV in response to a 2-V change in 1.5 µs, indicating a PSRR of about 60 dB at about 100 kHz.

Again, as in the case of load transients, the slew rate of the input voltage has a large effect on the apparent line transient response. A slowly changing input voltage, one well within the bandwidth of the LDO, can hide ringing or other undesirable behavior.

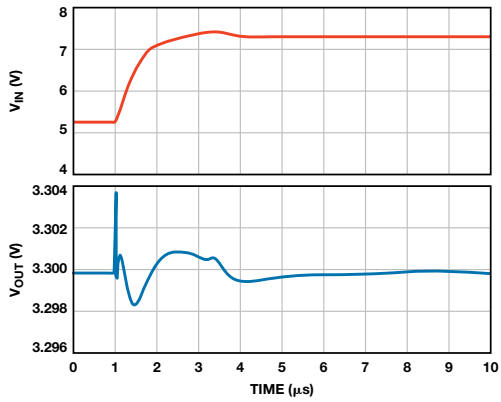


Figure 9. ADM7150 line transient response. 5 V to 7 V line step in 1.5 µs (red). Output voltage (blue).

Power-Supply Rejection

Simply put, PSRR is a measure of how well a circuit suppresses extraneous signals (noise and ripple) on the power supply input to keep them from corrupting the output. PSRR is defined as

$$PSRR = 20 \times \log(VE_{IN}/VE_{OUT})$$

where VE_{IN} and VE_{OUT} are the extraneous signals appearing at the input and output, respectively.

For circuits such as ADCs, DACs, and amplifiers, PSRR applies to the inputs that supply power to the internal circuitry. With LDOs, the input power pin supplies power to the regulated output voltage as well as to the internal circuitry. PSRR has the same relation as dc line regulation, but includes the entire frequency spectrum.

Power-supply rejection in the 100 kHz to 1 MHz range is very important, as switch-mode power supplies are frequently used in high-efficiency power systems, with LDOs cleaning up the noisy supply rails for the sensitive analog circuitry.

The LDO's control loop tends to be the dominant factor in determining power supply rejection. High value, low ESR capacitors can be beneficial, especially at frequencies beyond the gain-bandwidth of the control loop.

PSRR as a Function of Frequency

PSRR is not defined by a single value because it is frequency dependent. An LDO consists of a reference voltage, error amplifier, and a power-pass element, such as a MOSFET or bipolar transistor. The error amplifier provides dc gain to

regulate the output voltage. The ac gain of the error amplifier in large part determines the PSRR. A typical LDO can have as much as 80 dB of PSRR at 10 Hz, but the PSRR can fall to as little as 20 dB at a few tens of kilohertz.

Figure 10 shows the relationship between the error amplifier's gain bandwidth and the PSRR. This simplified example ignores parasitics from the output capacitor and the pass element. The PSRR is the reciprocal of the open-loop gain until the gain starts to roll off at 3 kHz. The PSRR then decreases by 20 dB/decade until it reaches 0 dB at 3 MHz and up.

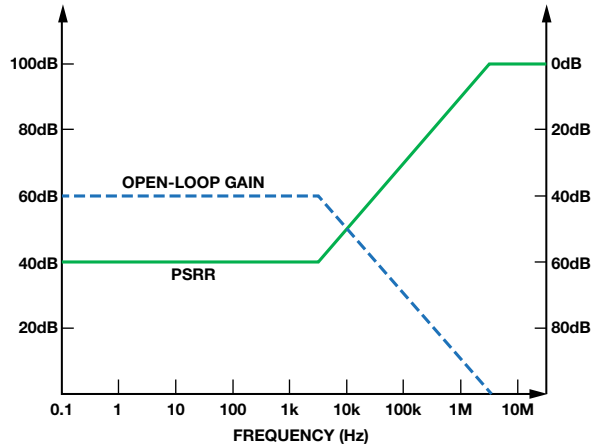


Figure 10. Simplified LDO gain vs. PSRR

Figure 11 shows three main frequency domains that characterize an LDO's PSRR: the reference PSRR region, the open-loop gain region, and the output capacitor region. The reference PSRR region is dependent on the PSRR of the reference amplifier and the LDO's open-loop gain. Ideally, the reference amplifier is fully isolated from perturbations in the power supply, but in practice, the reference need only reject power-supply noise up to a few tens of hertz because the error amplifier feedback ensures high PSRR at low frequencies.

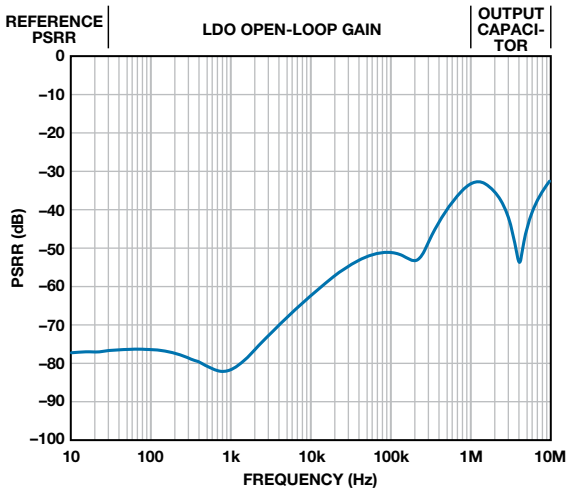


Figure 11. Typical LDO PSRR vs. frequency.

Above about 10 Hz, PSRR in the second region is dominated by the open-loop gain of the LDO. The PSRR in this region is a function of the error amplifier gain-bandwidth up to the unity gain frequency. At low frequencies, the ac gain of the error amplifier is equal to the dc gain. The gain remains constant until it reaches the 3-dB roll-off frequency. At frequencies above the 3-dB roll-off point, the ac gain of the error amplifier decreases with frequency, typically at 20 dB/decade.

Above the unity-gain frequency of the error amplifier, the feedback of the control loop has no effect on the PSRR, which is determined by the output capacitor and any parasitics between the input and output voltages. The ESR and ESL of the output capacitor, as well as the board layout, strongly affect the PSRR at these frequencies. Careful attention to layout is essential to reduce the effect of any high-frequency resonances.

PSRR as a Function of Load Current

The load current affects the gain bandwidth of the error amplifier feedback loop, so it also affects the PSRR. At light load currents, typically less than 50 mA, the output impedance of the pass element is high. The LDO's output appears to be an ideal current source due to the negative feedback of the control loop. The pole formed by the output capacitor and the pass element occurs at a relatively low frequency, so PSRR tends to increase at low frequencies. The high dc gain of the output stage at low currents also tends to increase the PSRR at frequencies well below the unity-gain point of the error amplifier.

At heavy load currents, the LDO output looks less like an ideal current source. The output impedance of the pass element decreases, lowering the gain of the output stage and reducing the PSRR between dc and the unity-gain frequency of the feedback loop. PSRR can fall dramatically as the load current rises, as shown in Figure 12. As the load increases from 400 mA to 800 mA, the PSRR of the ADM7150 decreases by 20 dB at 1 kHz.

The output stage bandwidth increases as the frequency of the output pole increases. At high frequencies, the PSSR should increase due to the increased bandwidth, but in practice, the high-frequency PSRR may not improve because of the decrease in overall loop gain. In general, PSRR at light loads is better than it is at heavy loads.

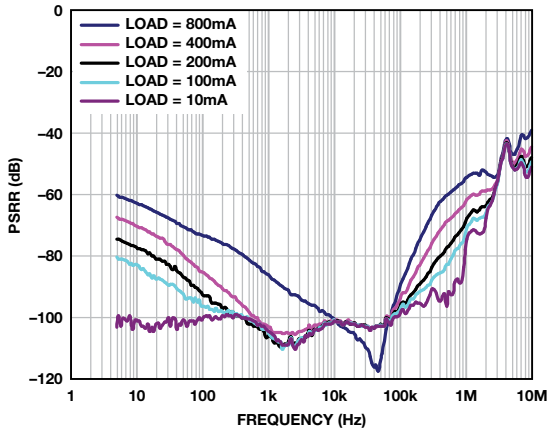


Figure 12. ADM7150 power-supply rejection vs. frequency. V_{OUT} = 5 V, V_{IN} = 6.2 V.

PSRR as a Function of LDO Headroom

PSRR is also a function of the input-to-output voltage differential, or headroom. For a fixed headroom voltage, PSRR decreases as the load current increases; this is especially apparent at heavy load currents and small

headroom voltages. Figure 13 shows the difference in PSRR vs. headroom voltage for a 5-V ADM7172 with a 2-A load.

As the load current increases, the gain of the pass element (PMOSFET for the ADM7172) decreases as it leaves saturation and goes into the triode region of operation. This causes the overall loop gain of the LDO to decrease, resulting in a lower PSRR. The smaller the headroom voltage, the more dramatic the reduction in gain. At small headroom voltages, the control loop has no gain at all, and the PSRR falls to nearly zero.

Another factor that reduces the loop gain is nonzero resistance of the pass element, RDS_{ON}. The voltage drop across RDS_{ON} due to the load current subtracts from the headroom of the active portion of the pass element. For example, with a 1-Ω pass element, a 200-mA load current reduces the headroom by 200 mV. When operating LDOs at headroom voltages of 1 V or less, this voltage drop must be accounted for when estimating the PSRR.

In dropout, the PSRR is due to the pole formed by RDS_{ON} and the output capacitor. At a very high frequency, the PSRR will be limited by the ratio of the output capacitor ESR to RDS_{ON}.

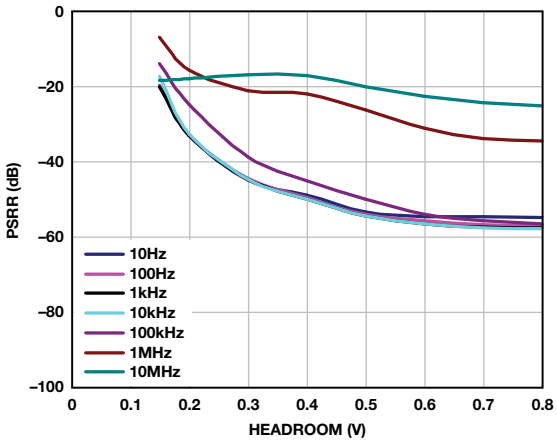


Figure 13. ADM7172 power-supply rejection vs. headroom, V_{OUT} = 5 V, 2 A load current.

Comparing LDO PSRR Specifications

When comparing LDO PSRR specifications, make sure that the measurements are made under the same test conditions. Many older LDOs specify PSRR at only 120 Hz or 1 kHz with no mention of headroom voltage or load current. At the least, PSRR in the electrical specification table should be listed for different frequencies. Ideally, typical characteristic plots of PSRR under different load and headroom voltages should be used to make meaningful comparisons.

The output capacitor also affects the LDO PSRR at high frequency. For example, a 1-µF capacitor has 10× the impedance of a 10-µF capacitor. The capacitor value is especially important at frequencies above the error amplifier's unity-gain crossover frequency, where the attenuation of power-supply noise is a function of the output capacitance. When comparing PSRR figures, the output capacitor must be the same type and value for the comparison to be valid.

Output Noise Voltage

Output noise voltage is the rms output noise voltage over a given range of frequencies (typically 10 Hz or 100 Hz to 100 kHz) under the conditions of a constant output current and a ripple-free input voltage. The major sources of output noise in LDOs are the internal reference voltage and the error amplifier. Modern LDOs operate with internal bias currents of just a few tens of nanoamps in order to achieve quiescent currents of 15 µA or less. These low bias currents require the use of bias resistors of up to a GΩ. Output noise typically ranges from 5 µV rms to 100 µV rms. Figure 14 shows the output noise vs. load current for the ADM7172.

Some LDOs, such as the ADM7172, can use an external resistor divider to set the output voltage above the initial set point, allowing a 1.2-V device to provide a 3.6-V output, for example. A noise reduction network can be added to this divider to return the output noise to a level close to that of the original fixed voltage version.

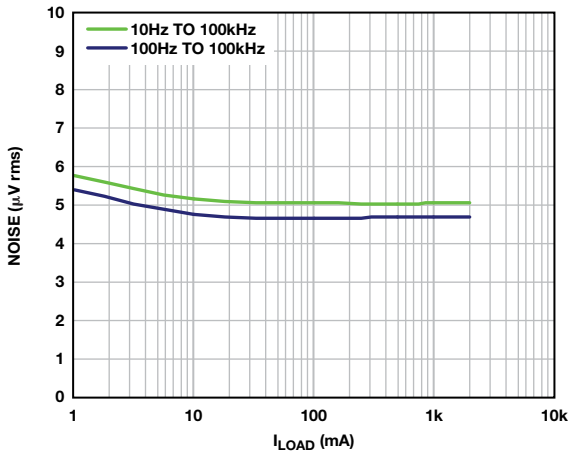


Figure 14. ADM7172 output noise vs. load current.

Another way to express the output noise of an LDO is the noise spectral density. The rms noise over a 1-Hz bandwidth at a given frequency is plotted over a wide frequency range. This information can then be used to compute the rms noise at a particular frequency for a given bandwidth. Figure 15 shows the noise spectral density from 1 Hz to 10 MHz for the ADM7172.

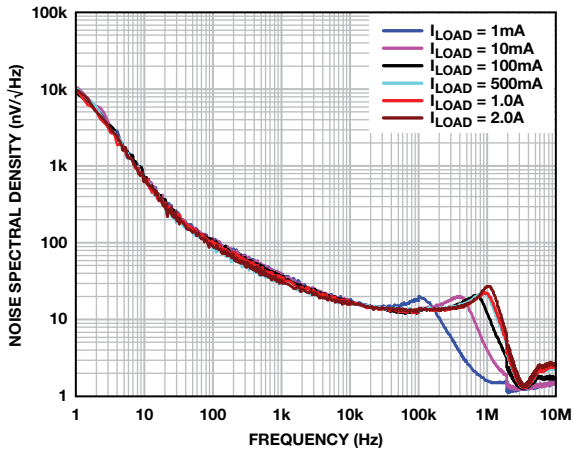


Figure 15. ADM7172 noise spectral density vs. load current.

Conclusion

LDOs are outwardly simple devices that provide a critical function. Many factors must be considered to apply them correctly and achieve optimal results. With a basic understanding of commonly used LDO terms, the design engineer can successfully navigate the data sheet to determine parameters that are most important for the design.

References

Linear Regulators

Marasco, Ken. "How to Successfully Apply Low-Dropout Regulators." *Analog Dialogue*, Volume 43, Number 3, 2009.

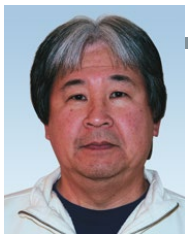
Morita, Glenn and Luca Vassalli. "LDO Operational Corners: Low Headroom and Minimum Load." *Analog Dialogue*, Volume 48, Number 3, 2014.

Morita, Glenn. "Low-Dropout Regulators—Why the Choice of Bypass Capacitor Matters." *Analog Dialogue*, Volume 45, Number 1, 2011.

Morita, Glenn. "Noise-Reduction Network for Adjustable-Output Low-Dropout Regulators." *Analog Dialogue*, Volume 48, Number 1, 2014.

Patoux, Jerome. "Low-Dropout Regulators." *Analog Dialogue*, Volume 41, Number 2, 2007.

Glenn Morita graduated from Washington State University with a B.S.E.E. in 1976. His first job out of school was at Texas Instruments, where he worked on the infrared spectrometer instrument for the Voyager space probe. Since then, Glenn has worked as a designer in the instrumentation, military and aerospace, and medical industries. In 2007, he joined ADI as an applications engineer with the Power Management Products Team in Bellevue, WA. He has over 25 years of linear and switch-mode power supply design experience at power levels ranging from microwatts to kilowatts. Glenn holds two patents for harvesting energy from body heat to power implantable cardio-defibrillators and an additional patent for extending battery life in external cardio-defibrillators. In his spare time, he enjoys collecting minerals, faceting gemstones, photography, and visiting national parks.



Glen Morita

Also by this Author:

Ask the Applications Engineer—41 LDO Operational Corners: Low Headroom and Minimum Load

Volume 48, Number 3

Notes

Analog Devices, Inc.
Worldwide Headquarters
Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA 02062-9106
U.S.A.
Tel: 781.329.4700
(800.262.5643,
U.S.A. only)
Fax: 781.461.3113

Analog Devices, Inc.
Europe Headquarters
Analog Devices, Inc.
Wilhelm-Wagenfeld-Str. 6
80807 Munich
Germany
Tel: 49.89.76903.0
Fax: 49.89.76903.157

Analog Devices, Inc.
Japan Headquarters
Analog Devices, KK
New Pier Takeshiba
South Tower Building
1-16-1 Kaigan, Minato-ku,
Tokyo, 105-6891
Japan
Tel: 813.5402.8200
Fax: 813.5402.1064

Analog Devices, Inc.
Asia Pacific Headquarters
Analog Devices
5F, Sandhill Plaza
2290 Zuchongzhi Road
Zhangjiang Hi-Tech Park
Pudong New District
Shanghai, China 201203
Tel: 86.21.2320.8000
Fax: 86.21.2320.8222

M02000484-0-3/15

analog.com/analogdialogue

ANALOG DEVICES