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Editor's Notes

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The Basics of MEMS IMU/Gyroscope Alignment

Sensor misalignment is often a key consideration for high performance motion control systems that use MEMS inertial measurement units (IMUs) in their feedback loops. Managing the impact that misalignment has on sensor accuracy can require unique packaging, special assembly processes, or even complex inertial testing in the final configuration. All of these things can have a major impact on important project management metrics such as schedule, investment, and the total cost associated with the IMU in each system. This article explores the three basic alignment concepts to understand and evaluate when architecting an IMU function for a system. (Page 3)

Multifunction: a Dilemma or Reality?

Next-generation aerospace and defense system designers are being challenged to develop advanced, highly configurable systems that combine a range of functions and requirements, integrating functionality that would have historically been implemented by separate standalone systems. This articles looks at a new generation of high performance, wideband components that are providing a solution to this challenge, supporting the high performance levels required for each system, but with a broad enough operating range to meet the multifunction challenge. (Page 9)

Low Power Synchronous Demodulator Design Considerations

"Synchronous Detectors Facilitate Precision, Low Level Measurements," published in the November 2014 issue of *Analog Dialogue*, discussed the benefits of using synchronous demodulation to measure low level signals in the presence of relatively high noise levels. This article extends the discussion by looking at some design considerations for sensor signal conditioning using synchronous demodulation in systems with strict power and cost constraints. (Page 12)

No Pain, High Gain: Building a Low Noise Instrumentation Amplifier with Nanovolt Sensitivity

Achieving nanovolt sensitivity in a circuit or system is a difficult goal that presents many design challenges. For systems that require low noise and high gain, the AD8428 in amp is a device that has the features required to implement a high performance design. This article addresses the considerations involved with low noise instrumentation design utilizing this device including noise analysis, noise vs. power trade-offs, using multiple in-amps to lower circuit noise, and SPICE simulation. (Page 16)

RF Sampling ADC Input Protection: Not Black Magic After All

The design of the input, or front end, of any high performance analog-to-digital converter (ADC), especially an RF sampling ADC, is critical to achieving the desired system-level performance in applications requiring the acquisition and digitization of signal bandwidths in the hundreds of megahertz. An input overvoltage event can damage the ADC and render the entire radio system useless, with the cost of replacing the ADC being substantial. This article details the considerations that must be given to implementing overvoltage protection in high performance ADC applications and how to achieve protection without sacrificing performance. (Page 19)

Liquid Level Sensing Using Capacitive-to-Digital Converters

Procedures such as infusions and transfusions require exact amounts of liquid to be administered and monitored, requiring an accurate, easy-to-implement method for sensing liquid level. This article provides the capacitance measurement basics and describes the 24-bit capacitive-to-digital converters and level sensing techniques that enable high performance capacitive sensing of liquid levels. (Page 24)

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Product Introductions: Volume 49, Number 2

Data sheets for all ADI products can be found by entering the part number in the search box at analog.com.

April

DAC, quad 16-bit, 2.4 GSPS TxDAC+®.....**AD9154**
LED Driver, 4-channel, high current, with adaptable power control.....**ADP8140**
Regulator, 4-channel, high current, with adaptable power control.....**ADP5054**

May

ADC, dual, 14-bit, 500 MSPS, with digital downconverters.....**AD9684**
ADC, 135 MHz BW IF diversity receiver.....**AD6679**
ADC, 8-channel, low noise, low power, 24-bit Σ-Δ.....**AD7124-8**
ADC, 32-bit, 10 kSPS Σ-Δ, with true rail-to-rail buffers.....**AD7177-2**
ADC, 16-bit, 1 MSPS/500 kSPS PulSAR.....**AD7915/AD7916**
Amplifier, dual low noise, 180 MHz, rail-to-rail input/output.....**ADA4807**
Amplifier, analog front end for photodetectors or other sensors.....**ADA4350**
Amplifier, low noise, precision, rail-to-rail output, JFET single op amp.....**ADA4610**
Amplifier, input protected, precision, low noise and bias current, single op amp.....**ADA4177**
Comparator, ultralow power voltage with reference.....**ADCMP380**
DAC, dual 16-Bit 2 GSPS TxDAC+.....**AD9152**
Downconverter, 4-channel, 24 GHz receiver.....**ADF5904**
Isolators, 3.75 kV rms, quad, digital, with input disable.....**ADuM140D/ADuM140E**
Multiplexer, 8:1 and dual 4:1 with fault protection and detection.....**ADG5348F/ADG5249F**
Multiplexer, 8:1 and dual 4:1 with fault protection and detection.....**ADG5208F/ADG5209F**
Regulator, 3-channel, integrated, low power dual buck and load switch.....**ADP5310**
Synthesizer, microwave, wideband, with integrated low noise VCO.....**ADF4355**
TEC Driver, ultracompact, 1 A.....**ADN8833**
TEC Controller, ultracompact, 1.5 A.....**ADN8834**

June

ADC, low noise, low power, multiplexed, 24-bit Σ-Δ.....**AD7172-4**
ADC, low power, low noise, precision integrated analog front end.....**AD7124-4**
Amplifier, dual-channel zero-drift op amp.....**ADA4522**
Analog Microcontroller, precision analog.....**ADuCM310**
VCO, MMIC with 10.38 GHz to 11.30 GHz and 5.19 GHz to 5.65 GHz (half frequency) range.....**HMC1164**
VCO, MMIC VCO with 8.45 GHz to 9.3 GHz and 4.225 GHz to 4.65 GHz (half frequency) range.....**HMC1160**

Analog Dialogue

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The Basics of MEMS IMU/Gyroscope Alignment

By Mark Looney

Introduction

Sensor misalignment is often a key consideration for high performance motion control systems that use MEMS inertial measurement units (IMUs) in their feedback loops. For the gyroscopes in the IMU, sensor misalignment describes the angular difference between each gyroscope's axis of rotation and the system defined *inertial reference frame*, also known as the *global frame*. Managing the impact that misalignment has on sensor accuracy can require unique packaging, special assembly processes, or even complex inertial testing in the final configuration. All of these things can have a major impact on important project management metrics such as schedule, investment, and the total cost associated with the IMU in each system. Therefore, sensor alignment is a metric that warrants consideration during early stages of the design cycle, while there is time to define the system architecture around the most efficient solution. After all, nobody wants to burn through 80% of their project schedule and budget to find out that their inexpensive sensor requires hundreds, maybe even thousands, of dollars in unexpected cost adders to meet nonnegotiable deliverables to their end users. Ouch!

There are three basic alignment concepts to understand and evaluate when architecting an IMU function for a system: error estimation, understanding misalignment impact on key system behaviors, and electronic alignment (after installation). Initial error estimation should include error contributions from both the IMU and the mechanical system that holds it in place during operation. Understanding the impact that these errors have on a system's key functions helps establish relevant performance goals that prevent overworking the problem, while at the same time managing the risk of missing key performance and cost commitments. Finally, some form of electronic alignment might be necessary for optimizing a system's performance/cost trade space.

Predicting Alignment Error After Installation

The alignment accuracy in an application will depend on two key things: the IMU's misalignment error and the precision of the mechanical system that holds it in place during operation. The IMU's contribution (Ψ_{IMU}) and the system's contribution (Ψ_{SYS}) are not typically related to each other, so estimating the total misalignment error often comes from combining these two error sources using a root-sum-square calculation:

$$\Psi_T = \sqrt{\Psi_{IMU}^2 + \Psi_{SYS}^2} \quad (1)$$

Some IMU specification tables quantify misalignment errors through parameters such as *axis to package misalignment error* or *axis to frame misalignment error*. Figure 1 provides an exaggerated view of these misalignment errors for each gyroscope in the ADIS16485, with respect to the edges of its package. In this illustration, the green, dashed lines represent the axes in the package defined reference frame. The solid lines represent the axes of rotation for the gyroscopes inside of the package and Ψ_{IMU} represents the maximum of the three misalignment terms (Ψ_X, Ψ_Y, Ψ_Z).

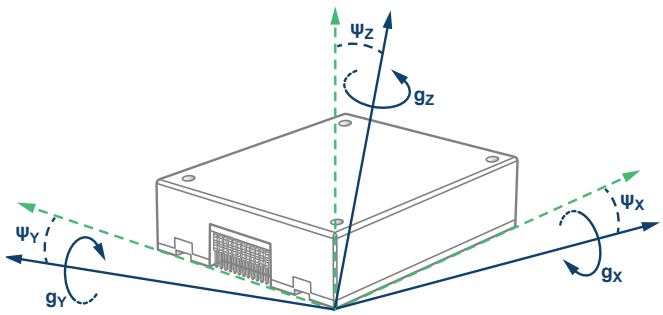

Figure 1. ADIS16485 axis to frame misalignment.

Predicting the system's contribution (Ψ_{SYS} in Equation 1) to misalignment error involves analyzing any opportunity for mechanical imperfection that can skew the IMU's resting place in the system, with respect to the global frame. When using an IMU that solders to a printed circuit board, this will involve consideration of things like original placement accuracy, variation in solder deposition, float during solder reflow, tolerances of key PCB features (like mounting holes), and tolerances of the system frame itself. When using a module level IMU, more direct coupling to the system enclosure may be possible, as shown in Figure 2. This type of interface has two key mechanical features that help manage the mounting skew errors, the mounting ledges (4×), and the mounting nest.

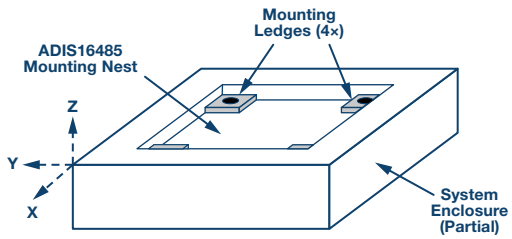

Figure 2. Nested baseplate design concept.

In this type of mounting scheme, variation in the height of the four mounting ledges is one example of mechanical variation that can cause mounting skew in the x-axis and y-axis. Figure 3 provides an exaggerated illustration to help explain the impact that this variation (H1 vs. H2) has on the mounting skew (Ψ_X), with respect to the x-axis.

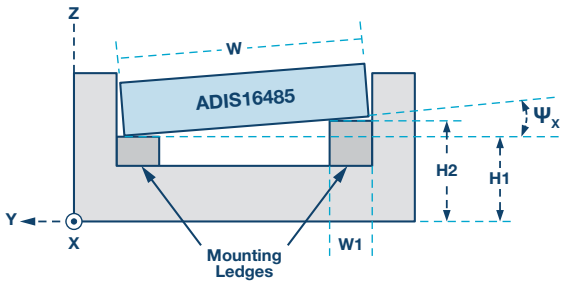

Figure 3. Misalignment error due to mounting ledge variation.

Equation 2 provides a relationship for predicting the x-axis skew angle (Ψ_X) associated with the difference in height (H2 to H1) and the span between the two points of contact (W to W1):

$$\Psi_X = \arctan\left(\frac{H2 - H1}{W - W1}\right) \; when \; H2 - H1 << W - W1 \qquad (2)$$

The variation in mounting ledge height will have a similar impact on mounting skew around the y-axis. In that case, substitute the package length (L) for the width (W) in Equation 2 to develop the following relationship for estimating y-axis skew angle (Ψ_Y).

$$\Psi_Y = \arctan\left(\frac{H2 - H1}{L - W1}\right) \; when \; H2 - H1 << L - W1 \qquad (3)$$

Figure 4 provides another example of how a mechanical attribute can impact mounting skew around the z-axis. In this case, machine screws will slide through mounting holes in the IMU body (in all four corners), through holes in the mounting ledge, and then into locking nuts on the backside of the mounting ledges. In this scenario, the difference between the diameter of the machine screws (D_M) and their associated pass-through holes (D_H) in the baseplate present an opportunity for skew in the z-axis.

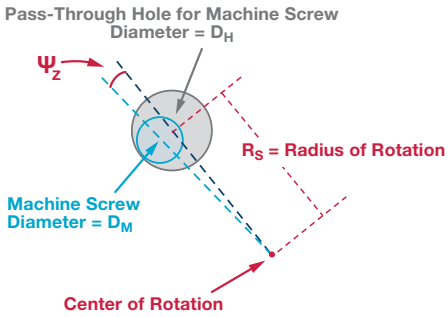

Figure 4. Mounting screw/hole impact on z-axis skew angle.

Equation 4 provides a relationship for predicting the opportunity for z-axis mounting skew (Ψ_Z), based on this difference in diameters and the radius of rotation (R_S), which is equal to one half of the distance between the two mounting screws in opposite corners.

$$\Psi_Z = 2 \times a\tan\left(\frac{D_H - D_M/2}{2 \times R_S}\right) \qquad (4)$$

Example 1

Estimate the overall misalignment associated with using 2 mm machine screws to mount the ADIS16485 onto 6 mm × 6 mm mounting ledges, which have 2.85 mm holes and a height tolerance of 0.2 mm.

Solution

Using the nominal width (W) of 44 mm, the x-axis skew angle (see Figure 3) prediction is 0.3°

$$\Psi_X = \arctan\left(\frac{H2 - H1}{W - W1}\right) = \arctan\left(\frac{0.2 \text{ mm}}{44 \text{ mm} - 6 \text{ mm}}\right) = 0.3°$$

The nominal distances between the mounting holes on each side of this package are 39.6 mm and 42.6 mm, respectively. These dimensions form the two sides of a right angle triangle, whose hypotenuse is equal to the distance between the two holes in opposite corners of the package. The radius of the rotation (R_S, see Figure 4) is equal to one half of this distance (29.1 mm), which leads to a prediction of 0.83° of skew in the z-axis.

$$R_S = \frac{\sqrt{39.6^2 + 42.6^2}}{2} \approx 29.1 \text{ mm}$$

$$\Psi_Z = 2 \times a\tan\left(\frac{D_H - D_M/2}{2 \times R_S}\right) = 2 \times a\tan\left(\frac{2.85 - 2/2}{2 \times 29.1}\right) \approx 0.83°$$

For the composite prediction formula in Equation 1, Ψ_{SYS} is equal to Ψ_Z (maximum from estimates) and Ψ_{IMU} is equal to 1° per the axis to frame misalignment error specification in the IMU's data sheet. This generates a total misalignment error estimate of 1.28°.

$$\Psi_T = \sqrt{\Psi_{IMU}^2 + \Psi_{SYS}^2} = \sqrt{1^2 + 0.8^2} = \sqrt{1.64} = 1.28°$$

Misalignment Impact on System Accuracy

Understanding the basic relationship between misalignment errors and the impact that they have on gyroscope accuracy is a good place to start when developing accuracy criteria

for an application. To start this process, Figure 5 provides a generic illustration of a three axis gyroscope system. In this diagram, the three solid green lines represent the three axes in the global frame, the black solid lines represent the axes of rotation for all three gyroscopes, and the Ψ-based labels represent the misalignment errors between global frame and gyroscope axes. Equation 5, Equation 6, and Equation 7 demonstrate the impact that the misalignment errors have on each gyroscope's response to rotation around its assigned axis in the global frame. In these equations, the cosine of the misalignment angle introduces a scale error.

$$G_X = \omega_X \times \cos(\Psi_X) \quad (5)$$

$$G_Y = \omega_Y \times \cos(\Psi_Y) \quad (6)$$

$$G_Z = \omega_Z \times \cos(\Psi_Z) \quad (7)$$

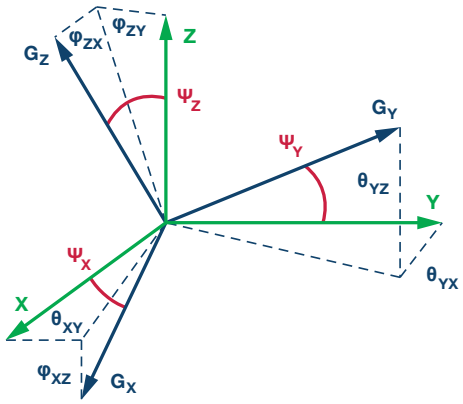

Figure 5. Orthogonal three-axis gyroscopes with alignment errors.

Misalignment errors also introduce cross-axis influences on each axis. Quantifying these influences requires breaking the misalignment angle for each axis down into two components, which relate to the two other axes. For example, Ψ_X has a y-axis component (ϕ_{XY}) and a z-axis component (ϕ_{XZ}), which results in the following expansion of the x-axis gyroscope response to rotation around all three axes in the global frame (ω_X, ω_Y, ω_Z):

$$G_X = \omega_X \times \cos(\Psi_X) + \omega_Y \times \sin(\phi_{XY}) + \omega_Z \times \sin(\phi_{XZ}) \quad (8)$$

This same expansion applies to the y-axis and z-axis gyroscopes:

$$G_Y = \omega_X \times \sin(\phi_{YX}) + \omega_Y \times \cos(\Psi_Y) + \omega_Z \times \sin(\phi_{YZ}) \quad (9)$$

$$G_Z = \omega_X \times \sin(\phi_{ZX}) + \omega_Y \times \sin(\phi_{ZY}) + \omega_Z \times \cos(\Psi_Z) \quad (10)$$

Integrating both sides of Equation 8, Equation 9, and Equation 10 produces similar relationships, which are in terms of angle displacement. In the resulting Equation 11, Equation 12, and Equation 13, the angles of interest are the angular displacement around the global frame ($\theta_{X\omega}$, $\theta_{Y\omega}$, $\theta_{Z\omega}$) and the integration of each gyroscope (θ_{XG}, θ_{YG}, θ_{ZG}).

$$\theta_{XG} = \theta_{X\omega} \times \cos(\Psi_X) + \theta_{Y\omega} \times \sin(\phi_{XY}) + \theta_{Z\omega} \times \sin(\phi_{XZ}) \quad (11)$$

$$\theta_{YG} = \theta_{X\omega} \times \sin(\phi_{YX}) + \theta_{Y\omega} \times \cos(\Psi_Y) + \theta_{Z\omega} \times \sin(\phi_{YZ}) \quad (12)$$

$$\theta_{ZG} = \theta_{X\omega} \times \sin(\phi_{ZX}) + \theta_{Y\omega} \times \sin(\phi_{ZY}) + \theta_{Z\omega} \times \cos(\Psi_Z) \quad (13)$$

Example 2

A ground-based, unmanned vehicle (UV) is using a MEMS IMU as a feedback sensor in a platform stabilization control (PSC) system for its antenna. This system employs an RSS tuner loop that requires the azimuth and elevation angles to stay within ±1° to maintain continuous communication. During the most dynamic conditions, the PSC relies heavily on the y-axis gyroscope's measurement for elevation angle control and the z-axis gyroscope's measurements for azimuth angle control. The maximum change in heading ($\theta_{Z\omega}$) during these dynamic conditions is 30° and there is no rotation around the x-axis or y-axis ($\theta_{X\omega} = \theta_{Y\omega} = 0$) during this maneuver.

Solution

Zero rotation around the x-axis and y-axis enable Equation 8 and Equation 9 to reduce to the following:

$$\theta_{YG} = \theta_{Z\omega} \times \sin(\phi_{YZ})$$
$$\theta_{ZG} = \theta_{Z\omega} \times \cos(\Psi_Z)$$

Starting with the y-axis, establish a maximum boundary of 1° for θ_{YG} and solve for the misalignment term Φ_{YZ}. This process establishes a maximum allowable misalignment error of 1.9° for the y-axis gyroscope.

$$\phi_{YZ} \le \sin^{-1}\left(\theta_{YG} / \theta_{Z\omega}\right)$$
$$\phi_{YZ} \le \sin^{-1}\left(1° / 30°\right)$$
$$\phi_{YZ} \le 1.9°$$

For the z-axis, set $\theta_{Z\omega}$ equal to 30° and establish a maximum boundary of 1,° for the difference between θ_{ZG} and $\theta_{Z\omega}$, then solve for Ψ_Z. This process establishes a maximum allowable misalignment error of 14.8° on the z-axis gyroscope.

$$\theta_{Z\omega} - \theta_{ZG} \le 1°$$
$$\theta_{Z\omega} - \theta_{Z\omega} \times \cos(\Psi_Z) \le 1°$$
$$\theta_{Z\omega} - 1° \le \theta_{Z\omega} \times \cos(\Psi_Z)$$
$$1 - 1° / \theta_{Z\omega} \le \cos(\Psi_Z)$$
$$\Psi_Z \le \cos^{-1}\left[1 - 1° / \theta_{Z\omega}\right]$$
$$\Psi_Z \le \cos^{-1}\left[1 - 1° / 30°\right]$$
$$\Psi_Z \le 14.8°$$

These calculations reveal that the cross-axis behaviors between the y-axis and z-axis will drive the alignment accuracy requirement of ~1.9,° for this specific maneuver/scenario.

Electronic Alignment

In cases where an IMU and attachment system will not meet critical system objectives, electronic alignment provides a method for reducing the misalignment errors. This process has two key steps: characterize the misalignment terms (after IMU installation) and develop a correcting alignment matrix that corrects the gyroscopes to respond as if they were aligned with the global frame, when it's applied to the gyroscope

array. Equation 14 provides a system model for this process, where rotation around each axis in the global frame ($\overline{\omega}$) are the three system inputs, the three gyroscope responses ($\overline{G}$) are the system outputs, and a 3 × 3 matrix (M) represents the system behaviors (including misalignment) between the inputs and outputs.

$$\overline{G} = M \times \overline{\omega} \tag{14}$$

Simple algebraic manipulation determines that product of the gyroscope measurements ($\overline{G}$) and inverse of M (M^{-1}) is equal to the global frame's rotation array ($\overline{\omega}$). Therefore, the alignment matrix is equal to M^{-1}.

$$\begin{aligned} M^{-1} \times \overline{G} &= M^{-1} \times M \times \overline{\omega} \\ M^{-1} \times \overline{G} &= \overline{\omega} \end{aligned} \tag{15}$$

Equation 8, Equation 9, and Equation 10 provide the basis for expanding Equation 14 to include the misalignment terms in Equation 16 and more generically in Equation 17 and Equation 18:

$$\begin{bmatrix} G_X \\ G_Y \\ G_Z \end{bmatrix} = \begin{bmatrix} \cos(\Psi_X) & \sin(\phi_{XY}) & \sin(\phi_{XZ}) \\ \sin(\phi_{YX}) & \cos(\Psi_Y) & \sin(\phi_{YZ}) \\ \sin(\phi_{ZX}) & \sin(\phi_{ZY}) & \cos(\Psi_Z) \end{bmatrix} \begin{bmatrix} \omega_X \\ \omega_Y \\ \omega_Z \end{bmatrix} \tag{16}$$

$$\begin{bmatrix} G_X \\ G_Y \\ G_Z \end{bmatrix} = \begin{bmatrix} M_{11} & M_{12} & M_{13} \\ M_{21} & M_{22} & M_{23} \\ M_{31} & M_{32} & M_{33} \end{bmatrix} \begin{bmatrix} \omega_X \\ \omega_Y \\ \omega_Z \end{bmatrix} \tag{17}$$

$$M = \begin{bmatrix} M_{11} & M_{12} & M_{13} \\ M_{21} & M_{22} & M_{23} \\ M_{31} & M_{32} & M_{33} \end{bmatrix} \tag{18}$$

Rotating the entire system around one axis at a time simplifies the system model enough to isolate each element in the matrix to one of the gyroscope measurements. For example, rotating the system around the x-axis ($\omega_X = \omega_{TR}$, $\omega_Y = 0$, $\omega_Z = 0$) while observing all three gyroscopes helps simplify the relationships for M11, M21, and M31 to the following:

$$M_{11} = G_X / \omega_{TR} \tag{19}$$

$$M_{21} = G_Y / \omega_{TR} \tag{20}$$

$$M_{31} = G_Z / \omega_{TR} \tag{21}$$

Using the same approach, y-axis rotation ($\omega_X = 0$, $\omega_Y = \omega_{TR}$, $\omega_Z = 0$) helps simplify the relationships for M12, M22, and M32 to the following:

$$M_{12} = G_X / \omega_{TR} \tag{22}$$

$$M_{22} = G_Y / \omega_{TR} \tag{23}$$

$$M_{32} = G_Z / \omega_{TR} \tag{24}$$

Finally, z-axis rotation ($\omega_X = 0$, $\omega_Y = 0$, $\omega_Z = \omega_{TR}$) helps simplify the relationships for M13, M23, and M33 to the following:

$$M_{13} = G_X / \omega_{TR} \tag{25}$$

$$M_{23} = G_Y / \omega_{TR} \tag{26}$$

$$M_{33} = G_Z / \omega_{TR} \tag{27}$$

Obviously, the accuracy of the motion profile ($\overline{\omega}$) and gyroscope measurements ($\overline{G}$) have a direct impact on this process. In particular, off-axis motion can have a significant impact on this process, so it should be a strong consideration when purchasing and deploying inertial test equipment that will execute on these requirements. With respect to the gyroscope accuracy, bias and noise are two threats to accuracy that typically require consideration during this process. One technique for managing the impact of residual bias error (b_E) in the gyroscope measurements is through using two different rates of rotation, which are equal and opposite to each other. For example, when rotating in the positive direction around the y-axis ($\omega_Y = \omega_{TR}$, $\omega_X = \omega_Z = 0$), Equation 28 describes the z-axis gyroscope response, with bias error. Equation 29 describes the z-axis gyroscope response when rotating around the y-axis in the negative direction ($\omega_Y = -\omega_{TR}$, $\omega_X = \omega_Z = 0$):

$$G_{ZP} = M_{32} \times \omega_{TR} + b_E \tag{28}$$

$$G_{ZN} = -M_{32} \times \omega_{TR} + b_E \tag{29}$$

Rearrange Equation 29 to relate to the bias error (b_E), substitute it into Equation 28, and then solve for M32. Notice how the bias error (b_E) drops out of the formula.

$$\begin{aligned} G_{ZN} &= -M_{32} \times \omega_{TR} + b_E \\ b_E &= G_{ZN} + M_{32} \times \omega_{TR} \\ G_{ZP} &= M_{32} \times \omega_{TR} + G_{ZN} + M_{32} \times \omega_{TR} \\ G_{ZP} - G_{ZN} &= M_{32} \times \omega_{TR} + M_{32} \times \omega_{TR} \\ G_{ZP} - G_{ZN} &= 2 \times M_{32} \times \omega_{TR} \end{aligned}$$

$$M_{32} = \frac{G_{ZP} - G_{ZN}}{(\omega_{ZP} - \omega_{ZN})} = \frac{G_{ZP} - G_{ZN}}{2 \times \omega_{TR}} \tag{30}$$

This formula assumes that the bias error is constant during both measurements, which is not a realistic expectation, so it is wise to understand the opportunity for variation (temperature, time, and noise) from measurement to measurement. When the measurements are taken in succession, under stable temperature conditions, noise is often the key error to manage in this process. The acceptable level of noise in the gyroscope measurements will depend on the alignment accuracy goal (Ψ_T) and the rate of rotation on each axis during the characterization (ω_{TR}). A common technique for noise reduction is through averaging a time record of gyroscope data, while the inertial conditions are constant. The Allan variance curves provides a tool for understanding the trade-off between repeatability (noise) and the averaging time.

Example 3

If the rate of rotation during characterization is 100°/s, the alignment accuracy goal is 0.1,° and the noise (rms) must be 10× less than the misalignment goal, how long do we need to average the outputs of the ADIS16485 to achieve these objectives?

Solution

Using a generic response between a gyroscope and input (rotation on test platform), the following calculations reveal that the total noise (rms) in each gyroscope must be less than 62°/hour.

$$G_{Noise} \le \frac{1}{10} \times \omega_{TR} \times \sin(\Psi_T)$$

$$G_{Noise} \le 0.1 \times 100 \,{}^{\circ}\!/_{\mathrm{s}} \times \sin(0.1^{\circ})$$

$$G_{Noise} \le 0.017 \,{}^{\circ}\!/_{\mathrm{s}} = \sim 62 \,{}^{\circ}\!/_{\mathrm{hour}}$$

Figure 6 provides an example of how to use the Allan variance curve for this IMU to select an averaging time to meet this requirement. In this case, an averaging time of 0.1 seconds meets the 62°/hour objective for repeatability, with some margin.

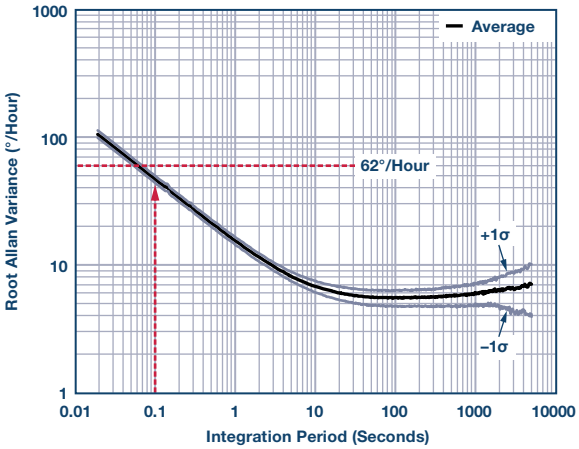

Figure 6. ADIS16485 Allan variance curve.

Note that this approach only accounts for the noise in the sensor itself. If the test platform has vibration that adds noise to the gyroscope measurements, that may require additional consideration and filtering.

Tips and Tricks for Simplifying the Process

Developing a triaxial inertial test system with the necessary precision and environmental control temperature typically requires a substantial investment in capital equipment and engineering development resources. For those who are developing first or second generation systems that have many questions to answer during development, these types of resources or time may not be available. This situation creates a need for a simpler solution, which can come through careful IMU selection and leveraging natural motion that is available in the instrument or in the application.

For example, sometimes working with angles may be more convenient than working with angular rate measurements. Equation 31 combines Equation 11, Equation 12, and Equation 13 to represent system behaviors (M) in terms of angles around the global frame ($\theta_{X\omega}$, $\theta_{Y\omega}$, $\theta_{Z\omega}$) and from integrating the gyroscope outputs (θ_{XG}, θ_{YG}, θ_{ZG}):

$$\begin{bmatrix} \theta_{XG} \\ \theta_{YG} \\ \theta_{ZG} \end{bmatrix} = \begin{bmatrix} M_{11} & M_{12} & M_{13} \\ M_{21} & M_{22} & M_{23} \\ M_{31} & M_{32} & M_{33} \end{bmatrix} \begin{bmatrix} \theta_{X\omega} \\ \theta_{Y\omega} \\ \theta_{Z\omega} \end{bmatrix} \quad (31)$$

With respect to device selection, axis to axis misalignment error is a key parameter to consider, because when it is lower than the axis to package misalignment parameter, it can help reduce the complexity of the inertial test profile (in Equation 16) associated with electronic alignment. While the axis to package misalignment parameter describes gyroscope orientation, with respect to an external mechanical reference, the axis to axis misalignment parameter relates the orientation of each gyroscope with respect to the other two gyroscopes. Most often, the ideal orientation for the three gyroscopes in a MEMS IMU is 90° from each other, so axis to axis misalignment relates to another common parameter for this behavior—cross-axis sensitivity. Using Figure 7 as a reference, axis to axis misalignment would represent the maximum of these three relationships:

$$\phi_{xye} = \phi_{xy} - 90^{\circ} \quad (32)$$

$$\phi_{yze} = \phi_{yz} - 90^{\circ} \quad (33)$$

$$\phi_{zxe} = \phi_{zx} - 90^{\circ} \quad (34)$$

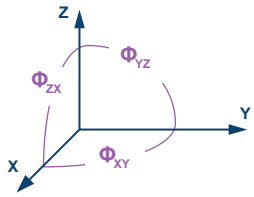

Figure 7. Axis to axis misalignment diagram.

The axis to axis misalignment parameter establishes the error associated with assuming that the sensors have perfect orthogonal alignment when developing an electronic alignment process. Using the perfectly orthogonal assumption, one can align all three axes through only two axes of rotation. For example, rotating around the y-axis and z-axis provides for direct observation of M_{12}, M_{13}, M_{22}, M_{23}, M_{32}, and M_{33}. Assuming perfect orthogonal alignment and applying some trigonometric properties enables calculation of the other three elements (M_{11}, M_{21}, and M_{31}) using the six elements and the following relationships:

$$M_{21} = M_{12} \quad (35)$$

$$M_{31} = M_{13} \quad (36)$$

$$M_{11} = \sqrt{1 - M_{12}^2 - M_{13}^2} \quad (37)$$

These identities result in the following update to the system model, where all nine elements in the M matrix are in terms of the six elements that come from y-axis and z-axis rotation.

$$\begin{bmatrix} G_X \\ G_Y \\ G_Z \end{bmatrix} = \begin{bmatrix} \sqrt{1-M_{12}^2-M_{13}^2} & M_{12} & M_{13} \\ M_{12} & M_{22} & M_{23} \\ M_{13} & M_{32} & M_{33} \end{bmatrix} \begin{bmatrix} \omega_X \\ \omega_Y \\ \omega_Z \end{bmatrix} \quad (38)$$

Conclusion

Inertial MEMS technology has made amazing advances in the past few years, providing system developers with a wide range of options inside a complex trade space that includes size, weight, power, unit cost, integration cost, and performance. For those who are architecting motion control systems with MEMS IMU for the first time, there are a lot of things to learn, with respect to selecting the right IMU and preparing to support critical system requirements with this IMU. Since alignment accuracy can have a significant impact on critical performance, cost, and schedule objectives, it is an important consideration. Even simple analytical tools can help identify potential risk items during conceptual and architectural design stages, while there is still time to influence device selection, mechanical design, post assembly calibration (electronic alignment), preliminary cost projections, and key schedule milestones. Taking this even further, others will find value in recognizing key MEMS IMU metrics and opportunities to replace triaxial inertial test equipment with natural motion available in their system to get to the best value (performance, total cost of deployment) out of their systems.

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Mark Looney

Also by this Author:

An Introduction to MEMS Vibration Monitoring

Volume 8, Number 2

Multifunction: a Dilemma or Reality?

By Duncan Bosworth

Next-generation aerospace and defense system designers are being pushed to develop advanced, highly configurable systems that combine a range of functions and requirements, integrating functionality that would have historically been implemented by separate standalone systems. Clearly this has the benefit of reducing the number of subsystems that need to be supported by any mission platform, reducing the overall size, weight, and power (SWaP), but with further need to support cognitive and real-time configurability, the challenges can seem daunting. However, a new generation of high performance, wideband components are potentially providing a solution to this challenge, supporting the high performance levels required for each system, but with a broad enough operating range to meet the multifunction challenge.

The ultimate goal for many of these future systems is a completely software determined architecture. This allows for the implementation and mode of operation to be changed dynamically, updated in the field, or factory configured with no, or very minor, hardware changes. The challenge is to support the superset of operational modes that the system may be required to enable. This requires that the underlying single piece of hardware is able to meet the specifications of all the possible modes of operation that may be needed.

An example of such systems in the defense world looking to combine functions are radar and communication platforms. In many cases, these systems look to support multimodes of legacy operation, but they are also starting to incorporate electronic warfare functionality. Radar systems are looking to support electronic support measures (ESM), and communication systems looking to implement signal intelligence (SIGINT) functionality, as well as multimode radar and multiwaveform communications respectively.

In both of these examples, the systems are looking to incorporate wideband and narrow-band functionality, functions that would typically drive very different requirements in terms of linearity and dynamic range, among other requirements. To meet the overarching goal, the designer may have to trade power or size if compromises to the specifications are not acceptable. As an example, consider an X band radar system and an electronic intelligence system (ELINT). The radar system will typically operate over a relatively narrow frequency range, typically hundreds of MHz within the 8 GHz to 12 GHz band. In contrast, the ELINT system will typically require operating over the 2 GHz to 18 GHz range, covering all of the S, C, and X frequency bands. If the assumption is made that both implementations have to be the same size, then compromises to the performance may need to be made to support the wider frequency range and coverage of the ELINT system. Typically in this instance, the linearity or power consumption of the signal chain can be traded for bandwidth.

If this same concept is taken down to the component level, the same issues are observed. For broadband or wideband systems, typically the performance of the component is sacrificed in at least one dimension, whether that be linearity, noise performance, or power. Table 1, as follows, illustrates a typical performance trade-off for wideband and narrow-band phase-locked loop (PLL) with an integrated voltage controlled oscillator (VCO). As seen, the narrow-band device has better typical phase noise, figure of merit, and power, but clearly this is at the expense of flexibility.

Table 1. Comparison of Typical Wideband and Narrow-Band PLLs with Integrated VCO

	ADF4351 Wideband PLL with VCO	HMC837 Narrow–Band PLL with VCO
Output Frequency	0.035 GHz to 4.4 GHz	1.025 GHz to 1.150 GHz
Figure of Merit	–221 dBc/Hz	–230 dBc/Hz
VCO P/N @ 100 kHz (dBc/Hz)	–114	–120
VCO P/N @ 1 MHz (dBc/Hz)	–134	–147
Size	5 mm × 5 mm	6 mm × 6 mm
Power	370 mW	168 mW

Although there will always be some trade-off and some compromise when multiple system specifications are implemented in a single system, the next generation of RF and microwave components, as well as high speed ADCs, will provide some relief to future system designers. Advances in CMOS and silicon-germanium (SiGe) processes, among others, are enabling a significant increase in digital functionality to be incorporated into next-generation devices. Advanced signal processing capabilities are able to provide calibration or digital compensation functionality, in addition to flexibility, enabling the overall system performance levels to be closer to their narrow-band counterparts, while maintaining the ability to be reconfigurable and utilize wider bandwidths for mode of operation as needed.

Figure 1 shows a generic wideband receiver architectural diagram based on a number of the latest RF and microwave components.

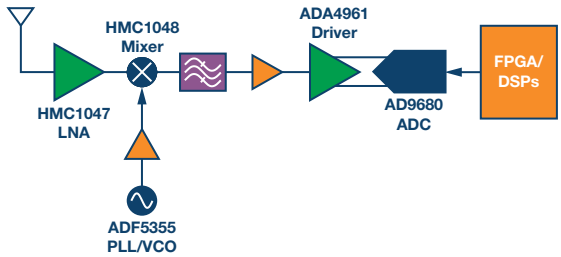


Figure 1. Possible wideband reconfigurable signal chain.

Although in practice the architecture described above may require additional filtering and gain stages to achieve a specific application requirement, the flexibility of the underlying components enables a very wideband surveillance system architecture to be implemented. In addition, configurable digital signal processing functionality has the ability to enable the signal chain to perform more narrow-band functions when needed. Furthermore, the system can support dynamic, real-time mode changing, potentially supporting more cognitive functions in conjunction with further digital signal processing downstream.

The first two stages of the proposed chain, the low noise amplifier (LNA) and mixer are implemented using GaAS technology. While advances are being made with wideband SiGe mixers, the use of GaAs and GaN devices for front-end components is still expected. In both cases, the HMC1049 and HMC1048 offer very wide performance and excellent IP3, which supports both narrow-band and wideband operations. These devices illustrate where process advances enable a single device to meet multiple specifications, without requiring additional digital functionality. The benefit of embedding digital functionality in an RF device can be seen in other elements of the signal chain.

The new ADF5355 PLL with integrated VCO supports RF outputs from 54 MHz to 13.6 GHz and provides a wide range of synthesizer frequencies to be used. Based on SiGe, the device is able to support such a wide range of operation by using four separate integrated VCO cores. Each of these cores use 256 overlapping bands, which allows the device to cover a wide frequency range without requiring large VCO sensitivity, and without sacrificing phase noise and spurious performance. The correct VCO and band are chosen automatically using digital calibration logic integrated inside the device. The device enables the signal chain to support RF scanning from 54 MHz up to 13.6 GHz, as well as fixed frequencies as needed. It does this while maintaining high performance, with typical phase noise levels of –138 dBc/Hz at 1 MHz offset, as required for more narrow-band system operations.

The ADA4961 ADC driver provides wideband performance with excellent linearity. Using SPI and embedded digital control, it achieves 90 dBc IMD3 performance at 500 MHz and –87 dBc at 1.5 GHz. Digital control is incorporated in the device to support gain control as well, with fast attack options enabling the device to be configured, as needed, to provide the optimal performance of the system. The fast attack also increases the flexibility of the system, as it provides rapid gain reduction when the FA pin is driven, typically by the overrange detection output of the ADC, which enables the ADC to remain out of saturation.

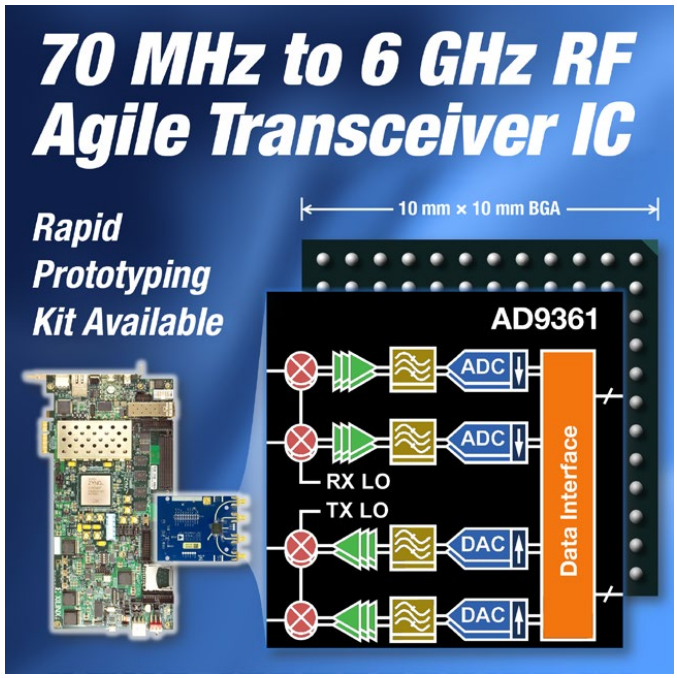
The AD9680 completes the chain and is one of the latest high speed converters. Based on 65 nm CMOS, the device supports sampling at up to 1 GSPS at a resolution of 14 bits. Using higher sample rates and the bandwidths of gigasample converters, the AD9680 potentially supports undersampling an IF in excess of 1 GHz. This supports the continued trend of moving the digital conversion point of the system closer to the antenna and increasing the flexibility of the system. The device not only provides industry-leading SFDR and SNR but also incorporates digital downconversion (DDC) signal processing, to provide customizable output bandwidths.

The digital signal processing configurability of the AD9680 ADC enables the device to support wideband surveillance, as well as narrow-band functionality. With the incorporated DDC disabled and bypassed, it can support an instantaneous surveillance bandwidth in excess of 500 MHz. Utilizing the DDCs, the digital numerically controlled oscillator (NCO) can be set to digitally mix a narrow-band IF to baseband before configurable decimation filters reduce the data rate, supporting output data bandwidths down to 60 MHz when the device is operated at the maximum ADC sample rate. The digital signal processing improves the SNR of the system for the lower bandwidth, again supporting the flexibility needed for a configurable wideband and narrow-band signal chain.

Although the example has focused on the receiver path, similar devices and levels of integration are available for the transmitter side. New DACs are incorporating highly configurable interpolation filters and digital upconversion functionality, and can be used in conjunction with similar broadband RF and microwave components, as previously mentioned.

The example described shows how new generation wideband devices are incorporating increasing levels of digital signal processing and functionality, and how this is enabling future systems to be dynamically configured for multimode operation with levels of performance previously not possible. This contradicts the view that narrow-band and wideband operations cannot coexist. It should be noted that this brief analysis has not included some of the filtering challenges, or an analysis of power. These factors may heavily influence the actual design choices and signal chain architecture. However, with more wideband higher performance devices, and increased levels of signal processing being developed, the future looks promising for highly configurable, cognitive, and software-defined systems.

Finally, and to illustrate the discussion further, integrated RF IC devices such as the AD9361 provide the ultimate level of integration and further demonstrate the disappearing boundary between digital and analog functionality. Supporting a direct conversion architecture, combined with digital filtering and calibration functionality, the AD9361 provides a high degree of flexibility able to support RF input frequencies from 70 MHz to 6 GHz and bandwidths of up to 56 MHz.

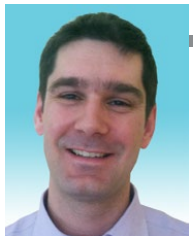


The configurability of the AD9361 supports a wide range of applications and uses, including radar, communications, and data links, as well as electronic surveillance and warfare. With digital calibration and processing, the device is able to overcome many of the typical issues found in a direct conversion system, and provides an unprecedented level of integration and configurability, again further supporting cognitive and multifunction systems.

Previously, this level of integration and associated performance was not possible. In addition, many system designers shied away from the use of direct conversion architectures, as the limitations of aspects, such as image rejection over frequency and temperature, could not be overcome. The increased coupling of digital and analog, with advanced calibration and processing now integrated into these devices, provides solutions to these challenges, increasing flexibility without significantly sacrificing performance and power consumption. Although it may still be able to obtain better performance using a more narrow-band, dedicated signal chain using discrete components, the gap is certainly narrowing.

The ultimate goal of a software-defined system, a single RF and microwave signal chain for all applications, would ideally be a single component such as a transceiver supporting multifunction and cognitive applications. In reality, for all systems this may still be some time away, but new advanced developments are getting closer to this goal with ever more functionality being incorporated into each new semiconductor device. In addition to simply improving traditional RF performance, digital signal processing is providing solutions to relieve and overcome some of the multimode challenges. It may not be long before a single solution, using a single device or a cascade of wideband devices, for all applications becomes available and the drive to truly software-defined systems become a reality.

Duncan Bosworth



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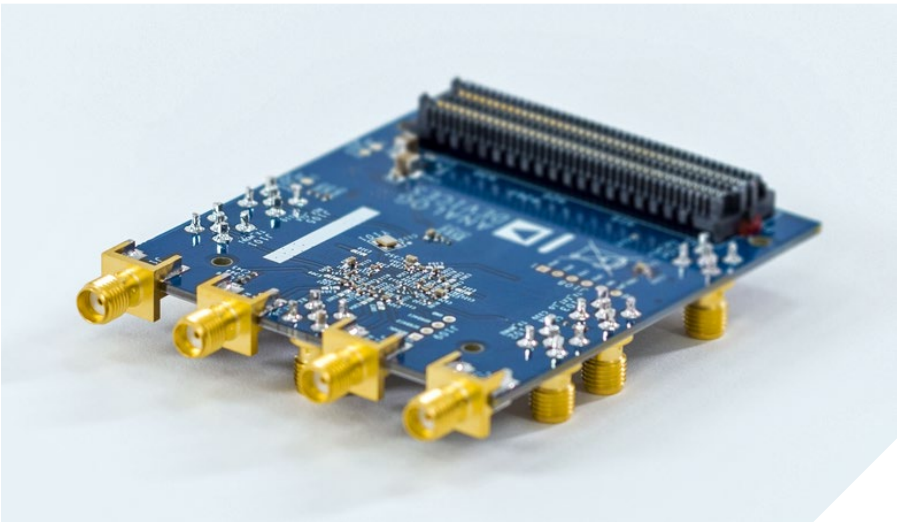

Low Power Synchronous Demodulator Design Considerations

By Brian Harrington

Introduction

"Synchronous Detectors Facilitate Precision, Low-Level Measurements," published in the November 2014 issue of *Analog Dialogue*, discusses the benefits of using synchronous demodulation to measure low level signals in the presence of relatively high noise levels. This article extends the discussion by looking at some design considerations for sensor signal conditioning using synchronous demodulation in systems with strict power and cost constraints. When carefully designed, analog systems are hard to beat for simplicity, low cost, and low power consumption. This architecture performs most of the signal processing in the analog domain.

Sensor Excitation

Sensors, which are ubiquitous, are used to measure temperature, light, sound, and a variety of other environmental parameters. Some sensors act as parameter-dependent voltage or current sources. Thermocouples, for example, generate a voltage that is proportional to the temperature difference between a reference junction and the measurement point. Most sensors have transfer functions that follow a known relationship with respect to the physical parameter. The transfer function is often an impedance, where current is the sensor input and the voltage across the sensor indicates the parameter of interest. Resistive sensors such as load cells, RTDs, and potentiometers are used to measure strain, temperature, and angle, respectively. To first order, resistive sensors are frequency independent and have no phase response.

Many sensors require ac excitation signals as their transfer functions change in frequency and phase. Examples include inductive proximity sensors and capacitive humidity sensors. Biometric impedance measurements can yield information about respiratory rate, pulse rate, hydration, and many other physiological parameters. In these cases, the magnitude, phase, or both may be used to determine the value of the sensed parameter.

In some applications, transducers turn a sample under test into a sensor. Colorimeters, for example, use an LED to shine light through a liquid sample under test. The light absorption of the sample modulates the amount of light detected by a photodiode to reveal characteristics about the liquid under test. Blood-oxygen levels can be determined by measuring the difference in light absorption of red and infrared light in vascular tissue. Ultrasonic transducers measure gas flow rates based on Doppler frequency shifts of the ultrasound as it travels through the gas. All of these systems can be implemented using synchronous demodulation.

Figure 1 shows a synchronous demodulation system for measuring a sensor's output signal. An excitation signal, f_x, acts as a carrier that the sensor modulates in amplitude, phase, or both as a function of the parameter being measured. The signal may be amplified and filtered before being modulated back down to dc by the phase-sensitive detector (PSD). An output filter (OF) limits the bandwidth of the signal to the frequency range of the parameter being measured.

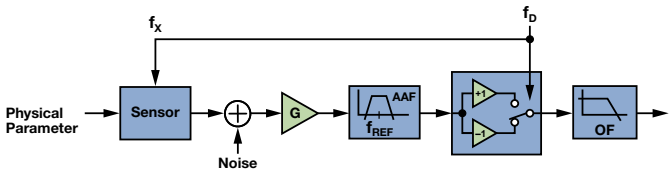

Figure 1. Synchronous demodulation system.

Noise at the sensor output may be due to internal sources or external coupling. Low frequency (1/f) noise often limits performance of the sensor or measurement electronics. Many sensors are also susceptible to interference from low-frequency environmental noise. Optical measurements are susceptible to background light and electromagnetic sensors can be susceptible to radiation from the power supply. Freedom to choose the excitation frequency to avoid noise sources is a key benefit of synchronous demodulation.

Choosing an excitation frequency that reduces the effect of these noise sources is an important way to optimize system performance. The selected excitation frequency should have a low noise floor and be far enough away from noise sources so that modest output filtering can reduce the noise to acceptable levels. Sensor excitation is often the largest item in the power budget. If the sensor's sensitivity vs. frequency is known, power consumption can be reduced by exciting the sensor at a frequency where its sensitivity is high.

The Phase-Sensitive Detector

Understanding the requirements of the antialiasing filter (AAF) and OF requires an understanding of the PSD. Consider a PSD that uses the excitation signal to synchronously multiply the input signal by +1 and –1. This is equivalent to multiplying the input signal with a square wave of the same frequency. Figure 2a shows the time domain waveforms for the input signal, reference, and PSD output for the case where the input signal is a square wave with arbitrary phase relative to the reference.

When the input and reference are perfectly in phase, the relative phase is 0°, the switch output is dc, and the PSD output voltage is +1. As the relative phase increases, the switch output becomes a square wave at twice the reference frequency, and the duty cycle and average value diminish linearly. At a relative phase of 90°, the duty cycle is 50% and the average value is 0. At a relative phase of 180°, the PSD output voltage is –1. Figure 2b shows the average output value of the PSD as the relative phase is swept from 0° to 360° for square wave and sine wave input signals.

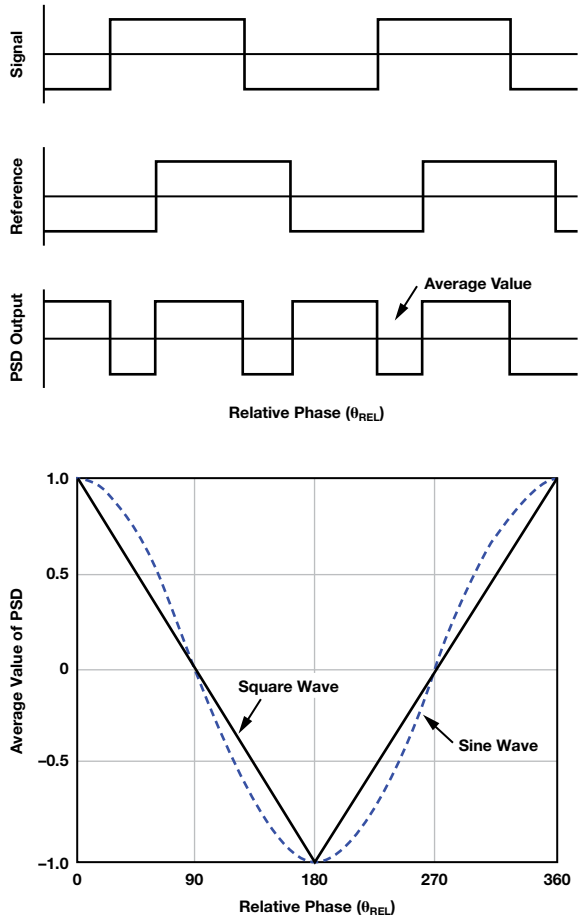

Figure 2. (a) Time domain waveforms of PSD. (b) Average value of PSD output as a function of relative phase.

The sine wave case is less intuitive than the square wave case, but it can be calculated by multiplying term by term and separating into sum and difference components as follows:

$$V_{PSD}(t) = \frac{2\sqrt{2}V_S}{\pi}\cos(f_R \pm f_S \pm \theta_S) - \frac{1}{3}\cos(3f_R \pm f_S \pm \theta_S) + \frac{1}{5}\cos(5f_R \pm f_S \pm \theta_S) - \ldots$$

As desired, the PSD produces a response proportional to the cosine of the relative phase of an input signal at the fundamental frequency, but it also produces a response to every odd harmonic of the signal. With the output filter considered part of the phase-sensitive detector, the signal transmission path looks like a series of band-pass filters centered at the odd harmonics of the reference signal. The bandwidth of the band-pass filters is determined by the bandwidth of the low-pass output filter. The PSD output response is the sum of these band-pass filters, as shown in Figure 3. The part of the response that appears at dc falls in the pass band of the output filter. The part of the response that appears at even harmonics of the reference frequency will be rejected by the output filter.

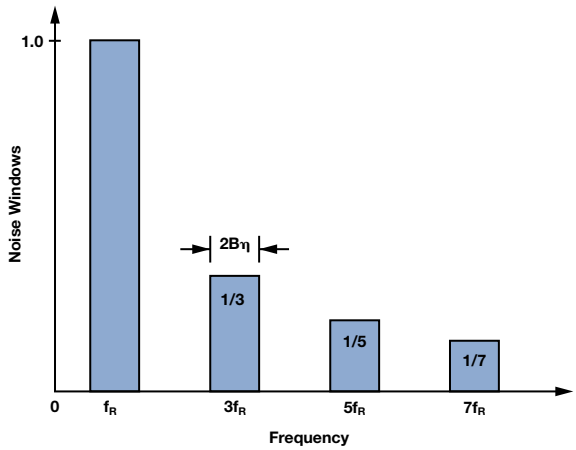

Figure 3. Signal input spectrum that contributes to PSD output.

At first glance, an infinite sum of harmonics aliasing into the output filter pass band seems to doom this approach. However, the impact of the noise aliasing is mitigated because each of the harmonic terms is scaled by a decreasing factor, and the noise at the various harmonics adds as the root sum of squares. We can calculate the noise impact of the harmonic aliasing assuming the noise spectral density of the input signal is constant.

Let V_n be the integrated noise in the transmission window centered at the fundamental frequency. The total rms noise, V_T is

$$V_T = \sqrt{\left(V_n^2 + \left(\frac{V_n}{3}\right)^2 + \left(\frac{V_n}{5}\right)^2 + \ldots\right)} = V_n\sqrt{\left(1^2 + \left(\frac{1}{3}\right)^2 + \left(\frac{1}{5}\right)^2 + \ldots\right)}$$

Using a handy formula for the sum of a geometric series that states

$$\sum_{k=0}^{n} \frac{1}{(2n+1)^2} = \frac{\pi^2}{8} = 1.23$$

the increase in the rms noise due to the harmonic windows is

$$V_T / V_n = \sqrt{\left(1^2 + \left(\frac{1}{3}\right)^2 + \left(\frac{1}{5}\right)^2 + \ldots\right)} = \sqrt{1.23} = 1.11$$

Thus, the rms noise due to all of the harmonic windows increases the total noise by only 11% or 1 dB. The output is still susceptible to disturbers in the pass band of the band-pass filters, and harmonic distortion from either the sensor or electronics before the PSD will cause errors in the output signal. If these harmonic distortion terms are unacceptably large, they can be reduced with an antialiasing filter. The requirements for the antialiasing and output filters will be considered in the following design example.

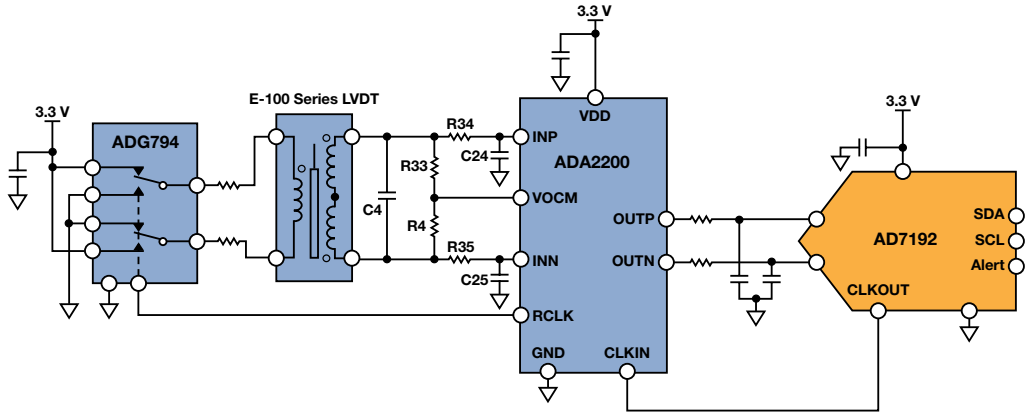

Figure 4. Simplified LVDT position-sensing circuit.

LVDT Design Example

Figure 4 shows a synchronous demodulation circuit that extracts position information from a linear variable displacement transformer (LVDT), which is a specially wound transformer that has a movable core that is affixed to the position to be measured. An excitation signal is applied to the primary. The voltage on the secondary changes in proportion to the position of the core.

There are many types of LVDTs and ways of extracting position from them. This circuit uses the LVDT in 4-wire mode. The two LVDT secondary outputs are connected such that the voltages oppose each other, performing a subtraction. When the LVDT core is in its null position, the voltages on the secondaries are equal, and the difference voltage across the windings is zero. As the core moves from the null position, the difference voltage across the secondary windings increases. The sign of the LVDT output voltage changes based on direction. The LVDT chosen for this example measures a ±2.5 mm, full-scale core displacement. The voltage transfer function is 0.25, which means that the differential output will be 250 mV per volt applied to the primary when the core is displaced 2.5 mm from the center.

Integrated Synchronous Demodulator

The ADA2200 integrated synchronous demodulator uses a unique charge sharing technology to perform discrete time signal processing in the analog domain. Its signal path consists of an input buffer, an FIR decimation filter that performs antialiasing filtering, a programmable IIR filter, a phase-sensitive detector, and a differential output buffer. Its clock generation functions synchronize the excitation signal to a system clock. Programmable features are configured through an SPI-compatible interface.

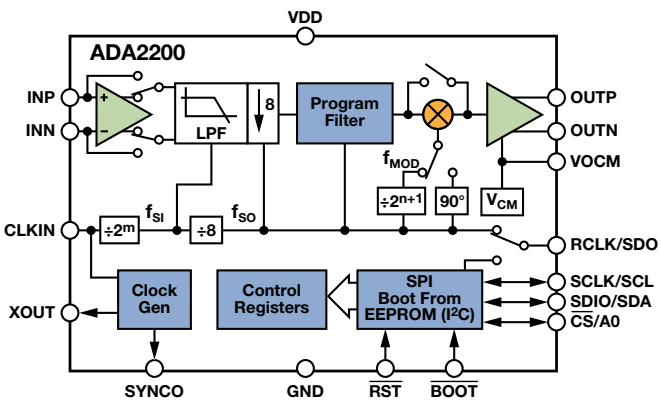

Figure 5. ADA2200 synchronous demodulator.

The 4.92 MHz clock generated by the AD7192 24-bit Σ-Δ ADC is used as the master clock. The ADA2200 generates all of the internal signals it needs for clocking the filters and PSD, as well as generating the excitation signal on the RCLK pin. It divides the master clock by 1024 to generate a 4.8 kHz signal to control the CMOS switch. The CMOS switch converts the low-noise 3.3 V source into a square-wave excitation signal to the LVDT. The 3.3 V supply used for the excitation source is also used as the ADC reference, so any drift in the voltage source will not degrade the measurement accuracy. At full-scale displacement, the LVDT will output a 1.6 V peak-to-peak output voltage.

Antialias Filtering

The RC network between the LVDT output and the ADA2200 input provides low-pass filtering of the LVDT output signal and also produces the relative phase shift required to maximize the demodulator's output signal. Recall from Figure 2b how the maximum PSD output occurs at relative phase shifts of 0° or 180°. The ADA2200 has a 90° phase control that enables ±90° relative phase offsets to be used as well.

Signal energy present at odd multiples of the demodulation frequency will appear in the pass band of the output filter. The FIR decimation filter implements antialiasing filtering, providing a minimum of 50 dB attenuation at these frequencies.

The IIR filter can provide additional filtering or gain if required. Since the IIR filter precedes the phase-sensitive detector, its phase response will affect the PSD signal output bandwidth. This must be taken into account in the design of the filter response.

Output Filter

The pass band of the output filter should be selected to match the bandwidth of the parameter being measured, but limit the broadband noise of the system. The output low-pass filter must also reject output spurs that are created at the even multiples of the PSD.

This circuit uses the LPF inherent in the AD7192 Σ-Δ ADC. It can be programmed to have a $sinc^3$ or $sinc^4$ response, with transfer function zeroes at multiples of the output data rate.

Figure 6 shows the sinc^3 transfer function normalized to the ADC output data rate.

Setting the output data rate of the ADC equal to the demodulation frequency rejects the spurs at the PSD output. The ADC's programmable output data rate acts as a selectable bandwidth output filter. The available output data rates (f_{DATA}) are 4.8 kHz/n, where $1 \le n \le 1023$. Thus, the ADC averages the demodulator output over n demodulation clock periods for each output data value. Because the master clock and the ADC clock are synchronous, the transfer function zeroes of the ADC's output filter will fall directly on every harmonic of the modulation frequency and all of the output spurs will be rejected for any value of n.

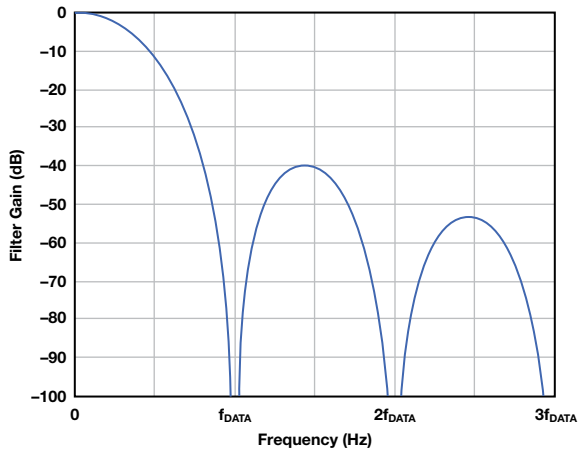

Figure 6. AD7192 sinc3 filter transfer function.

The programmable output data rate enables a straightforward trade-off between noise, and bandwidth/settling time. The output filter has noise bandwidth of $0.3 \times f_{DATA}$; 3 dB frequency of $0.272 \times f_{DATA}$; and settling time of $3/f_{DATA}$.

The ADC digital filter has a 3 dB bandwidth of about 1.3 kHz at the highest output data rate of 4.8 kHz. The RC filter between the demodulator and the ADC is relatively flat up to that frequency to minimize the bandwidth required by the ADC. In systems with lower maximum data rates, the RC filter corner frequency can be reduced proportionally.

Noise Performance

The output noise of the circuit is a function of the ADC output data rate. Table 1 shows the effective number of bits in the digitized data vs. the ADC sample rate assuming a 2.5 V full-scale output voltage. The noise performance is independent of the LVDT core position.

Table 1. Noise Performance vs. Bandwidth

ADC Data Rate (SPS)	Output Bandwidth (Hz)	ENOB (rms)	ENOB (p-p)
4800	1300	13.8	11.3
1200	325	14.9	12.3
300	80	15.8	13.2
75	20	16.2	13.5

If the output noise from the ADA2200 were frequency independent, the expected effective number of bits would increase by one bit for every 4× decrease in the output data rate. The ENOB doesn't increase as much at the lower output data rates due to the ADA2200 output driver's 1/f noise, which begins to dominate the noise floor at the lower output data rates.

Linearity

The linearity was measured by first performing a two-point calibration at core displacements of ±2.0 mm. From these measurements, the slope and offset were determined to establish a best straight line fit. Next, measurements were taken at core displacements across the ±2.5 mm full-scale range. The measured data was subtracted from the straight line data to determine the linearity error.

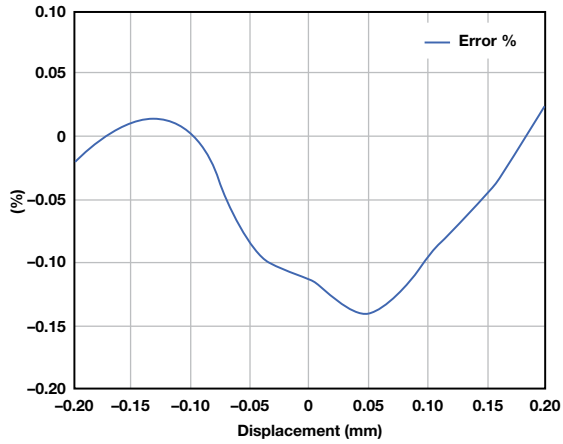

Figure 7. Position linearity error vs. LVDT core displacement.

The E Series LVDT used for the circuit evaluation specifies ±0.5% linearity over the ±2.5 mm displacement range. The circuit performance exceeds the LVDT specifications.

Power Consumption

The circuit consumes a total of 10.2 mW, including 6.6 mW for driving the LVDT and 3.6 mW for the remainder of the circuit. The circuit SNR could be improved by increasing the LVDT excitation signal at the cost of increased power consumption. Alternatively, the power consumption can be reduced by lowering the LVDT excitation signal and using a low power, dual op amp to amplify the LVDT output signal to preserve the circuit's SNR.

Conclusion

Many sensor signal conditioning challenges share characteristics that can be addressed with synchronous demodulation. Systems with excitation frequencies below 1 MHz and dynamic range requirements in the 80-dB-to-100-dB range can be addressed with low cost, low power analog circuits requiring minimal digital post processing. Understanding the operation of the phase-sensitive detector and the likely noise characteristics at the output of the sensor are key to determining the system filter requirements.

(continued on Page 23)

No Pain, High Gain: Building a Low Noise Instrumentation Amplifier with Nanovolt Sensitivity

By Moshe Gerstenhaber, Rayal Johnson, and Scott Hunt

Introduction

Building a voltage measurement system with nanovolt sensitivity presents many design challenges. The best available op amps, such as the ultralow noise AD797, can achieve less than 1 nV/√Hz noise at 1 kHz, but the nature of low frequency noise limits the achievable noise to about 50 nV p-p over a 0.1 Hz to 10 Hz band. Oversampling and averaging can reduce the rms contribution from flat band noise at the expense of a higher data rate and additional power, but oversampling does not reduce the noise spectral density and it has no effect on noise in the 1/f region. Furthermore, large front-end gain is needed to avoid noise contribution from subsequent stages, reducing system bandwidth. Without isolation, any ground bounce or interference will also appear at the output, where it may overwhelm the low intrinsic noise of the amplifier and its input signal. A well behaved low noise instrumentation amplifier (in-amp) simplifies the design and construction of such a system, and reduces residual errors due to common-mode voltage, power supply fluctuations, and temperature drift.

The AD8428 low noise in-amp provides a precise gain of 2000 and has all of the features required to solve these problems. With 5 ppm/°C max gain drift, 0.3 μV/°C max offset voltage drift, 140 dB min CMRR to 60 Hz (120 dB min to 50 kHz), 130 dB min PSRR, and a 3.5 MHz bandwidth, the AD8428 is ideally suited to low level measurement systems.

Most significantly, the 1.3 nV/√Hz voltage noise at 1 kHz and the industry-best 40 nV p-p noise from 0.1 Hz to 10 Hz enable high signal-to-noise ratio with very small signals. Two additional pins enable designers to change the gain or add a filter to reduce the noise bandwidth. These filter pins also provide a unique way to reduce the noise.

Using Multiple AD8428 In-Amps to Lower System Noise

Figure 1 shows a circuit configuration that further reduces the system noise. The inputs and filter pins of four AD8428s are shorted together, reducing the noise by a factor of 2.

The output can be taken from any one of the in-amps to maintain low output impedance. This circuit can be extended, dividing the noise by the square root of the number of amplifiers used.

How the Circuit Reduces Noise

The 1.3 nV/√Hz typical referred-to-input (RTI) spectral noise generated by each AD8428 is uncorrelated with the noise generated by the other amplifiers. The uncorrelated noise sources add as the root-sum-of-squares (RSS) at the filter pins. The input signal, on the other hand, is positively correlated. Each AD8428 generates the same voltage at its filter pins in response to the signal, so connecting multiple AD8428s doesn't change the voltage, and the gain remains 2000.

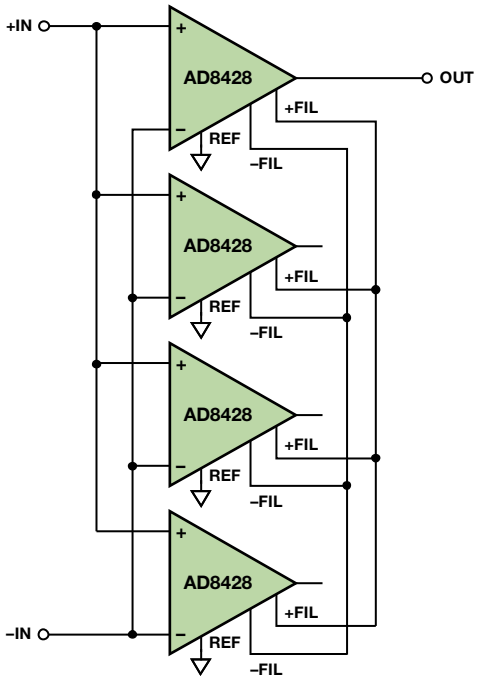

Figure 1. Noise reduction circuit uses four AD8428 in-amps.

Noise Analysis

The following analysis of the simplified version of the circuit in Figure 2 shows that two AD8428s connected this way reduces the noise by a factor of $\sqrt{2}$. The noise of each AD8428 can be modeled at its +IN pin. To determine the total noise, ground the inputs and use superposition to combine the noise sources.

Noise source e_{n1} gets amplified by a differential gain of 200 to the output of preamplifier A1. For this part of the analysis, the outputs of preamplifier A2 are noiseless with grounded inputs. The 6 kΩ/6 kΩ resistor divider from each output of Preamplifier A1 to the corresponding output of Preamplifier A2 can be replaced by its Thévenin equivalent: half of the noise voltage at the output of Preamplifier A1 with a 3 kΩ series resistor. This division is the mechanism that reduces the noise. The full nodal analysis shows that the output voltage in response to e_{n1} is $1000 \times e_{n1}$. By symmetry, the output voltage in response to noise voltage e_{n2} is $1000 \times e_{n2}$. The magnitude of e_{n1} and e_{n2} are both equal to e_n, and will add as RSS, causing an overall output noise of $1414 \times e_n$.

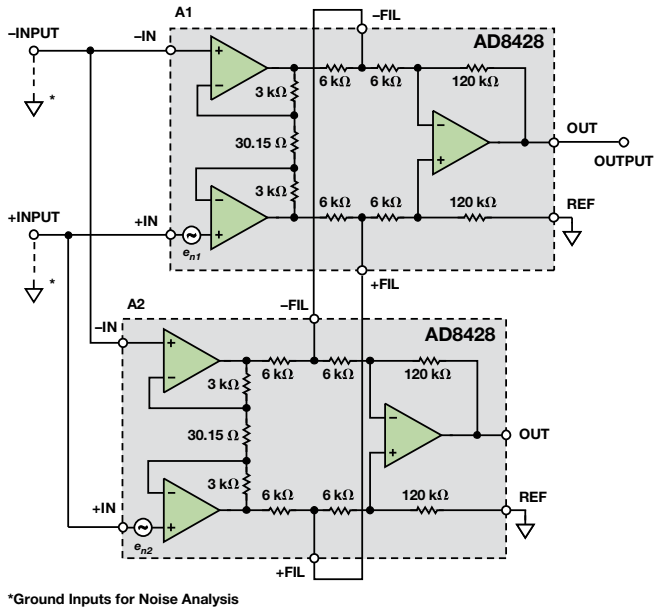

Figure 2. Simplified circuit model for noise analysis.

In order to refer this back to the input, the gain must be verified. Assume a differential signal V_{IN} is applied between +INPUT and –INPUT. The differential voltage at the output of the first stage of A1 will be $V_{IN} \times 200$. The same voltages appear at the outputs of Preamplifier A2, so there is no signal division through the 6 kΩ/6 kΩ divider, and nodal analysis shows an output of $V_{IN} \times 2000$. Thus, the total voltage noise RTI is $e_n \times 1414/2000$, or equivalently $e_n/\sqrt{2}$. Using the 1.3 nV/$\sqrt{\text{Hz}}$ typical noise density of the AD8428, the two amplifier configuration yields a noise density of about 0.92 nV/$\sqrt{\text{Hz}}$.

With additional amplifiers, the impedance at the filter pin changes, reducing the noise further. For example, using four AD8428s as shown in Figure 1, the 6 kΩ resistor from the preamplifier output to the filter pin is followed by three 6 kΩ resistors to each of the noiseless preamplifier outputs. This effectively creates a 6 kΩ/2 kΩ resistor divider, dividing the noise by four. The total noise of all four amplifiers then becomes $e_n/2$, as predicted.

Making the Noise vs. Power Trade-Off

The main trade-off is power consumption vs. noise. The AD8428 has very high noise-to-power efficiency, with input noise density of 1.3 nV/$\sqrt{\text{Hz}}$ for 6.8 mA maximum supply current. For comparison, consider the low noise AD797 op amp, which requires 10.5 mA maximum supply current to achieve 0.9 nV/$\sqrt{\text{Hz}}$. A discrete G = 2000, low noise in-amp built with two AD797 op amps and a low power difference amplifier could use more than 21 mA to achieve 1.45 nV/$\sqrt{\text{Hz}}$ noise RTI, contributed by the two op amps and a 30.15 Ω resistor.

In addition to the power supply considerations of using many amplifiers in parallel, the designer must also consider the thermal environment. A single AD8428 with a ±5 V supply will have a temperature rise of about 8°C due to internal power dissipation. If many devices are placed close together or in an enclosed space, they can mutually heat one another, and thermal management techniques should be considered.

Simulation with SPICE

Although it should not be used as a substitute for prototyping, circuit simulation with SPICE can be a useful first step in validating circuit ideas such as this. To verify this circuit, the ADIsimPE simulator and the AD8428 SPICE macro model were used to simulate the circuit performance with two devices in parallel. The results shown in Figure 3 demonstrate the expected behavior: a gain of 2000 and 30% lower noise.

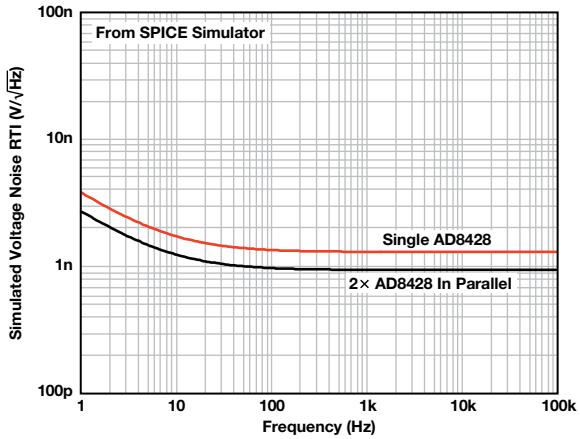

Figure 3. SPICE simulation results.

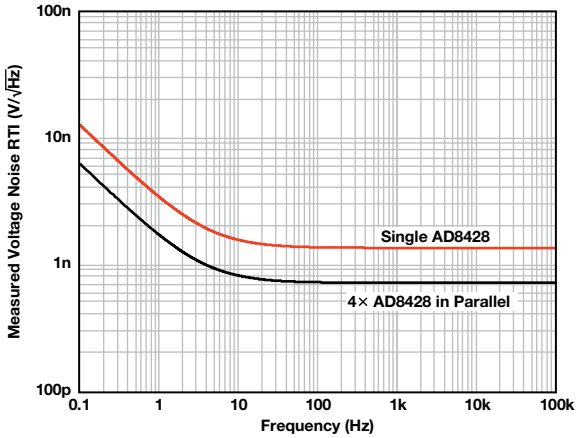

Figure 4. Measured voltage noise spectrum of circuit shown in Figure 1.

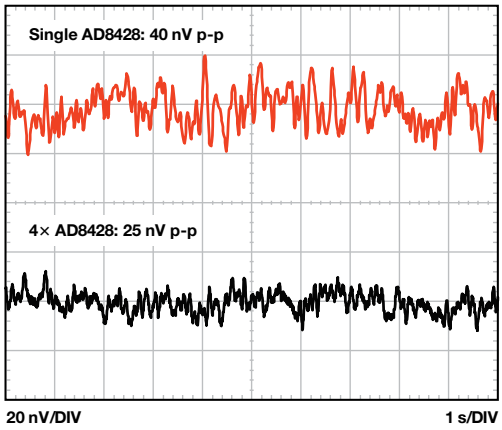

Figure 5. Measured 0.1 Hz to 10 Hz RTI noise of circuit shown in Figure 1.

Measurement Results

The full circuit with four AD8428s was measured on the bench. The measured RTI noise has a spectral density of 0.7 nV/√Hz at 1 kHz and 25 nV p-p from 0.1 Hz to 10 Hz. This is lower than the noise of many nanovoltmeters. The measured noise spectrum and peak-to-peak noise are shown in Figure 4 and Figure 5, respectively.

Conclusion

Nanovolt sensitivity is a difficult goal that presents many design challenges. For systems that require low noise and high gain, the AD8428 in-amp has the features required to implement a high performance design. Furthermore, its unique configuration allows it to add this unusual circuit to the nanovolt toolbox.

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Versatile, Low-Power, Precision Single-Ended-to-Differential Converter

Volume 46, Number 4

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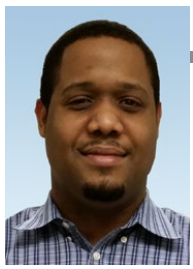

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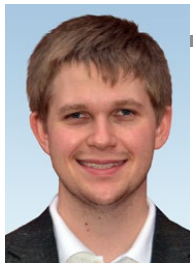

Scott Hunt

Also by this Author:

How to Stay out of Deep Water when Designing with Bridge Sensors

Volume 48, Number 1

RF Sampling ADC Input Protection: Not Black Magic After All

By Umesh Jayamohan

Introduction

The design of the input, or front end, of any high performance analog-to-digital converter (ADC), especially an RF sampling ADC, is critical to achieving the desired system-level performance. In many cases, the RF sampling ADC digitizes a signal bandwidth of hundreds of megahertz. The front end can be active (using an amplifier) or passive (using transformers or baluns) depending on the system's requirements. In either case, the components must be carefully chosen to provide optimum ADC performance in the frequency band of interest.

RF sampling ADCs are fabricated using deep submicron CMOS process technology, and the physics of semiconductor devices tells us that smaller transistor geometries support lower maximum voltages. Hence, the data sheet specifies the absolute maximum voltages that should not be exceeded due to reliability reasons. Comparing data sheets from older devices with those of state-of-the-art RF sampling ADCs demonstrates this decrease in voltage.

In receiver applications where the ADC digitizes the input signal, systems designers must pay careful attention to the absolute maximum input voltage. This parameter directly affects the ADC's lifetime performance and reliability. An unreliable ADC would render the entire radio system useless, and the cost of replacing it could be substantial.

To counter the risk from overvoltage stress, RF sampling ADCs include circuitry that detects high thresholds, allowing the receiver to compensate by adjusting the gain with an automatic gain control (AGC) loop. With a pipelined ADC, however, the inherent latency associated with the architecture can briefly expose the input to a high level, potentially harming the ADC inputs. This article discusses a simple method that can augment the AGC loop to protect the ADC.

Input Architectures

RF sampling ADCs are implemented with several different designs, the most common being the pipelined architecture, which cascades several stages to convert the analog signal to digital. The first stage, which is the most critical, can be buffered or unbuffered. The choice of which to use depends on design requirements and performance targets. For example, a buffered ADC usually offers better SFDR across frequency but consumes more power than an unbuffered ADC.

The front-end design will also change according to whether the ADC is buffered or unbuffered. The additional series resistance needed for unbuffered ADCs to handle the input charge kickback would also improve SFDR performance. Figure 1 and Figure 2 show simplified equivalent input circuits of the AD9625 unbuffered and AD9680 buffered RF sampling ADCs. Only the single-ended inputs are shown for simplicity.

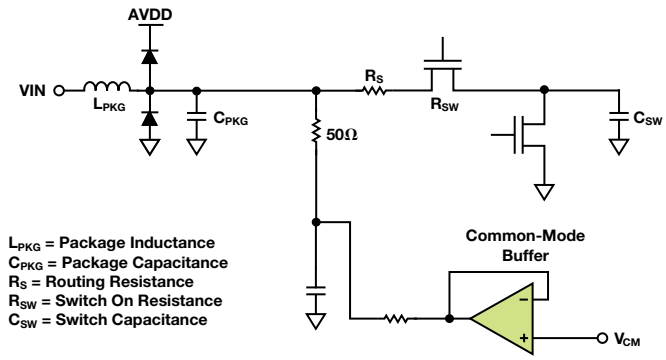

Figure 1. Equivalent circuit of an unbuffered RF sampling ADC input.

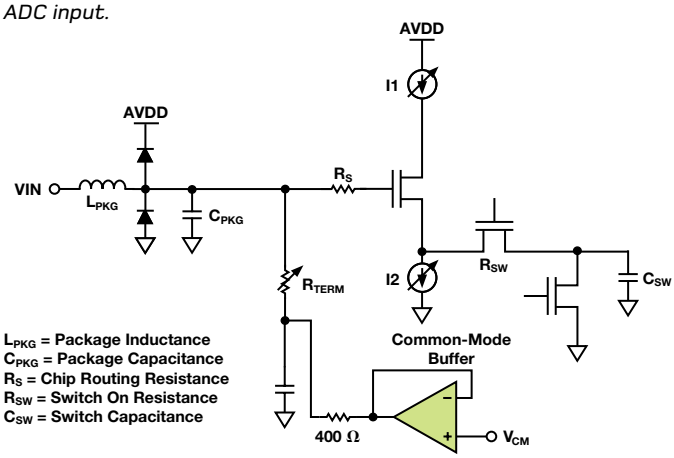

Figure 2. Equivalent circuit of a buffered RF sampling ADC input.

Regardless of the architecture, the absolute maximum voltage sustainable at the inputs of the ADC is governed by the voltages the MOSFETs can handle. The buffered input is more complex and burns more power than the unbuffered input. ADCs employ several different kinds of buffers, the most common of which is a source follower.

Failure Mechanisms

The failure mechanism will differ for buffered and unbuffered ADCs, but failure usually occurs when the maximum allowable gate source voltage (V_{GS}) or drain source voltage (V_{DS}) is exceeded. These voltages are illustrated in Figure 3.

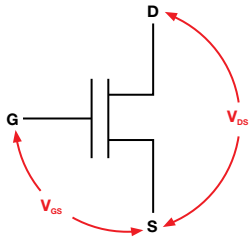

Figure 3. Critical voltages for MOS transistor.

For example, if V_{DS} exceeds the maximum allowable voltage, it causes a V_{DS} breakdown failure, which usually occurs when the MOSFET is in the off state and an excessive voltage is applied to the drain with respect to the source. If V_{GS} exceeds the maximum allowable voltage, it causes a V_{GS} punch through, also known as oxide breakdown. This usually happens when the MOSFET is on and an excessive voltage is applied to the gate with respect to the source.

Failure Mechanism in an Unbuffered ADC

Figure 4 shows an unbuffered ADC input. The sampling process is controlled by out-of-phase clock signals Φ and $\overline{\Phi}$, which are the sample/hold signal for MOSFET M1 and the reset signal for MOSFET M2. When M1 is on, M2 is off, and capacitor C_{SW} tracks the signal (sample or track mode). When M1 is off, M2 turns on after the comparators in the MDAC have made a decision, resetting the capacitor C_{SW}. This prepares the sampling capacitor for the next sample during the sampling phase. This circuit normally works like a well-oiled machine.

High voltage inputs, however, expose the circuit to stresses that violate the drain source voltage limit for M2. When a high voltage input is sampled (M1 is on, M2 is off), M2 is exposed to a large V_{DS}. M2 is off for less than one-half cycle of the sampling clock, but even this transient exposure can deteriorate the reliability of the circuit and render the ADC useless over time. M1 is exposed to a large V_{DS} when in reset mode (M1 off, M2 on), as the input signal is present on its drain.

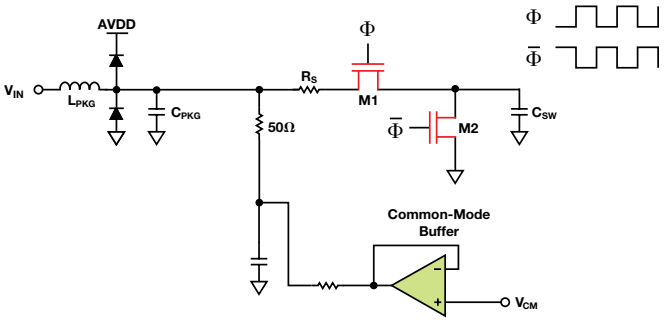

Figure 4. Failure mode in an unbuffered ADC input.

Failure Mechanism in a Buffered ADC

Figure 5 shows a buffered ADC input. The same clock scheme applies for the sampling and reset signals. Regardless of the phase, when the gate of Buffer M3 is exposed to a high voltage input, it stresses the circuitry that creates currents I1 and I2. Current Source I1 is implemented with a PMOS transistor, whereas I2 is implemented with an NMOS transistor. A high voltage at the gate of M3 causes excessive V_{DS} on both I1 and I2 MOSFETs. In addition, a high voltage on the gate of M3 can result in oxide breakdown (punch through).

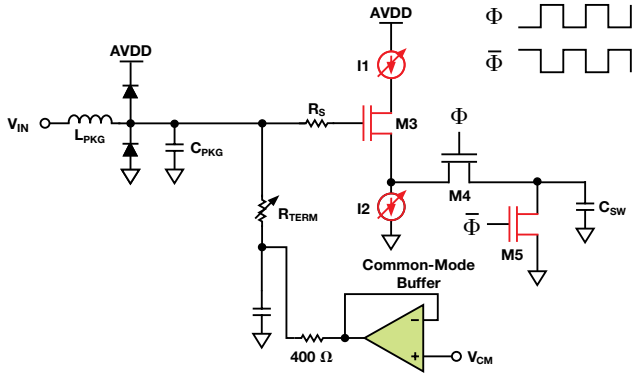

Figure 5. Failure mode in a buffered ADC input.

The breakdown mechanisms are different for buffered and unbuffered ADCs, so the absolute maximum input voltage also differs as shown in Table 1.

Table 1. Absolute Maximum Specifications for Buffered and Unbuffered ADCs

ADC	Process Node (nm)	Input Structure	Absolute Maximum Input Voltage (V)	Differential Swing (V p-p)
14-bit 105 MSPS	350	Buffered	7	9.2
14-bit 125 MSPS	180	Unbuffered	2.0	4.5
16-bit 250 MSPS	180	Buffered	3.6	6.0
12-bit 2.5 GSPS	65	Unbuffered	1.52	4
14-bit 1.0 GSPS	65	Buffered	3.2	4.6

ADC Input Protection Using a TVS Diode

ADC inputs can be protected against high voltages in several ways. Some ADCs, including RF sampling ADCs in particular, have built-in circuitry that detects and reports when programmed thresholds have been crossed. This fast detect output has some latency, as specified in the data sheet, so it still leaves the ADC inputs exposed for a short time.

The excess voltage can be limited by transient voltage stabilizer (TVS) diodes, but they compromise ADC performance during normal operation. Figure 6 shows a circuit that uses TVS diodes to protect against overvoltage conditions.

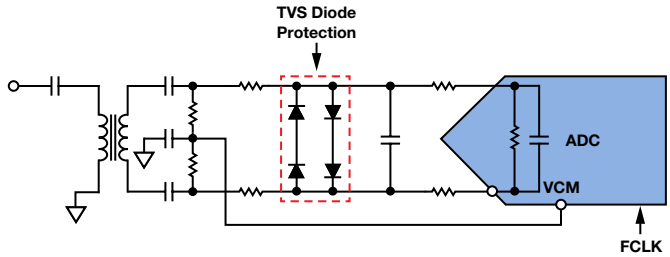

Figure 6. ADC front-end circuit with TVS diode protection.

Although the TVS diodes protect the ADC inputs by clamping the excess voltage, they severely degrade the harmonic performance. Figure 7 shows a comparison FFT of a 14-bit, 250 MSPS bufferless ADC with a 30 MHz, –1 dBFS input with and without the TVS diode in the front end.

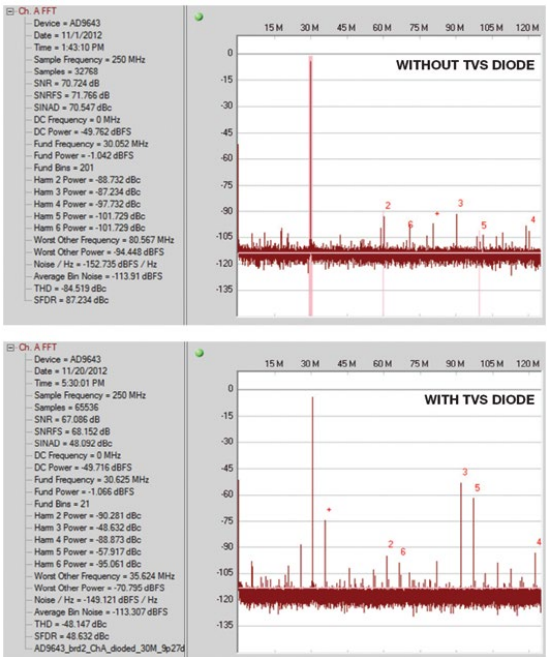

Figure 7. FFT comparison of ADC front-end circuit with and without TVS diode protection.

The TVS diodes especially degrade the odd harmonics because they act as reverse-biased diodes when not clamping. This PN diode has a junction capacitance, C_{J0}, that interacts with the nonlinear kickback current generated by the switching action inside the ADC to create a voltage that mixes with the analog input signal. The mixed-signal gets sampled inside the ADC and generates a significant third-order harmonic. A time domain plot of the overvoltage condition (Figure 8) shows the clipping action of the TVS diodes. This doesn't mean that the TVS diode is unsuitable for ADC input protection, but only that the diode specifications must be carefully considered so as to obtain the required performance. A more thorough look is needed in selecting the type of diode and its parameters.

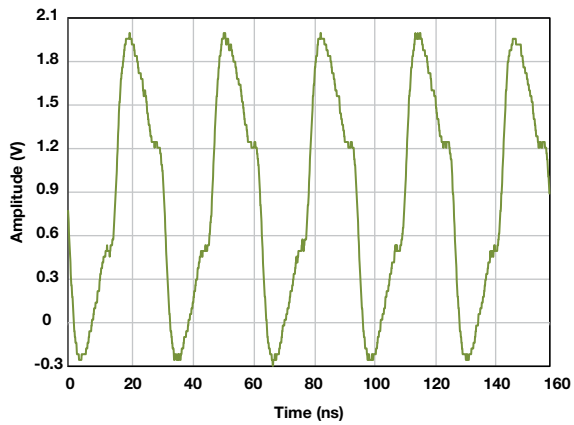

Figure 8. Clipped signal due to TVS diode protection in front-end circuit.

Protection of RF Sampling ADC Inputs Using Schottky Diodes

As bandwidths and sample rates have hit the GHz and GSPS range, RF sampling ADCs simplify radio receiver designs because they do not require as many mixing stages in front of the ADC, but this leaves the ADC inputs vulnerable to overvoltage stresses. Figure 9 shows a typical amplifier driven front-end design for an RF sampling ADC. The new generation of amplifiers specifically designed to interface with these ADCs have a fast attack input, which can be configured via the serial peripheral interface (SPI) to attenuate the outputs to a predetermined gain. The fast attack pin can be configured to respond to the fast detect output from the RF sampling ADC. The ADA4961 is an example of the new generation of amplifiers with the fast attack feature. The AD9680 and AD9625 are examples of RF sampling ADCs that have the fast detect feature.

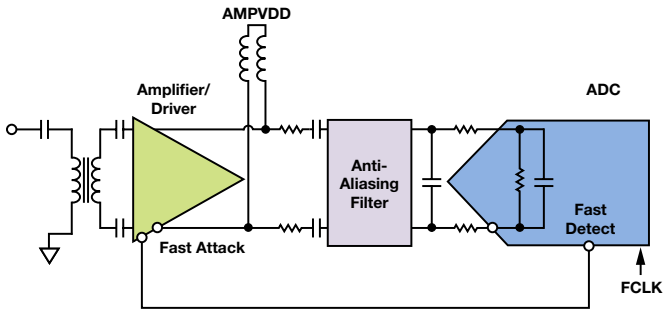

Figure 9. Amplifier with fast attack driving RF sampling ADC with fast detect.

The topology of Figure 9 is good as long as the input voltages are within range. If, for example, this receiver path is exposed to a sudden burst of high voltage at the input, the outputs are going to rise to the voltage of the amplifier's supply rail (5 V, in this case). This presents a huge swing in excess of the absolute maximum rated voltage at the inputs of the ADC. The fast detect has some latency (28 clock cycles or 28 ns for the AD9680-1000), so by the time the fast detect logic output tells the amplifier to assert a fast attack, the ADC has already been exposed to the high voltage for a few clock cycles. This might degrade the ADC's reliability, so system designs that can't tolerate this risk will need a secondary mode of protection. A fast-acting Schottky diode with very low device and parasitic capacitance is useful in these situations. Key parameters for specifying the diode can be found in the data sheet.

Reverse breakdown voltage (V_{BR})—the maximum input voltage at the AD9680 input pins—is about 3.2 V relative to AGND, so a reverse breakdown voltage of 3 V is chosen for the diode.

Junction capacitance (C_{J0})—the diode capacitance should be as low as possible to ensure that the diode does not affect the ADC's ac performance (SNR/SFDR) during normal operation.

Figure 10 shows a passive front end with a Schottky diode inserted in front of the ADC. The passive front end makes it easy to demonstrate that the Schottky diode can protect the ADC inputs without compromising the ac performance.

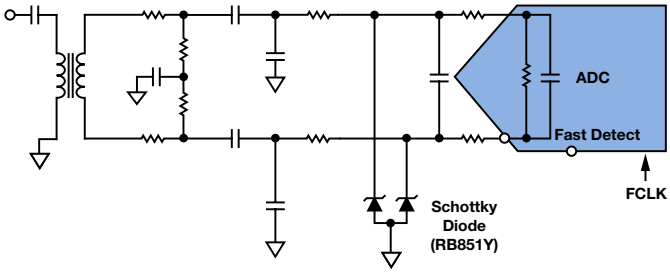

Figure 10. Passive front-end circuit showing RF sampling ADC and Schottky diode.

The RF sampling ADC was tested to input frequencies up to 2 GHz, so an RF Schottky diode was chosen (RB851Y). Table 2 shows the key parameters of the RB851Y that make it suitable for the application. Tests were conducted to show that the diodes prevented the ADC inputs from exceeding the absolute maximum voltage rating of 3.2 V with respect to AGND. Figure 11 shows a single-ended input (VIN+ pin of the ADC) exposed to a high voltage at 185 MHz. The Schottky diode clamps the voltage to around 3.0 V relative to AGND, preventing the ADC inputs from reaching the 3.2 V limit. Figure 12 shows a differential signal at the input of the AD9680 being clipped by the Schottky diodes.

Table 2. Key Parameters for the Schottky Diode Used to Protect RF Sampling ADC Inputs

Parameter	Value	Unit	Comments
Reverse voltage (V_R)	3	V	Absolute maximum rating at VIN± = 3.2 V per AD9680 data sheet
Capacitance between terminals (C_{J0}, or Ct)	0.8	pF	Less impact on ADC performance under normal conditions

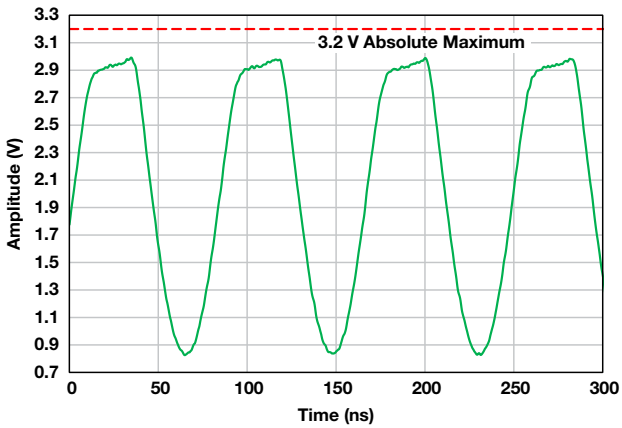

Figure 11. Single-ended ADC input being clipped by the Schottky diode.

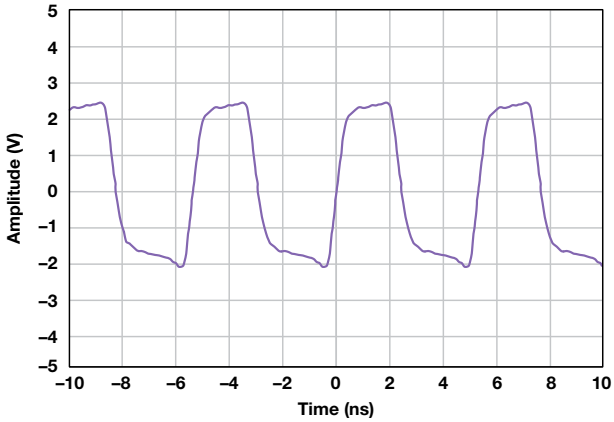

Figure 12. AD9680 differential inputs clipped by Schottky diodes.

Next, we measured performance during normal operation. The AD9680 was controlled as per data sheet recommendations, but the inputs were modified as shown in Figure 10. The analog input frequency was varied from 10 MHz to 2 GHz. The ultralow value of C_{J0} should not impact the ADC's SNR and SFDR performance.

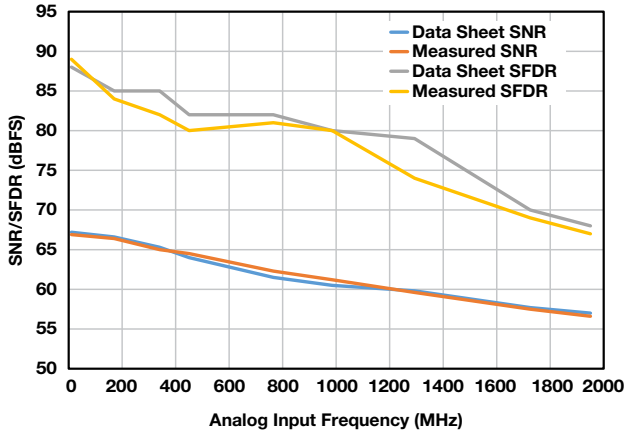

Figure 13. SNR/SFDR vs. analog input frequency for AD9680 with Schottky diode protection.

The Schottky diodes do not affect the SNR at all, but the SFDR deviates from the expected value at some frequencies, as shown in Figure 13. This may be caused by a mismatch in the differential signal or kickback from the ADC. The evaluation board is designed for a wide band, from dc to 2 GHz, so while it does a good job overall across the entire band, some components may interact with the Schottky diodes at certain frequencies.

Most applications do not use the entire 2 GHz band, so it is possible to tune the front end to the required signal bandwidth of interest by modifying the input for overvoltage protection. Careful selection of the Schottky diode can protect the ADC inputs, allowing a system designer to implement an amplifier driven front-end circuit using the latest fast attack and fast detect features, as shown in Figure 14.

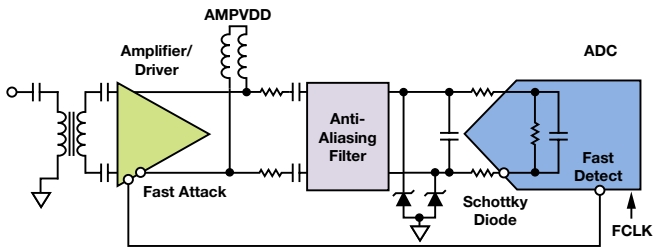

Figure 14. ADA4961 driving the AD9680 showing RF sampling ADC and Schottky diodes.

Conclusion

This article demonstrated the use of a Schottky diode to protect the inputs of an RF sampling ADC against overvoltage stresses. Careful scrutiny of the diode's data sheet is key. A plan to accommodate this circuitry is required to achieve optimal performance in the band of interest. The fast detect output of an RF sampling ADC can communicate with the fast attack input of the latest amplifiers to set the automatic gain control loop.

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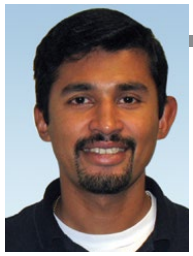

Umesh Jayamohan

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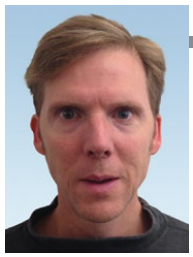


Brian Harrington

Liquid Level Sensing Using Capacitive-to-Digital Converters

By Jiayuan Wang

Introduction

Procedures such as infusions and transfusions require exact amounts of liquid to be monitored, so they need an accurate, easy-to-implement method for sensing liquid level. This article describes the 24-bit capacitive-to-digital converters and level-sensing techniques that enable high performance capacitive sensing of liquid levels.

Capacitance Measurement Basics

Capacitance is the ability of a body to store electrical charge. The capacitance, *C*, is given by

$$C = \frac{Q}{V}$$

where *Q* is the charge on the capacitor and *V* is the voltage across the capacitor.

In the capacitor shown in Figure 1, two parallel metal plates with area *A* are separated by distance d. The capacitance, *C*, is

$$C = \varepsilon_O \times \varepsilon_R \frac{A}{d}$$

where

- *C* is the capacitance in Farads
- *A* is the area of overlap of the two plates = a × b
- *d* is the distance between the two plates
- ε_R is the relative static permittivity
- ε_O is the permittivity of free space ($\varepsilon_O \approx 8.854 \times 10^{-12}$ F m^{-1})

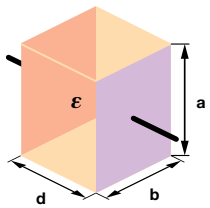


Figure 1. Capacitance of two parallel plates.

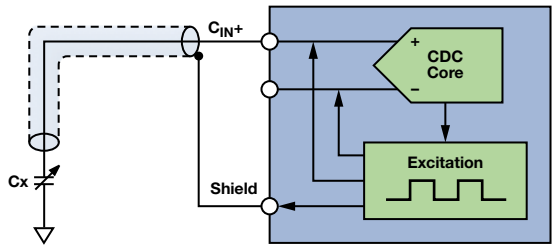
Capacitance-to-Digital Converter (CDC)

The single-channel AD7745 and two-channel AD7746 high resolution, Σ-Δ capacitance-to-digital converters measure capacitances connected directly to their inputs. Featuring inherently high resolution (21-bit effective resolution and no missing codes at 24 bits), high linearity (±0.01%), and high accuracy (±4 fF factory calibrated), they are ideal for sensing levels, position, pressure, and other physical parameters.

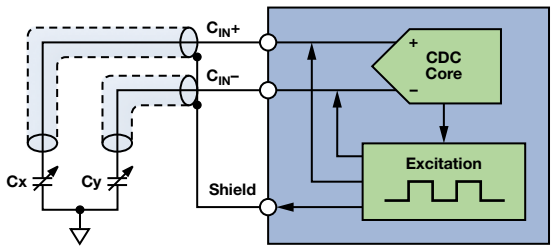
Functionally complete, they integrate a multiplexer, an excitation source, switched capacitor DACs for the capacitive inputs, a temperature sensor, a voltage reference, a clock generator, control and calibration logic, an I²C-compatible serial interface, and a high-precision converter core, which includes a second-order Σ-Δ charge-balancing modulator and a third-order digital filter. The converter works as a CDC for capacitive inputs and as an ADC for voltage inputs.

The measured capacitance, C_x, is connected between the excitation source and the Σ-Δ modulator input. A square wave excitation signal is applied to C_x during the conversion. The modulator continuously samples the charge going through the C_x and converts it to a stream of 0s and 1s. The digital filter processes the modulator output to determine the capacitance, which is represented by the density of 1s. The filter output is scaled by calibration coefficients. The external host can then read the final result via the serial interface.

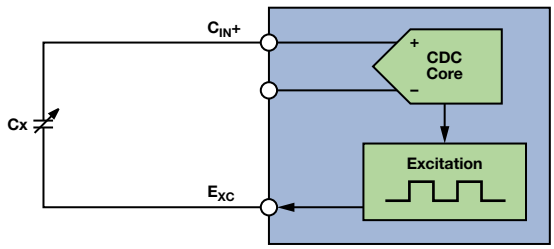
The four configurations shown in Figure 2 demonstrate how the CDC senses capacitance in single-ended, differential, grounded, and floating sensor applications.



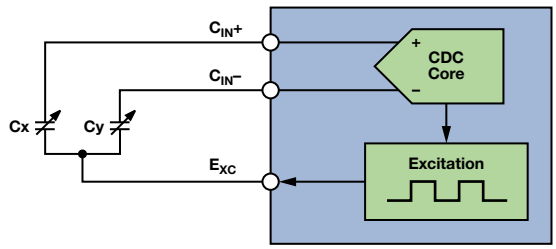
(a) Single-Ended Grounded Sensor



(b) Differential Grounded Sensor



(c) Single-Ended Floating Sensor



(d) Differential Floating Sensor

Figure 2. Configurations for single-ended, differential, grounded, and floating sensor applications.

Capacitive Level-Sensing Techniques

A simple technique for monitoring liquid levels is to immerse a parallel plate capacitor in the liquid, as shown in Figure 3. As the liquid level changes, the amount of dielectric material between the plates changes, which causes the capacitance to change as well. A second pair of capacitive sensors (shown as C_2) is used as a reference.

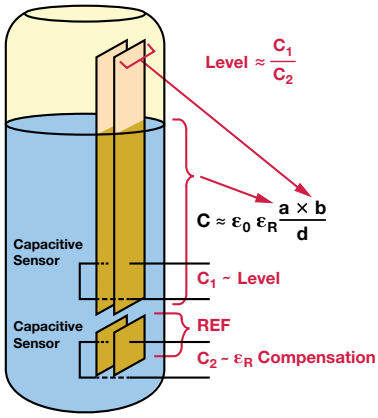


Figure 3. Capacitive level sensing.

Since $\varepsilon_{R(Water)} >> \varepsilon_{R(Air)}$, the capacitance of the sensor can be approximated by the capacitance of the submerged section. Thus, the level of the liquid can be calculated as C_1/C_2:

$$C_1 \approx \varepsilon_O \varepsilon_R \frac{Level \times b}{d}$$

$$C_2 \approx \varepsilon_O \varepsilon_R \frac{Ref \times b}{d}$$

$$Level \approx \frac{C_1}{C_2}$$

where

- *Level* is the length submerged into liquid
- *Ref* is the length of the reference sensor

Capacitive Level-Sensing System Hardware

With its two capacitance measurement channels, the 24-bit AD7746 is ideally suited for level-sensing applications. Figure 4 shows the system block diagram. The sensor and reference capacitances are converted to digital and the data is transmitted via the I²C port to the host PC or microcontroller.

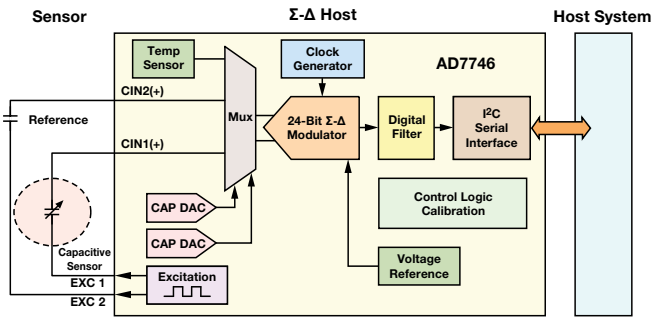


Figure 4. Capacitive level-sensing system.

The PCB design is critical for accurate measurements. Figure 5 shows the sensor board and CDC connection. To maintain accuracy, the AD7746 is mounted on the top surface of the PCB as close as possible to the two metal plates inside the 4-layer PCB. The ground plane is exposed on the back side of the PCB. Both input channels are used in the application. The sensor board is shown in Figure 6.

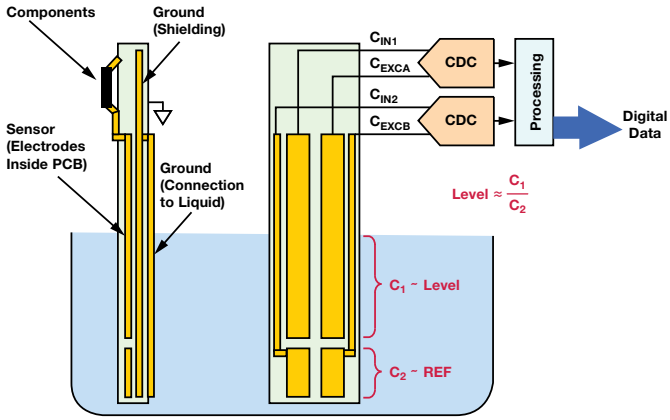


Figure 5. Sensor board and CDC connection.

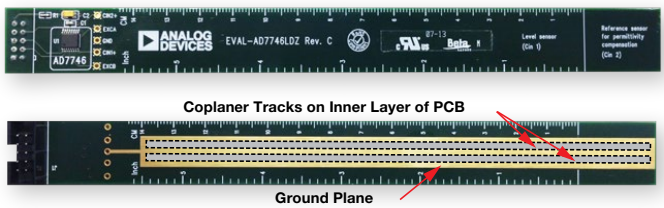


Figure 6. Picture for top-side and bottom-side PCB.

The sensor board is designed using two coplanar metal plates instead of two parallel plates. With parallel plates on a PCB, the dielectric is formed by the PCB material, air, and liquid. In contrast, the inner coplanar layer doesn't have to contact the liquid directly. For coplanar plates the approximate capacitance per length of track is

$$\frac{C}{l} = \frac{\pi \varepsilon_{R(eff)} \varepsilon_O}{ln\left(\frac{\pi(d-w)}{w+t} + 1\right)}$$

where

- d is the distance between the midpoints of the two parallel tracks
- l is the length of the tracks
- w is the width of each track (assuming they are the same)
- t is the thickness of the track
- The effective ε_R is determined by the ratio of d to h (h is the thickness of the PCB board)
  - For $d/h >> 1$; $\varepsilon_{R(eff)} \approx 1$
  - For $d/h \approx 1$; $\varepsilon_{R(eff)} = (1 + \varepsilon_R)/2$

From this equation, the measured capacitive is proportional to the length submerged into water, as the approximate capacitance per length of track for a coplanar sensor remains constant. Performing system calibration using LabVIEW® software can help achieve higher accuracy.

LabVIEW Software

A LabVIEW program running on the PC retrieves data from the CDC via the I²C serial interface. Figure 7 shows the graphical user interface (GUI) on the PC monitor. When the liquid level demonstration system is on, the real-time level data, ambient temperature, and supply voltage are displayed.

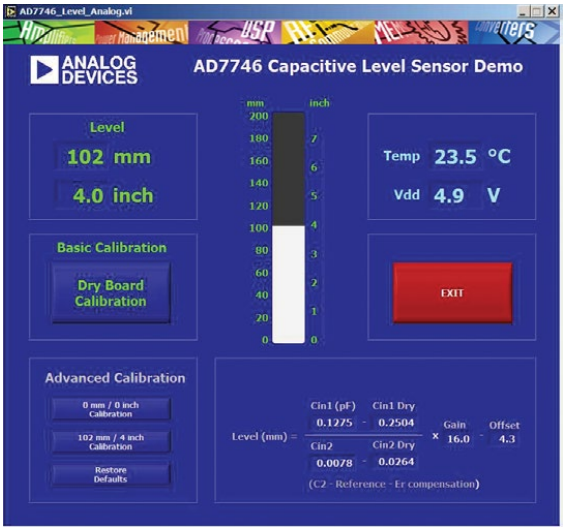


Figure 7. System GUI shown on PC monitor.

The level of liquid is derived as

$$Level = \frac{C_1 - C_{1DRY}}{C_2 - C_{2DRY}} \times Gain - Offset$$

The LabVIEW program includes basic calibration and advanced calibration to achieve a more accurate measurement. Dry (basic) calibration is used to determine C_{1DRY} and C_{2DRY}. The gain and offset can be derived from 0" and 4" calibration, since each calibration determines one equation with two first-order unknowns. The reference capacitor must be submerged into liquid during the calibration and measurement processes.

Conclusion

This article provides an introduction to the capacitive liquid-level sensing demonstration system.

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