Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing • Volume 50, Number 2, 2016

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Editor's Notes

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Practical Filter Design Challenges and Considerations for Precision ADCs

Precision analog-to-digital converters are popularly used in many applications, such as instrumentation and measurement, PLM, process control, and motor control. Current SAR ADCs go up to 18-bit or even higher resolution at x-MSPS, while Σ-Δ ADCs can be 24- or 32-bit resolution at hundreds of kSPS. It is critical that users limit their signal chain noise in order to achieve the rated performance of these high performance, high resolution converters. This article discusses the design challenges and considerations associated with implementing the analog and digital signal chain filters necessary in managing signal noise. (Page 3)

Replacing Discrete Protection Components with Overvoltage Fault Protected Analog Switches

The challenge of designing robust electronic circuitry often results in a design with a multitude of discrete protection components with associated cost, design time, and space additions. This article examines a fault protected switch architecture, along with the performance benefits and other advantages it offers vs. traditional discrete protection solutions. This new architecture is fabricated on a proprietary high voltage process that ensures a new level of fault protection while meeting the performance requirements of precision signal chains. (Page 8)

Designing for Low Noise Feedback Control with MEMS Gyroscopes

Noise in the output angular rate signals of a MEMS gyroscope can have a direct influence over critical system behaviors, such as platform stability, and is often the defining factor in the level of precision that a control system can support. Understanding the motion control system's dependence on gyroscope noise behaviors has a number of rewards for the designer, such as being able to establish relevant requirements for the feedback sensing element or, conversely, analyzing the system-level response to noise in a particular gyroscope. This article focuses on developing the most appropriate criteria for MEMS gyroscope selection and considerations for preserving the available noise performance throughout the sensor's integration process. (Page 13)

Op Amp Input Overvoltage Protection: Clamping vs. Integrated

In some applications, a situation may occur in which the inputs of an op amp get driven by voltages that exceed the level of the supply voltages—this is called an overvoltage condition. Overvoltage can result in certain aspects of the op amp's electrical performance being shifted beyond its data sheet guaranteed limits; it can even cause permanent failure of the device. The challenge then is to add overvoltage protection (OVP) circuitry at the input of the op amp without adding errors that result in a loss of system precision. This article compares and contrasts two approaches to input overvoltage protection. (Page 17)

Electromagnetic Flow Meters: Design Considerations and Solutions

There are multiple industry trends driving the need for a new flow measurement architecture, such as wastewater treatment plants, chemical/pharma plants, food and beverage processing, and pulp and paper production. These applications increasingly have the need to measure flow in the presence of high levels of solids, which is not easily achieved by most analog flow technologies. This articles focuses on the design considerations of implementing an electromagnetic flow meter architecture as a solution that simplifies system design, improves performance, and lowers cost and power. (Page 20)

Jim Surber [jim.surber@analog.com]

Product Introductions: Volume 50, Number 2

Data sheets for all ADI products can be found by entering the part number in the search box at analog.com.

April

4-channel, simultaneous sampling Σ-Δ ADC **AD7768-4**
3.3 V_{OUT}/5 V_{IN}, 2 A, ultralow noise adjustable output RF LDO **ADP7159**
Broadband, bidirectional, 1-bit GaAs IC digital attenuator **HMC802A**
Medium power MMIC amplifier operates from 71 GHz to 76 GHz **HMC7543**
MMIC oscillator with integrated 9.65 GHz to 10.41 GHz VCO **HMC1163**
Input selectable 2:8 differential fanout buffer for low noise clock distribution **HMC6832**

May

Low noise, 3 A low dropout linear regulator **ADP1763**
Low noise, low dropout linear regulator operates from a single input supply **ADP1762**
Low noise, low dropout linear regulator provides up to 1 A of output current **ADP1761**
6-bit digital phase shifter that is rated from 1.2 GHz to 1.4 GHz **HMC936A**
Broadband, nonreflective, GaAs, pHEMT, SP4T switch chip, covering dc to 18 GHz **HMC641A**
Integer-N synthesizer incorporates a 10 MHz to 1300 MHz digital phase frequency detector **HMC4069**
Broadband, nonreflective, GaAs, PHEMT, SP4T switch **HMC344A**
Digital phase frequency detector operates from 10 MHz to 1300 MHz **HMC3716**
6-bit digital attenuator operating from 0.1 GHz to 6 GHz **HMC1122**
Wideband microwave upconverter operates in the 6 GHz to 24 GHz frequency range **ADRF6780**
Dual receiver IC is fully compliant with the MC-GSM base station requirements **ADRF6614**
Low cost, GaAs, MMIC, 5 W, low distortion switch for transceiver applications **HMC574A**

June

Narrow-band optimized, high performance low noise amplifier family **ADL5721/ADL5723/ADL5724/ADL5725/ADL5726**
Digitally controlled, wide bandwidth, variable gain dual amplifier **ADA4522-1**
Highly efficient photometric sensor with integrated circuitry for gesture recognition **ADUCM310**
High efficiency digital input stereo Class-D audio amplifier **SSM3582**
Family of RF DACs enables a new level of communications performance **ADN4652**
Signal isolated, LVDS buffer operates at up to 600 Mbps with very low jitter **AD9162/AD9161**
Super Sequencer® is a configurable supervisory/sequencing device **ADM1260**
21 GHz to 24 GHz, GaAs, MMIC, I/Q upconverter **HMC7912**
Highly integrated IF receiver chip converts RF input signals from 800 MHz to 4 GHz **HMC8100**
17 GHz to 20 GHz, GaAs, MMIC, I/Q upconverter **HMC7911**
Integrated E-band, GaAs, MMIC, in-phase/quadrature downconverter chip **HMC7586**
Broadband, 5-bit, GaAs, IC digital attenuator achieves near dc operation **HMC539A**
Broadband, 6-bit, GaAs, MMIC, digital attenuator covers dc to 13 GHz **HMC424ALH5**
Broadband, 6-bit, GaAs, MMIC, digital attenuator covers dc to 3 GHz **HMC424ALH5**
4 CML output, low jitter clock generator with an integrated 5.4 GHz VCO **AD9530**
Dual-channel downconverting mixer with integrated PLL and VCO **HMC1190A**

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Practical Filter Design Challenges and Considerations for Precision ADCs

By Steven Xie

Introduction

Precision analog-to-digital converters are popularly used in many applications, such as instrumentation and measurement, PLM, process control, and motor control. Current SAR ADCs go up to 18-bit or even higher resolution at x-MSPS, while Σ-Δ ADCs can be 24- or 32-bit resolution at hundreds of kSPS. Users are facing more and more difficulties in limiting the signal chain noise, like in implementing filters, to take advantage of high performance ADCs without limiting the ADCs' capabilities.

This article discusses the design challenges and considerations associated with implementing analog and digital filters into the ADC signal chain to achieve optimum performance. As shown in Figure 1, the data acquisition signal chain can utilize analog or digital filtering techniques, or even a combination of both. Since precision SAR and Σ-Δ ADCs are commonly sampling within the first Nyquist zone, this article will focus on low-pass filters. It is not the intent to address specific low-pass filter design techniques in this article but rather their application in ADC circuits.

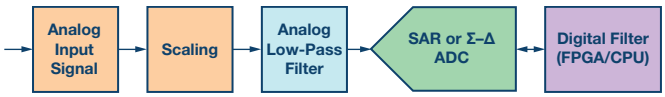


Figure 1. General data acquisition signal chain.

Ideal and Practical Filters

Ideal low-pass filters should have a steep transition band and excellent gain flatness in the pass band as shown by the brick wall dashed line in Figure 2. Furthermore, the stop band attenuation should reduce any residual out-of-band signal to zero. The response of some commonly used practical filters are shown in the colored lines in Figure 2. If the pass band gain is not flat or exhibits ripples, this response may scale the fundamental signal. The attenuation of the stop band is not infinite, which limits screening the noise out of band. There can also be a transition band without steep falloff, which degrades noise attenuation around the cutoff frequency. In addition, all non-ideal filters introduce a phase delay or group delay.

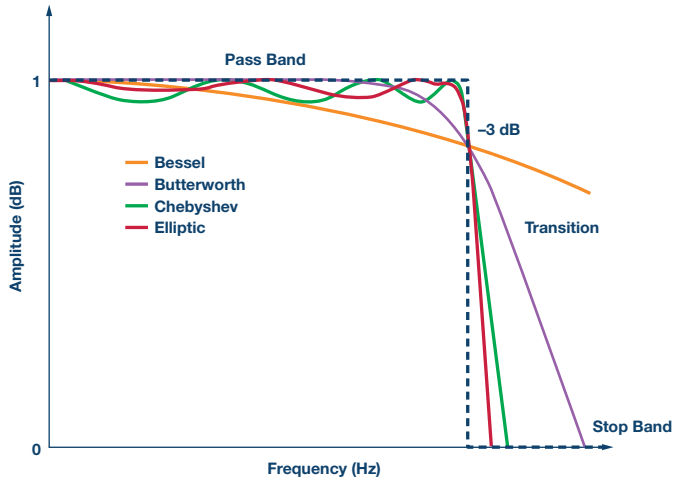


Figure 2. Ideal filter vs. practical filters amplitude response.

Analog Filter vs. Digital Filter

The analog low-pass filter can remove high frequency noise and interference from the signal path prior to the ADC conversion to help avoid contaminating the signal with aliased noise. It also eliminates the effects of overdriven signals beyond the bandwidth of the filter to avoid modulator saturation. In case of input overvoltage, the analog filter also limits the input current and attenuates the input voltage. Thus, it can protect the ADC's input circuitry. Noise peaks riding on signals near full scale have the potential to saturate the analog modulator of ADCs. They have to be attenuated with analog filters.

Since the digital filtering occurs after the conversion, it can remove noise injected during the conversion process. In real applications, the sampling rate is much higher than twice the fundamental signal frequency indicated by the Nyquist theorem. So, a postdigital filter could be utilized to reduce noise (such as input noise outside of signal bandwidth, power supply noise, reference noise, noise feed through digital interface, ADC chip thermal noise, or quantization noise) injected during the conversion process by using filtering techniques for a higher signal-to-noise ratio with even higher resolution.

Table 1 briefly lists the advantages and disadvantages of an analog filter vs. a digital filter.

Table 1. Analog Filter vs. Digital Filter

	Analog Filter	Digital Filter
Design Complexity	High for high performance filters	Low
Cost	High (depending on selected analog components)	Low (available CPU time)
Latency	Low	High
Additive Noise	Adds component thermal noise in band	May introduce digital noise due to quantization
ADC Input Protection	Yes	No
Programmable	No	Yes
Drift Error	Yes	No
Aging	Yes	No
Multichannel Matching Error	Yes	No

Analog Filter Considerations

Antialiasing filters are placed in front of ADCs, so these filters consequently are required to be analog filters. An ideal antialiasing filter features unity gain in the pass band with no gain variation and a level of alias attenuation that matches the theoretical dynamic range of the data conversion system in use.

ADCs exhibit different input resistance depending on their architecture, which impacts the input filter design. The following considerations pertain to designing an ADC's analog input filter.

Limitations of an RC Antialias Filter Interfacing to an ADC Front End

In the *Analog Dialogue* article "Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter," by Alan Walsh, there is an application example of an RC filter for the AD7980 ADC shown in Figure 3.

The calculated RC filter makes a low-pass filter with a cutoff bandwidth of 3.11 MHz. However, some designers may realize that 3.11 MHz is much larger than the input signal of 100 kHz, so the filter cannot efficiently reduce the noise out of band. To achieve higher dynamic range, they may replace the resistor with 590 Ω to get a 100 kHz, –3 dB bandwidth. There are two main problems with this approach. Since there will be more attenuation in the pass band, and up to 30% amplitude attenuation around 100 kHz for the example AD7980 ADC, signal chain accuracy will be greatly reduced. Smaller bandwidth means larger settling time, which makes the AD7980's internal sample and hold cap unable to fully charge in the specified acquisition time for the next valid conversion. This results in degraded accuracy for the ADC conversion.

The designer should ascertain that the RC filter in front of the ADC can fully settle within the target acquisition time. This is especially important for precision ADCs requiring a larger input current or having the equivalent smaller input impedance. Some Σ-Δ ADCs have maximum input RC value requirements in an unbuffered input mode. Extra narrow low-pass filters with larger resistors or caps that can be added in front of the input amplifier generally have a large input impedance. Alternatively, ADCs with very high input impedances can be selected, such as ADAS3022 with its 500 MΩ input impedance.

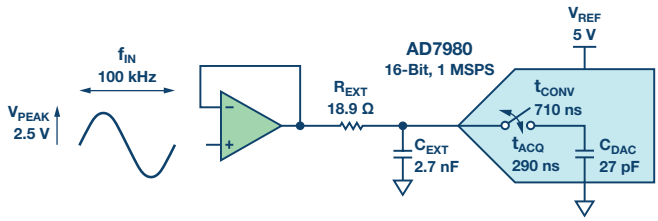


Figure 3. RC filter using AD7980 16-bit, 1 MSPS ADC.

1. Filter Settling Time for Multiplexed Sampling Signal Chain

A multiplexed input signal typically consists of large steps when switching between channels. In the worst case, one channel is at negative full scale, while the next channel is at positive full scale (see Figure 4). In this case, the input step size will be the full range of the ADC, when the mux switches channels.

One single filter after the mux can be used for the channels, which makes the design simpler and the cost lower. As discussed above, analog filters invariably introduce settling time. Every time the mux switches between channels, this single filter has to be recharged to the value of the selected channel, thus limiting the throughput rate. For a faster throughput rate, one filter for each channel in front of the mux can be an option, but this entails a higher cost.

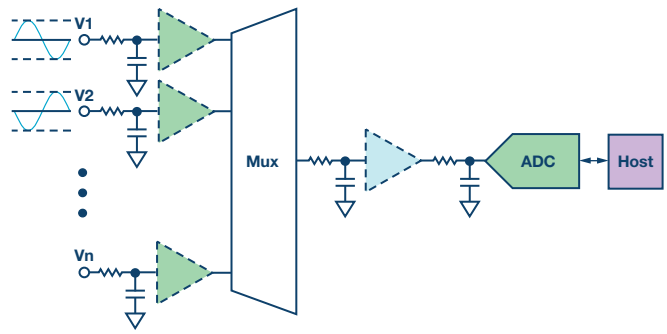


Figure 4. Multiplexed input signal chain.

2. Pass Band Flatness and the Transition Band Limitation vs. Noise

Applications encountering high noise levels, especially those with high levels of interference occurring close to the edge of the first Nyquist zone, require filters with aggressive roll-off.

However, as it is known for practical analog low-pass filters, the amplitude rolls down from low frequency to high frequency and has a transition band. More filter stages, or orders, may help improve flatness on in-band signals and render a narrower transition band. However, the design of these filters is complex because they are too sensitive to gain matching to be practical at a few orders of attenuation magnitude. Additionally, any component, such as a resistor or an amplifier, added in the signal chain will introduce in-band noise.

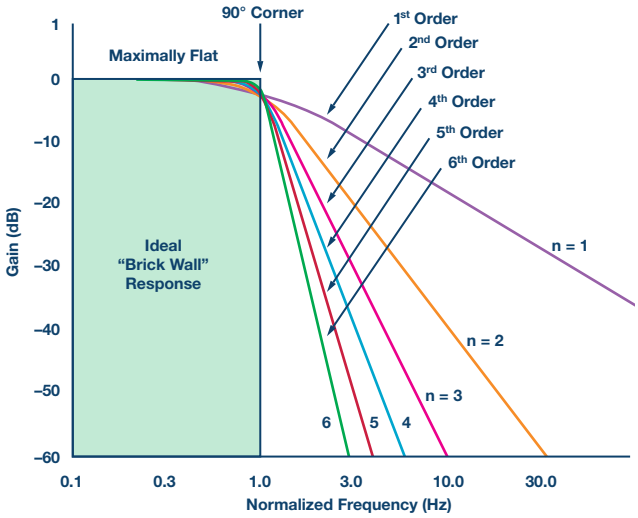


Figure 5. Ideal Butterworth filter transition band with different orders.

There is a trade-off in analog filter design complexity and performance for some specific applications. For example, in power-line relay protection with an AD7606, the protection channels have lower accuracy requirements for the fundamental 50 Hz/60 Hz input signal and its associated first five harmonics than the measurement channels. One first-order RC filter could be used for the protection channels, while a second-order RC filter provides better in-band flatness and more aggressive fall-off transition for the measurement channels.

3. Phase Delay and Matching Error for Simultaneous Sampling

Filter design is not just about frequency design; users may also need to consider time domain characteristics and phase response of the analog filters. Phase delay may be critical in some real-time applications. Phase alteration becomes even worse if phase varies according to input frequency. The phase variation in a filter is normally measured in terms of group delay. For a nonconstant group delay, a signal spreads out in time, causing a poor impulse response.

For multichannel simultaneous sampling applications, such as phase current measurement in motor control or power-line monitoring, the phase delay matching error should also be considered. Make sure the additional phase delay matching errors caused by the filters across multiple channels are negligible or within the signal chain error budget in the operating temperature range.

4. Component Selection Challenges for Low Distortion and Noise

For low harmonic distortion and low noise applications, users have to select qualified components in the signal chain design. Analog electronics are slightly nonlinear, which creates harmonic distortion. In Walsh's article, he discusses how to select a low distortion amplifier and how to calculate the amplifier noise. While active components such as amplifiers need low THD + N, the distortion and noise of passive components like common resistors and capacitors also need to be taken into account.

Resistors exhibit nonlinearity from two sources: the voltage coefficient and the power coefficient. Depending on the application, resistors manufactured by specific techniques, such as thin film or metal resistors, could be necessary in a high performance signal chain. The input filtering capacitors may also add significant distortion if not specified correctly. Polystyrene and NP0/C0G ceramic capacitors can be good alternatives to improve THD if the cost budget allows.

Besides amplifier noise, even resistors and capacitors have electronic noise that is generated by the thermal agitation of the charge carriers inside an electrical conductor at equilibrium. Thermal noise in an RC circuit has a simple expression, as higher R contributes to the filtering requirement as well as to more noise. The noise bandwidth of the RC circuit is 1/(4RC).

Two formulas are given to estimate the rms thermal noise of resistors and small capacitors.

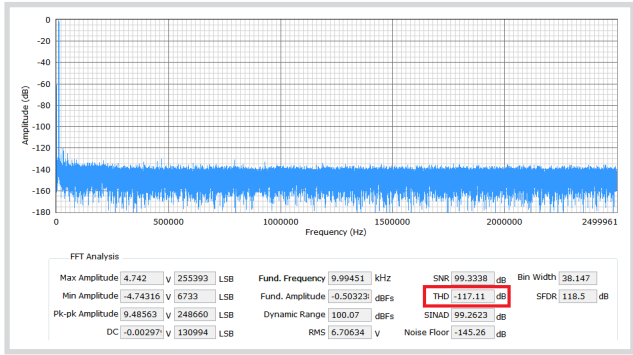
$$vn = \sqrt{4k_BTRf}$$
$$vn = \sqrt{k_BT/C}$$

k_B (Boltzmann constant) = $1.38065 \times 10^{-23} m^2 kgs^{-2} K^{-1}$

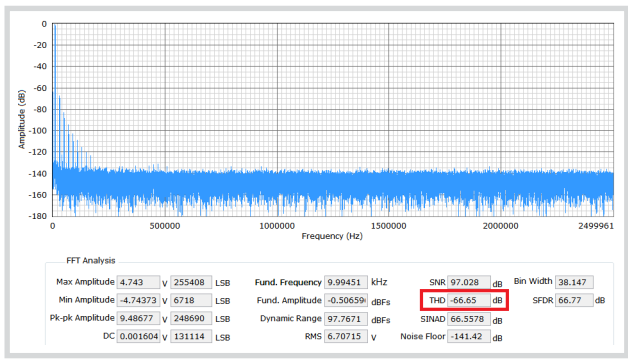
T is temperature in K

f is the brick wall filter approximation bandwidth

Figure 6 shows the THD performance effect of an NP0 cap vs. an X7R cap on an EVAL-AD7960FMCZ evaluation board: (a) shows the spectrum of a 10 kHz single tone sine wave with C76 and C77 being 1 nF 0603 NP0 caps while (b) shows the spectrum using 1 nF 0603 X7R caps.



(a) 0603 1 nF NP0 Cap



(b) 0603 1nF X7R Cap

Figure 6. NP0 vs. X7R caps effects on THD on an EVAL-AD7960FMCZ evaluation board.

With the previous design concerns in mind, the active analog filters can be designed using ADI's Analog Filter Wizard. It will calculate capacitor and resistor values, as well as select amplifiers required for the application.

Digital Filter Considerations

SAR and Σ-Δ ADCs have been steadily achieving higher sample rates and input bandwidths. Oversampling a signal at twice the Nyquist rate evenly spreads the ADC's quantization noise power into a double frequency band. Then it is easy to design digital filters to band-limit the digitized signal, and then decimate to the desired final sample rate. This technique reduces the in-band quantization error and improves ADC SNR. This technique reduces the pressure on the antialiasing filter by relaxing filter roll-off. Oversampling techniques reduce the demands on the filters, but requires higher sample rate ADCs and faster digital processing.

1. Actual SNR Improvement Utilizing an Oversampling Rate on an ADC

Utilizing oversampling and a decimation filter, the SNR improvement can be derived from the theoretical SNR for an N-bit ADC: SNR = 6.02 × N + 1.76 dB + 10 × log10[OSR], OSR = $f_s/(2 \times BW)$. Note that this formula only applies to ideal ADCs in which there is only quantization noise.

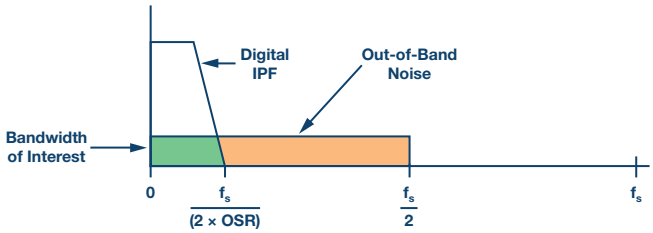


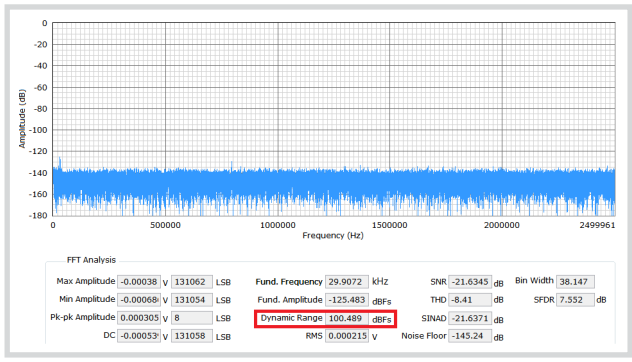
Figure 7. Oversampling of a Nyquist converter.

Many other sources introduce noise into ADC conversion codes. For example, there is noise from the signal source and signal chain components, chip thermal noise, shot noise, noise in power supplies, noise in the reference voltage, digital feedthrough noise, and phase noise due to sampling clock jitter. This noise may distribute uniformly in the signal band, and appear as flicker noise. Therefore, the actual achieved SNR improvement in the ADC is commonly lower than that calculated in the formula.

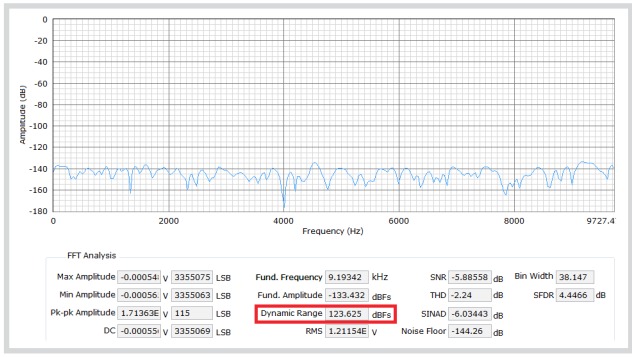
2. Dynamic Improvement with Oversampling on the EVAL-AD7960FMCZ Evaluation Board

In application note AN-1279, it is shown that the measured dynamic range of an 18-bit AD7960 ADC oversampled by 256× is 123 dB. This application is used for high performance data acquisition signal chains, such as spectroscopy, magnetic resonance imaging (MRI), and gas chromatography, as well as vibration, oil/gas, and seismic systems.

As shown in Figure 8, the measured oversampled dynamic range shows a 1 dB to 2 dB degradation from the theoretical SNR improvement calculation because the low frequency noise coming from the signal chain components limits the overall dynamic range performance.



(a) Dynamic Range without OSR



(b) Dynamic Range with OSR = 256

Figure 8. Dynamic range improvement with OSR 256.

3. Taking Advantage of an Integrated Digital Filter in SAR and Σ-Δ ADCs

Usually, digital filters reside in an FPGA, a DSP, or a processor. To reduce the system design effort, ADI provides some precision ADCs with integrated postdigital filters. For example, the AD7606 has a one-order postdigital sinc filter for oversampling. It is easily configured by pulling up or down the OS pins. The Σ-Δ ADC AD7175-x not only has a traditional sinc3 filter, but also sinc5 + sinc1 and enhanced 50 Hz and 60 Hz rejection filters. The AD7124-x provides a fast settling mode (sinc4 + sinc1 or sinc3 + sinc1 filter) function.

4. Trade-Off Latency with Multiplexing Sampling ADCs

Digital filters have the disadvantage of latency, which depends on the digital filters' orders and master clock rate. The latency should be limited for real-time applications and loop response time. The output data rate in the data sheet is the rate at which valid conversions are available when continuous conversions are performed on a single channel. When the user switches to another channel, additional time is required for the Σ-Δ modulator and digital filter to settle. The settling time associated

with these converters is the time it takes the output data to reflect the input voltage following a channel change. To accurately reflect the analog input following a channel change, the digital filter must be flushed of all data pertaining to the previous analog input.

For previous Σ-Δ ADCs, the channel switching speed is a fraction of the data output rate. Therefore, in switching applications such as multiplexing data acquisition systems, it is important to realize that the rate at which conversions are available is several times less than the conversion rate achieved when continuously sampling a single channel.

Some new ADI Σ-Δ ADCs, such as the AD7175-x, contain optimized digital filters to decrease the settling time when channel switching. The AD7175-x's sinc5 + sinc1 filter is targeted at multiplexed applications and achieves single cycle settling at output data rates of 10 kSPS and lower.

5. Avoid Aliasing by Decimation with Digital filters

As discussed in many articles, the higher the oversampling frequency, the easier the analog filter design becomes. When sampling at a higher rate than you need to satisfy Nyquist, a simpler analog filter could be used to avoid any exposure to aliasing from extremely high frequencies. It is difficult to design an analog filter to attenuate a desired frequency band without distortion, but easy to design an analog filter to reject high frequencies with oversampling. Then it is easy to design digital filters to band-limit the conversion signal, and then decimate to the desired final sample rate without losing desired information.

Before implementing decimation, it is necessary to ensure that this resampling will not introduce new aliasing problems. Make sure the input signal follows Nyquist Theorem referring to the sampling rate after decimation.

The EVAL-AD7606/EVAL-AD7607/EVAL-AD7608EDZ evaluation board can run at 200 kSPS per channel. In the following test, it is configured sampling at 6.25 kSPS with an oversampling rate of 32. Then, a 3.5 kHz, –6 dBFS sine wave is applied to the AD7606. Figure 9 shows a –10 dBFS alias image at 2.75 kHz (6.25 kHz – 3.5 kHz). Therefore, if there is no qualified antialias analog filter in front of the ADC, the digital filter could cause alias images by decimation when oversampling is used. An analog antialias filter should be used to remove such noise peaks superimposed on the analog signal.

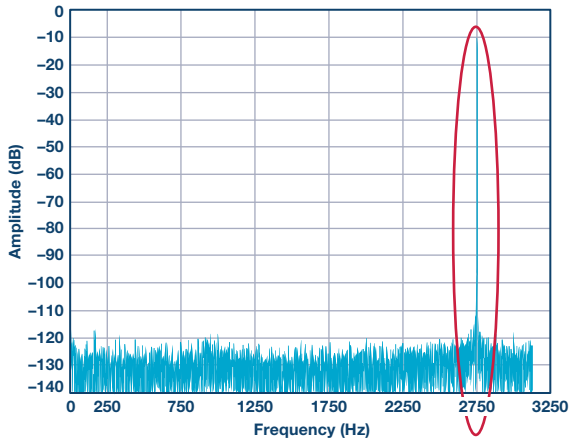


Figure 9. Alias when the OSR decimation sampling rate < twice the Nyquist frequency.

Conclusion

The challenges and considerations discussed in this article can help the designer implement practical filters to help achieve the objectives of a precision acquisition system. Analog filters have to interface to the nonideal input structures of SAR or Σ-Δ ADCs without violating system error budgets while digital filters should not cause errors on the processor side. It is not an easy task, and trade-offs must be made in system specifications, response time, cost, design effort, and resources.

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Steven Xie [steven.xie@analog.com] has worked as a product applications engineer with the China Design Center in ADI Beijing since March 2011. He provides technical support for SAR ADC products across China. Prior to that, he worked as a hardware designer in wireless communication base stations for four years. In 2007, Steven graduated from Beihang University with a master's degree in communications and information systems.

Steven Xie

Also by this Author:

Practical Filter Design Challenges and Considerations for Precision ADCs

Volume 49, Number 1

Replacing Discrete Protection Components with Overvoltage Fault Protected Analog Switches

By Paul O'Sullivan

Abstract

The challenge of designing robust electronic circuitry often results in a design with a multitude of discrete protection components with associated cost, design time, and space additions. This article discusses fault protected switch architecture, along with the performance benefits and other advantages it offers vs. traditional discrete protection solutions. A new novel switch architecture and proprietary high voltage process that provides industry-leading fault protection along with the performance required for precision signal chains is discussed. ADI's new portfolio of fault protected switches and multiplexers (ADG52xxF and ADG54xxF) uses this technology.

Analog input protection for high performance signal chains is often a pain point for system designers. There is typically a significant trade-off between analog performance (such as leakage and on resistance) and the level of protection that can be offered by discrete components.

Replacing the discrete protection components with overvoltage protected switches and multiplexers can offer significant benefits in terms of analog performance, robustness, and solution size. The overvoltage protected component sits between sensitive downstream circuitry and the input that is exposed to external stresses. An example of this would be the sensor input terminal in a process control signal chain.

This article details the issues caused by overvoltage events, discusses traditional discrete protection solutions and the associated drawbacks, presents the solution offered by overvoltage protected analog switches including features and system benefits, and finally introduces the industry-leading portfolio of ADI fault protected analog switches.

Overvoltage Issues—Back to Basics

When the input signal applied to a switch exceeds the power supplies (V_{DD} or V_{SS}) by more than a diode drop, the ESD protection diodes within the IC become forward-biased and current flows from the input signal to the supplies, as shown in Figure 1. This current could damage the part and may trigger a latch-up event if the current is not limited.

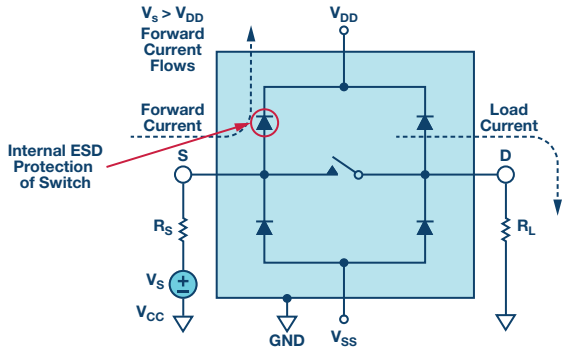


Figure 1. Overvoltage current path.

If the switch is unpowered, there are a couple of scenarios that could occur:

1. If the power supplies are floating, the input signal could end up powering the V_{DD} rail through the ESD diodes. In that case, the V_{DD} pin goes to within a diode drop of the input signal. This means the switch would effectively be powered, as would any other components using the same V_{DD} rail. This could lead to unknown and uncontrolled operation of devices in the signal chain.

2. If the power supplies are grounded, the PMOS device will turn on with negative VGS so the switch will pass a clipped signal to the output, possibly damaging downstream components that would also be unpowered (see Figure 2). Note: if there are diodes to the supply, they will forward bias and clip the signal to +0.7 V.

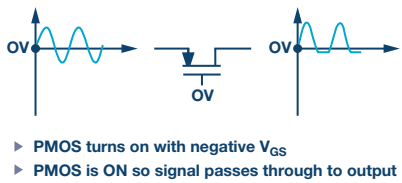


Figure 2. Overvoltage signal with power supply grounded.

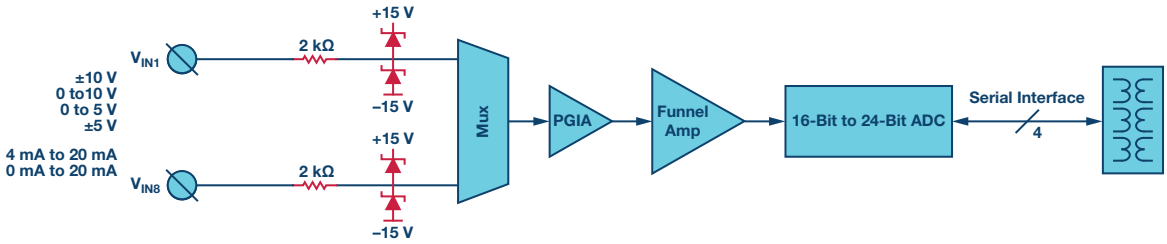


Figure 3. Discrete protection solution.

Discrete Protection Solution

Designers traditionally solve input protection issues with discrete protection components.

Large series resistors are used to limit the current during a fault, and Schottky or Zener diodes to the supply rails clamp any overvoltage signals. An example of such a protection scheme in a multiplexed signal chain is shown in Figure 3.

However, there are many disadvantages to using these discrete protection components.

1. The series resistor will increase the settling time of the multiplexer and slow down the overall settling time.
2. The protection diodes will introduce additional leakage current and varying capacitance that will impact the precision and linearity of the measurement.
3. There will be no protection in the floating supply condition as the ESD diodes to the supplies won't provide any clamping protection.

Traditional Switch Architecture

The diagram in Figure 4 gives an overview of a traditional switch architecture. The switch component (on the right hand side of Figure 4) has ESD diodes to each of the supply rails, at both the input and output side of the switch element. The external discrete protection components are shown here as well—the series resistor for current limiting and the Schottky diodes to the supplies for overvoltage clamping. There is often a requirement for a bidirectional TVS for additional protection in harsher environments.

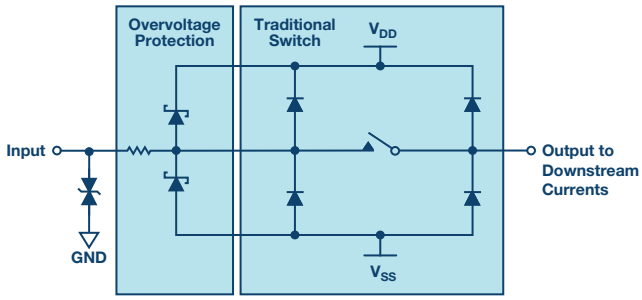


Figure 4. Traditional switch architecture with external discrete protection.

Fault Protected Switch Architecture

The fault protected switch architecture is shown in Figure 5. The ESD diodes at the input side are replaced with a bidirectional ESD cell, so the input voltage range is no longer limited by the ESD diodes to the supply rails. Therefore, the input can see voltages up to the limitation of the process (which is ±55 V for the new fault protected switches from ADI).

The ESD diodes remain at the output side in most cases as there usually isn't a requirement for overvoltage protection from the output side.

The ESD cell at the input side can still provide excellent ESD protection. The ADG5412F overvoltage fault protected quad SPST switch that uses this type of ESD cell achieves a 5.5 kV HBM ESD rating.

There may still be a requirement for an external TVS or a smaller current limiting resistor for more stringent cases such as IEC ESD (IEC 61000-4-2), EFT, or surge protection.

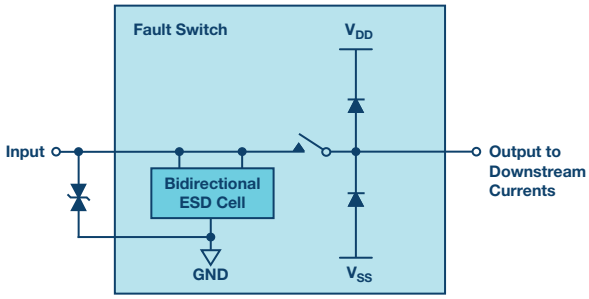


Figure 5. Fault protected switch architecture.

In the case of an overvoltage condition at one of the switch inputs, the affected channel turns off and the input goes high impedance. The leakage will remain low on the other channels, so the remaining channels can continue to operate as normal with minimal impact on performance. This allows for very little compromise between system speed/performance and overvoltage protection.

The fault protected switch can therefore greatly simplify the signal chain solution. The switch overvoltage protection removes the requirement for the current limiting resistors and Schottky diodes in many cases. The overall system performance is no longer limited by external discrete components that typically introduce leakage and distortion into a signal chain.

ADI Fault Protected Switch Features

The new portfolio of fault protected switches from ADI are built on a proprietary high voltage process that provides overvoltage protection up to ±55 V in both the powered and unpowered states. These parts provide industry-leading performance for fault protected switches for precision signal chains.

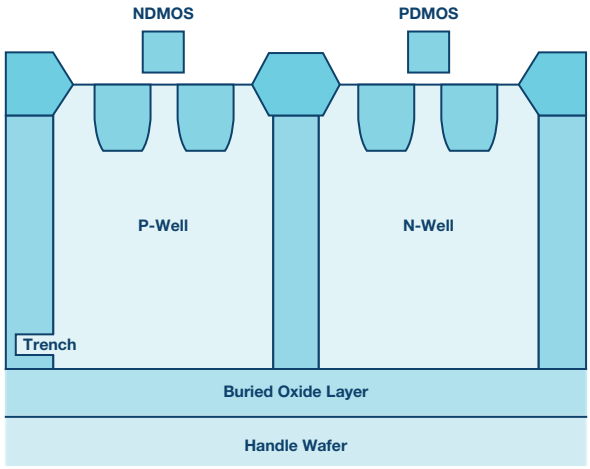


Figure 6. Trench isolated process.

Latch-Up Immunity

The proprietary high voltage process is also trench isolated. An insulating oxide layer is placed between NDMOS and the PDMOS transistors of each switch. Parasitic junctions, which occur between the transistors in junction-isolated switches, are eliminated and the result is a switch that is latch-up immune under all circumstances. The ADG5412F, for example, passes a JESD78D latch-up test of ±500 mA for a 1 second pulse width, which is the most stringent test in the specification.

Analog Performance

As well as achieving industry-leading robustness (overvoltage protection, high ESD rating, known state at power-up without digital inputs present), the new ADI fault protected switches also have industry-leading analog performance. Switch performance as always is a trade-off between low on resistance and low capacitance/charge injection. The choice of switch usually depends on whether the load is high impedance or low impedance.

Low Impedance Systems

Low on-resistance parts are usually used in low impedance systems, where the on resistance of the switch needs to be kept to a minimum. In low impedance systems, such as a power supply or gain stage, the on resistance and source impedance in parallel with the load can cause gain errors. Even though gain errors can be calibrated out in many cases, the variation of on resistance (R_{ON}) across signal range or between channels produces distortion that cannot be calibrated out. Therefore, low resistance circuits are more subject to distortion errors due to R_{ON} flatness and R_{ON} variation across channels.

The plot in Figure 7 shows the switch on resistance of one of the new fault protected switches across the signal range. As well as achieving very low on resistance, the R_{ON} flatness and matching between channels is also excellent. The parts have a patented switch driver design that guarantees a constant V_{GS} voltage and delivers flat R_{ON} performance across the input voltage range. The trade-off is a slightly reduced signal range where optimal performance can be achieved, which can be seen from the shape of the R_{ON} plots. There can be significant system benefits because of this R_{ON} performance in applications sensitive to R_{ON} variation or THD.

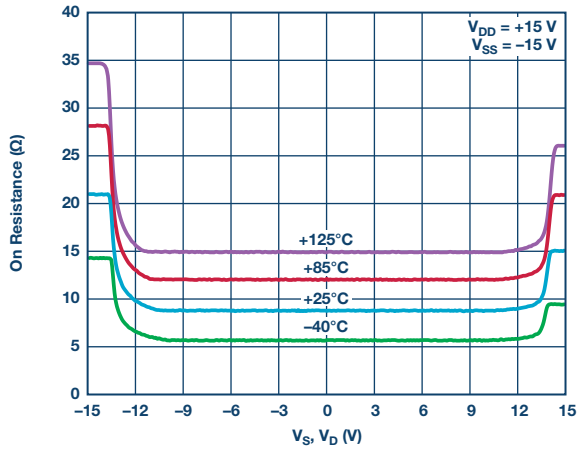


Figure 7. Fault protected switch on resistance.

The ADG5404F is the new latch-up immune, overvoltage fault protected multiplexer. Latch-up immune parts and overvoltage protected parts typically have higher on resistance and worse on-resistance flatness than standard parts. However, due to the constant V_{GS} scheme used in the ADG5404F design, the R_{ON} flatness is actually better even than the ADG1404 (industry-leading low on resistance) and ADG5404 (latch-up immune, but not overvoltage protected). In many applications, such as RTD temperature measurements, the R_{ON} flatness is actually more important than the absolute value of on resistance so the fault protected switch provides potential for increased performance in these systems.

The typical fault mode for a low impedance system is for the drain output to go open circuit in the case of a fault.

High Impedance Systems

Low leakage, low capacitance, low charge injection switches are most commonly used in high impedance systems. Data acquisition systems are typically high impedance due to amplifier loads on the multiplexer output.

- Leakage is the dominant source of error in high impedance circuits. Any leakage currents can lead to significant measurement errors.
- Low capacitance and low charge injection is also critical for faster settling. This allows for maximum data throughput in a data acquisition system.

The leakage performance of the new ADI fault protected switches is excellent. In normal operation the leakage current is in the low nA range, which is critical for accurate measurements in many applications.

Critically, the leakage performance is also very good even when one of the input channels is in fault. This means that measurements can continue on other channels until the fault

is fixed, thereby reducing system downtime. The overvoltage leakage current for the ADG5248F 8:1 multiplexer is shown in Figure 8.

The typical fault mode for a high impedance system is for the drain output to pull to the supply rail in the case of a fault.

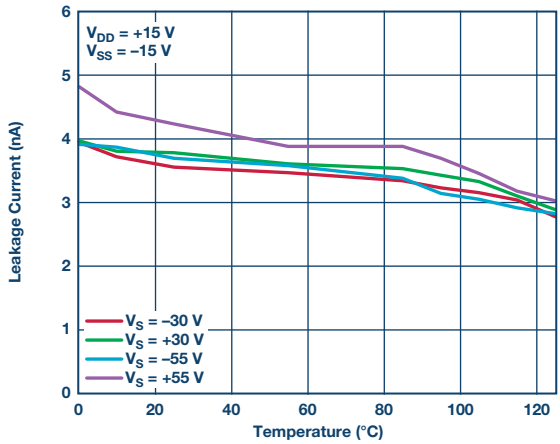


Figure 8. ADG5248F overvoltage leakage current vs. temperature.

Fault Diagnostics

Most of the new ADI fault protected switches also feature digital fault pins. The FF pin is a general fault flag, which indicates that one of the input channels is in fault. The specific fault pin (or SF pin) is a pin that can be used to debug which specific input is in fault.

These pins can be useful for fault diagnostics in a system. The FF pin first alerts a user to a fault. The user can then cycle through the digital inputs and the SF pin will identify which particular switch or switches are in fault.

System Benefits

The system benefits of the new portfolio of fault protected switches are captured in Figure 9. The benefits to a system designer are great, both in terms of ensuring optimal analog performance in a precision signal chain, and in terms of system robustness.

Features	System Benefits
Fault Protection ±55 V Overvoltage Protection	Prevents damage to downstream circuitry Reduces the need for discrete protection components
Fault Detection Digital Output Indicator for Fault Conditions	Alerts to source of fault Eliminates the need for complex fault detection software routines
High ESD Industry-Leading 5.5 kV HBM ESD	Eases board assembly Reduces ESD components
Precision Performance Low R_{ON} and R_{ON} Flatness Low Leakage Current	Prevents signal distortion Maximizes system performance

Figure 9. ADI fault protected switch—features and system benefits.

The benefits compared to discrete protection components are obvious and have been described in detail already. The proprietary high voltage process and novel switch architecture also gives the new range of ADI fault protected switches a number of advantages over competitor solutions.

- Industry-leading R_{ON} flatness for precision measurements
- Industry-leading fault leakage current to allow for continued operation on other channels not affected by a fault (10× better than competing solutions)
- Parts with secondary fault supplies for precision fault thresholds while still maintaining optimum analog switch performance
- Intelligent fault flags for system fault diagnostics

Application Examples

This first application example shown in Figure 10 is a process control signal chain, where a microcontroller is monitoring a number of sensors such as RTD or thermocouple temperature sensors, pressure sensors, and humidity sensors. In a process control application, the sensor may be connected at the end of a very long cable in a factory, with the potential for faults along the length of the cable.

The multiplexer in this case is the ADG5249F, which is optimized for low capacitance and low leakage. Low leakage is important for these type of small signal sensor measurements.

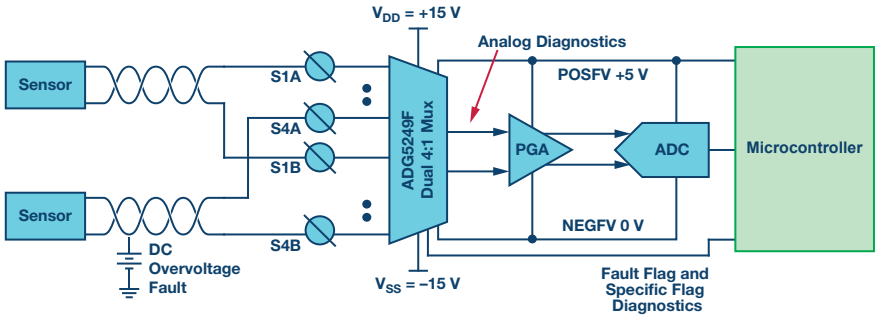


Figure 10. Process control application example.

Portfolio Summary

Table 1. Low On-Resistance Family of Fault Protected Switches

Product	Configuration	Fault Trigger Threshold	Output Fault Mode	Fault Flag
ADG5412F ADG5413F	Quad SPST	Primary supplies	Open circuit	General flag
ADG5412BF ADG5413BF	Quad SPST and bidirectional OVP	Primary supplies	Open circuit	General flag
ADG5462F	Quad-channel protector	Secondary supplies	Pull to secondary supply or open circuit (default)	General flag
ADG5404F	4:1 mux	Primary supplies	Pull to secondary supply or open circuit (default)	General and specific flags
ADG5436F	Dual SPDT	Primary supplies	Pull to secondary supply or open circuit (default)	General and specific flags

Table 2. Low Capacitance/Low Charge Injection Family of Fault Protected Switches

Product	Configuration	Fault Trigger Threshold	Output Fault Mode	Fault Flag
ADG5208F	8:1 multiplexer	Primary supplies	Pull to rails	None
ADG5209F	Differential 4:1 multiplexer	Primary supplies	Pull to rails	None
ADG5248F	8:1 multiplexer	Secondary supplies	Pull to secondary supplies	General and specific flags
ADG5249F	Differential 4:1 multiplexer	Secondary supplies	Pull to secondary supplies	General and specific flags
ADG5243F	Triple SPDT	Secondary supplies	Pull to secondary supplies	General and specific flags

The switch operates off ±15 V supplies, while the secondary fault supplies are configured for 5 V and GND to protect the downstream PGA and ADC.

The main sensor signal passes through the multiplexer to the PGA and ADC while the fault diagnostics are sent directly to the microcontroller to provide an interrupt in the case of a fault. The user can therefore be alerted to a fault condition and can determine which of the sensors is in fault. A technician can then be sent out to debug the fault and, if necessary, replace the sensor or cable in fault.

Because of the industry-leading low fault leakage specification, the other sensors can continue to be monitored even while one of the sensors is down and awaiting replacement. Without such low fault leakage, a fault on one channel could make all of the other channels unusable until the fault is repaired.

The second application example in Figure 11 is a portion of a data acquisition signal chain where the ADG5462F channel protector would add value. In this case there is a PGA with ±15 V supply rails, while the ADC downstream has as input signal range of 0 V to 5 V.

The channel protector sits between the PGA and ADC. It uses the ±15 V supply rails as its primary supplies to achieve optimum on resistance, and uses 0 V and 5 V for its secondary supply rails. The ADG5462F will allow the signal to pass through in normal operation, but will clamp any overvoltage outputs from the PGA to between 0 V and 5 V to protect the ADC. Therefore, like the previous applications example, the signal of interest is biased in the flat R_{ON} region of operation.

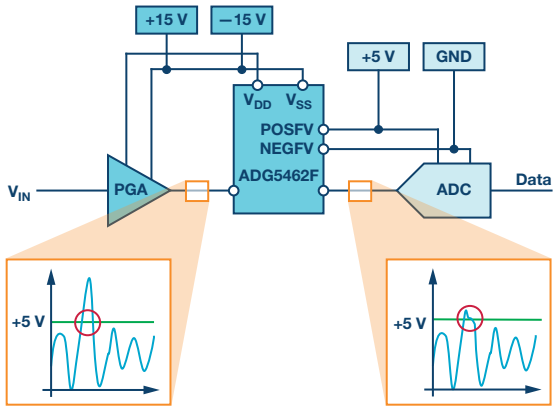


Figure 11. Data acquisition application example.

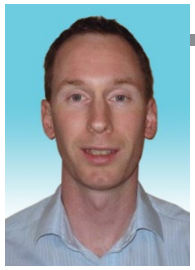
Summary

Replacing traditional discrete protection components with overvoltage protected switches and multiplexers can provide many system benefits in a precision signal chain. As well as saving board space, the performance benefits of replacing discrete components can be significant.

Analog Devices has a wide range of overvoltage protected switches and multiplexers. The latest families of fault protected devices are listed in Table 1 and Table 2. They are built on a proprietary high voltage and latch-up immune process and provide industry-leading performance and features for precision signal chains.

Paul O'Sullivan

Paul O'Sullivan [paul.osullivan@analog.com] is an applications engineer in ADI's Linear and Precision Technology business unit in Limerick, Ireland. He supports the switch/multiplexer product portfolio and previously supported the power management portfolio for ADI. He joined ADI in 2004 with a bachelor's degree in electrical and electronic engineering from University College Cork and an M.Eng. from University of Limerick.



Designing for Low Noise Feedback Control with MEMS Gyroscopes

By Mark Looney

Abstract

MEMS gyroscopes offer a simple way to measure the angular rate of rotation in packages that easily attach to printed circuit boards, so they are a popular choice to serve as the feedback sensing element in many different types of motion control systems. In this type of function, noise in the angular rate signals (MEMS gyroscope output) can have a direct influence over critical system behaviors, such as platform stability, and is often the defining factor in the level of precision that a control system can support. Therefore, low noise is a natural, guiding value for system architects and developers as they define and develop new motion control systems. Taking that value (low noise) a step further, translating critical system-level criteria, such as pointing accuracy, into noise metrics that are commonly available in MEMS gyroscope data sheets, is a very important part of early conceptual and architectural work. Understanding the system's dependence on gyroscope noise behaviors has a number of rewards, such as being able to establish relevant requirements for the feedback sensing element or, conversely, analyzing the system-level response to noise in a particular gyroscope. Once system designers have a good understanding of this relationship, they can focus on mastering the two key areas of influence that they have over the noise behaviors in their angular rate feedback loops: 1. developing the most appropriate criteria for MEMS gyroscope selection and 2. preserving the available noise performance throughout the sensor's integration process.

Motion Control Basics

Developing a useful relationship between the noise behaviors in a MEMS gyroscope and how it impacts key system behaviors often starts with a basic understanding of how the system works. Figure 1 offers an example architecture for a motion control system, which breaks the key system elements down into functional blocks. The functional objective for this type of system is to create a stable platform for personnel or equipment that can be sensitive to inertial motion. One example application is for a microwave antenna on an autonomous vehicle platform that is maneuvering through rough conditions at a speed that causes abrupt changes in vehicle orientation. Without some real-time control of the pointing angle, these highly directional antennas may not be able to support continuous communication while experiencing this type of inertial motion.

The system in Figure 1 uses a servo motor, which will ideally rotate in a manner that is equal and opposite of the rotation that the rest of the system will experience. The feedback loop starts with a MEMS gyroscope that observes the rate of rotation (ϕ_G) on the stabilized platform. The gyroscope's angular rate signals then feed into application-specific digital signal processing that includes filtering, calibration, alignment, and integration to produce real-time orientation feedback (ϕ_E). The servo motor's control signal (ϕ_{COR}) comes from a comparison of this feedback signal with the commanded orientation (ϕ_{CMD}), which may come from a central mission control system or simply represent the orientation that supports ideal operation of the equipment on the platform.

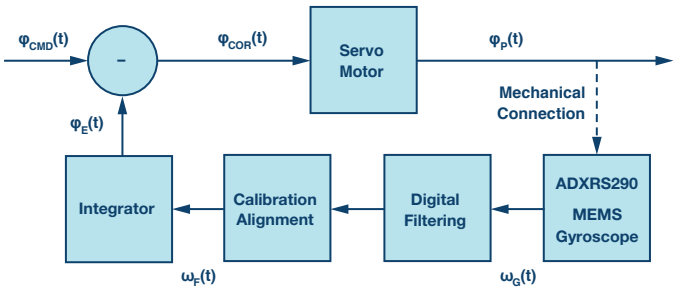


Figure 1. Example of a motion control system architecture.

Example Application

Moving from the architectural view of a motion control system in Figure 1, valuable definitions and insights also come from analyzing application-specific, physical attributes. Consider the system in Figure 2, which offers a conceptual view of an automated inspection system for a production line. This camera system inspects items that move in and out of its field of view on a conveyor belt. In this arrangement, the camera attaches to the ceiling through a long bracket, which establishes its height (see D in Figure 2), in order to optimize its field of view for the size of the objects it will inspect. Since factories are full of machinery and other activities, the camera can experience swinging motion (see $\phi_{SW}(t)$ in Figure 2) at times, which can cause distortion in the inspection images. The red dotted lines in this diagram provide an exaggerated view of total angular error ($\pm\phi_{SW}$) that comes from this swinging motion and the green dotted lines represent the level of angular error that will support the system's image quality objectives ($\pm\phi_{RE}$). The view in Figure 2 defines the key system-level metric (image distortion) in terms of linear displacement error (d_{SW}, d_{RE}) on the inspection surface. These attributes relate to the camera height (D) and the angular error terms (φ_{SW}, ϕ_{RE}) through a simple trigonometric relationship in Equation 1.

$$d_{SW} = D \times \sin(\varphi_{SW})$$
$$\varphi_{SW} = a\sin\left(d_{SW}/D\right)$$
$$d_{RE} = D \times \sin(\varphi_{RE}) \quad (1)$$
$$\varphi_{RE} = a\sin\left(d_{RE}/D\right)$$

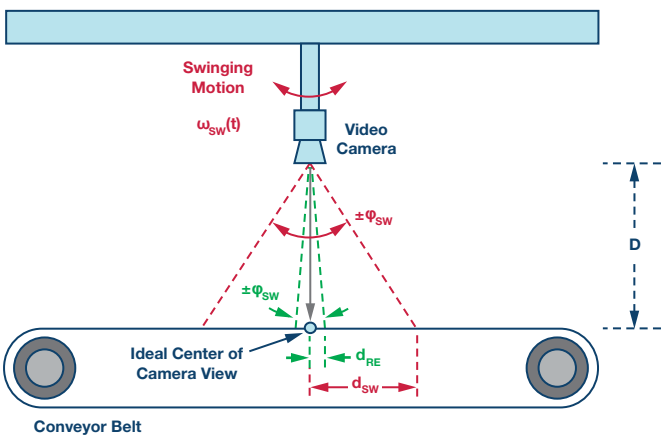


Figure 2. Industrial camera inspection system.

The most applicable motion control technique for this type of system is known as image stabilization. Early image stabilization systems used gyroscope-based feedback systems to drive servo motors, which adjust the orientation of the image sensor during the time that the shutter is open. The emergence of MEMS technology helped reduce the size, cost, and power of these functions in a revolutionary manner, which led to wider spread use of this technique in modern day digital cameras. Advances in digital image processing techniques, which still use MEMS-based angular rate measurements in their algorithms, have led to elimination of the servo motor in many applications. Whether the image stabilization comes from a servo motor or through digital postprocessing of image files, the fundamental function (feedback sensing) of the gyroscope remains the same, as does the consequence of its noise. For simplicity, this discussion focuses on the classic approach (servo motor on the image sensor) to explore the most relevant noise fundamentals, and how they relate to the most important physical attributes of this type of application.

Angle Random Walk (ARW)

All MEMS gyroscopes have noise in their angular rate measurements. This inherent sensor noise represents the random variation in the gyroscope's output, when it is operating in static inertial (no rotational motion) and environmental conditions (no vibration or shock). The most common metrics that MEMS gyroscope data sheets offer to describe their noise behaviors are rate noise density (RND) and angle random walk (ARW). The RND parameter typically uses units of °/sec/√Hz and provides a simple way to predict the total noise, in terms of angular rate, based on the gyroscope's frequency response. The ARW parameter typically uses units of °/√hour and is often more useful when analyzing the impact that noise has on angle estimation over specific periods of time. Equation 2 offers a generic formula for estimating the angle, based on the angular rate measurement. In addition, it also provides a simple formula that relates the RND parameter to the ARW parameter. This relationship represents a small adaption (single-sided vs. double-sided FFT) from the one in IEEE-STD-952-1997 (Appendix C).

$$\begin{aligned} \varphi_n(t) &= \int_0^{\tau} \omega_n(t) \times dt \\ \varphi_n(\tau) &= ARW \times \sqrt{\tau} \\ ARW &= \frac{60}{\sqrt{2}} \times RND \\ \varphi_n(\tau) &= \frac{60}{\sqrt{2}} \times RND \times \sqrt{\tau} \end{aligned} \tag{2}$$

Figure 3 provides a graphical reference that helps support further discussion of the behavior that the ARW parameter represents. The green dotted lines in this illustration represent the ARW behavior when the gyroscope has an RND of 0.004°/sec/√Hz, which equates to an ARW of 0.17°/√hour. The solid lines represent six separate integrations of this gyroscope's output over a period of 25 ms. The random nature of the angular errors, with respect to time, show that the ARW's primary utility is in estimating the statistical distribution of the angular errors over a specific integration time. Also note that this type of response does assume the use of high-pass filtering to remove initial bias errors in the integration process.

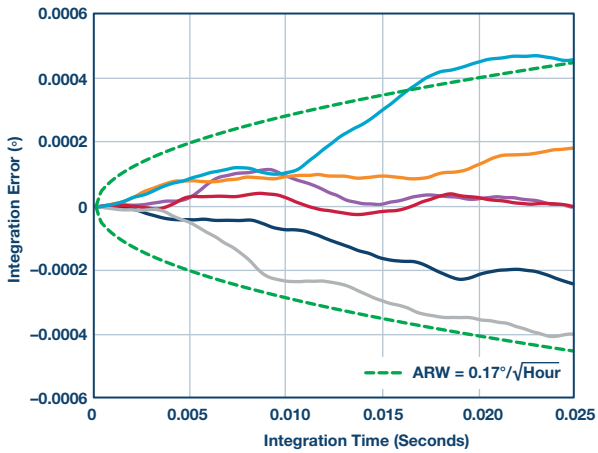


Figure 3. Angle random walk (ADIS16460).

Relating back to the application example in Figure 2, combining Equations 1 and 2 provides an opportunity to relate important criteria (physical distortion on the inspection surface) to noise performance metrics (RND, ARW) that are commonly available in MEMS gyroscope data sheets. In this process, assuming that the integration time (τ) from Equation 1 is equal to the image capture time provides another simplification that might be useful. Equation 3 applies the generic relationship from Equation 1 to estimate that when the camera is 1 meter (D) off of the inspection surface and the maximum allowable distortion error is 10 µm (d_{RE}), the angular error from the gyroscope (ϕ_{RE}) must be less than 0.00057°.

$$\begin{aligned} d_{RE} &= D \times \sin(\varphi_{RE}) \\ \varphi_{RE} &\le \arcsin\left(\frac{d_{RE}}{D}\right) \\ \varphi_{RE} &\le \arcsin\left(\frac{0.00001m}{1m}\right) \\ \varphi_{RE} &\le 0.00057° \end{aligned} \tag{3}$$

Equation 4 combines the results from Equation 3 and the generic relationship in Equation 2 to predict ARW and RND requirements for the MEMS gyroscope in a particular situation. This process assumes that the image capture times of 35 ms represents the integration time (τ) from Equation 2, which leads to predicting that the gyroscope's ARW needs to be less than 0.18°/√hour, or the RND must be less than 0.0043°/sec/√Hz to support this requirement. Of course, this may not be the only requirement that these parameters support, but these simple relationships do provide an example of how to relate to known requirements and conditions.

$$\varphi_{RE} \le \varphi_n \le 0.00057°$$

$$\varphi_n \le 0.0057°$$

$$ARW \times \sqrt{\tau} \le 0.00057°$$

$$ARW \times \le \frac{\sqrt{2} \times 0.00057°}{\sqrt{\tau}}$$

$$RND \le \frac{\sqrt{2} \times 0.00057°}{60 \times \sqrt{\tau}}$$

When τ can reach 0.035 seconds

$$ARW \times \le \frac{0.00057°}{\sqrt{\frac{0.035 \text{ seconds}}{3600 \text{ seconds}/hour}}} \quad (4)$$

$$ARW \times \le 0.18 \, {}^{\circ}/\sqrt{hour}$$

$$RND \le 0.18 \, {}^{\circ}/\sqrt{hour} \times \sqrt{2}/60$$

$$RND \le 0.0043 \, {}^{\circ\text{sec}}/\sqrt{Hz}$$

Angular Rate Noise vs. Bandwidth

Those who are developing systems that provide continuous pointing control may prefer to evaluate the noise impact in terms of angular rate, since they may not have a fixed integration time to leverage the ARW-based relationship. Evaluating the noise in terms of angular rate often involves some consideration of the RND parameter and the frequency response in the gyroscope's signal chain. The gyroscope's frequency response is often most influenced by filtering, which supports application-specific requirements for loop stability criteria and rejection of undesirable sensor response to environmental threats, such as vibration. Equation 5 provides a simple way to estimate the noise associated with a particular frequency response (noise bandwidth) and RND.

$$TN = \text{Total Noise}, \, {}^{\circ}/\text{sec} \; (rms)$$

$$TN = RND \times \sqrt{f_{NBW}}$$

$$where: \quad (5)$$

$$RND = \text{Rate Noise Density}, \, {}^{\circ\text{sec}}/\sqrt{Hz}$$

$$f_{NBW} = \text{Noise Bandwidth, Hz}$$

When the RND's frequency response follows a single-pole or double-pole, low-pass filter profile, the noise bandwidth (f_{NBW}) relates to the filter cutoff frequency (f_C) according to the relationships in Equation 6.

$$f_{NBW} = 1.57 \times f_C \text{ (single-pole, low-pass filter)}$$
$$f_{NBW} = 1.22 \times f_C \text{ (double-pole, low-pass filter)} \quad (6)$$

For example, Figure 4 offers two different spectral plots for the noise in the ADXRS290, which has an RND of 0.004°/sec/√Hz. In this plot, the blue curve represents the noise response when using a double-pole, low-pass filter, which has a cutoff frequency of 200 Hz filter, while the green curve represents the noise response when using a single-pole, low-pass filter, which has a cutoff frequency of 20 Hz filter. Equation 7 provides calculations for the total noise of each of these filters. As expected, the 200 Hz version has higher noise than the 20 Hz version.

$$TN = RND \times \sqrt{1.22 \times f_C}$$

$$TN_{200\,Hz} = 0.004 \, {}^{\circ\text{sec}}/\sqrt{Hz} \times \sqrt{1.22 \times 200}$$

$$TN_{200\,Hz} = 0.062 \, {}^{\circ}/\text{sec} \quad (7)$$

$$TN_{20\,Hz} = 0.004 \, {}^{\circ\text{sec}}/\sqrt{Hz} \times \sqrt{1.57 \times 20}$$

$$TN_{20\,Hz} = 0.022 \, {}^{\circ}/\text{sec}$$

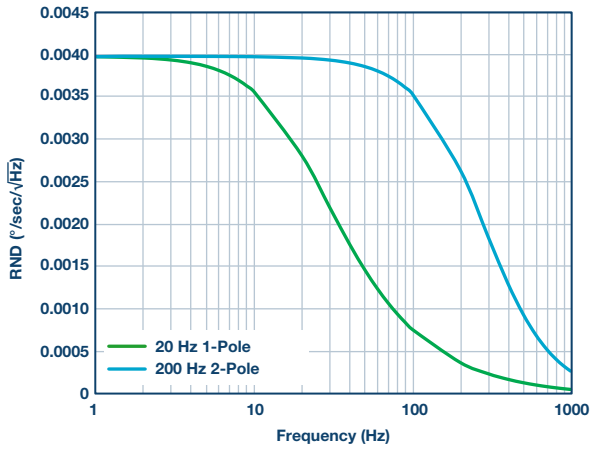


Figure 4. ADXRS290 noise density with filters.

In cases where the system requires custom filtering, whose frequency response ($H_{DF}(f)$) does not fit the simple single-pole and double-pole models in Equations 6 and 7, Equation 8 offers a more generic relationship for predicting the total noise:

$$TN = \sqrt{\int_0^F [RND^2(f) \times H_{DF}{}^2(f)] \times df} \quad (8)$$

In addition to influencing the total angular rate noise, gyroscope filters also contribute phase delay to the overall loop response, which has a direct impact on another important figure of merit in feedback control systems: phase margin at the unity-gain crossover frequency. Equation 9 offers a formula for estimating the phase delay (θ) that a single-pole filter (f_C = cutoff frequency) will have on the control loop's frequency response, at its unity-gain crossover frequency (f_G). The two examples in Equation 9 illustrate the phase delay at a unity-gain crossover frequency of 20 Hz, for filters with cutoff frequencies of 200 Hz and 60 Hz, respectively. This impact on phase margin can lead to specifying gyroscope bandwidths

that are 10× greater than the unity-gain crossover frequency, which can place even more emphasis on selecting a MEMS gyroscope with favorable RND levels.

$$\theta\,(f_G, f_C) = \text{a tan}\left(\frac{f_G}{f_C}\right)$$

$$\theta\,(20, 200) = \text{a tan}\left(\frac{20}{200}\right) = \sim 5.7° \quad (9)$$

$$\theta\,(20, 60) = \text{a tan}\left(\frac{20}{60}\right) = \sim 18.4°$$

Modern control systems often leverage digital filters, which may have different models for predicting their phase delay at critical frequencies for the control loop. For example, Equation 10 presents a formula for predicting the phase delay (θ) associated with a 16-tap FIR filter (N_{TAP}), which is running at the 4250 SPS (f_S) update rate of the ADXRS290, at the same unity-gain crossover frequency (f_G) of 20 Hz. This type of relationship can help in determining the total number of taps that a system architecture can allow for this type of filter structure.

$$\theta = \frac{N_{TAP} + 1}{2} \times \left(\frac{f_G}{f_C}\right)$$

$$\theta = \frac{16 - 1}{2} \times \left(\frac{20}{4250}\right) \times 360° \quad (10)$$

$$\theta = 12.7°$$

Conclusion

The bottom line is that noise in the angular rate feedback loops can have a direct influence on key performance criteria in motion control systems, so it should be a consideration as early as possible in the design process for a new system. Those who can quantify how angular rate noise will influence system-level behaviors will have a significant advantage over those who only know that they need low noise. They will be able to establish performance goals that create observable value in their applications, and they will be in an excellent position to quantify system-level consequences when other project objectives encourage consideration of a specific MEMS gyroscope. Once that basic understanding is in place, system designers can focus on identifying a MEMS gyroscope that meets their performance requirements, using bandwidth, rate noise density, or angle random walk metrics to guide their consideration. As they look to optimize the noise performance that they realize from the sensors they select, they can use the relationships with bandwidth (angular rate noise) and integration time (angle error) to drive other important system-level definitions that will support the most appropriate performance for the application.

Mark Looney [mark.looney@analog.com] is an *i*Sensor® applications engineer at Analog Devices in Greensboro, North Carolina. Since joining ADI in 1998, he has accumulated experience in sensor-signal processing, high speed analog-to-digital converters, and dc-to-dc power conversion. He earned B.S. (1994) and M.S. (1995) degrees in electrical engineering from the University of Nevada, Reno, and has published several articles. Prior to joining ADI, he helped start IMATS, a vehicle electronics and traffic solutions company, and worked as a design engineer for Interpoint Corporation.

Mark Looney

Also by this Author:

The Basics of MEMS IMU/Gyroscope Alignment

Volume 49, Number 1

Op Amp Input Overvoltage Protection: Clamping vs. Integrated

By Daniel Burton

Introduction

High precision op amps enable system designers to create circuits that condition signals (amplify, filter, and buffer) while maintaining the precision of the original signal. When information is contained in very small variations of the signal, it is critical that op amps in the signal path perform their operation while contributing very little dc and ac error. The precision of the total system depends on maintaining the precision of the signal path.

In some applications, a situation may occur in which the inputs of the op amp get driven by voltages outside the level of the supply voltages—this is called an overvoltage condition. For example, if an op amp is configured to run with its positive supply at +15 V and its negative supply at −15 V, any time an input pin goes more than one diode drop beyond those supply rails (such as ±15.7 V), the op amp's internal ESD protection diodes can be forward-biased and start conducting current. Excessive input current over long periods of time or even short periods of time, if the current is high enough, can damage the op amp. This damage can result in a shift in the electrical specification parameters beyond the data sheet's guaranteed limits; it can even cause a permanent failure of the op amp. When system designers are faced with this possible situation, they often add overvoltage protection (OVP) circuits at the inputs to the amplifier. The challenge then is to add OVP circuitry without adding errors (loss of system precision).

How Overvoltage Conditions Occur

Overvoltage conditions can be caused by a number of different situations. Consider a system where a remote sensor is located in the field—for example, measuring fluid flow in a refinery and sending its signal through a cable to data acquisition electronics that reside at a different physical location. The first stage in the data acquisition electronics signal path can often be an op amp configured as a buffer or a gain amplifier. The input to that op amp is exposed to the outside world and therefore can be subjected to overvoltage incidents, like a short circuit from a damaged cable or incorrectly connecting the cable to the data acquisition electronics.

Similarly, a situation that can cause an overvoltage condition is when an input signal that is usually within the input voltage range of the amplifier suddenly receives an external stimulus causing a transient spike that exceeds the op amp's supply voltages.

A third scenario that can result in an input overvoltage condition comes from the power-on sequence of the op amp and other components in the signal path. For example, if the signal source, such as a sensor, gets powered up before the op amp does, the output of the source can start to output a voltage that will then be applied to the input of the op amp even though the op amp supply pins have no power yet and are essentially at ground. This will create an overvoltage situation and likely force excessive current through the input of the op amp to ground (the unpowered supply pins).

Clamping: a Classic Overvoltage Protection Technique

A very popular way to add OVP is shown in Figure 1. When the amplitude of the input signal (V_{IN}) exceeds one of the supply voltages plus the forward voltage of a diode, the diode (D_{OVPP} or D_{OVPN}) will forward bias and send the current to the supply rails rather than into the op amp inputs where the excess current could damage the op amp. In this application, we are using an ADA4077, an extremely high precision op amp with a maximum power supply range of 30 V (or ±15 V).

The clamping diodes are 1N5177 Schottky diodes because they have a forward voltage of approximately 0.4 V, which is less than the forward voltage of the of the op amp's input electrostatic discharge (ESD) protection diodes; thus, the clamping diodes will start conducting current before the ESD diodes do. The overvoltage protection resistor, R_{OVP}, limits the forward current through the clamping diodes to keep them under their maximum current rating, preventing them from being damaged by excessive current. The resistor R_{FB} in the feedback loop is there because any input bias current on the noninverting input can cause an input voltage error across R_{OVP}—adding R_{FB} will null out the error by generating a similar voltage on the inverting input.

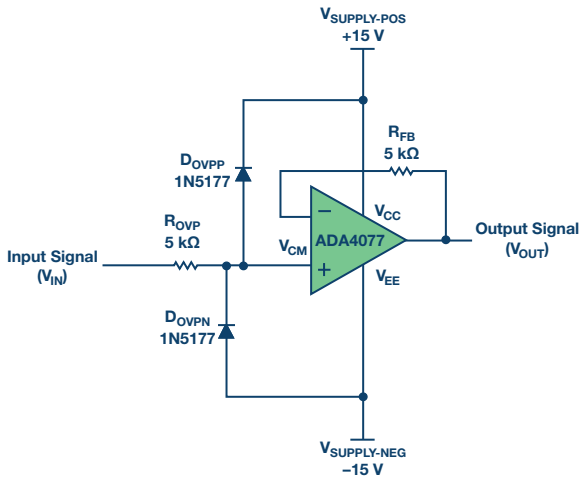


Figure 1. Classic clamping circuit for overvoltage protection.

The Trade-Off of a Diode Clamping Circuit—Reduced Precision

Although the classic circuit in Figure 1 protects the op amp inputs, it contributes a significant amount of error to the signal path. Precision amps generally have input offset voltages (V_{OS}) in the microvolts range. For example, the maximum V_{OS} for an ADA4077 is 35 µV over the full operating temperature range of –40°C to +125°C. Adding the external diodes and an overvoltage resistor contributes an input offset error that can be many times greater than the low offset inherent to the precision op amp.

Reverse-biased diodes exhibit a reverse leakage current that flows from the cathode through the anode to the supply.

When the input signal voltage (V_{IN}) is between the supply rails, the diodes D_{OVPP} and D_{OVPN} have a reverse voltage on them. With V_{IN} at ground (the middle of the input voltage range), the reverse current through D_{OVPN} is approximately equal to the reverse leakage current through D_{OVPP}. However, when V_{CM} moves above or below ground, a larger reverse current flows through one diode than the other. For example, when V_{CM} is at the top of the op amp's input voltage range, which is 2 V from the positive supply or 13 V in this circuit, diode D_{OVPN} will have a reverse voltage of 28 V across it. According to the 1N5177 diode's data sheet, this can cause a reverse leakage current of close to 100 nA. As reverse leakage current flows from the input signal (V_{IN}) through R_{OVP}, it will create a voltage drop across R_{OVP} that looks exactly like an increased input offset voltage to the signal path.

Of additional concern is that diode reverse leakage current increases exponentially with an increase in temperature, causing an increase in the offset voltage penalty of the clamping OVP circuit. As a baseline of comparison for op amp precision with no external overvoltage circuitry, Figure 2 shows the measured offset voltage of the ADA4077 over an input voltage range from −13 V to +13 V. The measurements were performed at three temperatures: 25°C, 85°C, and 125°C. Note that at 25°C, the V_{OS} of the ADA4077 used in this test reached only 6 µV; even at 125°C, the V_{OS} is only approximately 20 µV. When we add the external clamping OVP circuit to the same ADA4077 device and apply the input at V_{IN}, we see the results shown in Figure 3. At room temperature, the V_{OS} jumps to 30 µV—five times the signal path error of the ADA4077 alone. At 125°C, V_{OS} goes to over 15 mV—an increase of 750 times the 20 µV of the ADA4077! Precision is gone.

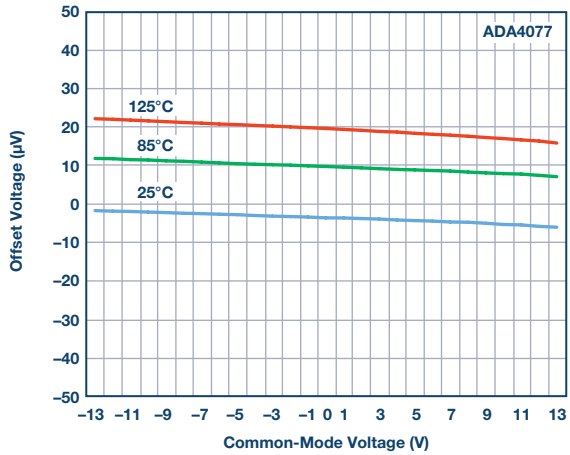


Figure 2. Input offset voltage vs. input voltage for ADA4077.

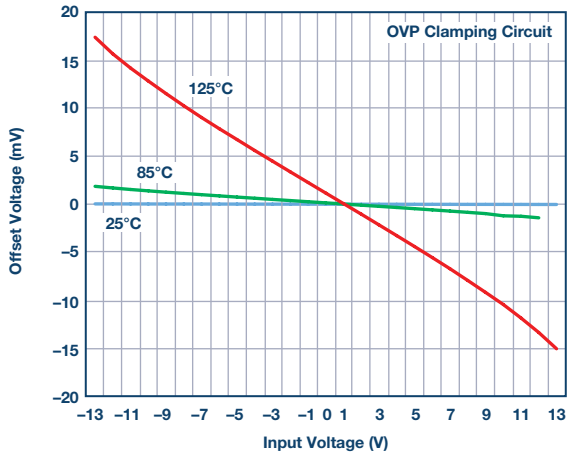


Figure 3. Input offset voltage vs. input voltage for an OVP clamping circuit added to ADA4077.

The 5 kΩ resistor does a great job protecting the clamping diodes as well as the op amp during an overvoltage condition but it adds quite a bit of offset error during normal operation when the diodes are leaking current across it (not to mention Johnson noise from the resistor). What we would like is a dynamic input resistance that has low resistance during operation within the specified input voltage range but high resistance during overvoltage conditions.

An Integrated Solution Provides the Answer

The ADA4177 is a high precision op amp that includes integrated overvoltage protection. The integrated ESD diodes act as overvoltage clamps to protect the part. Depletion mode FETs are in series at each input before the ESD diodes. They provide the dynamic resistance, which increases when the input voltage (V_{CM}) exceeds the supply voltages. As input voltage increases, the drain-to-source resistance (R_{DSON}) of an internal FET increases, thus restricting the current flow exponentially with the increased voltage (shown in Figure 4). Because the ADA4177 uses depletion mode FETs on the inputs and not a series protection resistor, the op amp doesn't suffer the offset voltage penalty across the resistor that the clamping OVP circuit does.

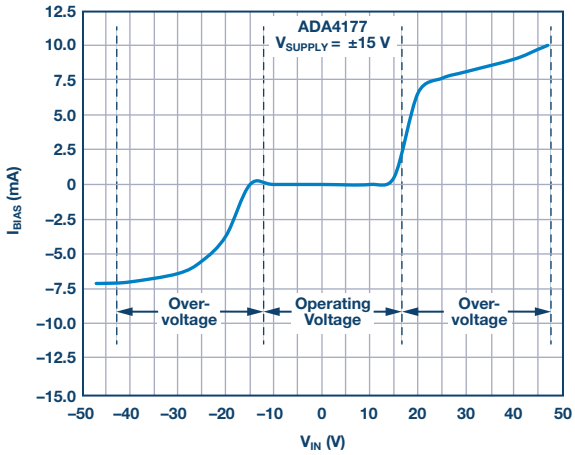


Figure 4. ADA4177 input bias current is restricted as overvoltage increases.

The ADA4177 can withstand voltages on its inputs of up to 32 V beyond the supply voltage. It limits overvoltage current to a typical 10 mA to 12 mA, protecting the op amp without the use of any external components. As shown in Figure 5, even at 125°C this tested unit is showing an offset voltage of only 40 µV. That's less than 3% of the error that the clamping circuit showed at that temperature. Precision is maintained!

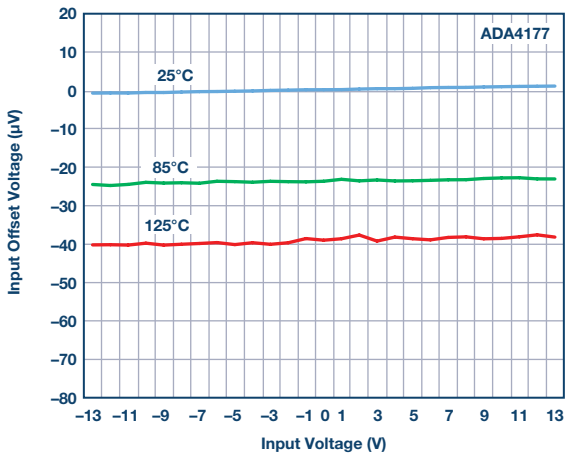


Figure 5. Input offset voltage vs. input voltage for ADA4177 with its integrated OVP.

What This Means to System Performance

When analyzing the effect of varying input voltage on the precision of the signal path, a system designer will consider the amplifier's common-mode rejection ratio (CMRR). This is a measure of how much of the common-mode input voltage is rejected from showing up on the output (or how little gets through). Since op amps are often configured to provide gain between the input and the output, we normalize the CMRR specification by referring to change in the input offset voltage, which is the change in output divided by the amplifier's closed-loop gain. The common-mode rejection ratio is a positive value expressed in dB and is calculated by the following formula:

$$CMRR = 20 \log (\Delta V_{CM}/\Delta V_{OS})$$

From this ratio, we see it is clearly desirable to keep the V_{OS} as small as possible. The ADA4177 is specified to have a guaranteed minimum CMRR limit of 125 dB over full operating temperature. Using the test results from the units measured in this experiment, we can calculate and compare the CMRR of the clamping circuit and the ADA4177. Table 1 shows the extreme loss of precision when using the classic clamping diode circuit and the excellent CMRR of the ADA4177 with its integrated FET overvoltage protection.

Table 1. CMRR Comparison of ADA4177 to Discrete OVP with Clamping Diodes

Overvoltage Protection Method	25°C	85°C	125°C
ADA4177	143 dB	145 dB	142 dB
ADA4077 and Clamping OVP	113 dB	78 dB	58 dB

References

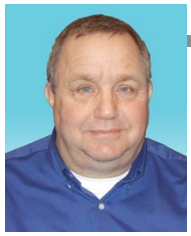
Arkin, Michael and Eric Modica. "Robust Amplifiers Provide Integrated Overvoltage Protection." *Analog Dialogue,* Volume 46, Number 1, 2012.

Video: "ADA4096-2 Input Overvoltage Protection Amplifier." Analog Devices, Inc.

Video: "ADA4177: Op Amp with OVP and EMI Provides Robustness and Precision." Analog Devices, Inc.

For more information on the ADA4177 and ADA4077, see the product pages and data sheets here: ADA4177 and ADA4077.

Daniel Burton [daniel.burton@analog.com] is an applications engineer at Analog Devices. He acquired his B.S.E.E. from San Jose State University and he has worked on sensing and precision linear signal paths for much of his career. Dan has been with Analog Devices since 2010, focusing on precision amplifiers and voltage references.



Daniel Burton

Electromagnetic Flow Meters: Design Considerations and Solutions

By Colm Slattery and Ke Li

Where Are Flow Meters Used in Industry Today?

"If you can't measure it, you can't manage it." An often heard quote in industry and particularly relevant to flow measurement. Simply stated, there is an increasing need to monitor more flow and often with more speed and accuracy. There are a few areas where industrial flow measurement is important, such as residential waste. With more and more focus on protecting our environment, the disposal and monitoring of waste is critical as we strive to create a cleaner and less polluted world. Humans are consuming vast quantities of water and this will continue as the world population grows. Flow meters are critical in both monitoring the residential effluent waste as well as being an integral part of the process control system in wastewater treatment plants.

Flow meters also find homes in many industrial control processes, including chemical/pharma, food and beverage, and pulp and paper. Such applications often have the need to measure flow in the presence of high levels of solids—not easily achieved by most flow technologies.

High end flow meters are needed in the area of custody transfer, which deals with the transfer and payment of a product transfer between two parties. An example would be oil transfer through a large pipeline. Here, even a small change in the accuracy of the flow measurement over time can result in significant revenue lost or gained for one of the parties.

Why Is Electromagnetic Induction Technology a Good Fit for Liquid Flow Measurement?

This technology has a number of advantages when it comes to liquid flow measurement. The sensors are generally inserted in line into the pipe's diameter, and are therefore designed such that they do not disturb or restrict the flow of the medium under measurement. As the sensors are not directly immersed in the liquid—there are no moving parts—there are no wear and tear concerns.

The electromagnetic method measures the volume flow, which means the measurement is insensitive to changes in effects such as fluid density, temperature, pressure, and viscosity. Once the electromagnetic flow meter is calibrated with water, it can be used to measure the other types of conductive fluid—with no additional correction. This is a significant advantage that other types of flow meters don't have.

Electromagnetic technology is particularly suitable for measuring within a solid-liquid two-phase medium, such as a liquid with suspended dirt, solid particles, fibers, or viscosity within a heavily conductive medium such as slurry. It can be used to measure the sewage, mud, ore pulp, paper pulp, chemical fiber slurry, and other media. This makes it particularly suitable, for example, to the food and pharmaceutical industry, where it can measure the flow of corn syrup, fruit juice, wine, medicine and blood plasma, and many other special media.

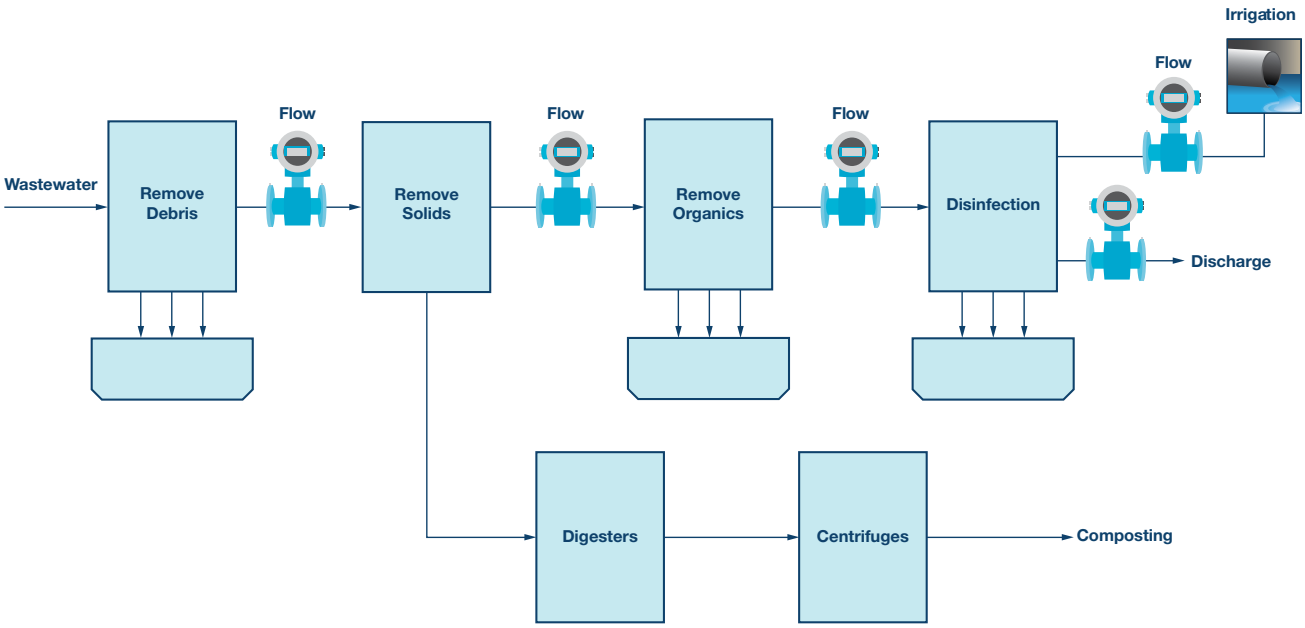


Figure 1. Simplified wastewater treatment plant.

How Does the Technology Work?

The working principle of a magnetic flow meter is based on Faraday's law of electromagnetic induction. According to Faraday's law, when the conductive fluid flows through a magnetic field of the sensor, an electromotive force proportional to the volume flow is generated between the pair of electrodes, which is perpendicular to the flow direction and the magnetic field. The amplitude of the electromotive force can be expressed as:

$$E = kBDv$$

Where E is the induced electric potential, k is a constant, B is the magnetic flux density, D is the inner diameter of the measuring tube, and v is the average velocity of the fluid in the axial direction of the electrode cross-section inside the measuring tube.

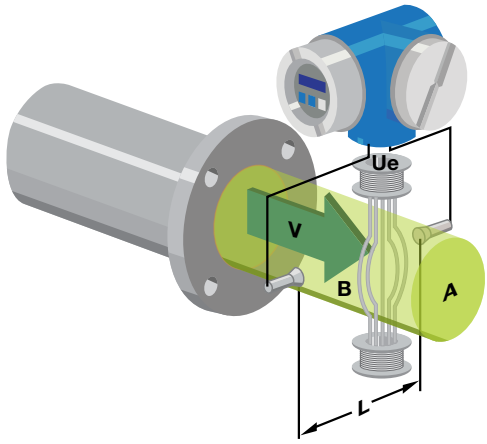


Figure 2. Working principle of the magnetic flow meter.

What Is the Output Range of the Sensor?

The sensor has a differential output. Its sensitivity is typically 150 microvolts/(mps) to 200 microvolts/(mps). Since the excitation current alternates its direction, the sensor output signal amplitude doubles. For the flow rate measurement range of 0.5 meters/second to 15 meters/second, the sensor output signal amplitude ranges from 75 microvolts to approximately 4 mV to 6 mV. Figure 3 shows the sensor output signal when being excited with constant current source and with fluid flowing through the sensor. The scope plot captured on the sensor output leads shows a very low level signal sitting on significant common-mode voltage. The purple trace is for the positive electrode and the red trace is for the negative electrode. The pink trace is the math channel that subtracts the positive and negative electrodes. The low level signal sits in the significant common mode.

What Is the Traditional Approach to Measuring the Sensor?

The traditional approach has been very much an analog one—a preamplifier stage with a high input impedance to mitigate against sensor leakage effects and with high input common-mode rejection, followed by a 3rd or 4th order analog band-pass filter, a sample-and-hold stage, and finally an analog-to-digital conversion. A typical analog front-end approach is shown in Figure 4. The sensor output signal is firstly amplified by an instrumentation amplifier. It is crucial to amplify the interested signal as much as possible, but also to avoid the amplifier output saturation by the unwanted dc common-mode voltage. This usually limits the gain of the first stage instrumentation amplifier to no more than ×10. A band-pass filter stage further removes dc effects and reamplifies the signal into to a sample-and-hold circuit—it is this difference signal, representing flow rate—that is then sent to an analog-to-digital converter.

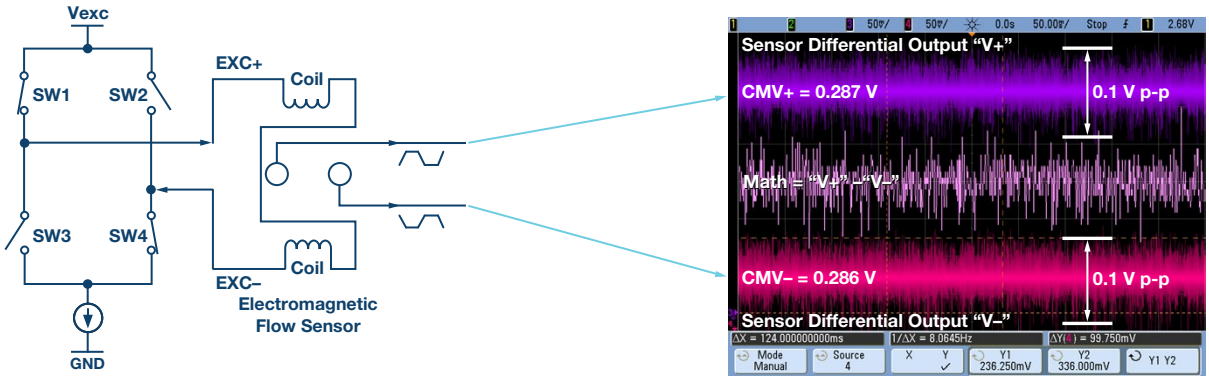


Figure 3. Output signal of electromagnetic flow sensor.

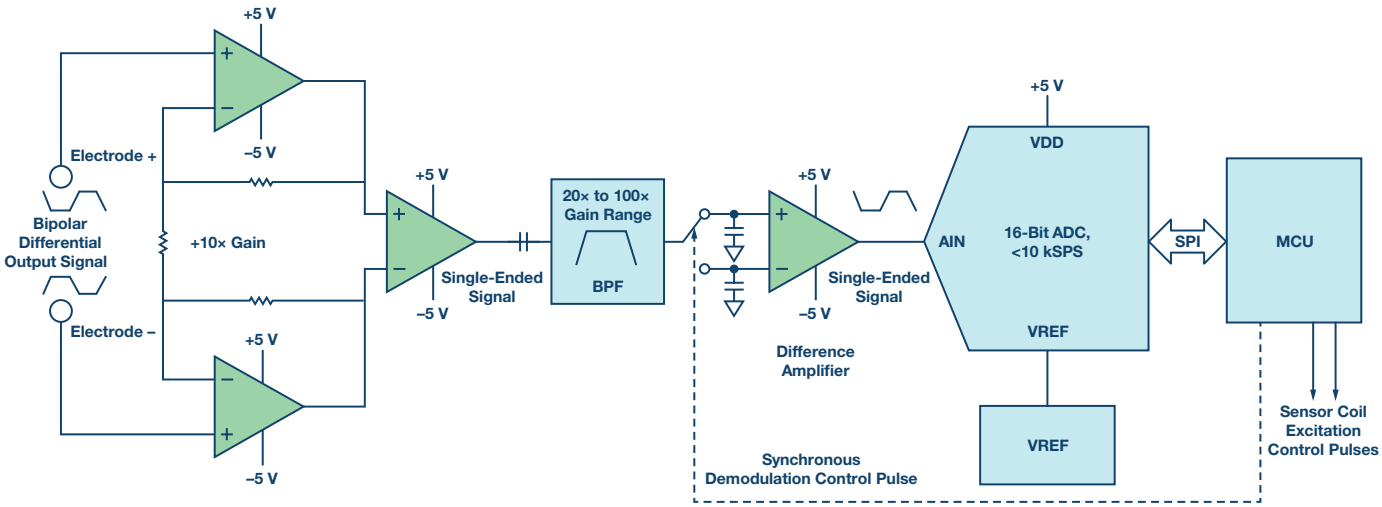


Figure 4. Traditional analog front-end approach.

What Are the Trends in the Market That Are Influencing Changes in the Electromagnetic Flow Meter Architecture?

There are multiple industry trends driving the need for a new architecture. One is the ever increasing need for more data. The ability to monitor other attributes in liquid other than flow is becoming more and more valuable. This may be, for example, to determine what contaminants may be in the liquid, or it may be to determine whether the liquid has the correct density/viscosity for the application. There are many such requirements and benefits of adding such diagnostics. It is not possible with the traditional analog approach to extract such information easily as most of the sensor information is lost during the synchronous demodulation phase.

There is also a continuing demand for increased productivity and efficiency in the manufacturing process. In a liquid dosing/filling application, for example, more and more filling nodes are being added, and as manufacturing processes scale, and the speed of the filling increases, this drives the need for faster and more accurate flow monitoring.

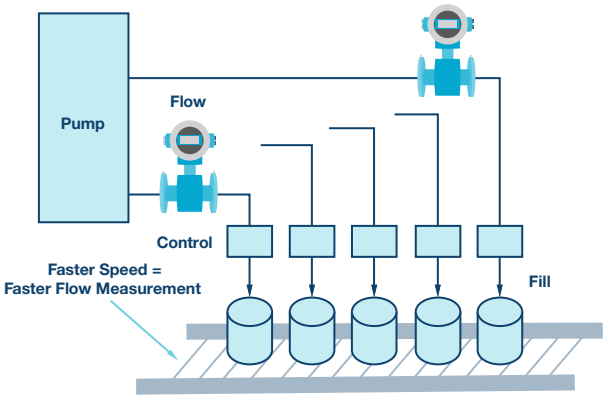


Figure 5. Liquid dosing/filling.

Traditionally, mechanical or weight technology has been used to determine the right amounts of liquid to add as part of either the dosing process or to determine exact fill amounts as part of the production process. These tend to be quite expensive and are difficult to scale. To meet this demand, flow meters, and EM flow in particular where liquids are concerned, have become the technology of choice.

What Does the New Architecture Look Like?

The oversampled approach greatly simplifies analog front-end design. The analog band-pass filter and the sample-and-hold stages can be removed. The front-end amplifier in the circuit now consists of only the one stage instrumentation amplifier—in our case, the AD8220 JFET input stage rail-to-rail output instrumentation amplifier, which can be directly connected to a high speed Σ-Δ converter.

What Is Important to the Analog Front End and How Does That Influence My Design?

The amplifier and the ADC are two of the most critical blocks in this application. The first stage amplifier has a number of key requirements.

One requirement is the common-mode rejection ratio (CMRR). The ions in the liquid electrolyte make directional movement, so electrical potential is developed between the electrodes and the fluid, which is what we call polarization. The electrical potential on the electrodes should equal each other if both electrodes are perfectly matched. The polarization voltages for different metals range from a few hundred mV to ±2 V. This is the dc common-mode voltage appearing at the sensor output and the input of the preamplifier. The preamplifier is key in rejecting this common mode.

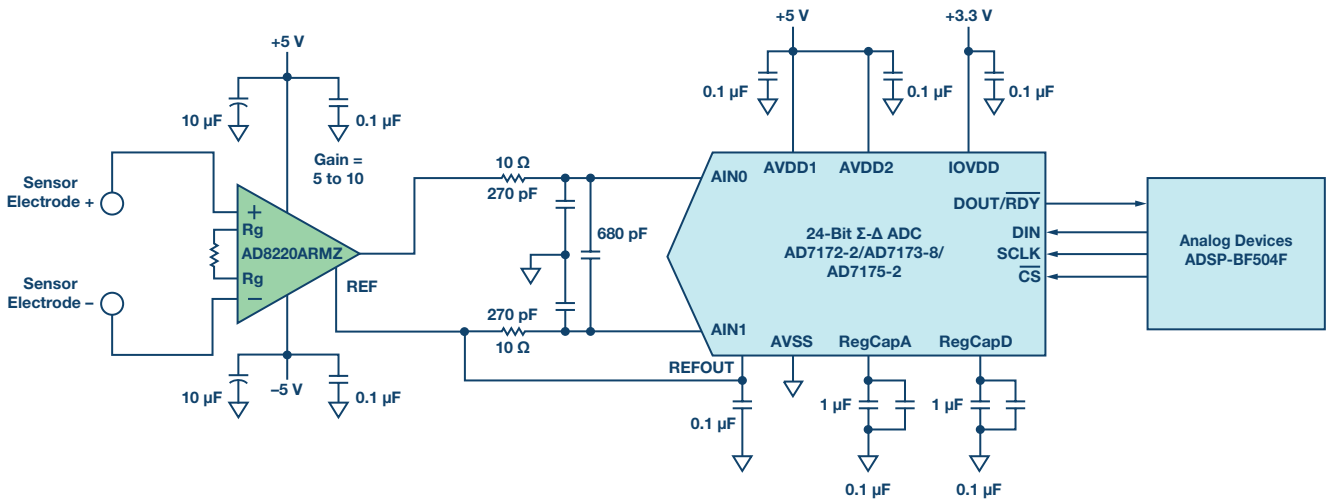


Figure 6. Oversampling architecture analog front end with AD8220 and AD717x-x.

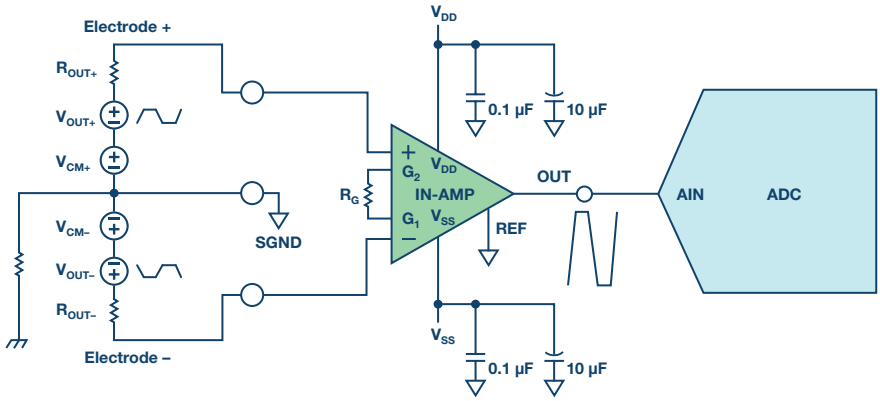


Figure 7. Common mode rejected by the preamplifier.

Table 1. Effects of Common-Mode Rejection on Actual Flow Rate

	CMRR vs. CMV DC and Noise After Rejection			
Common-Mode Rejection Ratio	120 dB	100 dB	80 dB	60 dB
0.28 V_{DC} Common-Mode	0.28 µV	2.8 µV	28 µV	280 µV
0.1 V Common-Mode Noise	0.1 µV	1 µV	10 µV	100 µV
Common-Mode Noise Translated into the Flow Rate of a 175 µV/(mps) Sensor	0.0006 mps	0.006 mps	0.06 mps	0.6 mps

Table 2. Effects of Amplifier Input Impedance on Flow Rate

Sensor Output Impedance (GΩ)	Amplifier Input Impedance (GΩ)	Reduced Signal Amplitude for 1 mps (µV)	Repeatability (%)	Error of Reading (%)
10	10	87.50	0.065%	0.196%
10	100	15.91	0.051%	0.154%
10	1000	1.73	0.049%	0.148%
10	10,000	0.17	0.049%	0.147%

A 100 dB CMRR would attenuate the 0.3 V_{DC} common mode to 3 µV, which is presented as a dc offset on the amplifier output that can subsequently be calibrated out. In an ideal scenario the common-mode voltage on the sensor would remain constant, but in reality it will change over time and be influenced by other effects such as liquid quality or temperature. The higher the CMRR, the better it will reduce the need for continuous background calibration and improve flow stability.

The metal material of the electrodes contact the electrolyte liquid. The frictions between the liquid electrolyte and the electrodes create ac common-mode voltages in higher frequencies. Though usually in smaller amplitudes, the ac common mode appears as a noise that is totally random and, thus, is more difficult to reject. This requires the preamplifier to have good CMRR not only on the dc range, but also in higher frequencies. AD8220 amplifier has excellent CMRR from dc to 5 kHz. For the AD8220 B grade, the minimum CMRR is 100 dB on dc to 60 Hz, and 90 dB up to 5 kHz, which rejects the common-mode voltage and noise to well around microvolt. With 120 dB CMRR, the 0.1 V p-p is reduced to 0.1 µV p-p. Table 2 shows the effect of poor CMRR rejection on the output sensor signal.

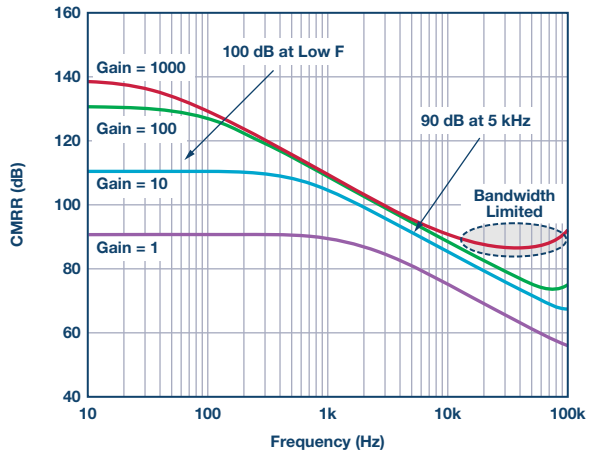


Figure 8. AD8220 dc and ac rejection of common-mode effects.

The low leakage current and high input impedance of the preamplifier stage is another critical parameter because the output impedance of the electromagnetic flow sensor could be as high as GΩ. High input impedance of the amplifier can avoid loading the sensor output too much that results in a reduced signal amplitude. The amplifier should have the leakage current low enough so that it won't become a notable error source when flowing through the sensor. The 10 pA maximum input bias current and 10^{13} Ω input impedance of AD8220 make the part capable of dealing with a wide range of output characteristics for electromagnetic flow sensors. Table 2 lists what impact the preamplifier's input impedance has to a high output impedance sensor of 10 GΩ.

Finally, the 1/f noise on the range of 0.1 Hz to 10 Hz sets the noise floor for the application. When configured to a gain of 10 the referred-to-input voltage noise of AD8220 is about 0.94 µV p-p, which resolves 6 mm/sec instantaneous and the sub-mms accumulative flow rate.

How Do I Choose My ADC and What Is Important Here in the Application?

The oversampling approach does bring challenges and pushes the performance requirement of the ADC block. With no secondary analog filter active gain stage, only a small portion of the ADC input range is used. Oversampling and averaging itself does not allow for dramatically increased performance as each sensor cycle needs to fully settle to be used for a flow calculation. Further, you need enough analog-to-digital samples from these limited data points to remove unexpected glitches as part of the firmware process.

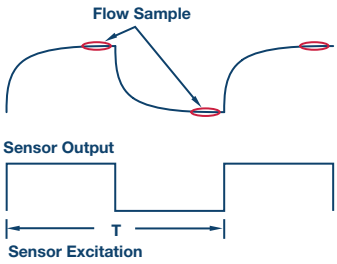


Figure 9. Flow signal sampling.

The oversampling architecture generally requires an ADC rate of >20 kSPS data rate—though the faster the better. This is not specifically related to the actual flow measurement. As there is no analog band-pass filter stage the raw sensor output is effectively seen by the ADC input. In this case, as the sensor's rising edges are not filtered, the ADC needs to have enough resolution during the rising and falling edges to capture these edges accurately enough.

The flow meter's accuracy itself can be determined as either an instantaneous flow measurement or an accumulative flow measurement. The flow meter standard uses the accumulative flow technique—measuring the average flow of a volume of water over a long period of time, say for 30 or 60 seconds. This, rather than the instantaneous flow measurement, determines the ±0.2% system accuracy. The instantaneous flow is applicable to the occasions where the real-time flow rate is important. It demands much higher levels of accuracies from the electronics. In theory, to resolve to 5 mm/sec instantaneous flow resolution the ADC will need to achieve 20.7-bit p-p resolution during one excitation period—a post-FIR filter of approximately 600 samples. This can be achieved by the analog front end.

The AD7172-2 provides the perfect combination of low input noise and high speed sampling for electromagnetic flow applications. The typical noise of AD7172-2 with 2.5 V external reference can be as low as 0.47 µV p-p. This means the final flow results can be refreshed at up to 50 SPS without the addition of extra amplification stages. Figure 10 shows the noise plots of the oversampling front-end circuit with AD7172-2.

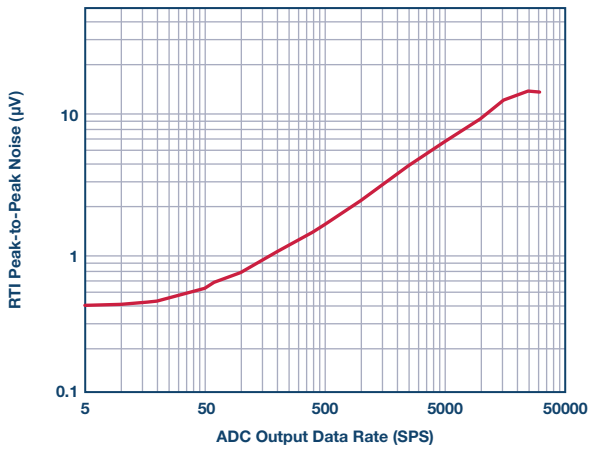


Figure 10. Test results of referred-to-input noise for oversampling architecture with AD8220 and AD7172-2.

Table 3. Noise Budget for an Analog Front End and ADC

Flow Rate Resolution for Sensor of 175 µV/(mps) Sensitivity	Signal Amplitude of Sensor Output at the Resolution	Budget for Referred-to-Input Noise of Analog Front End	ADC Noise Budget at 10 Gain of Oversampling Analog Front End
10 mm/sec	3.5 µV p-p	1.75 µV p-p	5.8 µV p-p/19.7 bit*
5.4 mm/sec	1.89 µV p-p	0.95 µV p-p	3.2 µV p-p/20.6 bit*
5 mm/sec	1.75 µV p-p	0.88 µV p-p	2.9 µV p-p /20.7 bit*

*Data from one FIR filter cycle and one instantaneous flow calculation.

Table 4. Comparison of Measurement Accuracy Over Sensor Excitation Frequency

Excitation Frequency (Hz)	6.25	12.5	25	50	100	200	400
With AD7172-2	0.12%	0.12%	0.13%	0.16%	0.19%	0.24%	0.33%
With Closest Competition	0.13%	0.15%	0.19%	0.25%	0.33%	0.46%	0.64%
Gap	12%	22%	47%	57%	77%	89%	95%

How Can We Get Faster Response to Meet Industry Needs for Higher Efficiency?

It's possible to increase the system update rates of the flow measurement by increasing the sensor excitation frequency. In this condition, there is less time when the sensor output is *settled*, and therefore less available samples to average. With an ADC of lower noise, the referred to sensor output noise can be further reduced. Using the same front-end driver, AD8220, configured in a gain ×10, the analog front-end performance can be benchmarked against the leading competition at higher update rates. Table 4 and Figure 11 show ADI's advantage gained at higher system update rates vs. the closest competitor.

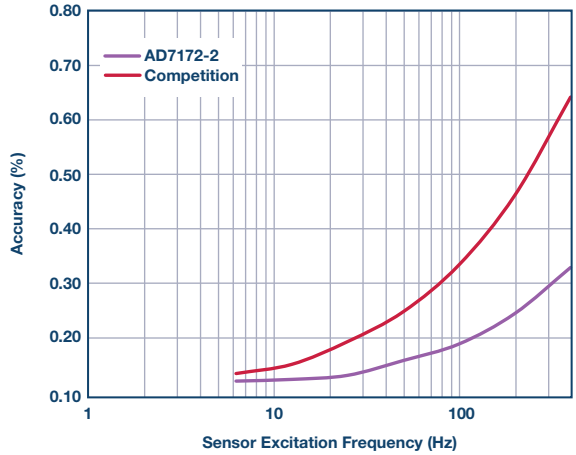


Figure 11. Comparison of measurement accuracy over sensor excitation frequency.

Will the In-Amp Be Able to Directly Drive the ADC and How Can I Be Sure of This?

Generally, this depends on the driving capability of the in-amp and the ADC's input structure. Many modern precision ADCs are based on a switched-capacitor architecture. The on-chip track-and-hold appears as a transient load to the upstream amplifier that it must be able to settle the switched-capacitor inputs to allow for accurate sampling.

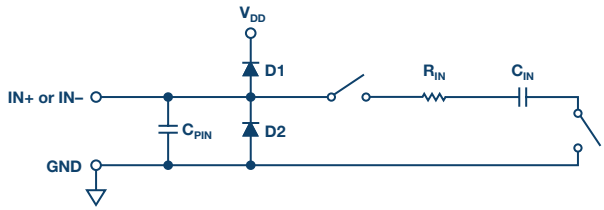


Figure 12. Equivalent analog input circuit.

The following equation can be used to check if the amplifier is to drive the ADC.

$$BW = 1/(2\pi \times (1/(2 \times MCLK) - T)) \times \ln[(FS - CMV)/(FS \times Error)]$$

Where:

BW is the minimum bandwidth required for the amplifier to drive the ADC.

MCLK is the ADC modulator clock frequency, Hertz.

T is the shorting phase time, seconds.

FS is the ADC full analog input range, volts.

CMV is the common-mode voltage of the ADC input range, volts.

Error is the settling error for the ADC sampling.

The AD7172-2, for example, has a modulator frequency of 2 MHz, a shorting phase time of 10 ns, a full input range of 5 V, a CMV of 2.5 V, and a settling error of 1 ppm. The resulting BW figure is 8.7 MHz, which would be required for the driver amplifier when AD7172-2 is in the unbuffered mode. This exceeds 1.7 MHz—the gain-bandwidth product capability of the AD8220 as well as many precision instrumentation amplifiers. The AD7172-2 has true rail-to-rail, integrated, precision unity-gain buffers on both ADC analog inputs. It is designed to drive the AD7172 input stage across all frequencies, and reduces the design complexity and risk for our customers. The buffers provide high input impedance with only 5 nA typical input current, allowing high impedance sources to be connected directly to the analog inputs. The buffers fully drive the internal ADC switch capacitor sampling network, simplifying the analog front-end circuit requirements while consuming a very efficient 0.87 mA typical per buffer. Each analog input buffer amplifier is fully chopped, meaning that it minimizes the offset error drift and 1/f noise of the buffer.

How Is the Magnetic Field Generated?

The magnetic field inside the measurement pipe is generated by applying the constant current through the coils that are installed next to the outside of the pipe. The coils often exist in pairs and are connected in series to each other. The coils are usually hundreds of turns of copper wire and thus are seen as a significant inductance load by its driver circuit. The coil inductances are typically around tens of to hundreds of millihenry plus 50 Ω to 100 Ω dc series resistance. The magnetic field alternates its direction within each cycle when the driver circuit changes the direction of the excitation current, which is done by turning on and off the different pair of switches on the H-bridge. The alternating frequency is generally an integer fraction multiple of the power-line frequency for noise cancelation. The driver circuit consists of a constant current source and an H-bridge under the control of the microprocessor.

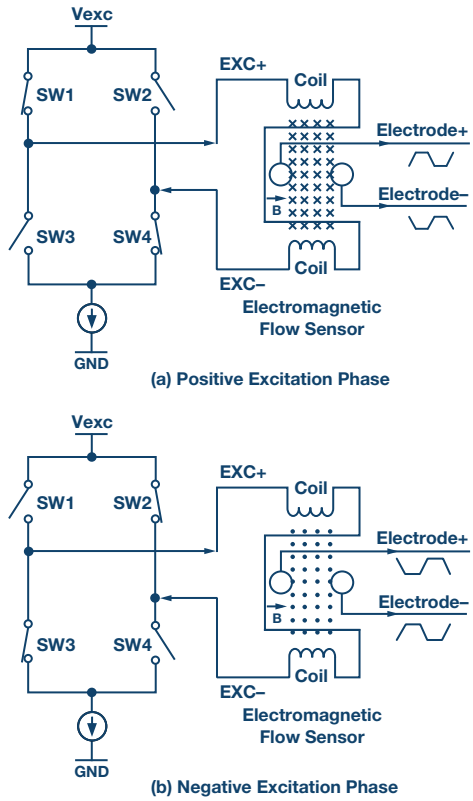


Figure 13. Magnetic field generation.

Is Power Dissipation Important?

Yes. The excitation currents for electromagnetic flow meters can be quite large, from up to 50 mA for smaller diameters up to 500 mA or 1 A for larger diameter pipes. The constant current circuit can consume a significant amount of power and board area when it's linearly regulated.

A switch-mode power supply can be used to save the power dissipated compared to the linear regulated constant current circuit. As shown in the diagram, ADP2441 is configured in the constant current source output mode. The 1.2 V ADR5040 output voltage is divided by two resistors to 150 mV. This 150 mV voltage is applied to the ADP2441 voltage track pin so that the voltage feedback pin will also be kept to 150 mV. When putting a 0.6 Ω current set resistor at the feedback pin, the ADP2441 will adjust its output current to its I_{SET} level. By adjusting the value of the current setting resistor connected to ADP2441 feedback pin, the constant current source can be tuned.

Table 5. Recommended Switching Regulators

Recommended ADI Switching Regulators	Efficiency
ADP2441	90% at 200 mA output (at 12 V), up to 1 A capable
ADP2360	90% at 10 mA output, up to 50 mA capable

Are There Any Other Benefits of This Drive Stage Design?

There are significant area benefits. Electromagnetic flow sensor driver circuits, also called excitation circuitry, are usually isolated from the signal conditioning circuit—1 kV basic isolation typically suffices. Conventional electromagnetic flow transmitters commonly use optical coupler isolation. Optocouplers tend to have poor reliability and are quite large. The ADuM7440 digital isolator combines high speed CMOS and monolithic air core transformer technology, providing four independent isolation channels in a small, 16-lead QSOP package.

Compared with the conventional scheme using an optical coupler, linear regulated constant current source, and discrete FET H-bridge in through-hole package, the power savings using the digital isolation approach could save more than 80% of the circuit area.

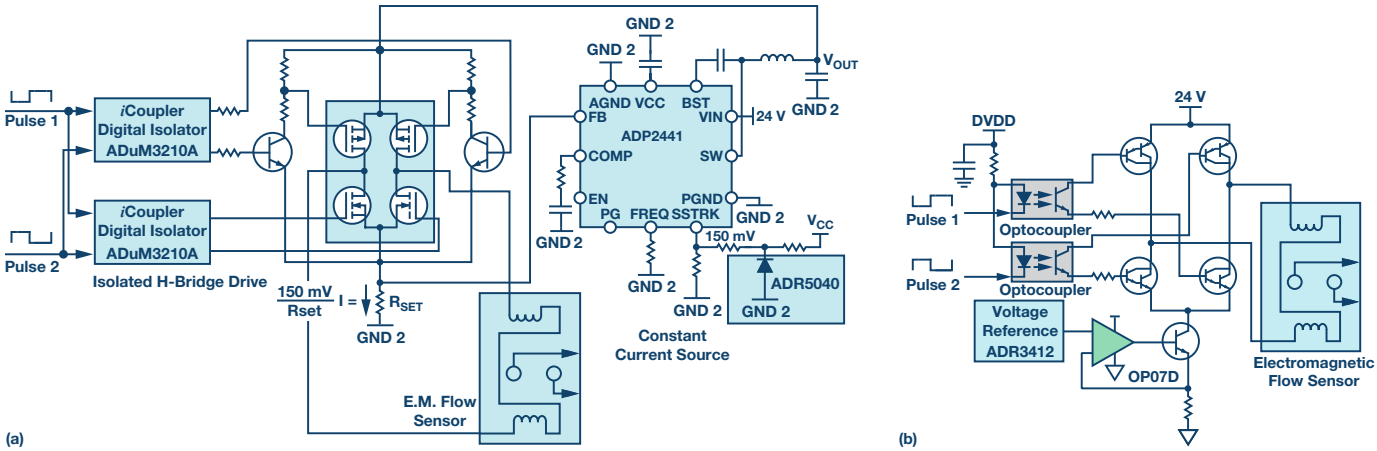


Figure 14. (a) Drive isolated H-bridge with SMPS and iCoupler.®
(b) Drive isolated H-bridge with linear regulated current source and optocoupler.

How Is Flow Rate Calculated?

In the digital domain, the ac flow signal will still need filtering and synchronous demodulation. Figure 15 illustrates how the algorithm implements the synchronous demodulation in the digital domain. A DSP issues Control Signal 1 and 2, a pair of complementary logic signals for the electromagnetic flow sensor coil excitation. Under the control of these two signals, the current flowing through the electromagnetic flow sensor coil reverses in each cycle—thus the direction of the magnetic field and therefore the sensor output on the electrodes also reverses in each cycle too.

Table 6. Key Component Comparison Used During the H-Bridge Drive Stage

Components	Qty	Package	Area (mm²)
PC817B	2	DIP-4	63.24
TIP127, PNP Darlington	2	TO-220	51.54
TIP22, NPN Darlington	2	TO-220	51.54
Total Area			333

Components	Qty	Package	Area (mm²)
ADUM7440ARQZ	1	QSOP-16	31
ZXMHC6A07N8	1	SOIC-8	31
MMBT3904LT1G	2	SOT-23	13.92
1SMA5917BT3G	1	SMA	13.55
Total Area			103.39

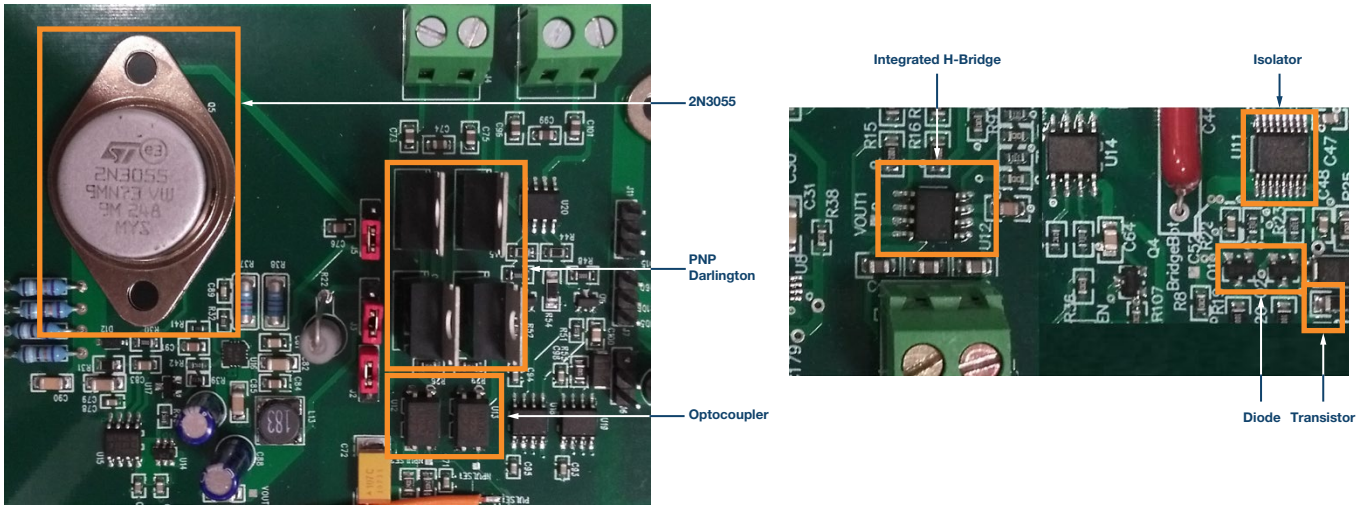


Figure 15. Area comparison of optocouplers vs. digital isolator design.

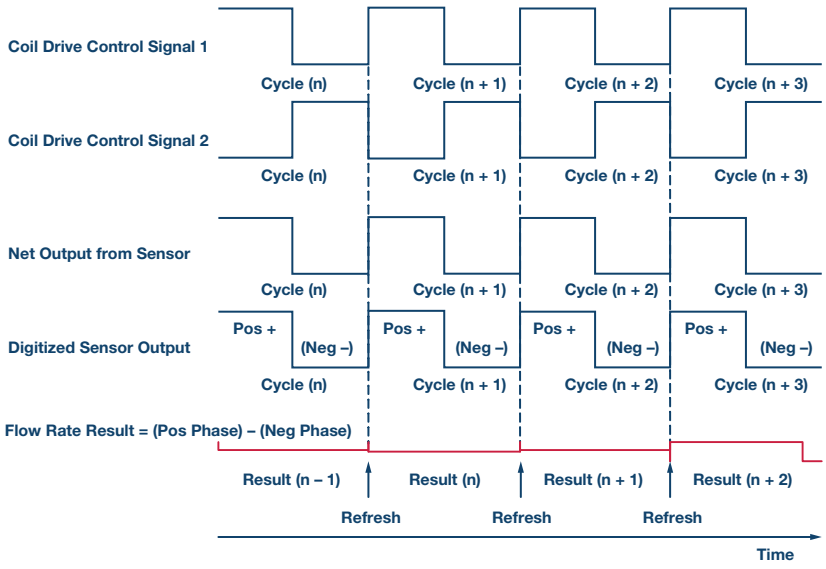


Figure 16. Synchronous demodulation and flow rate calculation in digital domain.

In the n[th] cycle, for example, the DSP (in our case, ADSP-BF504F) knows the timing and logic of Control Signal 1 and 2 when the ADC samples are coming in. This allows the DSP to sort these ADC samples in accordance with the logic status of the coil driving control signals into two arrays in the SRAM. That is, those time-stamped samples that are obtained during the positive half cycle are sorted into one group and those samples that are acquired in the negative half cycle are sorted into another group. Each set is subsequently passed through an FIR (finite impulse response) low-pass filter. The filter's cutoff frequency is set at 30 Hz, allowing the useful signal to pass rejecting the interferences of the power-line frequency and high frequency noise components. Figure 17 shows the profile of the FIR filter in the oversampling front-end design and that of the analog band-pass filter, which was used in the analog synchronous demodulation architecture.

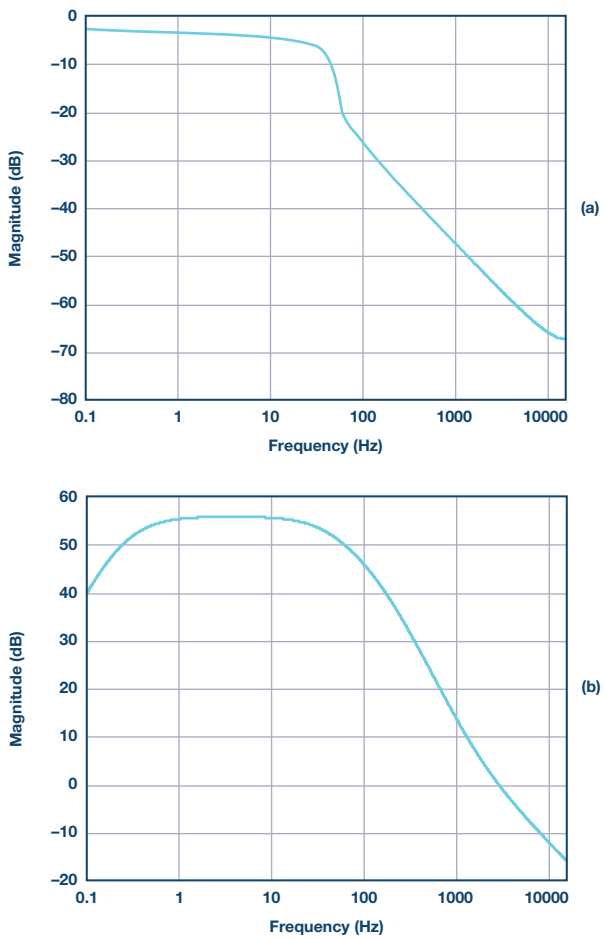


Figure 17. (a) Profile of a digital FIR low-pass filter. (b) Profile of an analog band-pass filter.

The algorithm then subtracts the two averages to get a value that is proportional to the flow rate. The resulting unit for this value is LSB per (meter/sec). This value needs to be further processed. The final flow rate computation is:

$$\text{FlowRate (mps)} = \frac{\Delta FlowRate \times V_{REF}}{(2^N - 1) \times G \times Sensitivity} \times K_T \times K_S - K_Z$$

Where:

$\Delta FlowRate$ is the subtraction result of the two averages from the positive and negative excitation phases, LSB.

V_{REF} is the ADC reference voltage,volts.

N is the number of ADC resolution bits.

G is the gain of the analog front end.

$Sensitivity$ is the nominal sensitivity of the sensor, V per (meter/second).

K_T is the transmitter coefficient.

K_S is the sensor coefficient.

K_Z is the zero offset.

How Do I Choose the Right Processor?

The choice of processor is an important one. Increasingly, there is a need for more processing capability, either to support more complex algorithm computations or for enhanced diagnostics or prognostics. There is also global movement to drive greater energy efficiency across electrical and industrial infrastructure. Customers are demanding more processing capability at lower power and at attainable cost points.

The digital filter for EM flow can demand a large amount of processing power. The 32-bit FIR filter used consumes 80 MIPS. The flow rate computation, the periphery communications driver, and data communication take 40 MIPS, 32 MIPS, and 20 MIPS, respectively. These add up to 172 MIPS in total. In this design the above tasks are done by an ADSP-BF504F digital signal processor of up to 400 MIPS capability. Already, nearly 50% of the processing capability has been used and this is before multilayer communication stacks, HART communications, diagnostics, safety monitoring functions, or LCM drivers have been included.

Table 7. MIPS Consumption

Task	MIPS
FIR Filter	80
Metering Data Processing	40
AD7172-2 Data Access	32
Others	20
Total	172

The on-chip peripherals are also key. The DSP has a variety of functions to implement, including SPI, UART, I²C, and pulsed output communications. There are 35 GPIOs available for the hardware control and logic input/output that are, for example, for controlling the LCD, keypad input, alarms, and diagnostics. The SRAM memory stores the filter coefficient, SPI data communication, LCM data cache, and machine state data, and internal status flags. The 68 kB on-chip static random access memory (SRAM) meets system-level requirements and consists of a 32 kB L1 instruction SRAM/cache and a 32 kB L1 data SRAM/cache. The memory is also needed for RS-485 and HART communication. 4 MB on-chip flash memory of ADSP-BF504F can be used to store the data for the program, the filter coefficients, and calibration parameters.

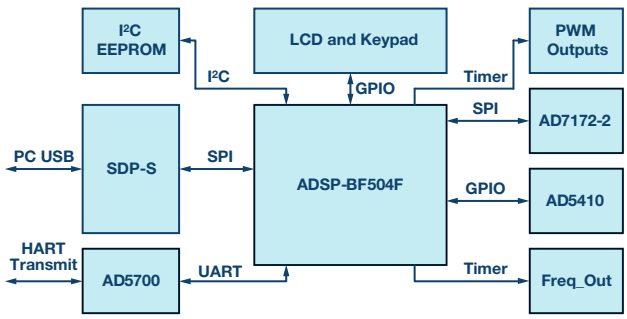


Figure 18. ADSP-BF504F peripheries.

Going forward, there will continue to be a push for more and more processing power. To meet this increased demand, the ADSP-BF70x Blackfin® processor series is a high performance DSP that delivers a class-leading 800 MMACS of processing power at less than 100 mW. The cost-effective eight member series includes up to 1 MB of internal L2 SRAM, eliminating external memory in many applications, while a second configuration features an optional DDR2/LPDDR memory interface. Table 8 shows the key features of the ADSP-BF7xx family.

What Does ADI Offer for Electromagnetic Flow Meter Solutions?

ADI has developed a system-level reference design to prototype the complete signal chain for an electromagnetic flow meter. The system is configured so that it can connect to any EM flow sensor type, apply the appropriate excitation frequency and voltage levels to generate the magnetic field (controlled by a Blackfin DSP), measure the sensor output, and apply postprocessing filters and algorithms to calculate flow rates. ADI calibrated the design in a real flow rig environment, shown in Figure 19, and stored calibration coefficients in memory. Single point or multipoint calibration is possible, allowing for an increased performance through multipoint linearization. In doing this, we were able to demonstrate that the performance of the analog front-end design can meet that of leading high end flow meters.

There are some key advantages of the oversampled architecture compared to the traditional architecture. There are significant area and cost savings—up to 50% and 20%, respectively. There are also power savings and enhanced system performance benefits due to the ability to save the sensor signal and apply postprocessing to it. For more information on ADI reference design, please contact cic@analog.com.

Table 8. ADSP-BF70x Blackfin Processor Family

Generic Device	DSP Core Performance	On-Chip Memory	External Memory	Key Connectivity Options	Other Features	Package
ADSP-BF700 ADSP-BF702 ADSP-BF704 ADSP-BF706	100 MHz to 400 MHz 800 MMACS, 16-bit 400 MMACS, 32-bit	132 kB L1 SRAM/cache L2 SRAM options of 128 kB 256 kB 512 kB 1 MB 512 kB L2ROM	N/A	ePPI, Sport (2), quad/dual SPI (3), I²C, UART (2), CAN 2.0 B (2), SD/SDIO/MMC (4-bit) USB 2.0 HS OTG	OTP, security accelerator, data integrity (with L1 parity and L2 ECC), WDT, RTC	QFN 88-lead, 12 mm × 12 mm
ADSP-BF701 ADSP-BF703 ADSP-BF705 ADSP-BF707			16-bit LPDDR DDR2	Above options plus SDIO/MMC/eMMC (8-bit) 4-channel, 12-bit ADC		BGA 184-ball, 12 mm × 12 mm, 0.8 mm

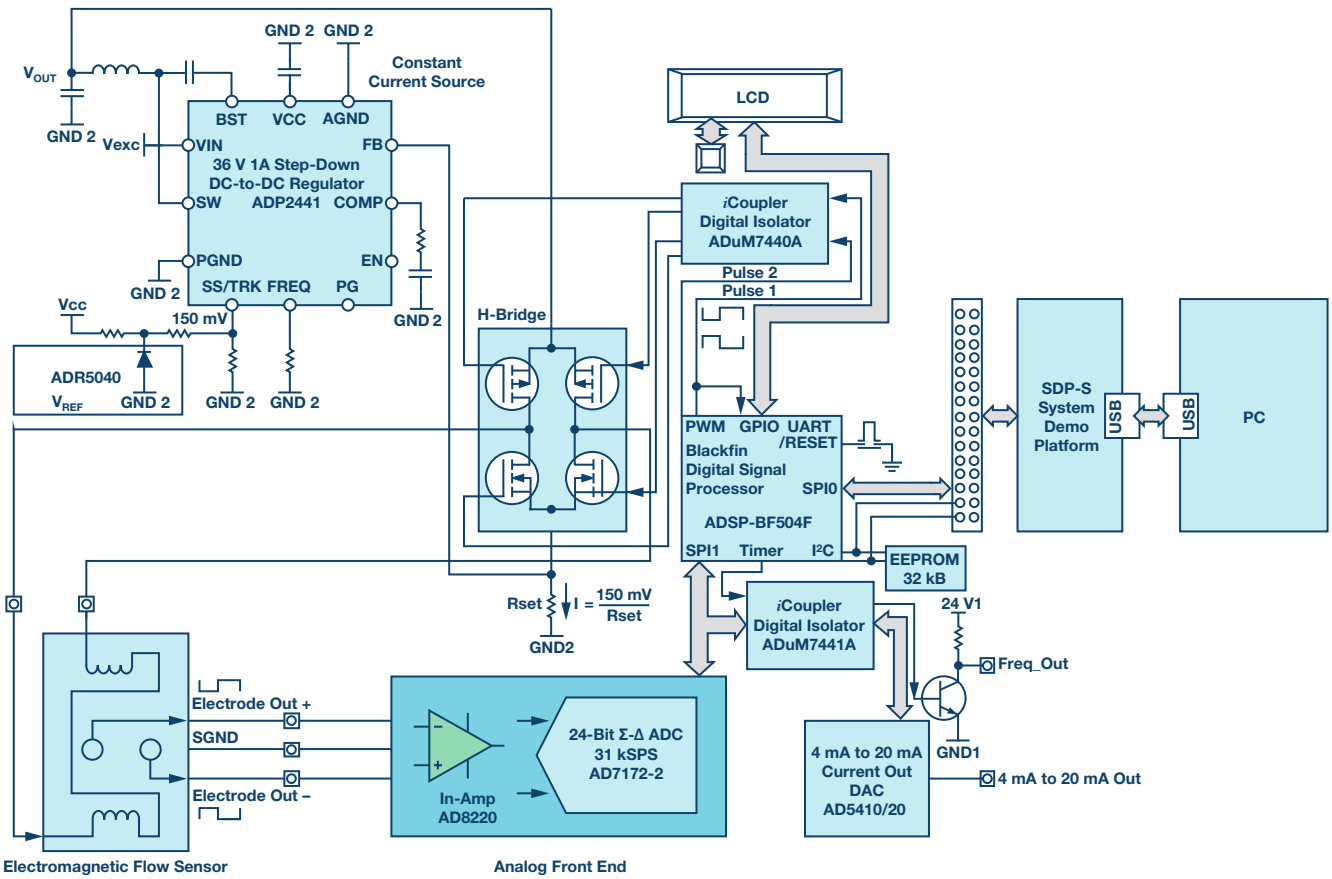


Figure 19. ADI complete solution.

Have You Measured Data from Your Design?

Evaluation Results

The reference design was tested while attached to 25 mm diameter electromagnetic flow sensors on a flow calibration rig with water at room temperature. With the excitation frequency set to 6.25 Hz, the basic error of ±0.2% of reading was achieved in the range of 0.5 meters/sec to 2 meters/sec. The test result data is shown in Table 9.

Table 9. Calibration Results of the Digital Oversampling Demo Board with DN25 Sensor

Flow Rate (mps)	Error of Reading (%)	Repeatability (%)
2.05	–0.14%	0.00%
1.01	0.03%	0.03%
0.49	0.07%	0.04%
0.21	0.42%	0.08%
0.10	1.15%	0.01%
0.05	2.74%	0.06%

Summary and Conclusion

Worldwide, but especially in Europe, more and more environmental regulations are coming on stream to monitor and control waste from both residential and commercial industries. Electromagnetic flow technology is the technology of choice for this application. The traditional architecture tended to be very much an analog approach. This has some disadvantages, such as the cost, area, power, response time, and limited system information. The trend in the industry is toward an oversampled approach. This puts significant challenges on the requirements for the ADC, as the update rates will increase by an order of 10×, but the benefit of averaging cannot be used, which pushes the ADC boundaries in terms of noise requirements at high update rates. There are also power challenges to be solved. The wide range of both liquid types and pipe diameter types create the need for a dynamic power control capability, effectively having a one design that fits all sensor type need with minimum power dissipation. The Blackfin DSP offers the right mix of low power and processing requirements for the flow meter application. It performs complex FIR filter algorithms to calculate flow rates while delivering a class-leading 800 MMACS of processing power at less than 100 mW. The complete design offers a much simplified approach to previous techniques with many advantages of cost, power, and area savings. For more information on ADI's reference design, please contact cic@analog.com.

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Colm Slattery [colm.slattery@analog.com] is a systems applications engineer in the Automation, Energy and Sensors business unit at Analog Devices, based in Limerick, Ireland. His focus area is process control, including field instruments and PLC/DCS controllers for process automation market. Colm graduated from University of Limerick with a bachelor of electronics. Prior to working at ADI, he worked for Microsemi.

Colm Slattery

Also by this Author:

Electromagnetic Flow Meters Achieve High Accuracy in Industrial Applications

Analog Dialogue 48-02, February (2014)

Ke Li [ke.li@analog.com] is an Analog Devices system applications engineer in the Automation, Energy, and Sensor business unit based in Limerick, Ireland. Ke joined Analog Devices in 2007 as a product applications engineer with the Precision Converters Group, located in Shanghai, China. Before this he spent four years as an R&D engineer with the Chemical Analysis Group at Agilent Technologies. He received a master's degree in biomedical engineering in 2003 and a bachelor's degree in electric engineering in 1999, both from Xi'an Jiaotong University.

Ke Li

Also by this Author:

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Notes

Analog Devices, Inc.
Worldwide Headquarters
Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA 02062-9106
U.S.A.
Tel: 781.329.4700
(800.262.5643,
U.S.A. only)
Fax: 781.461.3113

Analog Devices, Inc.
Europe Headquarters
Analog Devices, Inc.
Otl-Aicher-Str. 60-64
80807 München
Germany
Tel: 49.89.76903.0
Fax: 49.89.76903.157

Analog Devices, Inc.
Japan Headquarters
Analog Devices, KK
New Pier Takeshiba
South Tower Building
1-16-1 Kaigan, Minato-ku,
Tokyo, 105-6891
Japan
Tel: 813.5402.8200
Fax: 813.5402.1064

Analog Devices, Inc.
Asia Pacific Headquarters
Analog Devices
5F, Sandhill Plaza
2290 Zuchongzhi Road
Zhangjiang Hi-Tech Park
Pudong New District
Shanghai, China 201203
Tel: 86.21.2320.8000
Fax: 86.21.2320.8222

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