Analog Circuit Design

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(editors)

This volume of *Analog Circuit Design* concentrates on 3 topics: Operational Amplifiers, A-to-D converters and Analog CAD. The book comprises 6 papers on each topic written by internationally recognised experts. These papers have a tutorial nature aimed at improving the design of analog circuits. The book is divided into 3 parts:

Part I, Operational Amplifiers, presents new techniques for the design of Op-Amps in both bipolar and CMOS technologies. Two papers demonstrate techniques for improving frequency and gain behavior at high voltage. Low voltage bipolar Op-Amp design is treated in another paper. The realization of high-speed and high gain VLSI building blocks in CMOS is demonstrated in two papers. The final paper shows how to provide output power with CMOS buffer amplifiers.

Part II, Analog-to-Digital Conversion, presents papers which address very high conversion speeds and very high resolution implementations using sigma-delta modulation architectures. Analog-to-Digital converters provide the link between the analog world of transducers and the digital world of signal processing and computing. High-performance bipolar and MOS technologies result in high-resolution or high-speed convertors which can be applied in digital audio or video systems. Furthermore, the advanced high-speed bipolar technologies show an increase in conversion speed into the Giga Hertz range.

Part III, Analog Computer Aided Design, presents the latest research towards providing Analog circuit designers with the tools needed to automate much of the design process. The techniques and methodologies described demonstrate the advances being made in developing analog design tools comparable with those already available for digital design.

The papers in this volume are based on those presented at the Workshop on Advances in Analog Circuit Design held in Delft, The Netherlands in 1992. The main intention of the workshop was to brainstorm with a group of about 100 analog design experts on the new possibilities and future developments on the above topics. The result of this brainstorming is contained in *Analog Circuit Design*, which is thus an important reference for researchers and design engineers working in the forefront of analog circuit design and research.

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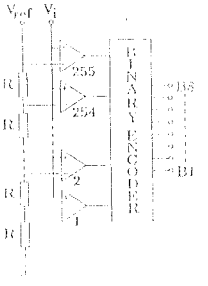

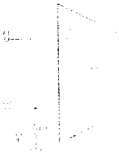

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Bandpass Sigma Delta A-D Conversion

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Abstract

Modern high performance radio systems increasingly rely on digital signal processing techniques. In many cases performance is limited by the A-D conversion process, particularly where high linearity is required. In this paper three examples are presented of bandpass sigma-delta A-D converters which offer a cost effective means of encoding narrowband IF signals to a high linearity and with low spurious content.

1. Introduction

The technique of base-band sigma-delta Analogue to Digital (A-D) conversion is well established and is frequently used in speech and communications applications [1,2]. More recently, single-bit conversion schemes have found a wider application in digital audio systems for both A-D converters and Digital to Analogue (D-A) converters where enhanced linearity especially at low signal levels is a principal advantage [3,4].

For RF applications the base-band conversion scheme requires demodulation of the message using two matched mixers fed by inphase and quadrature carriers as shown in Fig.1. The output of each mixer is then low pass filtered and subsequently encoded with separate A-D converters. While this approach may be satisfactory for low resolution systems it has inherent performance limitations due to *I-Q* imbalance, and lack of sensitivity at the carrier due to masking by DC offsets.

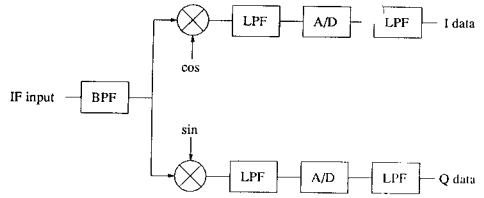

Figure 1: Conventional digital IF system architecture with analogue mix to baseband and separate A/D converters in the I and Q paths.

To ensure 40 *dB I-Q* image rejection, for example, an amplitude and phase match of better than 0.1 *dB* and 1 degree respectively is necessary. This would mean that a signal received at say 10 *kHz* above the IF centre frequency would produce an image component only 40 *dB* lower at a frequency 10 *kHz* below the IF centre frequency. For many applications this would present a serious limitation on resolution in the frequency domain, on single sideband reception for example. Similarly the presence of DC offsets and low frequency $1/f$ noise at the mixer outputs and A-D converter inputs will produce components which cannot be distinguished from signals at the IF centre frequency. This will place a restriction on reception and demodulation of signals requiring the extraction of a carrier component. The DC component may be removed by high pass filtering the digital *I,Q* signals, but this will produce a null in the response around the IF centre frequency.

A new design of sigma-delta A-D converter is presented which can encode the signal at the intermediate frequency and then by digital post processing convert to baseband *I* and *Q* as shown in Fig.2. This enables the quadrature mixing to be achieved with a high degree of accuracy. Orthogonality is guaranteed by sampling at four times the IF centre frequency (f_{IF}). The two local oscillator signals are then of the form 1, 0, -1, 0 and 0, 1, 0, -1 representing samples of cos $2\pi f_{IF}$ and sin $2\pi f_{IF}$. The resultant *I,Q* image rejection and DC offset is then set by the number of bits in the digital processing, which can be made arbitrarily larger than that of the A-D converter.

In this section the basic properties of baseband sigma-delta modulators will be explained and several simple equations will be derived to characterize key features of an example baseband coder. Later, when the conversion from baseband to bandpass is applied, these equations will be modified accordingly such that the effect of the transformation may be seen.

Fig.3 shows an example of a baseband sigma-delta modulator. A delayed version of the output signal $Y(Z)$ is subtracted from the input signal $X(Z)$ to produce the error signal $E(Z)$. The error signal is filtered by the loop filter $A(Z)$ to give a filtered error signal $F(Z)$, where $F(Z)$ is the weighted sum of the first and second integrals of $E(Z)$. The filtered error signal is quantized, often quite coarsely, to produce the output signal. The stability of the closed loop depends on the design of the loop filter and it is here that the subtleties of different designs exist. This is particularly true in the case of single bit modulators in which the open loop gain is not defined and consequently stability is much harder to predict.

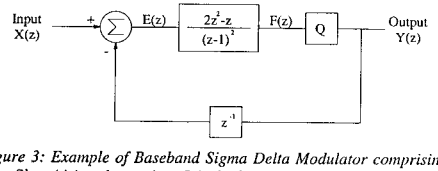

Figure 3: Example of Baseband Sigma Delta Modulator comprising loop filter A(z) and quantizer Q in feed forward path and single delay element in feed back path.

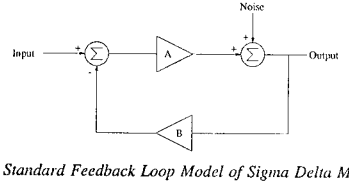

Figure 4: Standard Feedback Loop Model of Sigma Delta Modulator.

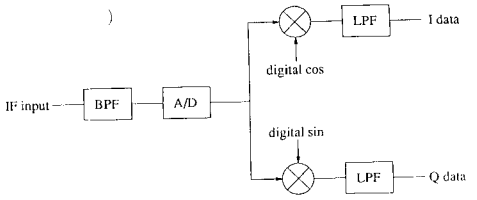

Figure 2: Alternative digital IF system architecture with single A/D converter encoding the IF signal and subsequent digital mix to baseband.

The technique of band-pass sigma-delta conversion is described and a method for designing band-pass A-D converters from existing baseband modulator designs is given. Practical results are described with the performance specified in conventional RF circuit terms.

The novel techniques described here are the subject of worldwide granted and pending patents.

2. Baseband Sigma-Delta Modulation

It is desirable in the transformation of a baseband sigma-delta modulator to its bandpass equivalent that certain of the basic properties of the coder remain unchanged. With the existence of a direct mapping technique from baseband to bandpass this condition is easily met and consequently much of the wealth of information regarding baseband coders which has been acquired over the last few decades may be applied almost directly to the bandpass equivalents. As a result parameters such as overload levels, noise power densities, signal shaping properties and statistical information about the signal levels within the coders already exist and the process of designing bandpass coders is greatly simplified.

The basic properties of the coder can be seen by considering the standard feedback loop model shown in Fig.4. In the figure, 'A' represents the filters in the feed forward path which would correspond to the loop filter and the gain of the quantizer, and 'B' represents the filters in the feedback path, which in the example modulator is just a simple delay. The additive noise source is a crude model of the noise added by the quantizer which is assumed to be white, though in practice this assumption is not accurate. The two properties of interest are the ways in which the modulator filters the signal and shapes the noise.

Using the feedback loop model it is simple to establish the transfer functions between each of the signal and noise inputs and the output. These transfer functions may be called the Signal Transfer Function (STF) and the Noise Transfer Function (NTF) respectively and are given by:

$$STF = \frac{A}{1 + AB} \tag{1}$$

$$NTF = \frac{1}{1 + AB} \tag{2}$$

It is desirable that the signal be encoded without phase or amplitude variation across the passband, and that the noise be heavily attenuated. At first glance both of these seem possible over a wide frequency range by making 'A' very large, but this cannot be achieved in practice because the loop would be unstable. However, 'A' can be made large over a narrow band of frequencies by making its gain frequency dependent. In baseband coders the loop filters have high gain at low frequencies and reduced gain at high frequencies to maintain stability. As a result, at low frequencies, the STF is virtually flat and the NTF heavily attenuates the quantizing noise.

Returning to the example modulator given in Fig.3, the STF and NTF may now be derived. Both derivations assume that the quantizer has unity gain, which for the single bit quantizer is not accurate. However, since the properties of the quantizer are unaffected by the baseband to bandpass transformation this will not affect the final results. With the unity gain assumption, the transfer functions are given below:

$$STF(Z) = \frac{2(Z-0.5)}{Z} \tag{3}$$

$$NTF(Z) = \frac{(Z-1)^2}{Z^2} \qquad (4)$$

At low frequencies the zero in the STF introduces very little phase and amplitude ripple to the signal, whilst the double zero in the NTF heavily attenuates low frequency noise at the output of the coder. Fig.5 shows the output spectrum of the example modulator with a sinusoidal input at $f_s/100$, where f_s is the sampling rate. The noise shaping properties of the coder are clearly seen.

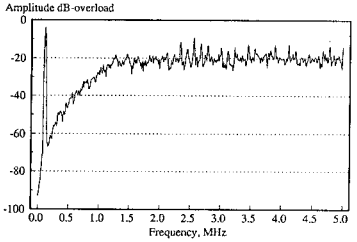

Figure 5: Output Spectrum of Baseband Sigma Delta Modulator.

Fundamental to the noise shaping properties of the coder is the open loop transfer function between the input and the output of the quantizer. This fact is readily confirmed in (2), the generalized formula for the NTF. When considering purely digital modulators it is best described as a simple Open Loop Transfer Function (OLTF), but when mixed digital and analogue architectures are considered, as in the case of sigma-delta A-D converters, this is more usefully described in terms of the Open Loop Impulse Response (OLIR). For practical reasons delay is implemented in the digital feedback path since it is cumbersome to achieve in an analogue filter, and consequently the digital loop filter in the feedforward path will have numerator and denominator of equal order. The OLIR then neglects the digital delay terms and describes only the true filtering properties of the loop filter.

Consider the conventional design of IF encoder sh[illegible] in Fig.1. Two separate A-D converters are used, one each to encode the I and Q components of the IF signal. The aim is to design one A-D converter to encode the IF signal directly.

A first step towards this can be made by repositioning the mix to baseband from the pre-conversion analogue domain to the post-conversion digital domain. As a result the I and Q signals to be encoded will no longer be at baseband but will be modulated by cosinusoidal and sinusoidal carriers respectively, each at half the sampling frequency. The effect of this is that the original baseband signals will now alternate in polarity from sample to sample, and the modified A-D converters must be able to accommodate this. The modification is easily made to the example baseband modulator of Fig.3. To achieve a polarity inversion with every clock cycle, an invertor is placed immediately following every delay element, or quite simply $-Z$ is substituted for Z in the original architecture.

It is then noted that the I-Q separation in the system architecture is achieved by sampling each A-D converter alternately, with a 180° phase difference between them. The two A-D converters are otherwise identical. It is therefore possible to arrange for one converter to encode both I and Q signals in a time multiplexed fashion by simply doubling the sample rate and replacing each delay element with a two stage shift register to keep I and Q data separate. Thus, for example, on even numbered sampling instants the in-phase component of the IF signal is presented to the modulator, and the corresponding in-phase data is encoded by the arithmetic operators of the modulator. Quadrature data is stored halfway down the shift registers within the modulator and is not affected. On odd numbered sampling instants the quadrature data is encoded whilst the in-phase data is stored in the shift registers. The conversion is made by substituting Z^2 for Z in the recently modified coder. Combining the two substitutions, i.e. $-Z^2$ for Z, gives the necessary substitution to convert the baseband coder into its quarter sampling rate bandpass equivalent.

Fig.6 shows the resulting modulator after $-Z^2$ is substituted for Z in the example coder of Fig.3. It is noted that the signals at the input summing node are now added, though negative feedback is still achieved since the two sample period loop delay corresponds to a 180° phase shift at the IF, and hence the signals are added out of phase to achieve cancellation.

The signal and noise transfer functions of the new modulator are given below.

$$STF(Z) = \frac{2(Z^2 + 0.5)}{Z^2} \qquad (9)$$

For the example [illegible]ulator the open loop transfer function is given by:

$$OLTF(Z) = \frac{2Z-1}{(Z-1)^2} \qquad (5)$$

Separating the delay from the filter elements gives:

$$OLTF(Z) = \frac{2Z^2 - Z}{(Z-1)^2} \cdot Z^{-1} \qquad (6)$$

for which the open loop impulse response can be shown to be:

$$OLIR(n) = (2 + n) \qquad n = 0, 1, 2, 3, \ldots. \qquad (7)$$

In virtually all baseband coders the OLIR takes the form of:

$$OLIR(n) = (P + Qn) \qquad (8)$$

where P and Q are the levels of the first and second order components of the impulse response respectively. Such separation of the different order components becomes highly relevant when analogue loop filters are designed, as will be seen in section 5.

This then concludes the overview of the basic features of baseband modulators and the conversion to bandpass will now be considered.

3. Conversion to Bandpass

It is possible to design sigma-delta modulators centred on any frequency from DC to $f_s/2$, and indeed any frequency above this, since the sampled data has many aliased images reflected about multiples of the sampling rate. Coders in which the IF lies between DC and $f_s/2$ are referred to as sampling coders, whilst those operating at an image frequency are referred to as subsampling coders.

This paper is concerned only with coders in which the IF is positioned at an odd multiple of the quarter sampling frequency since they have two distinct advantages over their counterparts. Firstly, the analogue loop filters required in the A-D converters are rather simpler in design, and secondly the digital mix to baseband I and Q signals is trivial to implement since the digital mixing signals are easily generated as cos = {1,0,-1,0} and sin = {0,1,0,-1}.

$$NTF(Z) = \frac{(Z^2 + 1)^2}{Z^4} \qquad (10)$$

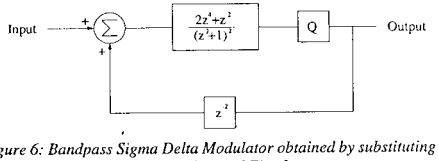

Figure 6: Bandpass Sigma Delta Modulator obtained by substituting $-Z^2$ for Z in the baseband modulator of Fig. 3.

Noise is now heavily attenuated around the quarter and three quarter sampling frequencies allowing IF signals to be encoded, whilst the signal transfer function is identical to that of the baseband coder except shifted to the IF position.

The open loop impulse response is still of importance in designing actual A-D converters, and is now given by:

$$OLIR(n) = \left(2 + \frac{n}{2}\right) \cdot \cos\frac{\pi n}{2} \qquad n = 0,1,2,3, \ldots \qquad (11)$$

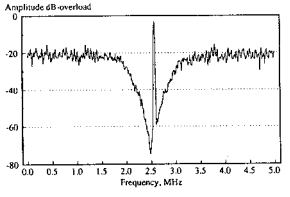

Figure 7: Output Spectrum of Bandpass Sigma Delta Modulator.

Fig.7 shows the output spectrum of the bandpass modulator for an input sinusoid at $f_s/100$ above the quarter sampling frequency. All the properties of the baseband coder are preserved but are translated to the IF position. The necessary loop filters are all that is now required before an actual A-D converter can be designed.

4. Analogue Loop Filter Design

Fig.8 shows a practical structure for a bandpass sigma-delta A-D converter. The digital loop filter of the example modulator is replaced by an analogue bandpass filter, the design of which is to be considered in this section. The single bit quantizer is replaced by a single bit A-D converter, i.e. comparator with a sampled output. The delay in the feedback path is still implemented digitally though the amount of delay introduced here is not the total required since delay already exists in the analogue elements of the circuit and the DACs will have some inherent delay between the arrival of data at their inputs and the temporal centre of the energy of their output pulses. Typically one half to one whole sample period of loop delay will be accumulated in these areas, leaving the remainder for the digital delay line. The single bit DACs must be included in the feedback path as the output of the digital delay line will not be sufficiently linear in most applications. For optimum linearity in the DACs a return to zero output pulse is required to minimize non-linear memory effects and consequently the output pulses from the DACs will be shorter than the sampling interval.

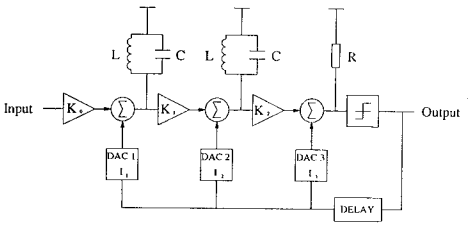

Figure 8: Practical Implementation of Bandpass Sigma Delta A-D Converter.

correction DAC and is required to compensate for effects caused by the finite width of the pulses of the two main DACs. This can be made clearer by considering the mathematics.

Firstly the impulse response of the digital loop filter (11) must be converted to a continuous time waveform by substituting t/T for n, where T is the sampling interval of the coder. The coefficient m comes from the sampling rate to IF ratio and is given by $m = 4 f_{IF}/f_s$.

$$OLIR(t) = \left(2+\frac{t}{2T}\right)\cdot\cos\frac{\pi tm}{2T} \qquad m = 1,3,5,... \qquad (12)$$

This then is the waveform which must be generated. Laplace analysis of the pulse waveform from the DACs and the response of the loop filters allows two expressions to be written which describe the filters pulse response both during and after the application of the pulses. If the pulse width is τ and is centred on $t = 0$ then the two equations for the open loop pulse response are

$$OLPR(t) = \left[\frac{I_1K_1K_2}{2\omega_n C^2}\left\{t+\frac{\tau}{2}\right\}\sin\omega_n\left\{t+\frac{\tau}{2}\right\} + \frac{I_2K_2}{\omega_n C}\sin\omega_n\left\{t+\frac{\tau}{2}\right\} + I_3\right]R \qquad -\frac{\tau}{2} \le t < \frac{\tau}{2} \qquad (13)$$

and

$$OLPR(t) = \left[\frac{I_1K_1K_2}{2\omega_n C^2}\left\{\tau\cos\frac{\omega_n\tau}{2}\sin\omega_n t + 2t\sin\frac{\omega_n\tau}{2}\cos\omega_n t\right\} + \frac{2I_2K_2}{\omega_n C}\left\{\sin\frac{\omega_n\tau}{2}\cos\omega_n t\right\}\right]R \qquad t \ge \frac{\tau}{2} \qquad (14)$$

where K_1 and K_2 are the gains of the buffer amplifiers in amps per Volt, ω_n is the IF frequency in radians per second and C and R are the values of the capacitors and the resistor shown in Fig.8. Values for I_1, I_2, K_1, K_2, C, R, and τ are selected to equate terms in $\cos\omega_n t$ and $t\cdot\cos\omega_n t$ in (14) to those in (12). Finally I_3 the current for DAC3, is selected to equate (13) and (12) at $t = 0$. The error term in $\sin\omega_n t$ found in (14) is cumbersome to remove, but by pulsing the DACs very slightly earlier than originally intended a phase shift can be introduced to compensate for this and no loss of performance is found. A more detailed analysis may be found in [5].

A loop filter has now been designed which closely matches the phase and amplitude response of the example digital filter, and an arrangement of DACs is provided to generate the desired open loop pulse response. This general approach may be used to design several different types of bandpass sigma-delta A-D converters and in the following section examples will be given of sampling, subsampling and interpolative coders.

The key to the design of the converter lies in the design of the loop filter, and for this two options exist; switched capacitor filters and true analogue filters. For lower performance applications switched capacitor implementations will suffice and allow complete integration of the converter, however, since the analogue input is effectively sampled at the input to the converter the normal *I-Q* mismatch and non-linearity problems associated with sample and hold circuits will be replicated in the output of the A-D converter. For more demanding applications true analogue filters offer the best solution since the need for a sample and hold is removed and any errors introduced by the sampling process, which now takes place after the loop filter, are subjected to the same noise shaping processes which govern the quantizing noise. This paper is concerned with the latter option.

For the coder to operate correctly the response of the loop filter to both the analogue input signal and the pulsed waveform from the DACs must match that of the digital loop filter. For the analogue signal the match need only occur in and around the passband since out-of-band components are not of interest and will have been removed before the converter by filtering. This match may be achieved simply by considering the required amplitude and phase response of the filter within the passband. For the digitized signal from the DACs the match must be broadband and is very complicated if considered in the frequency domain because the cyclic repetition of the digital filters frequency response is not matched by that of the analogue filter. For this reason a time domain analysis must be used to match the pulse response of the analogue filter at the sampling instants to the impulse response of the digital filter, usually referred to as 'impulse invariant design'.

Consider again the architecture shown in Fig.8. The twin buffered parallel LC filter has virtually identical phase and amplitude responses as the digital loop filter, both within the passband and considerably beyond. The main difference is that the original digital filter offered infinite gain at the resonant frequency whereas that of the LC filters will be determined by the Q-factors. Equations (1) and (2) show that this will have little effect on the STF but will limit the extent of noise shaping at the frequencies where the mismatch occurs. In practice this implies that in the centre of the passband, approximately 1% to 2% of Nyquist in width, the noise power spectrum flattens out rather than continuing to fall as the centre frequency is approached.

The desired impulse response is achieved with three DACs. The output of DAC1 is filtered by both LC filters and is used to generate the second order component of the impulse response, whilst the output of DAC2 is filtered only once and generates the first order component. DAC3 is a

5. Bandpass Sigma Delta A-D Conversion

The techniques demonstrated in the previous section may be applied generally to the design of several different types of converter and three examples will now be given. The first is a standard sampling converter in which the IF is positioned at one quarter of the sampling frequency and will allow direct use of the equations given earlier. The second example is a subsampling A-D converter in which the IF is positioned at three quarters of the sampling frequency. To implement this it is necessary to adjust the ratio of first and second order components of the open loop impulse response to accommodate the reduction in oversampling ratio. The third example is of an interpolating A-D converter, similar to the subsampling converter but in which a two bit quantizer is used in conjunction with a single bit DAC to extend the dynamic range whilst maintaining the linearity advantages of single bit D-A conversion.

6. Sampling Bandpass Sigma-Delta A-D Converter

The design of this type of A-D converter, the most basic in the bandpass sigma-delta family, has already been extensively described in the preceding sections and will not be covered further. The measured performance of a prototype converter will instead be described in some detail.

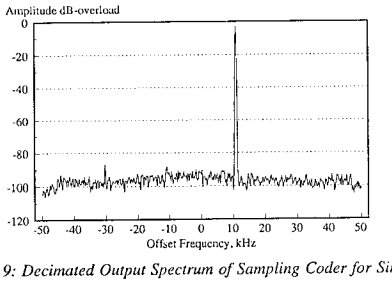

Figure 9: Decimated Output Spectrum of Sampling Coder for Single Tone Input 3 dB below overload.

A-D converters are usually characterized in t s of resolution, differential non-linearity etc., but this convention will not be adopted here since conventional analogue terms such as signal to noise ratio and third order intercept points are more relevant both to the applications of the converters and to the performance of the converters themselves. In all cases the reference power level used for measurements will be the overload point of the converter in question, and figures will be quoted in *dBO*.

Design Parameter	Sampling	Subsampling	Interpolative
IF	2.5 *MHz*	7.5 *MHz*	7.5 *MHz*
O/P word size	1 bit	1 bit	2 bits
O/P sampling rate	10 *MHz*	10 *MHz*	10 *MHz*
DAC size	1 bit	1 bit	1 bit
DAC rate	10 *MHz*	10 *MHz*	30 *MHz*
Bandwidth	100 *kHz*	100 *kHz*	100 *kHz*
Q-factor	100	300	300

Table 1: Design Parameters of the Sampling, Subsampling and Interpolative Bandpass Sigma-Delta A-D Converters.

The prototype converter to be described was designed to the parameters given in the first column of Table 1. Fig.9 shows the decimated output spectrum of the converter for a single tone input 3 *dB* below overload and positioned 10 *kHz* above the centre of the passband. The smaller signal to the left of the main tone is the third order distortion component of the converter which is aliased back into the passband. The first column of Table 2 describes the measured performance of the coder, giving the in-band noise power spectral density, the third order intercept point for a twin tone input and the spurious free dynamic range of the converter in a 1 *Hz* noise bandwidth for a single tone input.

The complete set of design parameters and measur. results for this converter are given in the second columns of Tables 1 and 2 respectively. Fig.10 shows the output spectrum of the prototype converter with a twin tone input 3 *dB* below the twin tone overload level. In theory the performance of the sampling and subsampling converters should be identical, and a very close match is seen in the measured results. The main cause for the fall in performance is that the required Q-factor of 300 was difficult to achieve in practice and consequently a lower value had to be accepted. This resulted in in-band noise and distortion components rising slightly and degrading the performance, however, the resulting linearity and spurious free dynamic range was still far better than that obtainable from equivalent flash converters.

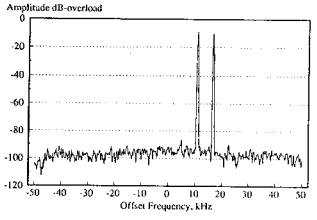

Figure 10: Decimated Output Spectrum of Subsampling Coder for Twin Tone Input 3 dB below overload

8. Interpolating Bandpass Sigma-Delta A-D Converter

The aim of the interpolating converter is to increase the dynamic range of subsampled converters by operating their DACs at four times the IF and to compliment this with extra levels in the quantizer rather than increasing the sampling rate. An interpolating look up table may be used to interface the low-speed multi-level data generated by the quantizer to the higher-speed single-bit DAC in a pulse density format.

In this example the data is interpolated by a factor of 3 to convert it from a two-bit to a one-bit data stream. With careful consideration of the phasing requirements the necessary interpolating function is found to be as

Performance	Sampling	Subsampling	Interpolative
Noise Power Density/Hz	-117 *dBO*	-114 *dBO*	-130 *dBO*
Third Order Intercept	26 *dBO*	24 *dBO*	32 *dBO*
Spurious Free Dynamic Range in 1 *Hz* Single tone input	95 *dB*	92 *dB*	108 *dB*

Table 2: Performance of the Sampling, Subsampling and Interpolative Bandpass Sigma-Delta A-D Converters.

This performance may be compared to that of conventional 'flash' A-D converters in which conversion is achieved with a large number of comparators with uniformly spaced switching thresholds. Within the passband the noise floor is equivalent to that of an 8 bit flash A-D converter sampling at 10 *MHz*; at the decimated output it is equivalent to an 11 bit flash A-D sampling at 200 *kHz*. However the linearity and spurious free dynamic range of the sigma-delta A-D converter are very much better than equivalent flash A-D converters. With flash converters distortion products tend not to fall with decreasing signal level and typical spurious free dynamic ranges are around 55 *dB*.

7. Subsampling Bandpass Sigma Delta A-D Converter

This is an example of a converter in which the IF is positioned in the second quantizing null, i.e. at three quarters of the sampling frequency. The design procedure is very similar to that of a sampling converter except for two main differences. Firstly, in order to encode a narrow passband at three quarters of the sampling frequency analogue loop filters with enhanced Q-factors will be required compared to those of a sampling A-D converter since the IF is three times higher in this example. Consequently the Q-factors will need to be exactly three times as large in order to achieve the same in-band performance. Secondly the impulse invariant design of the loop filter must now accommodate the higher IF of the loop filters and accordingly '*m*' is set to 3 in equation (12).

shown in Fig.11. .e combined response for all three pulses must then be used in the impulse invariant design of the loop filter. This will now be considered in more detail.

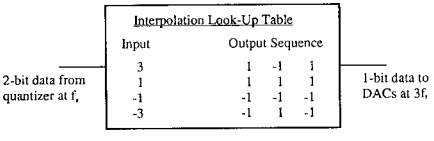

Figure 11: Definition of Interpolating Look-up Table to convert 4 level data to a 2 level bit stream.

Generalizing the design of the loop filter somewhat, its pulse response to the three pulses from the DAC must take the form of:

$$K\left(P+\frac{Qn}{2}\right)\cdot\cos\frac{3\pi n}{2} \tag{15}$$

where K is a scaling factor equal to the output levels of the quantizer and must therefore take on one of the values ±1 or ±3. If the response of the filter to a single pulse from the DAC is given by:

$$\left(R+\frac{Sn}{2}\right)\cdot\cos\frac{3\pi n}{2} \tag{16}$$

then the composite response to the code representing +3 is given by:

$$\left(R+\frac{Sn}{2}\right)\cdot\cos\frac{3\pi n}{2}-\left(R+\frac{S}{2}\left(n+\frac{2}{3}\right)\right)\cdot\cos\frac{3\pi}{2}\left(n+\frac{2}{3}\right)+\left(R+\frac{S}{2}\left(n+\frac{4}{3}\right)\right)\cdot\cos\frac{3\pi}{2}\left(n+\frac{4}{3}\right) \tag{17}$$

$$=3\left(\left(R+\frac{1}{3}S\right)+\frac{Sn}{2}\right)\cdot\cos\frac{3\pi n}{2} \tag{18}$$

whilst the composite response to the code representing +1 is given by:

$$\left(R+\frac{Sn}{2}\right)\cdot\cos\frac{3\pi n}{2}+\left(R+\frac{S}{2}\left(n+\frac{2}{3}\right)\right)\cdot\cos\frac{3\pi}{2}\left(n+\frac{2}{3}\right)+\left(R+\frac{S}{2}\left(n+\frac{4}{3}\right)\right)\cdot\cos\frac{3\pi}{2}\left(n+\frac{4}{3}\right) \quad (19)$$

$$=\left(\left(R+\frac{1}{3}S\right)+\frac{Sn}{2}\right)\cdot\cos\frac{3\pi n}{2} \quad (20)$$

These results are clearly of the correct form to achieve the desired response given in (15). Two aspects must be considered here. Firstly, in the interpolation lookup table I and Q separation must still be maintained and so the pulses relating to the inphase component of the signal must be time multiplexed with those relating to the quadrature component. Secondly a more detailed analysis of the circuit shows that the desired response of DAC3, the correction DAC, is now non-linear across the four coding levels, but this is simple to implement in practice.

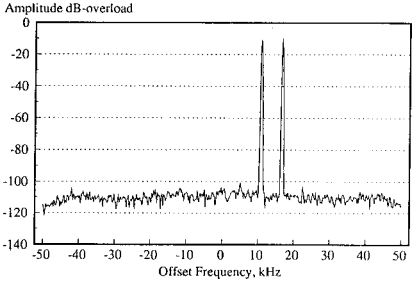

Figure 12: Decimated Output Spectrum of Simulated Interpolative coder for Twin Tone input 3 dB below overload.

The design specifications and the measured performance of the interpolative converter are given in the third columns of Tables 1 and 2 respectively whilst Fig.12 shows the output spectrum of the simulated converter for a twin tone input 3 *dB* below overload. Comparing the results with those of the subsampling coder the improved performance is soon observed. The overload point of the interpolative converter is 10 *dB* higher than that of its counterpart and this increase accounts for most of the improvement in the in-band noise power density, which is referred to the overload point of the converter. The linearity of the converter has also improved and consequently the third order intercept point has risen. Another improvement which is not shown in Table 2 is that as the overload condition is approached the in-band noise power density of the interpolative converter rises much less than in the subsampling and sampling coders. Comparing these results with those of flash converters the in-band noise performance is equivalent to 10 bits at 10 *MHz*, or at the decimated output equivalent to a 13 bit converter sampling at 200 *kHz*. Once again the linearity and spurious free dynamic range far exceed those of flash converters.

9. Implementation

All the designs presented can be implemented using discrete components. This allows easy experimentation with new ideas, though obviously an integrated version is more suitable for a final production model. Unlike switched capacitor implementations which allow the possibility of complete integration, the analogue filters discussed in this paper are not suitable for integration but do offer superior performance.

As with all analogue to digital conversion schemes using feedback, the performance of the converter is limited to the performance of the component producing the cancellation signal. The use of a single bit DAC eases the design, reducing it to a switch, thus optimising linearity. The noise floor of the DAC and hence the dynamic range of the converter is also limited by the quality of the clock signal driving it. The DAC output must possess minimum jitter at transition, needing close attention to clock phase noise and pattern-dependent charge-storage behaviour in the DAC itself.

One other factor that affects the noise floor of the converter is the Q factor of the loop filters. By separating the poles of the loop filters wider bandwidths may be encoded to a restricted dynamic range, and in this case low Q-factors will suffice for the loop filters. However, to encode high dynamic range, narrow bandwidth signals, the poles of the loop filters would typically be coincident and their Q-factors would be maximized to obtain the full dynamic range. Practically, Q-factors in excess of a few hundred are difficult to achieve and this then presents a limitation on the maximum attainable dynamic range.

For correct operation of the converter, the total open loop propagation delay, including any clock delay, must be approximately two sample periods. The effect this has on the implementation depends on the required sample clock frequency. This delay can be achieved by a combination of analogue and digital delay.

Once the input signal has been converted it is usually necessary to decimate the output data. This is not only to produce a multi-bit output, but also to reduce the data rate to one commensurate with the converters bandwidth. This allows further processing to be undertaken using general purpose devices.

Due to the speed and complexity of the decimation process an Application Specific Integrated Circuit (ASIC) is usually required. Cost and power consumption make CMOS ASICs attractive although they may not be fast enough for high sample frequencies. Operating at higher frequencies allows wider bandwidths to be encoded, but the signal processing requirements for decimation are more severe. For wide bandwidths the output from the decimator will be at a correspondingly high rate and if any further processing is required, this rate may be too high for a general purpose digital signal processor to handle. The solution would then be either complex discrete circuits or more ASICs adding considerable cost.

10. Conclusions

The sigma-delta A-D conversion technique has traditionally been applied at baseband where, by exploiting the linearity advantages of oversampled single bit D-A converters, high linearity decimated code may be produced. The technique may easily be adapted to operate at an intermediate frequency allowing high linearity conversion of IF signals without the need for pre-conversion mix to baseband *I* and *Q* components. With post-conversion mix to baseband and decimation the normal system limitations of *I-Q* mismatch and masking by DC offsets are virtually eliminated.

Three examples of bandpass sigma-delta A-D converter have been presented. The first is a sampling converter in which the IF was positioned at one quarter of the sampling frequency whilst the second is the subsampling equivalent with the IF positioned at three quarters of the sampling frequency. In both cases the decimated output is roughly equivalent to 11 bit PCM coding at 200 *kHz* but with substantially

improved linearity and spurious free dynamic range compared to multi-comparator flash conversion. The third example is an interpolative converter in which extended dynamic range is achieved with two bit quantization whilst a one bit DAC operating on an interpolated pulse density code is used to achieve maximum linearity. In this case the decimated output is roughly equivalent to 13 bit pcm at 200 *kHz* but again with significantly improved linearity and with lower spurious content than can be achieved with flash converters.

The converters may be employed for any application where high linearity conversion of narrowband IF signals is required and are particularly suited to high performance radio systems.

The novel techniques described in this paper are the subject of worldwide granted and pending patents.

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Biographies

Andrew M. Thurston received the B.A. Degree in Engineering from Trinity College, Cambridge University, in 1987, and the M.Sc. Degree in telecommunications and information systems from the University of Essex in 1989. He is currently working towards the Doctor of Philosophy Degree on the subject of bandpass sigma-delta A-D conversion at the University of Essex.

In 1987 he joined GEC-Marconi Research Centre as a research engineer in the Signal Processing Division, and is currently leader of the A-D Conversion Section. His areas of interest include oversampled conversion techniques and the design and implementation of analogue filters.

Timothy H. Pearce received the Masters Degree in semiconductor electronics from the University of Southampton in 1968. Since then he has been with GEC-Marconi Research Centre, and gained a wide range of experience in signal processing techniques, with a special interest in high performance analogue to digital conversion methods. He is currently manager of the Signal Processing Division within the Communications Research Laboratory. He is a member of the Institution of Electrical Engineers and a Chartered Engineer.

Malcolm D. Higman received the B.Eng. in Electronic Engineering from Reading University, England, in 1990. In December 1990 he joined the Signal Processing Division at the GEC-Marconi Research Centre where he is currently working on the development of high performance sigma-delta analogue to digital converters.

Malcolm Omar Hawksford is a Reader in the Department of Electronic Systems Engineering at the University of Essex, where his principal interests are in the fields of electronic circuit design and audio engineering. Dr. Hawksford studied at the University of Aston in Birmingham and gained both a First Class Honours B.Sc. and Ph.D. The Ph.D. programme was supported by a BBC Research Scholarship, where the field of study was the application of delta-modulation to colour television and the development of a time compression/time multiplexed system for combining luminance and chrominance signals.

Since his employment at Essex, he has established the Audio Research Group, where research on amplifier studies, digital signal processing and loudspeaker systems has been undertaken. Since 1982 research into digital crossover systems has begun within the group and more recently,

oversampling and noise shaping investigated as a means of analogue-to-digital/digital-to-analog conversion.

Dr. Hawksford has several AES publications that include topics on error correction in amplifiers and oversampling techniques. His supplementary activities include writing articles for *Hi-Fi News and Record Review* and designing commercial audio equipment. He is a member of the IEE, a chartered engineer, a fellow of the AES and of the Institute of Acoustics and a member of the review board of the *AES Journal*. He is also technical adviser for *HFN* and *RR*.