ANALOG DEVICES

MT-096
TUTORIAL

RFI Rectification Concepts

INPUT-STAGE RFI RECTIFICATION SENSITIVITY

A well-known but poorly understood phenomenon in analog integrated circuits is *RFI rectification*, specifically as it occurs in op amps and in-amps. While amplifying very small signals these devices can rectify large-amplitude, out-of-band HF signals, i.e., RFI. As a result, dc errors appear at the output in addition to the desired signal. The undesired HF signals can enter sensitive analog circuits by various means. Conductors leading into and out of the circuit provide a path for interference coupling into a circuit. These conductors pick up noise through capacitive, inductive, or radiation coupling. The spurious signals appear at the amplifier inputs, along with the desired signal. The spurious signals can be several tens of mV in amplitude however, which causes problems. Simply stated, it cannot be assumed that a sensitive, low-bandwidth dc amplifier will always reject out-of-band spurious signals. While this would be the case for a simple linear low pass filter, op amp and in-amp devices actually rectify high-level HF signals, leading to non-linearities and anomalous offsets. Methods of analysis for as well as the prevention of RFI rectification are discussed in this tutorial.

BACKGROUND: OP AMP AND IN-AMP RFI RECTIFICATION SENSITIVITY TESTS

Just about all in-amp and op amp input stages use emitter-coupled BJT or source-coupled FET differential pairs of some type. Depending on the device operating current, the interfering frequency and its relative amplitude, these differential pairs can behave as high-frequency detectors. As will be shown, the detection process produces spectral components at the harmonics of the interference, as well at dc! It is the detected dc component of the interference that shifts amplifier bias levels, leading to inaccuracies.

The effect of RFI rectification within op amps and in-amps can be evaluated with relatively simple test circuits, as described for the *RFI Rectification Test Configuration* (see page 1-38 of Reference 1). In these tests, an op amp or in-amp is configured for a gain of –100 (op amp), or 100 (in-amp), with dc output measured after a 100-Hz low-pass filter, preventing interference from other signals. A 100-MHz, 20-mV$_{p-p}$ signal is the test stimulus, chosen to be well above test device frequency limits. In operation, the test evaluates dc output shift observed under stimulus presence. While an ideal dc shift for this measurement would be zero, the actual dc shift of a given part indicates the relative RFI rectification sensitivity. Devices using both BJT and FET technologies can be tested by this method, as can devices operating at either low or high supply current levels.

In the original op amp tests of Reference 1, some FET-input devices (OP80, OP42, OP249 and AD845) exhibited no observable shift in their output voltages, while several others showed shifts of less than 10 µV referred to the input. Of the BJT-input op amps, the amount of shift decreased with increasing device supply current. Only two devices showed no observable output voltage shift (AD797 and AD827), while others showed shifts of less than 10 µV referred to the input

(OP200 and OP297). For other op amps, it is to be expected that similar patterns would be shown under such testing.

From these tests, some generalizations on RFI rectification can be made. First, device susceptibility appears to be inversely proportional to supply current; that is, devices biased at low quiescent supply currents exhibit greatest output voltage shift. Second, ICs with FET-input stages appeared to be less susceptible to rectification than those with BJTs. Note that these points are independent of whether the device is an op amp or an in-amp. In practice this means that the lower power op amps *or* in-amps will tend to be more susceptible to RFI rectification effects. And, FET-input op amps (or in-amps) will tend to be *less* susceptible to RFI, especially those operating at higher currents.

Based on these data and from the fundamental differences between BJTs and FETs, we can summarize what we know. Bipolar transistor action is controlled by a forward-biased p-n junction (the base-emitter junction) whose I-V characteristic is exponential and quite nonlinear. FET behavior, on the other hand, is controlled by voltages applied to a reverse-biased p-n junction diode (the gate-source junction). The I-V characteristic of FETs is a square-law, and thus it is inherently more linear than that of BJTs.

For the case of the lower supply current devices, transistors in the circuit are biased well below their peak f_T collector currents. Although the ICs may be constructed on processes whose device f_Ts can reach hundreds of MHz, charge transit times increase, when transistors are operated at low current levels. The impedance levels used also make RFI rectification in these devices worse. In low-power op amps, impedances are on the order of hundreds to thousands of kΩs, whereas in moderate supply-current designs impedances might be no more than just a few kΩ. Combined, these factors tend to degrade a low-power device's RFI rectification sensitivity.

Figure 1 summarizes these general observations on RFI rectification sensitivity, and is applicable to both op amps and in-amps.

- **BJT input devices *rectify readily***
    - **Forward-biased B-E junction**
    - **Exponential I-V Transfer Characteristic**
- **FET input devices *less sensitive* to rectifying**
    - **Reversed-biased p-n junction**
    - **Square-law I-V Transfer Characteristic**
- **Low I_{supply} devices versus High I_{supply} devices**
    - **Low I_{supply} $\Rightarrow$ *Higher* rectification sensitivity**
    - **High I_{supply} $\Rightarrow$ *Lower* rectification sensitivity**

Figure 1: Some General Observations on Op Amp and In-Amp Input Stage RFI Rectification Sensitivity

AN ANALYTICAL APPROACH: BJT RFI RECTIFICATION

While lab experiments can demonstrate that BJT-input devices exhibit greater RFI rectification sensitivity than comparable devices with FET inputs, a more analytical approach can also be taken to explain this phenomenon.

RF circuit designers have long known that p-n junction diodes are efficient rectifiers because of their nonlinear I-V characteristics. A spectral analysis of a BJT transistor current output for a HF sinewave input reveals that, as the device is biased closer to its "knee," nonlinearity increases. This, in turn, makes its use as a detector more efficient. This is especially true in low-power op amps, where input transistors are biased at very low collector currents.

A rectification analysis for the collector current of a BJT has been presented in Reference 1, and will not be repeated here except for the important conclusions. These results reveal that the original quadratic second-order term can be simplified into a frequency-dependent term, $\Delta i_C(AC)$, at twice the input frequency and a dc term, $\Delta i_C(DC)$. The latter component can be expressed as noted in Eq. 2, the final form for the rectified dc term:

$$\Delta i_C(DC) = \left(\frac{V_X}{V_T}\right)^2 \bullet \frac{I_C}{4} \qquad \text{Eq. 1}$$

This expression shows that the dc component of the second-order term is directly proportional to the *square* of the HF noise amplitude V_X, and, also, to I_C, the quiescent collector current of the transistor. To illustrate this point on rectification, note that the change in dc collector current of a bipolar transistor operating at an I_C of 1 mA with a spurious 10-mV_{peak} high-frequency signal impinging upon it will be about 38 µA.

Reducing the amount of rectified collector current is a matter of reducing the quiescent current, or the magnitude of the interference. Since the op amp and in-amp input stages seldom provide adjustable quiescent collector currents, reducing the level of interfering noise V_X is by far the best (and almost always the only) solution. For example, reducing the amplitude of the interference by a factor of 2, down to 5 mV_{peak} produces a net 4 to 1 reduction in the rectified collector current. Obviously, this illustrates the importance of keeping spurious HF signals away from RFI sensitive amplifier inputs.

AN ANALYTICAL APPROACH: FET RFI RECTIFICATION

A rectification analysis for the drain current of a JFET has also been presented in Reference 1, and isn’t repeated here. A similar approach was used for the rectification analysis of a FET's drain current as a function of a small voltage V_X, applied to its gate. The results of evaluating the second-order rectified term for the FET's drain current are summarized in Eq. 2. Like the BJT, an FET's second-order term has an ac and a dc component. The simplified expression for the dc term of the rectified drain current is given here, where the rectified dc drain current is directly proportional to the square of the amplitude of V_X, the spurious signal. However, Eq. 2 also reveals a very important difference between the *degree* of the rectification produced by FETs relative to BJTs.

$$\Delta i_D(DC) = \left(\frac{V_X}{V_P}\right)^2 \bullet \frac{I_{DSS}}{2} \qquad \text{Eq. 2}$$

Whereas in a BJT the change in collector current has a direct relationship to its quiescent collector current level, the change in a JFET's drain current is proportional to its drain current at zero gate-source voltage, I_{DSS}, and inversely proportional to the square of its channel pinch-off voltage, V_P—parameters that are geometry and process dependent. Typically, JFETs used in the input stages of in-amps and op amps are biased with their quiescent current of ~$0.5 \cdot I_{DSS}$. Therefore, the change in a JFET's drain current is independent of its quiescent drain current; hence, independent of the operating point.

A quantitative comparison of second-order rectified dc terms between BJTs and FETs is illustrated in Figure 2. In this example, a bipolar transistor with a unit emitter area of 576 μm^2 is compared to a unit-area JFET designed for an I_{DSS} of 20 µA and a pinch-off voltage of 2 V. Each device is biased at 10 µA and operated at T_A = 25°C.

- **BJT:**

  Emitter area = 576μm^2

  I_C = 10µA

  V_T = 25.68mV @ 25°C

  $$\Delta i_C = \left(\frac{V_X}{V_T}\right)^2 \bullet \frac{I_C}{4} = \frac{V_X^2}{264}$$

- **JFET:**

  I_{DSS} = 20µA (Z/L=1)

  V_P = 2V

  I_D = 10µA

  $$\Delta i_D = \left(\frac{V_X}{V_P}\right)^2 \bullet \frac{I_{DSS}}{2} = \frac{V_X^2}{400\text{x}10^3}$$

- **Conclusion: *BJTs ~1500* more *sensitive than JFETs!***

Figure 2: Relative Sensitivity Comparison - BJT Versus JFET

The important result is that, under identical quiescent current levels, the change in collector current in bipolar transistors is about 1500 times greater than the change in a JFET's drain current. This explains why FET-input amplifiers behave with less sensitivity to large amplitude HF stimulus. As a result, they offer more RFI rectification immunity.

What all this boils down to is this: Since a user has virtually no access to the amplifier's internal circuitry, the prevention of IC circuit performance degradation due to RFI is left essentially to those means which are external to the ICs.

As the analysis above shows, regardless of the amplifier type, *RFI rectification is directly proportional to the square of the interfering signal's amplitude*. Therefore, to minimize RFI rectification in precision amplifiers, the level of interference must be reduced or eliminated, *prior to the stage*. The most direct way to reduce or eliminate the unwanted noise is by proper filtering.

REDUCING RFI RECTIFICATION WITHIN OP AMP AND IN-AMP CIRCUITS

EMI and RFI can seriously affect the dc performance of high accuracy analog circuits. Because of their relatively low bandwidth, precision op amps and in-amps simply won't accurately amplify RF signals in the MHz range. However, if these out-of-band signals are allowed to couple into a precision amplifier through either its input, output, or power supply pins, they can be internally rectified by various amplifier junctions, ultimately causing an undesirable dc offset at the output. The previous theoretical discussion of this phenomenon has shown its basic mechanisms. The logical next step is to show how proper filtering can minimize or eliminate these errors.

Proper supply decoupling minimizes RFI on IC power pins. Further discussion is required with respect to the amplifier inputs and outputs, *at the device level*. It is assumed at this point that system level EMI/RFI approaches have already been implemented, such as an RFI-tight enclosure, properly grounded shields, power rail filtering, etc. The steps following can be considered as circuit-level EMI/RFI prevention.

Op Amp Inputs

The best way to prevent input stage rectification is to use a low-pass filter located close to the op amp input as shown in Figure 3.

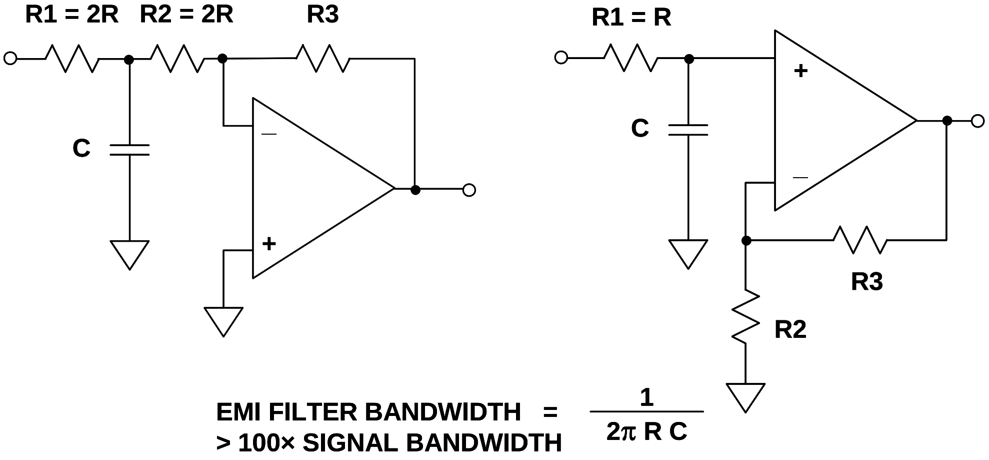


Figure 3: Simple EMI/RFI Noise Filters for Op Amp Circuits

In the case of the inverting op amp at the left, filter capacitor C is placed between equal-value resistors R1-R2. This results in a simple corner frequency expression, as shown in the figure. At very low frequencies or dc, the closed loop gain of the circuit is –R3/(R1+R2). Note that C cannot be connected directly to the inverting input of the op amp, since that would cause instability. The filter bandwidth can be chosen at least 100 times the signal bandwidth to minimize signal loss.

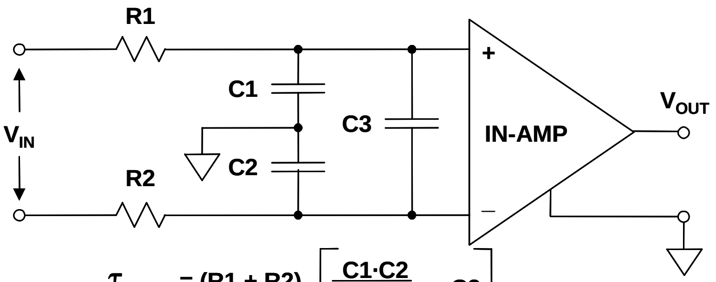
For the non-inverting case on the right, capacitor C can be connected directly to the op amp input as shown, and an input resistor with a value "R" yields the same corner frequency as the inverting case. In both cases low inductance chip-style capacitors should be used, such as NP0 ceramics. The capacitor should in any case be free of losses or voltage coefficient problems, which limits it to either the NP0 mentioned, or a film type.

It should be noted that a ferrite bead can be used instead of R1, however ferrite bead impedance is not well controlled and is generally no greater than 100 Ω at 10 MHz to 100 MHz. This requires a large value capacitor to attenuate lower frequencies.

Instrumentation Amplifier (In-Amp) Inputs

Precision in-amps are particularly sensitive to dc offset errors due to the presence of common-mode (CM) EMI/RFI. This is very much like the problem in op amps. And, as is true with op amps, the sensitivity to EMI/RFI is more acute with the lower power in-amp devices.

A general-purpose approach to proper filtering for device level application of in-amps is shown in Figure 4. In this circuit the in-amp could in practice be any one of a number of devices. The relatively complex balanced RC filter preceding the in-amp performs all of the high frequency filtering. The in-amp would be programmed for the gain required in the application, via its gain-set resistance (not shown).



$$\tau_{DIFF} = (R1 + R2)\left[\frac{C1 \cdot C2}{C1 + C2} + C3\right]$$

$$\tau_{CM} = R1 \bullet C1 = R2 \bullet C2$$

$$\tau_{DIFF} \gg \tau_{CM}$$

R1•C1 = R2•C2
R1 = R2 SHOULD BE 1% RESISTORS
C1 = C2 SHOULD BE ≤ 5% CAPACITORS

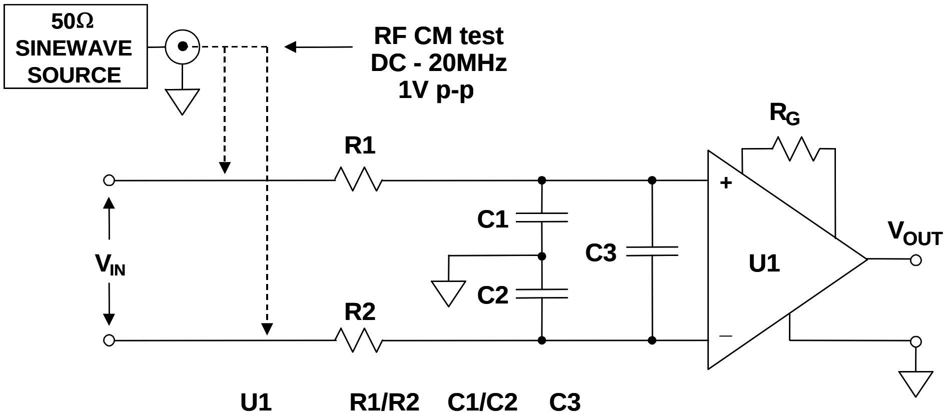
$$\text{DIFFERENTIAL FILTER BANDWIDTH} = \frac{1}{2\pi (R1 + R2)\left[\frac{C1 \cdot C2}{C1 + C2} + C3\right]}$$

Figure 4: A General-Purpose Common-Mode/Differential-Mode RC EMI/RFI Filter for In-Amps

Within the filter, note that fully balanced filtering is provided for both CM (R1-C1 and R2-C2) as well as differential mode (DM) signals (R1+R2, and C3 || the series connection of C1-C2). If R1-R2 and C1-C2 aren't well matched, some of the input common-mode signal at V_{IN} will be converted to a differential mode signal at the in-amp inputs. For this reason, C1 and C2 should be matched to within at least 5% of each other. Also, R1 and R2 should be 1% metal film resistors, so as to aid this matching. It is assumed that the source resistances seen at the V_{IN} terminals are low with respect to R1-R2, and matched. In this type of filter, C3 should be chosen much larger than C1 or C2 (C3 ≥ C1, C2), in order to suppress spurious differential signals due to CM-to-DM conversion resulting from mismatch of the R1-C1 and R2-C2 time constants.

The overall filter bandwidth should be at least 100 times the input signal bandwidth. Physically, the filter components should be symmetrically mounted on a PC board with a large area ground plane and placed close to the in-amp inputs for optimum performance.

Figure 5 shows a family of these filters, as suited to a range of different in-amps. The RC components should be tailored to the different in-amp devices, as per the table. These filter components are selected for a reasonable balance of low EMI/RFI sensitivity and a low increase in noise (vis-à-vis that of the related in-amp, without the filter).



U1	R1/R2 1%	C1/C2 ≤5%	C3 10%
AD620/621/622	4.02k	1nF	47nF
AD623	10k	1nF	22nF
AD627	20k	1nF	22nF

Figure 5: Flexible Common-Mode and Differential-Mode RC EMI/RFI Filters Are Useful With the AD620 Series, the AD623, AD627, and Other In-Amps

To test the EMI/RFI sensitivity of the configuration, a 1-Vp-p CM signal can be applied to the input resistors, as noted. With a typically used in-amp such as the AD620 working at a gain of 1000, the maximum RTI input offset voltage shift observed was 1.5 µV over the 20-MHz range. In the AD620 filter example, the differential bandwidth is about 400 Hz.

Common-mode chokes offer a simple, one-component EMI/RFI protection alternative to the passive RC filters, as shown in Figure 6.

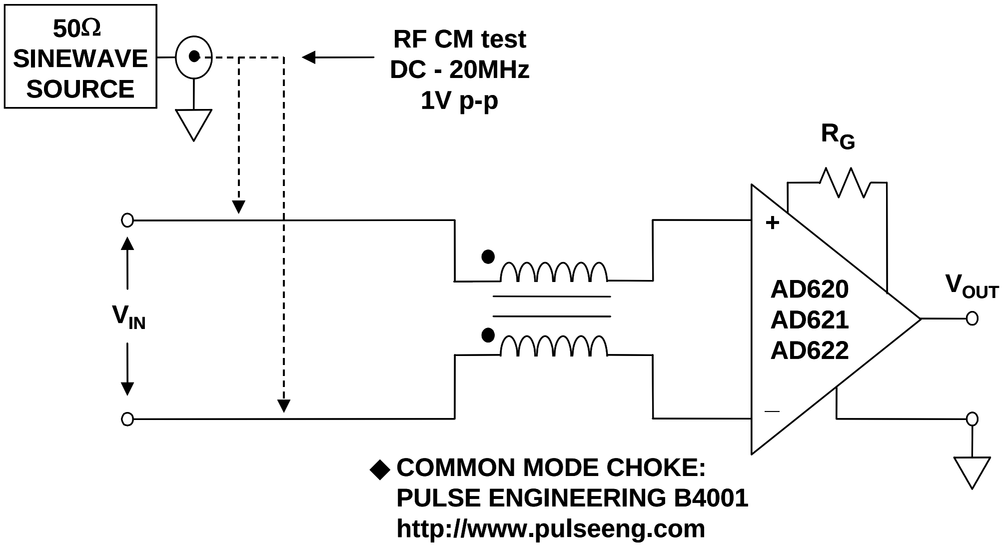


Figure 6: For Simplicity as Well as Lowest Noise EMI/RFI Filter Operation, a Common-Mode Choke is Useful With the AD620 Series In-Amp Devices

In addition to being a low component count approach, choke-based filters offer low noise, by dispensing with the resistances. Selecting the proper common-mode choke is critical, however. The choke used in the circuit of Figure 6 is a Pulse Engineering B4001. The maximum RTI offset shift measured from dc to 20 MHz at G = 1000 was 4.5 µV. Either an off-the-shelf choke such as the B4001 can be used for this filter, or, alternately one can be constructed. Since balance of the windings is important, bifilar wire is suggested. The core material must of course operate over the expected frequency band. Note that, unlike the Figure 5 family of RC filters, a choke-only filter offers no differential filtration. Differential mode filtering can be optionally added, with a second stage following the choke, by adding the R1-C3-R2 connections of Figure 5.

For further information on in-amp EMI/RFI filtering, see References 1-9.

Amplifier Outputs and EMI/RFI

In addition to filtering the input and power pins, amplifier *outputs* also need to be protected from EMI/RFI, especially if they must drive long lengths of cable, which act as antennas. RF signals received on an output line can couple back into the amplifier input where it is rectified, and appears again on the output as an offset shift.

A resistor and/or ferrite bead, or both, in series with the output is the simplest and least expensive output filter, as shown in Figure 7 (upper circuit).

Adding a resistor-capacitor-resistor "T" circuit as shown in Figure 7 (lower circuit) improves this filter with just slightly more complexity. The output resistor and capacitor divert most of the high frequency energy away from the amplifier, making this configuration useful even with low power active devices. Of course, the time constant of the filter parts must be chosen carefully, to minimize any degradation of the desired output signal. In this case the RC components are chosen for an approximate 3-MHz signal bandwidth, suitable for instrumentation or other low bandwidth stages.

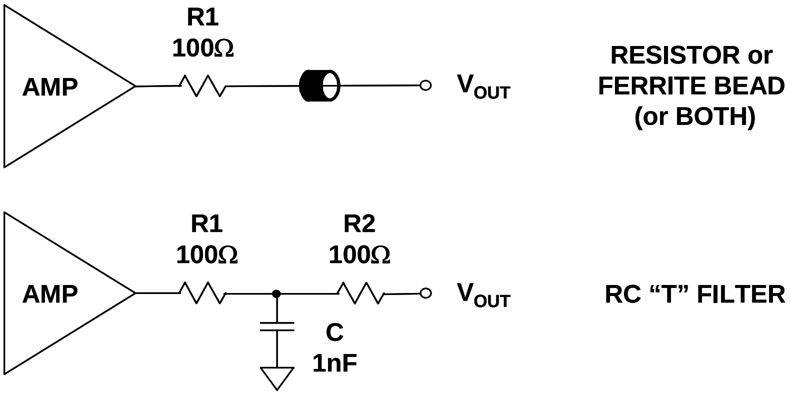


Figure 7: Op Amp and In-Amp Outputs Should be Protected Against EMI/RFI, Particularly if They Drive Long Cables

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