ABSTRACT

Title of Thesis:	**TESTING AND CHARACTERIZATION OF SILICON DEVICES AT CRYOGENIC TEMPERATURES**
	Jeffrey Foster Allnutt Master of Science, 2007
Directed By:	Professor Martin Peckerar Department of Electrical Engineering

Satellite and space exploration applications require electronics which are capable of operation at extremely low temperatures (T<40K). Low temperature device models are essential for the design of circuits operating in these extreme environments. To address these needs, a helium Dewar test setup has been constructed and used to evaluate several MOSFET devices, a bipolar device, and a tunneling structure. The temperature dependent performance of each has been characterized down to 20K and, in some cases, as low as 4K. Complete voltage and temperature dependent MOSFET characteristics have led to the development of a simulator which predicts device performance at cryogenic temperatures. A tunneling structure has demonstrated comparable low temperature voltage reference performance to that of a silicon germanium voltage reference circuit.

TESTING AND CHARACTERIZATION OF SILICON DEVICES AT CRYOGENIC TEMPERATURES

By

Jeffrey Foster Allnutt

Thesis submitted to the Faculty of the Graduate School of the
University of Maryland, College Park, in partial fulfillment
of the requirements for the degree of
Master of Science
2007

Advisory Committee:
Professor Martin Peckerar, Chair
Professor Neil Goldsman
Assistant Professor Pamela Abshire

© Copyright by
Jeffrey Foster Allnutt
2007

Acknowledgements

First, I would like to that my advisor, Dr. Martin Peckerar, for his continued guidance and support throughout my undergraduate and graduate education. Dr. Peckerar made my graduate education a reality and it has been a pleasure both working for him and having him as a personal friend.

I would also extend special thanks to the members of my committee, Dr. Neil Goldsman and Dr. Pamela Abshire, as both have assisted greatly in my education and research endeavors.

I would like to thank Akin Akturk for sharing much of his device knowledge with me and for his excellent modeling work in conjunction with my research. I would also like to thank Zenyep Dilli for providing me with several devices as well as a ring oscillator circuit. Thanks to Nicole Nelson and Marc Dandin for their help obtaining and using test equipment. I would like to thank Jimmy Wienke for taking this plunge with me and supporting me throughout, and thanks to all my lab-mates who have been there to answer questions and discuss ideas.

I would like to thank Shahid Aslam, Mike Johnson, Umesh Patel, and other members of the NASA Goddard Space flight center who have supported this research.

Finally, I would like to thank my family and friends. I am grateful to my parents for instilling in me the value of education and putting me in a position to succeed. I would also like to thank my friends who kept the local establishments busy without me, and Cameron for his vicarious support.

Table of Contents

Acknowledgements ..... **ii**
Table of Contents ..... **iii**
List of Figures ..... **v**
CHAPTER 1: Introduction **1**
1.1 Background 1
1.1.1 Semiconductor Device Physics 3
1.1.2 Low Temperature Phenomena 5
1.1.3 Low Temperature Testing Considerations 9
1.2 Research Objectives 14
1.2.1 Research Goals 14
1.2.2 Scope of Research 15
CHAPTER 2: Test Setup **18**
2.1 Cryogenic Test Dewar 18
2.1.1 Dewar Design 18
2.1.2 Internal Board Design 20
2.1.3 Thermal Considerations 21
2.2 Cooling Procedure 24
2.2.1 High-Vacuum Pump 25
2.2.2 Liquid Nitrogen Transfer 27
2.2.3 Liquid Helium Transfer 29
CHAPTER 3: Transistor Characterization **31**
3.1 MOSFET Characterization 31
3.1.1 Low Temperature Functionality 31
3.1.2 Low Temperature I-V Characteristics 35
3.2 BJT Characterization 48
3.2.1 Motivation and Test Procedure 48
3.2.2 BJT Test Results 49
3.3 MOSFET NOISE Analysis 51
3.3.1 Motivation 51
3.3.2 Test Setup and Measurement Process 52
3.3.3 Results 56
CHAPTER 4: Cryogenic Integrated Circuits **58**
4.1 Zener Diode Voltage Reference 58
4.1.1 Operation 58
4.1.2 Test Setup 60
4.1.3 Results 61
4.2 Ring Oscillator 67
4.2.1 Operation 67
4.2.2 Test Setup 68
4.2.3 Results 69
CHAPTER 5: Conclusions and Future Work **71**
5.1 Contributions 72

5.1.1 MOSFET Low Temperature Functionality 73
5.1.2 MOSFET I-V Characteristics 74
5.1.3 Zener Diode Voltage Reference 75
5.1.4 Cryogenic Testing Guide 76
5.2 Recommendations for Future Work 76
5.2.1 Full Process Characterization 76
5.2.2 Silicon MOSFET Voltage Reference 77
Appendix A: MOSFET Modeling and Simulation 78
A.1 Modeling 78
A.1.1 Semiconductor Device Equations 78
A.1.2 Incomplete Ionization and Mobility Modeling 80
A.2 Simulation 86
A.2.1 Current versus Temperature 86
A.2.2 I-V Characteristic Simulation 89
References 92

List of Figures

Figure 1: Energy Band Diagram of Silicon 3
Figure 2: Lattice Structure of (a) Intrinsic and (b) n-type Silicon 7
Figure 3: Storage Dewars: (a) Thermos beverage container and (b) Liquid helium Dewar 10
Figure 4: Infrared Laboratories test Dewar cross section [38] 11
Figure 5: Infrared Laboratories Test Dewar used for this research 19
Figure 6: Internal test board 20
Figure 7: Inside of test Dewar with proper wire heat-sinking to minimize heat injection 24
Figure 8: Alcatel pump and controller (left) and Balzers pressure gauge (right) 25
Figure 9: Dewar connected to vacuum pump 26
Figure 10: (a) LN_2 storage Dewar with fill tube and (b) Top view of test Dewar 27
Figure 11: Helium transfer from storage Dewar to test Dewar 30
Figure 12: Keithley 2700 (top) and Lakeshore 340 (bottom) 32
Figure 13: Schematic of MOSFET functionality test setup 33
Figure 14: Saturation Current versus Temperature (Device A) 34
Figure 15: Hewlett Packard 4156B Semiconductor Parameter Analyzer 36
Figure 16: Hewlett Packard 16058 Personality Board 37
Figure 17: Schematic of MOSFET I-V characteristic test setup 37
Figure 18: I_D versus V_{DS} family of curves at 37K (Device B) 39
Figure 19: I_D versus V_{DS} family of curves at 293K (Device B) 39
Figure 20: I_D versus V_{DS} Curves for Several Temperatures at $V_G = 5V$ (Device B) 40
Figure 21: I_D versus T Curves for linear and saturation regions (Device B). Current is normalized to 1 at room temperature to show rate of increase. 41
Figure 22: I_D versus V_{DS} curves for several temperatures at $V_G = 3V$ (Device C) 43
Figure 23: I_D versus T curves for linear and saturation Regions (Device C). Current is normalized to 1 at room temperature to show rate of increase. 44
Figure 24: Decrease in current after device saturation (Current Dip) as a function of temperature (Device C) 45
Figure 25: Saturation I_D versus T curves for several MOSFET devices. Current is normalized to 1 at T=120K to emphasize the rate of change at higher and lower temperatures. 47
Figure 26: I_C versus V_{CE} Curves for several temperatures at $I_B = 50\mu A$ (BJT) 50
Figure 27: I_C versus T in the forward active region of operation (BJT) 50
Figure 28: HP4396B Spectrum Analyzer 52
Figure 29: Stanford Research Systems SR570 Low-Noise Current Preamplifier 53
Figure 30: Schematic of MOSFET noise test setup 54
Figure 31: Resistive heater mounted on test board (bottom-middle) 55
Figure 32: MOSFET Noise versus Frequency at room temperature and 20K 57
Figure 33: Zener diode I-V characteristic 59
Figure 34: Zener diode voltage reference test setup 60
Figure 35: Zener diode reference voltage versus input voltage at T=37K 61

Figure 36: Reference Voltage versus Temperature for zener diode and SiGe voltage references (normalized to one at T=100K) 62
Figure 37: Zener diode reference voltage versus temperature near T=37K 63
Figure 38: SiGe reference voltage versus temperature near T=37K........................... 64
Figure 39: Zener diode voltage reference stability at T=37K.................................... 65
Figure 40: SiGe voltage reference stability at T=37K 66
Figure 41: Schematic of Ring Oscillator Circuit 68
Figure 42: Tektronix TDS 744A Oscilloscope 69
Figure 43: Frequency versus Temperature (Oscillator B) 70
Figure 44: Calculated ionization rates of phosphorus and Boron in Silicon at room temperature (left) and 50K (right) as a function of dopant concentration, using three different models 85
Figure 45: (a) Calculated and measured current versus temperature characteristic for device A, and (b) calculated doping profile at T=50K using Model 3. Colorbar shows concentration in cm^{-3} (V_{GS}=4V, V_{DD}=5V)... 87
Figure 46: Calculated MOSFET potential profiles at 40K, using (a) Model 1, and (b) Model 3 (V_{GS}=4V, V_{DD}=5V) 89
Figure 47: Calculated (circles) and measured (lines) I-V families of curves for (a) device A at 293K and device B at (b) 37K, (c) 60K, and (d) 120K, using Model 3 .. 90

CHAPTER 1: Introduction

1.1 Background

As space exploration, satellite communications, and other extraterrestrial activities become increasingly common, so too has the need for electronics that function at extremely low temperatures. The operational temperature of space assets can vary anywhere from a few Kelvin, in the cold of deep space, all the way up to 100-200K for satellites in near earth orbit exposed to the extremes of solar radiation [1]. While electronics do exist that operate at these temperatures, their development is severely limited by inefficient design tools and prohibitive costs. Two main reasons exist for these limitations. First, there is a lack of simulation and modeling capabilities in the low temperature electronics community. Standard semiconductor simulation models, such as the industry standard Berkeley Simulator (BSIM), only support temperatures down to approximately -55°C. These models do not take into account the physical changes that occur below this temperature and thus provide inaccurate simulation results for space applications. The second reason is due to a perceived need for exotic technologies such as silicon germanium based devices [2]. While these technologies are not without merit, they are more expensive and less widely available than standard silicon and are not absolutely necessary for every low temperature application. These technologies also suffer from the lack of a sound modeling basis for designs at low temperature.

The lack of modeling capabilities described above forces the designer to choose one of two approaches. One can either use rule-of-thumb estimates in which a device is fabricated and then tested at low temperature in the hope that it works, or

the device can be contained in a temperature controlled environment. The guess and check approach is extremely inefficient and has no guarantee of producing the desired results. The second approach has a much greater chance of success, but changing the environment instead of the device itself has many drawbacks, including increased power consumption, weight, and size, all of which are at a premium on a spacecraft. Furthermore, this option is not always available. Clearly, neither of these design approaches is desirable from an economic or feasibility standpoint.

The ideal environment for low temperature design would include the ability to accurately model and simulate circuits and low temperature, and the option to use standard silicon CMOS processes. By demonstrating and characterizing the functionality of standard silicon transistors over the range from room temperature to cryogenic space temperatures, the development of a physics based model that will accurately predict device operation over this range becomes possible. Such a model would allow for a systematic design process, no different then that used for standard circuit design at room temperature. The "guess and check" aspect of low temperature design would be eliminated, providing substantial time and cost savings. In addition, designers would have the ability to use relatively inexpensive, well-developed silicon CMOS processes for low temperature circuits.

This section will provide a brief background in semiconductor device physics and discuss low temperature phenomena that affect device performance. Specifically, the formation of impurity bands, as well as impurity dependent changes in activation energy will be discussed, as this is central to device operation at low temperature. In addition, this section will also provide background information on cryogenics and

mechanisms of heat transfer. It should be noted that the temperature of 37K appears several times throughout this work. This is due to the fact that much of this research was aimed at a NASA specification at this temperature. The body of work presented, however, is relevant over a large range, not just a single temperature.

1.1.1 Semiconductor Device Physics

This subsection will offer a brief background in semiconductor device physics. Discussion is limited to background information relevant to the understanding of low temperature effects.

The basis of any silicon semiconductor is an intrinsic silicon wafer that is nearly pure. Silicon is a column IV element, meaning that it has four valence electrons which form covalent bonds with four neighboring atoms. It follows from the application of quantum mechanics that the allowed energy levels of electrons in a solid can be grouped into bands [3]. These energy bands are separated by forbidden regions of energy that cannot be possessed by electrons in the material. These are so called bandgaps. The energy-band diagram of silicon is shown below in Figure 1.

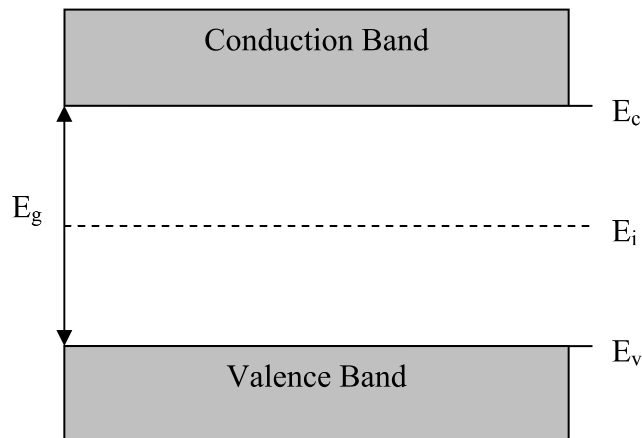


Figure 1: Energy Band Diagram of Silicon

In Figure 1, E_c and E_v represent the conduction and valence band energies, respectively. E_g is the energy difference between the conduction band and valence band, also known as the bandgap energy. E_i is the intrinsic Fermi level, the energy at which the probability of occupation of an energy state by an electron is one-half. At absolute zero temperature, the valance band is completely full of electrons and there are no mobile carriers in the conduction band, thus current conduction is impossible. As the temperature increases, electrons are promoted via thermal energy into the conduction band, leaving behind holes in the valence band. This ionization creates a free carrier concentration and allows for conduction to take place [4].

What differentiates a semiconductor from a metal is that metals have electrons in the conduction band even at absolute zero temperature, allowing for conduction at any temperature. Insulators, on the other hand, have a much larger bandgap energy that does not allow for the excitation of electrons into the conduction band at room temperature. In practice, the relatively large silicon bandgap energy of 1.1eV [5] leads to a low mobile carrier concentration and makes it a poor conductor even at room temperature. To obtain more desirable electrical properties, impurity atoms (dopants) are added to the intrinsic silicon.

Silicon dopants come from either column III (boron) or column V (arsenic or phosphorus) of the periodic table. A column V atom has five valence electrons, meaning that it will form four covalent bonds in the silicon lattice and have a loosely bonded extra electron. The addition of column V dopants creates impurity energy states in the forbidden region between the valence and conduction bands. Located close to the conduction band, these energy states reduce ionization energies and

increase the number of mobile carriers, making the doped silicon a much better conductor. Silicon doped in this fashion is known as n-type, and its electrical conductivity is dominated by electrons in the conduction band. Column III dopants work in the opposite fashion. Since they only have three valence electrons, they can be ionized by accepting an electron from the valence band, thus leaving behind a mobile hole. This type of doping produces p-type silicon, in which electrical conduction is dominated by holes in the valence band.

Over an intermediate range of temperatures in doped silicon, including room temperature, there is enough thermal energy to fully ionize all mobile carriers. This is due to the small energy gap between the impurity energy states and conduction band (or valence band for p-type). The mobile carrier concentration over this range is generally assumed to be the same as the doping concentration [4]. As temperature decreases below this range, however, there may no longer be enough thermal energy to ionize all the impurity atoms. This condition is known as incomplete ionization, or freeze-out [6]. As will be explained in the following subsection, doping and incomplete ionization are key to the understanding and modeling of low temperature device operation.

1.1.2 Low Temperature Phenomena

As temperature decreases, there are two physical phenomena that dominate device operation, increased mobility and incomplete ionization. High mobility is generally good for component performance as long as it can be modeled. Freeze-out is bad as it increases parasitic resistances and decreases a transistor's current drive capability.

Mobility is determined by two main scattering mechanisms, electron-phonon scattering and impurity scattering. Electron-phonon scattering is due to scattering in the silicon lattice, while impurity scattering is due to ionized impurities. At higher temperatures (near room temperature) scattering by ionized impurities is less effective since the faster moving carriers interact less effectively with stationary impurities [26]. Initially, as temperature decreases, mobility increases due to a decrease in the electron-phonon scattering rate [27-30]. This increase continues until the impurity scattering effect begins to dominate over the lattice vibrations, causing the mobility to reach a maximum value and then roll off. The location of the roll-off point is a function of doping. Temperature models have been developed which include these mobility effects as well as the decrease in current at lower temperatures due to the increase in built in potential [15, 27-28]. These models show an increase in MOSFET current for decreasing temperature in the region where electron-phonon scattering is dominant, followed by a sharp decrease in current in the region where impurity scattering begins to dominate. An accurate low temperature model, however, must also include the effects of impurity concentration as it pertains to incomplete ionization [31].

If one were to simply extract the mobile carrier occupancy of a band assuming an “activation energy” model then the promotion energy from the dopant level to the band-edge is fixed, significant freeze-out effects would be observed at temperatures below 77K. This, though, does not occur in modern, deeply scaled ($10^{18}/cm^3$) VLSI. This is due to the more heavily doped source/drain regions encountered in scaled structures. Heavy doping leads to impurity band formation. Impurity band formation

and charge conduction through this band has been studied ever since the introduction of solid-state devices [12-14]. To understand the formation of impurity bands it is important to understand how the semiconductor doping process works. Figure 2 below shows the lattice bond structures of intrinsic silicon and phosphorus doped n-type silicon.

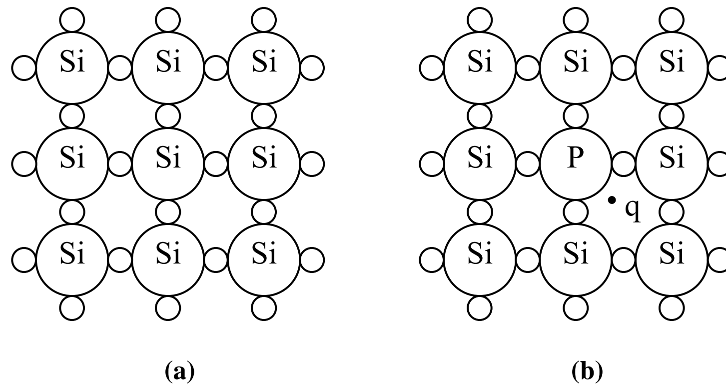


Figure 2: Lattice Structure of (a) Intrinsic and (b) n-type Silicon

The process of doping silicon creates impurity energy states in the forbidden gap between the conduction and valence bands. Increasing the impurity concentration causes increased interaction between the impurity states. Eventually, when doping exceeds $10^{16}/cm^3$, the impurity states themselves form a band. To clarify this, realize that most impurity atoms are situated far apart in the lattice and thus their bound electrons do not interact with one another [7]. As doping levels increase, however, the impurity atoms become situated closer together. When the distance between two such atoms shrinks to less than two Bohr radii, quantum mechanical mixing occurs due to Coulomb interaction [8]. Further increases in doping cause additional impurity atoms to interact with one another, leading to the formation of impurity clusters. At doping densities greater than 10^{18} cm^{-1}, clusters of three or more impurity atoms outnumber

isolated impurities [8-11]. This increase reduces activation energies in two ways. First, the clusters interact to broaden the impurity band and the density of states (DOS) associated with these bands [8]. Second, the dopant energy level approaches the conduction band since the excess electrons are less strongly bound to their column VI impurity cores [9].

Over the years, a number of theories have been proposed to explain how both doping concentration and temperature affect incomplete ionization, as well as the implications of these effects on device performance [15-25]. There have also been approaches developed to include incomplete ionization models in device simulators. Despite this work, there remains a level of ambiguity about the effects of incomplete ionization on device performance and inclusion of incomplete ionization models in device simulators. There have been several works that suggest that ionization rates decrease for higher dopant concentrations, with no full ionization observed at very high concentrations [20-25,32,33]. Recent works by Altermatt et al., however, suggest otherwise [16-18]. These papers predict a decrease in ionization rate beginning at doping densities of approximately 10^{18} cm^{-1} and then a return to full ionization near 10^{19} cm^{-1} due to Mott metal-insulator transition [34]. If this, in fact, what happens, then heavily doped devices may not suffer from incomplete ionization effects at low temperature as previously thought.

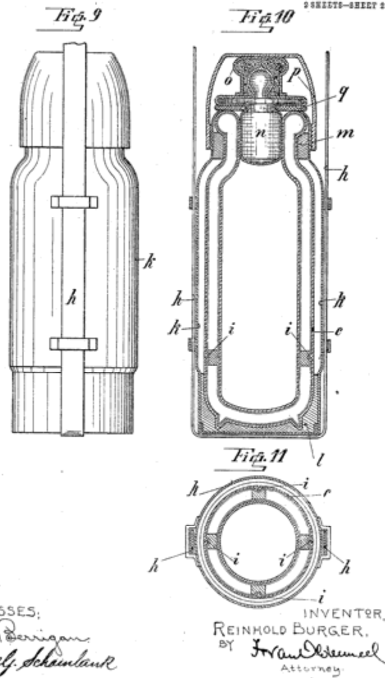
It is apparent from a review of the literature that a complete device data set that provides current-voltage characteristics from cryogenic temperatures up to room temperature is needed for heavily doped structures. This data would provide a reference point from which different incomplete ionization models could be verified

or disproved. This would subsequently allow for the development of a low temperature model which incorporates doping dependent incomplete ionization, impurity band conduction, and temperature dependent mobility effects to accurately predict low temperature operation. These data are provided in this thesis. They are, in fact, the major contribution of this work to the scientific literature.

1.1.3 Low Temperature Testing Considerations

Cryogenic testing presents many inherent challenges. Cooling a device to extremely low temperatures in an environment which permits electronic testing requires highly specialized equipment, as well as knowledge of the heat transfer processes which govern the temperature of the system. This section will serve as an introduction to the low temperature testing process and provide a general background on the mechanisms of heat transfer.

Cryogenic testing is performed inside a device called a Dewar (named after its inventor, James Dewar [35]), which is a container designed to keep its contents hotter or cooler than the ambient environment. In its simplest form, a Dewar is double-walled container with an evacuated region between its inner and outer walls. Two such containers are shown below. Figure 3a is a drawing from the patent application for the first commercial Dewar, also known as the Thermos beverage container [36]. Figure 3b shows a standard liquid helium Dewar. The vacuum region does not permit heat transfer via conduction or convection, and thus maintains the temperature of the contents for an extended period of time.



(a) **(b)**

Figure 3: Storage Dewars: (a) Thermos beverage container and (b) Liquid helium Dewar

The Thermos and liquid helium Dewar shown above are only useful for storing liquids. To perform actual low temperature testing, a more complicated type of Dewar is needed. The cross section of a test Dewar is shown below in Figure 4. Much like the containers shown above, this Dewar contains vacuum shielded vessels for liquid nitrogen and liquid helium. In addition, however, there is a radiation shielded vacuum chamber in which the device under test (DUT) is located. This Dewar minimizes convection and radiation (as well as unwanted conduction through air), and uses conduction from the helium vessel through the cold plate to the DUT as the only means of heat transfer. The following paragraphs will explain the three

mechanisms of heat transfer and chapter two will discuss the operation and use of the test Dewar in greater detail.

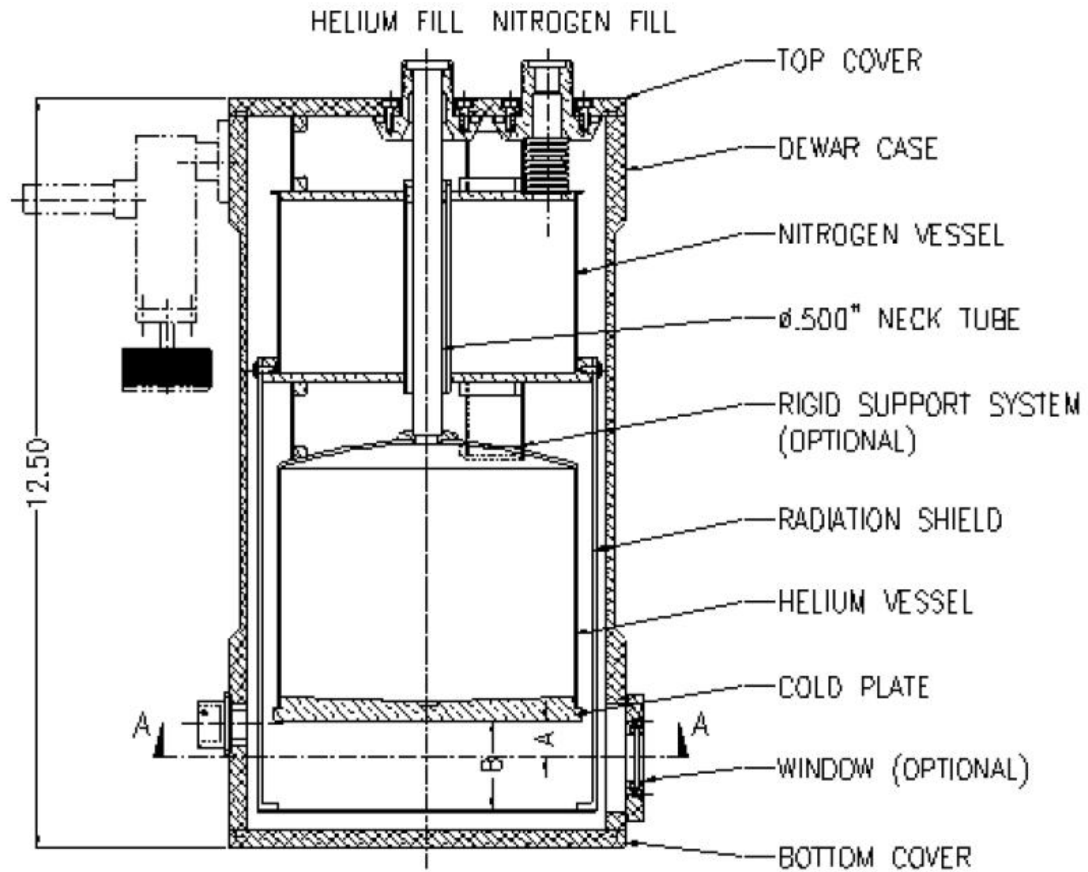


Figure 4: Infrared Laboratories test Dewar cross section [38]

Conduction, convection, and radiation are the three mechanisms of heat transfer. Of the three, radiation is the only one which can transfer energy through a vacuum. When designing a low temperature test setup, it is essential to understand how each of these processes works to achieve the desired cooling effects as efficiently as possible.

Conduction is the process by which thermal energy is transferred from a region of higher temperature to a region of lower temperature. It can occur within a single medium or across two mediums which are in physical contact with each other.

On an atomic scale, this transfer represents the exchange of kinetic energy between electrons in a material, either due to vibration of electrons in the lattice or the motion of free electrons [37]. Metals are good thermal conductors due to their high concentration of free electrons, whereas insulators have the opposite effect. Gases are very poor thermal conductors because of their large separation distance between particles [37]. The amount of energy transferred Q during time interval Δt due to conduction is given by the following formula:

$$\frac{Q}{\Delta t} = kA\frac{dT}{dx} \tag{1}$$

In the equation above, A is the cross-sectional area, T is the temperature difference over a length x or temperature gradient, and k is the thermal conductivity proportionality constant. Since the dominant heat transfer mechanism in a cryogenic test setup is conduction, this equation is very important. It determines how quickly thermal energy will be transferred out of the DUT through the cold plate, and hence, how fast the device will cool. Copper is generally used for the cold plate since it has very high thermal conductivity and thus achieves maximum energy transfer between the helium vessel and the DUT.

Convection is the transfer of thermal energy via circulation of warmer particles to cooler areas. For convection to occur, a heat source must be surrounded by a fluid medium. The source transfers heat to the fluid, which in turn causes it to become less dense and rise. The rising fluid is then replaced by the surrounding cooler fluid. This process continues until the heat source and the surrounding medium reach equilibrium [37]. This process can be accelerated by using a fan to increase the speed of circulation between hot and cold fluids.

If the DUT was not contained in a vacuum chamber, convection would occur in the opposite manner as that described above. The device under test would receive heat from the surrounding air, causing the air to descend and be replaced by warmer air. This process would continue until the device was at equilibrium with the surrounding air. This process would make cryogenic testing extremely inefficient, if not impossible. The test Dewar is thus pumped down to a very low vacuum pressure to minimize convection.

The third means of heat transfer is radiation. All objects radiate energy continuously in the form of electromagnetic waves produced by thermal vibrations of atoms [37]. The rate at which an object radiates energy is governed by Stefan's Law, which states that radiation rate is proportional to the fourth power of absolute temperature. This relationship is given below in (2), where P is the power radiated by the object, σ is a constant, A is the surface area, e is the emissivity constant, and T is the surface temperature. The emissivity constant is the ratio of energy radiated by the object to that radiated by a perfect black body.

$$P = \sigma A e T^4 \tag{2}$$

Since radiation is capable of propagating through a vacuum, the DUT inside the Dewar is susceptible to heating via radiation. This heating is obviously undesirable and would lead to temperature gradients across the device. To minimize this effect, the test chamber inside the Dewar is surrounded by a liquid nitrogen cooled, aluminum radiation shield. Thus, instead of seeing 300K radiation from the outer casing of the Dewar, the DUT sees the 77K, radiation shield, which minimizes

heating due to radiation and allows conduction to dominate the temperature of the device.

1.2 Research Objectives

1.2.1 Research Goals

The primary objective of this research is to advance the understanding of silicon device operation at cryogenic temperatures. Several different transistors will be tested and characterized at low temperature. A heavy focus is placed on MOSFETs since these devices have the potential for low temperature operation due to their higher doping concentrations. The goals of this testing and characterization process are to demonstrate MOSFET functionality at cryogenic temperatures and provide complete families of I-V curves at temperatures ranging from room temperature down below the NASA specification of 37K. In doing so, this research will provide the basis for the development and verification of a physics-based model that predicts device performance at any temperature. Such a model would enable the cost effective use of standard silicon MOSFETs in space and other low temperature applications.

In addition to testing and characterizing transistors, this research will explore an alternative to the use of expensive silicon-germanium (SiGe) based structures for the design of a low temperature voltage reference circuit. A zener diode reference with a temperature compensating resistor will be tested as a solution to meeting the specification of a 37K voltage reference. The goal of this study is not to discount the merits of SiGe technology, but rather to illuminate a more cost effective alternative for the specific application.

The third goal main goal of this research is to examine how changes in MOSFET device performance at low temperature affect circuit performance. A ring oscillator will be tested since it is a relatively simple circuit and its oscillation frequency is directly related to device current. Thus, changes in current with temperature should be reflected by an increasing or decreasing frequency of oscillation.

To meet these challenges, a helium Dewar based cryogenic test setup has been constructed and used to test several different devices. These include various MOSFET transistors, a bipolar junction transistor (BJT), a zener diode voltage reference, and two ring oscillator circuits. The following subsection will outline the scope of the research and the contributions made to the low temperature electronics community.

1.2.2 Scope of Research

This research investigates the operation of various semiconductor devices and circuits at low temperature. Chapter 2 focuses on the design and operation of a cryogenic test setup which facilitates testing of electronic components at low temperatures. The design of a specialized helium test Dewar is explained, and a description of the internal test board is also provided. This is followed by an explanation of the many thermal considerations that must be taken into account when designing a low temperature test setup. Several factors, including vacuum levels, outgassing, cleaning, and heat transfer are discussed. Finally, the complete, step-by-step cool down process is described in detail, providing pictures and descriptions of everything from pump down to helium transfer. This chapter aims to serve as a basic

reference which will minimize the steep learning curve associated with cryogenic testing.

Chapter 3 details the prcedures and results of the transistor characterization process. First, a MOSFET device is tested for functionality at cryogenic temperatures. A small transistor is used to reduce current and subsequently minimize self heating. Once transistor functionality is established, the I-V characteristics of several devices are measured over the entire temperature range of interest to provide the basis for a simulation model. One of the devices tested in this fashion is a large transistor. The results of this test provide insight into self heating effects. The I-V curve families of a bipolar junction transistor (BJT) are also measured to verify the theory of BJT freeze-out due to a lower doping concentration in the base. At the end of this chapter, a noise test is also conducted to measure the reduction in 1/f noise due to low temperature operation.

In chapter 4, two different types of circuits are tested at low temperature. The first of the two is a zener diode based voltage reference. A zener is chosen as a suitable alternative to a SiGe based voltage reference because it operates as a tunneling structure under reverse bias. These structures are extremely heavily doped ($>10^{19}/cm^3$) and should not be susceptible to incomplete ionization. The zener is tested in two configurations, with the series resistor outside the test Dewar to determine the zener temperature dependence and with the resistor inside the Dewar to provide temperature compensation. The results of these tests are compared against a SiGe voltage reference circuit which is also tested at low temperature. The second type of circuit tested in chapter four is an integrated ring oscillator. This test is

conducted to determine if increases in current due to decreasing temperature will correspond to increasing oscillation frequency.

CHAPTER 2: Test Setup

The first major challenge of this research was to design an environment suitable for testing electronic devices at cryogenic temperatures. To meet this challenge, a liquid helium based cryogenic test setup has been constructed with internal electrical connections for transistors and integrated circuits in various packages. This section will describe the test setup assembly process and discuss the many thermal considerations that must be taken into account when designing for low temperature. It will also describe the steps necessary to actually cool the Dewar and perform low temperature testing. The test setup and cool down procedures described in this chapter will form the basis for the low temperature measurements described in chapters three and four.

2.1 Cryogenic Test Dewar

2.1.1 Dewar Design

As was stated in chapter one, a highly specialized Dewar is required for low temperature testing. It must be able to not only store liquid like the Thermos-style Dewar shown in Figure 3a, but also provide a cold, dry, electronics testing compartment with connections to the outside world. The cross section of the test Dewar used for this research was shown in chapter one (Figure 4) and the actual Dewar is shown below in Figure 5.

Figure 5: Infrared Laboratories Test Dewar used for this research

The test Dewar consists of three main compartments, these include the liquid nitrogen (LN_2) tank, liquid helium (LHe) tank, and the device testing area below the helium tank. As was explained in chapter one, the DUT is heat sunk to the LHe chamber via a copper cold plate. Vacuum seals are located at the bottom plate, the top plate, and the pump connector. It is important to note that the sealed inner parts of the Dewar are kept under vacuum during testing to maintain insulation for the cryogenic holding tanks. A radiation shield which is heat sunk to 77K extends down from the liquid nitrogen tank to surround both the liquid helium tank and the test chamber. This increases the lifetime of the LHe and thus the hold time of the system as well.

2.1.2 Internal Board Design

To facilitate the testing of various transistor devices and other integrated circuits, a board has been mounted inside the Dewar on the cold plate. The board consists of a socket to accommodate both 40 and 28 pin dual-inline packages (DIP40, DIP28), a temperature sensor, and free space which can be populated with a heater or other various components as desired. The test board is shown below in Figure 6.

Figure 6: Internal test board

As shown in the photo above, the test board contains the following components: resistor (top left), zener diode voltage reference (top middle), transistor housed in a DIP40 package (middle), thermal diode sensor (top right), commercial MOSFET (bottom right), commercial BJT (bottom left beneath aluminum tape). Here, the board is shown with copper standoffs. This is one of several board configurations that have been used for this research. The board components, as well

as the thermal connections from the board to the cold plate, have been varied based on what is being tested and the desired cooling rate. Thermal considerations and cooling rate will be discussed in the next subsection.

2.1.3 Thermal Considerations

When performing cryogenic testing, thermal effects are of utmost importance. Improper design may result in a system exhibiting unacceptable temperature fluctuation, or worse, is impossible to cool down to the desired testing temperature. To ensure that this does not occur, many thermal considerations must be taken into account.

The first key to low temperature testing is a very high vacuum. If a sufficiently low pressure is not reached within the system, several adverse effects occur. First, particles left in the Dewar permit heat transfer via conduction and convection as described in chapter one, which prevents the cryogens from establishing equilibrium with the inner wall of their containers. This leads to rapid boil-off and make the system very difficult to cool. Second, a poor vacuum environment contains water vapor molecules. If the DUT is cooled within such a medium, then water vapor will condense on the cold surfaces, which can lead to failure for sensitive electronic components. The test Dewar should be pumped down to a pressure of at least $2*10^{-5}$Torr before cooling begins. This ensures that nearly all of the nitrogen, oxygen, and water vapor have been pumped out of the system, and only inert gases remain [46].

To achieve the desired low pressure, high vacuum grease is applied to each of the o-ring seals within the Dewar and a turbocharged vacuum pump is used. To

minimize pump-down time, outgassing materials such as electrical tape are avoided. Outgassing is the release of gas particles that have been trapped or absorbed inside a material [39]. At atmospheric pressure, the rate at which most materials outgas is relatively insignificant. In space applications, however, pressures are generally on the order of 10^{-6}Torr or lower; outgassing presents a challenge to maintaining such high-vacuum environments. NASA maintains a database which provides outgassing data for selecting spacecraft materials [40]. In addition to proper material selection, the inside of the Dewar is thoroughly cleaned with isopropyl alcohol before each test to remove outgassing impurities.

As was explained in chapter one, nearly all heat transfer within the evacuated test Dewar system occurs via conduction. To minimize temperature gradients across the test board and maintain consistent temperatures, standoffs are placed around the edges as well as in the middle of the board. This configuration ensures that the temperature measured by the thermal diode is as close as possible to that of the test components, since each is heat sunk via copper or aluminum to the board. In Figure 6, the board is shown with copper standoffs. These copper thermal connections are typically used, but brass standoffs are also used depending on the desired cooling rate. The thermal conductivity of brass is approximately 1/3 that of copper [41], so the rate of cooling can be increased or decreased accordingly. In any cryogenic test setup, there is an inherent tradeoff between cool down time and hold time, or the amount of time the system can remain cold. Increased thermal conduction between the cold plate and the DUT means that the device will cool faster, but also warm faster once the cryogens boil off. Thermal isolation between the cold plate and the

DUT has the opposite effect. The device will not cool as quickly, but it will remain cold for a longer period of time.

In addition to using different standoff materials, the rate of cooling is also affected by the addition (or subtraction) of mass from the system, which occurs in the form of different test components. This is due to the specific heat of the added material, which is a measure of the amount of energy required to raise the temperature of that material by 1K. Or, from a cooling standpoint, it is the amount of energy that must be removed to decrease the temperature by 1K. The heat capacity of a substance, which is a function of specific heat and mass, is given below:

$$Q = mc\Delta T \tag{3}$$

In (3), Q is energy, m is mass, and c is the specific heat of the material. It follows that as mass increases, the amount of energy required to change the temperature of the substance increases as well. When several components are being tested during the same cool down, the thermal conductivity between the board and the cold plate is increased to account for this increase in mass.

The last thermal consideration, which can be easily overlooked, is the internal Dewar wiring. Wires link the DUT to the outside world, and hence, provide a thermal link to a 300K environment. Two steps are taken to minimize heat injection from the wires. First, very thin gauge wires are used to minimize cross-sectional area and hence thermal conduction. Second, the wires are heat sunk to the 4.2K LHe cold plate, and then to the 77K radiation shield on their way out of the Dewar. If these steps are not taken, then the cooling power of the system will be severely compromised. In Figure 7 below, the inside of the test Dewar is shown after having

been prepared for cooling. This photo shows the outer casing of the Dewar, the radiation shield, and the board mounted to the cold plate. Note that the wires have been heat sunk to both the cold plate and the radiation shield using thermally conductive aluminum tape.

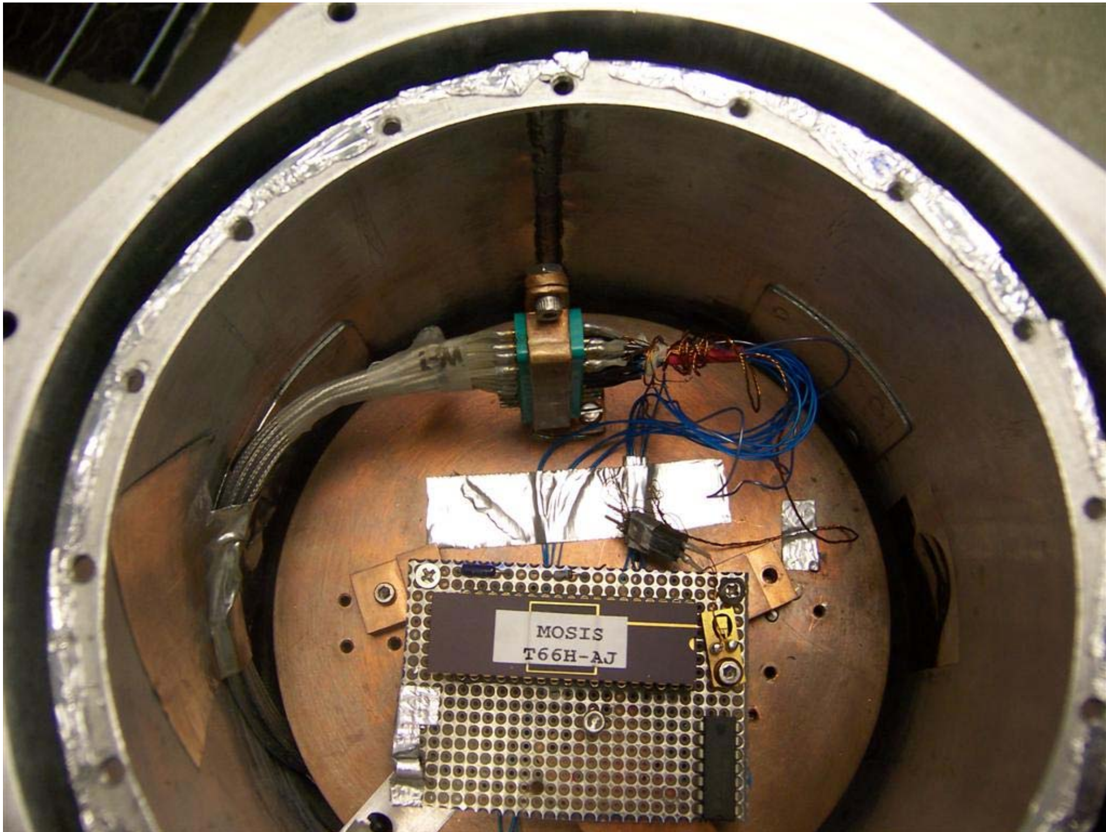


Figure 7: Inside of test Dewar with proper wire heat-sinking to minimize heat injection

2.2 Cooling Procedure

The process of cooling the test Dewar from room temperature down to temperatures below 37K requires several steps. The goal when cooling the system is to minimize the use of liquid helium, since it is considerably more expensive than its LN_2 counterpart. Steps are taken to use LHe as efficiently as possible. Since the cool

down process is the same regardless of which device is being tested, it is prudent to explain this procedure in a detailed, step-by-step fashion.

2.2.1 High-Vacuum Pump

The first step in the cool down process is to establish a high-vacuum environment. This is done using an Alcatel 2008A turbo pump connected to a CVF-100 controller and a Balzers pressure gauge. The pump and pressure gauge are shown below in Figure 8.

Figure 8: Alcatel pump and controller (left) and Balzers pressure gauge (right)

Initially, the pump itself and tube fixture must be evacuated. Since the pump has been evacuated many times and is designed minimize outgassing, this is usually

very quick process. After being on for a minute or two, the turbo spins up to speed and the pressure drops down to the order of 10^{-6}Torr. At this point, the pump is connected to the Dewar as shown in Figure 9 and the valves on both the Dewar and the pump are opened to allow evacuation of the Dewar.

Figure 9: Dewar connected to vacuum pump

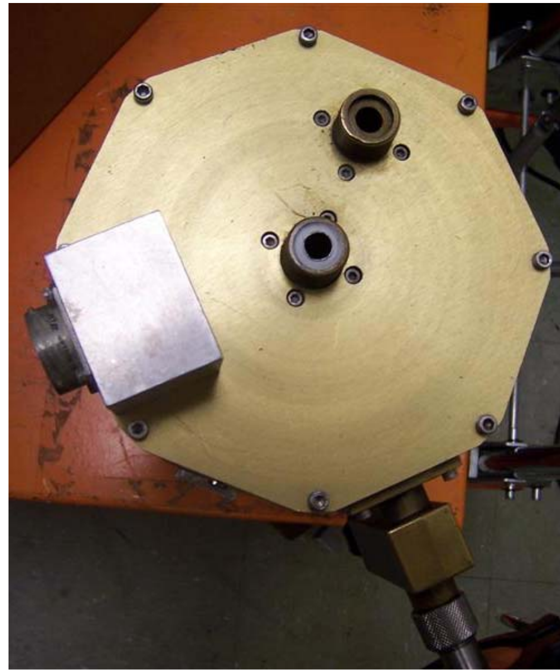
The amount of time required to pump down the test Dewar depends on volume and outgassing materials. If the system has been pumped down before and thus the components inside have already been outgassed, then pumping time is significantly reduced. This particular test Dewar has a relatively small volume and takes only a matter of minutes to pump down to a suitable fill pressure of $2*10^{-5}$Torr.

By contrast, large Dewars may take several hours to pump down to a reasonable fill pressure.

2.2.2 Liquid Nitrogen Transfer

Once the Dewar has reached a suitable vacuum, it remains attached to the pump while it is filled with LN_2. Liquid nitrogen filling is done using the direct injection fill tube connected to the storage Dewar as shown in Figure 10a. The fill tube connects to an internal tube which extends to the bottom of the tank. Since the LN_2 is stored under pressure, opening the release valve causes liquid to flow out of the storage tank. Figure 10b shows the top of the Dewar with openings for the LHe (middle) and LN_2 chambers.

(a)



(b)

Figure 10: (a) LN_2 storage Dewar with fill tube and (b) Top view of test Dewar

Initially, both the inner LHe and outer LN_2 tanks are filled with liquid nitrogen. This is done to cool the entire system as much as possible while saving LHe. If liquid helium was filled into a room temperature container, excessive amounts of the expensive cryogen would boil off. After approximately 1-2 hours, depending on the exact internal configuration, the nitrogen fill cools the system down to the LN_2 temperature of 77K. Once again, it should be noted that this cool down time is heavily dependent on the internal DUT configuration, which can range anywhere from a minutes to days. Once the temperature reaches 77K, or is within a few Kelvin, the Dewar is ready for the next step.

When the Dewar reaches equilibrium with the LN_2, the air valve is closed and pump is disconnected. At this stage, the cold inner surfaces of the test Dewar act like a pump. The inert gas molecules adsorb on to the 77K inner surfaces and do not permit conduction through the vacuum insulation [46]. If the pump is disconnected prematurely, the test Dewar will feel cold to the touch and condensation will appear on the outside surface, this is a telltale sign that internal equilibrium has not yet been reached. If this occurs, the pump should be reconnected to stop the condensation and give the inner surfaces of the test Dewar additional time to equilibrate with the 77K LN_2. After the pump is disconnected, the LN_2 is carefully dumped out of both chambers to make room for LHe in the inner tank. The outer chamber is then quickly refilled before the system begins to warm up. The test Dewar is now ready for liquid helium filling.

2.2.3 Liquid Helium Transfer

Liquid helium is stored in the Dewar shown above in Figure 3b. This Dewar is similar to one that stores LN_2, but has a special fitting on top with pressure release valves and an opening for a liquid helium transfer tube. The LHe transfer tube has an inner and outer chamber and utilizes the same vacuum insulation principle as the Dewar. It is also fitted with an o-ring seal to prevent pressure loss during fills. Without a vacuum tube, it would be impossible to transport a liquid with a boiling point of 4.2K through a room temperature medium. To initiate a fill, the pressure-release safety valves are closed and the transfer tube is slowly inserted into the top of the tank. As the warm tube contacts the cryogenic liquid, pressure builds up inside the storage tank and forces the LHe up through the tube and into the Dewar. When fill is complete, the safety valve is opened to release excess pressure and the tube is removed from the tank. Figure 11 shows a helium transfer in progress. In this picture a larger test Dewar is being filled than the one used in this research, but the transfer process is exactly the same.

Figure 11: Helium transfer from storage Dewar to test Dewar

Depending on the amount of LHe transferred to the test Dewar and the thermal considerations discussed earlier in this chapter, the system may reach the LHe temperature of 4.2K. In practice, the experiments conducted in this research were generally run over a temperature range from approximately 20K to room temperature. A minimum temperature of 20K is well below the NASA specification of 37K and is suitable for most space applications. If desired, the test Dewar could be reconfigured to cool much faster for 4.2K testing.

CHAPTER 3: Transistor Characterization

3.1 MOSFET Characterization

Low Temperature device operation is the central focus of this research. For reasons outlined in the introduction, modern silicon MOSFET devices with heavily doped source drain regions have the potential to function at cryogenic temperatures. These devices are the building blocks of integrated circuits, and are an attractive solution for low temperature applications due to the availability of advanced design tools and relatively low design and fabrication costs. This section provides detailed results and analysis of MOSFET operation at low temperature. A MOSFET device is first tested for basic functionality at cryogenic temperatures. After this has been established, a detailed characterization of multiple devices takes place over the entire temperature range. Ultimately, this characterization process has led to the development of a simulator which predicts I-V characteristics at any temperature for a specific device. The explanation of the model is given in Appendix A. In addition to I-V analysis, noise and self-heating effects are also explored in this chapter.

3.1.1 Low Temperature Functionality

The first test conducted was a MOSFET functionality experiment. The measurement equipment used for this test consisted of a Keithley 2700 multimeter and a Lakeshore 340 temperature controller. These instruments are shown below in Figure 12.

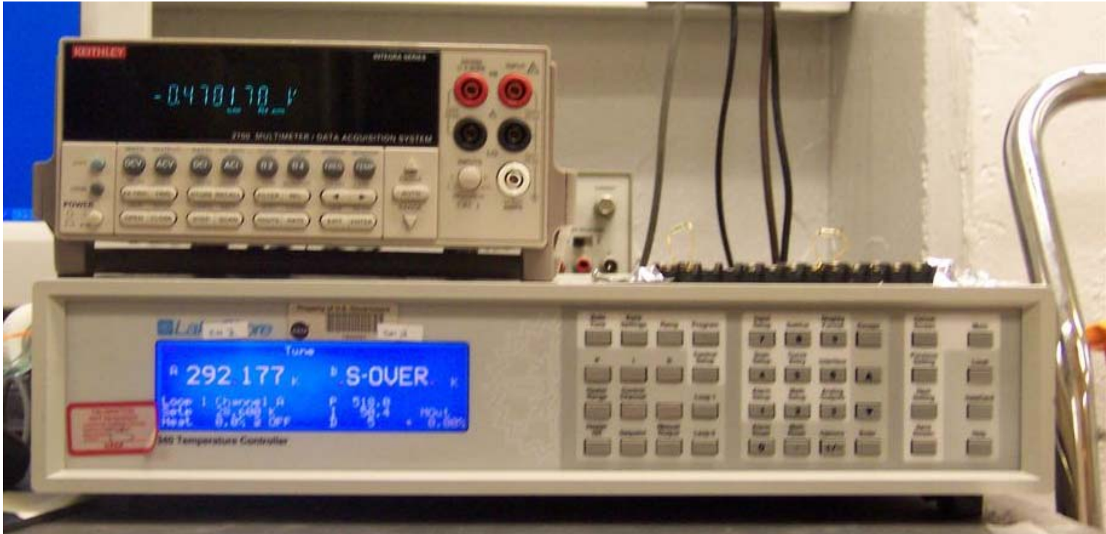


Figure 12: Keithley 2700 (top) and Lakeshore 340 (bottom)

The device used was an NMOSFET fabricated by MOSIS [42] in the AMI 0.6µm process (device A). This transistor had a minimum gate length of 0.6µm and a width/length ratio of 3/1. The goal of this test was to determine if the device was capable of operation at low temperature due to theorized decreases in activation energy brought about by the heavy doping levels of the modern MOSFET. Self-heating was minimized due to the very small size of the device, detailed discussion of self-heating effects given later on in this section.

The transistor was placed in the DIP40 socket, and the source, gate, and drain terminals were wired out of the test Dewar. The device was biased in saturation with the gate terminal connected to 4V, source terminal connected to ground, and drain current connected to 5V via a 1kΩ resistor. The resistor was located outside the Dewar to avoid any changes in current due to the temperature dependence of the resistor. Both the 5V source (V_{DD}) and drain voltage (V_D) were connected to the multimeter. The thermal diode, as always, was connected to the temperature

controller. Both instruments were connected to a LabVIEW equipped PC via the GPIB interface. A schematic of the setup is presented in Figure 13.

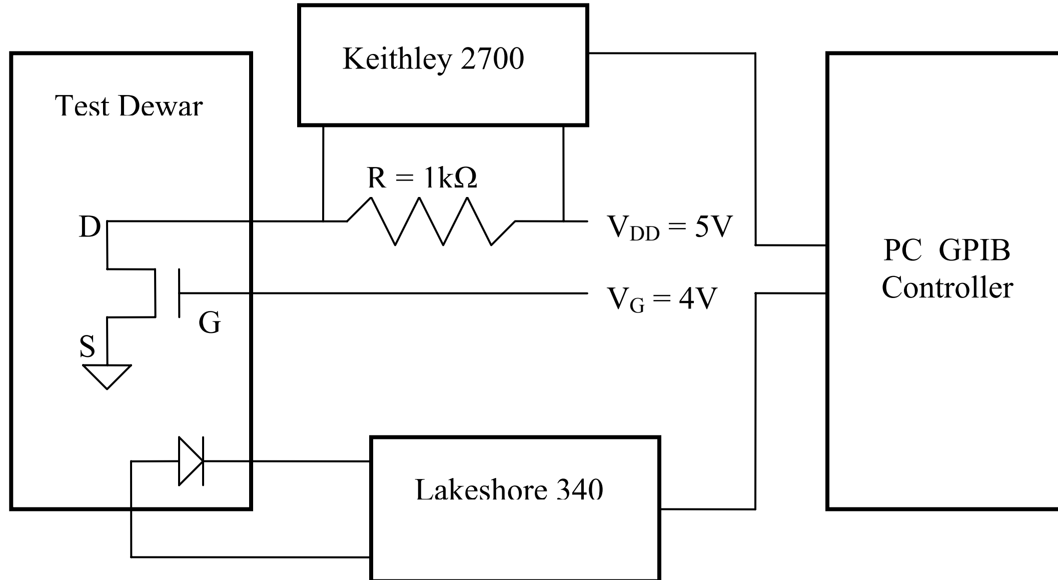


Figure 13: Schematic of MOSFET functionality test setup

Once the configuration shown above had been setup, the test Dewar was cooled to 20K using the procedure outlined in Section 2.3. The system was then allowed to slowly warm up to room temperature over a period of approximately three hours. As the DUT warmed, both the temperature and voltage across the resistor were recorded at 30 second time intervals. The voltage across the resistor was used to calculate drain current. It should be noted that this test was conducted using two different methods to explore possible self heating effects. First, V_{DD} was left on throughout the entire test as data was recorded. The second time around, V_{DD} was switched on immediately before each measurement and switched off immediately after. These two methods produced the same results, and thus it was concluded that

self heating was not affecting the test. The results of this measurement are shown below.

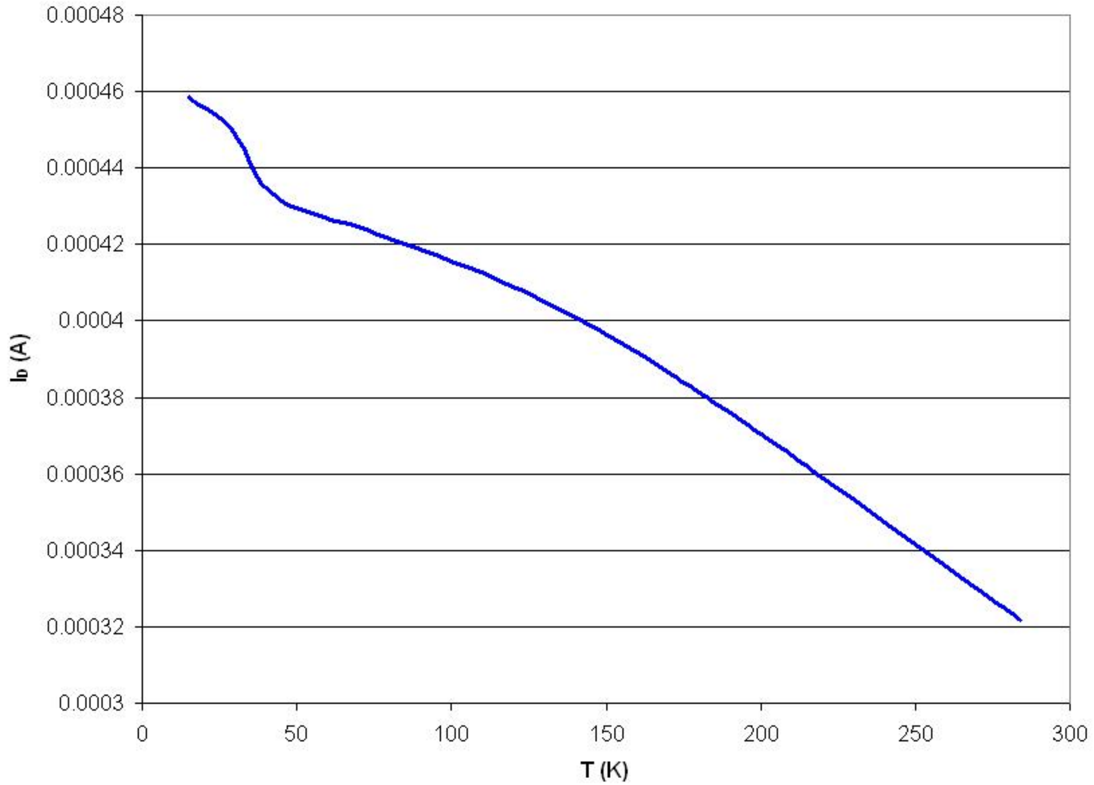


Figure 14: Saturation Current versus Temperature (Device A)

Figure 14 shows that as temperature decreases, current increases over the entire range of the measurement. The sharp roll off that would be expected for a device which is suffering from incomplete ionization was not observed. The plot can be explained in the following manner. Starting at room temperature, the initial increase in current is due to a reduction in the electron-phonon scattering rate. As the temperature continues to decrease, however, the rate of increase in current begins to level off. This is associated with the increase in impurity scattering, which begins to cancel out the electron-phonon scattering effect at lower temperatures. Below 50K,

impurity scattering gives way to a rise in conduction in the impurity band, which leads to a sharp increase in current. This test confirmed that the silicon MOSFET was a viable device at low temperature and allowed for progression to the next device test, described below.

3.1.2 Low Temperature I-V Characteristics

The results of the previous section established MOSFET functionality at cryogenic temperatures and provided insight into the physical processes which dictate MOSFET performance at low temperature. The next step was to further the understanding of these processes and enable the development of a low temperature model. To accomplish this, complete current-voltage characteristics, as opposed to single data points, were needed over the entire temperature the range of interest. This data was obtained by running a series of tests using the HP4156B semiconductor parameter analyzer, shown below in Figure 15.

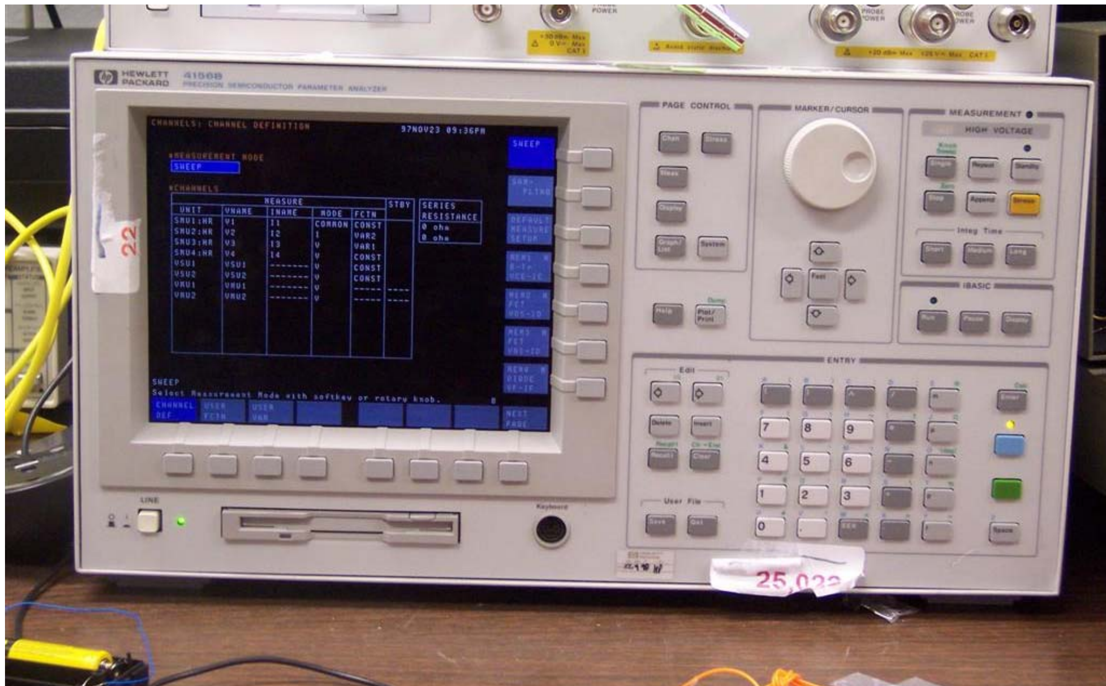


Figure 15: Hewlett Packard 4156B Semiconductor Parameter Analyzer

The parameter analyzer is a very robust instrument which can be configured to test a variety of different devices. It consists of four triaxial source-measurement units (SMUs) which are capable of sourcing voltage and measuring current simultaneously. It also has two coaxial voltage source units (VSU) and voltage measurement units (VMU). The SMUs interface with the transistor terminals via the HP16058 Personality Board shown in Figure 16. The schematic of this test setup is shown in Figure 17.

Figure 16: Hewlett Packard 16058 Personality Board

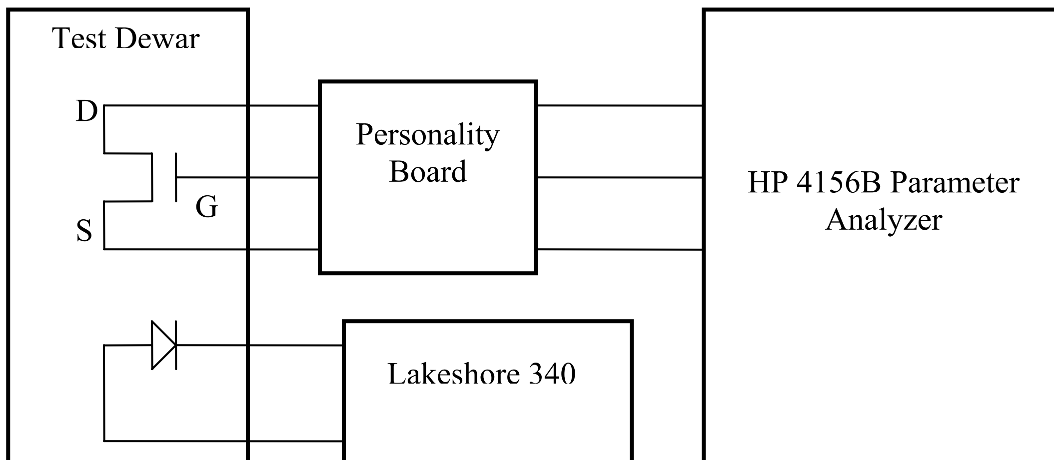


Figure 17: Schematic of MOSFET I-V characteristic test setup

Several MOSFETs were tested in this configuration. The first of which was a second small AMI 0.6μm transistor (device B) fabricated on the same run as device A. Device A was not used for this test because it began to malfunction after being cooled several times for the previous test. This was attributed to the thermal stresses on the package caused by repeatedly cooling the device from 300K down to approximately 20K as well as mechanical stresses associated with picking up the test Dewar to dump out the liquid nitrogen as described in Section 2.3.

Device B (DIP40 package) was mounted in the test Dewar in the same fashion as in Figure 7 and wired out to the personality board as shown in the schematic above. The following measurement settings were used on the 4156B: The source was grounded; the drain voltage was swept from 0-5V at gate voltages of 2, 3, 4, and 5V; the drain SMU was set to measure current. Drain current was then plotted as a function of the drain-source voltage (V_{DS}) for each gate voltage. The test Dewar was then slowly cooled to 20K over a period of approximately three hours. As the device cooled, the parameter analyzer sweep was run at various temperature intervals, producing a complete set of I-V curves at each temperature. The slow cool down rate of the system, combined with a sweep time of just a few seconds for the 4156B, ensured that the entire set of curves was measured within 0.5K of the desired measurement temperature. At colder temperatures, however, where rate of cooling was significantly slower, the temperature accuracy of these measurements increased to 0.1K or better. The results from this test are provided below (Figures 18-21).

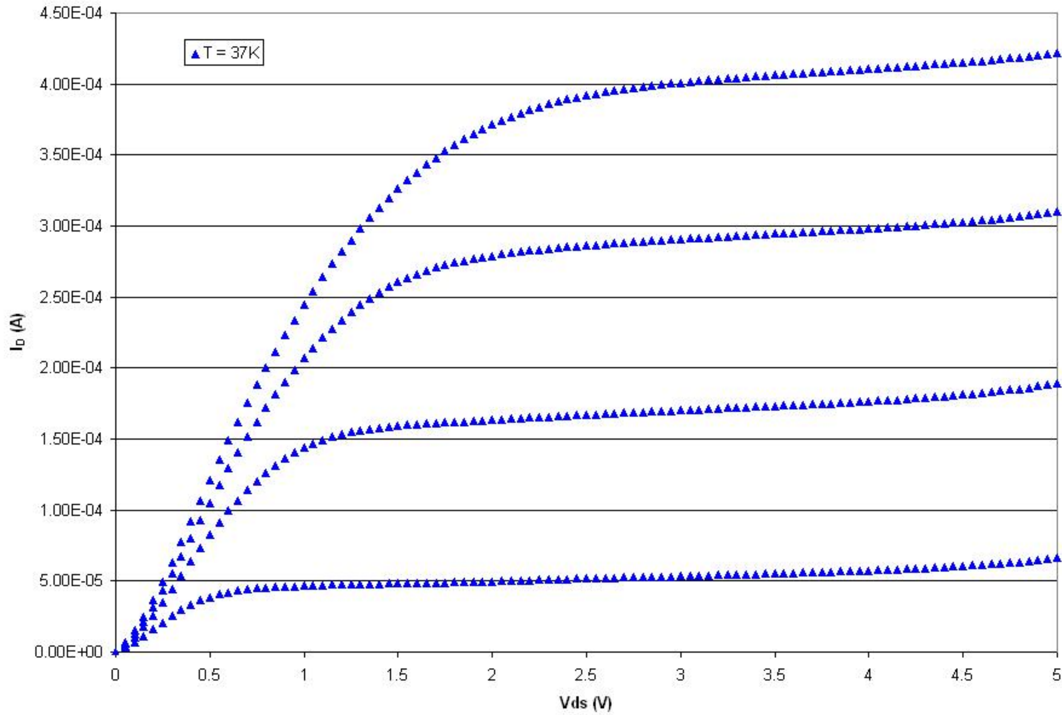


Figure 18: I_D versus V_{DS} family of curves at 37K (Device B)

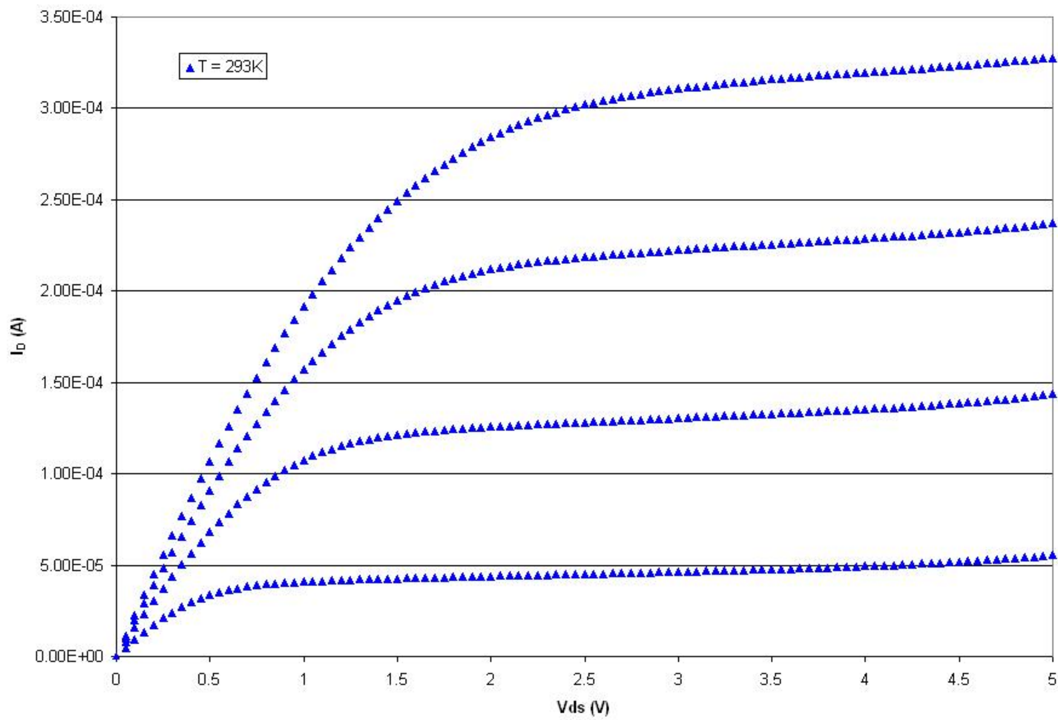


Figure 19: I_D versus V_{DS} family of curves at 293K (Device B)

Figure 18 and Figure 19 show the I_D versus V_{DS} families of curves for 37K and room temperature (293K), respectively. The current shows a similar increase as in the previous functionality test. In addition, Figure 18 shows that the MOSFET is functioning properly and producing a standard family of curves at 37K. Similar curves were obtained at other temperatures throughout the range of interest. For the sake of comparison, several of these curves are plotted together in Figure 20.

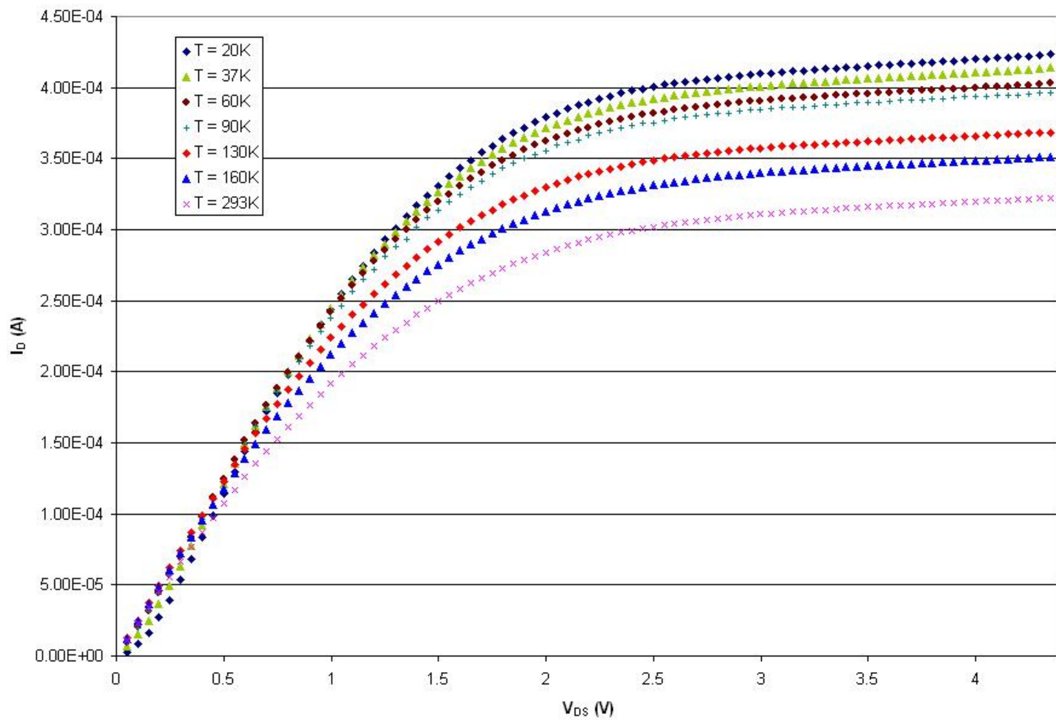


Figure 20: I_D versus V_{DS} Curves for Several Temperatures at V_G = 5V (Device B)

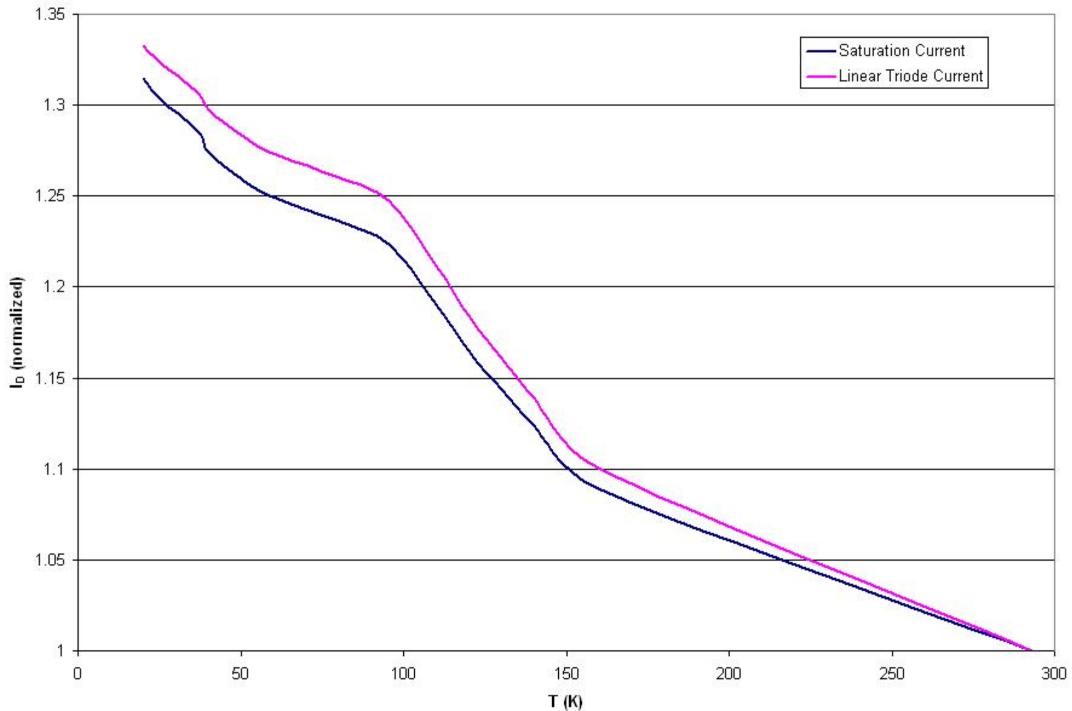


Figure 21: I_D versus T Curves for linear and saturation regions (Device B). Current is normalized to 1 at room temperature to show rate of increase.

Figure 20 shows of I_D versus V_{DS} curves at V_{GS}=5V for several different temperatures (some temperature measurements are omitted for clarity in this figure, but all are incorporated into Figure 21). This plot demonstrates that proper device behavior is occurring over the entire temperature range. The data from Figure 20, as well as the measurements taken at all other temperatures, is used to compare current versus temperature in the saturation (V_{DS}=4.5V, V_G=5V) and linear triode (V_{DS}=2V, V_G=5V) regions of operation (Figure 21). In this figure, the current has been normalized to 1 at 293K by dividing all measured currents by the current value at room temperature (for the same region of operation). This plot shows the percent increase in current from room temperature provides a convenient basis for comparison. It is apparent from Figure 21 that current in the linear region has a very

similar temperature dependence to that in the saturation region, indicating that channel pinch-off does not significantly affect dI_D/dT. This data set was key to this research, and as was discussed in the objectives section of chapter one, it did provide the basis for the development of a low temperature, physics based simulator. The development of the simulator was a collaboration of the characterization work performed here and the modeling efforts of Dr. Akin Akturk (University of Maryland). The development of the model and resulting simulations will be explained in detail in Appendix A.

The second MOSFET tested in this fashion (device C) was fabricated using the same process as devices A and B, but had a width of 200µm and a length of 6µm, making it much larger than the two previous devices. The large width of this transistor caused it to source much larger amounts of current, resulting in significant self-heating. Device C was tested in the same manner as device B to see how a larger device would perform at low temperature. The results of this test, which provided valuable insight into self heating effects, are shown below.

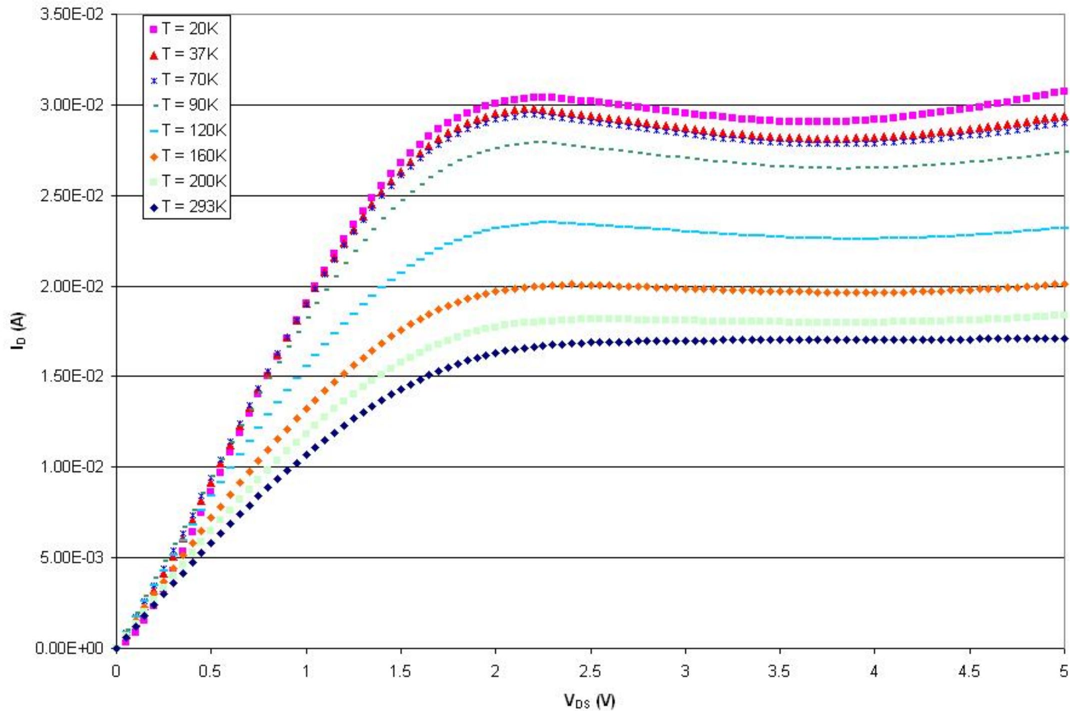


Figure 22: I_D versus V_{DS} curves for several temperatures at V_G = 3V (Device C)

Figure 22 shows the I_D versus V_{DS} family of curves for device C (the large "power" device) at several temperatures. At first glance, it appears as if the device is malfunctioning due to the decrease in current as the transistor enters saturation. Upon closer inspection, however, it becomes apparent this current "dip" is very pronounced at lower temperatures, but gradually disappears as temperature increases up to room temperature. This decrease in current after the device saturates is associated with self heating effects, which can be explained in the following manner. First, it is clear from Figure 14, Figure 21, and Figure 23 (below) that MOSFET current decreases with increasing temperature. In the linear region of operation, there is less current flowing through the device and therefore a smaller amount of heat is generated. In addition, the rate of change dI_D/dV_{DS} is much larger in this region than in saturation. Thus, as V_{DS} is swept through the linear region, the increase in current due to increasing

voltage dominates over any potential decreases in current due to self heating. When the transistor reaches saturation, however, there is a greater current flowing through it, and hence a greater amount of heat is produced. Also, dI_D/dV_{DS} in this region is significantly reduced. As a result, dI_D/dV_{DS} no longer dominates over dI_D/dT (self-heating), and the transient self heating effects shown in Figure 22 are observed. Eventually, device temperature stabilizes and current begins to increase.

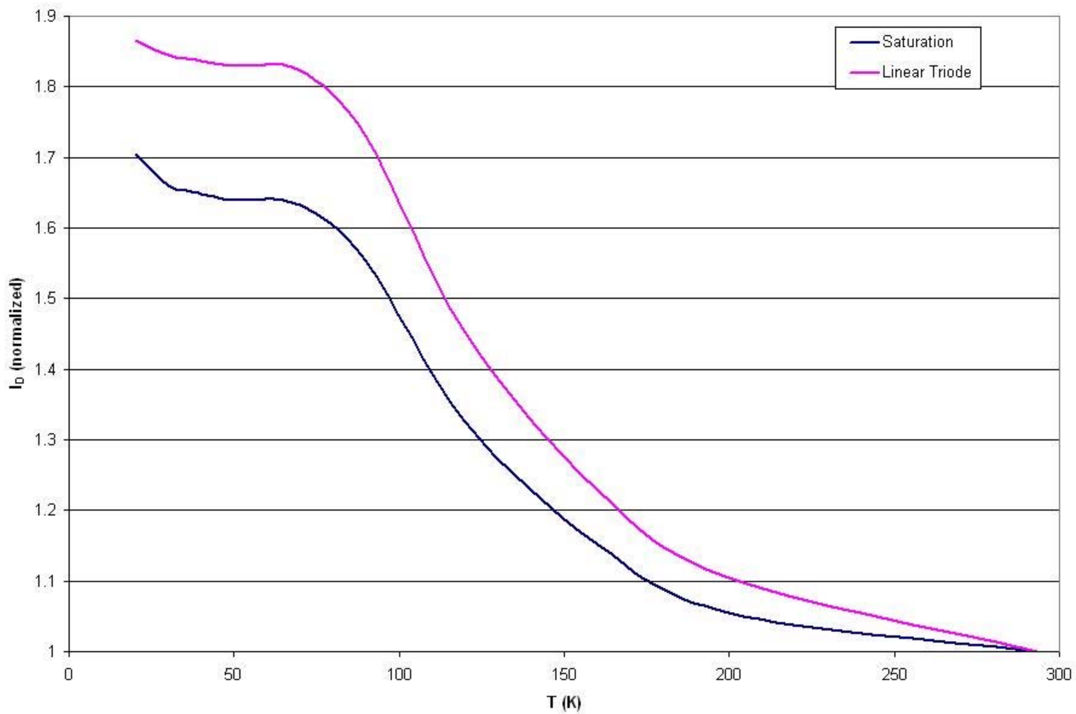


Figure 23: I_D versus T curves for linear and saturation Regions (Device C). Current is normalized to 1 at room temperature to show rate of increase.

Figure 23 shows the current versus temperature curves for device C in the saturation (V_{DS} = 4V, V_G = 3V) and linear triode (V_{DS} = 1.5V, V_G = 3V) regions of operation. Once again, the current has been normalized by dividing all measured currents for a given region of operation by the current value at room temperature for

that region. As with the smaller device, the two curves are very similar, but there is a larger discrepancy between current in the linear triode and saturation regions. The greater increase in linear triode current is attributed to self heating effects, which counteract the increase in saturation current at lower temperatures.

As a final method of analyzing this data, the transient self heating effects shown in Figure 24 were quantified by examining the reduction in voltage after the transistor reached saturation. For each measured temperature, the minimum current in the saturation region was subtracted from the current value at the edge of saturation. The result of this calculation is the "current dip" due to self heating effects. Current reduction as a function of measurement temperature is shown below in Figure 24.

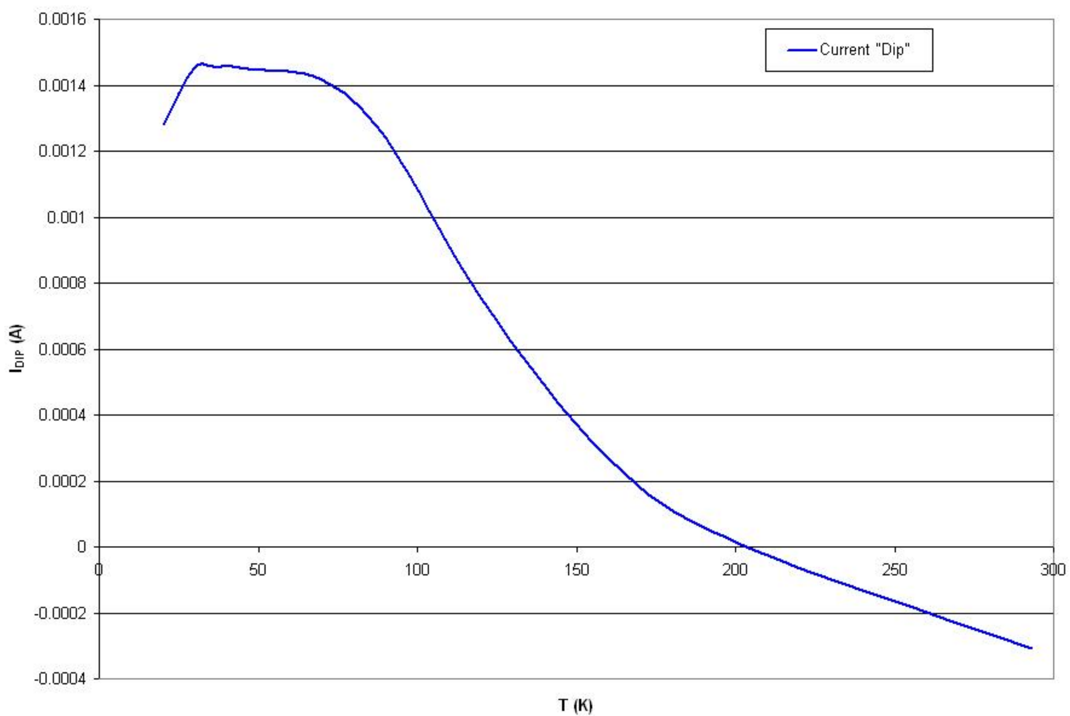


Figure 24: Decrease in current after device saturation (Current Dip) as a function of temperature (Device C)

At temperatures near 300K, the current dip is negative, indicating (as one would expect) that there was no decrease in current due to self heating at these temperatures. As temperature decreases, the current dip becomes positive and increases as well, indicating a rise in self heating. At the lowest measured temperatures (near 20K), the current dip levels off and slightly decreases. This may seem counterintuitive, but it is most likely a reflection of the MOSFET current versus temperature curve. At very low temperatures, self heating moves the curve across the region where increased impurity scatterings have caused the current to level off. Increasing the temperature of the device through this region results in a smaller decrease in current than would occur if the device were heated into the region where current decreases at a faster rate. Thus, although self heating may be greater at lower temperatures, this does not directly translate into greater decreases in current. It is apparent from this analysis that while large transistors can be used at low temperature, self heating effects must be considered to accurately model device performance.

As an additional step in the transistor characterization efforts of this research, the current versus temperature characteristics of devices fabricated in different processes were measured examine temperature dependent current effects in processes other than AMI 0.5µm. Two additional MOSFETs were tested, including a small IBM 0.13µm device with a width/length ratio of 2/1 (device D), and a commercial device fabricated by On Semiconductor (part number MC14007UB, device E). Size information was not available for the commercial device, but it sourced a greater amount of current than device B by a factor of approximately 10 and less current than

device C by a factor of approximately five. Thus, it was reasonable to assume that device E had an intermediate width/length ratio in between that of the very small and very large AMI devices. The results of testing these additional devices, as well as the earlier results from the AMI devices are shown below in Figure 25.

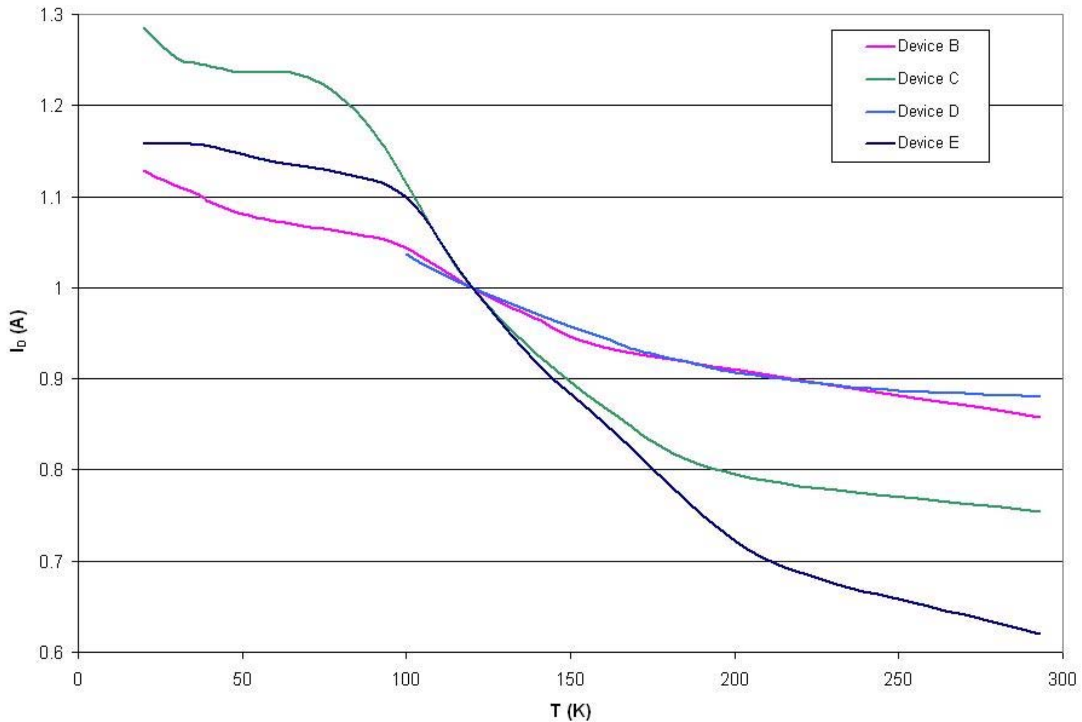


Figure 25: Saturation I_D versus T curves for several MOSFET devices. Current is normalized to 1 at T=120K to emphasize the rate of change at higher and lower temperatures.

In Figure 25, it is clear that the current through each MOSFET device increases with temperature and each curve seems to follow the same general trend, although rates of increase are different. It should be noted that the IBM device suffered ESD failure as a result of necessary disconnections and reconnections during the cool down process (the device was fabricated without any form of ESD protection), leading to the incomplete data set shown. The currents in this plot have

been normalized around 120K to emphasize the rate of change at higher and lower temperatures. Below 120K, the rate of increase in current appears to be positively correlated with transistor size, as evidenced by the curves for devices B, C, and E. At higher temperatures, this trend continues for the AMI devices, and is supported by the data for the small IBM transistor, which closely matches that of the minimum size AMI device. The commercial MOSFET, however, sees a faster drop off in current with increasing temperature than even the large AMI device, indicating that this device is more susceptible to electron-phonon scattering. It can be concluded from this discussion that the rate of change in device current as a function of temperature is both size and process dependent, and thus, different processes must be individually modeled at low temperature. Furthermore, successful designs must also include a detailed thermal model of device performance.

3.2 BJT Characterization

3.2.1 Motivation and Test Procedure

The doping dependent incomplete ionization models discussed in chapter one suggest that high levels of doping decrease activation energies and allow for impurity band conduction, thus improving device performance at low temperature. Silicon bipolar junction transistors are dependent on a relatively lightly doped base region to provide current drive, making them highly susceptible to incomplete ionization effects. This effect reduces the number of available mobile carriers at low temperature, making the BJT a poor choice for cryogenic applications. As a control experiment, a commercial BJT was tested at low temperature. The device used was a commercial silicon NPN transistor, part number P2N2222A. The goal of this

experiment was to characterize silicon BJT performance at low temperature and determine if the lower doping inherent to this device would indeed cause it to freeze-out when cooled, thus supporting the theory of impurity dependent activation energies.

The bipolar junction transistor was tested using a similar procedure as that used for the MOSFET devices. First, the device was soldered to the board inside the test Dewar and the package was affixed to the board using aluminum tape to maximize thermal conduction as shown in Figure 7. The base, emitter, and collector terminals were wired out and connected to the source measurement units of the 4156B via the personality board shown in Figure 16. The parameter analyzer was set to produce a family of I_C versus V_{CE} curves by sweeping V_{CE} from 0-1V at base currents of 10, 20, 30, 40, and 50μA. The test Dewar was then slowly cooled and I-V measurements were recorded in the same manner as with the MOSFET devices.

3.2.2 BJT Test Results

The results of the low temperature BJT test are shown on the following page:

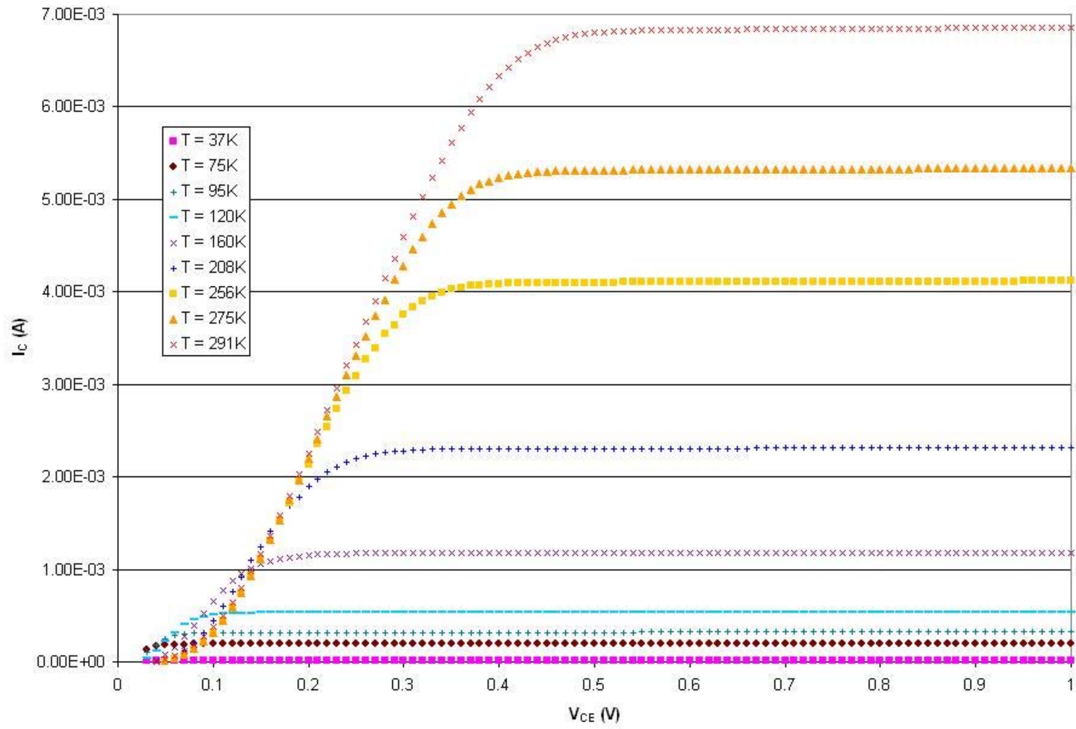


Figure 26: I_C versus V_{CE} Curves for several temperatures at $I_B = 50\mu A$ (BJT)

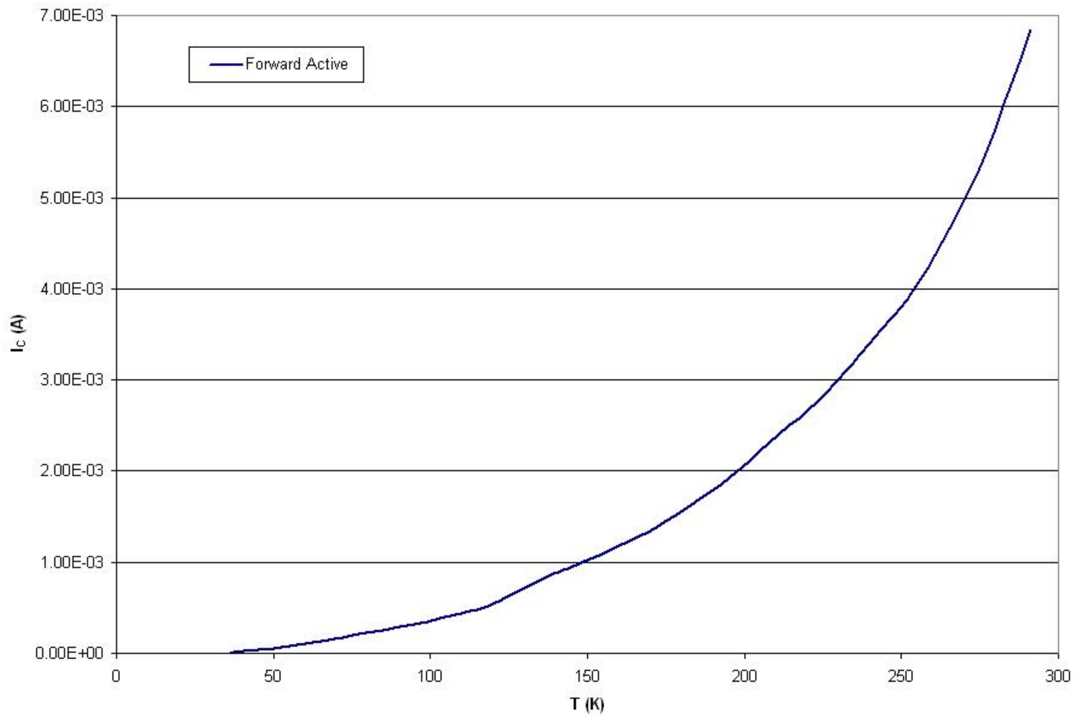


Figure 27: I_C versus T in the forward active region of operation (BJT)

Figure 26 shows I_C versus V_{CE} curves at several different temperatures with base drive current set at 50μA. The I-V curves for this device follow an opposite trend as those for the MOSFET devices. This is accentuated by Figure 27, which plots collector current versus temperature in the forward active region of operation (I_B = 50μA, V_{CE} = 1V). As is clear from both of the figures above, the BJT exhibited very poor low temperature performance. At room temperature, the device has a current gain (β) of approximately 140. A relatively small reduction in temperature to 240K reduced β by a factor of two. At the NASA target temperature of 37K, β was approximately 0.1, rendering the device essentially useless. This test confirmed the theory that standard silicon bipolar junction transistors are not suitable for use at cryogenic temperatures.

It should be pointed out that the component studied, while an industry standard, has been in process for almost 20 years. Base doping is relatively low ($<10^{18}$) and freeze-out is clearly a possibility.

3.3 MOSFET NOISE Analysis

3.3.1 Motivation

Although not the primary focus of this research, it was important to explore noise performance in order to make the claim that overall MOSFET device performance is better at low temperature. If increases in current were accompanied by increases in noise at low temperature, then MOSFETs might not be a viable low temperature solution. Thus, a spectrum analysis was conducted to determine noise performance

3.3.2 Test Setup and Measurement Process

To test transistor noise, a spectrum analyzer was employed along with a low-noise current preamplifier. The spectrum analyzer was used to measure transistor noise as a function of frequency. The current preamplifier was used to source a low-noise drain current through the MOSFET device. These devices are shown below in Figure 28 and Figure 29.

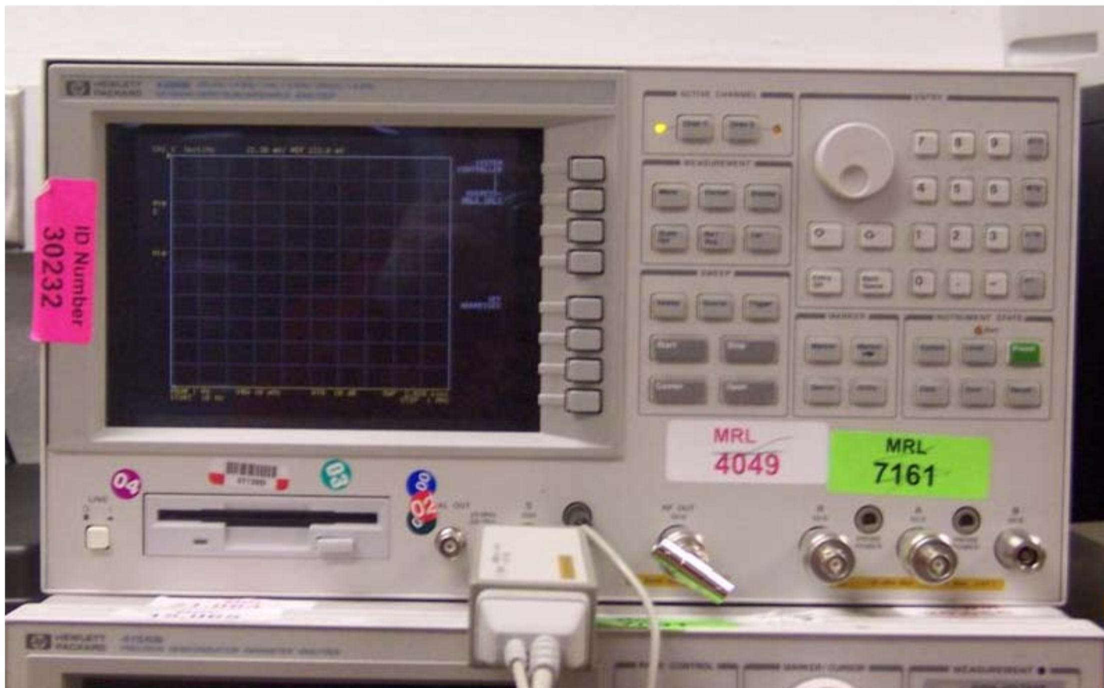


Figure 28: HP4396B Spectrum Analyzer

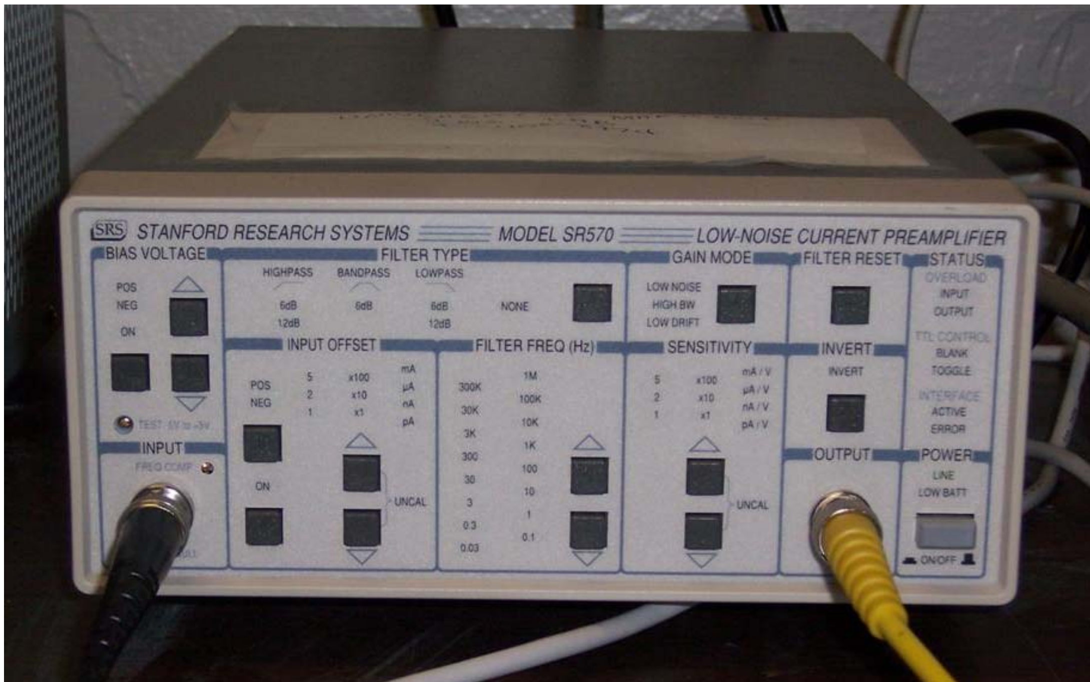


Figure 29: Stanford Research Systems SR570 Low-Noise Current Preamplifier

The spectrum analyzer was connected to the preamplifier using an Agilent 41800A active probe, shown connected to the spectrum analyzer in Figure 28. A buffer was placed in between the two instruments to protect sensitive equipment. The preamplifier was set to source a small amount of current through the drain of device C, and the gate and source terminals were connected to 3V and ground, respectively. The schematic for this test setup is shown below.

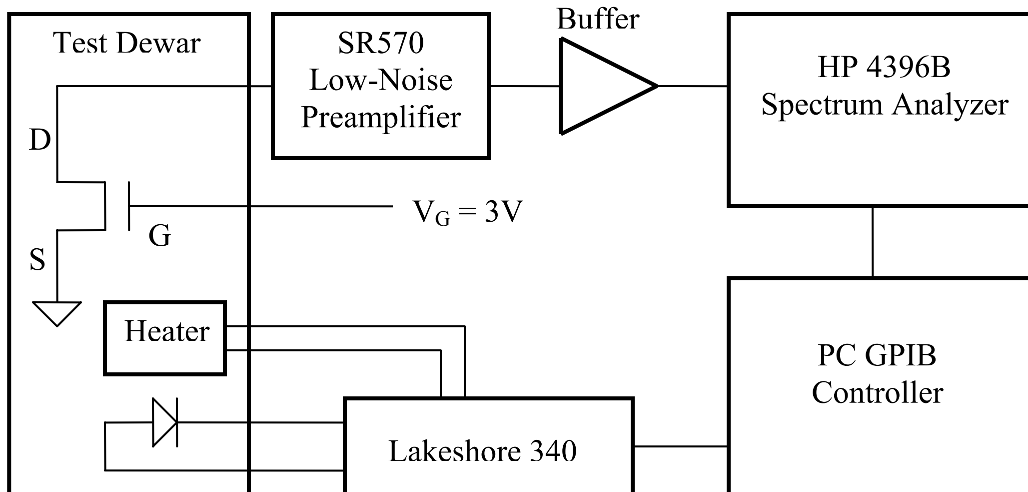


Figure 30: Schematic of MOSFET noise test setup

Since the noise test had a running time of approximately two hours, the Dewar was modified to increase hold time and maintain temperature stability. Small brass standoffs were used instead of copper standoffs as described in chapter two and a heater was mounted on the test board. The heater used was a 5W, 40Ω, wire wound resistor, housed in aluminum casing with a flat base to maximize heat transfer. The two terminals of the resistor were connected to the temperature controller as shown in Figure 30. In Figure 31, the heater is the gold-colored item mounted to the bottom-middle section of the board. Note that this picture is just to show how the heater was mounted to the board; the two terminals of the resistor had not yet been wired out of the test Dewar, nor had the brass standoffs been installed.

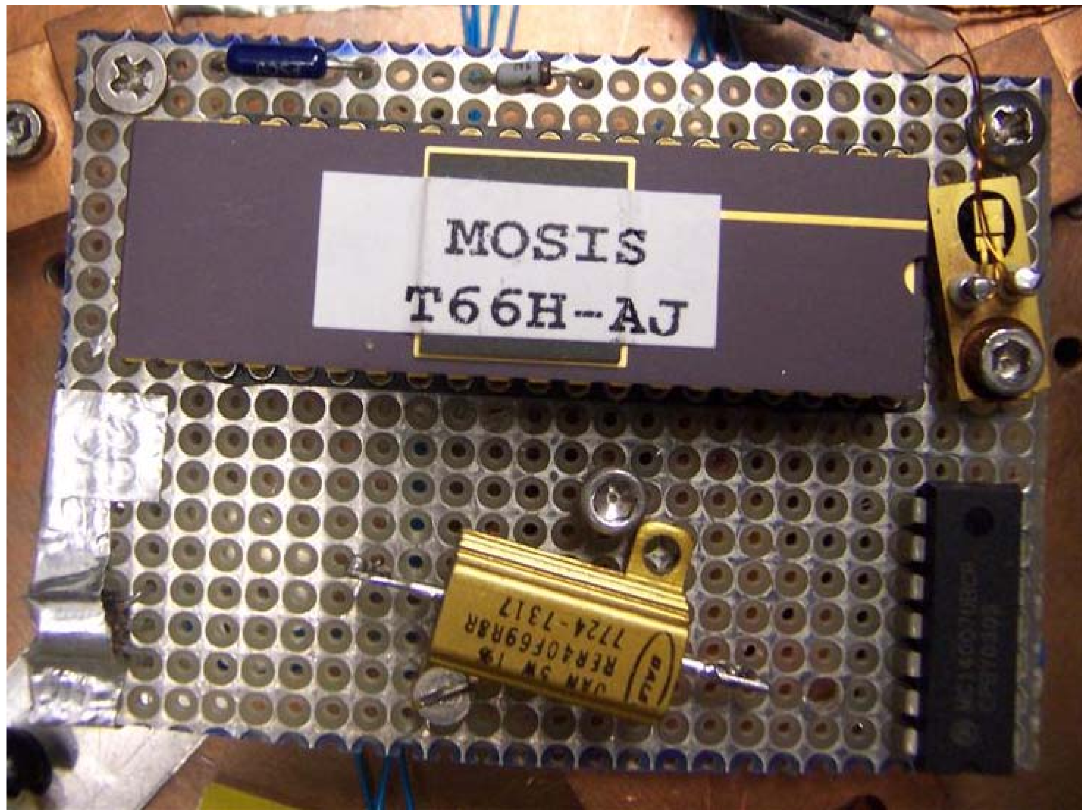


Figure 31: Resistive heater mounted on test board (bottom-middle)

Once all components were properly installed, the test Dewar was cooled to using the technique described in chapter two. Using the GPIB controller, the Lakeshore 340 was programmed with the heater resistance and power rating, as well as the desired system temperature. This information, along with the temperature read by the thermal diode, was used by the instrument to program a proportional-integral-derivative (PID) feedback control, which stabilizes the DUT at the desired temperature. When the temperature reached 20K, the heater switched on and stabilized the system. The drain current and gate bias were then turned on and a frequency sweep from 10Hz to 100kHz was conducted using the spectrum analyzer. As a basis for comparison, the same test was also run at room temperature. Since a low noise environment was unavailable for this test, the results were fed through a

software filter to remove 60Hz harmonics. The software filter functioned by first dividing all measured frequencies by 60 and then filtering out the data point closest to each integer value. Due to the relatively few number of data points taken per decade, this filter could only be applied to frequencies less than 1kHz. Application at higher frequencies would have resulted in the filtering of arbitrary data points. This is evidenced by the results shown in Figure 32, where the data is much cleaner at low frequency.

3.3.3 Results

The results of the noise test are shown below. At low frequencies, where the 60Hz harmonics have been filtered out, it is clear that flicker (1/f) noise is significantly reduced at low temperature. Specifically, at 10Hz, the noise figure decreases by a factor of 200. At higher frequencies, for reasons explained above, the data is contaminated by outside noise sources and cannot be filtered. Nonetheless, it appears that the noise floor at high frequencies is lower at for the 20K measurement than for the room temperature measurement. Despite the non-ideal conditions for this experiment, it can be concluded from the data that low frequency (1/f) noise performance is significantly better at 20K than at room temperature. At higher frequencies, noise performance at low temperature seems to improve, and at the very least is no worse than room temperature noise.

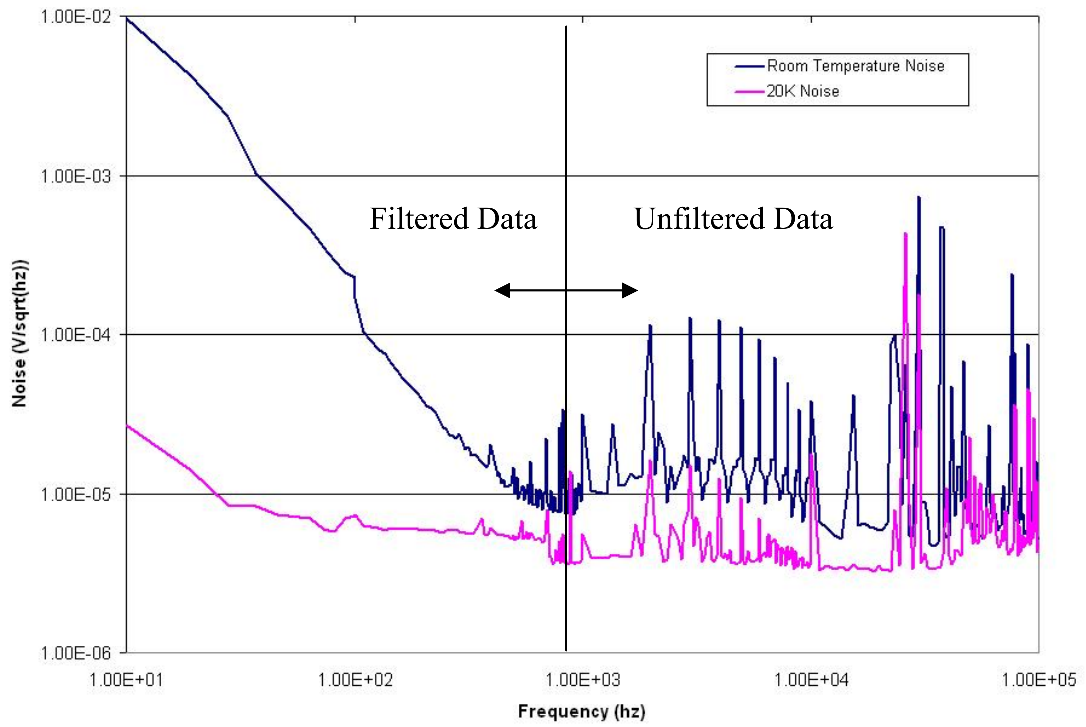


Figure 32: MOSFET Noise versus Frequency at room temperature and 20K

CHAPTER 4: Cryogenic Integrated Circuits

4.1 Zener Diode Voltage Reference

In addition to testing individual transistor components, the effects of cryogenic cooling on two electronic circuits were also explored. The first circuit tested was a Zener diode configured as a voltage reference circuit. As was discussed in chapter one, scientists at the NASA Goddard Space Flight Center have been working to develop a voltage reference circuit that will function at 37K. Such a circuit is necessary to provide power to the detector instruments which will be used on the upcoming James Webb Space Telescope. Research at NASA has focused primarily on the use of silicon-germanium (SiGe) based technology to meet this specification. This research aims to present a cheaper alternative to meet this specification using an inexpensive, readily available, commercial off the shelf (COTS) part, namely, a zener diode.

4.1.1 Operation

Under forward biased conditions, zener diodes operate in the same fashion as standard diodes, that is to say that once the junction built-in potential is reached, the device acts (ideally) as a short circuit. Under reverse bias conditions, however, operation is different. Standard p-n diodes do not conduct under reverse bias conditions until the negative applied voltage is made large enough to cause avalanche breakdown. This effect, also known as impact ionization, is caused by energized electrons slamming into the silicon lattice, which results in additional free electrons that lead to a domino effect. Zener diodes also enter a breakdown region under reverse bias, but breakdown is due to a different mechanism known as the tunneling effect. If the depletion region is made to be very narrow, and a carrier has sufficient

energy due to an applied reverse voltage, it will tunnel through the potential barrier and allow conduction to occur. By using heavily doped semiconductor materials to control the width of the depletion region, the zener breakdown voltage can be set at a desired value which is generally much less than that of a standard p-n diode. The I-V characteristic for a zener diode is shown below in Figure 33. Heavy doping guarantees impurity band formation and facilitates low-temperature operation.

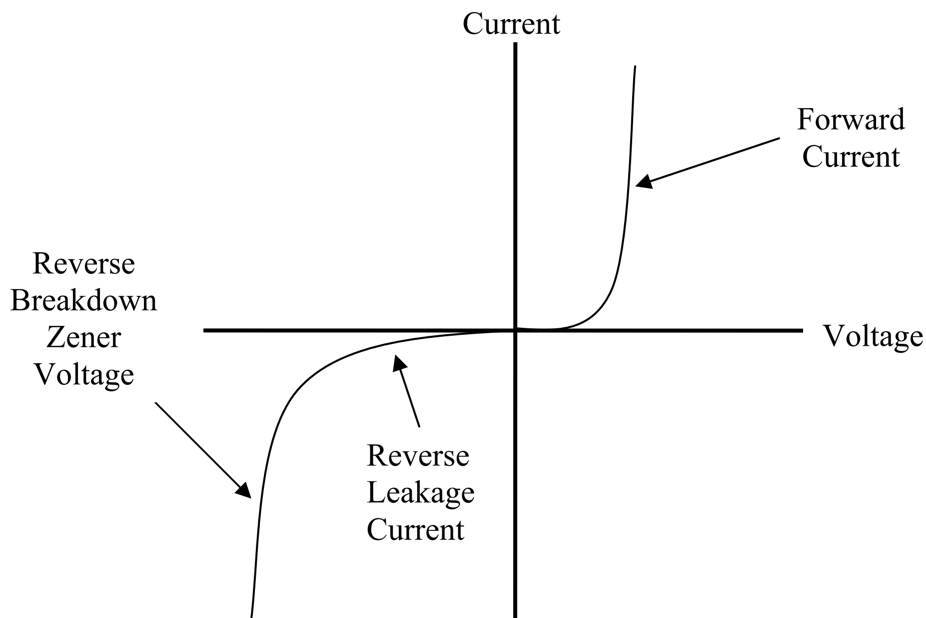


Figure 33: Zener diode I-V characteristic

As can be seen in Figure 33, when the zener diode enters the zener tunneling region, large changes in current produce very little change in voltage. It is this property that makes the zener diode device an effective voltage reference circuit. In addition, the tunneling effect described above is not susceptible to freeze out, since carriers need not be ionized to tunnel through the potential barrier. This makes the zener diode an attractive choice for low temperature applications.

4.1.2 Test Setup

A 5.1V zener diode (1N751) was used for this experiment. It was soldered on to the test board with the package in direct thermal contact with the board. A 10kΩ resistor was placed in series with the diode as a current limiter. The parameter analyzer was used to reverse bias the diode and measure the regulated zener voltage. A schematic of the test setup is shown below in Figure 34.

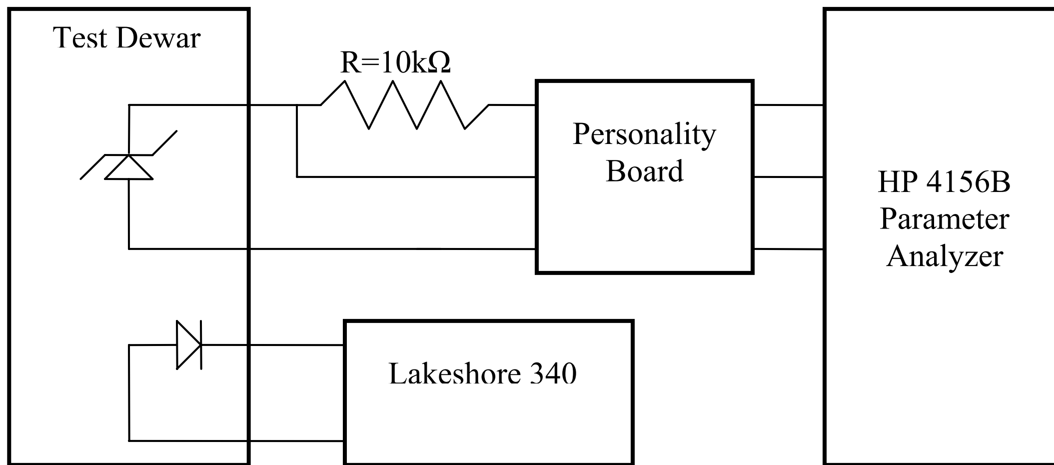


Figure 34: Zener diode voltage reference test setup

The test Dewar was cooled using the process described in chapter two. As temperature decreased, data was collected at various intervals. Measurements were performed by sweeping the reverse bias voltage from 0-15V and simultaneously measuring the voltage across the diode, producing a series of curves like the one shown in Figure 35. A stability test was conducted in addition to the aforementioned series of measurements. This was done by using the heater to maintain a test board temperature of 37K, and then logging data at one minute intervals for an hour.

4.1.3 Results

Figure 35 below shows the results of the first test at 37K. Initially, voltage increases rapidly as the diode moves through the reverse leakage region. Next tunneling breakdown begins to occur and the reference voltage stabilizes near the zener voltage of 5V. Note that the large voltage was used to compensate for the large current limiting resistor. The resistor or zener diode could easily be changed to accommodate smaller input or output voltages as desired.

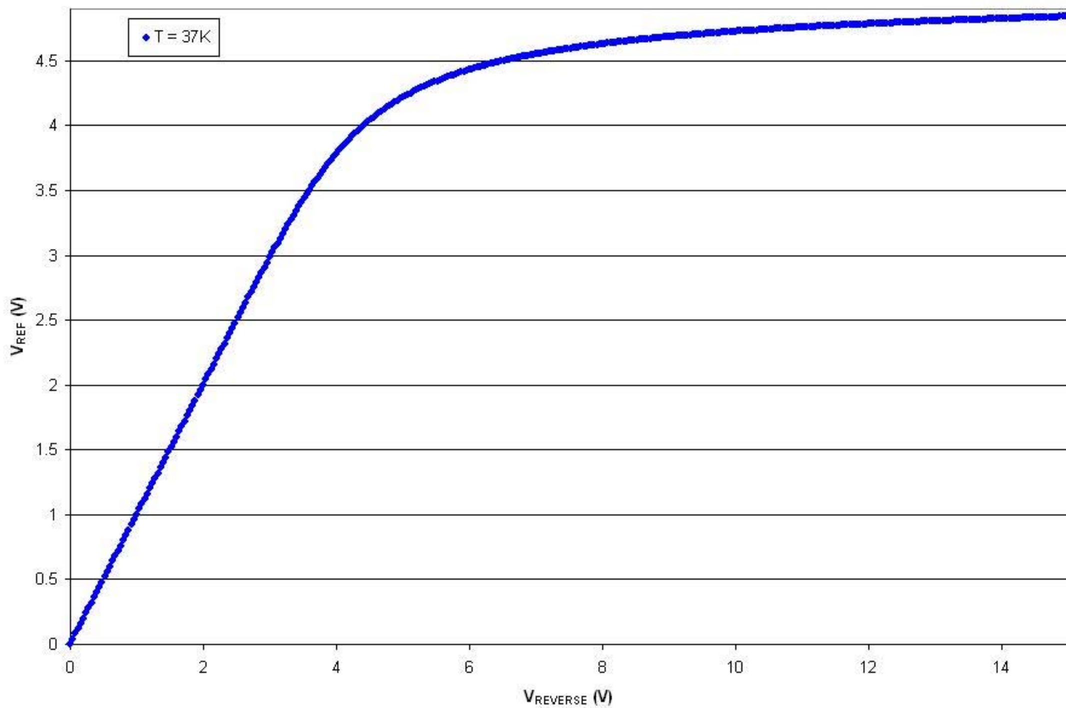


Figure 35: Zener diode reference voltage versus input voltage at T=37K

The plot above shows reference voltage as a function of input voltage, demonstrating that the zener functions as a voltage reference at 37K. The next step was to examine reference voltage as a function of temperature. As was mentioned both in chapter one and in the introduction to this section, the zener diode was tested

as an alternative to a silicon germanium based voltage reference circuit. To facilitate a comparison between the two, the normalized reference voltage of each was plotted as a function of temperature. This is shown below in Figure 36.

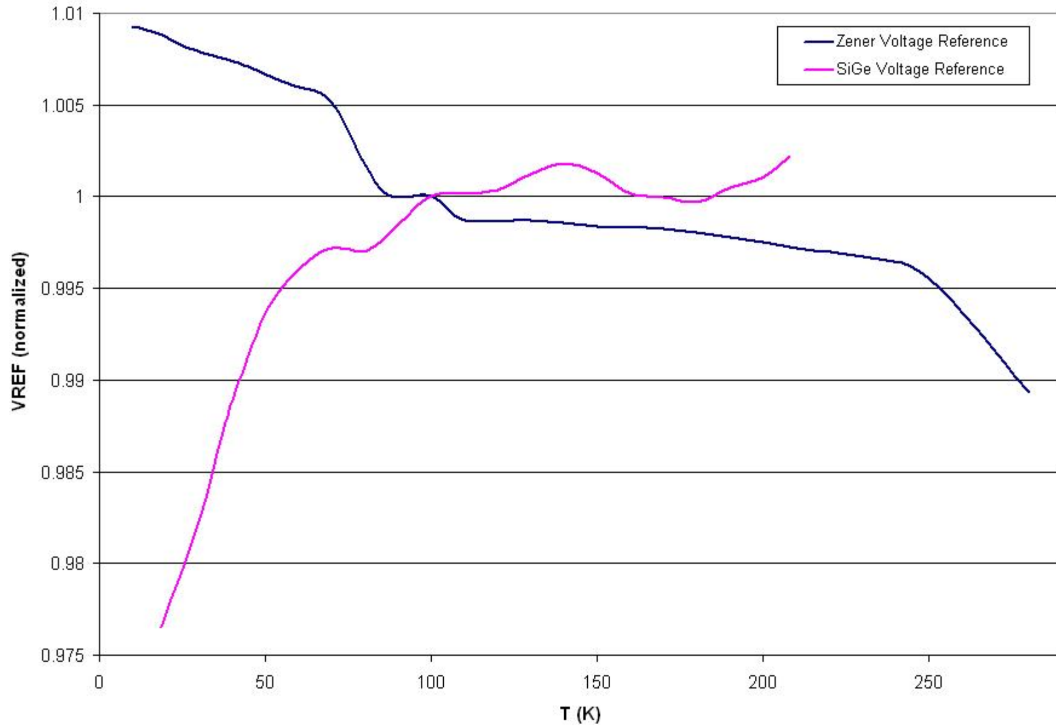


Figure 36: Reference Voltage versus Temperature for zener diode and SiGe voltage references (normalized to one at T=100K)

In the plot above, output voltage has been normalized to one at 100K to show the general V_{REF} versus temperature trend for both references. At first glance, it appears as if the zener reference is significantly outperforming its SiGe counterpart in the region of interest near 37K. The zener diode appears to have a considerably lower temperature dependence in this region, but is important to note that the zener plot has been normalized by a factor five (the zener voltage), whereas the SiGe plot has been

scaled by a factor of only 1.2. Hence, this plot cannot be used to compare rate of change.

To properly analyze dV_{REF} / dT near 37K, the actual (non-scaled) values of V_{REF} were plotted for the region around 37K in which they are very approximately linear. As evidenced by R^2 values better than 0.99, this was a very good approximation for the regions plotted (13-57K for zener, 18-50K for SiGe). A linear fit was then applied to both data sets, the slope of which provided the value of dV_{REF} / dT near 37K. This is shown below in Figure 37 (zener) and Figure 38 (SiGe).

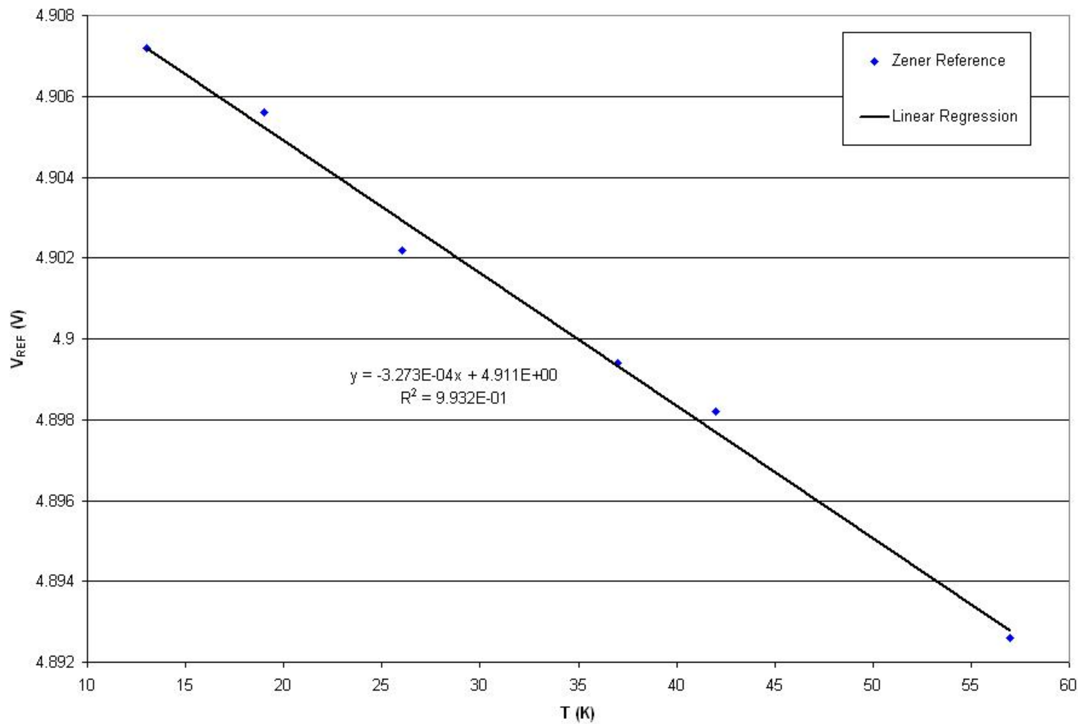


Figure 37: Zener diode reference voltage versus temperature near T=37K

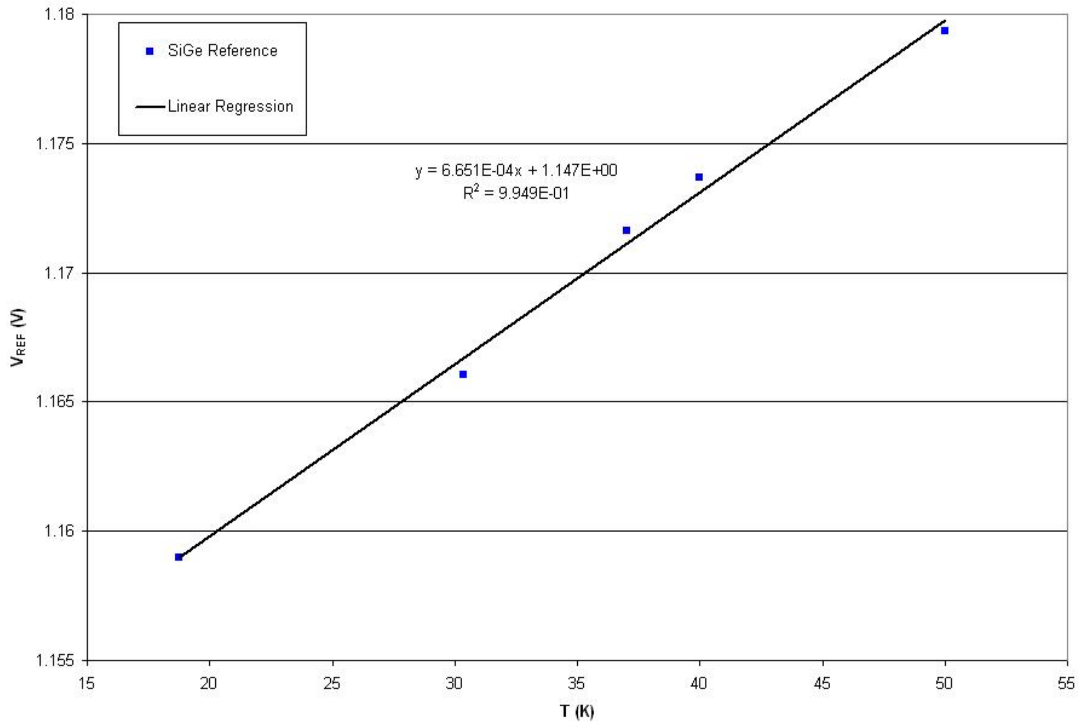


Figure 38: SiGe reference voltage versus temperature near T=37K

As can be seen in the plots above, the zener diode reference has a slope of 0.327mV/K. Compared to the SiGe reference, which exhibits a slope of 0.665mV/K, the zener resulted in an improvement by more than a factor of two. This experiment showed that the temperature dependent voltage reference characteristics of the zener diode were superior to those of the silicon germanium based reference.

As a final measure of voltage reference performance, the stability of the zener diode was examined at the target voltage of 37K. To conduct this measurement, the test Dewar was first cooled with liquid helium and the heater and temperature controller described in Section 3.1 were used to stabilize the system at the desired temperature. Once the equilibrium had been reached, the diode reverse bias voltage was switched on to 15V and output voltage was measured at one minute intervals for an hour. This data is shown below in Figure 39. As a basis for comparison, a similar

hour long stability test for the SiGe voltage reference which was conducted at an earlier date is shown in Figure 40.

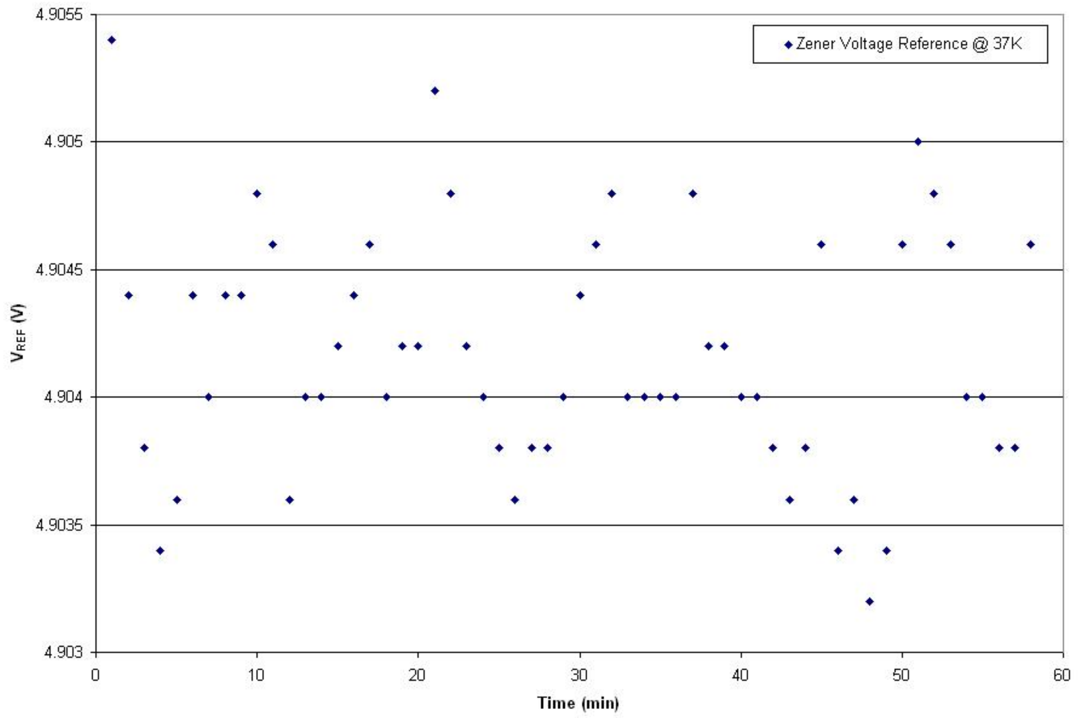


Figure 39: Zener diode voltage reference stability at T=37K

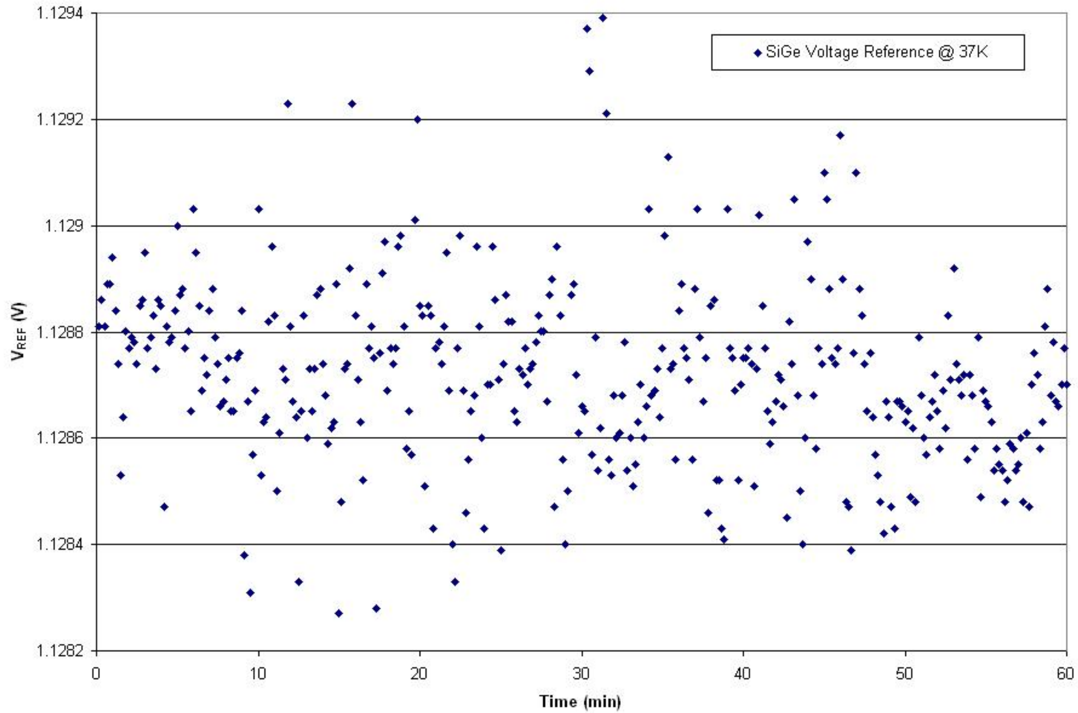


Figure 40: SiGe voltage reference stability at T=37K

Figure 39 and Figure 40 show variations in zener and SiGe reference voltages of 2.2mV and 1.2mV, respectively. The SiGe reference appears, at first, to demonstrate a better stability figure, but it should be noted that the SiGe was measured in a larger test Dewar with a longer hold time and better thermal isolation from the cold plate to the DUT. This allowed for temperature stability of $37 \pm 0.05\,\mathrm{K}$, as opposed to $37 \pm 1.2\mathrm{K}$ for the smaller Dewar in which the zener diode was tested. Based on the dV_{REF}/dT value of 0.327mV/Kdetermined above, temperature fluctuations are potentially responsible for as much as 0.78mV of variation in zener output voltage. By contrast, temperature fluctuations can account for only 65μV of variation in the SiGe reference, subtracting out these temperature variations results in a zener voltage swing of 1.42mV and a SiGe voltage swing of 1.13mV. Thus, the two references exhibit comparable noise-induced voltage fluctuations. For the given

application, it is clear that the silicon germanium voltage reference circuit performs on par with the more economical zener diode reference.

4.2 Ring Oscillator

The second circuit tested at low temperature was an integrated ring oscillator circuit. The goal of this test was see if improvements in device performance would translate into improved circuit performance. A ring oscillator was selected for this experiment due to the fact that oscillation frequency is a direct function of the device current. Also, it consists exclusively of MOSFET devices, meaning that freeze-out of bipolar devices would not be an issue

4.2.1 Operation

A ring oscillator consists of a chain of inverters, with the output of the last inverter fed back into the input of the first. The number of inverters in the chain must be odd, otherwise the output of the last inverter will be the same as the input to the first inverter, in which case oscillation will not occur. The expression for the frequency of oscillation is given in (4).

$$f_{osc} = \frac{I_D}{NC_{TOT}V_{DD}} \quad \textbf{(4)}$$

In the expression above, f_{osc} is the frequency of oscillation, I_D is the MOSFET drain current flowing through the individual inverters, N is the number of inverter stages, C_{TOT} is the total intrinsic capacitance of the inverter, and V_{DD} is the voltage difference between the positive and negative rails. As can be seen from this equation, the frequency of oscillation is a direct function of device current. Therefore, decreases in temperature should lead to increases in oscillation frequency.

4.2.2 Test Setup

The chip used for this experiment was a 31-stage ring oscillator fabricated in the AMI 1.6μm process. All transistors used in the design were of minimum length. The inverter stages each consisted of an NMOS transistor and PMOS transistor with width/length ratios of 2.5/1 and 7.5/1, respectively. A four-stage output buffer was also included in the design, which consisted of four inverters with progressively increasing sizes linked in the same manner as in the oscillator. The first buffer-inverter was the same size as those used for the oscillator, the following three increased in size by factors of 4, 19, and 50, respectively. The schematic of this circuit is shown below in Figure 41.

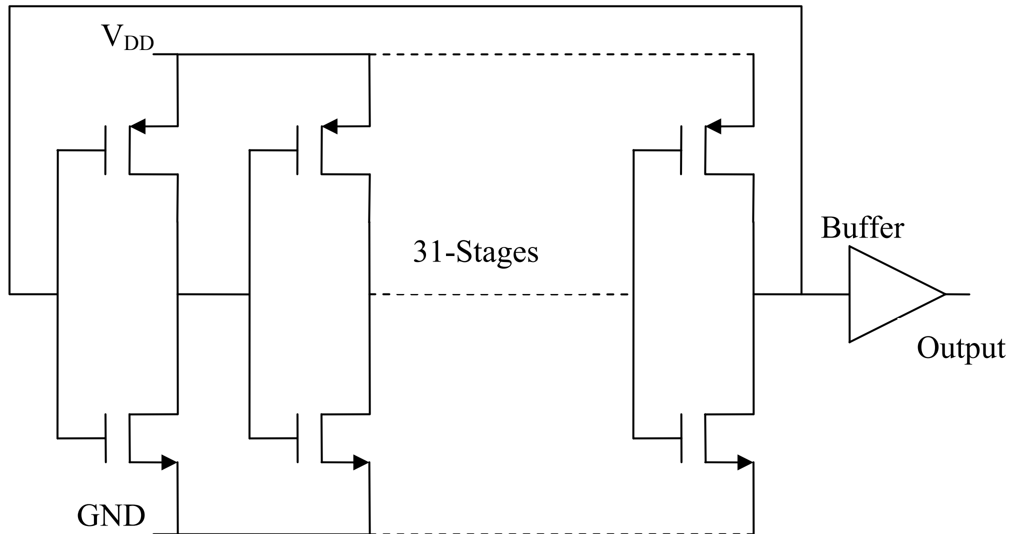


Figure 41: Schematic of Ring Oscillator Circuit

The ring oscillator was tested using a low rail voltage of 2V to minimize self heating. To measure oscillation frequency, the oscillator output was connected to a Tektronix TDS 744A oscilloscope, shown below in Figure 42.

Figure 42: Tektronix TDS 744A Oscilloscope

To begin this experiment, the test Dewar was slowly cooled using the process described in chapter two. As oscillator temperature decreased, measurements were taken by switching on the power supply and then immediately pausing the oscilloscope waveform to minimize self heating effects on the measurement. The oscillation frequency of the waveform was then recorded. Although the aforementioned steps were taken to reduce self heating, it was still clearly present as evidenced by increasing temperature on the thermal diode readout as soon as the power was switched on. The recorded frequency data from each measurement was used to plot oscillator frequency as a function of temperature.

4.2.3 Results

The resulting frequency versus temperature plot is shown below in Figure 43. As expected, frequency increased with decreasing temperature. The temperature response was similar to that of the individual MOSFET devices tested in Chapter 3,

but the region of large dI_D/dT increase that was generally observed in the 90-150K range has been shifted to the left. This is associated with self heating effects. Also, at the lowest temperature, there is a slight decrease in frequency which is likely due to human error. Since self heating occurs very quickly at extremely low temperatures, measuring the oscilloscope waveform after the power supply has been on a fraction of a second longer will result in a decreased oscillation frequency. For the most part, however, this experiment demonstrated the expected results and corroborated the measurements taken in Chapter 3.

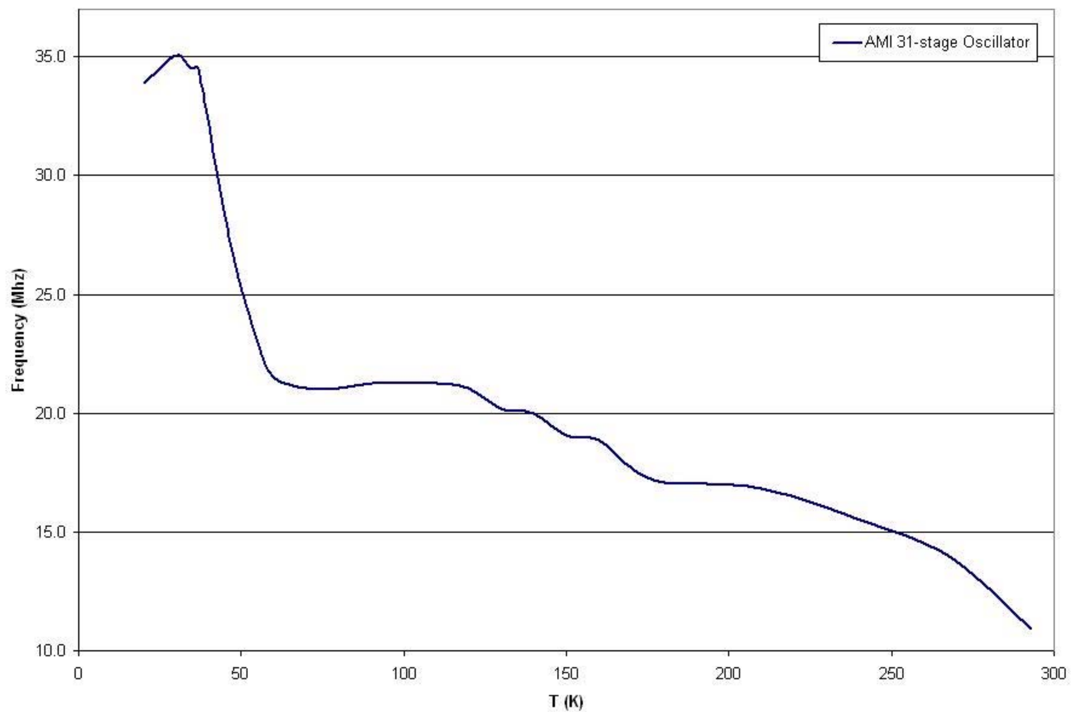


Figure 43: Frequency versus Temperature (Oscillator B)

CHAPTER 5: Conclusions and Future Work

The research presented in this thesis focused on the design of a low temperature test environment, followed by a subsequent testing and characterization effort involving several devices and circuits at low temperature. The primary goal of this work was to explore the temperature dependent operation of silicon MOSFET devices. The functionality of these devices was established at temperatures down to 20K, and significant improvements in current and flicker noise were demonstrated at cryogenic temperatures. Transient self heating effects were also observed and characterized in a very large MOSFET. In contrast to the improved performance of the MOSFETs, an older designed BJT, with a relatively lightly doped base, was shown to suffer from incomplete ionization effects. The MOSFET data was combined with a temperature dependent mobility model and a dopant dependent activation energy model to produce a simulator which predicts MOSFET operation accurately over the full measured temperature range (Appendix A). A secondary goal was the temperature dependent characterization of a tunneling structure. A zener diode was configured as a voltage reference circuit, and measured performance was comparable to that of a silicon germanium voltage reference, with the zener diode exhibiting better temperature dependent characteristics. Finally, a ring oscillator circuit was tested at low temperature to show that the oscillation frequency, which is proportional to device current, increased in a manner similar to the current increases exhibited by individual MOSFETs.

5.1 Contributions

Ultimately, this research advances the understanding of silicon devices and impurity related effects at very low temperatures. The main scientific and technical contributions of this research are as follows:

1. MOSFET functionality has been established over the entire temperature range from room temperature to 20K. Improvements in device performance at low temperature due to impurity band concentration and decreased ionization energy have been demonstrated. These improvements are shown to translate into improved ring oscillator performance.

2. MOSFET I-V characteristics, including variations in gate voltage and drain-source voltage, have been characterized from room temperature to 20K, allowing for the development of a physics based simulator that accurately predicts device performance over this range.

3. A zener diode voltage reference has been characterized at low temperature, demonstrating better voltage versus temperature performance than a silicon germanium voltage reference circuit at temperatures near 37K. The tunneling method of carrier transport through the device is shown to be insensitive to incomplete ionization effects.

4. A comprehensive guide to low temperature testing is provided, which includes information on test Dewar design, thermal considerations, board setup, equipment, and the cooling process.

5.1.1 MOSFET Low Temperature Functionality

The functionality of MOSFET devices at low temperature was investigated using a liquid helium test Dewar. A small feature size transistor was used to minimize self heating. The device was mounted on a board inside the test Dewar and wired out to a power supply and multimeter. A temperature sensing diode was also mounted on the board adjacent to the transistor package. As the Dewar was cooled, both temperature and drain current measurements were recorded using a LabVIEW based PC instrument controller. The results showed that the device functioned over the entire measured range from room temperature to 20K. At lower temperatures, the sharp roll off that would be expected for a case where incomplete ionization occurs was not observed. Initially, current increased due to an increase in the electron-phonon scattering rate. At lower temperatures, the rate of increase began to level off due to impurity scattering, but then increased once again due to conduction in the impurity band. This test showed that freeze out was not significantly affecting the low temperature operation of the device, and that mobility increased as a function of decreasing temperature. Opposite low temperature effects were observed with bipolar junction transistor, which has a much lower base doping concentration than the source/drain regions of the MOSFET.

As a second functionality metric, MOSFET noise was investigated at low temperature. The device was cooled and stabilized at 20K using a resistive heater. A turn-on voltage was applied to the gate and low noise current preamplifier was used to source a small amount of drain current. A spectrum analyzer was then used to perform a noise analysis, and the low frequency data was fed through a software filter to remove 60Hz harmonics. The same test was run at room temperature as a basis for

comparison. The results of this test showed that maximum low frequency (1/f) noise was reduced by a factor of 200 when temperature was reduced from 293K to 20K. High frequency data was less conclusive, but there appeared to be a reduction in noise in this region as well.

5.1.2 MOSFET I-V Characteristics

To further explore MOSFET operation at low temperature and provide a more complete data set for temperature dependent device modeling and simulation, a series I-V curves were measured at various temperatures over the entire range of interest. A semiconductor parameter analyzer was used to produce families of curves by sweeping I_D versus V_{DS} at different gate bias voltages. The results showed the expected MOSFET family of curves at all measured temperatures, indicating that the device continued to function properly as temperature decreased to 20K. In addition, it was shown that MOSFET current versus temperature characteristics were very similar in the saturation and linear regions of operation, indicating that channel pinch-off did affect the temperature dependent current.

This test was conducted on multiple transistors. In each case, the current versus temperature characteristic followed the same general trend, indicating that the physical mechanisms dictating current flow were the same. In general, the current through larger devices seemed to increase at a faster rate for decreasing temperature than for smaller devices, but this rate is process dependent as well. Data from a very large device showed transient self heating effects that led to reductions in current once the device reached saturation. At higher temperatures near room temperature, there was no reduction in current as a result of minimal self heating. Decreasing temperature

resulted in an expected increase in the current “dip” after device saturation, indicating greater self heating at lower temperatures. At the lowest temperature of 20K, the current “dip” decreased slightly. This was associated with the flat region of the current versus temperature characteristic that occurs below 60K.

Data from a small transistor tested in this fashion was used to develop a physics based simulator. The simulator utilized incomplete ionization models with activation energies that were doping dependent, as well as a temperature dependent mobility model which accounted for the different scattering mechanisms and impurity band conduction. With the inclusion of these effects, the simulator demonstrated the capability to predict device operation at any temperature over the measured temperature range. Compared to commercial simulators, which are only valid down to the military specification of -55°C, this is a significant improvement.

5.1.3 Zener Diode Voltage Reference

The low temperature voltage reference capabilities of a zener diode were tested to see if the tunneling nature of the device made it less susceptible to temperature dependent effects. The diode was placed in series with a current limiting resistor and reverse biased in the zener breakdown region; measurements were recorded down to 13K. At temperatures near the NASA specification of 37K, the zener reference had a temperature coefficient $dV_{REF}/dT =$ 0.327mV/K, which was a factor of two improvement over the temperature coefficient of a silicon germanium voltage reference which was also tested for comparison. The stability of each reference at 37K was also measured. The SiGe reference exhibited a variation of 1.2mV, compared to 2.2mV for the zener. It should be kept in mind, though, that the zener reference was

tested in a less stable temperature environment. This temperature instability added as much as 0.78mV of variation (based on the temperature coefficient) to the total observed zener variation. This experiment showed that the zener tunneling structure resulted in a device which had better temperature performance than a SiGe based voltage reference and comparable noise-induced voltage fluctuation. Overall, the performance of the two devices was very similar, though the zener has a substantial advantage from a cost perspective.

5.1.4 Cryogenic Testing Guide

One of the major challenges associated with this research was the learning curve associated with cryogenic testing. Chapter two of this work is presented as a guide to low temperature testing. The information in this chapter is a combination of knowledge gained largely through conversations with NASA engineers, as well as personal experience. This chapter includes, among other things, information about test Dewar design, board design, thermal conduction, thermal isolation, vacuum pressure, outgassing, adsorption, and cryogen filling. The end of the chapter presents a comprehensive, step-by-step procedure to efficiently conduct a helium fill. It is hoped that this will serve as a useful guide to getting started with cryogenic electronics testing.

5.2 Recommendations for Future Work

5.2.1 Full Process Characterization

This research fully characterized the temperature dependent functionality of two MOSFET devices fabricated using the AMI 0.6μm process. One of the transistors was of minimum size and the other was very large (leading to relatively high power,

high temperature operation). It was clear from the measurements that the two devices exhibited some differences in their respective current versus temperature dependencies. To model an entire process as opposed to a single device, the research conducted in Chapter 3 should be expanded to include transistors of many different width/length ratios. This data, combined with an appropriate self heating model, could be used to develop a low temperature simulator which is accurate for an entire process. To measure self-heating more accurately, test structures could potentially be fabricated with built in thermal diodes on the die. A unified simulation model that accounts for transistor size and self heating effects would make low temperature circuit design a reality.

5.2.2 Silicon MOSFET Voltage Reference

Given the success of low temperature MOSFET performance demonstrated in this research, both in terms of current and noise, it is plausible that a low temperature voltage reference could be realized using these devices. If the voltage reference design took into account the increase in current at 37K demonstrated by this research, then it is likely it could be made to outperform both the silicon germanium circuit and the zener diode. Having said this, it would be necessary to first perform the additional characterization work described above before circuit simulation could occur during the design process. Self heating effects would also need to be accounted for.

Appendix A: MOSFET Modeling and Simulation

A.1 Modeling

As was discussed in chapter one, the primary goal of this research was to characterize MOSFET transistors at low temperature. Specifically, the aim was to provide a complete data set over the entire temperature range of interest that could be used for device modeling. In doing so, this would provide the basis for the development of a physics based simulator which accurately predicts device operation at any temperature. The results of this characterization work, combined with the modeling efforts undertaken by Dr. Akin Akturk (University of Maryland), have combined to produce a device simulator which accounts for impurity dependent changes in ionization and temperature dependent mobility effects to accurately predict transistor operation from 20K to room temperature [31]. A summary Dr. Akturk's modeling work, along with a comparison of simulated and measured MOSFET characteristics, is presented here.

A.1.1 Semiconductor Device Equations

To obtain device performance at cryogenic temperatures, a self-consistent solution is found for the Poisson equation (1) and the coupled differential semiconductor equations, which are the electron and hole current continuity equations (2) and (3), respectively:

$$\nabla^2\phi = -\frac{q}{\varepsilon}\left(p - n + D\right) \quad \textbf{(5)}$$

$$\frac{\partial n}{\partial t} = \nabla.\left(-n\mu_n\nabla\phi + \mu_n V_{\mathrm{th}}\nabla n\right) + \mathrm{GR}_n \quad \textbf{(6)}$$

$$\frac{\partial p}{\partial t} = \nabla.\left(p\mu_p \nabla \phi + \mu_p V_{\text{th}} \nabla p \right) + \text{GR}_p \quad \textbf{(7)}$$

Here, solution of the Poisson equation gives the electrostatic potential ϕ, and the continuity equations provide the electron concentration n and the hole concentration p. Additionally, q represents the electronic charge, ε is the dielectric constant, D is the net ionized doping concentration, μ_n and μ_p are the carrier mobilities, V_{th} is the thermal voltage, and GR_n and GR_p are the Shockley-Read-Hall generation-recombination rates.

The parameters in the above equations depend either explicitly or implicitly on temperature. The following are the explicit temperature dependencies of most of the parameters used to obtain device performance details [27, 28], the mobility and the incomplete ionization models, which are central to this discussion, will be explained later on.

$$n_o(T) = n_o(T_o)\left(\frac{T}{T_o}\right)^{1.5} e^{\left(-E_g(T)/2kT + E_g(T_o)/2kT_o\right)} \quad \textbf{(8)}$$

$$E_g(T) = E_g(T_o)\left(1 - 2.4\text{x}10^{-4}(T - T_o)\right) \quad \textbf{(9)}$$

$$V_{\text{th}}(T) = V_{\text{th}}(T_o)\left(\frac{T}{T_o}\right) \quad \textbf{(10)}$$

$$\phi_{\text{bi}}(T) = V_{\text{th}}(T)\ln\left(\frac{n}{n_o(T)}\right) \quad \textbf{(11)}$$

$$\upsilon_{\text{sat}}(T) = \upsilon_{\text{sat}}(T_o)\left(\frac{1 + e^{-T/2T_o}}{1 + e^{-1/2}}\right) \quad \textbf{(12)}$$

Starting with the intrinsic carrier concentration $n_o(T)$ of silicon (Si). Equation (8) shows that the intrinsic carrier concentration, compared to its value at room temperature (1.45×10^{10} cm^{-3} at T_o=300K), decreases predominantly exponentially as temperature drops. Specifically, simulations show that intrinsic carrier concentration changes from 6.86×10^{4}cm^{-3} to 1.59×10^{-11} cm^{-3}, 2.43×10^{-42}cm^{-3} and to 3.69×10^{-83}cm^{-3}, as temperature is lowered down to 200K, 100K, 50K and to 30K, respectively. Furthermore, Equation (9) includes the effects of bandgap broadening at colder temperatures. The final three equations show the temperature dependencies of the thermal voltage $V_{\mathrm{th}}(T)$, built-in potential $\phi_{\mathrm{bi}}(T)$, and the saturation velocity $\upsilon_{\mathrm{sat}}(T)$.

A.1.2 Incomplete Ionization and Mobility Modeling

Three ionization models have been considered for phosphorus (P) and boron (B), as these are the donor and acceptor atoms, respectively, of the devices modeled. Each model suggests different effects of dopant concentration on activation energies, resulting in different predictions for low temperature device performance. A temperature dependent mobility model has also been developed. In Section 5.2, each incomplete ionization model is combined with the mobility model to allow for device simulation. In all three models, impurity band broadening has been ignored due to the narrow energy width of the band [17].

The first model considered was the simplest of the three. It takes the activation energies of phosphorus in silicon (Si:P) and boron in silicon (Si:B) as constants that are independent of the dopant densities, which are $\Delta E_{\mathrm{Si:P}} = 45.5$ meV and $\Delta E_{\mathrm{Si:B}} = 44.39$ meV [17]. Using Fermi-Dirac Statistics, the net ionized dopant density as a function of space and temperature can be expressed as the difference

between the net ionized donor concentration and the net ionized acceptor concentration. This is given below [15,43]

$$D(r,T) = \frac{N^0_{\text{Si:P}}(r,T)}{1+\dfrac{n(r,T)}{g_d N_C(T) e^{-\Delta E_{\text{Si:P}}/kT}}} - \frac{N^0_{\text{Si:B}}(r,T)}{1+\dfrac{p(r,T)}{g_a N_V(T) e^{-\Delta E_{\text{Si:B}}/kT}}} \tag{13}$$

In (13), $N^0_{\text{Si:P}}(r,T)$ and $N^0_{\text{Si:B}}(r,T)$ are the total (ionized and unionized) donor and acceptor concentrations. N_C and N_V are the effective densities of states at the conduction band edge and valence band edge, respectively. These terms are multiplied by the scale factors g_d (=1/2) and g_a (=1/4) to account for the band degeneracies.

The second incomplete ionization model takes into account the decrease in activation energies due to increases in dopant concentration, which subsequently decrease the average distance between dopants. This model uses the same equation (13) as Model 1 for the net ionized dopant density, but the activation energies used in the exponential terms are expressed as a function of dopant concentration, as shown below [21-25].

$$\Delta E_{\text{Si:P}}(r,T) = 45.5 - 3.1\times 10^{-8}\left(N^0_{\text{Si:P}}(r,T)\right)^{1/3} \tag{14}$$

$$\Delta E_{\text{Si:B}}(r,T) = 44.39 - 3.037\times 10^{-8}\left(N^0_{\text{Si:B}}(r,T)\right)^{1/3} \tag{15}$$

In (14) and (15), total dopant concentrations are in cm^{-3} and activation energies are in meV. This model predicts higher ionization rates than the first model, but incomplete ionization still occurs, even very high dopant densities. It should be noted that an approximate equation for (14) and (15) can be derived using the screening of the impurities by one another. For a screening length λ and a uniform impurity

distribution with impurities a distance of d $(=N^{-1/3})$ apart, the lowering of the potential barrier due to two neighboring impurities is [21]:

$$\Delta E \simeq 2\frac{\left(q/4\pi\varepsilon\right)\exp(-d/2\lambda)}{\left(d/2\right)} - \frac{\left(q/4\pi\varepsilon\right)\exp(-d/\lambda)}{\left(d\right)} \quad \textbf{(16)}$$

In this expression, the first term is the maximum potential at half distance between two neighboring impurities, and the second term is the potential in the case of an isolated impurity. Assuming λ is much greater than d and using the first order terms of the Taylor expansion, this equation becomes (17), which is an expression for activation energy similar to those given in (14) and (15).

$$\Delta E \simeq 3\left(\frac{q}{4\pi\varepsilon}\right)d^{-1} \simeq 3.8\times10^{-8}N^{1/3} \quad \textbf{(17)}$$

The third model, based upon recent papers by Altermatt et al., suggests full ionization rates at high dopant densities [16-18]. In this model, activation energy drops as a stronger function of dopant concentration compared to equations (14) and (15) used in Model 2. In addition, the incomplete ionization is partially compensated for by the fraction of carriers in localized states. These factors result in full ionization for high dopant densities.

In Model 3, the net ionized donor (phosphorus) and acceptor (boron) concentrations are related to the activation energies and carrier concentrations as follows:

$$\frac{N^{+}_{\text{Si:P}}(r,T)}{N^{0}_{\text{Si:P}}(r,T)} = \frac{b_d}{1+\dfrac{n(r,T)}{g_d N_C(T) e^{-\Delta E_{\text{Si:P}}/kT}}} + (1-b_d) \quad \textbf{(18)}$$

$$\frac{N^{-}_{\text{Si:B}}(r,T)}{N^{0}_{\text{Si:B}}(r,T)} = \frac{b_a}{1+\dfrac{p(r,T)}{g_a N_V(T) e^{-\Delta E_{\text{Si:B}}/kT}}} + (1-b_a) \quad \textbf{(19)}$$

In the above equations, b_d and b_a represent the fractions of carriers in localized states, which are functions of the dopant densities as given in [16-18]. As in Model 2, the activation energies used in the above equations are functions of dopant concentrations. These expressions are given below:

$$\Delta E_{\text{Si:P}}(r,T) = \frac{45.5}{1+\left(\dfrac{N^{0}_{\text{Si:P}}(r,T)}{3\times 10^{18}}\right)^{2}} \quad \textbf{(20)}$$

$$\Delta E_{\text{Si:B}}(r,T) = \frac{44.39}{1+\left(\dfrac{N^{0}_{\text{Si:B}}(r,T)}{1.7\times 10^{18}}\right)^{1.4}} \quad \textbf{(21)}$$

Here, the ionized dopant density is once again expressed as the difference between the net ionized donor concentration and the net ionized acceptor concentration, as in equation (13). This is written as follows:

$$D(r,T) = N^{+}_{\text{Si:P}}(r,T) - N^{-}_{\text{Si:B}}(r,T) \quad \textbf{(22)}$$

It should be noted here that Equation (22) reduces to Equation (13) for the net ionized doping density if the fractions of carriers in localized states are set to 1 in Equations (18) and (19).

Figure 44 shows the ionization rate, which is the ratio of ionized dopants to the total dopant concentration, as a function of doping at (a) room temperature and (b) 50K. For the doping levels considered in Figure 44, it is assumed that the electron (hole) concentration is equal to the ionized donor (acceptor) level. Equation (22) is then solved for the ionized doping level. At room temperature for the highest doping level of 10^{20} cm^{-3}, Model 1, which assumes constant activation energies, results in the lowest ionization rate of 10 to 20 percent. This is followed by the higher ionization rate (above 60 percent) of model 2 (activation energy changes with the average distance between impurities), and the full ionization of model 3. At 50K in the vicinity of the highest doping level, model 2 (3) gives higher ionization rates that are close to full ionization than model 3 (2) for the donor (acceptor) doping, while the ionization rates associated with model 1 are much lower. For the simulated NMOSFET, the channel acceptor doping is 2×10^{17} cm^{-3} and the peak source-drain donor doping is 10^{20} cm^{-3}. Thus, ionization rates for these specific doping levels may have a greater influence on the device performance. At room temperature, ionization rate for the lower channel acceptor level is about 80 percent for all models. However at 50K, Model 2 indicates approximately 10 times higher ionization rate compared to those calculated using Models 1 and 3. The next section will explain how these rates affect simulator performance.

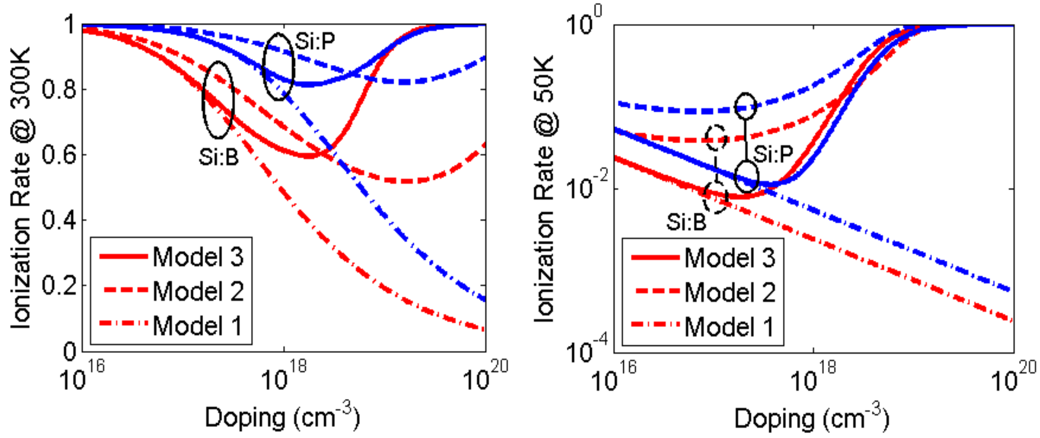


Figure 44: Calculated ionization rates of phosphorus and Boron in Silicon at room temperature (left) and 50K (right) as a function of dopant concentration, using three different models

The final step in the development of a device simulator is the development of a temperature dependent mobility model. This model used considers the temperature dependencies of the bulk mobility and acoustic phonons separately. For acoustic phonons, the following temperature dependent form is used [44]:

$$\mu_{ac}(\tilde{T}) = \frac{1 + \left(\beta / \tilde{T}\right) E_{\perp}^{2/3}}{\alpha E_{\perp}} \tag{23}$$

In (17), $E_{\perp}$ is the local electric field in the normal direction of the channel, $\tilde{T}$ is the ratio of the device temperature T to the room temperature 300K ($\tilde{T} = \frac{T}{300\text{K}}$), and α and β [46,47] are adjusted empirically for the simulated device. Bulk mobility, on the other hand, is written as a product of $\mu_b(\tilde{T})$ and $\mu_b(N)$, which incorporate effects of the temperature and the impurity concentration, respectively. The following data was extracted for the temperature dependent part of the bulk mobility using the measured data:

$$\mu_b(\widetilde{T}) = 12.19 \times \widetilde{T}^4 - 33.56 \times \widetilde{T}^3 + 25.37 \times \widetilde{T}^2 - 4.07 \times \widetilde{T} + 1.08 \qquad \textbf{(24)}$$

Here, as was discussed in chapter one, mobility increases due to suppressed electron-phonon scatterings down to approximately 190K. It reaches a peak and then rolls off as temperature decreases, due to increased impurity scatterings. Below 50K, however, the rate of this decrease gets lower. This is associated with the mobility enhancement due to conduction in the impurity band, which is more influential at colder temperatures. Total mobility due to bulk and acoustic phonons is then obtained using the Matthiessen's rule as follows:

$$\mu(N, E_\perp, \widetilde{T}) = \frac{\left(\mu_b(N)\mu_b(\widetilde{T})\right)}{1 + \alpha\left(\mu_b(N)\mu_b(\widetilde{T})\right)E_\perp\left(1 + \left(\beta/\widetilde{T}\right)E_\perp^{2/3}\right)^{-1}} \qquad \textbf{(24)}$$

Finally, to account for the lateral and vertical electric fields, the above expression is used in the Hiroki model [45].

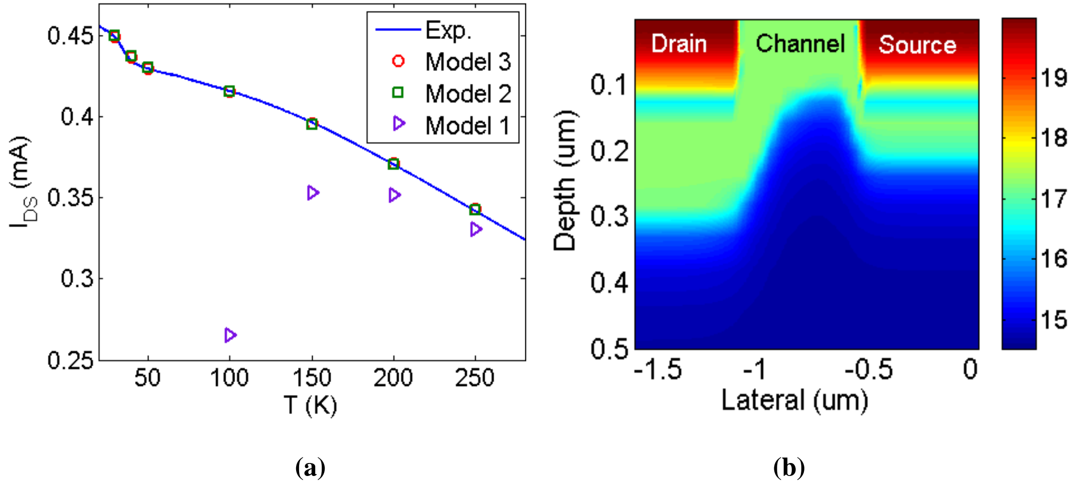
A.2 Simulation

The three incomplete ionization models were each combined with the temperature dependent mobility model and the semiconductor device equations to form three different simulators. In this section, each simulator is tested against the measured data to determine the validity of each model for use in a low temperature simulator. Special emphasis is placed on Model 3, which was developed in conjunction with the research presented in this paper.

A.2.1 Current versus Temperature

To first test the performance of each incomplete ionization model, the simulator was programmed for device A and run in the configuration used for the

functionality test described in Chapter 3. The measured results, as well as the simulated results for each of the three models are shown below in Figure 45a. Figure 45b shows the doping profile of the transistor at 50K using Model 3.

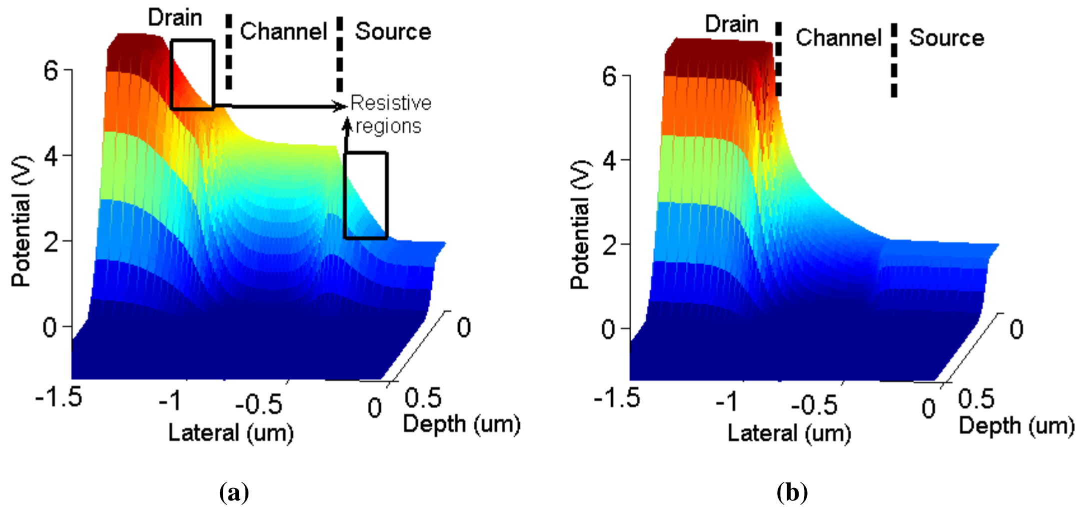


(a) **(b)**

Figure 45: (a) Calculated and measured current versus temperature characteristic for device A, and (b) calculated doping profile at T=50K using Model 3. Colorbar shows concentration in cm^{-3} (V_{GS}=4V, V_{DD}=5V)

In Figure 45a, the measured current versus temperature curve of device A is the solid line (also shown in Figure 14, Chapter 3). As was described in chapter three, the current initially increases as temperature decreases from room temperature due to suppressed electron-phonon scattering rates. The increase in drain-to-source current as a function of temperature then starts to roll off for temperatures below 100K. This is associated with electron-impurity scatterings, which become comparable or higher than electron-phonon scatterings at lower temperatures. For temperatures below 50K, however, the current increases sharply as temperature decreases. This rise is attributed to additional conduction in the impurity band. Each of these three different current-temperature behaviors is characterized by the mobility model given in the previous section.

Figure 45a also shows calculated current versus temperature curves using the three different incomplete ionization models detailed in the previous section. It is apparent from this figure that use of Model 2 or 3 for incomplete ionization gives similar performance curves, which match closely to that measured. As a reminder, the differences between model 2 and 3 are the change in activation energies as a function of doping and the additional effects of localized states. Activation energy in Model 2 decreases with shorter average distance between the impurities, but does so at a slower rate than model 3, in which localized states also contribute to the total ionization rate. Since ionization rates due to Models 2 and 3 are similar and close to full ionization for the higher doping levels of the source and drain regions, but quite different for the channel doping level, the similar current values calculated using Models 2 and 3 suggest that the current is less sensitive to the channel dopant ionization. This is associated with the gate-field driven channel formation. Here, different ionization rates in the channel might have affected the threshold voltage. This effect is minimal, however, due to the low hole concentration in the channel which gives rise to full ionization in the channel as shown in Figure 45b. Furthermore, even assuming full ionization everywhere in the NMOSFET, though it is not physical, introduces minimal error in the calculated current compared to the measured curve.



(a) (b)

Figure 46: Calculated MOSFET potential profiles at 40K, using (a) Model 1, and (b) Model 3 (V_{GS}=4V, V_{DD}=5V)

The calculated currents in Figure 45a using Model 1 (doping-independent activation energies) initially show current increase with temperature lowering, followed by peaking at approximately 175K, and later current roll off. In this model, the main reason current is substantially lower compared to those other calculated values, especially at cryogenic temperatures, is that the source and drain regions become very resistive due to low ionization rates. Thus, the applied drain voltage drops across these resistive regions as shown in Figure 46a, resulting in low currents. However, the calculated potential profiles of the source and drain regions using the other models are approximately flat, as shown in Figure 46b, thanks to high ionization rates and the consequent abundance of carriers.

A.2.2 I-V Characteristic Simulation

After first testing each of the incomplete ionization models in the previous simulation, a second simulation was run using Model 3 in an attempt to reproduce the I-V families of curves measured in Chapter 3 for device B. Simulations were

conducted at room temperature (for device A), and for temperatures of 37K, 60K, and 120K (device B). The results of these simulations are shown below in Figure 47.

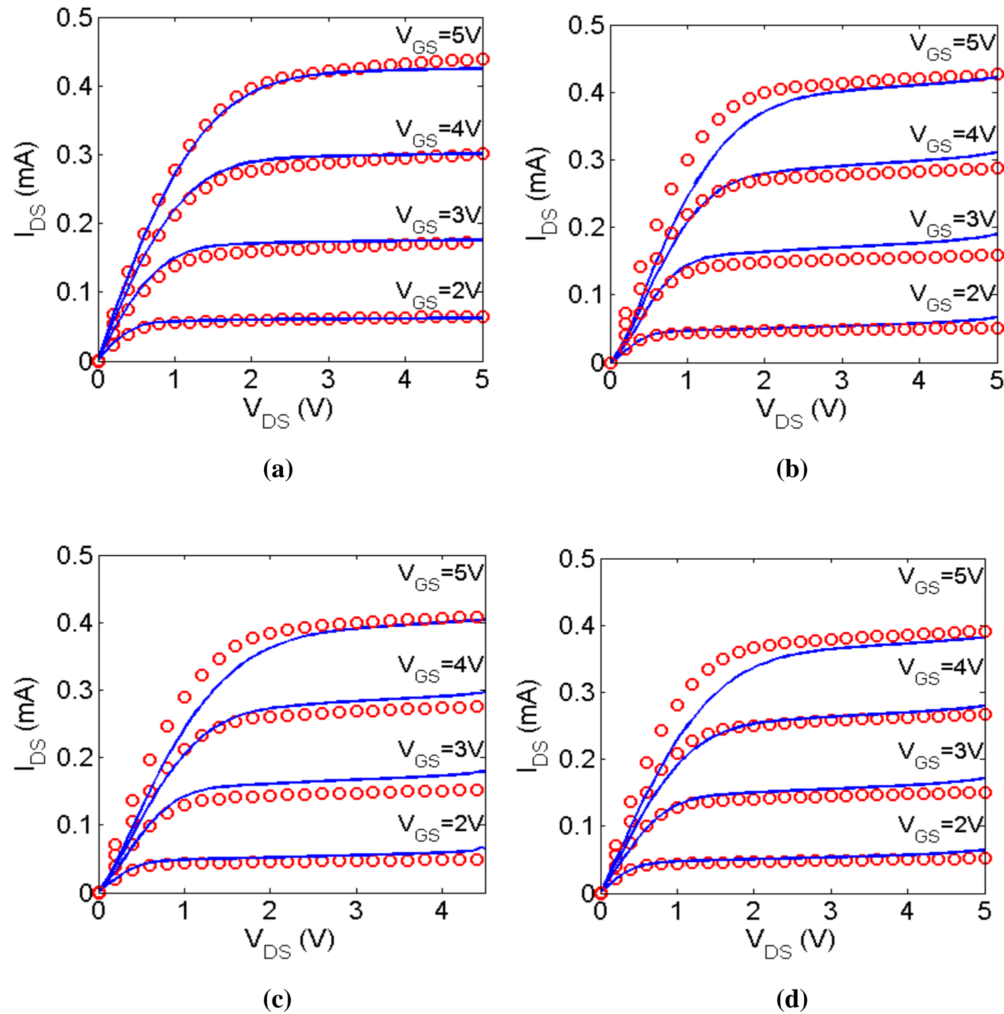


Figure 47: Calculated (circles) and measured (lines) I-V families of curves for (a) device A at 293K and device B at (b) 37K, (c) 60K, and (d) 120K, using Model 3

The simulations shown above were run by first extracting a parameter set and simulating current for device A, and then dividing the simulated currents by a scale factor to predict device B. This was done because the two devices were fabricated on the same run, but device A sourced a greater amount of current for the same applied

voltage than device B. As is clear from analysis of Figure 47, overall simulator performance is excellent. There is some over-predicting in the triode region at higher gate voltages which could potentially lead to inaccuracies for devices operating in this region. On the whole, however, the model shows that by incorporating impurity dependent changes in activation energy and temperature dependent mobility effects, as well as extracting low temperature device parameters, an accurate low temperature MOSFET simulator can, in fact, be developed.

References

[1] R. R. Ward, W. J. Dawson, R. K. Kirschman, O. Mueller, R. L. Patterson, J. E. Dickman, and A. Hammoud, "Ge-based semiconductor devices for cryogenic power electronics," 5th Workshop on Low Temp. Electronics, 2002.

[2] J.D. Cressler, "On the potential of SiGe HBTs for extreme environment electronics," *Proc. of the IEEE,* **93,** 1559, (2005).

[3] C. Kittel, *Introduction to Solid State Physics*, New York, Wiley, 1976.

[4] Y. Taur, T. Ning, *Fundamentals of Modern VLSI Devices*, New York, Cambridge University Press, 1998.

[5] N. Arora, *MOSFET Models for VLSI Circuit Simulation*, Springer-Verlag, Wien, (1993).

[6] S. M. Sze, *Physics of Semiconductor Devices*, Wiley, New York. (1981).

[7] G. A. Thomas, M. Capizzi, F. DeRosa, R. N. Bhatt, and T. M. Rice, "Metal-insulator transition in a doped semiconductor," *Phys. Rev. B.* **23**, 5472 (1981).

[8] D. F. Holcomb and J. J. Rehr, "Percolation in Heavily Doped Semiconductors," *Phys. Rev.* **183**, 773 (1969).

[9] R. Riklund and K. A. Chao, "Concentration-fluctuation model of a doped semiconductor in the nonmetallic regime: Pseudocluster investigation," *Phys. Rev. B.* **26**, 2168 (1982).

[10] D. New and T. G. Castner, "Donor clusters in silicon. Results of ESR measurements," *Phys. Rev. B.* **29**, 2077 (1984).

[11] D. New, "Donor clusters in silicon. II. ESR simulations," *Phys. Rev. B.* **32**, 2419 (1985).

[12] E. M. Conwell, "Impurity band conduction in germanium and silicon," *Phys. Rev.* **103(1)**, 51 (1956).

[13] P. P. Debye, and E. M. Conwell, "Electrical Properties of n-type germanium," *Phys. Rev.* **93(4)**, 693 (1954).

[14] K. R. Atkins, R. Donovan, and R. H. Walmsley, "Low-temperature impurity conduction in n-type silicon," *Phys. Rev.* **118(2)**, 411 (1960).

[15] A. Akturk, N. Goldsman, Z. Dilli and M. Peckerar, "Device performance and package induced self-heating effects at cryogenic temperatures," *Proc. of SISPAD*, 240 (2006).

[16] P. P. Altermatt, A. Schenk, and G. Heiser, "A simulation model for the density of states and for incomplete ionization in crystalline silicon. I. Establishing the model in Si:P," *Jour. of Appl. Phys.* **100**, 113714 (2006).

[17] P. P. Altermatt, A. Schenk, B. Schmithusen, and G. Heiser, "A simulation model for the density of states and for incomplete ionization in crystalline silicon. II. Investigation of Si:As and Si:B and usage in device simulation," *Jour. of Appl. Phys.* **100**, 113715 (2006).

[18] A. Schenk, P. P. Altermatt, and B. Schmithusen, "Physical model of incomplete ionization for silicon device simulation," *Proc. of SISPAD*, 51 (2006).

[19] N. F. Mott, "Metal-insulator transition," *Rev. of Modern Phys.* **40(4)**, 677 (1968).

[20] H. Watanabe, and S. Takagi, "Effects of incomplete ionization of impurities in poly-Si gate and band gap narrowing on direct tunneling gate leakage current," *Jour. of Appl. Phys.* **90(3)**, 1600 (2001).

[21] T. F. Lee, and T. C. McGill, "Variation of impurity-to-band activation energies with impurity density," *Jour. of Appl. Phys.* **46(1)**, 373 (1975).

[22] G. D. Mahan, "Energy gap in Si and Ge: Impurity dependence," *Jour. of Appl. Phys.* **51(5)**, 2634 (1980).

[23] M. R. Shaheed, and C. M. Maziar, "A physically based model for carrier freeze-out in Si- and SiGe- base bipolar transistors suitable for implementation in device simulators," *Proc. of Bipolar/BICMOS Cir. & Tech. Meeting*, 191 (1994).

[24] G. L. Pearson, and J. Bardeen, "Electrical properties of pure silicon and silicon alloys containing boron and phosphorus," *Phys. Rev.* **75(5)**, 865 (1949).

[25] S. R. Dhariwal, V. N. Ojha, and G. P. Srivastava, "On the shifting and broadening of impurity bands and their contribution to the effective electrical bandgap narrowing in moderately doped semiconductors," *IEEE Trans. on Elec. Dev.* **32(1)**, 2395 (1985).

[26] Muller and Kamins, *Device Electronics for Integrated Circuits*, 2nd edition, New York, Wiley (1986).

[27] A. Akturk, N. Goldsman, and G. Metze, "Self-consistent modeling of heating and mosfet performance in three-dimensional integrated circuits," *IEEE Trans. on Elec. Dev.* **52(11)**, 2395 (2005).

[28] A. Akturk, N. Goldsman, L. Parker and G. Metze, "Mixed-mode temperature modeling of full-chip based on individual non-isothermal device opeartions," *Solid State Elec.* **49(7)**, 1127 (2005).

[29] F. H. Gaensslen, V. L. Rideout, E. J. Walker, J. J. Walker, "Very Small MOSFET's for low-temperature operation," *IEEE Trans. on Elec. Dev.* **24(3)**, 218 (1977).

[30] F. F. Fang and A. B. Fowler, "Transport properties of electrons in inverted silicon surfaces," *Phys. Rev.* **169**, 619 (1965).

[31] A. Akturk, J. Allnutt, Z. Dilli, N. Goldsman, M. Peckerar, "Device Modeling at Cryogenic Temperatures: Effects of Incomplete Ionization," (under review for publication)

[32] W. Nuyts and R. van Overstraeten, "Influence of the incomplete ionization of impurities of the capacitance of p-n junctions," *Jour. of Appl. Phys.* **42**, 3988 (1971).

[33] G. Xiao, J. Lee, J. J. Liou, and A. Ortiz-Conde, "Incomplete ionization in a semiconductor and its applications to device modeling," *Microelectronics and Reliability*. **39**, 1299 (1999).

[34] N. F. Mott, "Metal-insulator transition," *Rev. of Modern Phys.* **40(4)**, 677 (1968).

[35] James Dewar, ″The Adsorption and Thermal Evolution of Gases occluded in Charcoal at Low Temperatures," *Proc. Roy. Soc.* **74**, 126, (1904).

[36] U.S. patent application. U.S. Patent number 872,795, (1907).

[37] Serway, Beichner, *Physics for Scientists and Engineers,* 5th edition, Orlando, Harcourt (2000).

[38] http://www.irlabs.com/pdf/science_technology_catalog.pdf, last visited April 2007

[39] J. Blears, J. E. Greer, J. Nightingale, "Factors Determining the Ultimate Pressure in Large High-vacuum Sytems," *Advances in Vacuum Science and Technology.* **1**, 473, 1960.

[40] http://outgassing.nasa.gov, last visited April 2007

[41] D. Lide, *CRC Handbook of Chemistry and Physics 86th edition*, Boca Raton, CRC Press, (2005).

[42] http://www.mosis.org, last visited April 2007

[43] A. Akturk, N. Goldsman, and G. Metze, "Self-consistent modeling of heating and mosfet performance in three-dimensional integrated circuits," *IEEE Trans. on Elec. Dev.* **52(11)**, 2395 (2005).

[44] C. Lombardi, S. Manzini, A. Saporito, M. Vanzi, "A physically based mobility model for numerical simulation of nonplanar devices," *IEEE Trans. on Comp.-aided Design* **7(11)**, 1164 (1988).

[45] A. Hiroki, S. Odanaka, K. Ohe, and H. Esaki, "A mobility model for submicrometer mosfet device simulations," *IEEE Elec. Dev. Lett.* **8(5)**, 231 (1987).

[46] Personal communications with Anh La, Joseph Adams, and Shahid Aslam at NASA Goddard Space Flight Center (June 2006 – April 2007).