A Novel High PSR Voltage Reference with Secondary Temperature Compensation

Ning Zhi-Hua, He Le-Nian, Wang Yi, Shao Ya-Li
Institute of VLSI Design
Zhejiang University
Hangzhou, PR of China
ningzh@vlsi.zju.edu.cn

***Abstract*—A novel voltage reference based on Kujik [1] bandgap is proposed in this paper. An extra amplifier and bipolar are used to produce a current of positive temperature coefficient, which is for compensating the Kujik bandgap reference in high temperature. The reference finally has a temperature coefficient of only 10 ppm/℃. A negative feedback loop is introduced to provide a pre-regulated power supply for the voltage reference, which has increased the power supply rejection (PSR) of the voltage reference to -120 dB@dc. The circuit has been designed with TSMC 0.35 μm CMOS process, and the measurements agree our design.**

Keywords- voltage reference; Kujik bandgap; PSR; secondary temperature compensation

I. INTRODUCTION

At present high-performance ADC, DAC and power management chips need voltage references independent of temperature and supply. In order to improve the temperature characteristics of the voltage reference, many temperature-compensated voltage references [2-8] are proposed. In addition, to reduce the ripple sensitivity of the voltage reference, the research of high power supply rejection (PSR) [9-11] voltage reference is also a hotspot.

As the bandgap reference has a very good temperature characteristic, more and more voltage references are based on it. Reference [2] uses the PNP transistor and NPN transistor to introduce two currents of different temperature coefficients, which are used to produce a voltage reference of low temperature drift. With the simultaneous use of the NPN and PNP transistors, it sets higher requirements for process, and this structure does not possess a high PSR feature. Voltage reference in [11] is of high PSR performance but does not have a secondary temperature compensation, also large power consumption is needed. Besides, voltage references in [2-11] are all based on Gray structure, the basic structure and the improved one of which are shown in Fig. 1(a) and Fig. 1(b), respectively. The disadvantage of these bandgaps is that an external resistive load would affect the output of the reference and its temperature characteristics. One solution is to add an output buffer. However, because of the limitation of the buffer, it's difficult for the reference to get a high PSR. Another bandgap reference is Kujik structure [1], shown in Fig. 1(c). It is not sensitive to resistive load, and because the output of the reference is located in a negative feedback loop, this structure is suitable for the design of the reference of high PSR. However, it is hard for Kujik bandgap to introduce a current for secondary temperature compensation in standard CMOS technology, thus traditional Kujik bandgap has a poor temperature characteristic, normally larger than 20 ppm/℃. Voltage reference presented in this paper is based on Kujik bandgap and a novel secondary temperature compensation idea is introduced. The reference is designed with TSMC 0.35 μm CMOS process. Measurement results show the reference is of good temperature characteristics, high PSR and low power consumption.

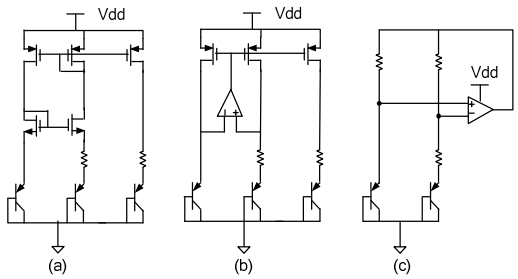

Figure 1. (a)Original Gray bandgap (b) Improved Gray bandgap (c) Kujik bandgap

Section Ⅱ describes the structure of the voltage reference proposed in this paper. Section Ⅲ introduces a novel method of secondary temperature compensation and the related calculation is illustrated. In section Ⅳ the PSR of the reference is quantized. Section Ⅴ is measurement results and a comparison between this work and other papers is remarked.

II. STRUCTURE OF THE VOLTAGE REFERENCE

The voltage reference presented in this paper is shown in Fig. 2, it includes bias, pre-regulator, bandgap core, secondary compensation and start-up. The core circuit is a typical Kujik bandgap reference; secondary temperature compensation circuit is composed of an op-amp and a bipolar transistor and the current I_{NL} with positive temperature coefficient is produced. Pre-regulator circuit provides a pre-regulated power supply for other sub-circuits, which increases the PSR of the system.

978-0-7695-4031-3/10 $26.00 © 2010 IEEE
DOI 10.1109/iCECE.2010.781

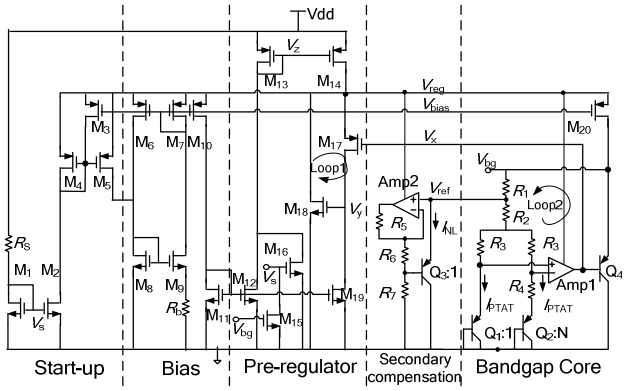

Figure 2. Schematic of the voltage reference proposed by this paper

III. PRINCIPLE OF TEMPERATURE COMPENSATION

Assume V_{ebni} is the threshold voltage of the bipolar Q_i, and V_{ebi} is the actual voltage difference between the emitter and base of Q_i. From the core of the bandgap reference and secondary compensation circuit in Fig. 2 we can conclude that:

$$V_{bg} = V_{eb1} + I_{PTAT}(2R_1 + 2R_2 + R_3) + I_{NL}R_1 \tag{1}$$

$$I_{PTAT} = \frac{V_T \ln N}{R_4} \tag{2}$$

Since Q1 works in the saturation region,

$$V_{eb1} = V_{ebn1} \tag{3}$$

From [13], we have

$$V_{eb1} = V_{go} + T \times \frac{V_{ebn1o} - V_{go}}{T_o} + (\alpha - \gamma)V_T \ln(\frac{T}{T_o}) \tag{4}$$

V_{ebn1o} is the threshold voltage of transistor Q_1 at the temperature of T_o; V_{go} is the bandgap voltage at the temperature of T_o.

By setting an appropriate value of R_1~R_4, we can make $V_{To}\ln N(2R_1+2R_2+R_3)/R_4=V_{go}-V_{ebn1o}$, then the bandgap reference obtains a first-order temperature compensation. Fig. 3(a) shows the simulation curve of bandgap reference vs temperature after first-order temperature compensation.

V_{eb3} can be expressed as

$$V_{eb3} = \frac{V_{ref}R_6}{R_6 + R_7} = \left[V_{eb1} + I_{PTAT}(2R_2 + R_3)\right]\frac{R_6}{R_6 + R_7} \tag{5}$$

Since Q_1 and Q_3 are identical, we can suppose V_{ebn3} and V_{ebn1} are equal (in fact, due to the different emitter currents, there is tiny difference). Therefore, V_{eb3} can be rewritten as

$$V_{eb3} = \left[V_{ebn3} + I_{PTAT}(2R_2 + R_3)\right]\frac{R_6}{R_6 + R_7} \tag{6}$$

Equation (6) can then be rearranged into

$$V_{eb3} - V_{ebn3} = I_{PTAT}(2R_2 + R_3)\frac{R_6}{R_6 + R_7} - \frac{R_7 V_{ebn3}}{R_6 + R_7} \tag{7}$$

Since V_{ebn3} is inversely proportional to temperature, from equation (7) we know V_{eb3}-V_{ebn3} is proportional to temperature. When $I_{PTAT}(2R_2+R_3)R_6>R_7V_{ebn3}$, I_{NL} is produced and I_{NL} is also in proportion to temperature. I_{NL} is used to compensate the bandgap reference in high temperature. I_{NL} can be described as

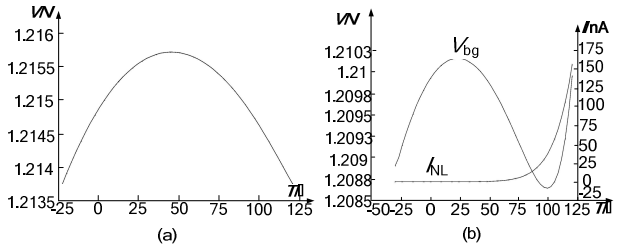

Figure 3. (a)Temperature curve of V_{bg} after 1st-order compensation (b) Temperature curves of I_{NL} and V_{bg} after secondary compensation

$$I_{NL} = \varepsilon u\left(T - T_{on}\right) \tag{8}$$

T_{on} represents the temperature when V_{eb3}=V_{ebn3}, and ε is the slope of I_{NL}.

The simulation results of I_{NL} and the bandgap reference V_{bg} after secondary compensation are shown in Fig. 3(b). Thus the temperature coefficient of bandgap reference has been improved from 13 ppm/℃ to 8.6 ppm/℃ after secondary compensation.

Fig. 4(a) and (b) are the internal structure of Amp1 and Amp2 respectively.

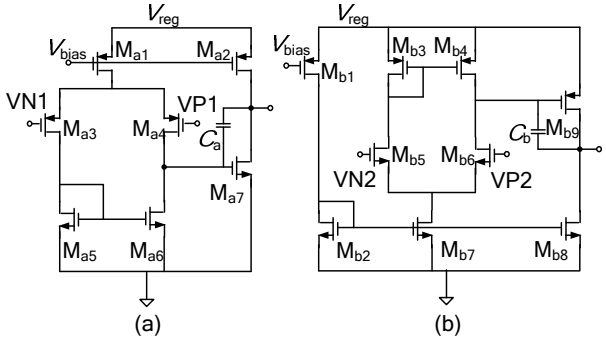

Figure 4. (a) Schematic of Amp1 (b) Schematic of Amp2

IV. CACULATION OF PSR

There are two negative feedback loops in the voltage reference: Loop 1 in the pre-regulator and Loop 2 in the bandgap core (Fig. 2). To calculate PSR of the voltage reference, we assume

$$PSR1 = \frac{V_{reg}}{\mathrm{Vdd}} \tag{9}$$

$$PSR2 = \frac{V_{bg}}{V_{reg}} \tag{10}$$

*PSR*1 represents the supply rejection of the pre-regulator and *PSR*2 represents the supply rejection of the bandgap core. So the PSR of the voltage reference can be written as

$$\mathrm{PSR} = PSR1 * PSR2 \tag{11}$$

Since Q_4 and M_{20} constitute an emitter follower, the gain from V_x to V_{bg} equals to 1. Therefore, V_{reg}/V_x=PSR2. To calculate PSR2, we redraw the block diagram of Loop 2 in Fig. 5(a). Assume H is the gain from V_{reg} to V_{bg}, and A_{C2} is the loop gain of Loop 2. The transfer function can be written as

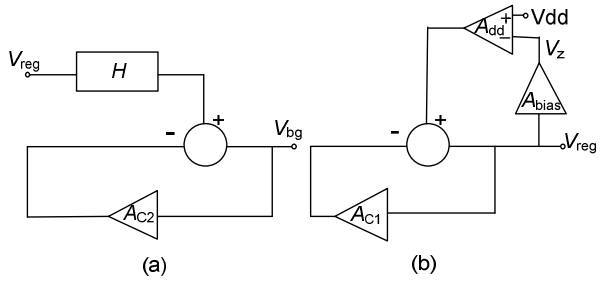

Figure 5. (a) Block diagram of Loop 2 (b) Block diagram of Loop 1

$$\mathrm{PSR}2=\frac{V_{\mathrm{bg}}}{V_{\mathrm{reg}}}=\frac{H}{1+A_{\mathrm{C2}}} \tag{12}$$

Loop 2 has three stages: the first stage of Amp2, the second stage of Amp2 and the emitter follower. Assume the gain from V_{reg} to the output of stage i is $A_{\mathrm{dd}i}$, while the open loop gain of stage i is A_i, and H is shown as

$$H=A_{\mathrm{dd1}}A_2A_3+A_{\mathrm{dd2}}A_3+A_{\mathrm{dd3}} \tag{13}$$

While A_{C2} is shown as

$$A_{C2}=(\beta_1-\beta_2)A_1A_2A_3 \tag{14}$$

Loop 2 has two feedback branches, and β_1 and β_2 are the feedback factors of the two.

Assuming $g_{\mathrm{bias}}=i_{\mathrm{bias}}/V_{\mathrm{reg}}$, from [14] we have

$$g_{\mathrm{bias}}=\frac{1+g_{m9}R_{\mathrm{b}}}{\left(1+g_{m9}R_{\mathrm{b}}-\dfrac{g_{m9}}{g_{m8}}\right)\left[r_{o7}\,\|\,(r_{o9}+R_{\mathrm{b}})\right]} \tag{15}$$

In this equation, g_{bias} represents the supply rejection of the bias, R_{b} is the resistor in the bias (Fig. 2), and $g_{\mathrm{m}i}$ is the transconductance of MOS transistor M_i. In the following article, $g_{\mathrm{mQ}i}$ stands for the transconductance of the bipolar transistor Q_i. Therefore,

$$A_{\mathrm{dd1}}=\frac{g_{\mathrm{bias}}g_{ma1}}{2g_{m7}}\left(r_{oa3}\,\|\,\frac{1}{g_{ma5}}\right)\approx\frac{g_{\mathrm{bias}}g_{ma1}}{2g_{m7}g_{ma5}} \tag{16}$$

$$A_{\mathrm{dd2}}=\frac{g_{\mathrm{bias}}g_{ma2}}{g_{m7}}\left(r_{oa2}\,\|\,r_{oa7}\right) \tag{17}$$

$$A_{\mathrm{dd3}}=\frac{g_{\mathrm{bias}}g_{m20}}{g_{m7}}\left(r_{o20}\,\|\,\frac{1}{g_{m\mathrm{Q4}}}\right)\approx\frac{g_{\mathrm{bias}}g_{m20}}{g_{m7}g_{m\mathrm{Q4}}} \tag{18}$$

A_i can be written as

$$A_1=g_{ma3}\left(r_{oa4}\,\|\,r_{oa6}\right) \tag{19}$$

$$A_2=g_{ma7}\left(r_{oa2}\,\|\,r_{oa7}\right) \tag{20}$$

$$A_3\approx 1 \tag{21}$$

We can also write β_1 and β_2 as

$$\beta_1=\frac{R_4+\dfrac{1}{g_{m\mathrm{Q2}}}}{2(R_1+R_2)+R_3+R_4+\dfrac{1}{g_{m\mathrm{Q2}}}} \tag{22}$$

$$\beta_2=\frac{\dfrac{1}{g_{m\mathrm{Q1}}}}{2(R_1+R_2)+R_3+\dfrac{1}{g_{m\mathrm{Q1}}}} \tag{23}$$

With equation (12~21), PSR2 can be written as

$$\mathrm{PSR}2\approx\frac{H}{A_{\mathrm{C2}}}\approx\frac{A_{\mathrm{dd1}}A_2A_3+A_{\mathrm{dd2}}A_3}{(\beta_1-\beta_2)A_1A_2A_3}=\frac{g_{\mathrm{bias}}\left(\dfrac{g_{ma1}}{2g_{ma5}}+\dfrac{g_{ma2}}{g_{ma7}}\right)}{g_{m7}g_{ma3}(\beta_1-\beta_2)(r_{oa4}\,\|\,r_{oa6})} \tag{24}$$

To calculate PSR1, we redraw the block diagram of Loop 1 in Fig. 5(b). A_{dd} is the gain of M_{14}. A_{bias} is the gain from V_{reg} to V_z. A_{C1} is the loop gain of Loop 1. From [8], we have

$$A_{\mathrm{C1}}=\left[g_{m17}-\frac{g_{\mathrm{bias}}g_{m10}g_{m19}}{g_{m7}g_{m11}}\right]g_{m18}\times(r_{o17}\,\|\,r_{o19})R_{\mathrm{reg}} \tag{25}$$

R_{reg} is the output resistance of V_{reg}. A_{dd} can be written as

$$A_{\mathrm{dd}}=g_{m14}\left(1-\frac{r_{o12}}{\dfrac{1}{g_{m13}}+r_{o12}}\right)R_{\mathrm{reg}} \tag{26}$$

To simplify expression, we note

$$\xi=\frac{V_z}{\mathrm{Vdd}} \tag{27}$$

Thus

$$\xi=\frac{V_z}{\mathrm{Vdd}}=\frac{V_{\mathrm{reg}}}{\mathrm{Vdd}}\times\frac{V_z}{V_{\mathrm{reg}}}=\mathrm{PSR}1\cdot A_{\mathrm{bias}} \tag{28}$$

A_{bias} can be written as

$$A_{\mathrm{bias}}=\frac{-g_{\mathrm{bias}}g_{m10}g_{m12}}{g_{m7}g_{m11}g_{m13}} \tag{29}$$

Calculate PSR1

$$\begin{aligned}\mathrm{PSR}1&=\frac{V_{\mathrm{reg}}}{\mathrm{Vdd}}=\frac{(1-\xi)A_{\mathrm{dd}}}{1+A_{\mathrm{C1}}}\approx\frac{(1-\xi)A_{\mathrm{dd}}}{A_{\mathrm{C1}}}\\&=\frac{(1-\xi)g_{m7}g_{m11}g_{m14}}{g_{m18}(1+g_{m13}r_{o12})(r_{o17}\,\|\,r_{o19})}\\&\times\frac{1}{(g_{m7}g_{m11}g_{m17}-g_{\mathrm{bias}}g_{m10}g_{m19})}\end{aligned} \tag{30}$$

Note

$$\eta=\frac{g_{m7}g_{m11}g_{m14}}{g_{m18}(1+g_{m13}r_{o12})(r_{o17}\,\|\,r_{o19})}\times\frac{1}{(g_{m7}g_{m11}g_{m17}-g_{\mathrm{bias}}g_{m10}g_{m19})} \tag{31}$$

From equation (31) we know $\eta\ll 1$, and

$$\mathrm{PSR}1=(1-\xi)\eta \tag{32}$$

According to equation (28) and (32), PSR1 can be rewritten as

$$\mathrm{PSR}1=\frac{\eta}{1+\eta A_{\mathrm{bias}}}\approx\eta \tag{33}$$

With equation (11)(24)(31)(33), we can conclude the power supply rejection of the reference

Table 1. Comparison between this work and others

	Paper[2]	Paper [3]	Paper [5]	***This work***
process	0.25μm CMOS	0.6μm CMOS	0.18μm CMOS	0.35μm CMOS
area	0.108 mm^2	0.136 mm^2	0.186 mm^2	0.248 mm^2
Power consumption	50 μA	<20 μA	43 μA	23 μA
Operating voltage	⩾0.9 V	1.5-2V	⩾0.9 V	2.2 V~5.5 V
Output voltage	536 mV	1.2525 V	657 mV	1.210 V
Operating temperature range	0~100 ℃	0~100 ℃	0~150 ℃	-25~120 ℃
Temperature coefficient	13.4 ppm/℃	15.2 ppm/℃	10~40 ppm/℃	10~30 ppm/℃
PSR	-25.5 dB@10kHz	-70 dB@dc -42 dB@10 MHz	-55 dB@dc	-120 dB@dc -80 dB@10 kHz
Sensitive to resistive load	yes	yes	yes	no

$$\mathrm{PSR} = PSR1 * PSR2 = \frac{g_{\mathrm{bias}} g_{m11} g_{m14} \left(\frac{g_{ma1}}{2 g_{ma5}} + \frac{g_{ma2}}{g_{ma7}} \right)}{g_{m18} g_{ma3} (\beta_1 - \beta_2)(r_{oa4} \parallel r_{oa6})(1 + g_{m13} r_{o12})} \times \frac{1}{(g_{m7} g_{m11} g_{m17} - g_{\mathrm{bias}} g_{m10} g_{m19})(r_{o17} \parallel r_{o19})} \quad (34)$$

In the traditional Kujik bandgap reference, the PSR of the reference is only *PSR*2. However, here a pre-regulator has been introduced which can improve the PSR from *PSR*2 to *PSR*1**PSR*2. Fig. 6 shows the simulation curves of *PSR*1 and PSR.

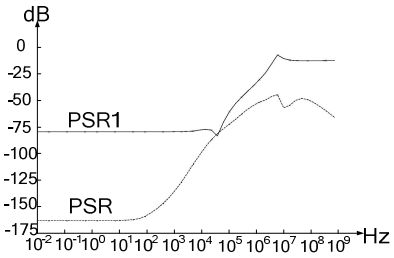

Figure 6. Simulation curve of PSR1 and PSR

V. MEASUREMENTTS AND COMPARISON

The voltage reference is designed with TSMC 0.35um CMOS process. Fig. 7 shows the photograph of this chip. Measurements show that the reference has a best temperature coefficient of only 10 ppm/℃, the PSR is -120 dB@dc and -80 dB@10 kHz, and the whole consumption is only 23 μA. Table 1 shows the comparison between this work and other papers. From the comparison, we can see that the voltage reference proposed by this paper is of excellent PSR performance, good temperature characteristics and low power consumption. In order to save one mask, high resistive resistor is not used in our design, so the area of this chip is larger than others.

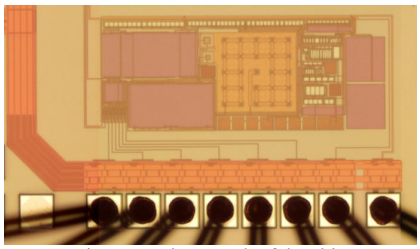

Figure 7. Photograph of the chip

REFERENCES

[1] Kujik K E, "A precision Reference Voltage Source," *Journal of Solid-State Circuits*, vol 8, no. 3, pp.222-226, June 1973

[2] Ker Ming-dou and Chen Jung-sheng, "New curvature-compensation technique for CMOS bandgap reference with Sub-1-V Operation," *Transactions on Circuits and Systems*, vol 53, no 8, pp. 667-671, August 2006

[3] Leung C Y, Leung K N and Mok P K T. "Design of a 1.5 V high-order curvature-compensated CMOS bandgap reference," Circuits and Systems, ISCAS, 2004, pp. 49-52.

[4] Hsiao Sen-wen, HuangYen-chih, Liang David, et al. "A 1.5-V 10-ppm/℃ 2nd-order curvature-compensated CMOS bandgap reference with trimming," Circuits and Systems, ISCAS, 2006, pp. 565-568

[5] Xing Xin-peng, Wang Zhi-hua and Li Dong-mei. "A low voltage high precision CMOS bandgap reference," Norchip Conrerence, 2007, pp. 1-4

[6] Zhang Ke, Guo Jian-min, Kong Ming, et al. "A programmable CMOS voltage reference based on a proportional summing circuit," ASICON ,2007, pp. 534-537

[7] Xiao Du, Li Wei-min, Zhu Xiao-fei, et al. "A curvature-compensated bandgap reference with improved PSRR," ASICON, 2005, pp.529-533

[8] Zhang Chuan, He Shu-zhuan, Zhu Ying, et al. "A high precision CMOS bandgap reference with second-order curvature-compensation," ASICON ,2007, pp. 553-556

[9] Tham K M, Nagaraj K. "A low supply voltage high PSRR voltage reference in CMOS process," *Journal of Solid-State Circuits*, vol 30, no 5, pp. 586-590, May 1995

[10] Ashrafi S F, Atarodi S M, Chahardori M. "New low voltage, high PSRR, CMOS bandgap voltage reference" SOC Conference, 2008, pp. 345-348

[11] Hoon S K, Chen Jun, Maloberti F. "An improved bandgap reference with high power supply rejection" Circuits and Systems, ISCAS, 2002, pp. 833-836

[12] Song B S, Gray P R. "A precision curvature-compensated CMOS bandgap reference". *Journal of Solid-State Circuits*, vol 18, no 6, pp. 634-643, December 1983

[13] Tsividis Y P. "Accurate analysis of temperature effects in I_C-V_{BE} characteristics with application to bandgap reference sources". *Journal of Solid-State Circuits*, vol 15, no 6, pp.1076-1084, December 1980

[14] Gong Wen-chao, Wang Yi, Cui Chuan-rong, etc, "Novel CMOS current reference with high power-supply rejection ratio", *Journal of Zhejiang University(engineering Science)*, vol 9, 2008