20A Trapezoidal Reference Current Pulse Generator for the Evaluation of Current Transducers

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***Abstract*—The design and evaluation of a high precision pulsed current source for the dynamic characterisation of shunts and burden resistors is described. This generator uses a set of current mirrors based on ratio resistor networks to amplify a 10 mA DC current reference and to subsequently generate a pulse by means of a complementary pulse approach. Simulations and preliminary results of the complementary pulse circuit will be presented.**

I. Introduction

In order to increase the luminosity of the proton beams injected into the LHC at CERN, a new linear accelerator (LINAC4) is being built to replace the old injector (LINAC2). LINAC4 is a $160\,\mathrm{MeV}$ pulsed beam, $\mathrm{H}-$ accelerator. Its magnets' current will be pulsed at approximately $2\,\mathrm{Hz}$ repetition rate with about $1\,\mathrm{ms}$ rise times and $2\,\mathrm{ms}$ pulse width. Current stability during the pulse flat-top and pulse-to-pulse flat-top repeatability are required to be better than $100\,\mathrm{ppm}$. These requirements pose a power converter control and measurement challenge. Characterisation of the current measuring devices used in the power converters is an important part of this challenge. Current measurement transducers are normally specified in DC and at specific frequencies. Time domain characterisation is not readily available, making it difficult to estimate the device's pulse response. For a pulsed application with requirements given in the time domain, a time domain characterisation is more appropriate. For this purpose, two methods can be considered: the reference device method and the reference pulse method. In the first, the *DUT* is compared against a device with a well-known response, accurate enough to be used as a reference. The second one does not require a reference measuring device and relies on a reference source to produce a well-known, accurate pulse. The method chosen for this application was the latter. The main reasons are to avoid the use of a second measuring channel requiring synchronised acquisition and mathematical operations for scaling the outputs. In addition, this option would require multiple reference devices to satisfy requirements for different current ranges. The effect of thermal dynamics and *power coefficient* [1] are also a concern as it is difficult to estimate their impact for a pulsed application with such small duty cycles. A market survey of pulsed current sources concluded that none were available or completely satisfactory; the $100\,\mathrm{A}$, $100\,\mathrm{kHz}$ transconductance amplifier based on NIST design [2], [3], which was also considered, has, indeed, an estimated temperature coefficient as high as $5\,\mathrm{ppm}/^{\circ}\,\mathrm{C}$. As a consequence, a project was launched to develop this *pulsed calibrator* which also envisages a future use in faster applications. This development uses ratiometric techniques based on commercial low-cost thin film resistor arrays, succesfully utilised by CERN and METRON, to amplify and then pulse a well-known, accurate DC current [4]. This $10\,\mathrm{mA}$ DC is produced by the same reference device which is at the heart of the CERN power converters calibration architecture, the *PBC* [5], [6], [7].

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II. Proposal

A. Requirements and working principle

The pulsed calibrator is a programmable reference pulse current generator which is intended for the evaluation of current measuring devices, in particular, burden resistors and shunts. For this reason, the required compliance voltage is limited to $2\,\mathrm{V}$. This does not exclude the future use of a booster device to increase compliance voltage which would allow the testing of zero flux type of transducers. The pulsed calibrator has five current output values: $0.5\,\mathrm{A}$, $1\,\mathrm{A}$, $5\,\mathrm{A}$, $10\,\mathrm{A}$, $20\,\mathrm{A}$. Parameters such as flat-top duration, repetition rate and rise time are configurable. A modular construction, consisting of 4 current modules ($0.5\,\mathrm{A}/1\,\mathrm{A}$, $5\,\mathrm{A}$, $5\,\mathrm{A}$, $10\,\mathrm{A}$), facilitates calibration and inter-comparison; the nominal currents of the modules match the different full scales of the *CDC* (CERN DCCT Calibrator) [5]: $1\,\mathrm{A}$, $5\,\mathrm{A}$ and $10\,\mathrm{A}$. The $0.5\,\mathrm{A}$ current level can either be calibrated by means of the *CDC* at half scale or by means of the *PDC* (CERN Portable DCCT Calibrator) which amplifies the reference $10\,\mathrm{mA}$ DC current [4] by a factor of 50 and it is based on the same principle, which will be detailed in II-B. Actual values of the output currents will not be trimmed; the design is only focused on stability and precision performance and the device will therefore require calibration. Transducer performance in pulsed accelerator applications

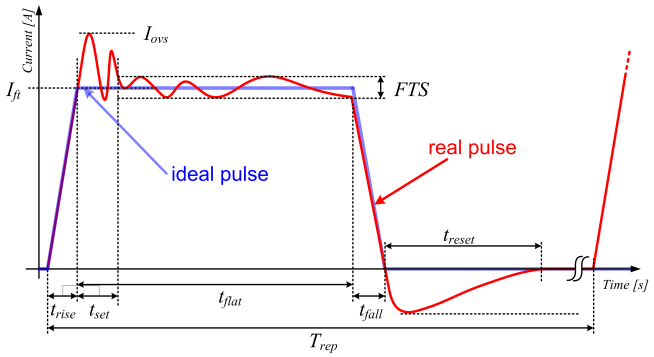

Fig. 1. Pulse parameters.

(such as LINAC4) is normally only important during during the flat-top of the pulse, as this corresponds to the beam passage. The main performance requirements for the pulsed calibrator are summarised in Tab. I and graphically presented in Fig. 1.

TABLE I
MAIN PERFORMANCE REQUIREMENTS OF THE CALIBRATOR

Flat-Top Duration t_{flat}	100 μs to 10 ms
Minimum t_{rise} / t_{fall}	100 μs
Repetition Period T_{rep}	20 ms to 1 s
Flat-Top Stability FTS	40 ppm
Settling Time t_{set}	$<$ 100 μs ($t_{flat} >$ 2 ms) $<$ 25 μs ($t_{flat} <$ 2 ms)
Flat-Top Average Pulse-to-Pulse Repeatability	$<$ 10 ppm
Flat-Top Average Pulse-to-Pulse 1 h Repeatability	$<$ 10 ppm
Flat-Top Average 1 year Stability	$<$ 20 ppm
Temperature Coefficient	$<$ 2 ppm /° C
Flat-Top Noise (rms)	$<$ 10 ppm (10 Hz - 100 Hz) $<$ 20 ppm (100 Hz - 10 kHz) $<$ 30 ppm ($>$ 10 kHz)

As previously mentioned, the reference current pulse is generated from a high precision DC current source [4]. This is done by using the complementary pulse approach detailed in subsection II-C. The reference current is injected into the *primary* of the ratio network assembly. The voltage across the primary is sensed and used to generate the amplified secondary current by means of two current paths, both pulsed and complementary to each other, in such a way that the *secondary* of the ratio network assembly always sees a DC current. The ratio between *primary* and *secondary* resistors corresponds to the current amplification. The modular approach requires the generation of 4 copies of the reference 10 mA DC current, one for each identical module, without significant degradation of performance. This is also achieved using ratio network based current mirrors as shown in Fig. 2.

B. Ratio Networks Current Amplifier

Since a current amplifier with a predictable pulse response (to handle transients), excellent TC matching and reasonable cost was needed, it was decided to use thin film arrays of same

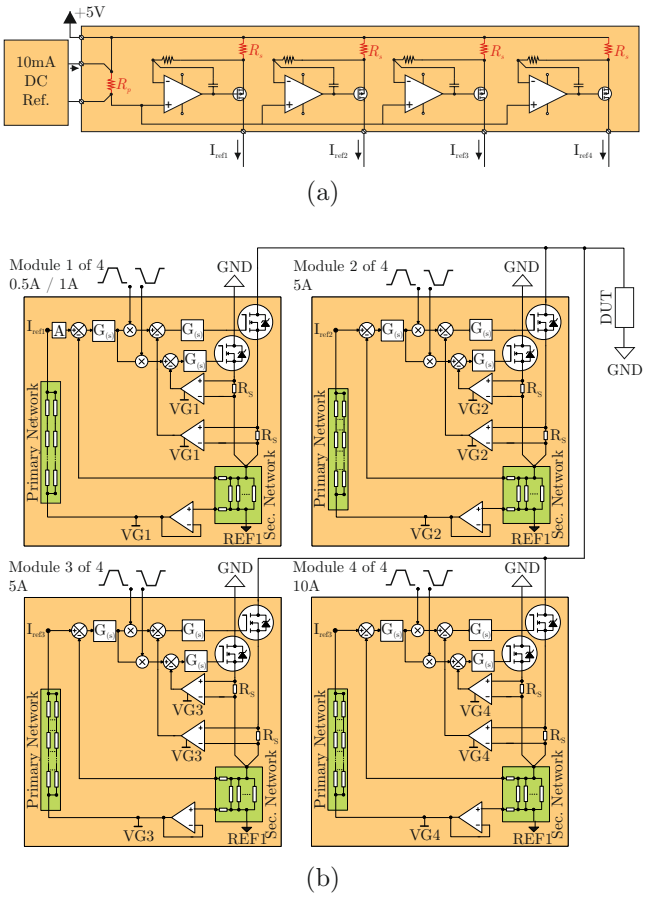

Fig. 2. Block diagram of the pulsed calibrator.

value elements in series/parallel configurations. The idea behind the ratiometric solution is that accurate, stable ratios can be implemented from low-cost array resistors using averaging techniques. Metron had previously investigated the thin film arrays performance for CERN and it was apparent that they would make a good choice for this application. The prior work had shown that the TC matching of resistances dissipating different power levels was not a trivial problem. Because of the parabolic nature of the resistance/temperature characteristic matching at room temperature is not valid when the power levels and thus the temperatures, differ in use. Each resistance will be operating on a different tangent of the parabola.By using arrays of identical thin film resistance elements, it is possible to get excellent thermal coupling between unpowered and powered elements on the same substrate and in the same package. However, multiple arrays are needed to handle the power levels at high currents and the *trick* is to get networks of arrays, whose individual TCs may be quite different, to operate together with the same matching performance as for the elements in a single array. The arrays chosen were 8 resistor arrays on single substrates in SOIC packages due to their cost, availability and TC matching performance. For a total package thermal resistance to ambient R_{th} by dissipating power in individual elements and measuring the consequent

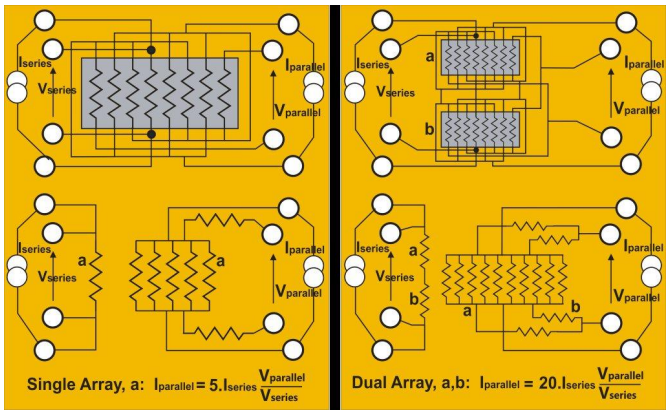

Fig. 3. Connecting multiple arrays to make networks.

change in value of other elements it was found that the thermal resistance between adjacent elements is about $R_{th}/20$. Thus if some elements are powered to cause the package temperature to rise by, say, $50°$ C then the difference between powered and unpowered elements will be less than $3°$ C. It was decided to make networks of ten arrays on PCBs and then use these networks in parallel as required to provide the power handling capabilities of Fig. 2. To fabricate the networks requires careful wiring of the arrays to maintain the excellent matching, actually, the statistical averaging of the multiple networks tends to attenuate the random element variations within the arrays. Fig. 3 shows how a single array is used and how two can be wired together in a way that preserves the element matching and allows for simple paralleling of the high current path. Note also that current flow in elements of the parallel path is in opposing directions to minimise inductance. For a current amplifier, the reference $10\,\mathrm{mA}$ PBC current creates a voltage, V_{series}, across the series path of the array. The amplifier feedback servo loop forces current through the parallel path until a required ratio between V_{series} and $V_{parallel}$ is achieved, this ratio being that to provide the required output current from the network. Fig. 3 also shows the transfer function equation for the simple cases of a single array network and a dual. In general, the current gain for a n array network is given by:

$$I_{parallel} = 5\ n^2 I_{series} \frac{V_{parallel}}{V_{series}} \qquad (1)$$

and if V_{series} is attenuated in a precision voltage divider array network within the servo loop, then virtually any ratio is possible and will better the matching performance of the elements in single arrays.

C. Complementary Pulse Approach

The basic idea of the complementary pulse approach is to keep the current in the ratio networks constant, in order to safely neglect any dynamic effects (including the effect due to power coefficient [1]) therefore ensuring the performance of the system is independent from output pulse parameters. Once the ratio networks have reached a steady state thermal condition, the current is then steered from the DUT path (i_{OUT}) to a *dummy* path (i_{COMP}), as shown in Fig. 4. This is done by means of two different loops: one external loop that controls the value of the DC current in the *secondary* of the ratio network *amplifier*, and two internal loops (one for each branch) controlling the steering from one branch to the other; the loop arrangement is shown in Fig. 2 (b) for each one of the modules. As the external loop controls the sum of the current of the two branches ($i_{DC} = i_{OUT} + i_{COMP}$), and $i_{COMP} = 0$ (i_{COMP} MOSFET not conducting during the flat-top of i_{OUT}), the asymmetries and nonlinearities of the internal loops (such as differences between the sense resistors of each branch and the quadratic transfer of the output devices) do not affect the final i_{OUT} pulse flat-top precision. However, these parameters could affect the error in the edges and the settling time of the output pulse. The mismatch between the sense resistors of the internal loops will produce an error in the rising and falling edges of the pulse; even though the error in the edges of the pulse is not a critical parameter, it can be reduced by selecting low tolerance resistors, and attaching them to the same heatsink in order to match the operating temperature of the two resistors. On the other hand, the quadratic transfer of the output MOSFETs could produce an increase in the settling time of the output current if the loop gain is not enough.

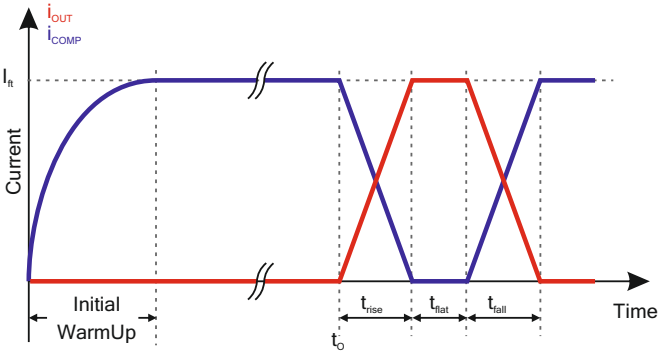

Fig. 4. Complementary pulse principle

One drawback of the complementary pulse approach is that each module is effectively driving a DC current and therefore power dissipation is significant. The DC power dissipation was an important factor in the choice of the resistance value for the resistor arrays, which is a trade-off between power dissipation and *SNR* (the smaller the values the smaller the voltage to be sensed). For the current mirrors and the $0.5\,\mathrm{A}\,/1\,\mathrm{A}$ module the power constraint is not really critical; the chosen resistor array is the Vishay TOMC with values $1\ k\Omega$ and $100\ \Omega$ respectively. Their parameters are summarized in table II. For the high current modules the best compromise between power dissipation and *SNR*, easily available on the market as a low-cost *off-the-shelf* component with the required ratio stability specifications was chosen to correspond to a resistance value of $26\ \Omega$, in the form of IRC's tantalum nitride film on silicon resistor arrays; its parameters are summarised in table III. Even

TABLE II
PARAMETERS OF THE RESISTOR ARRAYS USED FOR THE CURRENT MIRRORS AND THE 0.5 A /1 A MODULE.

Absolute TCR	$\pm 25\,\mathrm{ppm}/^\circ\mathrm{C}$
Tracking TCR	$\pm 5\,\mathrm{ppm}/^\circ\mathrm{C}$
Absolute Tolerance	$\pm 0.1\,\%$
Relative Tolerance $1\,\mathrm{k}\Omega$	$\pm 0.025\,\%$
Relative Tolerance 100Ω	$\pm 0.1\,\%$
Element Power Rating @ 70° C	$100\,\mathrm{mW}$
Package Thermal Resistance	$106.67^\circ\,\mathrm{C}\,/\,\mathrm{W}$

TABLE III
PARAMETERS OF THE RESISTOR ARRAYS USED FOR THE 5 A AND 10 A MODULES.

Absolute TCR	$\pm 50\,\mathrm{ppm}/^\circ\mathrm{C}$
Tracking TCR	$\pm 10\,\mathrm{ppm}/^\circ\mathrm{C}$
Absolute Tolerance	$\pm 0.5\,\%$
Relative Tolerance	$\pm 0.25\,\%$
Element Power Rating @ 70° C	$100\,\mathrm{mW}$
Package Thermal Resistance	$45.83\,^\circ\,\mathrm{C}\,/\,\mathrm{W}$

with this resistance value, the low voltage level across the *secondary* requires special attention in particular in the choice of the sensing amplifiers. As the main concern is to reduce the thermal coefficient of the sensed voltage, zero drift amplifiers were used.

III. Simulations and Experimental Results

Two types of experimental tests were carried out to assess the performance of the system: static tests and dynamic tests. The static tests aim at verifying the stability and temperature coefficient of the stages that can affect the overall accuracy of the pulse flat-top, such as the $10\,\mathrm{mA}$ reference current mirrors and the ratio networks modules. On the other hand, the dynamic tests allow the evaluation of the time domain parameters of the output pulse, such as initial transients, settling time and pulse-to-pulse repeatability.

A. Static measurements. Current Mirrors

Fig. 5 shows the test setup for the current mirrors' stability; the *DUT*, a prototype board implementing the block diagram of Fig. 2 (a), is placed inside a climatic chamber, each output is then compared with a PBC in a back-to-back configuration. This configuration allows comparing two current sources of the same magnitude by connecting them in anti-parallel and measuring the difference current with a large value shunt resistor [4]. By placing the PBCs and shunt resistors outside the oven (ambient temperature T_{amb} is controlled within a variation of $\pm 1°\mathrm{C}$) the response of the DUT to temperature cycles can be evaluated. The initial errors and temperature coefficients of the four $10\,\mathrm{mA}$ current mirrors are shown in Fig. 6. The temperature was cycled from $T_0 = 30^\circ\,\mathrm{C}$ to $T_1 = 50^\circ\,\mathrm{C}$, with a $10\,\mathrm{h}$ rise time and $15\,\mathrm{h}$ period. The worst case temperature coefficient (evaluated as the slope of the curves) is $TC = -0.14\,\mathrm{ppm}/^\circ\,\mathrm{C}$ and no nonlinearities are observed. Some additional drift, indicated by the distance in the y direction of each curve with respect to the others, can be observed in the first cycle for mirrors 1, 2 and 4 but it is nevertheless smaller than $1\,\mathrm{ppm}$. Another prototype board (Fig. 2 (a)) was also tested and results show different initial errors, as expected, but a very similar TC of about $-0.1\,\mathrm{ppm}/^\circ\,\mathrm{C}$; this agreement confirms the principle of the design (the measured TC is only a small part of the target temperature coefficient, tab. I).

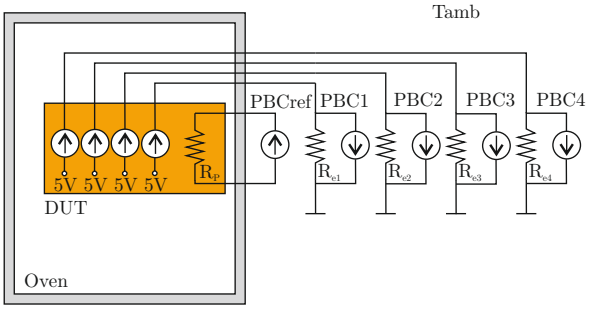

Fig. 5. Test setup for the current mirrors evaluation.

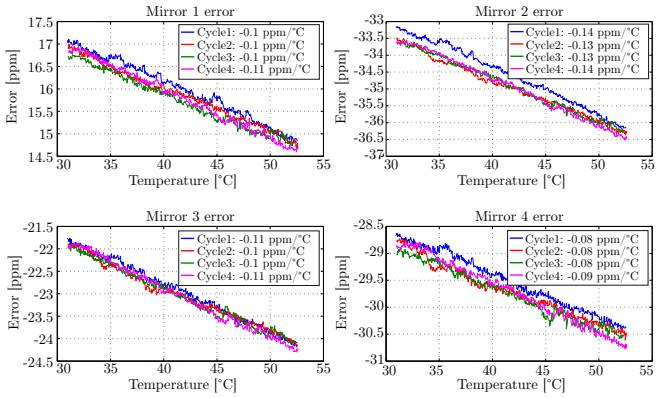

Fig. 6. Initial errors and temperature coefficients of the four $10\,\mathrm{mA}$ current mirrors.

B. Static measurements. Ratio Networks

Fig. 7 shows the test setup for the ratio networks' evaluation. The ratio networks are placed inside a climatic chamber, and the voltage drop across both *primary* and *secondary* produced by two reference current sources (*CDC* and *PBC*) are recorded with two HP3458A DVMs. The ratio error is defined as:

$$E_{[ppm]} = \left(\frac{n V_{R_P}}{V_{R_S}} - 1 \right) \times 10^6 \qquad (2)$$

where $n = 1$ for the $5\,\mathrm{A}$ modules and $n = 2$ for the $10\,\mathrm{A}$ module. The ratio error during temperature cycles for one of the $5\,\mathrm{A}$ modules is shown in Fig. 8 (top) and its temperature coefficient in Fig. 8 (bottom). The temperature is cycled from $T_0 = 23^\circ\,\mathrm{C}$ to $T_1 = 53^\circ\,\mathrm{C}$ in periods of $15\,\mathrm{h}$ with $10\,\mathrm{h}$ rise time. The time span of approximately 5 days allows an evaluation of the ratio stability by looking at the *maxima* and the *minima* of the recorded waveforms: the ratio drift over time estimated by this method is approximately $1.2\,\mathrm{ppm}$

neglecting the first cycle which is affected by thermal settling (Fig. 8). The resulting worst case temperature coefficient is $-0.13\,\mathrm{ppm}\,/^\circ\,\mathrm{C}$. The same test was repeated later with 2 temperature cycles and the results confirmed the TC and drift estimations above. During the test, the impact of thermal e.m.f.s on the TC was evaluated by reversing the current on both primary and secondary. Fig. 9 shows estimations of the primary and secondary thermal e.m.f.s (estimations do not take into account DVM offsets, but ambient temperature is constant to within $\pm 0.2^\circ\,\mathrm{C}$ in the laboratory where these tests were performed, so TCs are entirely due to thermal e.m.f.s). During the *slow* temperature increases, the secondary thermal e.m.f. remains constant whereas the primary shows a slightly positive TC; this induces an error of approximately $\pm 0.025\,\mathrm{ppm}\,/^\circ\,\mathrm{C}$ when evaluating the TC without *current reversal*. The second 5 A module was also tested, showing a temperature coefficient and a drift comparable with the first as depicted in Fig. 10. Moreover, thermal e.m.f.s and their respective TCs were consistent. The temperature, as reported in Figs. 8 to 10, is approximately $4^\circ\,\mathrm{C}$ higher than the programmed temperature because temperature was independently measured close to the ratio networks board. This was housed in a cardboard box with a foam top cover to avoid thermal e.m.f.s generated by temperature gradients caused by the climatic chamber's fan.

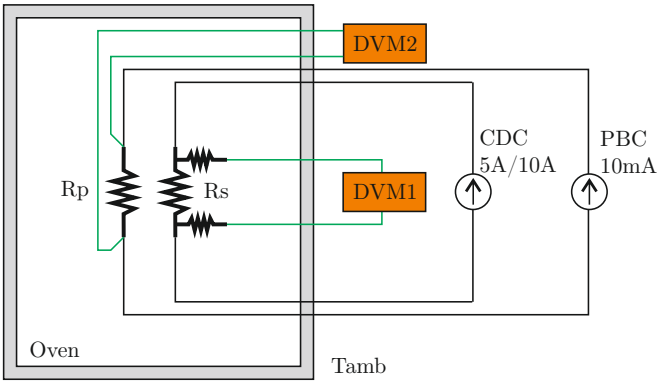

Fig. 7. Test setup for the ratio networks evaluation.

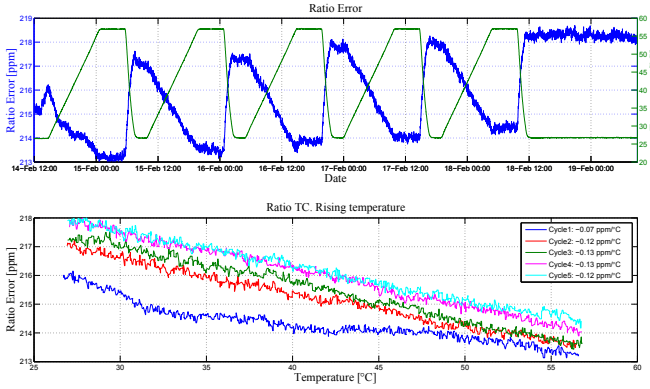

Fig. 8. Error of the ratio of the first 5 A module under temperature cycles (top) and its temperature coefficient (bottom).

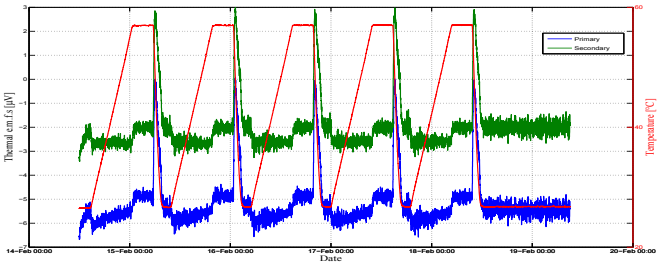

Fig. 9. Residuals of the *current reversal* evaluation of the ratio error.

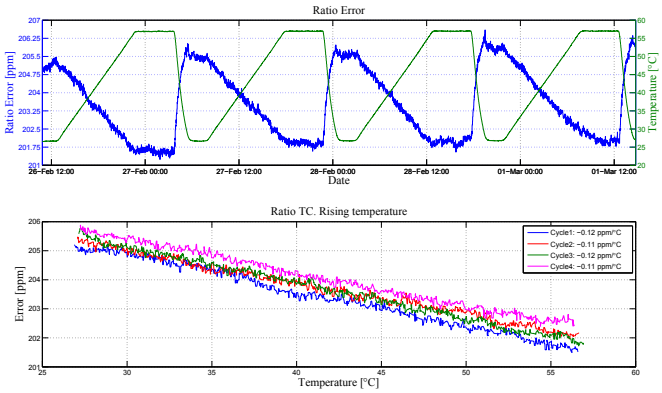

Fig. 10. Error of the ratio of the second 5 A module under temperature cycles (top) and its temperature coefficient (bottom).

Fig.11 shows the test results for the 10 A module. In this case, the measured temperature is approximately $8^\circ\,\mathrm{C}$ higher than the programmed temperature due to increased power dissipation w.r.t. 5 A modules. The observed drift is approximately 1.5 ppm and the observed worst case temperature coefficient is $-0.21\,\mathrm{ppm}\,/^\circ\,\mathrm{C}$. In this case the error due to thermal e.m.f.s is more pronounced and amounts to approximately $\pm 0.07\,\mathrm{ppm}\,/^\circ\,\mathrm{C}$. Thermal e.m.f.s contribute oppositely for voltage measurements of the ratio with positive and negative test currents giving reversal differences of $\pm\ 3 - 5\,\mathrm{ppm}$ and circa $\pm 15\,\mathrm{ppm}$ for the 5 A and 10 A modules respectively. Calibration must therefore be performed with *current reversal*.

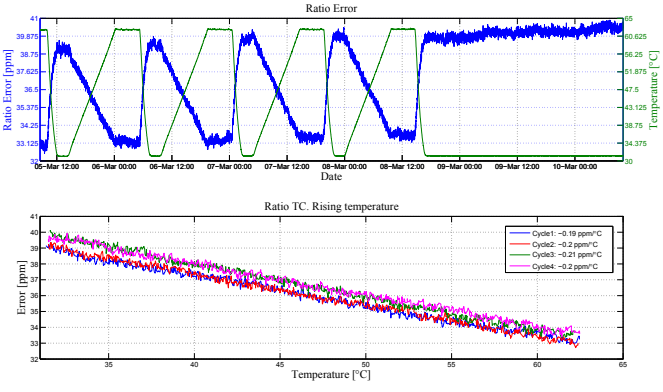

Fig. 11. Error of the ratio of the 10 A module under temperature cycles (top) and its temperature coefficient (bottom).

C. Dynamic tests. Transient behavior

Dynamic behaviour of the 1 A output pulse was characterised by means of an NI PXI-4071 DVM, sampling at 1.8 MS / s in the 1 V range in order to correctly capture the transient at the end of rise time. As the resolution at this sampling frequency is only slightly better than 10 bits, several pulses were acquired and then averaged to increase resolution. The output current is measured by recording the voltage across a 1Ω HITEC reference burden [8], and then compared with the SPICE simulation results. Other tests with different reference resistors are being performed and will be presented in the final paper. Fig. 12 (a) shows the rising edge of the pulse. The initial transient is produced by the MOSFET going out the *cutoff* region and is not relevant since the only interest for the application is in the flat-top of the pulse. Fig. 12 (b) shows the settling of the pulse, the response presents an overshoot of 0.8 %, and it then settles to the desired ±20 ppm error band in approximately 30 μs.

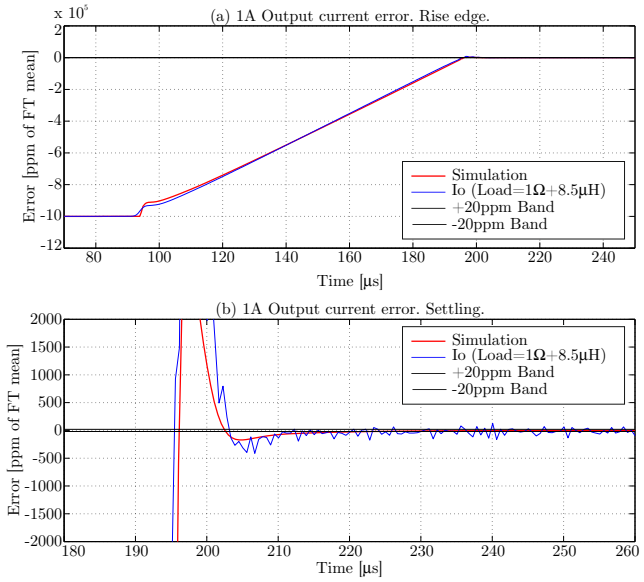

Fig. 12. Average of the acquired output pulses and simulation results superposed.(a) Rising edge. (b) Settling to ±20 ppm.

For the pulse-to-pulse assessment, an NI PXI-4462 Digital Signal Analyser was used with a sampling rate of 200 kS / s; the pulse-to-pulse repeatability is evaluated by taking the average value of each pulse's flat-top and comparing it with the previous one. Using a sufficiently small repetition period, it is safe to assume the ambient temperature constant between adjacent pulses and neglect any error due to the poorer performance of the NI PXI-4462 in terms of stability and temperature coefficient with respect to the NI PXI-4071. Fig. 13 shows the pulse-to-pulse error for the 1 A output, with a flat-top length $t_{flat} = 1$ ms and 60 ms repetition period. The overall acquisition lasted approximately 42 min corresponding to about 42000 pulses. The standard deviation of the pulse-to-pulse error is $\sigma_{p-p} = 3.86$ ppm. Using a coverage factor of 2, the pulse-to-pulse repeatability is then $Rep_{p-p} = 2\sigma_{p-p} = 7.72$ ppm. For comparison purposes, the same test has been performed with a purely DC voltage using a Fluke 732A Zener 1 V voltage reference; for this test, the obtained standard deviation was $\sigma_{p-p} = 1.6$ ppm.

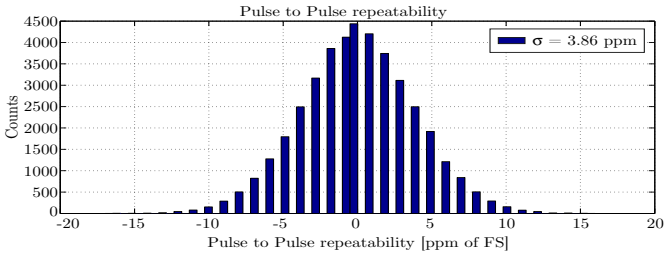

Fig. 13. Pulse-to-pulse repeatability of the 1 A flat-top average.

IV. Conclusion

The design and evaluation of a high precision pulsed current source for the dynamic characterisation of current transducers has been described. The proposed solution is currently suitable only for shunts and burden resistors, but it has been designed so that it could be used with a compliance voltage booster device which would allow the testing of zero flux type of transducers. The working principles of the ratio networks' current amplification and complementary pulse forming have been detailed as well as its modular design which simplifies calibration and inter-comparison. Preliminary results, in close agreement with simulation results, have been presented and show that the proposed design is able to meet the demanding requirements of the instrument.

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