A 0.662ppm/℃ High PSRR CMOS Bandgap Voltage Reference

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Abstract

A novel low temperature coefficient (TC) high power supply rejection ration (PSRR) CMOS bandgap voltage reference (BGR) is implemented in TSMC 0.35μm CMOS Technology. This design can be applied to voltage regulators particularly used in implanted chips. The temperature compensation is optimized by adjusting proper ratio of resistances which have opposite TC. Its PSRR is improved by using cascode current mirrors and adopting an independent current source structure. The design operates within a range of 2.3V to 5.5V and has a line sensitivity of 0.116%/V. At room temperature, the reference voltage is 1.14V and has a measured TC of 0.662ppm/℃ in a wide temperature range of -40℃ to 125 ℃. The circuit performs a PSRR property of 96dB@1KHz and more than 30dB@1MHz with a start-up time below 5μs.

1. Introduction

As the essential block of analog and mixed-signal circuits, BGRs are widely used in analog to digital converters, DC-DC chips and noise sensitive wireless transceivers for their high accuracy and temperature independence. Therefore low TC high PSRR BGR has been a research hot spot since his first birth.

Traditional BGR circuit is first-order temperature compensated. It achieves the close to zero TC by a linear combination of the base-emitter voltage V_{BE} with a negative TC and the different of two base-emitter voltages $\triangle V_{BE}$ with a positive TC. While V_{BE} is nonlinear with temperature and can be given by [1]

$$V_{BE} = V_G(T_0) + \frac{T}{T_0}\cdot[V_{BE}(T_0) - V_G(T_0)] - (\eta - m)V_T \ln\left(\frac{T}{T_0}\right) \quad (1)$$

where V_G is the bandgap voltage of silicon extrapolated at 0K, T_0 is the reference temperature, η is a temperature constant depending on the technology, m is the order of the temperature dependence of the collector current, and V_T is the thermal voltage. Therefore, the conventional BGRs cannot meet the requirement of high precision applications. To improve the TC of BGR, many high-order temperature compensation techniques have been reported, such as piecewise linear curvature correction technique [2], exponential temperature compensation technique [3], quadratic temperature compensation technique [4] and so on. What's more, the property of high PSRR is also extremely required in BGRs for precision circuits over a wide frequency range. As already known, there are various techniques that improve PSRR like cascode technique [5], pre-regulated circuit [6], and pseudo floating voltage source technique [7]. In general, these proposed BGRs with well high PSRR have a relatively high TC. So, the BGRs with low TC and high PSRR should be still designed for the demand of high precision.

In this paper, a novel low TC high PSRR CMOS BGR is carried out using the TSMC 0.35 μm CMOS technology. The low TC is realized by adjusting opposite TC resistances to eliminate the nonlinearity of V_{BE}. The high PSRR is achieved by using cascode technique and independent current source structure.

The reminder of this paper is organized as follows. A detailed description of the proposed BGR is presented in section 2. Section 3 shows the simulation results. Finally, the conclusions are described in section 4.

2. Improved bandgap voltage reference

2.1 The realization of temperature compensation

The proposed BGR is shown in Figure 1, including start-up circuit, independent current source, bandgap core, operational amplifier and bias circuit. Bandgap core circuit comprises of temperature compensated circuit and AMP2. To ensure the absolute symmetry of Q1 and Q2 in layout design, the emitter area of Q1 is 8 times as much as of Q2. PMOS transistors MP4~MP9 form a high swing cascode structure, which increases the output resistance, reduces mismatch current by channel length modulation, thereby improves the accuracy of the current mirror. Resistances R1a, R1b, R1c, and R3 are implemented in high-resistive poly resistor (HpolyR) while R2a, R2b, R2c are P-diffusion resistors (PdiffR). Like the conventional BGRs, the high gain operational amplifier AMP2 enforces the voltages of nodes A and B to be equal. So a proportional-to-absolute-temperature (PTAT) loop is formed by Q1, Q2, and R3. The PTAT current I is, thus, generated

$$I = \frac{V_{BE2} - V_{BE1}}{R_3} = \frac{V_T \ln 8}{R_3} \quad (2)$$

For perfect matching in layout, the chosen value of resistors in the room temperature is given by

$$R1c = \lambda R1a = \lambda R1b, R2c = \lambda R2a = \lambda R2b \quad (3)$$

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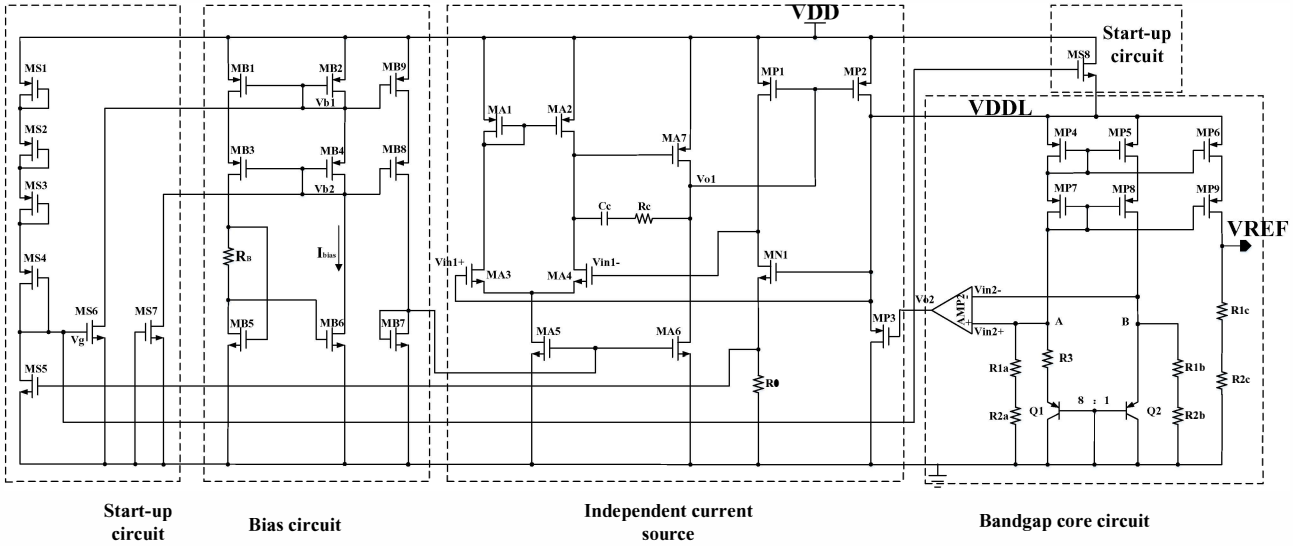

Figure 1. The schematic of proposed bandgap reference

So the output voltage V_{REF} can be given by

$$V_{REF} = \lambda\left(V_{BE2} + V_T \ln 8 \frac{R1b}{R3} + V_T \ln 8 \frac{R2b}{R3}\right) \quad (4)$$

where $\frac{R1b}{R3}$ is temperature independent constant since they are HpolyR. However, the ratio $\frac{R2b}{R3}$ is temperature dependent due to different types of resistors. R2b is a PdiffR which has a positive TC set as K_{pdiff} and R3 is a HpolyR which has a negative TC set as K_{poly}. So the Taylor series expansion of $\frac{R2b}{R3}$ can be represented by

$$\frac{R2b(T)}{R3(T)} = \frac{R2b(T_0)}{R3(T_0)}\left[1 + K_{pdiff}(T - T_0)\right] \times \left[1 + K_{poly}(T - T_0) + {K_{poly}}^2(T - T_0)^2\right] \quad (5)$$

where $K_{pdiff} > 0, K_{poly} < 0$. Combining with equations (1), (4) and (5), the high order term TC of V_{BE2} can be well offset by properly choosing the ratio $\frac{R1b}{R3}$ and $\frac{R2b}{R3}$.

2.2 The realization of High-PSRR

To achieve high PSRR, bandgap core is supplied from an independent current supply to shielding the effects of power supply noise. Independent current source circuit [8] is illustrated in Figure 1. It sources current to main branch and MP3 transistor sinks the reminder. This current receives a feedback signal from bandgap core to have high power supply independence. Transistors MP6 and MP9 are responsible to provide the regulated voltage (VDDL) for the bandgap core circuit.

The cascode current mirrors in bandgap core circuit are also enhanced PSRR which leads to less fluctuation in the branch's current and thus in V_{REF}.

The bias circuit is composed of MB1~MB6 and R_B. PMOS transistors MB1~MB4 constitute the cascode current mirror structure and realize 1:1 current copy. So the bias current I_{bias}, as shown in Figure 1, can be get

$$V_{GS5} - V_{GS6} = I_{bias} R_B \quad (6)$$

And the saturation current I_{sat} can be given by

$$I_{sat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \quad (7)$$

where μ_n is electron mobility, C_{ox} is unit area gate-oxide capacitance.

Combing (6) and (7), the I_{bias} can be written as:

$$I_{bias} = \frac{2}{\mu_n C_{ox} {R_B}^2}\left(\sqrt{\left(\frac{L}{W}\right)_5} - \sqrt{\left(\frac{L}{W}\right)_6}\right)^2 \quad (8)$$

With the equation (8), it is clear that I_{bias} is independent of the supply voltage. Thus, the PSRR of the proposed BGR can be enhanced. The bias current sources current to the two stage operational amplifier. This operational amplifier must be designed to be a low noise and low offset opamp in addition to having a high frequency bandwidth in order to guarantee the expected PSRR. There the opamp used miller compensation structure including Cc and Rc in order to ensure the stability of the loop.

2.3 Start-up circuit design

The proposed BGR has two possible equilibrium points, so a start-up circuit is necessary. It is shown in Figure 1, including MS1 ~ MS8. MS1 ~ MS4 are four diode connected PMOS transistors. When the circuit begins to power on, MS1 ~ MS4 are gradually switched on as well as the gate voltage of MS6 ~ MS8 Vg increases. Then MS6, MS7 forced Vb1, Vb2 to reduce and pmos transistors start turn on, the system start working. The start-up current flowing through MS8 is injected into bandgap core circuit, which makes the point voltages quickly set up to close to the static working point，reduces the start-up time. Then the circuit will be driven to the desired stable. The gate voltage of MS5 is high and MS5 conducts, pulls down the voltage Vg and makes MS6 ~ MS8 to be cut-off. Then the start-up circuit will turn off and have no influence on the steady state of the circuit.

3. Simulation result

The proposed low TC high PSRR BGR shown in Figure 1 has been validated with TSMC 0.35μm CMOS process with a 3.3V power supply voltage. Figure 2 shows the TC of the BGR. At room temperature, V_{REF} is 1.14V and the measured TC of BGR is 0.662ppm/℃ with temperature range from -40℃ to 125℃.

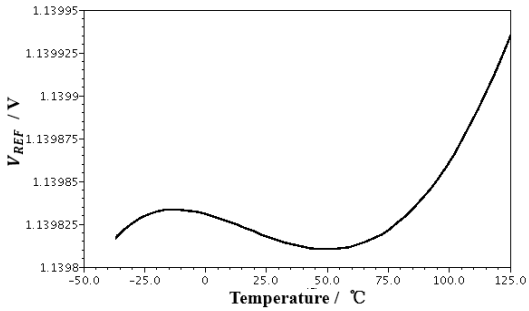

Figure 2. Temperature cofficient of the proposed BGR

The proposed BGR achieves a PSRR of 96dB@1KHz, and greater than 30dB@1MHz shown in Figure 3.

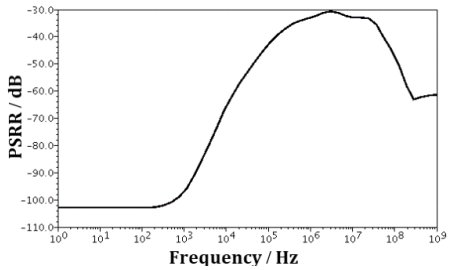

Figure 3. Measured PSRR at room temperature

Figure 4 is the start-up time of the proposed BGR. The power is on 15us later. After 5us, the reference will attain a stable value.

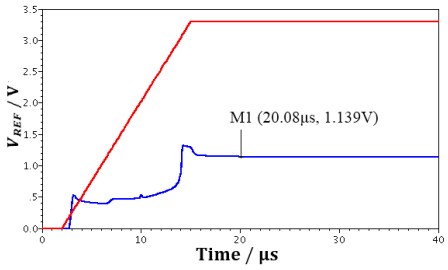

Figure 4. The start-up procedure for the proposed circuit

The measured supply dependence at room temperature is shown in Figure 5. In the supply voltage range from 2.3V to 5.5V a mean V_{REF} of 1.14V is generated, and the line sensitivity is about 0.116%/V.

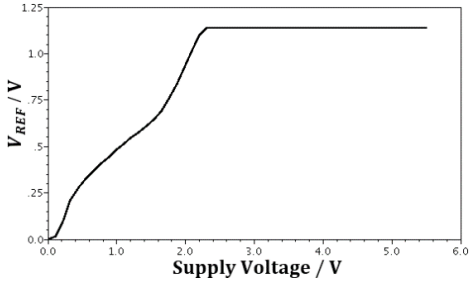

Figure 5. Measured V_{REF} as a funtion of power supply

4. Conclusion

In this work, an ultra-low TC high PSRR CMOS BGR has been presented. By adjusting the ration of different resistances, a TC of 0.662ppm/℃ is realized over a wide temperature range of 165℃ (-40℃ ~ 125℃). The inner independent current source provides a local supply voltage less sensitive to the power supply voltage for bandgap core. PMOS cascode current mirrors are used here to further improve PSRR. Simulation results show that the PSRR is 96dB@1KHz and more than 30dB@1MHz. The line sensitivity was 0.116%/V in the power supply range of 2.3V-5.5V. The start-up time is only 5μs at room temperature. Implemented and verified in TSMC 0.35μm CMOS technology, the proposed circuit can be well used for power management in high-standard embedded chips.

Acknowledgments

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