AN ACCURATE CURRENT SOURCE WITH ON-CHIP SELF-CALIBRATION CIRCUITS FOR LOW-VOLTAGE DIFFERENTIAL TRANSMITTER DRIVERS

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ABSTRACT

An accurate CMOS current source for current-mode low-voltage differential transmitter drivers has been designed and fabricated. It is composed of binary weighted current mirrors with built-in switch-cap based self-calibration circuits. Experimental results show that it achieves the specified ±1% accuracy with 16% reference current variation, 42% power supply variation, 10% load variation, and CMOS process variation respectively.

1. INTRODUCTION

To achieve long transmission distance without causing strong emission, current mode transmitter drivers require accurate current sources. Various techniques [1] [2] [3] [4] [5] have been developed to improve the accuracy of current mirrors in low voltage supply applications. The main principle is to match the drain-source voltages of the mirroring transistors. However, there are many other factors that can cause the current source to be inaccurate, such as process variation, temperature variation, voltage supply variation, and the aging of components [6] [7], to compensate for which, tunable current mirrors have been developed [8] [9]. The binary weighted digital tunable CMOS current mirror proposed in [10] [11] is a generic tunable current mirror architecture, which can be tuned by different kinds of trimming or tuning methods without re-fabrication. However, the manufacturing cost of currently available trimming is usually prohibitive. In addition, most of these trimming methods can only compensate for the process variation and can only be done once. Proposed in this paper is an on-chip self-calibration scheme to automatically measure and tune the binary weighted current mirrors, so that the output differential voltage is within a specified range around the desired value. The manufacturing cost of the on-chip self-calibration circuits is minimal comparing with the currently available trimming methods. The design of the self-calibration current mirror presented in this paper is to provide an accurate current source for current-mode low-voltage differential transmitter drivers.

2. TRANSMITTER DRIVER WITH BINARY WEIGHTED CURRENT MIRROR

The schematic of the proposed binary weight current mirror is shown in Figure 1. The current is mirrored from a current reference to five pairs of simple current sources/sinks. One of them is the main source/sink. The other four are binary weighted with relative size of 1x, 2x, 4x, and 8x. The main mirror is always on. The other four can be turned on or turned off by the switches, controlled by the binary code Q_0, Q_1, Q_2 and Q_3. The total output current, i_{out}, can be expressed by

$$i_{out} = i_{main} + Q_0 i_0 + Q_1 i_1 + Q_2 i_2 + Q_3 i_3 ,$$

where i_{main} is the current of the main current source/sink, i_0, i_1, i_2, and i_3 are the currents of the current sources/sinks with size of 1x, 2x, 4x, and 8x respectively, and Q_0, Q_1, Q_2, Q_3 are the binary codes that control the switches of the binary weighted current sources/sinks. The output of the current-mode driver is the differential output voltage, v_{od}, which is determined by $V_{od}=i_{out}R_L$, wherein R_L is the external floating load resistance. The differential digital signals, InP and InN, control the direction of the i_{out}. Note that the transistors controlled by Qi, InP and InN work only in switch mode – either fully on or fully off, so the current mirrors are actually not in cascaded structure. Thus, they are easy to maintain in saturation region even if there's large mismatch between the sinking and sourcing current sources.

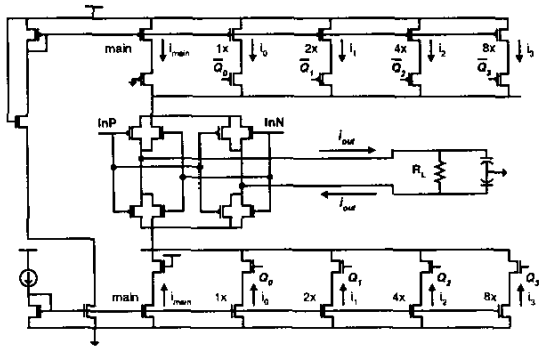

Figure 1. Current mode transmitter driver with binary weighted current mirrors

3. ON-CHIP SELF-CALIBRATION

The first problem of self-calibration is when to perform the calibration. There are two possibilities: the first is to stop the driver from transmitting signals while performing the calibration and the second is to perform the calibration while the driver is transmitting signals. The first method usually means that the circuit is calibrated every time when it wakes up from a power-saving mode to operation. If more frequent calibrations are

This research is partially supported by Texas Instruments Inc.

needed, the driver is required to pause transmitting from time to time. The second method can monitor and tune the current in real-time without interfering the normal operation of the driver. However, it is difficult to measure the output accurately and nondestructively when the driver is transmitting high-frequency signals. In addition, since the calibration circuits are on all the time, it will consume more power than the first method. The choice should be a balance of the application requirements and the overhead introduced by the calibration. In this design, the first method is used.

The schematic of the self-calibration circuit is shown in Figure 2. The basic idea is to first measure the output voltage, then, by adjusting the binary switches to increase or decrease it to within a specified range around the desired value, V_{ref-} to V_{ref+}. Our previous attempts using source followers and opamp subtracter to measure the differential output voltage [12] results less accuracy than expected due to the offsets of the source followers, the opamp, and the comparators. In this design, switch-capacitor circuits are used to deal with the offset errors.

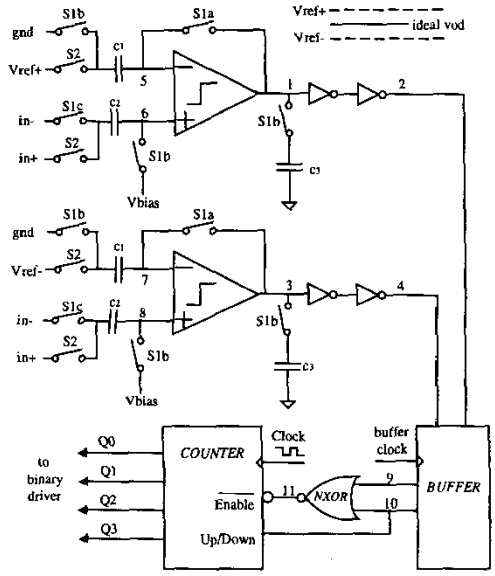

Figure 2. On-chip self-calibration circuit

The switch-capacitor based self-calibration circuit operates in two phases. In phase I, switches S_{1a}, S_{1b}, S_{1c} are closed and the comparators work as a unity gain buffer; C_3 is connected to the output point of the comparator to increase the phase margin and ensure the stability. The bias voltage, V_{bias}, is to bias the input voltages of the comparator into the common mode range; its absolute accuracy will not affect the final calibration accuracy. At the end of phase I, the offsets of the comparator are stored in the capacitor C_1: $VC_1 = V_5 = V_{bias} + V_{offset}$ and $VC_2 = V_{bias} - V(in-)$. The switch close time S_{1a} is slightly earlier than S_{1b}, while S_{1b} is slightly earlier than S_{1c}. This is to reduce the correlation of these switches and minimize the clock feed through effect. In phase II, C_3 is disconnected thus the comparators work at higher speed. Since V_{ref+} and in+ are connected to C_1 and C_2 respectively in phase II, the stabilized voltages at the end of phase II are, $V_5 = V_{ref+} + VC_1 = V_{ref+} + V_{bias} + V_{offset}$, mean while, $V_6 = V(in+) + VC_2 = V(in+) + V_{bias} - V(in-)$. The output V_1 is high, while $V(in+)-V(in-) > V_{ref+}$, and is low, while $V(in+)-V(in-) < V_{ref+}$.

This design compares a differential signal with one of the reference voltage (V_{ref+} or V_{ref-}) using a single comparator, while removing the comparator input offset. V_{ref+}, and V_{ref-} define the tolerant range around the desired vod voltage. This range is determined the size of the minimum adjustable (1X) current source. The smaller the 1X current source, the more accurate the current source is. However, with fixed number of the binary bits, the tunable range is also smaller. Additional control bits can be added to increase the accuracy and the tunable range. In this design, the minimum current source is 1% of the desired current and the range defined by V_{ref+} and V_{ref-} is designed to be slightly larger than 1% to ensure that the vod can jump into this range. The comparator outputs are input to a NXOR gate to determine whether the measured output voltage is within the desired range. Then a counter is used to count the digital control bits up or down according to the position of the output voltage relative to the reference voltages. The comparison results and the actions to be taken are listed in Table 1.

Table 1. Comparison results and actions to be taken

Condition	Vod vs. V_{ref+}	Vod vs. V_{ref-}	Action
1	Low	Low	Count up
2	High	High	Count down
3	Low	High	No action
4	High	Low	No action

Figure 3 shows a simulation waveform when the V(in+)-V(in-) $<V_{ref}$ for points 1 and 2. In phase I, the V_1 is $V_{bias} + V_{offset}$. In phase II, it either rises up or drops down according to the comparison result. Two serial connected inverters are used for two purposes: to speed up the output of the comparison, and to match the load of the two comparators. An additional clocked buffer is used to pass the comparison results to the logic block after the comparison results are stabilized at the middle of phase II. The counter has a clamping logic, so that it cannot jump from 1111 to 0000 when counting up, or vice versa. After the output voltage reaches the desired range, the counting will stop.

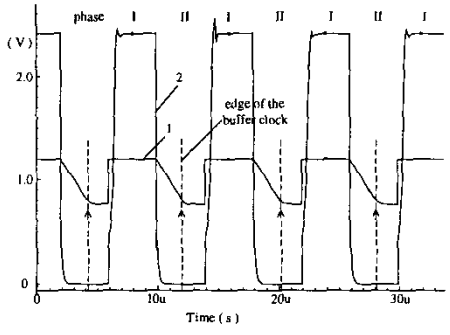

Figure 3. Comparator output when vod < V_{ref}

Figure 4 shows a sample output of the transmitter during the calibration. It starts at about 3% error and ends at less than 1% error.

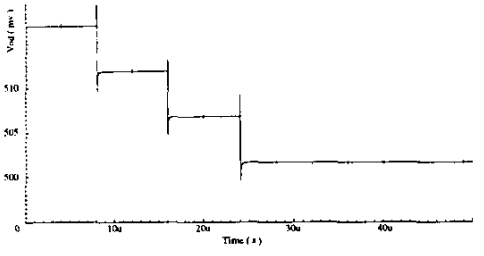

Figure 4. Simulated output current during calibration

4. TEST RESULTS AND DISCUSSION

The test chip is fabricated through TSMC 0.35μm process, the chip area of the transmitter with binary weighted current mirror is 255μm x 295μm and the calibration circuit takes additional 364μm x 200μm, as shown in Figure 5. Some sphere circuits to aid the testing are also presented. Figure 6 shows the test configuration. An external load resistor and parasitic capacitors are connected to the output pins of the driver and are measured by multi-meter and oscilloscope. The outputs of the driver are also connected to the self-calibration circuit internally. We intentionally added a multiplexer between the outputs of the calibration circuit and the binary weighted driver, so that we can use both automatic tuning as well as manual tuning by input the Q values externally. The power supply, the reference current, the load resistor and the calibration clock are all adjustable for the convenience of the testing. In this design, the load resistance is 50Ω and the desired output is 500mv. The fastest calibration clock fed into the counter is 500 KHz during simulation and slows down to 300 KHz in real chip because of the parasitic.

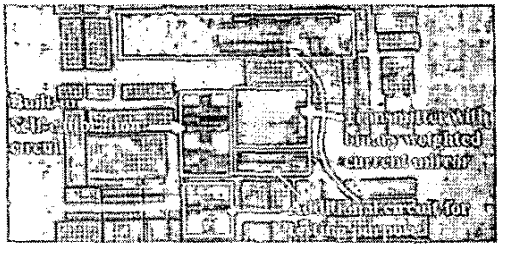

Figure 5. Micrograph of the test chip

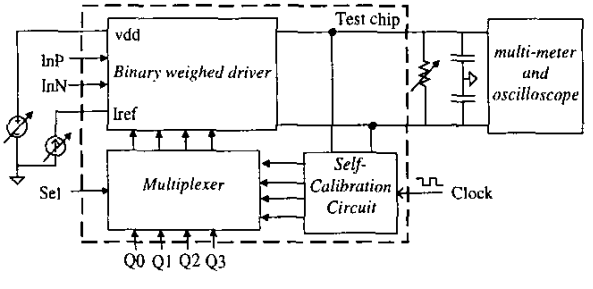

Figure 6. Test configuration

Figure 7 shows the measured output voltage as a result of manually adjusting the binary control bits of the current mirror. It shows very good linearity; the mean square error is 0.02% of the desired output value.

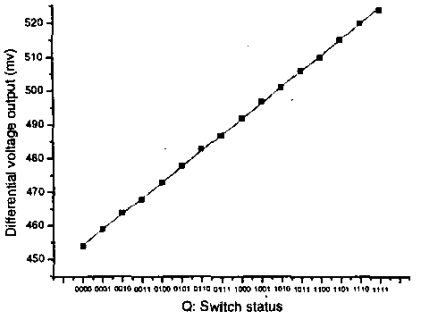

Figure 7. Measured linearity of the binary source

The self-calibration circuit has also been tested with various working conditions. Figure 8 shows that with self-calibration, the output voltage is within the specified ±1% range, with -7% to +10% variations on input reference current. Without calibration, the corresponding output voltage varies from -6.8% to 8.8%. Figure 9 shows that with self-calibration, the output voltage is within the specified ±1% range, with –6% to +12% variations on power supply voltage. Without calibration, the corresponding output voltage varies from –21% to +21%. Figure 10 shows that with self-calibration, the output voltage is within the specified ±1% range, with –4% to 6% variation on the external load. Without calibration, the corresponding output voltage varies from –4% to 6%. Two possible output values, (a) and (b) can be obtained in a single chip after calibration, but they are both within ±1% error. This is mainly caused by the temporal noise of the testing circuit. Effects of process variation among ten test prototype chips are also characterized; ideal power supply, current reference and load are used during this test. Measured data in Figure 11 shows that there is about 2.5% error due to process variation. After self-calibration, the errors of all chips are reduced to the specified ±1% range.

Since the power supply, the reference current, and the load are provided externally in this test chip, testing of the temperature effect is carried out by heating the chip only. The result shows a very small, about 0.01% per °C output shift. That is too small to trigger the calibration since it is still within ±1% accuracy.

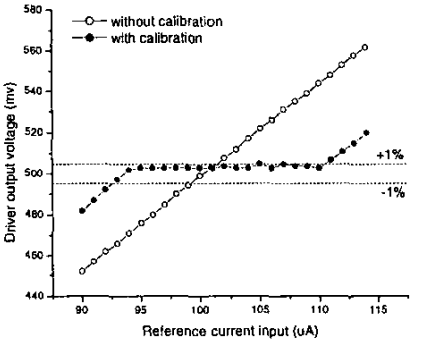

Figure 8. Current reference variation

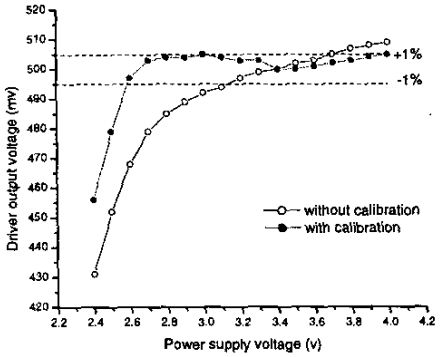

Figure 9. Power supply variation

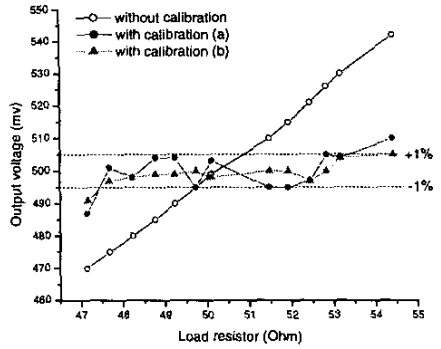

Figure 10. Load resistance variation

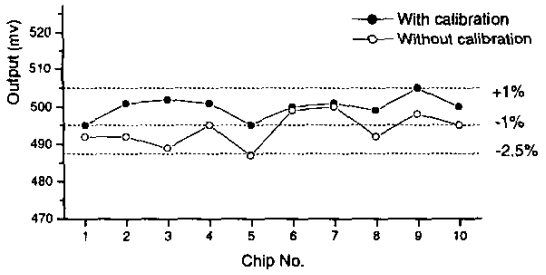

Figure 11. Process variation among several chips

Since the power supply, the reference current, and the load are provided externally in this test chip, testing of the temperature effect is carried out by heating the chip only. The result shows a very small, about 0.01% per °C output shift. That is too small to trigger the calibration since it is still within ±1% accuracy.

In this design, $V_{ref\pm}$ is provided externally. An on-chip bandgap reference and regulator can have about 2% variation. Thus, the major error contributors are (1) the accuracy of the SC circuits due to process variation, which is limited to ±1% as shown from the experimental results and (2) the reference voltage accuracy at the final stage. The estimated overall accuracy is about 4%. Without calibration, about ±8% output voltage variation was found from circuit simulation through standard process, voltage and temperature variations. The main error contributors are from transistor mismatch (about ±1%), load accuracy (±1%), power supply (±2%), reference (±1%), and temperature (±1%). These factors are difficult to compensate individually. The proposed work calibrates upon their collective effects, thus it can deals with larger range of power supply variation, lower reference current accuracy, lower load precision, and larger process variation. As a result, a higher yield can be achieved.

In this design, 4-bit digital control accuracy is used. Increasing the number of the bits will help increase the accuracy further. Additionally, to make the circuits more robust and to increase the yield factor, a thermometer-code based current mirror can be used, in the place of the binary weighted current mirror of this design; since defect on individual sources has less significant effect on the overall current output in thermometer codes than the binary codes.

5. SUMMARY

The binary weighted current mirror with on-chip self-calibration can compensate for errors introduced by process variation, temperature variation, power supply and current reference variations. Measurement shows that ±1% accuracy can be achieved with 16% reference current variation, 42% power supply variation, 10% load variation, and CMOS process variation respectively.

6. REFERENCES

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