Synthesis of a current source using a formal design methodology

Anand M. Pappu, Alyssa B. Apsel
School of Electrical and Computer Engineering
Cornell University
Ithaca, New York 14853
Email: amp46@cornell.edu

***Abstract*— In this paper we present our work on variation-tolerant current source design. The three-transistor-plus-resistor circuit we present, offers more than 2X reduction in standard deviation of the output current at reduced circuit complexity (in a $0.18\mu m$ technology). Moreover, our circuit can be used to mirror a reference current at various locations on the die without incuring mismatches due to process variations while requiring minimum voltage headroom and layout area. The circuit topology itself is derived from a formal methodology presented here.**

I. Introduction

In analog circuit design, process variations both on-die and between wafer runs can have many deleterious effects. Problems resulting from these variations include unpredictable bias conditions, variations in target bandwidth and skew, functionality issues and reduction in yield. Unfortunately, these variations are expected to worsen in deep sub-micron technologies due to difficulties in printing and uniformly doping nanometer-scale geometries [1]. Robust circuit design with performance tolerant to these variations is a tremendous challenge.

A variety of techniques have been used in the past in designing variation-robust circuits. These techniques include feedback techniques and feed-forward techniques like correlating process parameters and using fundamental constants.

Feedback analysis gives us a powerful method of designing variation-robust circuits. In a feedback circuit with a large loop-gain, metrics of importance (like gain) depend on the feedback elements and are robust to the variations in the feed-forward block. Hence, employing off-chip precision elements in the feedback block improves the robustness of the circuit. This solution however, is not attractive for low-cost or dense circuits.

Another interesting technique is making the output characteristics proportional to fundamental constants like bandgap voltage, temperature etc. Bandgap referenced circuits and PTAT circuits fall under this category.

Bandgap referenced and PTAT voltage sources can in-turn be used to generate robust current sources. A current source is one of the basic building blocks in any analog system. Current through a transistor affects its transconductance and thus gain and bandwidth of a circuit become susceptible to variations in the current source output. In this context, designing compact and variation-robust current sources assumes great significance. In order to meet the compactness and area constraints, a constant current source is usually laid-out at one part of the chip and its output is mirrored to locations where a constant current is required. With technology scaling into deep sub-micron and nano regimes, threshold voltage and kappa ($\kappa = \mu C_{ox}\frac{W}{L}$) mismatches across the chip tend to introduce large variations in current mirroring too. Prior work in designing constant current sources has largely ignored this problem.

Sengupta et al [2] have designed a variation compensated current source with a PTAT voltage input by utilizing process parameter correlations to their advantage. In a CMOS process, threshold voltage and kappa have an inverse variation relationship. Thus, designing a circuit with output current variation proportional to $\Delta V_{Th} + C\Delta\kappa$ where C is a constant, reduces the variation in the output current.

With such a variety of techniques available, finding a starting point for designing a novel variation-robust circuit becomes challenging. We have therefore, tried to obtain a formalism for designing such circuits. Our formalism is presented in the next section. While our formalism gives a starting point for designing circuits it does not obviate the need for ingenious design but rather helps to guide the direction of circuit design. In section III, we demonstrate a circuit produced by our methodology that reduces the standard deviation of current variation by half. Moreover, our circuit can be used to mirror a reference current at various locations on the die without incuring mismatches due to process variations.

II. Formalism

Current through a circuit is a function of the circuit topology, bias points and process parameters. Mathematically, this can be abstracted as

$$I = \mathcal{F}(C, \overline{b}, \overline{P}) \tag{1}$$

where C is the topology, $\overline{b}$ is the set of bias points, $\overline{P}$ is the set of process parameters and $\mathcal{F}$ is the function that relates the output current to these "variables". When a circuit is fabricated, variations in the output current result from variations in the bias points and process parameters.

$$\Delta I = f(\overline{b}, \overline{P}) \tag{2}$$

where the function f depends on the partial derivatives of $\mathcal{F}$ with respect to $\overline{b}$ and $\overline{P}$ and is unique for a given topology C. Depending on the circuit topology employed, the function f could be strong or weak. For example, in $I = \kappa(V_{gs} - V_{Th})^2$, current variation is a linear function of the process parameters κ, V_{Th}. Variations in these process parameters lead to a standard deviation over mean ($\frac{\sigma}{\mu}$) greater than 10% in IBM's BiCMOS7WL ($0.18\mu m$ technology).

One design procedure could be outlined thus: 1. Write any equation for the output current through a circuit. 2. Make sure the equation is dimensionally correct. 3. Mathematically ensure that the variations in the current are not a strong function of process and bias (i.e., equate ΔI to zero). 4. Come up with a circuit topology that implements the equation.

All the current sources that are already known in literature are particular cases of this design methodology. This can be shown easily using an example: Let us assume that we chose the equation

$$I = I_{in} e^{\frac{-I_{in}R}{U_T}} \tag{3}$$

where I_{in} is a process dependent current, $U_T = \frac{kT}{q}$ and R is a (relatively process independent) resistor. Variation in the output current is equal to

$$\Delta I = e^{\frac{-I_{in}R}{U_T}} (1 - \frac{I_{in}R}{U_T}) \Delta I_{in} \tag{4}$$

Thus by choosing R such that $(1 - \frac{I_{in}R}{U_T}) = 0$ for nominal values of I_{in}, we minimize variations in the current I. The only task left in obtaining a process independent current source is implementing the equation $I = I_{in} e^{\frac{-I_{in}R}{U_T}}$ which is done using the BJT-based bipolar peaking current source topology shown below.

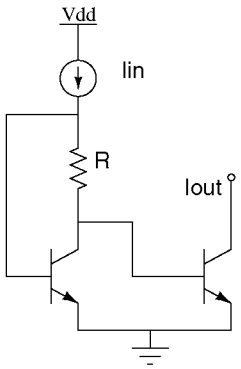

Fig. 1. Bipolar peaking current source implements $I = I_{in} e^{\frac{-I_{in}R}{U_T}}$

The above mentioned method could be used to prove that *any* existing current source could have been obtained using our formalism. More importantly, using this formalism, we can obtain new current sources not seen before. Replacing current, I, with other circuit metrics like g_m, V, BW we can extend our methodology to obtain novel variation robust circuits. In the following section, we demonstrate the "addition-based" current source obtained through our formalism.

III. Addition-based current source

Let's choose our output current I to be the sum of two currents

$$I = I1 + I2 \tag{5}$$

where $I1 = \kappa_1(V_{gs1} - V_{Th})^2$ and $I2 = \kappa_2(V_{gs2} - V_{Th})^2$. Using our formalism, we now need to calculate ΔI. If we assume for the moment that V_{gs1} does not vary, we obtain

$$\Delta I1 = -2\kappa_1(V_{gs1} - V_{Th1})\Delta V_{Th1} + \Delta\kappa_1(V_{gs1} - V_{Th1})^2 \tag{6}$$

$$\Delta I2 = -2\kappa_2(V_{gs2} - V_{Th2})\Delta V_{Th2} + \Delta\kappa_2(V_{gs2} - V_{Th2})^2 + 2\kappa_2(V_{gs2} - V_{Th2})\Delta V_{gs2} \tag{7}$$

A. Simplify using M1 size = M2 size

In order to simplify the expression for ΔI, we assume that ($V_{gs1} \equiv V_{gs}$) is the average/nominal value of V_{gs2} and that the $\kappa_1 = \kappa_2 \equiv \kappa$. Since the transistors M1, M2 are of the same size and have the same gate voltage, their threshold voltages track each other if they are close to each other on the chip. Hence, $\Delta V_{Th1} = \Delta V_{Th2}$. Using these assumptions, we obtain

$$\Delta I2 = \Delta I1 + 2\kappa(V_{gs2} - V_{Th})\Delta V_{gs2} \tag{8}$$

$$\Delta I = 2\Delta I1 + 2\kappa(V_{gs2} - V_{Th})\Delta V_{gs2} \tag{9}$$

$$\Delta I = 0 \Rightarrow \Delta V_{gs2} = -2\Delta I1/g_m \tag{10}$$

where $g_m = 2\kappa(V_{gs} - V_{Th})$. Eq.10 gives us information as to when $\Delta I = 0$ as well as a clue to implementation. We need to make the gate voltage of the second transistor equal to the voltage produced by running the current I_1 through a resistor $R = 2/g_m$. We can thus implement the "addition-based current source" via the following circuit.

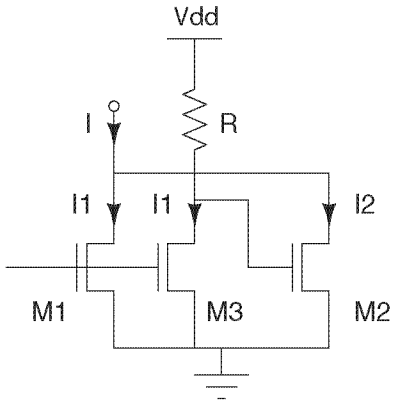

Fig. 2. Addition-based current source

In this circuit, M1 and M3 are assumed to match each other due to their proximity. The gate voltage of transistor M2 then changes by $\Delta V_{gs2} = -\Delta I1 R$ satisfying our design criterion. The power supply V_{dd} depends on the gate voltage V_{gs}, R and I_1.

We simulated the circuit in IBMs BiCMOS7WL technology and ran a full monte-carlo simulation on the process variation. When matching between M1 and M3 is enabled in the simulation and an ideal resistor with no variation is used, we

observe a near zero standard deviation of $\sigma = .7\mu A$ for a mean current of $\mu = 320\mu A$, verifying our calculations. The value of the resistor for which we obtain the minimum standard deviation matches well with the equation $2/g_m = R \parallel 1/g_{ds}$. (Note that g_{ds} plays a significant role due to the short gate length of all the transistors, $= 0.18\mu m$). The output when matching between M1 and M3 is disabled is shown in Fig. 3. The plot shows the histograph of the output current of our circuit and the output current of an NMOS transistor. We observe an improvement of over 2X in the standard deviation. The net variation in the output current is due to mismatch between transistors M1 and M3. In the previous analysis

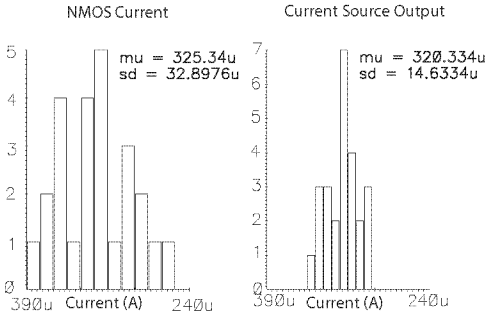

Fig. 3. Comparison of Monte Carlo simulations

we assumed an ideal resistor. We now calculate the standard deviation of the output current after relaxing this constraint. With resistor variations, output current variation as the sum of current variations in the two transistors becomes

$$\Delta I = \Delta I1 + (\Delta I1 + (-\Delta I1 R - I_1 \Delta R) g_{m2}) \quad (11)$$

$$= \Delta I_1 (2 - R g_{m2}) - I_1 g_{m2} \Delta R \quad (12)$$

We now choose the value of the resistor R such that the standard deviation over mean of the output current is minimized. Given a random variable $Z = aX + bY$, where a and b are constants and X and Y are random variables, we can write

$$\sigma_Z^2 = a^2 \sigma_X^2 + b^2 \sigma_Y^2 + 2ab\rho\sigma_X\sigma_Y \quad (13)$$

where ρ is the correlation coefficient of the two random variables X and Y. Using this, we can write

$$\sigma_I^2 = (2 - R g_{m2})^2 \sigma_{I1}^2 + I_1^2 g_{m2}^2 \sigma_R^2 \quad (14)$$
$$-2(2 - R g_{m2}) I_1 g_{m2} \rho \sigma_{I1} \sigma_R$$

Differentiating σ_I^2/I^2 with respect to the value of the resistor and equating it to zero, we obtain the value of the resistor R

$$R = 2/g_{m2} * \frac{\rho_I^2 + \rho_I \rho_r \rho}{\rho_I^2 + \rho_r^2 + 2\rho_I \rho_r \rho} \quad (15)$$

where ρ is the cross-correlation coefficient between R and I_1, $\rho_I = \sigma_{I1}/I_1$ and $\rho_r = \sigma_R/\mu_R$. Values of ρ, ρ_r and σ_{I1}/μ_{I1} are statistical constants. Using a value of the resistor predicted by the equation 15 gave us the minimum standard deviation. This is shown in Fig. 4, with an improvement of almost 2X in the standard deviation.

(All the results presented henceforth, include M1-M3 mismatches and resistor variations.)

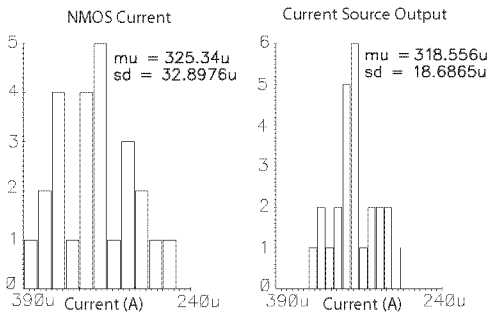

Fig. 4. Current variation when resistor variations are included

B. Size M1 ≠ size M2

The addition-based current source has multiple degrees of freedom including the supply voltage for the resistor, M2 size and the value of the resistor. So far, we fixed the size of M2 to be the size of M1 and kept $V_{gs1} = V_{gs2}$ while scaling the power supply. In applications where the power supply is predetermined, we could alternatively scale the size of M2 and obtain a minimum standard deviation in the output current.

Fig. 5 shows that we once again obtain an improvement of 2X in the standard deviation of current variation with the addition-based current source. This result is better than the previously published results while considerably reducing the circuit complexity [2], [3].

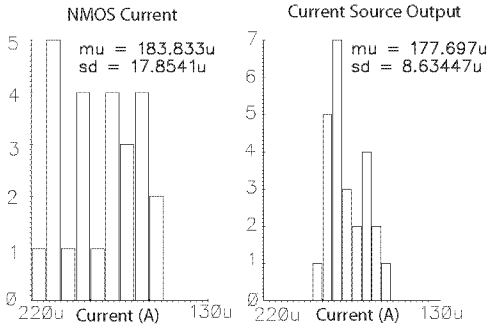

Fig. 5. Current variation when M2 size scaled and power supply kept constant to minimize standard deviation.

C. Operation in deep submicron regimes

In designing the addition-based current source, we assumed square-law MOS devices and obtained the required conditions for minimum output current standard deviation. For devices in deep short channel regime, we need to modify the square-law to the α-model, $I \propto (V_{gs} - V_{Th})^{\alpha}$ [4]. Using this equation and following our formalism, we obtain sizing for transistor M2 for minimum variance.

$$g_{m2} = \frac{1}{R - \frac{1}{g_{m1}}} \quad (16)$$

We pushed the devices into deep short channel regime by increasing the gate-source voltage. Fig. 6 shows the improvement in standard deviation with our current source. Once again, we observe an improvement of over 2X.

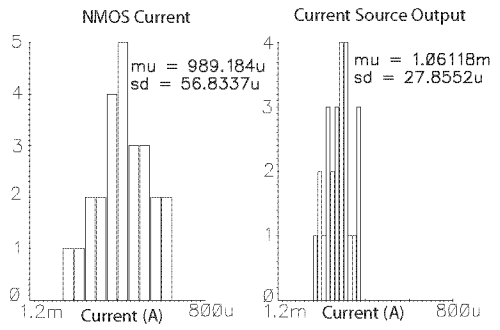

Fig. 6. Comparison of NMOS current variation and the addition-based current source output variation is shown. All the devices operate in deep short channel regime.

D. Current Mirroring

An interesting advantage of our circuit, apart from the 2X improvement in standard deviation is that it can be used to mirror currents across the die while minimizing variations due to threshold and kappa mismatches. Fig. 7 illustrates this. In a traditional current mirror, as the distance between the two transistors increases, output current becomes susceptible to variations in the threshold voltage and kappa. The gate voltage generated by the diode connected transistor becomes dependent on the local threshold voltage and kappa. In the addition-based current source, the gate voltage V_g generated is compensated for process variations. And for a given gate voltage, as shown in the previous sections, the output current does not depend strongly on the process parameters. To the best of our knowledge, all the previous designs assumed the current mirroring mismatches as a given and have not addressed them [2], [3], [5].

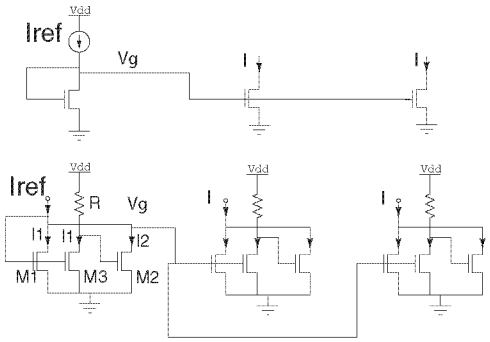

Fig. 7. Improved current mirroring using the "addition-based current source"

E. Temperature compensation

Output current variation of our current source with temperature is plotted in Fig. 8. It shows a variation of $\pm 3.4\%$ over $120°C$ temperature variation. This can be reduced to $\pm 1.2\%$ variation with the use of a PTAT voltage source to bias M1 and M3 transistors as shown in Fig. 8.

Temperature compensated current sources based on bandgap references with variation of about 0.5% have been reported earlier [5]. Unfortunately, these circuits are complicated and do not compensate for process variations. Among circuits that

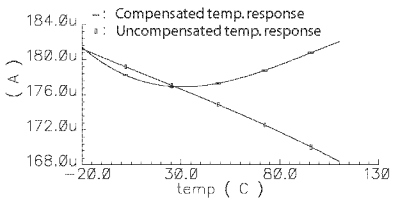

Fig. 8. Variation of output current with temperature with and without compensation

compensate for both process and temperature, our temperature results are comparable or better without incuring the complexity penalty of large circuits [2], [3]. This allows our circuit to be easily replicated in arrayed architectures. Our current source also imposes a minimum voltage headroom constraint on the circuit it is connected to since the output current is from a saturated NMOS transistor requiring a headroom of only $V_{gs} - V_{Th}$. This makes it useful for low-voltage operation.

IV. Conclusion

In summary, we have presented a formalism for process invariant circuit design and an example current source that shows more than 2X improvement in the output current standard deviation. This improvement along with the compact design and low voltage headroom requirement make it ideal for use in arrayed cells. The "addition-based current source" also solves the problem of mirroring current across the die while compensating for threshold and kappa variations. Replicating a reference current across a die or a wafer will now not involve process-related variations.

Our formalism provides a starting point for designing process invariant circuits. With this we can obtain a number of topologies hitherto not seen. Our formalism thus makes a fundamental contribution towards variation-robust circuits. This is essential for improving the predictability and yield degradation due to process variations as technologies continue to scale.

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References

[1] S. Borkar, T. Karnik, and V. De, "Design and reliablity challenges in nanometer technologies," in *Proc. Design Automation Conference (DAC'04)*, 2004, pp. 75–75.

[2] S. Sengupta, K. Saurabh, and P. E. Allen, "A process, voltage and temperature compensated cmos constant current reference," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS'04)*, May 2004, pp. 23–26.

[3] S. Tang, S. Narendra, and V. De, "Temperature and process invariant mos-based reference current generation circuits for sub-1v operation," in *Proc. IEEE International Symposium on Low Power Electronics and Design (ISLPED'03)*, Aug. 2003, pp. 199–204.

[4] K. A. Bowman, B. L. Austin, J. C. Eble, X. Tang, and J. D. Meindl, "A physical alpha-power law mosfet model," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 1410–1414, Oct. 1999.

[5] J. Chen and B. Shi, "1v cmos current reference with $50ppm/°c$ temperature coefficient," *Electronic Letters*, vol. 39, pp. 209–210, Jan. 2003.