An Automated Josephson-Based AC-Voltage Calibration System

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***Abstract*— This paper describes a new calibration system developed at INMETRO to guarantee traceability of low-frequency alternating current (ac) voltage calibrations (<1 kHz) to a programmable Josephson ac waveform synthesizer. The automated full-synchronous system allows the synchronization of a commercial calibrator or signal synthesizer with a programmable Josephson voltage synthesizer system to be made by employing digital sampling and signal processing techniques, aided by adaptive digital control. It allows accurate determination of the spectral content of ac signals with minimum human intervention. System operation, measurement techniques, and data analysis are detailed.**

***Index Terms*— AC voltage, digital signal processing, Josephson, measurement standards, power, spectral analysis.**

I. Introduction

DESPITE the fact that the Josephson effect was discovered 52 years ago [1], it could only effectively be employed in ac metrology rather recently, especially for the very accurate characterization of time-varying (ac) signals, a realm dominated by the use of thermal converters (TCs) or ac–dc transfer measurements. Although TCs are the most accurate root-mean-square (rms) detecting devices ever devised, a full characterization of ac signals, e.g., the determination of their spectral content was not fully possible with such devices. This task is best done by using digital sampling techniques, since accuracy, resolution, and speed of analog-to-digital converters (ADCs) kept pace with progresses in semiconductor technology.

Due to the evident economic importance of this subject, many national metrology institutes (NMIs) seek traceability of their ac units to quantum standards. INMETRO is also focused on this task and developed its own ac voltage calibration system, which integrates a programmable step-driven Josephson voltage synthesizer (PJVS) developed at the National Institute of Standards and Technology (NIST) [2], [3], a nearly perfect frequency to voltage converter.

Our system differs from developments done in [4] and [5] in respect with hardware and the automated frequency and phase high resolution synchronization of signals with the ac Josephson waveform, all managed by independent digital regulators. The hardware makes use of multiple direct digital synthesizers (DDSs) operating with a common clock and regulated by adaptive algorithms in a control software. Further, it possesses multichannel capabilities and allows thus ac power measurements to be done, provided that transducers are added to the system. The system as a whole enables the comfortable and reliable use of a PJVS. Special algorithms allow synchronizing ac sources without an internal time base as, e.g., a Wien oscillator. Hereupon, the system helps to fathom the limits of ultrapure sine synthesis and to ensure traceability of harmonic content measurements. Next, the system, procedures, algorithms, and measurements are described.

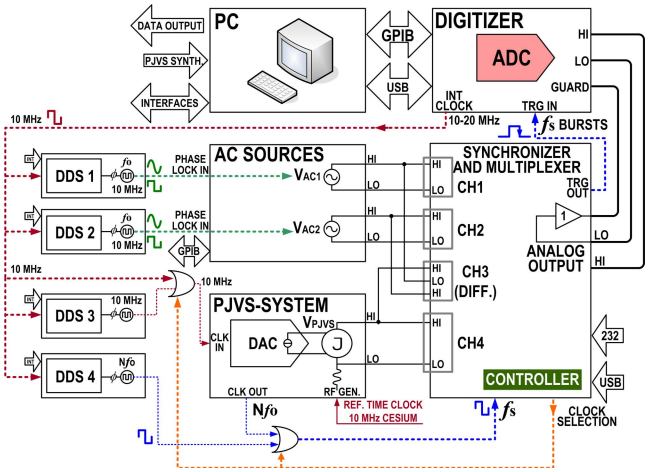

Fig. 1. PJVS-based calibration system. The PJVS, synchronizer, four DDSs, and a digitizer, connected to a personal computer for measurement automation, build its core. Dotted lines: clocking signals (see text).

II. PJVS-Based AC Calibration System

Fig. 1 shows the block diagram of the system. The PJVS (at the bottom middle) operates as a stand-alone waveform synthesizer and generates stepwise-approximated ac signals with quantized plateaus [2], [3]. A radio-frequency oscillator, locked to the 10 MHz of a cesium time standard generates the microwave bias signal (of ∼20 GHz) for the Josephson arrays in a helium dewar. The device under test (DUT) is a calibrator V_{AC1}, which is phase locked by DDS 1. A second source V_{AC2}, also a DUT, is phase locked by DDS 2. For the case of sources with analog phase locking, the DDSs' outputs are a sine, whereas for digital sources a square wave. The third DDS allows synchronization of the PJVS to other sources, which do not possess internal frequency locking capability (Section III-B), and DDS 4 adjusts the position of the integration window of the ADC on each PJVS waveform. In addition, it delivers the ADC sampling clock f_s to the synchronizer, which acts as a synchronous multiplexer. The time-base reference of the DDSs is the internal 10-MHz reference clock

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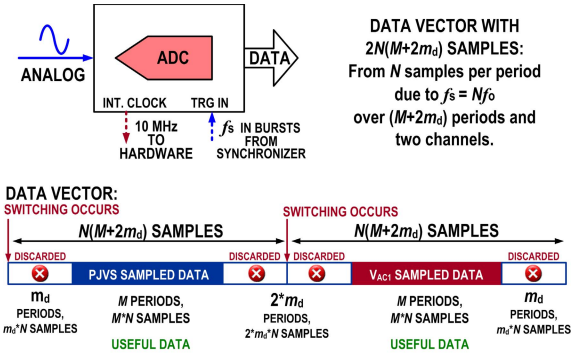

Fig. 2. Data sampled in the pairs of sets according to the programmable setup of the synchronizer. A number of discarded periods m_d before and after a useful data set precludes corrupted samples due to channel switching (or multiplexing and relay bouncing) of being further processed.

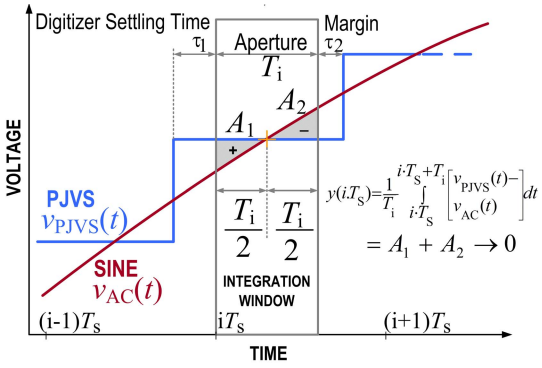

Fig. 3. Integration window is placed on a plateau with enough settling time allowance τ_1 for the ADC, where $\tau_1 > \tau_2$ for a given integration time T_i. The margin at the right τ_2 is set to minimum, to maximize τ_1. A differential sample $y(i \cdot T_s)$ is the mean value of the two areas A_1 and A_2.

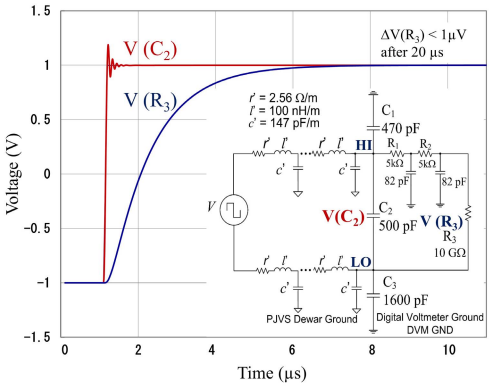

Fig. 4. Step response of PJVS wiring and DVM input circuitry. Inset: wiring model of the system PJVS (to the left of HI and LO terminals of the DVM). The DVM input stage is represented by the analog filter and ADC input impedance of 10 GΩ ($R3$). PJVS rise time assumed was 100 ns. No galvanic connection between dewar and DVM ground (GND) exists.

of the ADC, as is the circuitry for updating the bias current sources built by digital-to-analog converters (DACs) of the PJVS (CLK IN input of the PJVS system in Fig. 1).

The synchronizer manages data acquisition and the routing of clock signals at DDS 3 and DDS 4 as represented by the OR gates at their outputs, representing clock selectors. It releases trigger bursts at the sampling rate f_s to the ADC (a highly accurate integrating digitizer of 28 bits resolution). It possesses four channels and a matrix of relays to route analog signals to the ADC. Channels 1 and 2 (CH1 and CH2) are for direct measurements of V_{AC1} and V_{AC2}, respectively. Channel 3 (CH3) allows differential voltage measurements to be made by connecting the HI and low (LO) digital voltmeter (DVM) inputs in series opposition with the HI output either of the PJVS or of V_{AC2} (to the HI terminal of the DVM) with respect to the HI of V_{AC1} (tied to the LO of the DVM). Differential signals $v_{PJVS}(t) - v_{AC1}(t)$ and $v_{AC2}(t) - v_{AC1}(t)$ can thus be sampled, similarly as described in [6]. A buffer amplifier of unity gain feeds $v_{AC1}(t)$ to the guard terminal of the DVM to reduce common-mode errors when doing differential measurements. Channel 4 (CH4) is used for direct measurements of the PJVS, i.e., $v_{PJVS}(t)$. Worth mentioning, the synchronizer ties the LO terminals of the sources to a single Mecca reference point (the LO of PJVS) and allows further the synchronization of both calibrators (or DUTs V_{AC1} and V_{AC2}) and the PJVS with a resolution up to some nanoradian if desired. Coherent signal generation and sampling takes thus place.

The controlling computer reads the file containing pertinent information about the signal of the PJVS system, controlled by its own computer (not shown in Fig. 1). This information includes the number of steps N, the exact value of each quantum step voltage and finally the signal frequency f_o. This results in a sampling rate $f_s = 1/T_s = Nf_o$. Fig. 2 shows the data record related to two bursts of sampling pulses leading to $N \cdot (M + 2 \cdot m_d)$ samples of each channel selected by the multiplexer. M stands for the desired number of periods of the signal on the record, and m_d for discarded ones. Each plateau is sampled (or integrated) by a window of aperture (or integration time) $T_i < T_s$ properly placed on the plateau (Fig. 3).

The DVM input circuitry requires some settling time prior to digital conversion [7]. A considerable part of the plateau is thus left for the signal to settle, as shown in Fig. 3. Settling times are more important when doing direct measurements and may be as much as 100 μs. The choice of aperture T_i must thus consider aspects of accuracy [8], noise, bandwidth, and settling time allowance τ_1, which is related to the PJVS wiring. Modeling the wiring of the PJVS from the arrays to the outside using a transmission line model and a lumped model of the DVM input circuitry (determined by careful measurements) considering stray capacitances is shown in Fig. 4 allowing the estimation of signal settling time allowance for the system. Slight overshoot at the DVM inputs arises from resonance effects of the distributed inductances of the PJVS system with stray capacitances. Fig. 4 indicates that after 20 μs a step response shall stabilize within 1 μV/V. The reason of larger settling time has its origin in the ADC internal electronic circuitry and its associated delays. Settling time allowance can be determined by precise shifting the sampling window on the plateau from the left to right and noting the resultant variations of direct PJVS samples for different apertures T_i. This indicates proper values of τ_1, τ_2, and T_i. Variations of the order of 1 μVV^{-1} or smaller are deemed acceptable in the light of presently attainable measurement uncertainties (Table I), which are limited by the ac source amplitude stability and DVM noise contributions.

The placement of the sampling window is automated as follows. The PJVS signal may start at any plateau. The plateau

center may be located by using the clock update rate of the PJVS DAC (CLK OUT output, synchronous to each plateau transition), or by making fine phase increments with DDS 4 and simultaneously detecting signal variations that correspond to plateau transitions. Once the location of plateau transitions is determined, the alignment of the integrating window is a straightforward process. Both alternatives lead to proper placement of the sampling window that compensates also for internal trigger delays in the DVM. The next step is to do a phase shift in DDS 4 output. This can be done in two ways: 1) either by programming the internal phase register of the DDS 4 with an offset phase (to a resolution of 2^{14} steps) and 2) by varying the sampling frequency f_s in much finer and calculable steps during a finite time-span Δt and thereafter setting f_s back to its original value. This allows very precise and small phase increments to be attained, which need later be regulated by digital proportional integrating regulators (i.e., in a feedback). For example, in the case $f_s = 1$ kHz, a variation of f_s of ± 1 in 10^{12} parts of f_s (i.e., $\pm 0.000\,000\,001$ Hz) to be maintained over a time span Δt of 0.1 s leads to a phase slip of the signal to be sampled of merely ± 0.68 nrad each 0.1 s. This corresponds to a ± 0.1 ps shifting in time, and over a Δt of 1 s of just ± 1 ps. After phase adjustments, the sampling frequency f_s gets back to its nominal value for full synchronous measurements. Although even finer adjustments are possible due to the large number of DDS bits, noise in the ac signal imposes limits on phase resolution that can be discriminated by measurement [9]. Cramer–Rao lower bounds [9] though predict phase resolutions of tens of nanoradian for amplitudes of 10 V and a DVM noise density of 200 nV $\mathrm{Hz}^{-1/2}$. The position of the integrating window on the PJVS plateau defines the target phase ϕ_{PJVS} to be used by another digital feedback to synchronize the DUTs with the PJVS. Fortunately, differential measurements errors are not overly sensitive to minor phase misalignment as also verified in [5], [6], and [10]. Although the DAC synchronization algorithm briefly described exceeds by far the needs of differential measurements with a PJVS, it was employed extensively as described next.

III. Phase Synchronization of AC Signals

A. Synchronization of Phase-Locked DAC Sources to the PJVS

DUT and PJVS must nearly be in phase to exploit the advantages of differential voltage measurements. To bring the fundamental of $v_{\mathrm{AC1}}(t)$ or $v_{\mathrm{AC2}}(t)$ in phase with that of $v_{\mathrm{PJVS}}(t)$, the same procedure as for the positioning of the integration window is employed. This time though by varying f_o, phase shifting the output of the ac sources in time. Fig. 5 shows schematically how the synchronization of DACs with the PJVS occurs. Sampled data from direct measurements of, e.g., $v_{\mathrm{AC1}}(t)$ are used to compute the phase either by fast Fourier transform (FFT) or from the auto- and cross-correlation density functions (Wiener–Chintshin theorem). A regulator amplifies the phase residual. For a number of synchronization attempts $m < p$ (p an integer), the adaptive finite impulse response (FIR) filter is first kept inoperative, i.e., it has unit gain, and the proportional

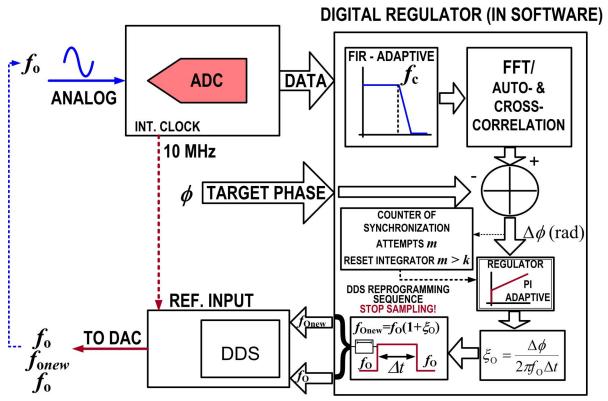

Fig. 5. Algorithm for the digital synchronization of DACs with the PJVS.

integrative (PI) regulator has only a proportional coefficient equal to one (no integrative component). This means that the missed residual phase $\Delta\phi$ is simply added back to approximate the phase of the ac signal to the target phase ϕ_{PJVS}. This process of sampling, processing the phase and DDS reprogramming is repeated. In case the phase residue $\Delta\phi$ in the next synchronization attempt (or repetition) is still greater than a threshold defined by the user (e.g., 30 μrad) and $m > p$ (e.g., for $p = 5$ repetitions) the adaptive FIR filter is engaged to reduce noise. When this happens, the proportional (P) regulator becomes PI [11] with coefficients set within proper limits to ensure stable operating conditions at all times and starts annihilating remanent systematic phase deviations not reduced by the P regulator. The smooth transition of regulator coefficients from P to PI shortens its response time, avoids unnecessary overshoots, and improves regulation, because the integrator buffer starts with small values of phase residuals. On each synchronization attempt, a phase residual $\Delta\phi = \phi_{\mathrm{AC}} - \phi_{\mathrm{PJVS}}$ yields a required fractional dimensionless infinitesimal increment ξ_o to be applied on f_o that results in a new frequency $f_o(1 + \xi_o)$ to compensate for that residual phase ($\Delta\phi$). The step variation from f_o to $f_o(1 + \xi_o)$ is kept for a time-span Δt, and ξ_o is calculated according to

$$\xi_o = \frac{\phi_{\mathrm{AC}} - \phi_{\mathrm{PJVS}}}{2\pi f_o \Delta t}. \tag{1}$$

In case commercial calibrators with analog phase-locking capability are used, it may be necessary to wait longer for the calibrator phase to settle. During this time no sampling occurs. In addition, the regulator must not work indefinitely, since this is indicative of either ac source jittering or some extraneous interference. If for some reason, e.g., interference, the regulator does not ensure synchronization, a reset of the integrator takes place nulling its register, as shown schematically in Fig. 5, when $m > k$ attempts (k integer and selectable), and the regulation process starts over again.

After the ac signal is phase synchronized within predefined threshold limits, the digital regulator is shutoff. Now, the system runs coherently and meaningful measurements may be done. Fig. 6 shows this condition, where the two signals are phase locked with the DVM integration window aligned at the intersection of both waveforms.

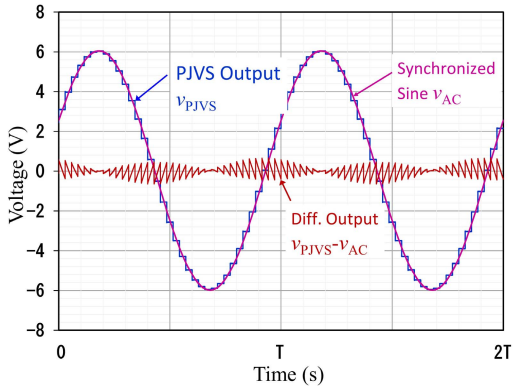

Fig. 6. Signals synchronized by the hardware and digital regulators, and the resulting differential voltage.

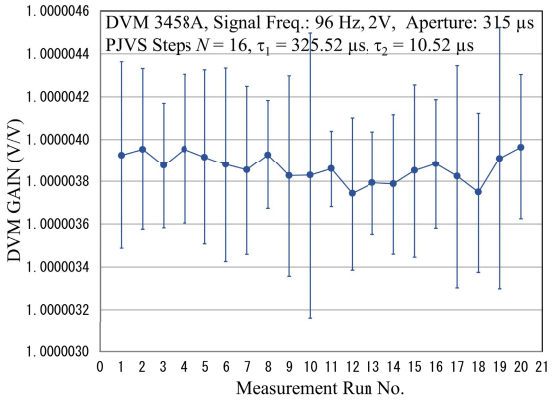

Fig. 7. DVM-ADC gain determined by PJVS direct measurements with $N = 16$ steps, sine waveform. Bars: standard deviation of five measurements (not of the mean).

B. Synchronization of Sources Without Phase-Locking Capabilities

There are innumerable commercial ac sources or synthesizers, which do not allow synchronization with an external reference clock signal. In case the source circuitry uses an internal quartz time base that is not externally accessible, the addition of a small piece of hardware [12] or implant to extract or inject an external time-base clock signal into the hardware might be recommended. This is though not mandatory. Other signal generators, like a Wien oscillator, have their oscillation frequency solely dependent on discrete component values. Although it is indeed possible to force synchronization by injecting a feeble signal close to oscillator's natural frequency, such a procedure will invariably increase its distortion. Furthermore, from time-to-time, the oscillator phase may slip at an accelerated pace, remaining unsynchronized until it finds itself at a quasi-stable point, staying there for some time, until the run out process starts over again. In such cases, we prefer to synchronize the sampling ADC and track it to oscillator's frequency variations over time. Such a method, based on control theory, was described in detail in [13]. This problem can also be solved by the application of estimation theory, as suggested in [14]. The advantage of the first method relies on the lower computation burden and fast software implementation when using a digital signal processor. For that, the 10-MHz reference of the PJVS-DACs is made tunable using DDS 3 (Fig. 1), which is continuously programmed to track the natural frequency variations of f_o as described in [13]. This keeps the PJVS phase locked to the oscillator and not the other way.

IV. Measurement Procedures

A. ADC Gain Calibration

The measurement starts by determining the DVM-ADC gain at a given signal amplitude, fundamental f_o, sampling rate T_s^{-1}, and aperture T_i. The stepwise-approximated PJVS signal is direct sampled on each plateau (Fig. 3) with enough settling time allowance τ_1 (Fig. 3) over a large number of periods M. The sampled data with MN samples are stored in the first half of the data record, as shown in Fig. 2. The multiplexer allows also synchronous direct measurements of, e.g., V_{AC1}. Its sampled data are stored in the second part of the record. A third record of the same length MN is assembled with the PJVS synthesis file (tabulated values). From the three records, information on the DVM can be extracted. We prefer to do the analyses in the frequency domain, and because the system runs coherently to the very common time base of the digitizer, least squares estimations agree with Fourier transform on sampled data. Hence, the PJVS synthesis data vector is FFT ([f]{data vector}), as is the PJVS measured data vector. The DVM gain at a frequency f, i.e., $G(f)$ is defined as a FFT ratio of spectral lines, as follows:

$$G(f) = \frac{\text{FFT } [f]\{\text{PJVS Synthesis Data Vector}\}}{\text{FFT } [f]\{\text{PJVS Measured Data Vector}\}}. \quad (2)$$

It may be interpreted as the coefficient to be used to correct for the DVM gain [8] on the sampled data vector $\mathbf{A}$ (of ac quantities), or FFT $[f]\{\mathbf{A}\}$. The DVM ADC-gain-corrected magnitude of the fundamental of V_{AC1} is thus $G(f_o) \cdot$ FFT $[f_o]\{\mathbf{A}\}$. Fig. 7 shows the measured DVM-ADC gains for 20 measurement runs, with five repetitions per run. A measurement (or measurement run) is the average result of p (an integer) data acquisitions (repetitions), i.e., mean of p records of FFT data, from which the mean and standard deviations are calculated. Standard deviations of repetitions (not of the mean) are also plotted in Fig. 7 and are of the order of $0.5 \cdot 10^{-6}$ VV^{-1}. DVM noise is its main contributor to the measured dispersion.

B. AC Differential Measurements

In this case, the whole data record (Fig. 2) is filled with $2MN$ differential sampled data, i.e., integral average of $v_{DIFF}(t) = v_{PJVS}(t) - v_{AC1}(t)$ over the aperture T_i, according to the inset equation in Fig. 3 for an integrating ADC. Assuming the PJVS signal shall approximate a sine waveform by step functions with peak value V_{PJVSm}, the differential sampled voltages are minimized (i.e., tend to zero) when the peak of $v_{AC1}(t)$, i.e., V_{AC1m} satisfies the relation

$$V_{AC1m} = \frac{V_{PJVSm}}{\text{sinc}(\pi f_o T_i)} \quad (3)$$

where the sinc function stands for the sine cardinalis $[\sin(x)]/x$, and x for $\pi f_o T_i$, due to the integrating char-

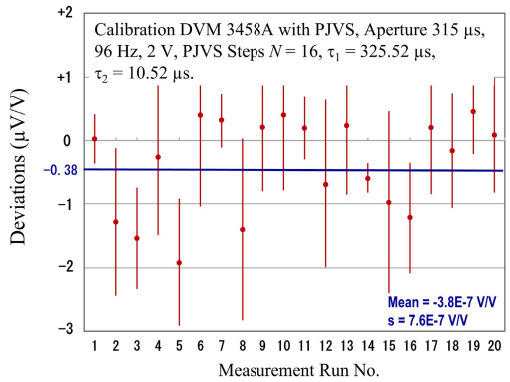

Fig. 8. Deviations of amplitude determinations using direct measurements (after correcting for the DVM gain) compared with those from differential measurements, i.e., $\{V_{\mathrm{ac1}}$ direct–V_{ac1} differential$\}/V_{\mathrm{ac1}}$ differential. The standard deviation of 0.76 $\mu\mathrm{VV}^{-1}$ is the sample standard deviation (not of the mean). The bars correspond to sample standard deviations for five repetitions per point.

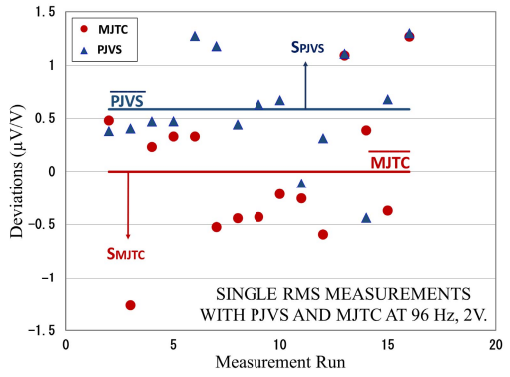

Fig. 9. Deviations of amplitude determinations of PJVS differential measurements (triangles) compared with mean of ac–dc transfer rms measurements (the zero line). Circles: deviations of single ac–dc transfer measurements with respect to their mean value. Arrows: standard deviation of measurement (not of the mean).

acteristic of the DVM-ADC (Agilent 3458 A multimeter). The determination of ac signals (from differential samples) must thus rely on the PJVS synthesis (tabulated) data vector $\{v_{\mathrm{PJVS}}(i\cdot T_{\mathrm{s}}),\ i=0,\ldots,2MN\}$ as

$$v_{\mathrm{AC1}}(i\cdot T_{\mathrm{s}}) = v_{\mathrm{PJVS}}(i\cdot T_{\mathrm{s}}) - v_{\mathrm{DIFF}}(i\cdot T_{\mathrm{s}}). \tag{4}$$

When the FFT of the data is calculated, each spectral component of FFT $[f]\{v_{\mathrm{PJVS}}(i\cdot T_{\mathrm{s}})$, for $i=0,\ldots,2MN\}$ must be corrected for the $\mathrm{sinc}(\pi f T_{\mathrm{i}})$. Coherent measurements with the internal time-base clock of the DVM do not require accurate determination of T_{i} since the product fT_{i} is a constant.

Because the DVM used in the system presents nonlinearities of the order of 10^{-7} parts of its full dynamic range at dc, we used it to validate amplitude determinations of differential and direct measurements. The direct measurements of V_{AC1}, corrected for the DVM gain (Section IV-A and Fig. 7), must agree with V_{AC1} amplitude estimations obtained from differential measurements, provided settling time allowance is enough. Fig. 8 corroborates this. The agreement in the mean is <1 $\mu\mathrm{VV}^{-1}$, i.e., $-3.8\ 10^{-7}$ VV^{-1}.

Amplitude determinations from differential measurements were also validated by ac–dc thermal transfer measurements. A calibrated multijunction TC (MJTC) was used in a fast synchronous ac–dc transfer measurement system, as described

TABLE I
UNCERTAINTY BUDGETS FOR AC SOURCE CALIBRATION ($k=1$) AT 96 Hz

Contribution	Estimation (μV)		Uncertainty ($\mu\mathrm{VV}^{-1}$)
DVM			
Sampling Noise	0.5	Gaussian	0.25
Gain	0.004	Gaussian	0.002
Quantization	0.006	Rectangular	0.002
AC SOURCE			
Sync. jitter	2	Gaussian	1
Drift	1	Gaussian	0.5
Amplitude instability	3	Gaussian	1.5
phase-misalignment due to Synchronization	<2	Gaussian	1
Total Uncertainty:			2.1

in [15]. The deviations of each measurement with respect to the MJTC (i.e., MJTC mean is the zero reference line) is shown in Fig. 9. Here too, the agreement is within a margin around uncertainties of ±1 $\mu\mathrm{VV}^{-1}$ for the TC. The standard deviation of the measurement is slightly higher for the MJTC because of a preresistor (for protection purposes) connected in series with the MJTC, which reduced its output voltage to $\sim$17 mV and its sensitivity. Its nominal full-scale output voltage is $\sim$100 mV. Without the series resistor, the MJTC measurement dispersion was reduced to ±0.3 $\mu\mathrm{VV}^{-1}$.

C. Product of AC Voltages and AC Power

The measurement of the product of ac voltages is aimed at ensuring traceability of ac power to quantum standards. Many NMIs have endeavored efforts toward developing quantum-based ac power standards [16]–[18], either by using direct measurements [18], or by determining amplitudes via differential measurements with signals phase aligned with a PJVS [16], [17]. Measurement uncertainties for ac power at power frequencies are not limited by low voltage measurements with a PJVS, but by transducers, since traceability must be ensured at higher magnitudes.

The system of Fig. 1 allows ac power measurements to be done as well. The relative phase stability between V_{AC1} and V_{AC2} for power measurement is as important as the voltage stability and must be ensured by a tight frequency synchronization with the DVM internal 10-MHz time base. Furthermore, new ac sources of low-phase noise and high stability with their voltage and current amplifiers will be integrated into the system together with an inductive voltage and current transformer, and shunt. This paper is still in progress.

V. MEASUREMENT UNCERTAINTIES

Differential measurements are the pillar of PJVS-based ac measurements. The main components of uncertainty of such determinations are identified as: 1) contributions from the sampler (noise, nonlinearity, gain errors, drift, and bandwidth); 2) from the ac source (noise, drift, amplitude instabilities, and jitter); and 3) contribution from the synchronization process (regulator residual phase threshold). Uncertainties associated with the PJVS (such as leakage) and multiplexer

(relay contact series resistances and crosstalk between channels) are negligible. Table I lists, as an example, typical contributions for calibrations using an analog phase-locked commercial calibrator at 96 Hz, 2 V with $N = 16$, $M = 1024$, and $T_i = 315$ μs, for a coverage factor $k = 1$.

VI. Conclusion

The presented PJVS-based automated ac calibration system [19] shall maintain the unit volt from dc up to 1 kHz traceable to the SI in Brazil. Hitherto conducted investigations corroborate its metrological feasibility. Compared with other developments [4], [5], [16]–[18] our system represents a quantum vector voltmeter, which uses adaptive digital control for dynamic frequency synchronization and phase alignment of signals to allow either direct measurements (e.g., for ADC characterization) or differential measurements (e.g., for DAC characterization). The ADC sampling window is also aligned comfortably with high phase accuracy on the PJVS' plateaus after selecting the desired DVM settling time allowance. The frequency and phase synchronization can work with any ac source, even with those without frequency synchronization capability as described in Section III. In its core stays the current NIST step driven PJVS [2], [3], the world's best quantum ac standard ever devised. Ongoing investigations aim at mathematical modeling of its measurement uncertainties and their reduction, on broadening its frequency range up to 5 kHz, ADC characterization by nonlinear models, and on ensuring traceability to complex waveforms [20]. Future development efforts are aimed at the construction of new lowest phase noise ac sources of high stability, transducers and amplifiers. The developed PJVS-based ac system is a valuable tool to applied investigations on digital signal processing algorithms in metrology, and in a very near future, it will link the unit of ac power to the Josephson voltage standard.

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