225A/22V HIGH PRECISION CURRENT SOURCE USING INTERLEAVED MODULES AND DIGITAL REGULATION

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***Abstract* –This paper presents a first prototype of a high power high stable current source with digital control that will be used in the new Brazilian Synchrotron Source. The output rate is 225A/22V and its topology is based on two Buck converters operating in parallel and in the interleaving mode. This work presents the conceptual design and the first results, as well the detected problems.**

***Keywords* –BUCK CONVERTER, DIGITAL REGULATION, INTERLEAVING, POWER SUPPLY.**

I. INTRODUCTION

The Brazilian Synchrotron Light Laboratory (LNLS), located in Campinas-SP, has built and operated the first Synchrotron Light Source in the southern hemisphere and the only one in Latin America [1], named UVX. Now it is building a second one, called Sirius, which will be a fourth generation synchrotron source, with 3GeV energy and much higher brilliance, as well as the lowest emittance among not only those in operation, but also in construction process [2, 3].

Due to the requirements of this new particle accelerator, the field that will be generated by the magnetic lattice needs to be highly stable and accurate to provide a very stable electron beam in order to obtain the radiation for scientific experiments. The Power Supplies (PS) that feed these magnets are an important element in order to get the necessary field quality. In some parts of the magnetic lattice is necessary the use of current sources with capabilities to feed magnets with hundreds of amperes and a long term stability and ripple better than 20ppm in relation to their nominal current, among other requirements.

Since the implementation of the Digital Regulation System (DRS) with low power PS [4] achieved good results, it was decided to use it with a more powerful power stage like those that will be used to feed magnets as dipoles, quadrupoles and sextupoles of Sirius' Storage Ring. Then, a prototype was designed and built to validate the adopted solutions.

The operation characteristic of this kind of PS is stay in an adjusted value with the required stability along all the operation time. During the turn-on and turn-off process the set point gradually increase or decrease using respectively a soft-start and soft-stop ramp. However, if some disturb occurs during the operation, the protection system trips the PS in a hot shutdown.

The maximum value of the output current of this kind of PS must be 175A or 350A, and the voltage 200V or 400V. However, the maximum values chosen for the prototype were 225A and 22.5V, because they correspond to the characteristics of an available magnet that could be used as load. Moreover, these values allow using this prototype as a spare unit of other kind of PS used in UVX.

II. DESCRIPTION OF THE POWER SUPPLY SYSTEM

Figure 1 shows the first prototype of this PS with DRS assembly, which includes the UDC (control board) and HRADC (High Resolution ADC board). This system is connected to a specific power stage desirable for the application, what makes possible standard control hardware to be used in different kinds of situations.

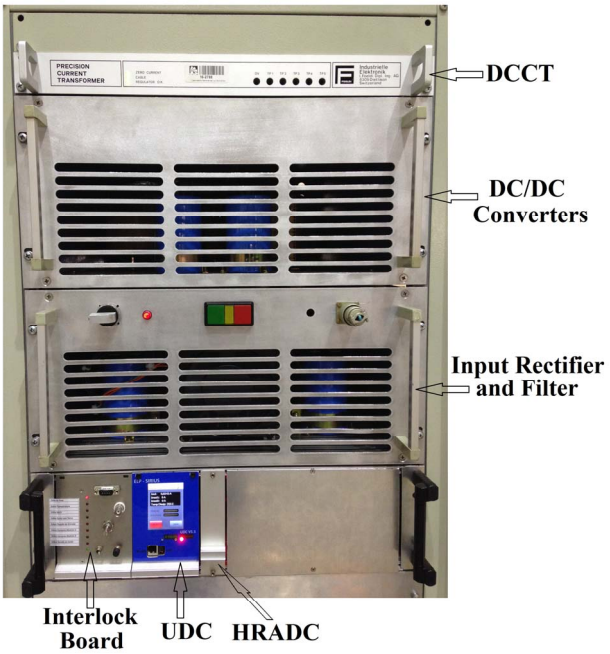

Fig. 1. Power Supply view.

In the Power Stage, two modules are connected in parallel to reduce the current in each switch and consequently the EMI (Electromagnetic Interference) level generated by their commutation. Another reason to use modules in parallel is the possibility to use the interleaving technique, which helps to reduce the output ripple since its frequency will be the switching frequency multiplied by the number of modules [5, 6]. Figure 2 shows a simplified schematic of the power stage.

A three-phase rectifier without regulation generates the DC link voltage, which value is available only for supervision and protection, as well the output voltage.

A DCCT (DC Current Transformer) was used to feedback the output current with a relation of 250A/10V.

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This is a high precision current-to-voltage transducer that uses the zero-flux principle [7]. The output analog signal is converted to digital by the HRADC board and subtracted from the reference value in order to get the error signal. The output current reference can be obtained locally by HMI (Human Machine Interface), remotely by one of the communication interface or by waveforms recorded in the internal memory. In all these cases, for safety reasons, any change in the reference value is implemented in steps of 100mA each 25ms, but this limitation that can be adjusted.

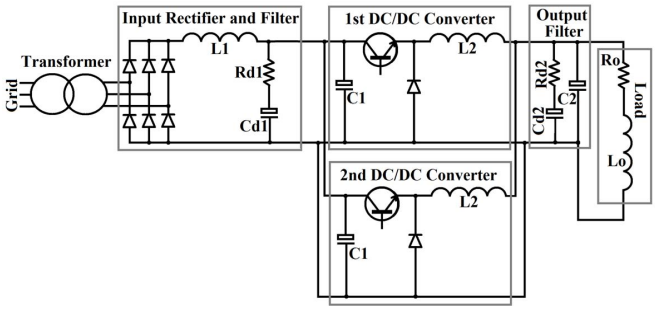

Fig. 2. Simplified schematic of power stage.

Output current regulation is performed by a simple PI running at the same frequency that the Pulse Width Modulator (PWM).The gain values K_p and K_i, as well many others parameters (feedback status, output current reference, other control variables, etc.) can be set while the PS is operating. Figure 3 shows the simplified block diagram of the control system.

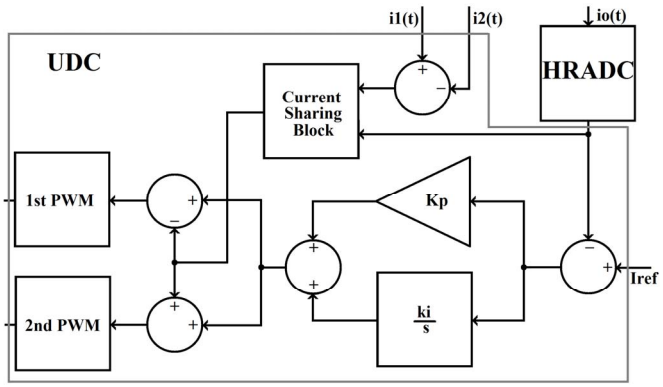

Fig. 3. Block diagram of control circuit.

The current of each module is measured using Hall sensors once it does not need to have high precision. These values are used in the compensation loop to equalize them and for interlock. The equalization in the previous PS was made adjusting manually the module currents and the unbalancing among modules could be detected only by manual inspection [8]. With the DRS, the equalization of the modules starts with 5A in the output and when the difference between module currents is higher than 1A. The routine is implement by the firmware and works with an actuation frequency of just 5Hz in order to minimize possible perturbations in the output during the compensation. If an unbalancing is detected, each cycle will take away 0.03A from the module with more current and transfer to the other module. The limit for correction corresponds to 3A between modules because a greater difference can indicate any problem with one of them, but if it will be necessary other limit it can be changed. All this operations are performed by the Current Sharing Block in figure 3. For static PS, the equalization does not need a high performance along the full range, but for cycling ones, it does.

The PWM signals are sent to the IGBT drivers by optical fibers in order to get galvanic insulation between the control and the power circuits, as well as keeping them far from one each other in order to decrease the effect of the EMI generated by switching.

System variables and other parameters are accessible via bus interface (RS485) or HMI, both available in the front panel. The HMI is a thin-film-transistor (TFT) display with a resistive touch-screen that makes possible creating a full custom user interface for local adjust and to visualize system variables, without a computer or other external tools. Through the navigation menu, it is possible to control the PS and have access to routines for test execution.

For remote control, it can be used the communication bus (RS485) with a maximum baud rate of 10Mbps. The high-level control system can have access to several kinds of system variables by this communication port.

III. CONTROL DESIGN

In order to design the control of the PS it will be considered the block diagram showed in figure 4.

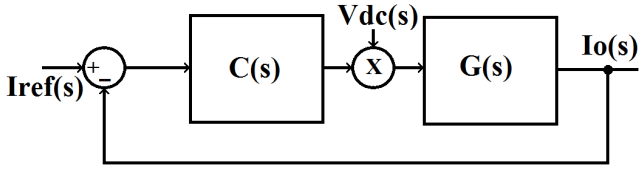

Fig. 4. Considered system for design.

The transfer function G(s) represents the output filter and the load, and is given by:

$$G(s) = \frac{s \cdot N_1 + 1}{s^4 \cdot D_4 + s^3 \cdot D_3 + s^2 \cdot D_2 + s \cdot D_1 + D_0} \quad (1)$$

where:

$$D_4 = R_{d2} \cdot L_{eq} \cdot L_o \cdot C_2 \cdot C_d \quad (2)$$

$$D_3 = L_{eq} \cdot L_o \cdot (C_{d2} + C_2) + R_o \cdot R_{d2} \cdot L_{eq} \cdot C_2 \cdot C_{d2} \quad (3)$$

$$D_2 = L_{eq} \cdot R_o \cdot (C_{d2} + C_2) + R_{d2} \cdot C_{d2} \cdot (L_{eq} + L_o) \quad (4)$$

$$D_1 = L_{eq} + L_o + R_o \cdot R_{d2} \cdot C_{d2} \quad (5)$$

$$D_0 = R_o \quad (6)$$

$$N_1 = R_{d2} \cdot C_{d2} \quad (7)$$

Effects associated to the interleaved structure differ from the dynamics of an equivalent single module only for

frequencies higher or equal the switching frequency, and since this model is based on average values, they can be disregarded. The only important consideration is that the equivalent inductance of the output filter is the parallel association of the individual inductance L_2:

$$L_{eq} = \frac{L_2}{2} \tag{8}$$

However, due to the high time constant of the load, equation (1) can be approximated to the load transfer function:

$$G(s) \cong \frac{1}{L_o} \cdot \frac{1}{s+{R_o}/{L_o}} \tag{9}$$

The transfer function C(s) represents the compensator circuit. It can be given by:

$$C(s) = \frac{s \cdot K_p + K_i}{s} \tag{10}$$

Then, the transfer function between the output current and the reference, in closed loop and considering a constant DC link voltage will be:

$$\frac{I_o(s)}{I_{ref}(s)} = \frac{K_p \cdot V_{dc}}{L_o} \cdot \frac{s+{K_i}/{K_p}}{s\cdot\left(s+{R_o}/{L_o}\right)+\frac{K_p \cdot V_{dc}}{L_o}\left(s+{K_i}/{K_p}\right)} \tag{11}$$

In this application, it is interesting to choose the relation K_i/K_p as the same that R_o/L_o in order that the system can be reduced to a first order one given by:

$$\frac{I_o(s)}{I_{ref}(s)} = \frac{K_p \cdot V_{dc}}{L_o} \cdot \frac{1}{s+\frac{K_p \cdot V_{dc}}{L_o}} \tag{12}$$

As a first order system, there are no oscillations in the output for an input step, and the value of K_p can be calculated according to the desired response time. For an input step with amplitude I_p and an initial value Io_i, the output current must follow the equation:

$$i_o(t) = I_p \cdot \left(1 - e^{-t/\tau}\right) + Io_i \tag{13}$$

where:

$$\tau = \frac{L_o}{K_p \cdot V_{dc}} \tag{14}$$

One possible definition to the response time is the needed time to the output current reach 95% of the final value, which corresponds to approximately three times the time constant τ.

IV. SIMULATIONS, MEASUREMENTS AND RESULTS

A prototype was designed and built to verify experimentally the behavior of this topology. During the tests, the room temperature variation was less than 2°C.

The design took into account the available components at LNLS, and the value of them were: 380V/37V/6kVA three-phase transformer, L_1=100µH, R_{d1}=60mΩ, C_{d1}=100mF, C_1=14.4mF, L_2=50µH, R_{d2}=0.9Ω, C_{d2}=80µF, C_2=10µF, R_o=100mΩ, L_o=40mH.

With these components, the value of the DC link was 52V without output current and 45.5V with the nominal current. In the simulations, it was considered 50V.

For a desired 20ms response time, (14) gives a K_p=0.12. Then, making the relation $K_i/K_p=R_o/L_o$, the value of K_i was 0.3. In order to verify the accuracy of the model it was compared the effect in the output current of a 2A step (from 110.5A to 112.5A) in the PS with simulations using Matlab (only the closed loop transfer function) and PSPICE (all the circuit, including switching). The di/dt limitation of 100mA/25ms was off during this test. The result is showed in figure 5, where can be observed that both simulations presented almost the same result, then validating the used model. Comparing the simulations with the PS, the difference is small and can be explained by the simplifications of the model and the deviations of the component values.

The RMS and peak-to-peak ripple was measured for full (DC to 1MHz) and limited (DC to 1kHz) bandwidth, from zero to the nominal current, with steps of 10%. Figure 6 shows the RMS ripples with limited bandwidth, where can be seen that the maximum value was 14ppm.

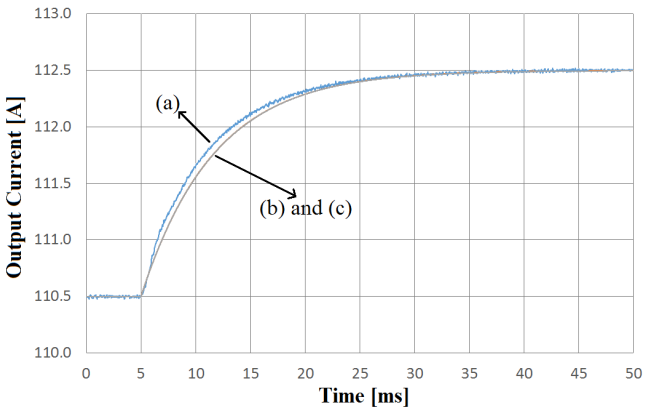

Fig. 5. Step response obtained with the Power Supply (a) and simulating with PSPICE (b) and Matlab (c).

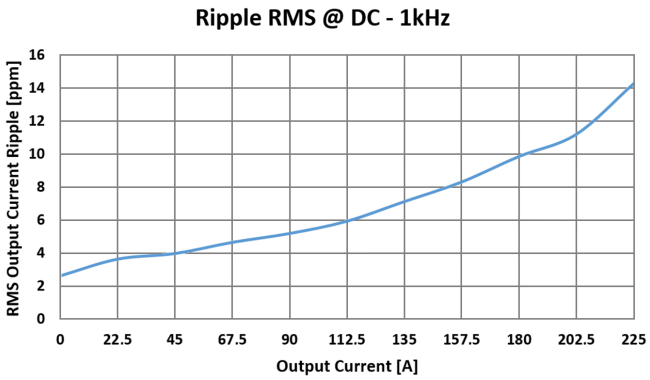

Fig. 6. RMS output current ripple for DC to 1kHz bandwidth.

In order to verify the current sharing between the modules, it was programmed a triangular reference from zero to the maximum current, with a rise and fall time of one hour. The result is shown in figure 7, where can be seen that the module currents are very similar. Figure 8 shows a detail of the figure 7, for the maximum difference of 2.5A between each module output current, which corresponds to approximately 1% of the nominal current.

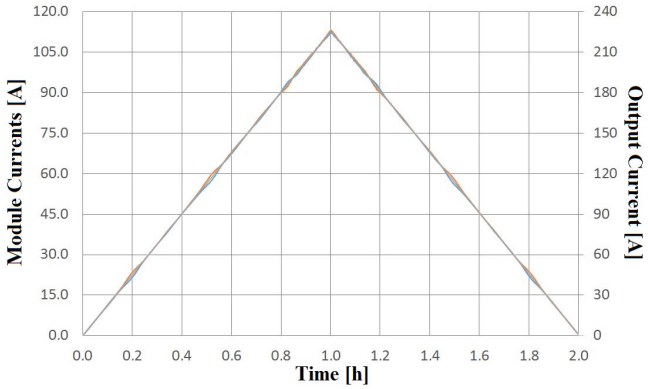

Fig. 7. Current sharing between modules along full PS range.

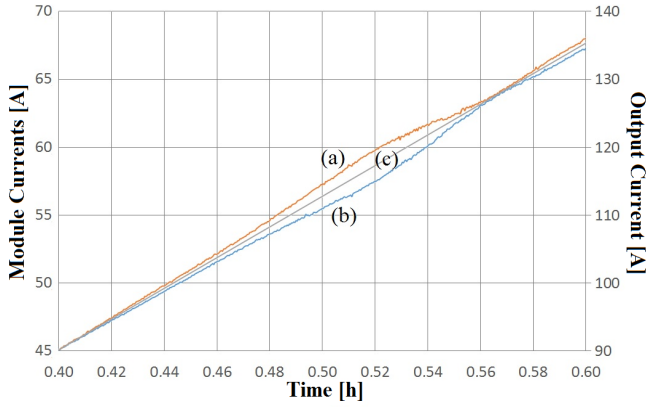

Fig. 8. Detail of figure 6, where (a) and (b) are the module currents and (c) is the output current.

The long-term stability was verified for 10%, 50% and 100% of the nominal current, along 12 hours. The maximum deviation was 44ppm, taking in account the warm-up variation, and less than 20ppm if does not, what happened with the nominal current. However, in some tests it was seen perturbations on the output as can be seen in figure 9. Turning on and off loads to the grid, it was observed variations in the DC-link voltage due to fast mains changes. Figure 10 shows a detail of output current variation during one of these transitions. Solutions to solve this problem by control strategies were explored and will be presented in other work in this conference [9].

The obtained efficiency was 79% and the power factor 0.95. Some tests were made changing the switching frequency, from the initial value of 10kHz to 5kHz and after to 20kHz. The efficiency did not change in the first case but decreased to 77% in the second one.

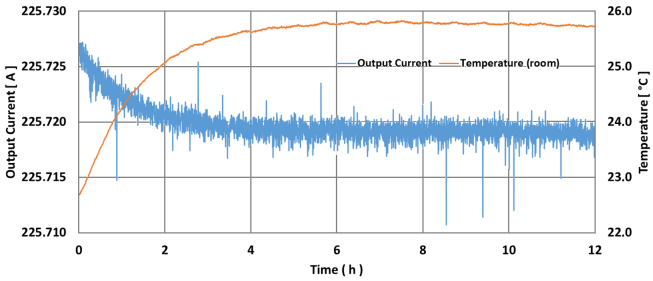

Fig. 9. Long-term stability test for 225A with spikes due to mains variations.

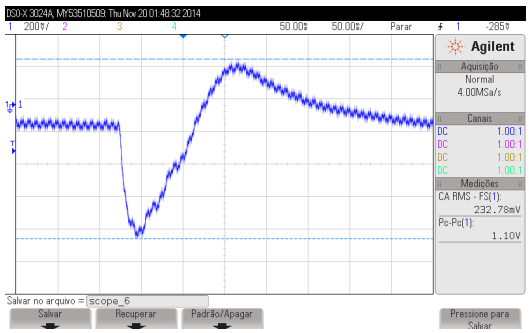

Fig. 10. Detail of a perturbation in the output current (50mA/div, 50ms/div).

V. CONCLUSIONS

Although the prototype was assembled using available components at LNLS, for a concept proof, the results were satisfactory. For example, ripple and long-term stability are already within the 20ppm specification.

The high susceptibility with the mains variations must be reduced with changes in the control strategy, which will be presented in other work in this conference. However, the rectifier filter could also be improved to decrease the DC-link transients.

No perturbation was observed in the output current during the equalization of the module currents, but tests must be made with a higher actuation frequency and lower allowed difference between modules. Other strategies to improve the current sharing also are been studied for the next prototype.

A second prototype is been built now with dedicated components and with the second version of DRS, so the expectation is to obtain better results. The output rate will be 200A/200V and once the IGBTs will be the same used in the first prototype, what means the same conduction losses, the efficiency must be improved.

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