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The Dual-Slope Conversion Improvement

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Abstract: The dual-slope ADC (DSADC) is a type of analog-to-digital conversion with low input bandwidths. It is pretty slow, but its ability to reject high-frequency noise and fixed low frequencies such as 50 Hz or 60 Hz makes it useful in noisy industrial environments and applications. It provides very good resolution. For the practical measurements in the Institutes laboratory an instrument is designed and realized. The base DSADC method is used, but improved by multiple conversions to make the measuring more precise and the time *shorter.* The special attention is paid to the problems occurred in practical realization and the way to overcome them. The paper describes the proposed and applied solutions, functional principles and achieved performances of the realized instrument.

Keywords: Small resistance measurement, Accuracy, A/D conversion.

1 Introduction

In regard to needs and purposes, there are many ways to convert the analog electrical signal either voltage or current to digital form. For the precise resistance measurement in the laboratory of Mining and Metallurgy Institute Bor, the dual-slope method is chosen.

A current, proportional to the input voltage, charges a capacitor for a fixed time interval *t*-charge. At the end of this interval the device resets its counter and applies an opposite-polarity (negative) reference voltage to the integrator input. With this opposite-polarity signal applied, the capacitor is discharged by a constant current until the voltage at the output of the integrator reaches zero again. The time *t*-discharge is proportional to the input voltage level and used to enable a counter. The final count provides the digital output, corresponding to the input level. The dual-slope conversion is convenient for standard measurement in 4-digits resolution. For this method the integrated circuits like ICL7106 and ICL7135 are used. The conversion speed takes approximately a hundred ms per conversion.

The successive approximations, flash, dual slope, ΔΣ (delta sigma), or other kind of analog-to-digital conversion (A/D conversion, ADC) is often in use [1 – 3].

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Being the fastest way of conversion, the flash conversion is applied in any case the time occurs as a critical factor. The flash A/D converter is realized by a set of parallel comparators; one for each comparison level. It becomes more complicated because of great number of comparators, i.e. for 8-bit conversion it needs 256 comparators. To decrease that number of applying elements the multi-passing method is applied. However, this method still seems quite complex. Consequently, the conversion speed is very high: for 8-bit conversion it takes a couple of nanoseconds.

The method of successive approximations A/D conversion is a slightly bit slower than a previous one, but simpler. It could be used for higher resolutions.

Consequently, the conversion time takes about hundred nanoseconds.

Nowadays for the most accurate measurements the ΔΣ conversion is usually applied. The low price 8-pin micro integrated circuits providing 24-bits A/D conversion, like LTC2400 (Linear Technology) already exists on the market.

A lot of experiments using different conversion methods have been performed and their results have been compared [4, 5]. The multiple dual-slope (MDS) method shows the best effects. However, for the high accurate measurements authors developed their own A/D converter circuits based on the multiple dual-slope AD 6½ and 7½ digits AD conversion method.

The popular design based on earlier described way called dual-slope ADC, solves an inherent single-slop problem called calibration drift, which leads to inaccuracy over time because the integrator is not linked to the clock signal (i.e., the sawtooth waveform is not synchronized with the counter clock) [6].

2 Multiple Dual-Slope A/D Conversion

The dual-slope ADC (DSADC) is a type of analog-to-digital conversion which converts an unknown input voltage U_X into a digital representation through the use of an integrator, Fig. 1 [7]. The unknown input voltage is lead to the input of the integrator and allowed to ramp up for a defined fixed time period, i.e. the run-up period t_R. Then a known reference voltage of opposite polarity U_R is applied to the integrator and is allowed to ramp down until the integrator output returns to zero (the run-down period t_X).

The input voltage is computed as a function of the reference voltage, the constant run-up time period t_R, and the measured run-down time period t_X as:

$$U_X = U_R \frac{t_X}{t_R}. \tag{1}$$

The run-up period can be defined and is usually chosen as a number of clock pulses (1000 for example) to make the measured voltage value calculation

easier. If the reference voltage takes integer value, for instance 1 V, and run-down counter reaches value of 1234, the expression (1) becomes simply:

$$U_X = \frac{1\,\mathrm{V}}{1000} t_X = \frac{1\,\mathrm{V}}{1000} 1234 = 1.234\,\mathrm{V}\,. \tag{2}$$

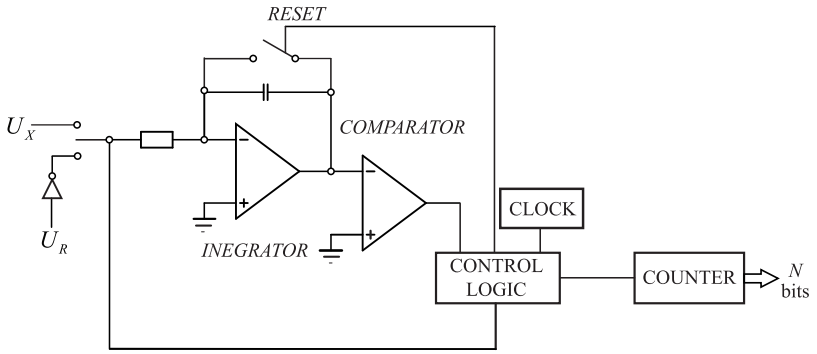

Fig. 1 – *Classical dual-slope converter block diagram.*

The run-down time measurement is also made in units of the converter's clock, in order to establish higher resolutions. Likewise, the speed of the converter can be improved by sacrificing resolution [8].

The resolution of the dual-slope integrating A/D conversion is determined primarily by the length of the run-down period and by the time measurement resolution, i.e. the frequency of the controller's clock. The required resolution in number of bits dictates the minimum length of the run-down period for a full-scale input [9].

The multiple dual-slope conversion is a modification of classical DSADC performing the conversion process multiple times and consequently, and measuring the cumulative time, i.e. total pulse number [10]. The overall principle scheme of the converter is shown in Fig. 2.

Fig. 2 is used to explain the A/D conversion process. In the initial state the upper D flip-flop is reset and low signal on its Q output turns the input switch to connect the measured U_X voltage to resistor R_1. The capacity charging starts by current I_X directly proportional to the connected input voltage, because the other resistor end is at the zero potential. During the integration period, i.e. the first phase, the integration capacitor voltage raises. It continues the defined time period measured by clock pulses, signal integrates in Fig. 3 [11]: for example 10 000. After that the D flip-flop output is changed and turns the switch to connect the referent voltage U_R to the integrator input. Because the voltage has the opposite polarity, the capacity discharging starts and it is the beginning of the second phase (de-integration, reference integrate). At the same time as a

signal RI (Fig. 2.) activates the pulse counter, the partial integration starts as well. The integration capacitor voltage now decreases.

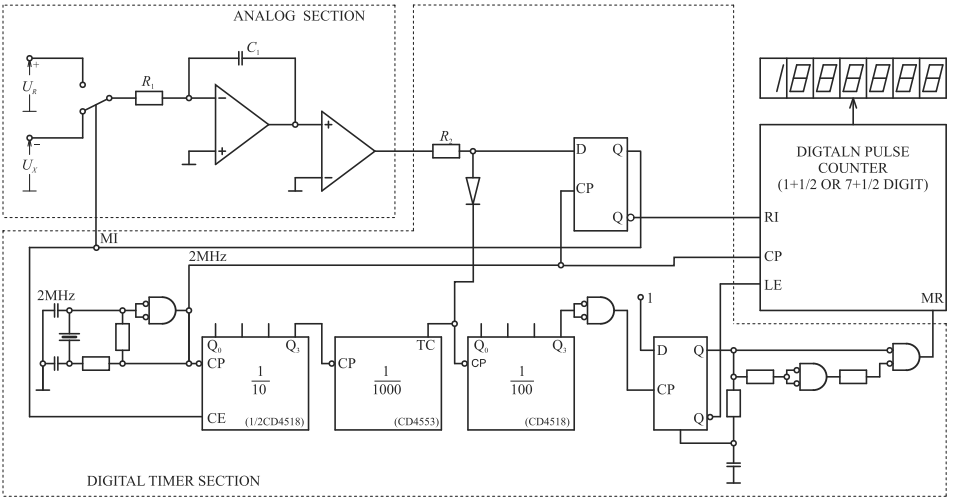

Fig. 2 – *The MDSAD converter overall functional diagram.*

For a better understanding, see Fig. 3, where the waveform at the integrator output is shown. So, t_R is fixed, while t_X duration is proportional to the value of U_X.

$$t_X = t_R \frac{U_X}{U_R}. \tag{3}$$

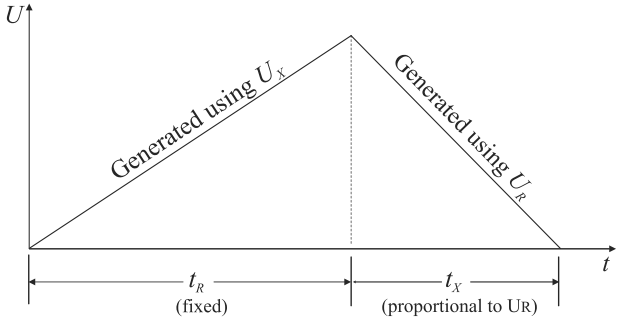

Fig. 3 – *Phases of dual-slope conversion.*

When it reaches the starting value, i.e. zero volts, the counted number of clock pulses is proportional to the U_X voltage intensity. At that moment the D flip-flop changes its state, the next partial conversion – which represents a new conversion cycle – starts. It is repeating the defined number of times; in our case 100 for 6½, and 1000 for 7½ digit conversion. At that time the complete

conversion process is finished. Throughout the entire period, the counter cumulates the number of clock pulses counted in every reference voltage integration phase.

The voltage on the integration capacitor (C_1 in Fig. 2) remains the same, i.e. zero volts, at the start and at the end of complete conversion process. It means that the capacitor charge stored in first integration phase by current I_X should be the same as that one, lead while the second de-integration phase, discharging by opposite current I_R. That can be expressed as:

$$\int_0^T \left(I_R - I_X\right) \mathrm{d}t = 0 \,. \tag{4}$$

where T is the duration of conversion. Assume that 6½ digit conversion is in question. For complete conversion process hundred partial integrations and de-integrations has to be performed, Fig. 4 - upper part. The expression (4) can be split in the partial sums and shown as:

$$\int_0^{t_1} \left(I_R - I_X\right) \mathrm{d}t + \int_{t_1}^{t_2} \left(I_R - I_X\right) \mathrm{d}t + \cdots + \int_{t_{99}}^{t_{100}} \left(I_R - I_X\right) \mathrm{d}t = \sum_{i=1}^{100} \left(I_R - I_X\right) \mathrm{d}t = 0 \,, \tag{5}$$

where t_i is the partial conversion (integration) duration, and i = 1, 2, 3,…, 100.

Every partial conversion consists of both charging i.e. integrating phase duration $t_{R,i}$ and discharging i.e. de-integrating phase duration $t_{X,i}$. Because the currents I_X and I_R are constants the previous expression becomes:

$$I_X \sum_{i=1}^{100} t_{R,i} - I_R \sum_{i=1}^{100} t_{X,i} = I_X t_R - I_R t_X = 0 \,, \tag{6}$$

where t_R is the duration of all integration periods (in that case $100 \times 10000 = 1000000$ pulses), t_X duration of all discharging i.e. de-integration periods expressed as total counted pulses number (n_X), and T is the total conversion time, $T = t_R + t_X$. If we note the constant counter frequency by f and numbers of pulses as n_X and n_R respectively, the relation between currents can be expressed as:

$$\frac{I_X}{I_R} = \frac{t_X}{t_R} = \frac{f n_X}{f n_R} = \frac{n_X}{n_R} = \frac{n_X}{1\,000\,000} \,. \tag{7}$$

The measuring and referent voltage comparison gives the next relation:

$$\frac{U_X}{U_R} = \frac{R_1}{R_1}\frac{I_X}{I_R} = \frac{R_1}{R_1}\frac{n_X}{n_R} = \frac{n_X}{1\,000\,000} = k_U n_X \,, \tag{8}$$

or

$$U_X = U_R \frac{R_1}{R_1}\frac{n_X}{n_R} = \frac{U_R}{1\,000\,000} n_X = k_U n_X \,, \tag{9}$$

where the constant k_U does not depend of resistance R_1 and in particular case it is:

$$k_U = \frac{U_R}{1\,000\,000}. \tag{10}$$

Obviously, the previous expression shows a relation between two currents, or voltages. Hence, it is very suitable for measurement of quantity as electrical resistance (the comparison method), measuring bridges adjustment, strain intensity etc.

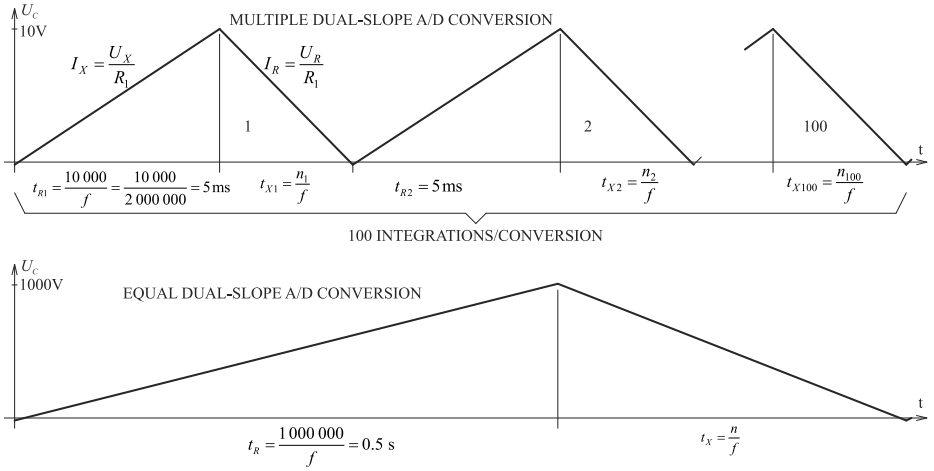

Fig. 4 – *Comparison between multiple and single DSAD conversion.*

If the referent voltage is set to integer number of volts (1 V for example), the counted number of pulses is equal to measuring current (in Ampere), or voltage (in Volt). All that is left within the process is to define the right decimal point position. In this case the maximal measuring voltage value could reach 7 V. The integration and de-integration is done using the same resistor, it is not a measuring error source and the resistance value is irrelevant. This choice has been made to allow the integration voltage wide area. The operational amplifier supply voltage of ± 8 V and referent voltage of 5 V give the counted pulse number of about 1 400 000. The ADC duration can be calculated as:

$$t_{ADC} = \frac{\left(n_R + n_X\right)}{f} = \frac{n_R}{f}\left(1 + \frac{U_X}{U_R}\right) \tag{11}$$

and the assuming the previous chosen values it is:

$$t_{ADC} = \frac{\left(n_R + n_X\right)}{f} = \frac{1\,000\,000 + n_X}{2\,000\,000} = \frac{1}{2}\left(1 + \frac{U_X}{U_R}\right). \tag{12}$$

If the voltage is zero, the time is 0.5 s, and for maximal value (10 V) the conversion takes near 1.5 s. For the 7-digit conversion the time is 10 times longer.

3 Realized Instrument

The multiple dual-slope A/D converter is designed and realized by the integration of three functional modules: analog section, digital control and timer and counter with display (Fig. 2).

The main task of analog module is to provide the voltages integration and de-integration, i.e. charging and discharging the integration capacitor [12]. It might be assumed that designing and realizing a high performance dual-slope converter is an easy job. However, this is not the case because there are too many error sources during the conversion and in a practical circuit a host of pitfalls must be avoided. These include the non-ideal characteristics of all elements and FET switches and capacitors as well, and the switching delay in the zero crossing detector [13]. The way how most of them have been overcame is described in that chapter, using Fig. 5.

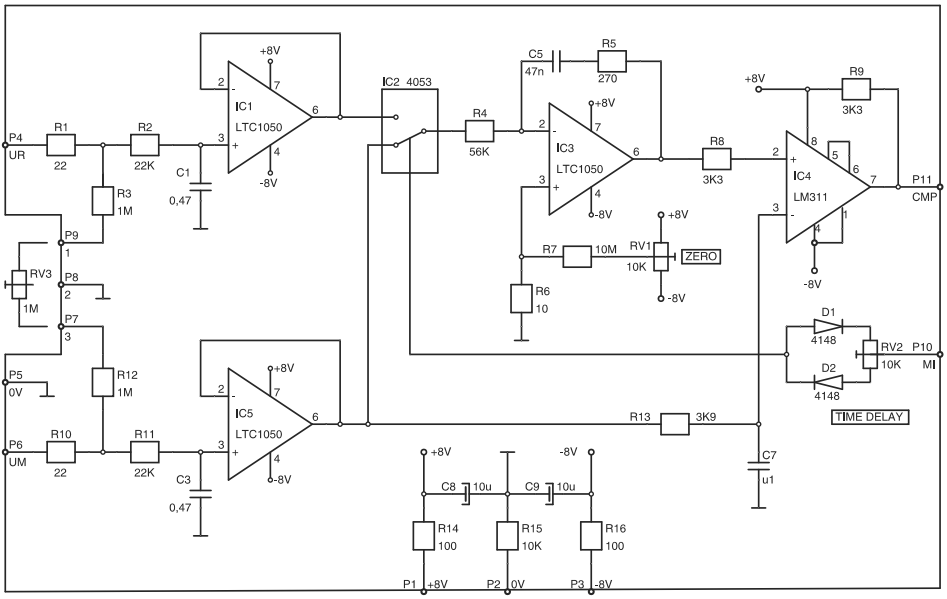

Fig. 5 – *Analog section of realized dual-slope converter.*

The integrated circuits IC1 and IC5 are the unity-gain amplifiers with very high input resistance. They have a role to lead the voltages U_R and U_M to the resistor R_4 eliminating the analog switches statically resistance. The resistors R_1, R_3, R_{10} and R_{12} together with potentiometer R_{V3} are in use for some small

conversion corrections. Using the chosen values it is possible to reach the ± 12 ppm of input voltages dissension. Input filters are made of R_2, C_1, R_{11} and C_3. The capacitors C_2 and C_4 eliminate transient occurrences appeared at the analog switch state changing. The permanent resistor R_4 connection to the IC1 and IC5 outputs via low switch resistance eliminates the input to switch output charge injection. The delay of switch state changing, i.e. transition time provokes the difference of switch-on and switch-off period duration. If this difference is 10 ns only, for one second conversion the error is about ±2 digits, or ±2 ppm. To eliminate that influence, the diodes together with potentiometer are used (the final version is realized by one diode and resistor and resistance is empirically determined) [14].

The operational amplifier IC3 together with capacitor C_5 runs as an integrator. The serially connected C_5 and R_5 (relatively low resistance) have the role to accelerate the changes of the integrator output voltage. In such a way comparators' reaction is faster. Although the IC3 input offset voltage is too small, the correction circuit build of potentiometer R_{V1} and voltage divider R_6 and R_7 is retained. There is a possibility for some of the offset voltage to occur, which is caused by thermo or similar effects. The drop in voltage appears due to printed circuits links on the board. Hence, the zero potential of input and power voltage is separated. But, a certain low voltage (about 10 μV) could occur as a consequence of very small current through the printed links. The mentioned correction circuit has to eliminate this and similar unwanted voltages. The voltage correction could reach about ±8 μV for the whole potentiometer range, and it is relative value of near ±1.5 ppm for the voltage of 5 V. All three operational amplifiers (type LTC1050) have very low input offset voltage of about 0.5 μV and small bias current (10 pA in range), slew rate is about 4 V/μs and amplifying above 140 dB. Because of the cited characteristics those circuits could be consider as the ideal operational amplifiers.

The dual-slope conversion has two phases. In the first one, i.e. the integration, the capacitor is charging. In the second phase, i.e. the de-integration, the integrator output voltage decreases to the initial value. Initial value should not be zero. If the comparison with zero is done, then the mean value becomes positive. However, because of the capacitor's imperfection and a dielectric absorption some unwanted phenomenon has been occurred. The solution of this problem is found in the special AD converter operation regime, when the mean value of capacitor voltage is near zero. The integrator voltage is changed within limits of $\pm U_M$ (Fig. 6 and 7). The simple analysis shows that the time constant of a half of integration period (0.005 s) provides the necessary conditions. It gives $R_4C_5 = 0.0025$ s. At last, the comparator output voltage is comparison by measuring one and signal goes out of this module. The most part of time this voltage is positive. When it becomes negative, the first positive

clock edge changes the analogue switch state and the next integration begins. The resistor R_5 is used to increase the integrator voltage and the output become high again. The integrated circuit LM311 is in use. The module is supplied by symmetrical ±8 V voltages. The resistors R_{14}, R_{15}, R_{16} and capacitors C_8 and C_9 have a role of power filter.

The main function of digital module (Fig. 6) is to provide all of control signals necessary for other sections to operate. The elementary clock of 2 MHz is produced by quartz oscillator. The clock accuracy is not as important as the running stability itself. Although the oscillator works very stable, the input voltage is additionally stabilized by resistor R_7 and Zener diode ZD1. The input diode D_1 protects the circuits of wrong input voltage polarity.

The main clock (2 MHz) runs the first IC4A decade counter, which output is connected to the input of three digits decade counter IC3, Fig. 6. In that sense the time interval of 10 000 pulses (5 ms) for measuring voltage integration is provided. During this time the diode D2 holds the flip-flop input *D* at the low level. The negative edge of 9998th clock pulse via pin 2 of IC4A sets the flip-flop (Q3 becomes high), Fig. 6. At that moment the output signal, TC (Fig. 7) of IC3 counter changes own state to high. It takes about 360 ns and the lower flip-flop input *D* is unblocked and ready to carry the comparator state at the first positive edge of next clock pulse. It is the edge of 9999th pulse. While the integration period the input voltage was positive and the flip-flop output *Q* was low.

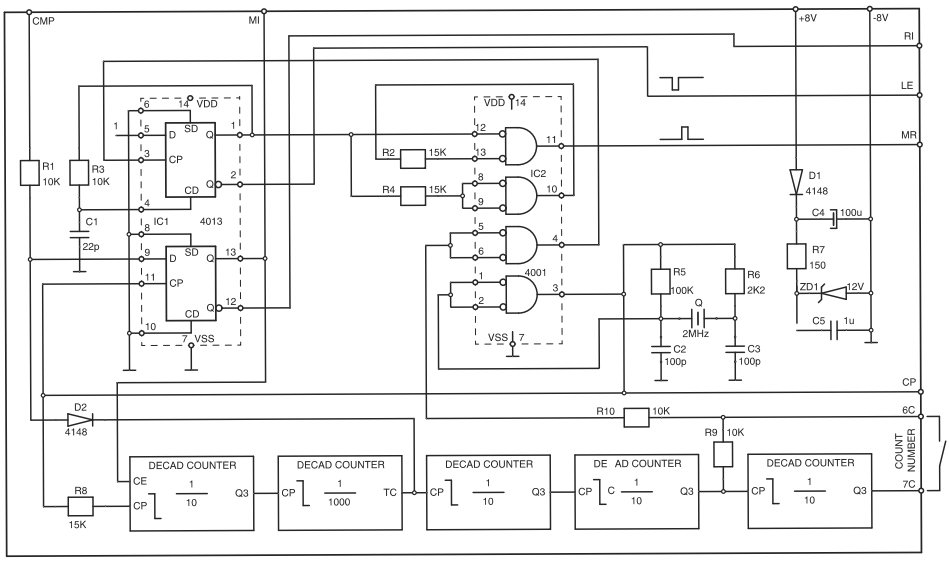

Fig. 6 – *Electrical scheme of digital section of MDSAD converter.*

At that moment it rises to high and changes the state of analogue switch (Fig. 5). The de-integration starts. It happens at positive edge of 9999th pulse with a delay of about 60 ns. At the same time the signal referent integration (R_I, i.e. de-integration) starts the counter to measure the capacitor discharging time. When the integrator output voltage drops below the comparison level, the analog switch changes its state. It is the end of a current partial integration. The next one starts and so on. The same process repeats 100 times. Throughout the entire period the counter increments but only in the de-integration periods. The end of 100th cycle resets the Q3 output of IC5A and this signal, via IC2 circuit sets the first monostable *D* flip-flop with a period of 250 ns. The same inverted pulse (LE – Latch Enable in Figs. 6 and 7) freezes the counter state (the total count of pulses) and enables it to be shown on a display. Inverted and delayed signal LE generates the master reset (MR) which clears the counter and prepares the new conversion cycle.

It is noticeable that the next conversion starts with the capacitor integration voltage at the end of previous cycle as the initial value. It is convenient for rounding the values; the result in previous step will be corrected by the actual one.

If the described process repeats ten times, the 7-digits conversion is performed. The added counter IC4B is used for those purpose.

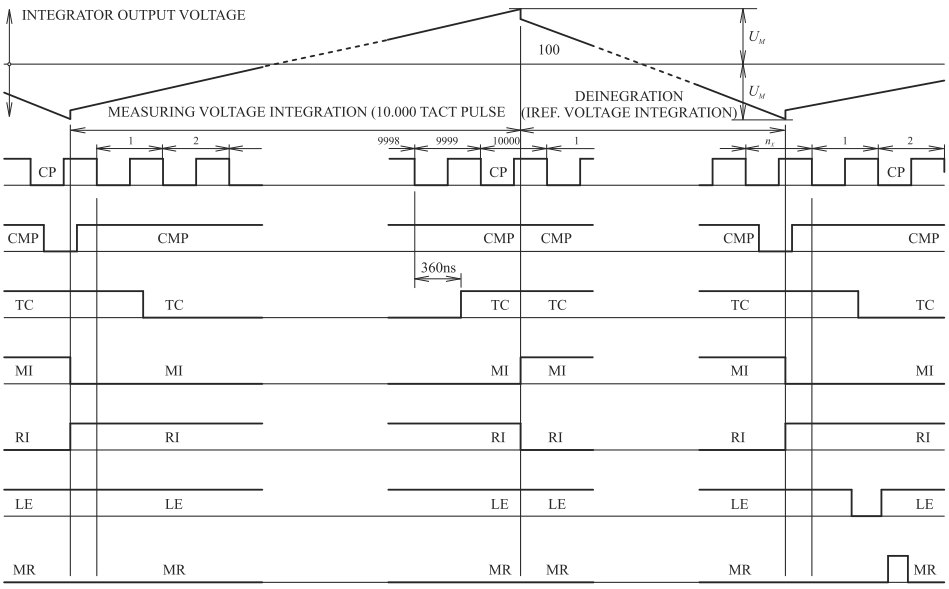

Fig. 7 – *The main conversion control signals*.

The digital counter and display module is designed as an autonomous part, because it could be used for other purposes as well (the frequency meter up to 10 MHz, for example). In this case, this is accomplished at digital parts board, and the CMOS circuits input protection resistors are omitted. The counter consists of three sections of three-digit CMOS serially connected counters type 4553 with multiplexed BCD outputs. The BCD outputs are connected to 7 – segment display via decoders 4511. The control signals generating in the digital module drive the display assembly. The whole digital module is supplied by 12 V and has the common minus pole with the analog section.

5 Functional Characteristics

Based on the described multiple dual-slope AD conversion method the instrument – resistor comparator is made.

Considering all of the occurred problems and using the proposed solutions, realized measuring unit reaches good performances. Some of the instrument measuring errors are not possible to compensate. For example: self discharge of the capacitor, drift of the offset- and reference voltage and uncertainty in the switching of the comparator. The error sources like:

- the difference of resistance in both analogue switch states,
- the analogue switch charge injection,
- the delayed time of analogue switch state changing,
- integration capacitor dielectric absorption and similar

are proven to be successfully overcame, mainly by the above discussed and proposed solutions. The instrument measuring results [15] achieved in practice are shown in **Table 1**.

Table 1
The realized instrument characteristics.

Measuring range	1 kΩ	10 kΩ	100 kΩ	1 MΩ	10 MΩ	100 MΩ	1 GΩ
Measuring current	3.6 mA	0.5 mA	50 μA	5 μA	500 nA	50 nA	5 nA
Electric power	13 mW	2.5 mW	250μW	25 μW	2.5 μW	0.25 μW	25 nW
Resolution 6/7 digits	1 mΩ/ 0.1 mΩ	10 mΩ/ 1 mΩ	0.1 Ω/ 10 mΩ	1 Ω/ 0.1 mΩ	10 Ω/ 1 Ω	100 Ω/ 10 Ω	1 kΩ/ 100 Ω
Comparison error(ppm)	1/0.2	1/0.1	1	10	100	0.1%	1%

6 Conclusion

For standards of lab measurements there is a need for high levels of accuracy. Because the response time is not of great significance, the described solution is convenient to improve the dual-slope AD conversion method [16].

Mentioned instrumentation method is usually used in the laboratories where high precision of metal resistances measuring is required and is necessary for determining its elementary characteristics [17]. In addition, there are several applications where high sensitivity is required, and such a method is very useful in those cases. Many instruments use similar measurement method to one presented in the paper [18]. However, the precision and the measuring scale of those instruments are significantly less than proposed one.

In the practical usage of the realized instrument a few unwonted effects occur. These effects are making the additional problems and insecurities in the measuring results worse. This paper describes some more or less conventional metrology methods which have been developed and applied to improve and determine the realized instrument performances. In general, the simple fundamental methods seemed to produce the best results. There are often several valid ways to achieve the same objective in metrology, and the methods chosen are somewhat dictated by available standards and equipment.

The method presented here may not be practical in every laboratory, but this should at least provide ideas for alternative measuring methods.

7 Acknowledgment

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