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An FPGA implementation of a Quantum Analog to Digital Converter

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***Abstract*—This paper presents the development of a Field Programmable Gate Array (FPGA) hardware description applied to a novel Analog-to-Digital converted based on a Josephson Arbitrary Waveform Synthesizer. The aim of this system is to reduce uncertainties and obtain direct traceability for voltage waveform measurements at input frequencies up to 1 MHz. The FPGA controls a high frequency ADC and an optical transceiver which is used to drive a Josephson junction array (JJA) at 10 Gbps. It also filters the ADC readings and transfers the measured data to a PC via 1 Gbps-Ethernet.**

***Index Terms*—Analog-digital conversion, FPGA, Josephson effect, Signal sampling, Sigma delta, Voltage measurement.**

I. Introduction

High-accuracy analog-to-digital (ADC) and digital-to-analog (DAC) converters are used nowadays in many applications, for example in audio players, electrical energy measurements and in medical devices. These components must be characterized in terms of effective resolution, noise-free bits, distortion and other parameters. The electrical metrology community is concerned with the traceability and uncertainty of these measurements in order to ensure their quality and allow the development of improved instrumentation and devices [1].

The EMPIR joint research project 15SIB04 QuADC [2] aims to develop a quantum-accurate ADC based on Josephson junction arrays (JJAs) in order to reduce the uncertainty of voltage waveform measurements up to input frequencies of 1 MHz. The target uncertainty levels require 17 effective bits for high frequency signals and 27 bits for low frequency input signals, up to 1 kHz.

The core of this novel ADC is a Josephson Arbitrary Waveform Synthesizer (JAWS) [3], based on a JJA consisting of SNS (superconductor - normal metal - superconductor) junctions. When a high frequency current pulse is applied to the JJA it generates a quantized voltage-time integral pulse. Therefore, a quantum accurate voltage is obtained using a pulse pattern, i.e. pulse width modulation (PWM), and averaging these quantized voltage pulses over time. In this way, the system generates low distortion signals using high frequency binary pulses.

A simplified block diagram of the QuADC is presented in Fig. 1. The signal to be measured and a feedback signal are fed to an amplifier where they are subtracted. The amplifier output is filtered with a low-pass filter to push the high frequency noise far away from the signal bandwidth. Then, the filter output is measured with a low resolution quantizer, implemented with a commercial ADC. A decimator filter processes the quantizer readings in order to increase the effective resolution. The feedback signal is generated by the JAWS, which is driven in real-time with a Field Programmable Gate Array (FPGA) that produces a PWM pulse pattern proportionally to the quantizer reading. The PWM codes are stored in a look-up table (LUT) which is addressed by the quantizer readings. The indexed data is loaded into the input register of an optical interface to produce an optical pulse pattern. These pulses are transmitted by an optical fibre to a photodiode used to drive the JJA which is located in a cryostat at 4.2 K. An FPGA is a good solution to perform all this task because it is flexible, it has low latency and can be synchronized with an external signal.

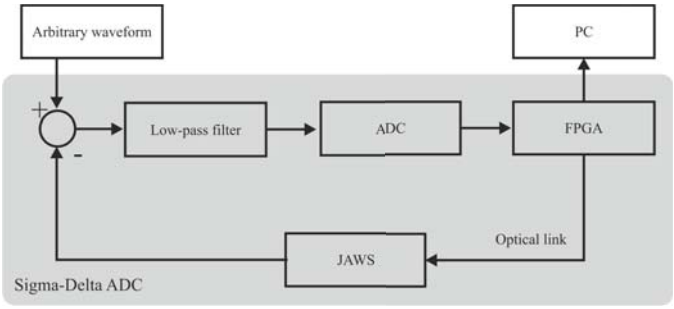

Fig. 1. Simplified block diagram of the QuADC, the shadowed box indicates the sigma-delta ADC. The voltage difference between the generator under test and the JAWS is fed to a low-pass filter. Its output is measured with the ADC and the FPGA drives the JAWS in order to cancel the ADC reading. The measured values are processed in the FPGA and transferred to the PC.

This topology produces a sigma-delta ADC, taking advantage of a low-pass filter to push the noise out of the signal bandwidth and of a decimator filter to eliminate the high frequency noise. In this way, a fast oversampling with a resolution of a single or small number of bits is used with digital filtering to exchange resolution for bandwidth [4]. The low-pass filter was designed as a 4^{th} order continuous-time sigma-delta modulator with a topology of cascade of integrators with feedforward summation (CIFF structure) [5].

II. FPGA design

Fig. 2 presents the system block diagram, including the signal paths and system clocks. The system is controlled by a Xilinx Zynq-7000 FPGA (model XC7Z045 FFG900-2) implemented in the evaluation board ZYNQ ZC706. This device reads the ADC and generates the pulse pattern. These operations are synchronized using three clocks linked via a

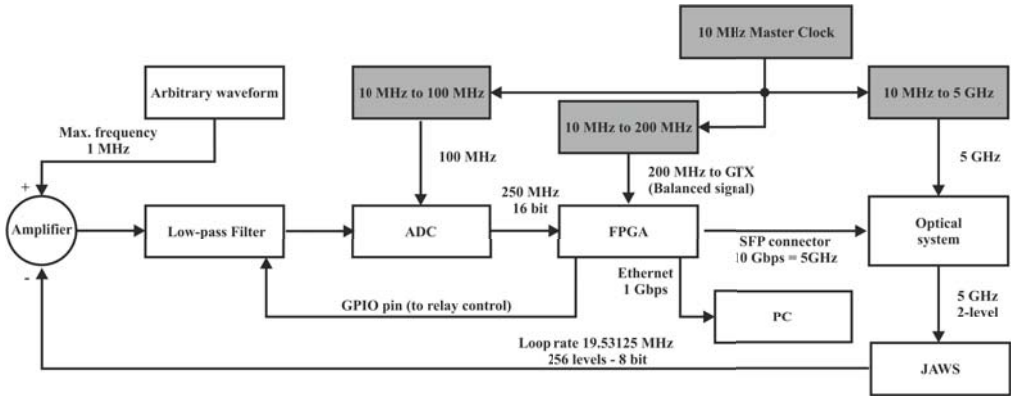

Fig. 2. Block diagram of the QuADC indicating related clocks. The ADC, FPGA and the optical system are synchronized with a 10 MHz master clock and using some clock generators, which are identified in grey.

10 MHz timing link. The FPGA filters the ADC readings and communicates with PC to periodically transfer the processed data. The communication with the PC is performed by 1 Gbps Ethernet. In addition, the FPGA controls some relays included in the filter to reset its capacitors, to zero the voltage input and to invert the voltage inputs. The hardware description is written in VHDL93 and the system is implemented using Vivado 2017.4. Fig. 3 shows the main functional block of the FPGA hardware description.

The quantizer is implemented with the commercial board FMC164 from 4DSP (now Abaco Systems). The ADC board is connected to the FPGA through the FMC VITA 57.1 connector. The IP core FMC16x [6], mainly based on IODELAY and SERDES primitives, was developed to deal with the ADC board.

The Processor System (PS) of the Zynq is used to control the GigaBit Ethernet and 4 million ADC samples can be sent to the PC. The decimator filter was designed as a cascade of two finite impulse response polyphase filters. The first filter reduces the sampling frequency by 2 and the second by 5, giving an equivalent sampling frequency ten times lower. The system has two main operating modes. One is the stand-by and configuration state, where the system can be configured and waits until the measurement start. The other is the measurement mode, where the feedback loop is closed and the FPGA performs the tasks described above.

The JAWS update time, defined by the time difference between two consecutive outputs of the LUT, determines the closed-loop rate and period. In that time interval the FPGA must read the ADC, index the LUT and output the appropriate pulse code to drive the JJA. Therefore, the total delay between acquisition and feedback have to be close to the loop period, its maximum value is 200 ns corresponding to a loop rate of 5 MHz.

A. A Josephson digital-to-analog converter

The Josephson junction array is used by the FPGA as an ideal DAC. In the first prototype, the loop rate is between 5 MHz and 20 MHz, and the JAWS will be driven at 10 Gbps. Therefore, to use the JAWS as a DAC, an upsampling from MHz to GHz is performed by the PWM method, which allows interpolation, increasing the effective resolution. For example, if a loop rate of the order of 20 MHz is required, the pulse pattern for one row of the LUT must have 500 high frequency pulses, (since 10 Gbps$/$20 MHz). This value is replaced with $512 = 2^8$ to use a binary size and the loop rate is adjusted to be 19.53125 MHz. The JAWS system requires return-to-zero (RZ) current pulses in order to generate quantized voltage pulses. Therefore, in between every value in the pulse pattern a data bit equal to zero must be added. The LUT stores 256 configurable values and the RZ pulses are added in software by the FPGA. The mean value of each row gives the corresponding DAC level and the resolution can be calculated as the full scale divided by 256. Thus, an equivalent 8-bit DAC is obtained, that goes from zero up to full scale minus the resolution. When a given ADC reading indexes the table, the corresponding row will be transmitted. After sending the last value of that row, a new ADC reading indexes the table. Therefore the FPGA will send a constant flow of pulses and the output of the implemented DAC does not return to zero.

A sample from the ADC is recorded at a rate equal to the closed loop frequency and the eight most significant bits (MSB) are used as the address of the 256 bit x 256 rows ROM, which implements the LUT. Then, the output of the LUT is RZ coded and sent at 10 Gbps through a GTX transceiver. The output of the GTX is connected to a Small Form-factor Pluggable (SFP+) tranceiver. The pulse sequence is transmitted as raw data with the lowest jitter available, and without pauses or flow control bits. These last ones are not required since the JJA will convert each pulse into a quantized output guaranteeing zero bit lost or data corruption. The GTX transceiver requires a balanced clock input of 200 MHz via specific SMA connectors to generate the 10 Gbps.

B. Clocks and Timing

The system is synchronized with a master clock of 10 MHz from which three other clocks are derived for use as a reference clock for the ADC, the GTX transceiver and the

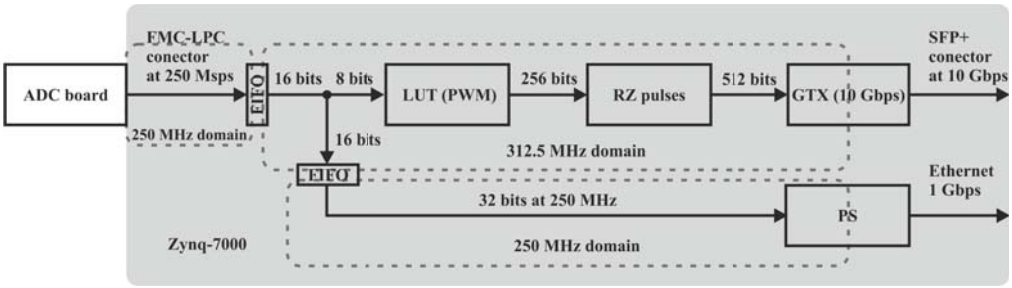

Fig. 3. Block diagram of the FPGA indicating the clock domains (dashed boxes). In the 312.5 MHz domain, the FPGA indexes the LUT, convert to RZ pulses and feeds the GTX transceiver. The processor system is used to communicate with a PC. All the domains are connected with FIFOs.

optical system [7], see Fig. 2. Inside the FPGA, the three subsystems, the FMC16X core, the PS and the SFP, are in unrelated clock domains. As a Clock Domain Crossing (CDC) technique, small FIFOs were used (IN_FIFO primitives). This organization is presented in Fig. 3.

The external clock to the FMC164 board synchronizes the sampling clock and the communication with the FPGA, this clock defines the corresponding domain. The FPGA reads all the time the ADC at 280 MHz. However, to index the LUT the most recent value is used.

The GTX is configured to work at 10 Gbps with 32 bit data packages. The clock of the GTX subsystem is therefore $10\ \text{GHz}/32 = 312.5$ MHz. Each row in the LUT has 256 bits which must be doubled to be converted to RZ pulses, so 512 bits are sent to the GTX in 16 packages of 32 bits.

The measured output of the ADC is transferred to the PC at 250 MHz and it is not synchronized with the master clock. This data is outside of the feedback loop and can therefore be processed at an arbitrary rate without altering the system performance.

C. GTX

The Xilinx 7 Series FPGA Transceivers Wizard was used to configure two identical GTX. One of them is used to output the data at 10 Gbps. The other is used for debugging and is configured as a 5 GHz clock, output via SMA connectors. Both GTX were configured for 32 bit inputs at 312.5 MHz, without any custom coding required. Xilinx recommends the use of an external clock source for the GigaBit transceivers. However, for testing purposes, the GTX Transceiver wizard files were modified to provide an internal clock for the GTX from the PS.

III. Validation and test

For test purposes, extra functionality was added using push buttons and dip switches of the evaluation board ZC706. Three push buttons were used to guarantee a known pattern at the LUT output, fixing its input as bottom, middle and upper values. The dip switches were used to multiply the number of ADC samples by 2, 4 and 8 respectively.

A Python script was developed to control the IP core and to obtain data. The user can specify the desired quantity of data and the ADC clock source. In addition, the data source can be selected to be either the ADC sample or an internal counter, which is useful to test the data transfer. The data received is saved to a file and another Python script is used to produce graphics in order to examine the recorded date.

The pulse pattern output was examined and some results are presented below. In all the cases, the GTX output was transmitted as an electrical signal via an SMA connector and measured with an oscilloscope of 12.5 GHz of bandwidth. In addition, a pulse signal to identify the start of each LUT row was included when the first data package is sent to the GTX transceiver.

A. Pulse pattern

The output pulse pattern was verified in order to obtain the correct generation. Fig. 4 shows an example obtained with a low frequency sinusoidal signal input. It is clear that the pulse density changes between the consecutive PWM patterns, corresponding to different DAC levels. The pulse pattern was verified by counting the number of positive pulses within a loop period.

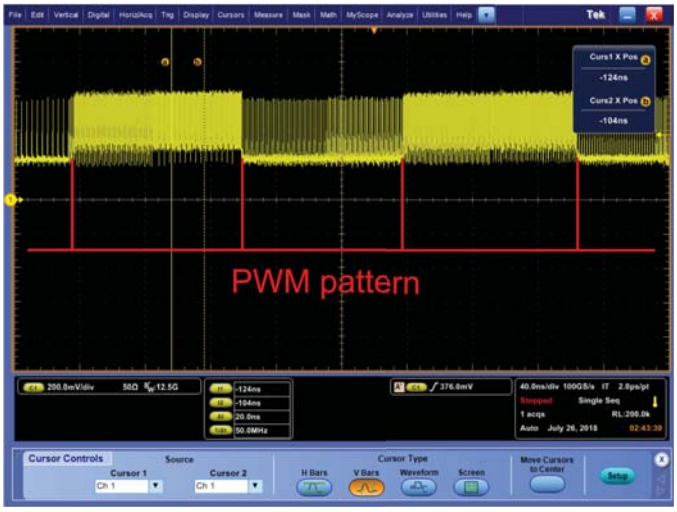

Fig. 4. A pulse pattern corresponding to a low frequency sinusoidal signal, the PWM pattern can be observed.

B. 10 Gbps electrical signal jitter

A pulse train signal was configured in the FPGA and the output signal was measured by the oscilloscope. The measured

jitter was less than 3 ps. Fig. 5 shows an eye diagram of the 10 Gbps output.

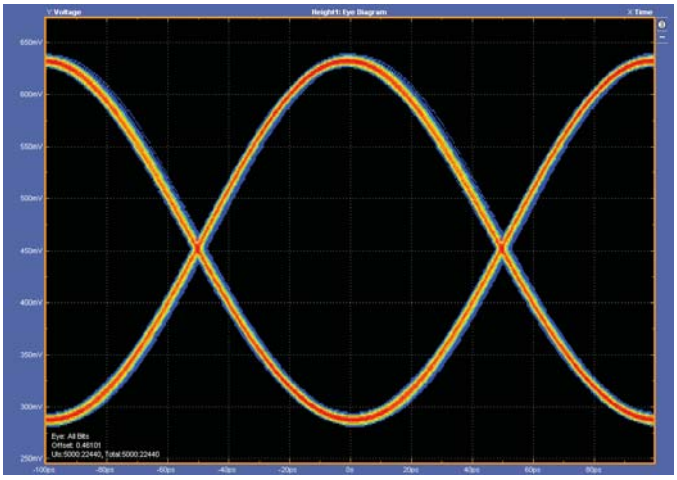

Fig. 5. Eye diagram of the 10 Gbps electrical signal showing a low jitter.

C. GTX delay

To measure the delay time between the LUT row being sent to the GTX transceiver and the output of the first data pulse, the trigger signal described above and the GTX output were examined as shown in Fig. 6. In this test, a full scale pulse pattern was generated and the theoretical mid point of the pattern was found with the cursor 'a' and the trigger signal. The measured mid point of the pattern was found with the cursor 'b' and knowing the theoretical full scale pattern. The time difference between a and b corresponds to the GTX delay time and was found to be 21 ns. This is equivalent to a delay of 6.5 cycles of the 312.5 MHz clock.

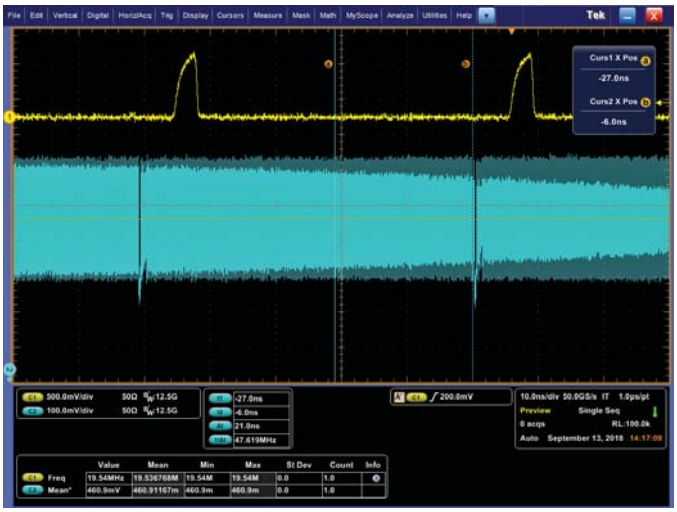

Fig. 6. Measurement of the GTX delay. The upper signal corresponds to the trigger and the lower signal is the GTX output. The pulse pattern was verified counting the number of positive pulses within the PWM pattern.

IV. Results

The whole system includes the QuADC IP core and adds an AXI4-Stream Data FIFO and AXI DMA, both from Xilinx. Also, the PS, the system reset and two AXI interconnect blocks must be considered. As common resources, 3059 LUTs, 4065 FFs and 8 BRAM were occupied. A shared GTXE2_COMMON and two GTXE2_CHANNEL primitives (one for normal data and one as 5GHz clock for test) were used. The ADC clock recovery uses one IDELAYE2 and one ISERDESE2, and additional four ISERDESE2 are consumed for the four data wires. Finally, two IN_FIFO were used for CDC.

V. Conclusion

A quantum analog-to-digital converter is under development with the aim of improving voltage waveform measurement traceability at frequencies up to 1 MHz. The system will be managed with a state-of-the-art FPGA. It reads a low-resolution high speed ADC, generates an optical pulse pattern to drive a Josephson Arbitrary Waveform Synthesizer, filters the ADC data and communicates with the PC. Tests were successfully performed in order to verify correct pulse pattern generation for a given ADC reading. The pulse pattern output was studied and a jitter of 3 ps and a GTX transceiver delay of 21 ns were measured.

Further works will be made in order to improve the design. The most relevant is to implement a new ADC with a higher sampling frequency and smaller delay. The memory size available to record data will be increased and communication with a PC will be implemented by 10 Gbps Ethernet.

Acknowledgment

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