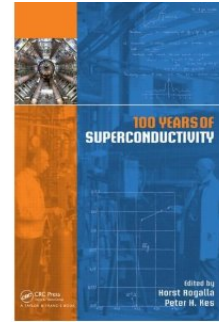


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7.8 History of Superconductor Analog-to-Digital Converters

Oleg Mukhanov

An Analog-to-Digital Converter (ADC) is a mixed-signal electronic circuit that converts an electrical signal from the analog domain to the digital domain, typically providing N binary bits at the sampling frequency f_s . The higher speed of superconducting circuits comparable to conventional circuits provided an initial interest in superconductor technology for ADC applications. One can find technical details of superconductor ADCs in earlier reviews, e. g., [1], [2]. In contrast here, we focus on a historical perspective of the ADC development identifying important trends and milestones as well as acknowledging main actors.

Similar to superconductor digital electronics, early superconductor mixed-signal circuits were based on cryotrons, pre-Josephson switching elements. A patent for the first superconductor analog-to-digital converter (ADC) was filed in 1960 [3], just in a few years after the initial cryotron-based digital circuit implementation. The projected speeds of the order of microseconds per ADC switching operation was rather attractive goal at that time. Several years later, the cryotrons were replaced by faster Josephson junctions in superconductor circuits including ADCs. The early Josephson-junction based ADC was a simple thermometer-code "totalizer" circuit patented in 1969 and presented an A-to-D conversion idea rather than a complete ADC circuit [4].

The first superconductor ADC circuit of a practical significance was a successive-approximation ADC invented in 1974 by M. Klein of IBM [5]. It consisted of a sample-and-hold circuit and four comparators made of serially connected Josephson junctions being switched to a voltage state at a predetermined control signal levels. This design was fabricated and tested in 1977 to show a 25 MHz bandwidth. In general, this ADC design was following semiconductor implementations using Josephson junctions. All early ADCs were focused on exploiting only the high switching speed of superconducting devices starting from cryotrons and then Josephson junctions. As in digital circuits, these first ADCs were viewed as a faster version of their semiconductor counterparts.

The realization that superconductivity offers much more than the higher speed led to innovations in ADC circuits. These new truly superconductive ADCs were exploiting fundamental features of superconductivity unavailable in other technologies: magnetic flux quantization, extremely high sensitivity, quantum accuracy, and low noise. For instance, the magnetic flux quantization provides a natural ruler which may be used to provide a large number of quantum-mechanically accurate thresholds for the ADCs.

Newer superconductor ADCs generally fall into two categories: *Nyquist-sampling parallel* ADCs and *oversampling* ADCs. An ideal Nyquist ADC samples a signal at a sampling rate $f_s = 2f_N$, where f_N is Nyquist frequency. The Nyquist ADCs are usually composed of a large number of *separate quantizers* arranged in parallel – each defining a single quantization level. The performance of such an ADC is limited by the precision of the quantization levels. These parallel-type ADCs are best for digitizing *high bandwidth signals* when a *moderate resolution* up to 8 bits is adequate.

In the oversampling ADCs, the signal is sampled at a frequency $f_s \gg 2f_N$ using a *single quantizer*. Then, feedback techniques and digital filtering are used to reduce or shape (move out of band) the

quantization noise and enhance the effective dynamic range. Oversampling ADCs are built using a “delta” or more often a "delta-sigma" modulator (sometimes called "sigma-delta"). In semiconductor technology, more robust sigma-delta ADCs are overwhelmingly preferred to delta ADCs. In superconductor technology, the availability of a close-to-ideal integrator in the feedback loop makes delta ADCs practical. The oversampling-type ADCs are best for digitizing relatively *lower bandwidth signals* but with the *maximum possible resolution*.

Superconductor Parallel-Type ADCs

Early Superconductor Parallel ADCs: Historically, the very first true superconductor ADC was of the Nyquist type, more specifically – a parallel-type Flash ADC. In 1975, H. Zappe of IBM pioneered the idea that periodic nature of superconducting quantum interference devices (SQUIDs) allows the formation of an n -bit flash ADC with only n comparators, rather than the 2^n-1 single-threshold comparators usually required in the conventional semiconductor flash ADCs [6]. It provides a unique solution for drastic reduction of a circuit complexity, and at the same time, allows faster sampling.

This ADC design signifies the first use of superconductor’s natural magnetic flux quantization. It also exploited the extreme field sensitivity of quantum interference devices, so that a very small analog signal could be converted. This was a truly pioneering invention. This first ADC design relied on the use of SQUID comparators with different inductance values and therefore was difficult for a practical ADC implementation. These difficulties were resolved by 1979, when R. Harris, C. Hamilton and F. Lloyd of NBS (now NIST) demonstrated a 200 MS/s 4-bit Flash ADC circuit using a Pb-alloy fabrication process [7]. They improved Zappe’s design by using optimally designed identical SQUID comparators with variable the coupling of signal (Fig. 1).

This work inspired a significant activity aimed to improve the ADC accuracy-bandwidth performance. Hamilton and Lloyd proceeded to demonstrate a 6-bit ADC at 4 GS/s [8]. By 1988, S. Ohara, T. Imamura, and S. Hasuo of Fujitsu extended sampling rate to 5 GHz by implementing the ADC using a 3- μm Nb/ AlO_x /Nb process [9]. A great deal of the development took place in University of California, Berkeley (UC Berkeley), NBS/NIST, and TRW aimed to the development of better SQUID comparator [1].

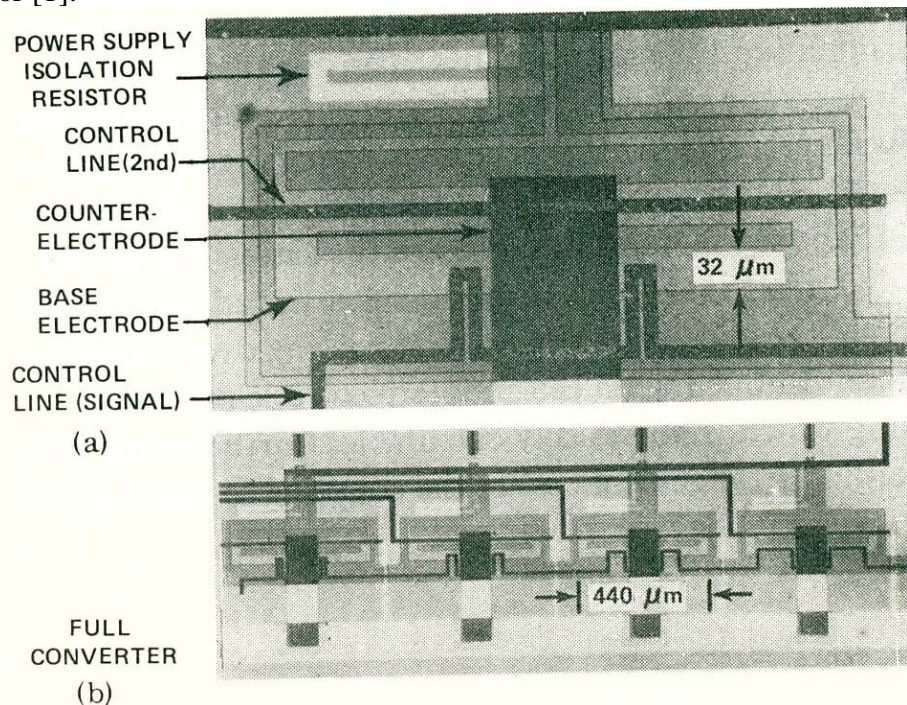


Fig. 1. The 1979 world’s first implementation of superconducting flash ADC at NBS/NIST [7]: (a) microphotograph of one of 4 SQUID Flash ADC comparators. (b) microphotograph of a complete 4-bit ADC.

Quasi-one junction SQUID (QOS) Comparator for Flash ADC: The most significant and influential flash ADC improvement was the 1988 invention of the QuasiOne-junction SQUID (QOS) comparator by H. Ko and T. Van Duzer at UC Berkeley [10]. This new comparator had a greater than 5x improvement over the previous designs in analog bandwidth and sampling rate. The main design goal was to eliminate the hysteresis and dynamic distortions caused by the vortex-to-vortex transition in the two- and three-junction SQUID comparators. This was achieved by a low-inductance, one-junction SQUID. For signal sampling, an additional junction was inserted in the one-junction SQUID loop (Fig. 2a). This QOS comparator set the design trend for many years. Even today, the QOS remains the basis for the latest ADC comparator designs.

In following years, the QOS-based flash ADCs were extensively developed for instrumentation applications, such as wideband transient digitizers. P. Bradley of HYPRES (originally from UC Berkeley), demonstrated a 6-bit Flash ADC with about 4 effective bits at 5 GHz and 3 effective bits at 10 GHz using a beat frequency test method [11]. The flash ADC consisted of a linear array of six active comparators with analog signal applied via an R-2R ladder and producing a Gray-coded digital output. In 1993, this Flash ADC was cryopackaged within an APD Gifford-McMahon (G-M) cryocooler and successfully operated as a rack-mounted demo unit at HYPRES (Fig. 2b,c). In fact, this was the first superconducting ADC (or any digital or mixed-signal LTS integrated circuit) operating on a 4K closed-cycle refrigerator.

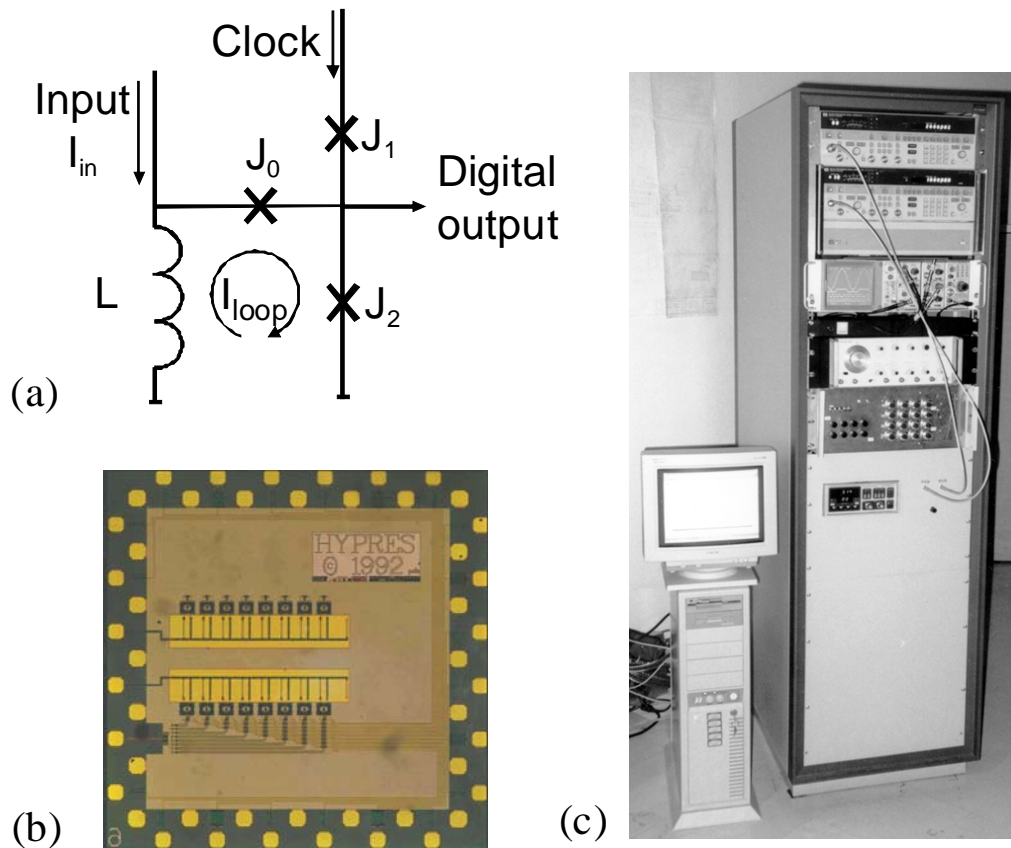


Fig. 2. (a) Schematic of Quasi One-junction SQUID (QOS) comparator (1988) [10]. (b) HYPRES 1992 4 GHz Flash ADC chip based on QOS comparators and fabricated using the 1993 standard HYPRES 3- μ m process. (c) The demonstration setup of a cryocooled 4 GHz Flash ADC using a 3-stage APD HS-4 cryocooler with a 1 W capacity at 4.2 K. The cryocooler cold head occupied the bottom compartment while test equipment occupied the top compartment of the standard rack.

SFQ Flash ADC: The demonstrated flash ADC design was quite successful, although it suffered from so called “duty cycle” problem when thresholds for the rising and falling edges appeared to be shifted for high slew rate signals. At that time, a paradigm shift from the latching type to non-latching single flux quantum (SFQ) logic influenced the designs of flash ADCs. Consequently, two new SFQ ADC comparators were proposed. One of these designs was based on Quantum Flux Parametron

(QFP), which provided high accuracy although was too complex. The alternative SFQ comparator design was introduced by S. Rylov of HYPRES in 1997 [12]. This SFQ comparator followed the general QOS basic design but was implemented using RSFQ design principles with shunted Josephson junctions and was integrated with a SQUID wheel (a phase tree). The duty cycle problem was compensated to a substantial degree by the insertion of a simple negative feedback resistor. This design became the comparator of choice for HYPRES transient digitizer.

Getting more Bits: Error-Correction and Interleaving: Like all parallel ADCs, the superconductor flash ADC is susceptible to fabrication mismatches in circuit components and conditions. This flaw can be corrected with a real-time digital error correction technique, called the look-back algorithm. This technique was developed by C. Anderson of IBM in 80s and then finally published in 1993 [13]. In this scheme, two comparators, offset from each other by a dc $\Phi_0/4$ flux bias, are used for each bit. This ensures that at most one comparator can be close to threshold for any input signal value. The look-back error-correction logic also converts the original Gray code output to standard binary. Furthermore, one can synthesize additional bits of lower significance. In addition to the error-correction, the bit-interleaving technique can be used to add one more bit of resolution without increasing the slew rate of a comparator. It adds an additional least significant bit (LSB) by XOR-ing outputs of 90-degree phase shifted (interleaved) additional comparators.

Applications: Transient Digitizer based on Flash ADC: Finally, all these techniques led to the development of a transient digitizer. There are several important areas of scientific and commercial instrumentation in which the precision, speed, and dynamic range of superconductor ADCs are of a great interest.

One of the key technical difficulties in the development of the high-speed flash ADC digitizers is the output interface bandwidth. A superconductor flash ADC produces digital output data at tens of Gbit/s which exceeds today's data link per line capabilities and speed of semiconductor electronics. The only way to connect to the conventional world is to slow down the data using two possible approaches: *on-chip memory buffering* and *demultiplexing*.

Fig. 3 shows a transient digitizer developed at HYPRES by S. Kaplan et al. in 1998 [14] using an on-chip memory. It consists of a superconductor flash ADC, combined with fast RSFQ shift register memory circuits to store the digitized data for subsequent readout at much slower data rate. A prototype instrument, comprising a superconductor integrated circuit (Fig. 3b) along with a room temperature interface and data acquisition electronics, was demonstrated for single-shot pulse capture. Each digitizer chip contained a 6-bit flash ADC coupled to a bank of 32-stage shift registers through a set of acquisition control switches. Despite the superior ADC performance compared to the semiconductor counterparts, the low capacity of the digitizer memory was the limiting factor for commercialization. As in the case of digital processors, the lack on a large capacity memory prevented the insertion of superconductor digitizers into a marketplace.

An alternative transient digitizer design proposed by M. Maezawa, et al. in AIST, Japan in 2001 was based on the use of demultiplexers [15]. The digitizer consisted of a 2-bit 16 GS/s flash ADC similar to the one described above. It was followed by a 1:16 RSFQ demultiplexer and output drivers. This demultiplexer-based architecture can avoid the superconductor memory bottleneck. However, the number of output lines are larger by the demultiplexing ratio (e.g., by 16), which presents a cryopackaging and cost challenge for faster and higher resolution ADCs.

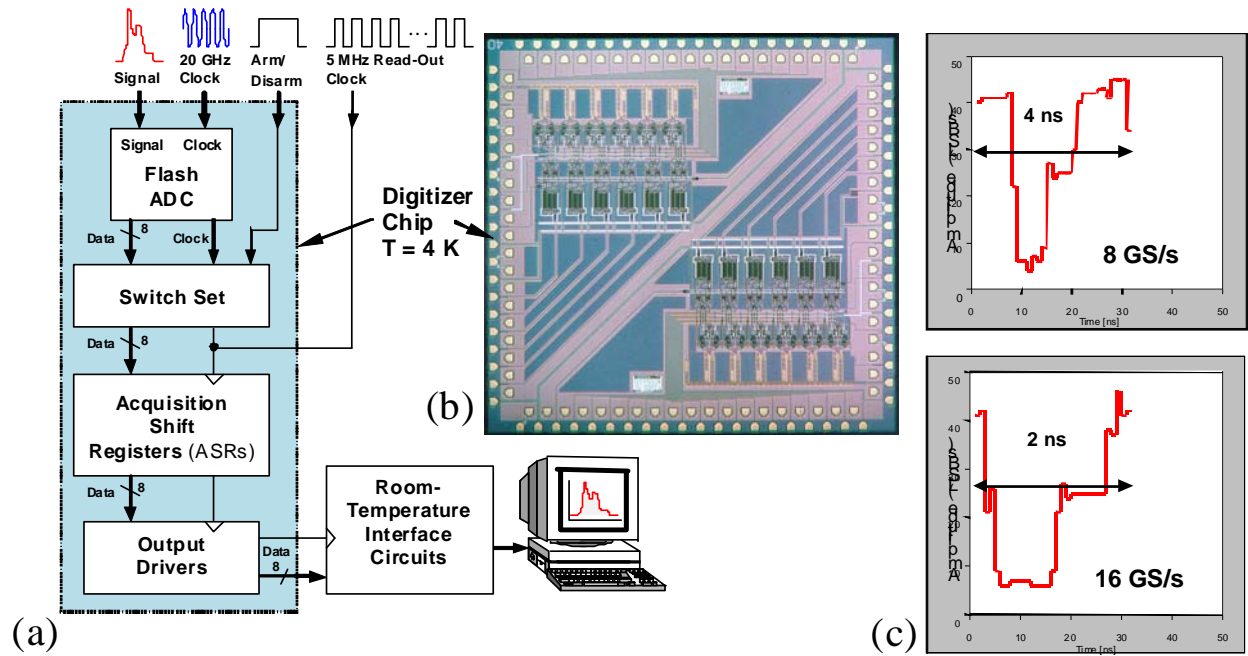


Fig. 3. A 1998 HYPRES superconductor transient digitizer: (a) Block diagram. (b) A superconductor chip with two transient digitizers based on a 6-bit flash ADC and a 32-bit-deep memory. (c) A fast pulse capture: 4 ns for 8 GS/s (top) and 2 ns for 16 GS/s (bottom).

Recent Flash ADCs: Complimentary QOS Comparator: Relatively fast development of parallel-type superconducting ADCs in the 1980s-1990s was considerably slowed after 2000 by the lack of dedicated government-sponsored development programs, requirements for the superfast transient measurements, and competition from conventional instruments. Similarly on commercial marketplace, product development goals were shifted from instrumentation to wireless communications which required a different ADC type – oversampling ADCs. Fortunately, recent attention to ultra-fast optical communications has been renewed after several years of low interest caused by the “dark fiber” overcapacity problem. This has opened an attractive opportunity for flash ADCs in the optical communication systems and their measuring instruments. Sampling speeds exceeding 100 GS/s became a target for the flash ADCs.

In 2008, H. Suzuki et al. from the SRL ISTEK, Japan, invented a new flash ADC comparator capable of operating with the required speed if fabricated with a 40 kA/cm^2 critical current density process. The new comparator is the latest development of the famous QOS comparator – Complementary QOS (CQOS). It finally solved the long-standing “duty cycle” problem plaguing previous QOS designs. The new design is based on a differential pair of the identical SFQ QOSs connected at the decision-making part. The signal is applied to both QOSs complementarily (Fig. 4a) and cancels the asymmetrical distortions [16]. In 2010, a 4-bit CQOS comparator test circuit showed the 3-bit binary and 4-bit Gray-code operation at 15 GS/s in beat frequency tests. For low frequency input, correct high-speed sampling operation up to 50 GS/s at 10 kA/cm^2 were observed. A complete 5-bit flash ADC with the look-back error-correction and bit-interleaving circuits (Fig. 4b) was assembled for testing on a 1 W G-M cryocooler [17].

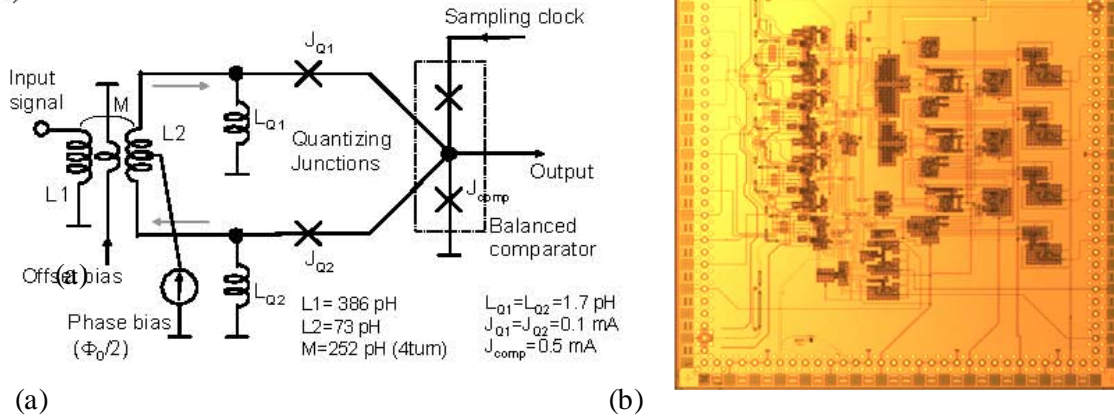


Fig. 4. A 2008 Complimentary QOS comparator Flash ADC (ISTEC, Japan): (a) CQOS schematic. (b) Flash ADC chip (2010) with integrated error-correction and interleaving circuits [17].

Superconductor Oversampling ADCs

The availability of fundamental flux quantization in superconductivity inspired several different oversampling delta and delta-sigma ADC designs. These are counting delta and sigma-delta type ADCs, a phase modulation-demodulation (PMD) delta ADC, and conventional delta and sigma-delta ADCs. While having quite different design approaches, most of them take advantage of the unique availability of *implicit feedback* and signal integration inherent to a SQUID loop, which is a result of fundamental conservation of flux in a superconducting loop. The SQUID loop automatically accumulates the total flux with opposite sign (sum of antfluxons) of all SFQ pulses (fluxons) emitted by the Josephson junction.

Counting V/F ADC: The first idea of superconductor oversampling ADC was suggested by McDonald of NBS/NIST at the 1976 Navy Summer Study on Superconductive Electronics. He proposed to use the ac Josephson effect to perform direct voltage-to-frequency (V/F) conversion. A single Josephson junction (Fig. 5a) can act as a voltage-controlled oscillator (VCO) and produce an SFQ pulse train at a rate proportional to the applied analog voltage as $f = 2eV/h = V/\Phi_0$. The generated SFQ pulses representing threshold crossings are to be counted over a time interval. This critical ability to count low-power SFQ pulses was provided in 1978 when J. Hurrell and A. Silver invented a binary counter based on a two-junction SQUID with overdamped Josephson junctions [18], [19]. The speed and simplicity of the counter circuit was a profound manifestation of the potential of superconductor circuits utilizing SFQ switching. Amazing switching speed of 100 GHz was experimentally demonstrated by C. Hamilton and F. Lloyd of NBS/NIST in 1982 [20].

This basic design was further developed and improved to increase its performance. In order to increase *resolution* of quantization process, a multi-junction VCO was proposed at TRW. It is based on interleaving of several single-junction VCOs while maintaining a fixed phase shift of one junction to another [21]. In order to increase the *sensitivity* of the V/F ADC, one can use a SQUID with a sensitive input transformer biased into the voltage state as a pulse generator as it was proposed at HYPRES [22]. Overall, the V/F counting A/D conversion is equivalent to a low-pass first-order *sigma-delta modulation* with implicit feedback [2].

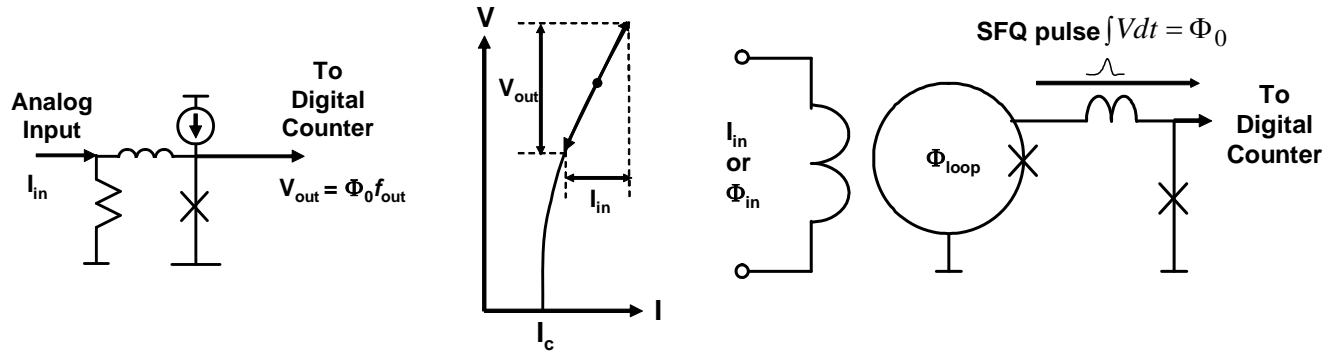


Fig. 5. Basic oversampling Counting ADC modulators. (a) Voltage-to-frequency (V/F) sigma-delta ADC modulator and its operating region. (b) Flux quantizing unidirectional delta (Tracking) ADC modulator.

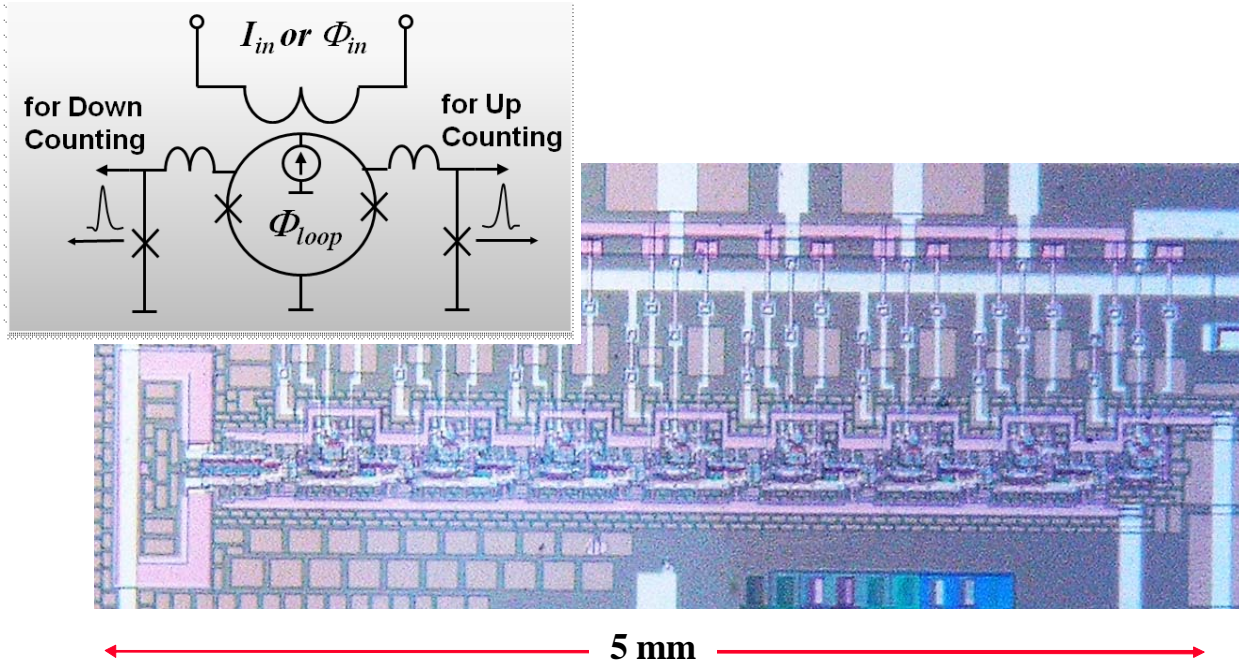


Fig. 6. First RSFQ-based Tracking ADC with a bi-directional (Up/Down) counter (1990). It was fabricated with a 5- μm all-Nb process with 500 A/cm². Inset: Basic bi-directional ADC modulator schematic.

Counting Flux Quantizing (Tracking) ADCs: The fundamental linearity of flux quantization in a superconducting loop is used for constructing another counting ADC design - a flux quantizing or tracking ADC which was first described by G. Lee of TRW in 1989 [23], [1]. In this design, the input signal current is coupled into a SQUID loop, which generates one SFQ pulse for each Φ_0 change in flux. In contrast to the V/F ADCs, the SFQ pulses are generated in response to increments or decrements of the signal, i.e., only changes of signal are registered. Similarly to the V/F ADC, these SFQ pulses can be counted by using binary counters to reconstruct the signal. Each time the input increases the flux in the loop (Φ_{loop}) by Φ_0 , the junction switches, creating a fluxon-antifluxon pair, one of which propagates as an SFQ pulse and the other decreases Φ_{loop} by Φ_0 (Fig. 5b). This automatic subtraction of the output signal from the input makes it equivalent to low-pass first-order *delta modulation*, where the output is proportional to the signal derivative $d\Phi/dt$. Since RF signal is sensed by a SQUID transformer, this ADC has an extremely high sensitivity similar to that of a SQUID.

This concept can be expanded to accommodate both polarities of input signal derivative. Fig. 6a shows a scheme with a two-junction quantizer, biased such that one of them switches when the flux in the loop changes by $+\Phi_0$ and the other when it changes by $-\Phi_0$, followed by bi-directional (up and down) counting implemented either using two counters or a single bi-directional counter [1]. In 1990, the joint Moscow State University (MSU) and IREE, USSR group implemented the first RSFQ-based

tracking ADC featuring bi-direction counter with non-destructive readout allowing uninterrupted signal tracking (Fig. 6b) [24].

Phase Modulation-Demodulation (PMD) ADC: One of the problems associated with the flux-quantizing (tracking) delta ADCs is the hysteresis of the SQUID quantizer in response to changing polarity of the signal derivative. In order to solve this, a dc voltage-biased single-junction SQUID quantizer (Fig. 7a) was introduced by S. Rylov, et al. of HYPRES in 1994 [25]. The voltage source (or phase generator) continuously pumps flux into a quantizer at a constant rate, which then leaves the quantizer via the only junction with the timing modulated by the derivative of the analog signal (Fig. 9a). The modulated SFQ pulse train is passed for SFQ phase (time) demodulation to a synchronizer - a clocked sampling circuit generates a '1' or a '0' indicating whether or not an SFQ pulse arrived during that clock interval. Higher SFQ phase resolution can be achieved by either higher clock or by adding more channels of the synchronizer. Typical sampling clock of this PMD ADC is in tens of GHz limited by the speed of subsequent digital signal processing circuits.

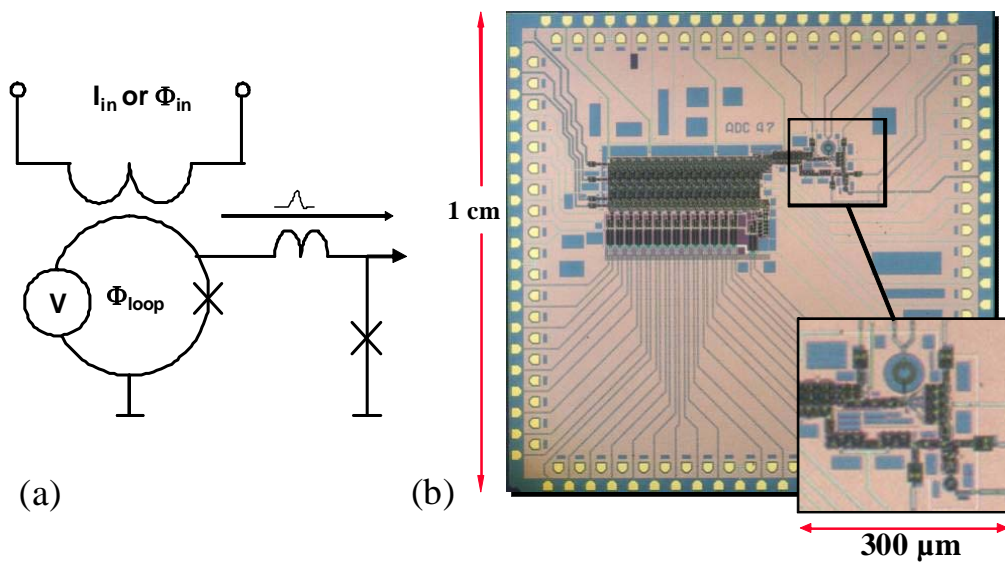


Fig. 7. Phase modulation demodulation (PMD) delta ADC invented in 1994. (a) Flux quantizer for PMD ADC modulator. (b) Second-generation PMD ADC chip consisting of a low-pass PMD delta modulator (in the inset) and a 15-bit decimation digital filter operating at 19.6 GS/s. This chip contains ~6,000 Josephson junctions fabricated at 1 kA/cm² process in 2000.

Similarly to the flash ADC digitizers, the oversampling ADC produces digital output data at tens of Gbit/s which exceeds today's data link per line capabilities and speed of semiconductor electronics. There two possible approaches to this interface problem: *on-chip digital filtering* and *demultiplexing*.

A digital decimation filter reduces the sampling rate, narrows output bandwidth, and generates additional bits. For oversampling superconductor ADCs, sinc-type digital filters were implemented using fast RSFQ logic capable of operating at the same speed as the sampling speed of the ADC. One of the key factors in successful development of the PMD ADCs was the adoption of a new design of the digital filter with programmable bandwidth developed by V. Semenov et al. in 1997 [26] and then perfected by T. Filippov et al. of SUNY Stony Brook [27]. By 2001, O. Mukhanov et al. of HYPRES and SUNY team [28] demonstrated a PMD ADC (Fig. 7b) with over 11 effective bits or 68 dB signal-to-noise ratio (SNR) for 145 MS/s output and maximum operation speed up to 19 GS/s. This was the world's fastest operation of the most complex (6,000 Josephson junctions) superconductor digital or mixed-signal circuit of that time.

A large variety of PMDs ADCs were developed including ADCs with serialized digital output, multi-rate ADC with doubled modulator sampling rate for communications and signal intelligence

applications. The ADC fabrication using 4.5 kA/cm^2 allowed sampling rate up to 34 GS/s. In 2006, I. Vernik et al. of HYPRES [29] demonstrated 13.5 effective bits for 10 MHz signal with a PMD ADC chip cryopackaged onto Sumitomo G-M cryocooler. By 2008, A. Inamdar et al. of HYPRES [30] achieved 14.5 effective bits (SNR=89.2 dB) at 29 GS/s sampling clock, while the multi-rate PMD ADCs operated up to 46 GS/s. In order to increase dynamic range of the PMD ADC, a quarter-rate PMD quantizer (QRQ) was introduced by A. Inamdar and S. Rylov et al. in 2006 [31] to increase the maximum ADC slew rate and to add two more bits of resolutions.

Higher-Order Delta ADC: Improvement of ADC performance is expected with higher order ADC modulators. V. Semenov's group at SUNY developed a low-pass delta ADC modulator based on a synchronous quantizer with two feedback loops and two integrators: an implicit loop due the conservation of magnetic flux in the superconducting loop of the quantizer and an explicit loop formed with the Josephson amplification circuit and a low-pass filter. A complete ADC chip with decimation digital filter was demonstrated its operation at up to 10.5 GHz clock in 1998 [32]. Although the modulator has two loops, its performance was still similar to a first-order modulator. In order to obtain the second-order characteristics, it is necessary to increase the explicit feedback gain. Achieving higher gain is difficult in superconductor technology, since it requires the construction of SFQ amplifiers (drivers).

Sigma-Delta ADC: In 1992, J. Przybysz et al. of Westinghouse invented a low-pass sigma-delta ADC modulator based on a synchronous quantizer with an analog L-R integrator (Fig. 8a) [33]. It has an implicit feedback due to the magnetic flux conservation and demonstrates the sigma-delta "noise shaping", i.e. suppressed noise at low frequencies. By 2006, the first order sigma-delta ADC has reached 77 dB SNR for a 10 MHz signal at 16 GS/s clock as it was demonstrated by A. Yoshida et al. of SRL ISTEK and the Hitachi group [34]. Demultiplexing was used in order to bridge the disparity in data rates between superconductor ADC modulator and semiconductor digital signal processing.

Due to the quadratically rising noise, a simple first-order decimation filter is insufficient to filter out the high-frequency noise. A second order modulator can improve SNR from 9 to 15 dB/octave of oversampling. However as for the delta ADC described above, the lack of broad-band amplification in superconductor technology makes construction of a second order sigma-delta ADC difficult. In 1994, J. Przybysz et al. proposed a two-loop modulator design employing an additional explicit feedback loop with the required substantial gain M (Fig. 8b) [35].

There have been several attempts in the US and Japan to realize this challenging amplification task, which has to deliver enough gain ($M \sim 64$) within a very short time, below the high-speed clock period. In 2003, S. Hirano et al. of SRL ISTEK, Japan demonstrated an amplifier based on a magnetically coupled Josephson transmission line (JTL) tree and serially connected SQUIDS demonstrated close to 12 dB/octave power spectrum characteristics although at a relatively low 1.2 GHz clock rate [36].

In 2004, realizing the difficulty of building a second-order sigma-delta ADC, A. Sekiya et al. of Nagoya University [37] found a way to increase first-order sigma-delta ADC SNR and sensitivity by using a multi-bit modulator following the PMD approach. The 4000-junction ADC chip consisting of a modulator and decimation filter was demonstrated using NEC standard Nb process with 2.5 kA/cm^2 .

Finally in 2008, Q. Herr et al. of Northrop Grumman [38] developed an SFQ amplifier with the required gain. A second-order sigma-delta ADC circuit featuring a high gain ($50\Phi_0$) quantum-accurate feedback amplifier (Fig. 8c) was built using HYPRES' commercial 4.5 kA/cm^2 Nb process. It achieved 81 dB SNR or 13.1 effective bits over a 10 MHz band at a 5 Gs/s sampling clock. Since the ADC chip did not have an on-chip digital filter, the sampling speed was limited by the output interface. The measured performance was in agreement with the linearized model which showed that the amplifier delay does not have to be shorter than the sampling clock period.

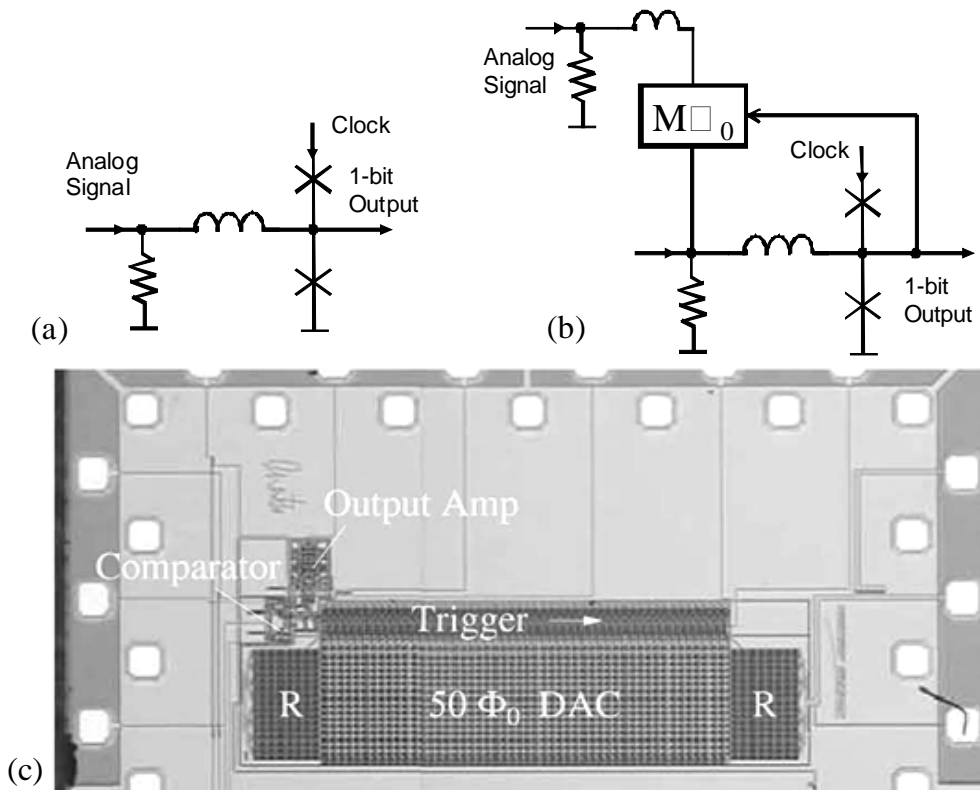


Fig. 8. Superconductor low-pass sigma-delta modulator. (a) 1993 first-order modulator with implicit feedback and input L-R integrator. (b) 1994 second-order modulator showing the critical feedback $M\Phi_0$ amplifier. (c) Northrop Grumman 2-order sigma-delta ADC with a $50\Phi_0$ feedback amplifier demonstrated in 2008.

Band-pass Sigma-Delta ADC: Superconductor technology is particularly suitable for implementing band-pass ADC designs exhibiting a peak performance around a particular frequency. Superconductivity features two major advantages: low-loss materials allowing very high Q resonators and high clock rates allowing direct sampling of multi-GHz RF signals. J. Przybysz and D. Miller of Westinghouse invented a first-order band-pass sigma-delta ADC modulator by replacing the front-end LR integrator with an LC resonator [39]. It suppresses the quantization noise around the resonant frequency f_{LC} , rather than at dc . The expected first-order noise shaping of sigma-delta modulator with lumped-element resonator was demonstrated by T. Hashimoto et al. of SRL ISTEK in 2001 [40]. In 2002, J. Bulzacchelli et al. of IBM [41] demonstrated a band-pass ADC with distributed microstrip-based resonators exhibiting the desired noise suppression around 2.2 GHz up to a sampling rate of 45 GHz. The demonstrated performance (SNR of 49 dB and dynamic range of 57 dB over ~ 20 MHz bandwidth at 2.2 GHz) exceeded that of semiconductor band-pass modulators at that time. Due to the lack of on-chip digital filters, the digitized data was stored using on-chip buffers for subsequent slow readout.

D. Kirichenko of HYPRES developed a family of continuous-time sigma-delta band-pass ADC modulators employing an implicit feedback and lumped-element resonators. Band-pass ADCs centered around various RF frequencies: 1 GHz, 4 GHz, 5GHz, 7.5 GHz, and 20 GHz were demonstrated [42]. Similarly to the low-pass ADC, a first order sigma-delta ADC cannot provide sufficient performance desired for directly digitizing receiver architectures. In 2007, D. Kirichenko developed a second-order delta-sigma ADC modulator with two lumped LC resonators (Fig. 9a) by introducing an explicit feedback loop using JTLs as active delay elements in addition to a D flip-flop to control the phase of the feedback signal [43].

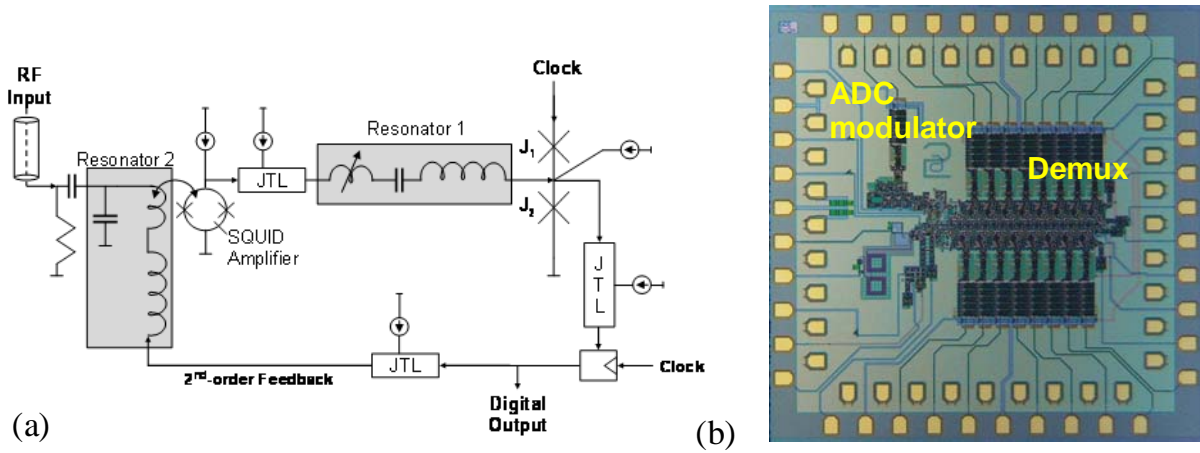


Fig. 9. A 2007 HYPRES second-order band-pass sigma-delta ADC. (a) Schematics of ADC modulators with implicit and explicit feedback loops. (b) X-band ADC chip consisting of second-order band-pass ADC modulator centered for 7.4 GHz and digital signal processor.

Typically, the clock frequency for a band-pass sigma-delta ADC is chosen to be $f_{clk} = 4f_0$, where f_0 is the center of the band of interest, e.g., 30 GHz for X-band. One can also use a lower clock frequency with some performance penalty. In this scheme, called RF undersampling, one can take advantage of the sampling process that replicates the input analog frequency band, centered at f_0 , translated by multiples of the sampling frequency (f_{clk}). The world's first Ka-band ADC with a 20.362 GHz center frequency was tested in the RF undersampling mode using a 27.136 GHz clock [43].

In 2008, D. Kirichenko invented ADC modulator with *two* implicit feedback paths exhibiting a quasi-instantaneous feedback implemented by connecting two resonators directly to the comparator. The RF input was split and applied through inductive coupling to each resonator. In addition, a SQUID amplifier stage was used to connect two LC resonators in series to get the desired loop filter transfer function. Such a band-pass ADC equipped with a 1:16 deserializer was demonstrated with a 31.6 dB SNR in 660-915 MHz band at 10.24 GS/s clock [44].

Multi-Modulator ADC: Challenges in achieving higher performance encourage adaptation of ADC architecture approaches known in conventional semiconductor ADC technology: time-interleaving, sub-ranging, cascading, and others.

Time-interleaving allows the increase of effective sample rate by using several parallel comparators sampled by the same clock. The actual performance gain in the interleaved oversampling ADC depends on various factors, including feedback-loop delay in comparison to the effective clock period. In 1999, V. Semenov of SUNY [45] invented a time-interleaved delta modulator consisting of two delta modulators shifted by half a clock period, this requires interleaving both comparator and feedback functions. Since interleaving cannot be achieved with the implicit feedback of SQUID quantizers, separate explicit feedback loops are implemented using stacked SQUIDs.

Sub-ranging is capable of significant increase of dynamic range by using several modulators to digitize different ranges of signal amplitude. This approach can be applicable for two-delta, two-sigma-delta, or combined delta and sigma-delta modulator combinations. A. Inamdar of HYPRES [31] showed that the two-delta sub-ranging ADC based on the proven PMD ADC modulators is capable of a significant SNR improvement (23 dB) with a quite conventional 26 GS/s sampling clock.

ADC Applications: Digital Receivers based on Oversampling ADCs: Since 1990s, rapid technological progress in wireless commercial and defense communications and related radar and electronic-warfare applications is driving the demand for much higher ADC performance. These applications can greatly benefit from the ability to directly digitize wideband RF signals. Conventional narrow-band technology implements a separate analog receiver with one or more downconversion steps for each sub-band. A wideband software-defined radio (SDR) receiver needs mixed-signal and digital components capable of delivering extreme speed, linearity, dynamic range, noise, and

sensitivity. As it was realized around 2000 in USA, Japan, and Europe, the unique features of superconductor technology and ADC circuits, in particular, can make a true SDR possible [46]-[48].

In a *Digital-RF* architecture [49], data conversion and digital processing take place at RF rather than at baseband - the analog filter and up/down-conversion stages from/to lower IF or baseband are eliminated (Fig. 10). A wideband RF signal is applied directly to an ADC modulator producing an oversampled low-bit-width digital code at a very high data rate (tens of Gbps). This high-rate data stream is processed before down-conversion using a relatively low-complexity but very high-throughput processor, an *RF DSP*, to implement various functions such as digital signal-combining from multiple channels, true-time delay for digital beamforming, adaptive active cancellation of transmit channels, correlation-based digital filtering, etc. Finally, this high-rate data is down-converted to baseband using digital mixers and decimation filters for further processing and decoding. Back-end processing is implemented using conventional semiconductor parts and placed at ambient temperature.

The first practical implementation of the Digital-RF architecture – superconducting Digital-RF channelizing receivers extract different frequency bands-of-interest within the broad digitized spectrum. The single-bit oversampled data, from either a low-pass delta or band-pass delta-sigma modulator, are applied to one or more channelizers, each comprising digital In-phase (I) and Quadrature (Q) mixers and a pair I and Q digital decimation digital filters. Digital channelization performed in two steps, the first at full ADC sampling clock frequency with RSFQ digital circuits and the second at reduced (decimated) clock frequency with commercial field programmable gate array (FPGA) chips at room temperature.

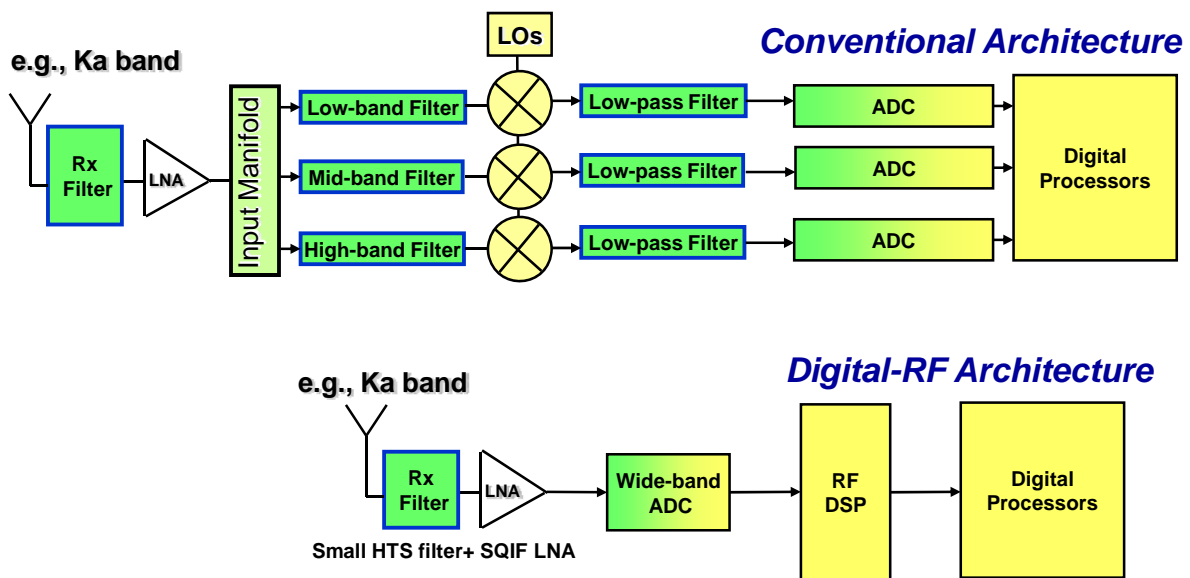


Fig. 10. Comparison of conventional (top) and Digital-RF receiver (bottom) architectures. In the digital-RF architecture, data conversion is carried out directly at RF frequencies using a wideband oversampling ADC modulator. The digitized RF data stream is then processed at very high data rate in an *RF DSP* before being digitally down-converted and filtered to baseband for further processing.

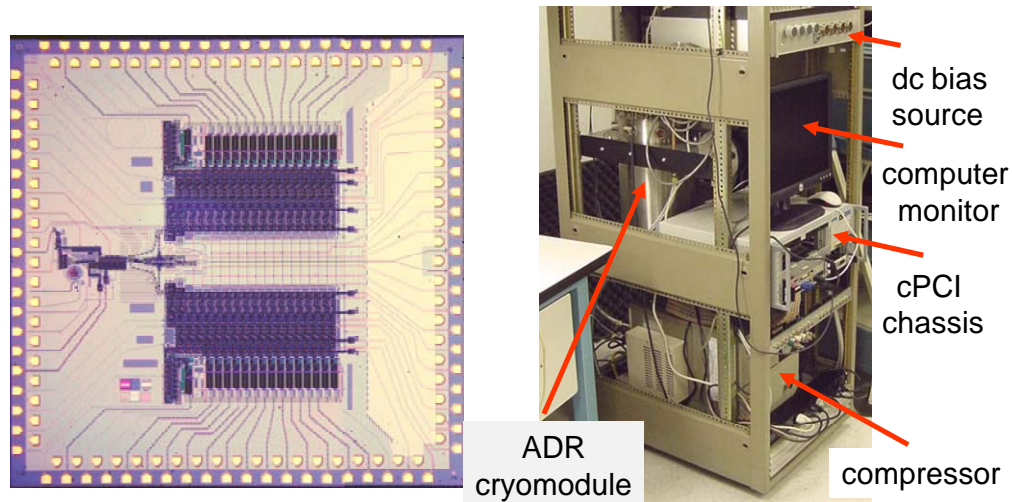


Fig. 11. World's first Digital-RF System: – 2005 HYPRES channelizing receiver: (a) Microphotograph of a single-channel All-Digital Receiver (ADR) chip based on the first-order low-pass delta ADC, digital In-phase and Quadrature (I&Q) mixer, and decimation digital filters. This $1 \times 1 \text{ cm}^2$ chip consists of $\sim 11,000$ JJs and dissipates $\sim 3.5 \text{ mW}$. (b) Photo of the cryopackaged ADR test setup (ADR-0) using commercial Sumitomo 2-stage GM cryocooler mounted into the lower part of standard 19-inch rack [49].

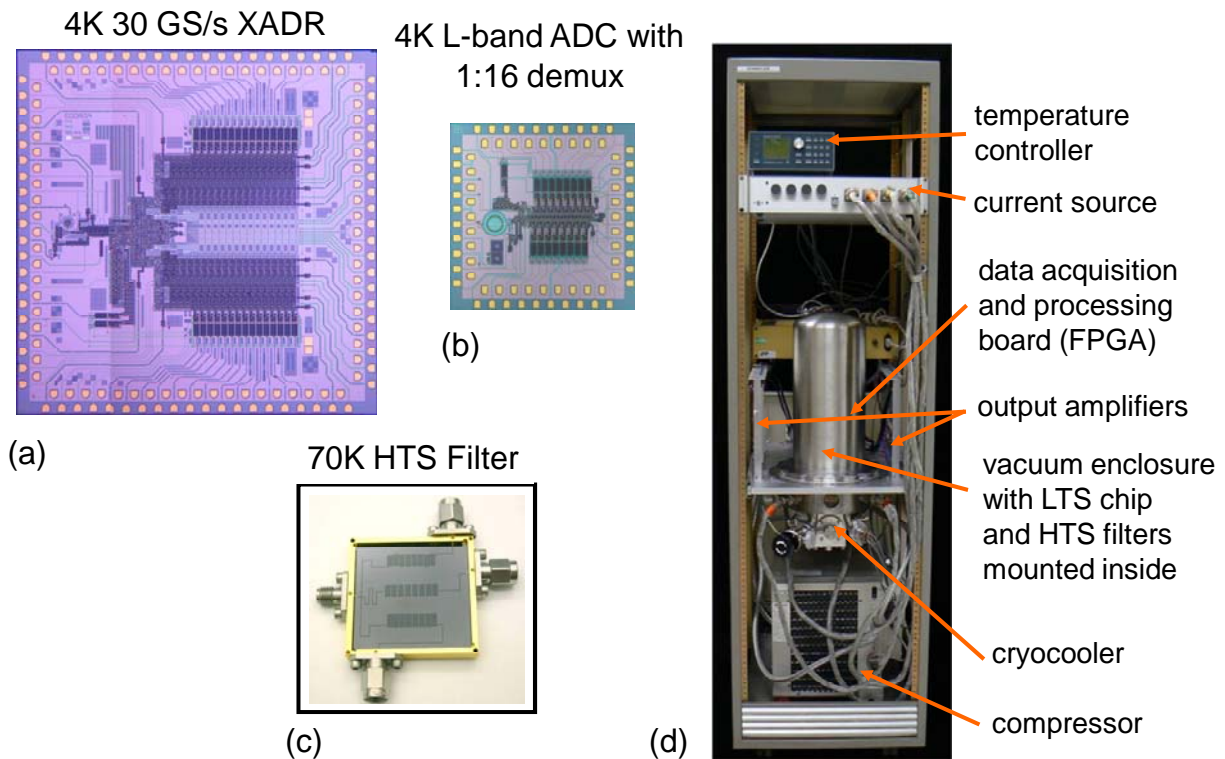


Fig. 12. Digital-RF Receiver and its key components: (a) World's first (2006) X-band single-chip Digital-RF Receiver (XADR) directly digitizes 7.5 GHz RF signal at 30 Gs/s . This $11,000$ -junction chip consists of a band-pass second-order continuous-time delta-sigma ADC modulator, digital I&Q mixer, and two digital filters; (b) L-band ADC integrated with a $1:16$ RSFQ demux (2008); (c) HTS filter developed by University of Waterloo, Canada (2008); (d) HYPRES (2008) modular ADR system built using hybrid temperature hybrid technology (ht^2) approach.

In 2004, the first Digital-RF channelizing receiver chip was produced at HYPRES (Fig. 11a). It consisted of a 20 GS/s low-pass phase PMD ADC modulator. This ~11,000 junction chip was fabricated using a 1.0 kA/cm² process and tested up to 20 GHz clock rate. In 2005, the ADR chip was integrated onto a commercial Sumitomo SRDK 101D cryocooler capable of cooling 125 mW at 4.2 K. It is mounted into a standard 19-inch rack, which also houses a cryocooler compressor, interface and control hardware (Fig. 11b). This word's first Digital-RF receiver system was done under support and guiding from D. Van Vechten of the U.S. Office Naval Research.

Satellite communications with high carrier frequencies and wide bandwidths (e.g., X-band: 500 MHz BW around 7.5 GHz; Ka-band: 1 GHz BW around 20.5 GHz) can benefit from wideband Digital-RF channelizing receivers by eliminating bulky analog channelizing and downconversion stages. In 2006, D. Gupta et al. of HYPRES [42], [43] assembled and delivered ADR-1, an X-band digital receiver system, to the Joint SATCOM Engineering Center (JSEC) in Ft. Monmouth, NJ to receive wideband X-band signals from the XTAR, DSCS, and WGS satellites. The receiver was successfully integrated with a digital I&Q MODEM, demonstrating demodulation of satellite signals including a video data transmission. In 2007, the ADR-1 system was upgraded with installing faster a 30-GHz chip fabricated 4.5 kA/cm² process (Fig. 12a).

In subsequent years, more ADR systems based on low-pass PMD delta ADCs and band-pass sigma-delta ADCs were assembled and delivered. In 2008, new-generation ADR systems featuring modular cryopackaging design were delivered. These ADRs demonstrated the *hybrid temperature hybrid technology* (ht²) system integration concept, where different components of the system are operated at different temperatures to optimize the overall performance. For example, the system included a high-temperature superconductor (HTS) filter developed in University of Waterloo (Fig. 12c) which was placed at 70 K on the first stage of the cryocooler and connected to the ADR chip located at the second (4K) stage. In January 2009, D. Gupta et al. of HYPRES, ViaSat, and Navy team [50] demonstrated the world's first multi-net Link-16 data link in which analog outputs from two Link-16 terminals, operating with independent hopping patterns, were combined and applied to the superconductor chip with L-band sigma-delta ADC chip integrated with RSFQ 1:16 demux (Fig. 12b).

By 2010, HYPRES ADR systems went through three generations. Third-generation ADR systems expanded to house two chip modules with 80 high-speed digital I/Os, up to four 17-channel interface amplifier assemblies and two current sources. The design is modular and allows for independent service of each chip module and quick field replacement when necessary. The system re-configurability enabled by the modular design allowed ADR-5 to be configured and used for satellite communication tasks. D. Gupta et al. [50] demonstrated operation with the XTAR satellite without utilizing a low-noise amplifier usually required for this application. This was another step towards fully digital receivers. ADR-5 system worked up to 32 GHz clock frequency with a variety of phase and amplitude modulated waveforms at 30 Msymbol/s.

The digital channelizing receiver approach can be extended to include multiple ADC modulators and multiple channelizer units on a multi-chip module. It is also possible to integrate a multi-band but single-channel digital-RF receiver on a single 10 x 10 mm² chip by integration of multiple ADC modulators to a single channelizer. A chip integrating four ADC modulators (centered at 850 MHz, 4 GHz, 7.5 GHz and 12 GHz), 1x4 digital switch matrix and 1:16 demultiplexer (Fig. 20) was demonstrated in 2010 by S. Sarwana et al. of HYPRES [51].

ADC Applications: Sensor Readout

The inherent low noise, low power, high sensitivity, and radiation hardness of superconductor ADCs can be applied for many sensor technologies, especially for cooled detector arrays. Both flash-type and oversampling-type ADCs can be used for this application.

In 2001, A. Sun et al. of TRW [52] demonstrated a NbN 10 K V/F type ADC for cryocooled infrared (IR) focal plane detector arrays. A Nb 4 K 16-bit PMD delta ADC with a serial optical-fiber output to minimize heat load was demonstrated by D. Gupta et al. [53] in 1998 for an IR-array readout.

A Nb V/F type ADC with a SQUID-based VCO was used for measuring the integrated charge of a current pulse for superconductor tunnel junction (STJ) X-ray detector readout. Furthermore, this digital

counter can also be used to count the number of SFQ clock pulses between successive time events to produce a TDC on the same chip. Such a dual-function signal and time digitizer was recently demonstrated by joint US-Japanese team with 1 μ A full-scale current and 30 ps time resolution [54].

The exceptionally low power of RSFQ technology allows integration of an ADC or TDC in a single cryopackage with the cooled detectors. The integration of the cooled semiconductor detector, Visible Light Photon Counter (VLPC), was demonstrated by O Mukhanov et al. [55] in 1998 with a single-hit TDC chip equipped with a sensitive SQUID-based V/F ADC.

The extreme radiation hardness of superconductor electronics was a motivation for the readout of a high-energy particle microstrip detector. In this design, a simple delta ADC based on a very sensitive flux-controlled comparator was demonstrated for CERN high-energy physics experiments by joint US-Italian team [56].

Superconductor Materials for ADC Implementation: LTS vs HTS

Superconductor ADCs are medium-scale integrated circuits requiring substantial number of Josephson junctions for complete systems. Even if an ADC modulator can be implemented with a rather few junctions, the subsequent demultiplexer, drivers or digital filter can easily require hundreds or thousands of junctions. This requires well controlled integrated circuit fabrication, with reproducible junction properties. Most of the complete ADC circuits have been demonstrated to date using low-temperature superconductor (LTS) niobium Josephson junctions, operating at about 4 K.

Slightly higher temperature superconductors, NbN with T_c up to about 17 K, were used by TRW team to implement counting ADCs with 16-bit resolution. It was demonstrated to operate at 10 K for infrared sensor applications [52].

The possibility of drastic reduction of size, weight and power (SWaP) of cryocooler was the main motivation to implement high-temperature superconductor (HTS) ADCs. There have been major efforts to develop a reproducible technology for Josephson junctions based on YBa₂Cu₃O₇ (YBCO), although the high temperatures required for epitaxial deposition of these materials makes a true multilayer process difficult to achieve.

Several HTS ADC projects were active in Japan (Hitachi, SRL ISTEK), Europe (Twente Univ., Chalmers Univ., Karlsruhe Univ.), and USA (Conductus, Northrop Grumman) for a number of years. Some key components of ADCs, including a simple first-order sigma-delta oversampling ADC modulator, QOS comparator for flash ADC have been demonstrated [57]-[61]. In 1997, G. Gerritsma et al. of University of Twente [62] reported on the effort to build a 4-bit flash ADC based on QOS comparators using ramp junction technology. Functionality of QOS comparators was demonstrated at low speed. In 2004, H. Sugiyama et al. of SRL ISTEK [63] demonstrated high-speed operation of a QOS comparator based on high- T_c multilayer technology. A circuit containing 10 interface-engineered ramp-edge Josephson junctions was fabricated on a La-substituted YBa₂Cu₃O_y ground plane. The output voltage as a function of the input current for the QOS indicated correct operation as a periodic comparator at clock frequency of 94 and 77 GHz at 35 and 40 K, respectively.

At this moment, it seems unlikely to have the HTS technology reach the required complexity in the near future. On the other hand, a progress in compact 4 K cryocoolers can make Nb-based ADCs useful for a wider range of applications.

CONCLUSIONS

The unique features of superconductivity, featuring the high speed of Josephson junctions and the quantum precision of magnetic flux quantization, found their applications in wide variety of superconductor ADCs. Both Nyquist-sampling flash ADCs and oversampling ADCs of different designs were demonstrated (Fig. 21). Applications in wireless communications, fast measurement, and sensor readout led to a construction of system prototypes and demonstration units based on using 4K cryocoolers. The QOS – most influential. PMD is most produced.

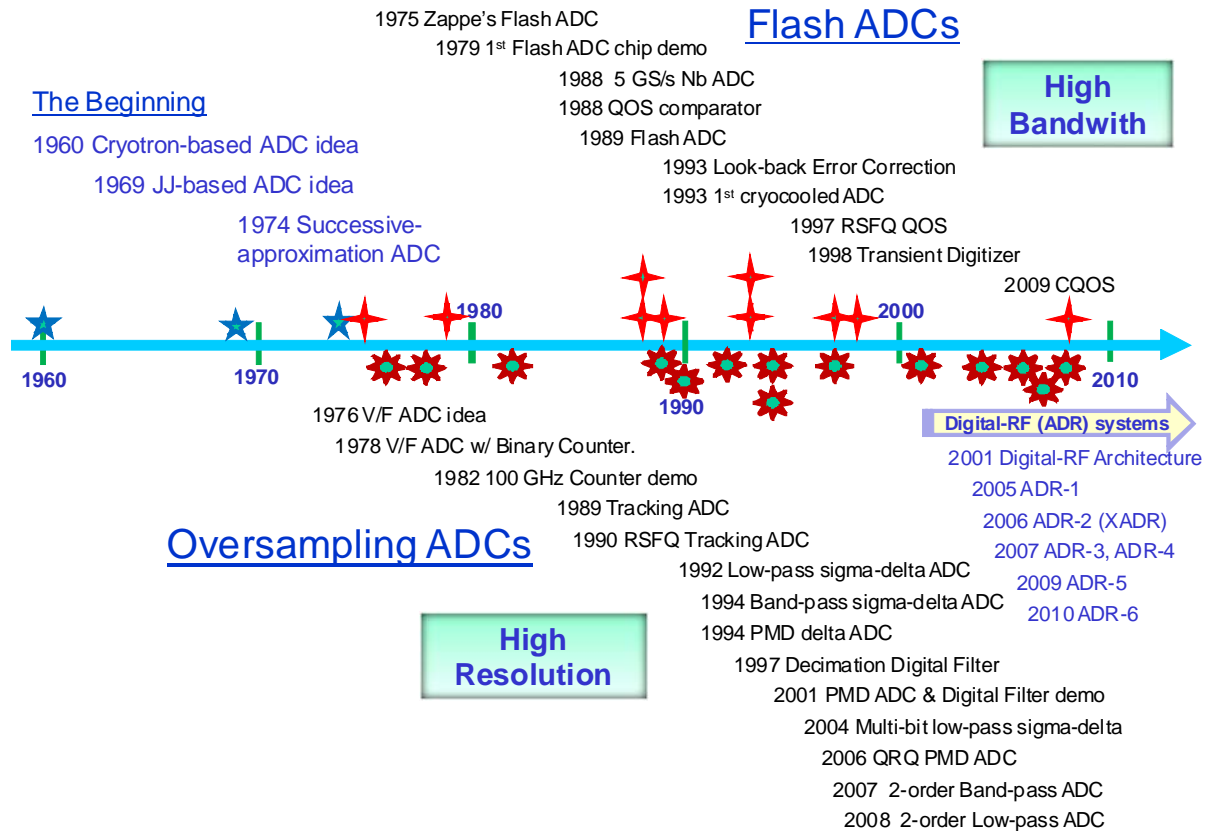


Fig. 13. Superconductor ADC development timeline.

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