A 25-Bit Reference Resistive Voltage Divider

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Abstract—**An automated 25-bit reference resistive voltage divider is described. It features microcomputer-controlled self-calibration and autobalancing voltage ratio measurement to eight significant digits, with an uncertainity (2σ) of three parts in 10^8 (of the 10-V input) or the equivalent of one least significant bit (LSB). To achieve this accuracy, sources of error have been critically examined, carefully controlled, and accounted for.**

I. Introduction

At the National Research Council of Canada, self-checking 13- and 22-bit voltage dividers have been built and evaluated [1], [2]. They are based on a switching technique for resistive voltages dividers by Cutkosky [3]. The uncertainty in the voltage ratios they provide is typically a few parts in 10^7 of the 10-V input.

In the 25-bit reference voltage divider and calibration system to be described, higher accuracy and precision have been achieved by dealing concretely with the small but finite effects of the divider's switch contact, wiring, leakage, and output resistances on the calibration and on the ratio realized. As a result, it can measure arbitrary voltage ratios (between 0 and 1) to eight significant digits with an uncertainty (2σ) of three parts in 10^8 of the input, or the equivalent of one least significant bit (LSB). The experimental verification of its accuracy will also be described.

II. System Description

A block diagram of the automated system is given in Fig. 1. The 25-bit voltage divider is entirely passive. It consists of an improved 13-bit self-checking (Cutkosky) divider terminated by a 12-bit potentiometer. Thus the higher-order Cutkosky divider provides the composite divider with the requisite accuracy, while the potentiometer extends its resolution without increasing its output resistance [4]. As before, switching is effected by latching relays, simply controlled and monitored by a microprocessor which also interfaces to the IEEE-488 bus. The two main system operations, autocalibration and autobalancing ratio measurement, are designed to be software driven by the desktop computer. This makes an extremely versatile system which may be tailored for the experimental investigation of systematic errors as well as for other customized applications.

The 13-bit divider is made up of 40-kΩ (R_{nom}) wire-wound resistors, initially matched to $\pm 20 \times 10^{-6}$; the 12-bit potentiometer is made from 0.01-percent metal-film resistors contained in one package. In practice, however, only the first 10 or 11 binary stages of this divider were found to require periodic recalibrations or corrections. The calibration routine takes about 90 s to complete, and is less sensitive to external influences than the ratio measuring routine.

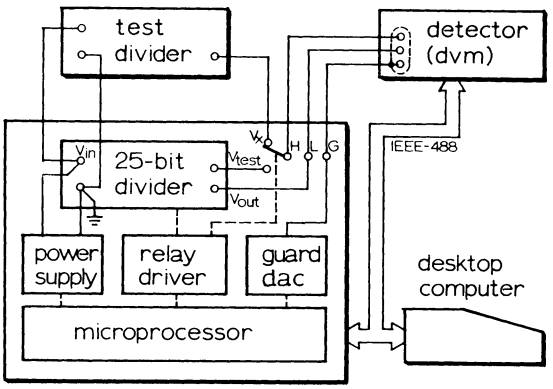

Fig. 1. Block diagram of the automated reference voltage divider system using a DVM as detector, shown calibrating a test divider.

The system detector is a digital voltmeter (DVM) of 100-nV resolution. Throughout this paper, a ±10-V input is assumed, and each measurement calls for eight DVM readings, four taken in each reversed dc polarity. The DVM helps to speed up the autobalancing process in ratio measurements, but its nonlinearity hardly matters because the final imbalance never exceeds ±25 μV. Unless otherwise stated, all uncertainties will be 1σ estimates.

III. Error Considerations

The following analyses deal mainly with the errors of the Cutkosky divider on which the accuracy of the system depends.

A. Autocalibration

Let $G_t = V_{out}/V_{in}$ be the voltage transfer ratio of the N-bit divider ($N = 13$ in this case) and let $T_j = 0$ or 1 ($j = 1, 2, \cdots, N+1$) denote the individual setting of the toggle switches of the divider (Fig. 2).

Cutkosky [3] has shown that it is sufficient to make $2N$ individual measurements to completely calibrate an N-bit divider, neglecting switch and wiring resistances. Referring to the divider of Fig. 2, the self-checking or autocalibration process consists of following an established switching sequence and making N pairs of measurements

Manuscript received June 23, 1986.

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IEEE Log Number 8613424.

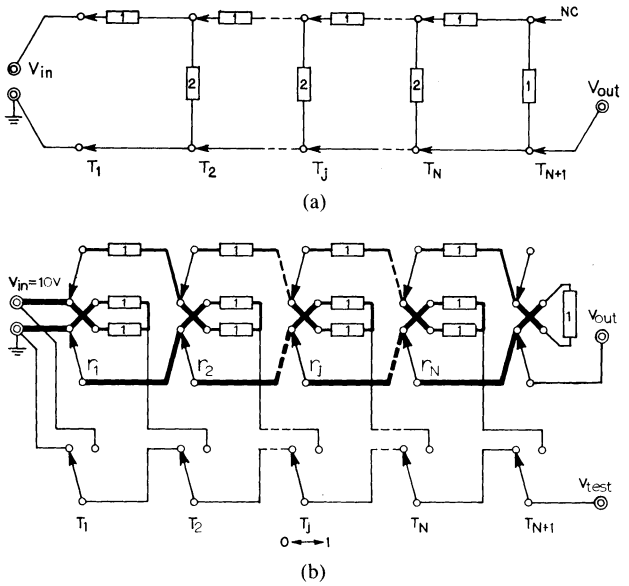

Fig. 2. (a) An N-bit Cutkosky voltage divider with cascaded DPDT switches T_j, each drawn as a pair of interchangeable contacts. With all switches at zero (as shown), all horizontal "dropping resistors" appear in the upper branch. Resistance values indicated are relative to R_{nom}. (b) Wiring diagram for the same divider. Heavy links identify the requisite low-resistance connections. Additional SPDT switches give access to internally generated V_{test} for self-checking purposes.

of the normalized quantity $d = (V_{out} - V_{test})/V_{in}$. For example, to calibrate the kth stage, one measures $d_{k,1}$ with T_{k+1} set to 1 and all other switches to 0, and then $d_{k,2}$ with T_k also set to 1. Hence, a set of N differences, $\Delta_j = d_{j,1} - d_{j,2}$, can be calculated, each Δ_j being a measure of the "resistance mismatch" in the jth stage.

From the above set of Δ_j's the ratio G_t may be computed in a number of ways [1], [3] for any given switch setting configuration of the divider. The following alternative approach is found to be useful in dealing with the introduction of switch and wiring resistances. Since derivations of the equations to follow are often lengthy but straightforward, only the reasoning behind them will be given.

To begin with, let the voltage developed across the "dropping resistor" in the jth stage, when divided by V_{in}, be the "weight" w_j of that stage, which carries a nominal value of $1/2^j$. To account for the small resistance mismatches ($\Delta_j << 1$) in a cascade of stages, these N weights can be computed as follows:

$$w_1 = (1 - \Delta_1)/2$$

$$w_2 = (w_1 + \Delta_1 - \Delta_2)/2 = (1 + \Delta_1 - 2\Delta_2)/2^2$$

and in general

$$w_j = (w_{j-1} + \Delta_{j-1} - \Delta_j)/2. \qquad (1)$$

Hence, G_t can be obtained as a summation of the form

$$G_t = \sum_{j=1}^{N} (b_j w_j) \qquad (2a)$$

$$\approx \sum_{j=1}^{N} (b_j/2^j) \qquad (2b)$$

where the binary coefficient b_j depends on whether the jth bit is ON ($b_j = 1$) or OFF ($b_j = 0$). In the circuit representation of Fig. 2(a), it is apparent that switching any dropping resistor into the lower branch of the circuit directly between V_{out} and ground effectively turns that bit ON, because its voltage drop contributes directly to V_{out}. By inspection, the "down/up" location of each dropping resistor in terms of b_j can be derived from the following logical equation:

$$b_j = T_j \oplus b_{j-1}, \qquad b_0 \equiv 0. \qquad (3)$$

Conversely, in trying to realize a transfer ratio of G_t, the approximation (2b) can be solved for b_j's and the required switch settings can be derived from the dual relationship of (3), viz.

$$T_j = b_j \oplus b_{j-1}, \qquad b_{N+1} \equiv 0. \qquad (4)$$

The assessment of the uncertainity in Δ_j forms an important part of this study. Each Δ_j is obtained from the difference of two successive measurements; it is influenced by the switches' thermal EMF and the detector input noise and drift. Any common-mode dependence of Δ_j would constitute a systematic error and should be eradicated. Numerous sets of autocalibrations were conducted to examine the effects of the common-mode and guard voltages, delay, and integration times for taking a DVM reading, etc. It was found that using a driven guard circuit (Fig. 1) and reversed dc measurements delivers the smallest uncertainty in autocalibration. The pace of the calibration operation has also been optimized by starting with the LSB and by tailoring the necessary time delays. Through numerous repeated autocalibrations with the chosen DVM, it has become quite clear that each measurement of any one Δ_j by the adopted routine is uncertain by $\pm 7 \times 10^{-9}$. How much this would contribute to the uncertainty in the resulting G_t could be calculated in each case from (1) and (2), but this is rarely done in practice. Instead, a worst-case uncertainty of $\pm 9 \times 10^{-9}$ may be assigned, which is equal to $\sqrt{N + 1}/3$ times the above value (cf. [3, section III]).

B. Switch and Wiring Resistances

The switches used in the driver must meet certain thermal EMF, insulation-, and contact-resistance requirements. Based on experience, pulse-operated latching relays are used. The armatures of these relays work with gold-plated contact pads that have been carefully laid out and interconnected (and reinforced with copper strips where necessary) on a printed circuit board. Contact-resistance measurements on isolated relays of this type gave 32 ± 1.2 mΩ as typical for one set of contacts, and $(32/n) \pm (1.2/\sqrt{n})$ mΩ for n paralleled contacts. To control uncertainity, multiple relay contacts are employed for the first five switches. Noting that the current is halved in each succeeding switch, one can estimate ratio corrections for the divider as in Table I. Wiring resistances (assumed fixed) will increase these estimates but the uncertainties should remain. This has been confirmed by

TABLE I
VOLTAGE RATIO CORRECTIONS (1σ ESTIMATES) FOR DPDT SWITCHES IN THE 13-BIT DIVIDER

SWITCH #	PARALLELED CONTACTS/POLE	CONTACT RESISTANCE (mΩ)	V RATIO CORRECTION (10^{-6})
1	15	2.1 ± 0.3	.025 ± .004
2	7	4.6 ± 0.4	.029 ± .003
3	7	4.6 ± 0.4	.015 ± .002
4	4	8.0 ± 0.6	.012 ± .001
5	4	8.0 ± 0.6	.006 ± .001
6	1	32 ± 1.2	.012 ± .002
7	1	32 ± 1.2	.006 ± .001
8	1	32 ± 1.2	.003 ± .001
9 - 14	1	32 ± 1.2	≤ .002 ± .000
Total			.112 ± .006*

* Root-sum-squares uncertainty of total correction.

measurements. The results of these effects in determining G_t will be examined next.

Using Fig. 2(b) as a model, one notes that switch and wiring resistances in series with the dropping resistor may be considered an integral part of the latter. On the other hand, those resistances in series with the "zero-resistance" connecting links should be accounted for. For the sake of brevity in the following analysis, they are expressed as resistive ratios r_j with respect to the R_{nom} of the divider. If e_j denotes the voltage across r_j, it follows that $e_j = V_{\text{in}} \cdot r_j/2^j$ and that the following summation

$$q = \sum_{j=1}^{N} (r_j/2^j) = \sum_{j=1}^{N} (e_j/V_{\text{in}}) \tag{5}$$

is simply the ratio of the sum of voltage drops across all r_j's to V_{in}.

Suppose that a set of Δ_j's is experimentally determined as before and that a set of w_j's is computed as in (1). The problem is how to formulate G_t to account for the presence of r_j's.

In contrast with the ideal-contact case, further analysis shows that each Δ_j now contains a contribution from twice the voltage drops across succeeding (lower-order) switches, and that the actual weight w_j' has a residual value of $r_j/2^j$, even when that bit is OFF ($b_j = 0$). The situation can best be summarized by the following two equations:

$$\begin{aligned} w_1' &= [r_1 + b_1(1 - \Delta_1)(1 - 2q)]/2 \\ w_2' &= [r_2 + b_2(1 + \Delta_1 - 2\Delta_2)(1 - 2q)]/2^2 \\ &\vdots \\ w_j' &= [r_j + b_j(1 + \Delta_1 + \cdots + \Delta_{j-1} - 2\Delta_j) \\ &\quad \cdot (1 - 2q)]/2^j \end{aligned} \tag{6}$$

and

$$G_t' = \sum_{j=1}^{N} w_j'. \tag{7}$$

Since the individual r_j in the actual circuit is difficult to ascertain, the individual w_j' cannot be determined and it appears that G_t' cannot be calculated precisely from (7). However, (7) can be rewritten as

$$G_t' = q + (1 - 2q) \sum_{j=1}^{N} (b_j w_j) = q + (1 - 2q)G_t \tag{8}$$

which is a very useful result indeed. First, one determines G_t exactly as before, in spite of contact and wiring resistances. Second, q may be obtained from one single *in-situ* measurement of $V_{\text{out}}/V_{\text{in}}$ with all switches set to 0. Third, G_t' is calculated from G_t in a manner analogous to a "renormalization" of the ratio with respect to remote input terminals. Therefore, the effect of (small) wiring resistances from the divider to the remote input terminals is transparent to the user if the input wiring detail shown in Fig. 2(b) is followed.

C. Loading

The output resistance R_{out} of the Cutkosky divider can be calculated precisely [4]. For the 13-bit divider at hand, it has a maximum value of $3.1 \times R_{\text{nom}}$ or nearly 0.125 MΩ, and it is most frequently distributed around the value of $2.5 \times R_{\text{nom}}$ or 0.1 MΩ. These being fairly large resistances, both internal leakage and external loading must be carefully controlled so that one can interrelate the voltage and resistance ratios of this divider with confidence.

Internal leakage or loading is minimized by adopting a sensible relay-board layout. The latching relays are driven through opto-triacs by a transformer-coupled 60-Hz supply, whose common is connected to the guard voltage. This is particularly effective in controlling the leakage from the lower order stages of the divider (where R_{out} is higher).

Inasmuch as this is a ground-referenced system, loading between V_{out} and ground must be controlled and accounted for. The addition of an isolation amplifier to this divider's output has not been pursued for fear of compromising its overall performance. A small number of commercial DVM's compatible with the use of a driven guard circuit were examined as a differential detector for the system. In general, the input HI-to-ground resistance (RHG) is much larger than the input LO-to-ground resistance (RLG). Therefore, it is prudent to present the input HI to the unknown voltage V_x (e.g., from the test divider in Fig. 1) whose precise source resistance is not always known. The chosen DVM has an RHG in excess of 8 TΩ. Its RLG amounts to <0.02 TΩ without a driven guard and increases to 0.20 TΩ when guarded at the mean input potential. Measurements showed that its RLG is moderately time-dependent after a dc reversal and that it could vary up to ±15 percent. The resulting maximum correction of $(-0.62 \pm 0.09) \times 10^{-6}$ would not be acceptable. To

TABLE II
UNCERTAINTY ASSIGNMENT FOR THE DIVIDER

Source	1σ Estimate
Autocalibration Correction	± .009 × 10^{-6}
Switch, wiring Correction	± .008
Detector Loading Correction	± .009
Potentiometer	± .005
Allowable Drift after Cal.	± .005
Simple Sum	± .036 × 10^{-6}
Root-sum-squares	± .017 × 10^{-6}

overcome this problem, the effective RLG must be increased.

To this end, the guard circuit was overdriven and the system was programmed to measure the correction, when R_{out} was loaded by RLG, as a function of both the guard overdrive and the elapsed time after a dc reversal. As a result of this study, a guard voltage equal to 112 percent of the mean input potential is adopted in order to limit the measurable maximum correction to $(-0.071 \pm 0.009) \times 10^{-6}$ (i.e., RLG = 1.7 TΩ) when readings are taken 6–8 s after a dc reversal. Measuring this correction can be included as a part of the calibration routine.

D. Overall Uncertainty

Table II sums up the various uncertainties from identified sources. The switch and wiring correction uncertainty has been adjusted by $\sqrt{2}$ to reflect the situation of two poles/switch. Since the sources are not correlated, summing these uncertainties by root sum squares (RSS) is justifiable. A 2σ estimate for the total RSS uncertainty amounts to $\pm 0.034 \times 10^{-6}$ or the equivalent of 1 LSB of this 25-bit divider.

IV. VERIFICATION

The elegantly simple method of obtaining self-checking resistive ratios by Thompson [5] was adopted for the purpose of verifying the divider accuracy. With only six nominally equal resistors, very accurate voltage ratios of $n/10$ ($n = 1, 2, \cdots, 9$) are provided by the geometric mean of the ratios realized from the dual-network configurations (Fig. 3).

The resistive ratio device constructed for the above purpose uses a stud-and-plug interconnection arrangement (Fig. 4), where heavy copper studs (hexagonal blocks) are mounted on a thick polytetrafluorethylene (PTFE) sheet. The seven numbered studs have six 40-kΩ wirewound resistors (matched to ±0.005 percent) soldered to alternate ends of their center posts, in sequence. Thus, the node between resistors can be thought to locate itself at the geometric center of the stud. The resistance between adjacent nodes was found to be 46 ± 6 μΩ when a copper plug was inserted into the rimmed hole between them. Therefore,

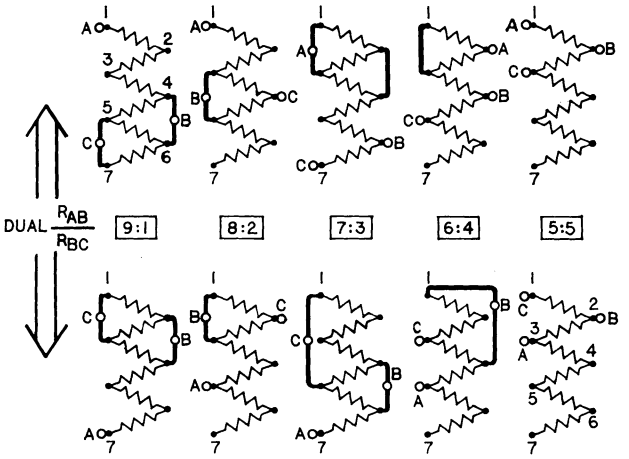

Fig. 3. Dual configurations of networks (after Thompson [5]) producing resistance ratios for each step of a single-decade divider. Network has six nominally equal resistors connected in series. Thick lines represent shorting links.

two 40-kΩ resistors could be connected in parallel with about 1×10^{-9} error. The lettered studs were used as terminals for accessing the resistance ratio produced.

Following Thompson's circuits (Fig. 3) the resistive ratio device was configured (by means of up to five plugs) for a ratio of $n/10$, immersed in a 23.00°C oil bath and measured by the fully corrected divider (in terms of a voltage ratio). The network was inverted end for end and the resulting complementary ratio $(1 - n/10)$ measured. Then the dual-network configuration for the same ratios was implemented and measured. Using $n = 1, 2, \cdots, 5$, five sets of measurements were made and the results have been tabulated as items (A) and (B) in Table III. One notes that the sum of the complementary ratios from inverted networks should add up to unity, a necessary condition for good accuracy. Geometric means (C) should be perfect ratios of $n/10$, except for the consideration of a small load coefficient of -0.025×10^{-6}/mW. Based on the changes in dissipation between configurations, small corrections (D) can be applied. Deviations of the corrected results (E) from perfect $n/10$ would indicate the accuracy of the divider at those ratios. As can be seen, these deviations are less than the above 2σ uncertainty estimate.

Finally, the binary divider settings that produce ratios of $n/10$ do not have an obvious correlation with one another, and there is every reason to believe any arbitrary ratio produced should be equally valid. To attempt to verify this point, the divider was also compared with a manually adjusted Kelvin–Varley divider over many decades and on several occasions. Although first-decade ratio discrepancies were occasionally found to be as large as 0.12×10^{-6}, most incremental ratio comparisons showed much smaller discrepancies.

V. CONCLUSION

To fully exploit the self-checking feature of the Cutkosky divider, this paper addresses the problems arising

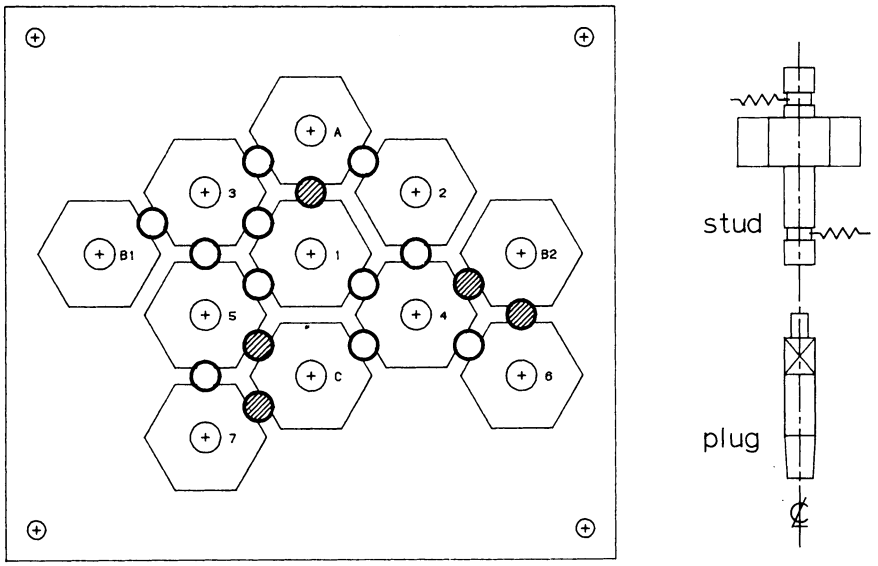

Fig. 4. Copper stud-and-plug arrangement for producing resistance ratios of $n/10$. Six equal resistors are connected between the seven numbered studs. Circles between studs locate rimmed holes to receive up to five shorting plugs. As an example, with plugs inserted into the shaded holes, the ratio R_{BC}/R_{AC} (= 1/10) is accessible through terminals A, B_2, and C.

TABLE III
MEASURED RESISTIVE RATIOS FROM A SIX-ELEMENT (40 kΩ) NETWORK IN A 23.00° C OIL BATH

n	Nominal Ratio	$\frac{n}{10}$	$1-\frac{n}{10}$	Sum
1	(A)	.099 999 298	.900 000 702	1.000 000 000
	(B)	.100 000 712	.899 999 268	0.999 999 980
	(C)	.100 000 005	.899 999 985	
	(D)	-.000 000 005	+.000 000 005	
	(E)	.100 000 000	.899 999 990	
2	(A)	.199 998 295	.800 001 681	0.999 999 976
	(B)	.200 001 744	.799 998 249	0.999 999 993
	(C)	.200 000 020	.799 999 965	
	(D)	-.000 000 008	+.000 000 008	
	(E)	.200 000 012	.799 999 973	
3	(A)	.300 002 031	.699 997 949	0.999 999 980
	(B)	.299 997 934	.700 002 044	0.999 999 978
	(C)	.299 999 982	.699 999 996	
	(D)	-.000 000 012	+.000 000 012	
	(E)	.299 999 970	.700 000 008	
4	(A)	.399 996 234	.600 003 765	0.999 999 999
	(B)	.400 003 753	.599 996 231	0.999 999 984
	(C)	.399 999 994	.599 999 998	
	(D)	-.000 000 006	+.000 000 006	
	(E)	.399 999 988	.600 000 004	
5	(A)	.499 997 605	.500 002 393	0.999 999 998
	(B)	.500 002 393	.499 997 605	0.999 999 998
	(C)	.499 999 999		
	(D)	.000 000 000		
	(E)	.499 999 999		

(A), (B): Measured ratio, dual configurations
(C): Geometric mean of (A) and (B)
(D): Correction for dissipation change in resistors between configurations
(E): Corrected mean ratio

from switch and wiring resistances, as well as from output loading, and offers practical solutions to these problems. It has resulted in an automated 25-bit reference voltage divider system whose ratio corrections and measurement uncertainties arising from identified sources have been carefully examined.

The total uncertainty of this divider system has been given a 2σ estimate of $\pm 0.034 \times 10^{-6}$. An accurate self-checking resistive ratio device has been built and used to verify the proper application of corrections to the divider and the absence of any significant systematic errors.

Through periodic autocalibrations the high accuracy of this reference divider can be reliably maintained, which is obviously an important consideration for standard laboratory applications. This divider has been used in the calibration of 7-decade voltage dividers and solid-state voltage references.

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