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HFC 50 D / E

Dual Cryogenic Ultra Low Noise RF-Amplifier

- Datasheet -

Version 2.38 / 2016

Features:

- **Ultra Low Input Noise (typ. 0.3nV/√Hz @ 10MHz)**
- **Frequency Range 160kHz to 50MHz**
- **Input Impedance approx. 10MOhm**
- **Dual Channel Version with Adjustable Channel matching**
- **Output Impedance 50 Ohm or 75 Ohm**
- **Wide Temperature Range T = 300K down to T = 4.2K**

Typical Setup and Application

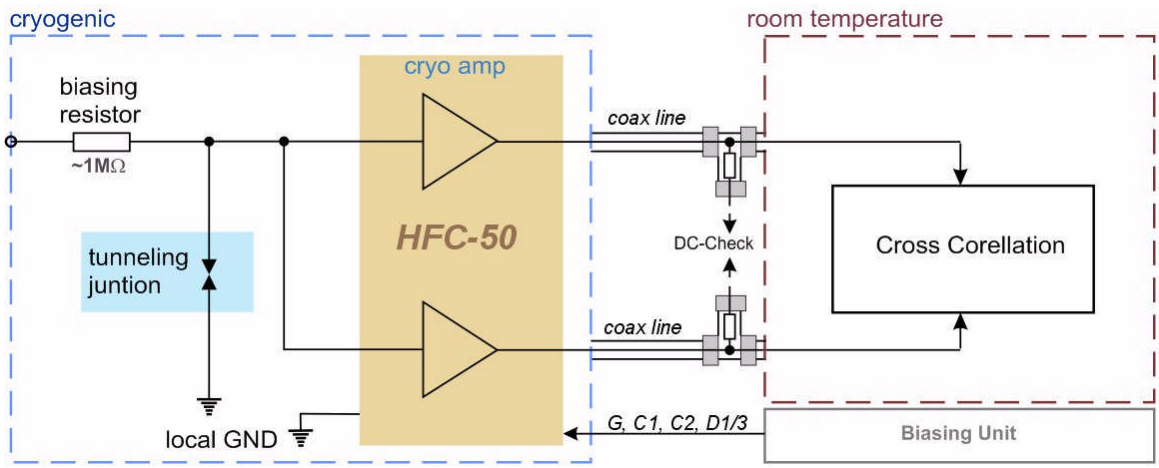


Figure 1:

Typical connection scheme and application: measurements of tunneling currents (e.g. shot noise measurements) in a 4.2K environment at a tunneling junction (e.g. break-junction, QPC, STM-tip).
The cold part is connected to the warm by cryogenic lines, i.e. coaxial cables and DC-Wires. A Biasing unit provides the required DC voltages. At room temperature the signals of interest are further processed, e.g. by a second amplifier and/or a cross correlator.

Introduction

The HFC 50 D/E represents an ultra low noise 2-channel FET preamplifier, operating in room temperature down to deep cryogenic environments (T = 4.2K, liquid Helium). The HFC 50 covers a frequency range from 0.16 to 50MHz (in terms of +/-3dB deviation) and has an exceptionally low input voltage and current noise. It features a very high input impedance of nominally 10MΩ (each channel vs. GND), suited to sense signals originating from sources with very high source resistance, like currents from ion traps or STM/QPC tunneling signals. The output signals appear on corresponding solder pads with inversed polarity referenced to the input in order to obtain high stability.

The device incorporates the latest GaAs (Gallium Arsenide) semiconductor technology, which allows for operation over a very wide temperature range and makes it possible to perform well in strong magnetic fields to B = 7T. Version HFC 50 **E** equals version HFC 50 D, but offers an additional (uncalibrated) silicon temperature diode for temperature monitoring. In comparison to its predecessor HFC 50 C/D the new device offers a substantially improved voltage and current noise floor (< 0.4nV/√Hz, < 20fA/√Hz @1MHz), an outstanding low 1/f noise and improved channel matching.

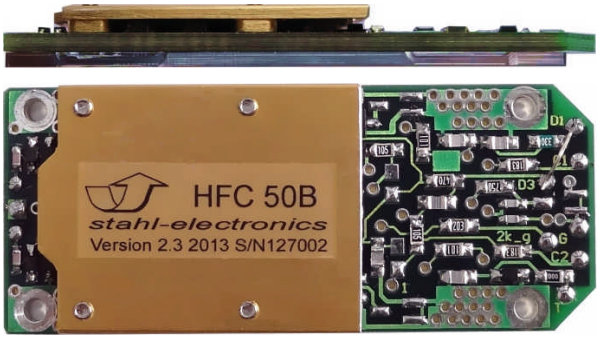


Figure 2: side and top view

Block Diagram

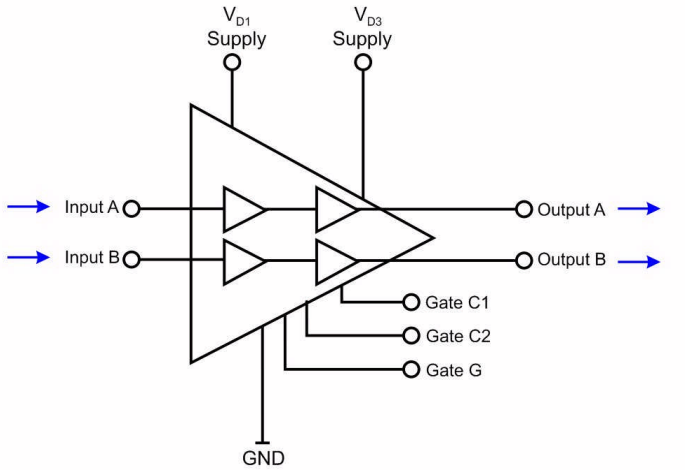


Figure 3: Internal structure of the HFC50 amplifier

Solder Pad Locations

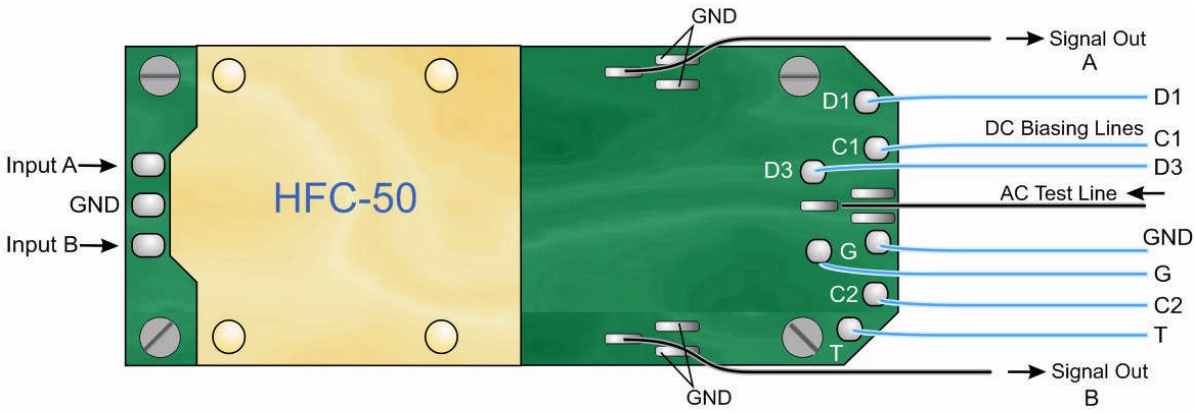


Figure 4: Location of solder pads

Front Side:	Remarks:
Input A	high impedance input
GND	reference GND for input lines
Input B	high impedance input
Rear Side	Remarks:
Signal Out A	AC Output signal, superposed to DC monitoring signal
positive power supply line D1*)	apply typ. +3.5V, draws typically 3mA
biasing line C1	typ. -1V … +1V, draws few µA, may be left open
positive power supply line D3 *)	apply typ. +3.5V, draws typically 1mA
AC Test Line	see text
GND	reference GND for outputs, connects internally to input GND
biasing line G	apply here typ. -5.2V @ 300K, -1.0V to -2.0V at 4.2K, draws few µA, needs adjustment to define biasing
biasing line C2	typ. -1V … +1V, draws few µA, may be left open
Temperature T	internally connected with silicon diode to GND (HFC50E)
Signal Out B	AC Output signal, superposed to DC monitoring signal

***) Note:** D1 and D3 are connected when device is shipped and may be kept connected for most applications.

Case Outline

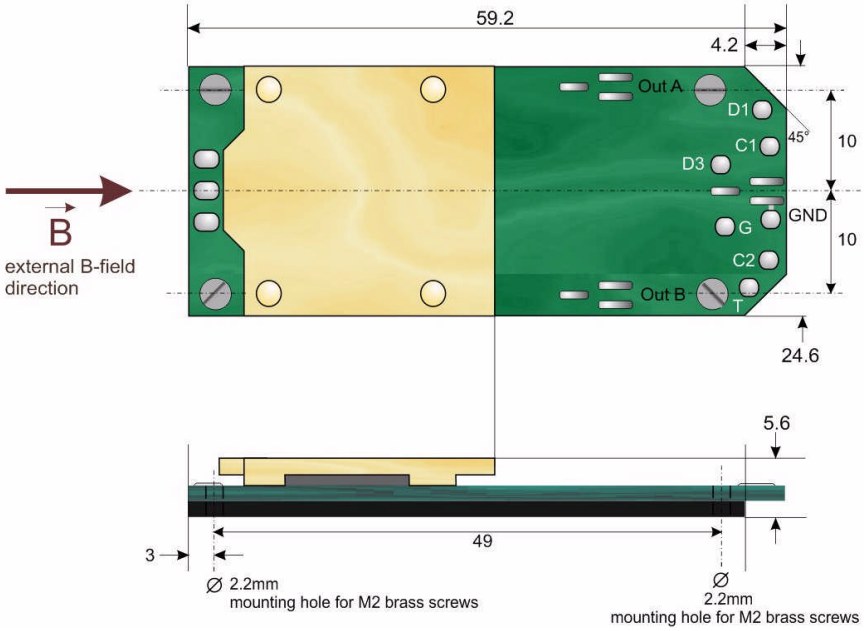


Figure 5: Case dimensions and orientation within external magnetic field. Dimension in Millimeters

Caution: Electrostatic Sensitivity

This device can be damaged by ESD (Electrostatic Discharge), especially the **input and output lines**. It is strongly recommended to handle the device with appropriate precaution. Failure to observe proper handling and installation procedures can cause serious damage. This ESD damage can range from subtle performance degradation to complete device failure.

Practical Hint:
*In case the device is picked up by hand, ensure that the ground pin or aluminium case is touched **first** before touching any other pin. After transportation the destinations ground has to be on the same potential as the devices ground. Therefore connect both grounds first before making any other connection or changing the device position (ground balancing). Whenever the device is moved or electrically connected/disconnected always ensure that the possible ocurring voltages on connector pads stay well below approx. 5V referenced to device GND. Note that failure to comply with proper ESD handling can easily damage the device and voids warranty.*

Absolute Maximum Ratings

Stress above these ratings may cause permanent damage or degradation of device performance. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

Quantity	Limits		Remarks
	min.	max.	
pos. Supply Voltage V_{D1}, V_{D3}	0	+5.0	
neg. Biasing pad G	-6V	0V	
Additional Biasing C1, C2	-3V	+2V	
Input Voltage absolute value AC		10V pk (DC) 0.5Vpp	
Input Current		3mApp	AC current through input
Output Voltage	Under normal conditions no voltage source must be applied to the outputs.		
Storage Temperature, Baking	1 K	125°C	Baking is possible up to 125°C, max. for 24 hours
Temperature changes	-	+/-15 degrees Kelvin per minute	exceeding this temperature slew/fall rate may damage the device due to formation of mechanical cracks
Storage Humidity		65% @ 40°C	

Table 1: Absolute Maximum Ratings

Characteristic Data and Operating Parameters

Note: This device is shipped alternatively with one of two output impedance options, 50 or 75 Ohms, 50 Ohms is the default value.

Parameter	typical Value	Remarks/Conditions
Freq. Range for ±3dB deviation .	160 kHz....50 MHz	output connected to 50 or 75 Ohm load, V_{D1} = V_{D3} = 3.5V to 4.0V amplification plot see fig. 13.
Voltage gain @ f = 1MHz	50Ω output, T = 300K 4.6 V/V 9.3 V/V 75Ω output, T = 300K 5.6 V/V 11.7 V/V 50Ω output, T = 4.2K 14.5 V/V 29.1 V/V 75Ω output, T = 4.2K 17.4 V/V 33.8 V/V	$V_{D1/3}$ = 3.5V; C1 = C2 = 0V; G ≈ -5.0 V at 300K or G ≈ -1.0V at 4.2K*, 50 Ω output load, output unloaded 75 Ω output load, output unloaded 50 Ω output load, output unloaded 75 Ω output load, output unloaded
Gain Polarity	inverting	inverted polarity in favour of increased device stability
Channel gain matching @ T = 3.9K to 12K	untrimmed typ. +/-4% trimmed typ. +/-2%	see also fig. 15 trimming range see fig. 8
Input Impedance vs. GND at either input	10MΩ +/-5 % capacitively coupled to GND	f <= 0.1 MHz
Input Capacitance either input vs. GND	6.2 pF	f_{test} = 2MHz
Output Impedance, max. Output Power	50 Ω or 75 Ω +/-8% (standard option: 50 Ohms) 10mW	f_{test} = 0.1MHz ... 25MHz
Input Noise @ T = 4.2K (each channel) voltage noise density, f = 1MHz current noise density, f = 1MHz	 0.3 nV/√Hz approx. 17 fA/√Hz	 see also fig. 12 a, b
Operating voltages V_{D1}, positive supply voltage 1 V_{D3}, positive supply voltage 3 G, negative supply voltage C1, C2 biasing voltages	 +3.5 V +3.5 V -1.0 V... -5.2V -0.3 … +0.3 V	 T = 300K down to 4.2K Note: biasing being supplied through RC filter, see figure 10, is recommended
Supply Current supply current I_{D1+D3}	5.4mA @ 300K; 3.7mA @ 4.2K	
Temperature Diode (pad T) forward voltage	U_F = 0,70 V , T = 300K 1,8V , T =4.2K	I = 5µA measurement current to GND
Power Consumption	13mW @ 4K … 50K	
General Operating Temperature	T = 4.2 K … 300 K	
External magnetic field	B = 0 … 7T	place the amplifier in parallel with an external B-field, with respect to the long side (see also fig. 5)
Geometrical Size, Weight	25mm x 6mm x 59.2 mm, 15gr.	
Outgassing	(to be determined)	
Remark: This table represents typical values at low magnetic fields B < 2T. Parameters may vary at higher B-fields. * Note: bias voltages brought to amplifier through filter circuitry in figure 10 and adjusted such that DC output voltage equals 0.9V.		

Table 2: Characteristic Data

Voltage Supplies and Operation

To bring the device into basic operation a positive supply voltage (connected to pads D1 and D3) is required as well as a negative biasing voltage (apply to pad G). D1 and D3 may be commonly powered with +3.5V (see (*), depending on serial number) versus GND (they draw a current of approx. 4mA to 5mA together) and pad G with about -5.2V (@300K). See also subsequent diagram for illustration of basic supply circuitry and figure 9. (Please always ensure proper ESD handling (see page 4) whenever changing the device place or wiring attached.)

The device features an internal regulation loop compensating the major part of temperature related and short term drift effects. However, the negative biasing voltage (pad G) should be brought to a value, such that the DC component of both output voltages is at approximately 0.9V (*). A more negative bias at pad G will increase the DC output voltage, a more positive one will lower the latter. If, by voltage adjustment on pad G, the outputs stay at their recommended DC level, a stable operation over a wide temperature range as well as good channel matching is achieved. Normally a DC voltage of approximately -5.2V (@300K) or -1.0V at 4.2K at pad G is required to fulfill the latter condition.In order to monitor the DC output value one may connect a Bias-T to the roomtemperature outputs.

The biasing pads C1 and C2 do not have to be connected for normal operation and may be left open. For fine adjustment of the amplification factor of each channel their voltage may be varied (C1 for channel A, C2 for channel B). Figure 8 shows the influence of C1 or C2 variation on the amplification factor. This feature of slight amplification change may be specially useful in applications where good channel matching is essential, e.g. in experiments using cross-correlation techniques for noise suppression.

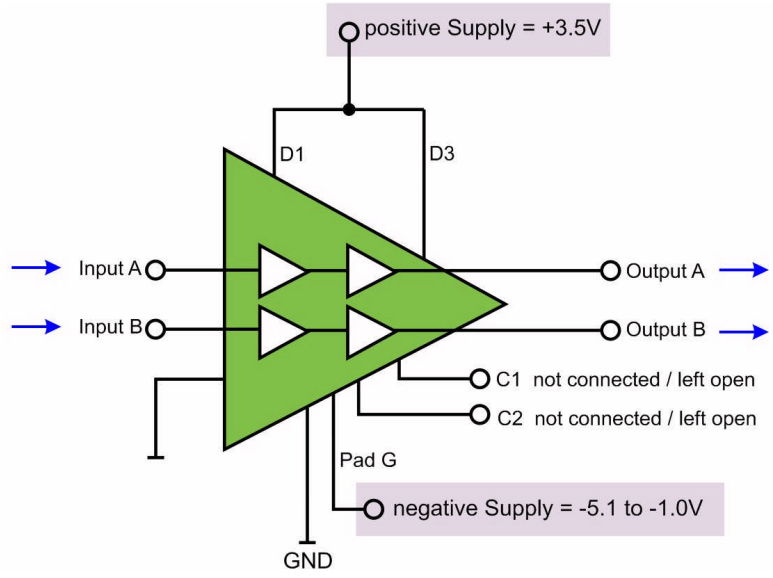


Figure 6: Basic operation requires a positive and a negative supply voltage of +3.5V and -5.1V to -1.0V

Note: The positive supply pads D1 and D3 are by default shipped with a shorting bridge between them. For operation below T = 4.2 K or in order to achieve fine adjustment of noise characteristics, the voltages on pads D1 and D3 may be carefully varied with maximum difference up to 0.8V. Consult manufacturer for further details.

(*): Important Note: due to parameter variations please see also appendix for biasing parameters for certain serial numbers.

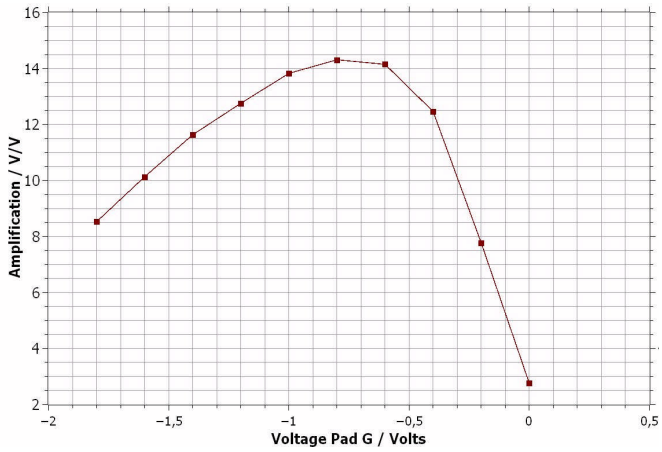


Figure 7: Variation of pad G voltage affects the overall amplification factor (data taken at T = 10K, 50 Ohm termination). Note that the filter circuitry shown in figure 10 was used to apply the biasing voltage.

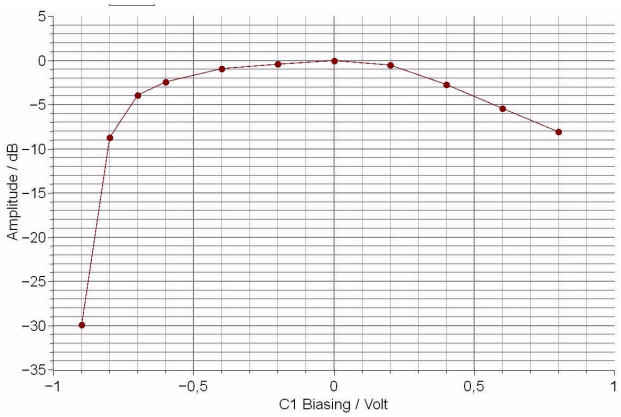


Figure 8: Variation of pad C1 voltage influences the amplification factor (here expressed in dB referenced to the amplification at C1 = 0V). This feature is used for amplification fine-adjustment in cross-correlation applications. If not required, C1 may be left open or connected to GND. C1 influences channel A, correspondingly C2 acts on channel B in the same way.

Automatic Biasing

The device requires a negative Biasing Voltage (Pad/Line G) to establish proper operating conditions, as mentioned before. A way to check correct operation is to regularly check the DC level (e.g. with a standard multimeter) of the 2 outputs, for instance using a bias-T (as indicated in figure 1).

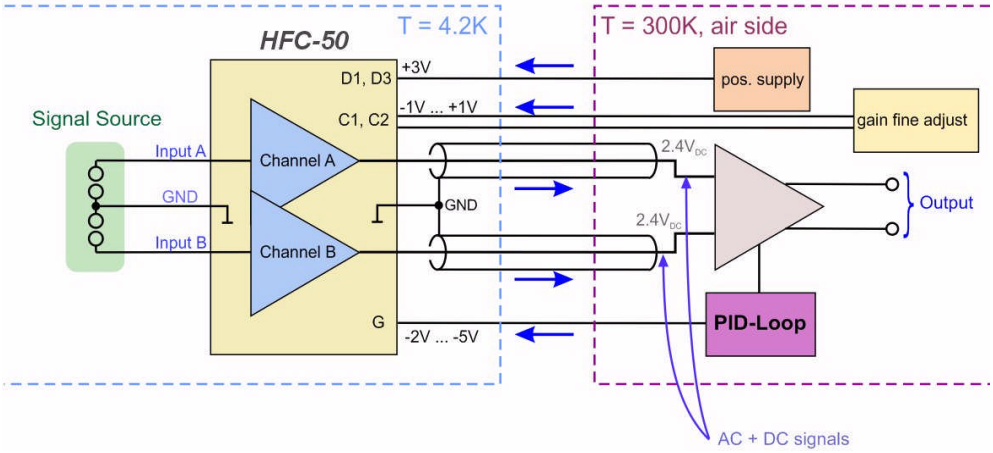


Figure 9:
A PID-regulation loop may be implemented to achieve automatic biasing, i.e. regulation of biasing voltage G. The loop ensures that the DC output levels of both amplifier paths stay at a defined level, e.g. 0.9V_{DC}.

This DC level should be around 0.9V at 4.2K or 1.1V at 300K vs. GND, for each channel and should be readjusted manually by changing the negative bias voltage G in case large temperature changes occur (see also appendix for device-specific values).
Automatic biasing/regulation electronics (e.g. type A3-5b) are also available from the manufacturer of the HFC-50. In this case the DC levels are electronically measured, averaged over the two channels and the biasing voltage G accordingly corrected to keep the DC-output voltage levels constant at the desired value. In case of user-based solutions, a simple I-regulation (P I D without differential and proportional part) will usually suffice to ensure proper automatic regulation. The I-component (e.g. implemeted with a standard operational amplifier) should be around 1 Volt/sec. per 10mV deviation from the set value.

AC Test Line

The device features an additional input which is located at the rear side beside the biasing voltage pads (see also figure 4). This input should be connected with a twisted pair or coaxial line and serves for test purposes. Any RF signal coupled here (75Ω termination resistor) is first attenuated by a factor of 2.43 and then fed to the inputs using a small capacitance of 0.8pF each channel. This capacitance is small enough not to affect seriously device performance when connected to signal sources like ion traps or tunneling junctions, but offers the possibility to permanently check device functionality. E.g. given an (external) input capacitance of 6pF being connected to an input, the overall attenuation (AC Test Line input → signal input) amounts to 1/37, which means that e.g. a 1mV signal at the AC Test Line input will appear as 27µV at the HFC 50 inputs. The internal attenuator is implemented as a broadband circuitry, such that any frequency within the nominal frequency range of 0.3 to 50MHz may be applied.

Bias Filtering and Shielding

Grounding and Shielding at the input and output side are very important issues of concern. A proper grounding and shielding is essential to maintain good device performance and low noise characteristics, and to avoid the creation of parasitic oscillations, which is a common problem to high frequency amplifiers having a high-impedance input. To ensure a “clean” electrical environment, provide good ground connections especially around the amplifier input. All lines from a signal source to the amplifiers inputs should be kept as short as possible. The connections may be implemented as coaxial lines for shielding reasons. Each signal output on the HFC 50 therefore consists of 3 solder pads. The center one is the AC signal line, the outer ones represent AC ground, to be connected to the coaxial shield GND (or: twisted pair GND in case twisted pair lines are used).
Please note that insufficient grounding or shielding around the signal source, which connects to the HFC 50 input, may lead to a considerably increased noise level and furthermore increases the risk of self-oscillations. These uncontrollable oscillations appear typically at frequencies of about 50 to 500 MHz and are often an indication of insufficient shielding or grounding. In case this occurs, a small metal shield (Faraday cage), completely enclosing both signal source and amplifier input will normally remove that problem. This shield should be connected to the input ground pad.

For optimum noise performance the supply lines (providing the biasing voltages on pads G, C1, C2, D1 and D3) should be filtered well and be supplied from a well-stabilized power supply. Blocking capacitors of 100nF from the biasing supply lines to ground may support power supply stabilization.

If the device will be mounted inside a vacuum setup, an appropriate way to minimize unwanted noise is the implementation of a filter bank right before the vacuum feedthroughs, in minimal geometrical distance (e.g. < 5cm). Therefore the vacuum vessel inside may be kept free of disturbing noise interference. The subsequent graph depicts a possible arrangement of a simple and inexpensive RC-low pass filter set, which usually does a good job to establish a noiseless environment. DC supply signals come from the left and should enter the (shielded) vacuum setup right after this filter bank at the right.

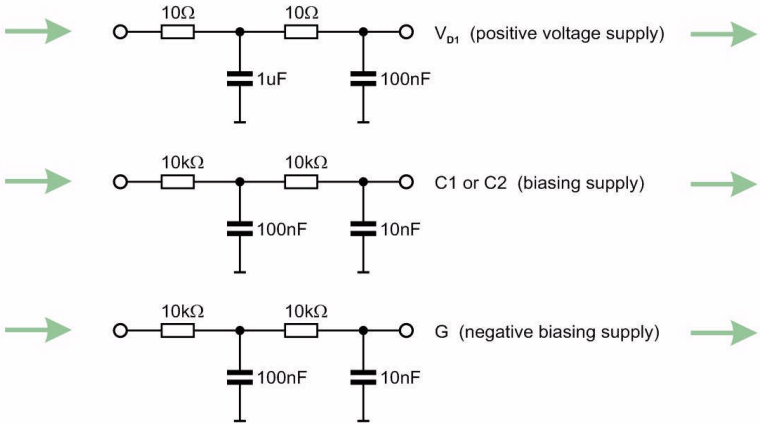


Figure 10: Inexpensive RC filter can establish a low-noise environment. Supply voltages should enter the vacuum setup in which the HFC 50 is mounted through such a filter bank, located directly at the vacuum feedthroughs in close proximity.

Operation in Magnetic Fields

At magnetic fields above approx. 0.5T the internal biasing parameters change with the strength of the external field. However, as long as the direction of the external field is parallel to the long side of the amplifier (see also fig.5, offset < 5°) and an external PID-loop compensates for drifts (variations in amplification factor), the amplification is kept stable on a 5 to 10% level up to approx. B = 6T.

Thermal Anchoring

Mounting the device is possible in a vacuum setup (e.g. cold-head cryostat) whereas immersion into a cryogenic liquid (Nitrogen, Helium) is not recommended (possibility of stability problems). In a vacuum cryostat good thermal coupling to the cold reservoir (cold finger, Helium cryostat cold plate) is recommended to ensure proper operation and low noise. Thermal connection may be established using the mounting screw holes in the base plate of the amplifier, specially using brass screws. Brass metal contracts stronger when getting cold compared to most other metals and printboard substrate, therefore tightening the thermal connection upon being cooled down. Note that a thermally conducting agent like “Apiezon N” grease between the metal pieces of different temperatures also significantly increases the thermal heat flow and should be used (carefullly apply a thin layer of 10µm to 50µm thickness). Use primarily the front side holes for mounting, use rear holes only if there is no access to the front side holes. Attention: **Beware** of bending the amplifier on a non-flat substrate and eventually

only connect the front side holes in case of doubts. Bending the amplifier (in the cold state) can lead to fatal cracks and device failure.

Commissioning in Vacuum or Cryogenic Setup

After wiring the device and mounting into a cryogenic dewar or vacuum chamber (always connect ground lines first for ESD reasons), the device should be checked and eventually powered up with appropriate supply voltages.

Figure 11
Picture showing a wired HFC 50A amplifier. The inputs have been shorted (left side) for testing purposes. The coaxial output lines and biasing lines are visible at the right hand side.

However, *before* power is applied to the device, one should carefully check the cable connections in order to avoid damage or malfunction. With a standard multimeter (DMM) one can perform a quick check of resistances. The following table lists typical terminal values of the HFC 50 lines versus GND.

Line designator or Pad	Resistance vs. GND	Remark
C1	1 MΩ	value only slightly differs over 4K-300K range
C2	1 MΩ	value only slightly differs over 4K-300K range
G	160kΩ to 245 kΩ	value only slightly differs over 4K-300K range
D1 & D3 (connected)	410Ω to 600Ω	value may change from 300K to 4K to some degree (approx. 25%) and depends on the multimeter being used.
AC test Line	75 Ω	value only slightly differs over 4K-300K range
Signal Out A	approx. 35 kΩ	Since the device output features protection diodes, the value shown on a DMM display depends on the measurement current and voltage in resistance measuring mode.
Signal Out B	approx. 35 kΩ	
T	typ. U_F = 0,79V	DMM in diode mode

Table 3: typical resistance values of HFC 50 D / HFC 50 E lines versus GND, measured with standard multimeter.

Cool-Down Procedure and Readjustments

Once mounted inside a vacuum or cryostat setup, it is recommended to re-check the cabling (using a multimeter in Ω-Mode, table above) as mentioned before. In case the latter is correct, one may power-up the device. A typical consumption current of 5.4mA at room temperature will be drawn from (joined) D1 and D3 pads as positive supply current. The biasing currents on G, C1 and C2 are minor and only in the µA range. Subsequently adjust the voltage on G such that a DC-output voltage of 1.1V (room temperature, later 0.9V at 4.2K) is measured on the output lines (see also appendix for device-specific values).

Apart from an eventual fine adjustment on C1 and C2 in certain cases (vary these voltages around zero or leave open) the device is now operational. A test signal may be applied through the test line input, in case the latter had been wired up. During cool down in a cryostat or during the pumping process in a vacuum vessel one may from time to time recheck the resistance of lines (as described

above), or once the device is powered up monitor the DC output value of each channel since the latter represent an important measure of the device functionality. In general the device is operational over the complete range from 300K to 4.2K, however at temperatures between 150K and 80K the device is in a transitional state with potentially unstable DC biasing conditions. Therefore it is rather recommended not to operate the device within the temperature range mentioned above. During cool down phases below 150K it is safer to avoid applying any power, this also includes the voltages on G, C1 and C2.

During cool-down/warm-up procedures always maintain a temperature rise or decrease of no more than +/-15 degrees Kelvin per minute. Note that exceeding this temperature slew/fall rate may damage the device due to formation of mechanical cracks. **Never apply thermal shocks to the device, like dipping it into an cryogenic liquid**.

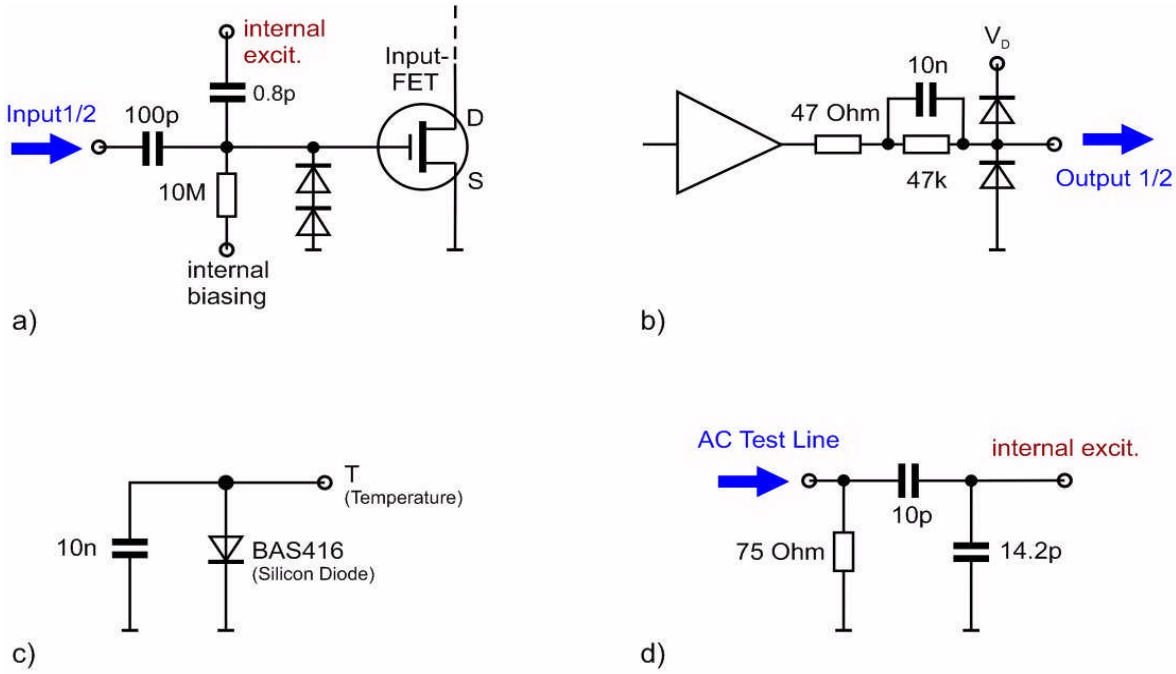
Adjustment after Cool-Down

Once the final desired operating temperature is reached one may re-check lines again, power-up the device and determine the DC voltages on the output lines. They should reside at approx. 0.9V (if voltages on D1 and D3 are set to 3.5V) each output, and may be brought back to this value by changes on the pad G biasing (see also appendix for device-specific parameter values).

Note, that thermal anchoring has considerable influence on biasing conditions. In case of a poor thermal connection, any change on the biasing voltages may take up to a few seconds to settle the new operating point.

Remark: The manufacturer offers biasing regulation circuitry (e.g. device A3-7), which frees the user widely from any adjustments. Please refer to corresponding datasheet.

Input/Output Circuit Details



The diagrams above depict details of the internal input/output circuitry.

Section a) is a simplified diagram of the front-end input, showing the implementation of AC signal coupling and protection circuitry, b) shows the output circuitry (preserving DC and AC information), c) depicts the temperature sensor and d) the AC Test Line circuitry, intended for testing the two amplifier channels when already mounted in the final target application.

Typical Performance Data:

Input Noise

- Voltage Noise density

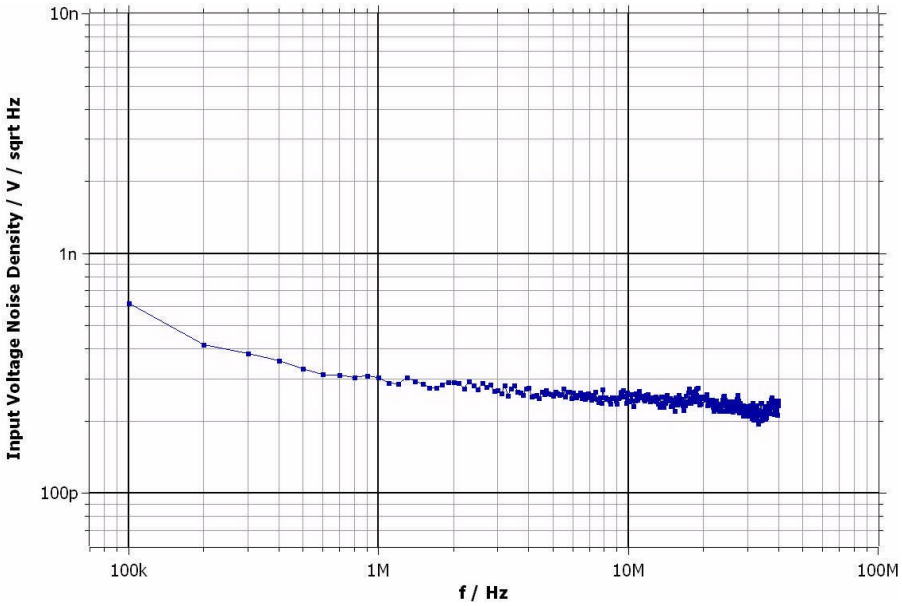


Figure 12a: Input voltage noise density (V/sqrt Hz) at T = 4.2K , measured in a vacuum cryostat. Operating parameters: $V_{D1/3}$ = +3.5V, C1=C2 = 0V

- Current Noise density

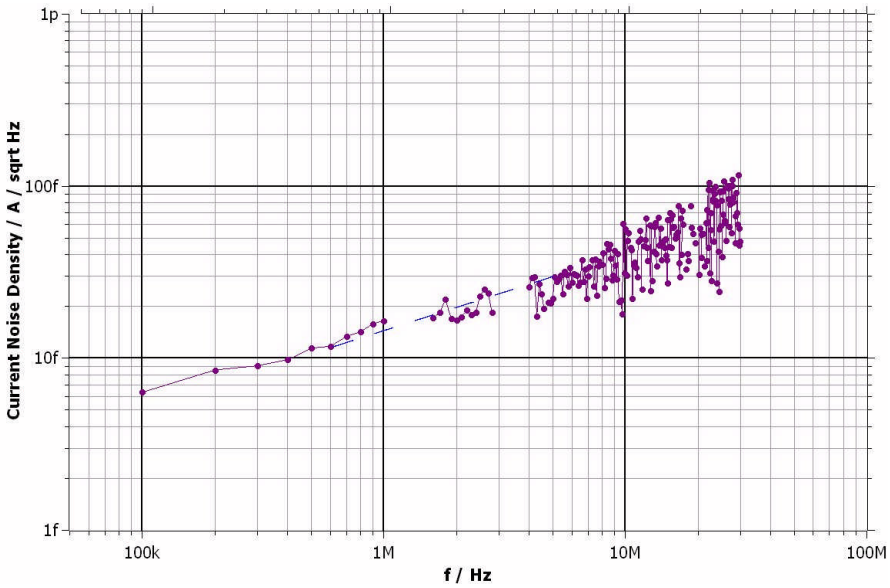


Figure 12b: Input current noise density (A/sqrt Hz) at T = 9.1K , measured in a vacuum test cryostat, inputs left open and shielded.
Operating parameters: $V_{D1/3}$ = +3.5V, C1=C2 = 0V

Amplification Frequency Response

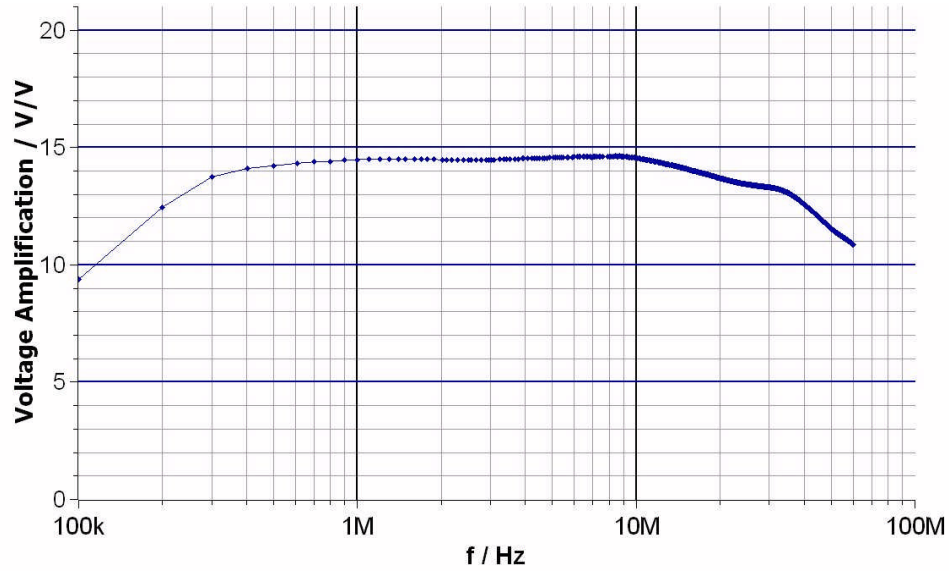


Figure. 13: amplification in V/V (50 Ohm terminated) versus frequency at T = 4.2K, 50Ω output version. Operating parameters: $V_{D1/3}$ = +3.5V, C1=C2 = 0V

Amplification Mismatch (uncorrected)

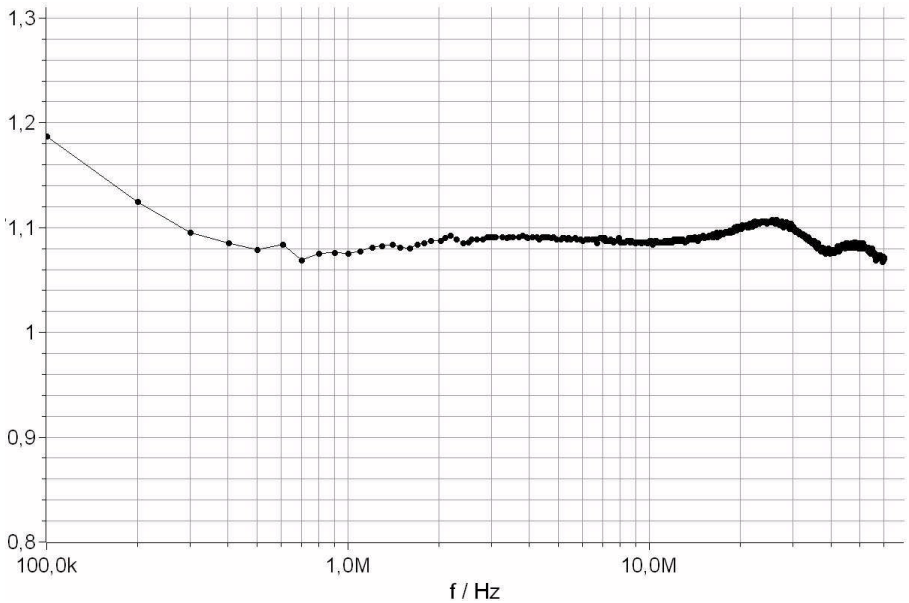


Figure 15: Typical ratio of amplification factor, channel 1 to channel 2, as function of frequency. Operating parameters: $V_{D1/3}$ = +3.0V, C1=C2 = 0V, channels were not trimmed to match. T = 4.2K. Mismatch can be reduced by trimming (change of C1, C2) to about 1 to 2 %, see text.

Appendix:

Nominal values for positive suppy V_{D1}, V_{D3} biasing G and DC outputs

Device Serial Number (batch 2015, 2016)	$V_{D1} = V_{D3}$	G (@ 4.2K to 15K)	DC-Output Voltage
127011	3.0 to 3.5 V	-1.0 V	0.9 V
127012	3.5 V	-1.0 V	0.9 V
127013	4.0 V	-1.5 V	1.6 V
127014	4.0 V	-1.5 V	1.6 V

Note that for proper operation the DC-Output values are important, G may be adapted accordingly.

Photograph of mounted amplifier

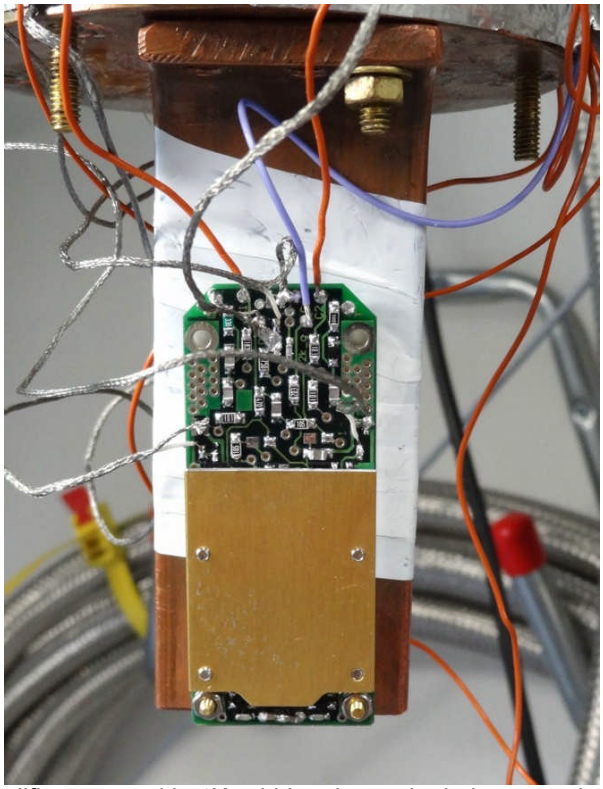


Figure 16: Photograph of amplifier mounted in 4K cold-head cryo rig during commissioning phase.