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(54) VOLTAGE CLAMP

(57) A voltage clamp circuit (200) which operates using a voltage controlled current source (I0) where the change of the polarity of the voltage controlled current source controls whether it is clamping or not. While clamping, the stability of the control loop uses the capacitance of the output (C1) to create and single pole roll-off of the loop gain and while not clamping, uses the capacitance (C2) of the circuit which sets the clamping voltage to produce the roll-off. The circuit operates in a linear fashion both while clamping and not clamping, which allows for a faster response when clamping is needed.

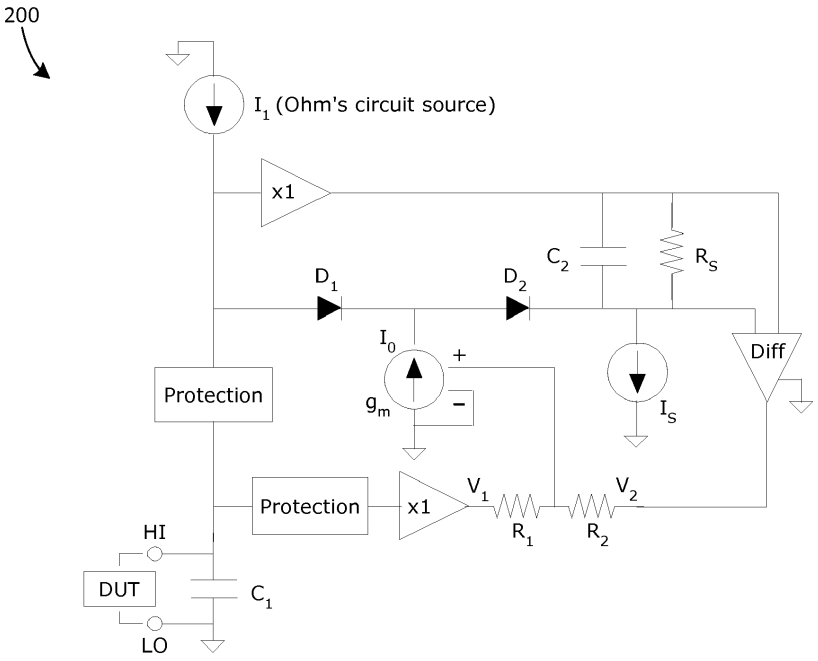

FIG. 2

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Description

Technical Field

[0001] This disclosure relates generally to voltage clamps and, more particularly, to voltage clamps designed for dry circuit ohms clamping.

Brief Description of the Drawings

[0002]

FIGURE 1 illustrates an example of a loop concept circuit on which certain voltage clamp design embodiments in accordance with the disclosed technology are based.

FIGURE 2 is a block diagram illustrating an example of a voltage clamp circuit coupled with a device under test (DUT) in accordance with certain embodiments of the disclosed technology.

FIGURE 3 is a block diagram illustrating an alternative example of a voltage clamp circuit coupled with a DUT in accordance with certain embodiments of the disclosed technology.

Detailed Description

[0003] Dry circuit resistance generally requires a sourcing circuit that limits the maximum applied voltage across the device under test (DUT) to less than a few tens of millivolts (e.g., 20mV to 30mV). This is typically needed to prevent the breaking down of a thin oxide that can form on electrical contacts within the DUT, such as a relay contact or a contact within a connector pair.

[0004] Embodiments of the disclosed technology are generally directed to a circuit having a maximum voltage limit and a maximum current limit. The circuit may include a first current source configured to drive the output of the circuit (i.e., by setting the maximum current) and a second current source having a polarity that is opposite the polarity of the first current source, and is coupled with a resistance.

[0005] A voltage-controlled current source may be configured to, when its current has a polarity opposite that of the first current source, remove current from the output and, when its current has a polarity that is opposite that of the second current source, remove current from the node common to the second current source and the resistance, thus reducing the current through the resistance.

[0006] The circuit may include a component configured to compare the output voltage to the voltage across the resistance and drive the voltage controlled current source's input such that there is a negative feedback.

[0007] The circuit may include a first capacitance added to the output of the circuit to provide a single pole roll off of the output voltage from the input to the voltage controlled current source. The circuit may also include a second capacitance added across the resistance to provide a single pole roll off of the voltage across the resistance from the input to the voltage controlled current source.

[0008] FIGURE 1 illustrates an example of a loop concept circuit 100 on which certain voltage clamp design embodiments in accordance with the disclosed technology are based. In the example 100, a capacitor C causes a 20dB/dec roll-off where $\frac{g_m}{C}$ represents the gain-bandwidth of the circuit. The current source g_m should have a constant gain for frequencies less than or equal to $\frac{g_m}{C}$.

[0009] FIGURE 2 is a block diagram illustrating an example of a voltage clamp circuit 200 coupled with a DUT in accordance with certain embodiments of the disclosed technology. In the example, a current source I_0 is steered by the two diodes D_1 and D_2 to regulate the voltage on one of two capacitors C_1 or C_2. When the I_0 current is negative, the Ohm's current source I_1 is diverted through the first diode D_1, thus reducing the current flowing to the HI connection.

[0010] When the I_0 current is positive, however, the I_S current source is supplied through the second diode D_2, thus reducing the current flowing through a source resistor R_S. The loop circuit 200 generally either regulates $\frac{V_1}{R_1}$ to be equal to $\frac{-V_2}{R_2}$ (i.e., with the first diode D_1 conducting) or regulates $\frac{V_2}{R_2}$ to be equal to $\frac{-V_1}{R_1}$ (i.e., with the second diode D_2 conducting).

[0011] In the example 200, a voltage V_1 may be clamped to $\frac{R_1}{R_2} R_S I_S$. Thus, $\frac{R_1}{R_2} R_S I_S$ generally needs to be set between 20mV and 30mV to meet the needs for dry circuit testing. The loop bandwidth is $\frac{g_m}{C_1}$ when D_1 is conducting and switches to $\frac{g_m}{C_2}$ when D_2 is conducting.

[0012] The ohm's current source protection will generally drop voltage when current is flowing through it. Therefore, the capacitor C_2 and source resistor Rs may be bootstrapped to follow the ohm's current source's voltage. This advantageously prevents both of the diodes D_1 and D_2 from turning on at the same time. A differential stage, Diff, may be used to translate the voltage across the source resistor Rs to ground to be mixed against the voltage V_1.

[0013] In the example 200, the first capacitor C_1 is used to limit the rate that the voltage V_1 rises when a conduction path (e.g., the DUT) between the HI and LO connections is suddenly removed, e.g., to minimize the over-

shoot. Using the capacitance-g_m interaction to control stability generally avoids problems that the capacitance may present in situations where a normal voltage source loop is used.

[0014] FIGURE 3 is a block diagram illustrating an alternative example of a voltage clamp circuit 300 coupled with a DUT in accordance with certain embodiments of the disclosed technology. In the example 300, the clamp voltage for V_1 is $I_S * R_S$.

[0015] Examples provide a voltage clamp circuit, comprising a first current source configured to drive an output of the circuit, the first current source having a polarity, a second current source coupled with a resistance, the second current source having a polarity that is opposite the polarity of the first current source, a voltage-controlled current source having a polarity and configured to, when its polarity is opposite that of the first current source, remove current from the output and, when its polarity is opposite that of the second current source, remove current from a node common to the second current source and the resistance, a first capacitance coupled with the output, and a second capacitance coupled across the resistance.

[0016] Some examples further comprise a component configured to compare the output voltage to the voltage across the resistance.

[0017] In some examples the component is further configured to drive an input of the voltage-controlled current source such than there is a negative feedback.

[0018] In some examples the first current source is configured to drive the output of the circuit by setting a maximum current.

[0019] In some examples the first capacitance is configured to provide a single pole roll off of the output voltage from the input to the voltage-controlled current source.

[0020] In some examples the second capacitance is configured to provide a single pole roll off of the voltage across the resistance from input to the voltage controlled current source.

[0021] Having described and illustrated the principles of the invention with reference to illustrated embodiments, it will be recognized that the illustrated embodiments may be modified in arrangement and detail without departing from such principles, and may be combined in any desired manner. And although the foregoing discussion has focused on particular embodiments, other configurations are contemplated.

[0022] In particular, even though expressions such as "according to an embodiment of the invention" or the like are used herein, these phrases are meant to generally reference embodiment possibilities, and are not intended to limit the invention to particular embodiment configurations. As used herein, these terms may reference the same or different embodiments that are combinable into other embodiments.

Claims

1. A voltage clamp circuit, comprising:

   a first current source configured to drive an output of the circuit, the first current source having a polarity;
   a second current source coupled with a resistance, the second current source having a polarity that is opposite the polarity of the first current source;
   a voltage-controlled current source having a polarity and configured to:

      when its polarity is opposite that of the first current source, remove current from the output; and
      when its polarity is opposite that of the second current source, remove current from a node common to the second current source and the resistance;

   a first capacitance coupled with the output; and
   a second capacitance coupled across the resistance.

2. The circuit of claim 1, further comprising a component configured to compare the output voltage to the voltage across the resistance.

3. The circuit of claim 2, wherein the component is further configured to drive an input of the voltage-controlled current source such than there is a negative feedback.

4. The circuit of any previous claim, wherein the first current source is configured to drive the output of the circuit by setting a maximum current.

5. The circuit of any previous claim, wherein the first capacitance is configured to provide a single pole roll off of the output voltage from the input to the voltage-controlled current source.

6. The circuit of any of claims 1 to 4, wherein the second capacitance is configured to provide a single pole roll off of the voltage across the resistance from input to the voltage controlled current source.

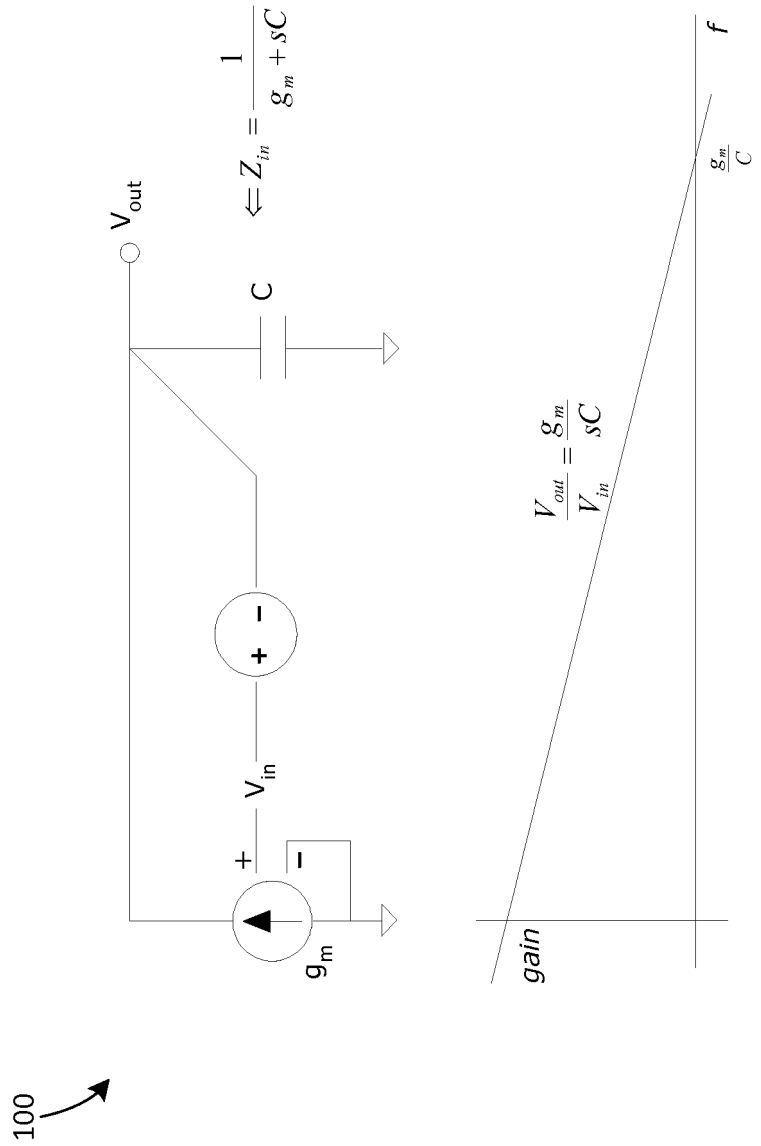
100
V_{out}
$\Leftarrow Z_{in} = \frac{1}{g_m + sC}$
C
+
-
V_{in}
+
-
g_m
$\frac{V_{out}}{V_{in}} = \frac{g_m}{sC}$
gain
f
$\frac{g_m}{C}$

FIG. 1

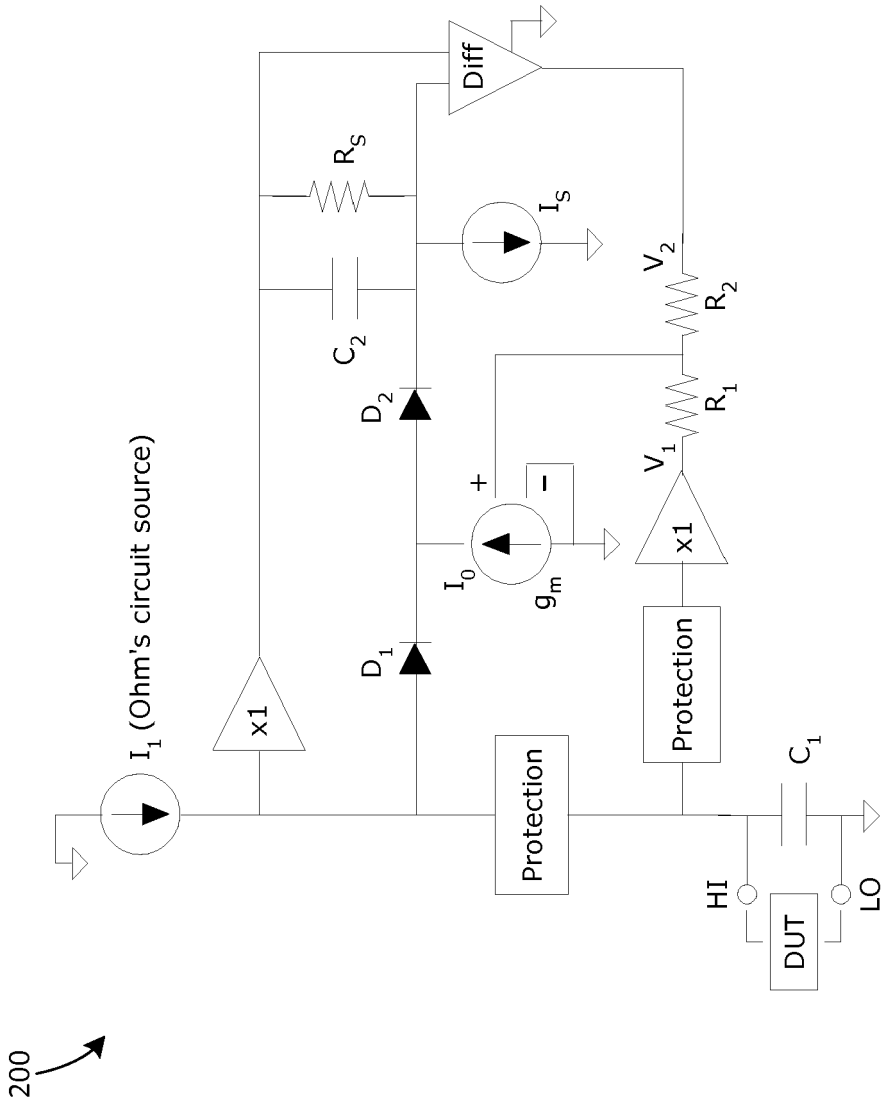
200
I1 (Ohm's circuit source)
x1
Diff
RS
IS
C2
D2
D1
+
−
I0
gm
V1
x1
V2
R2
R1
Protection
Protection
C1
HI
LO
DUT

FIG. 2

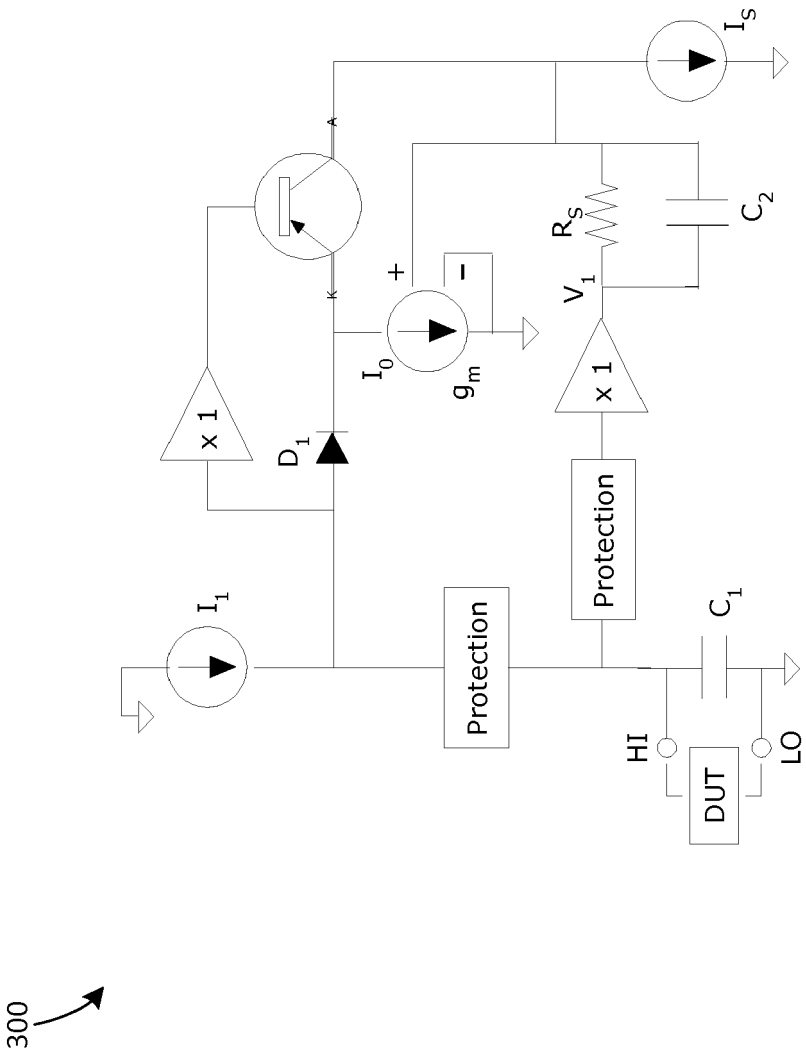
300
I_S
R_S
C_2
V_1
+
−
I_0
g_m
x 1
D_1
x 1
Protection
I_1
Protection
C_1
HI
DUT
LO

FIG. 3

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EUROPEAN SEARCH REPORT

Application Number
EP 15 19 5715

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	15 April 2016	Meliani, Chafik

CATEGORY OF CITED DOCUMENTS

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EPO FORM 1503 03.82 (P04C01)

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